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Experimental performance analysis of a CMOS amplifier considering different layout techniques

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Abstract In order to obtain high-performance systems on chip (SoC) using complementary metal oxide semiconductor (CMOS) technology is necessary to increase the robustness and decrease the delay, power consumption, and surface area of the integrated circuits. We present an experimental performance analysis of a class AB CMOS amplifier designed with different layout techniques (serpentine, concentric, and interdigitated). These layout techniques are evaluated in function of product potency delay area and amplifier characteristics such as electrical gain, common mode rejection ratio, power supply rejection ratio, offset, and slew rate. Based on the experimental performance results of the class AB CMOS amplifier, serpentine technique reduces its surface area to 64 %, and decreases the power consumption close to 39 % with respect to the conventional technique. In the SoC design, serpentine layout technique could be used to improve the electrical performance of their CMOS amplifiers.

Keywords CMOS amplifier · Integrated circuits · Layout techniques · Systems on chip

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1 Introduction

Recent advances of submicron technologies to fabricate integrated circuits (ICs) have allowed the development of systems on chip (SoC), which can have millions of transistors with optimal performance characteristics such as integration density, speed, and power consumption [1, 2]. However, the high power consumption of these systems reduces the batteries lifetime, which affects the progress of more complex systems based on IC. In order to reduce this power consumption is necessary the application of new layout techniques with different levels of abstraction during the IC design such as algorithm, architecture, circuit, layout and technology. In particular, the geometric aspect (layout) of the electronic components of a SoC represents a decisive factor to determine the performance of electronics circuits, in particular the analog circuits [3]. Layout design of electronic components must consider the trade-off existing between their power consumption and surface area without affect the operating characteristics of the electronic circuits. Generally, the ICs (analog, digital or mixed-mode) require optimization of their main characteristics such as surface area, speed, power consumption, and immunity to electronic noise [4, 5]. In order to evaluate different layout techniques, we present the experimental performance analysis of two-stage amplifiers designed with three layout techniques (serpentine, concentric, and interdigitated). These techniques optimize several amplifier characteristics such as integration density, power consumption, gain, power supply rejection ratio (PSRR), common mode rejection ratio (CMRR) and slew rate (SR). The proposed amplifiers are fabricated using a 0.6 μm complementary metal oxide semiconductor (CMOS) technology, which uses three metal and two poly layers.

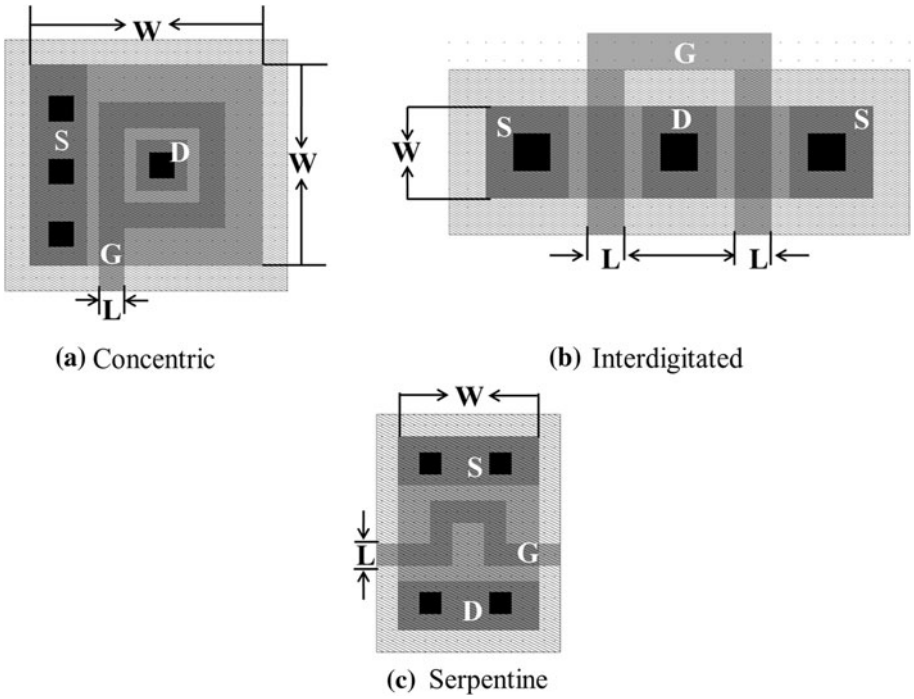

Fig. 1 Layout styles used in this work: **a** concentric, **b** interdigitated, and **c** serpentine

After the introduction, the paper is organized as follows. Section 2 presents the characteristics of the different layout techniques proposed to design a class AB CMOS amplifier. Section 3 reports the geometrical and electrical parameters of the class AB CMOS amplifier design. Section 4 indicates the electrical performance results of the class AB CMOS amplifier. The paper ends with the conclusions and proposal for further work.

2 Proposed layout techniques

Several layout techniques for analog, digital and mixed-mode ICs have been designed to reduce the parasitic elements of different devices. This characteristic is important for the design of high performance circuits, which present low power consumption, reduced delay, and high immunity to electronic noise. In this work, we designed an IC layout considering three layout techniques to obtain high performance circuits: concentric or enclosed form [6, 7], interdigitated or comb [8], and serpentine [9]. In addition, a conventional technique will be used to compare its results with those of the three proposed techniques. Figure 1 shows the three layout considered in this work: (a) concentric, (b) interdigitated, and (c) serpentine.

Metal-oxide semiconductor field-effect transistors (MOSFETs) with concentric or enclosed layouts are used in high radiation environments. They must tolerate these environments and operate with high of drain-to-source leakage current due to turn-on of parasitic transistors [10, 11]. On the other hand, the interdigitated or comb layout is the most attractive layout technique used in the design of analog ICs. Generally, the interdigitated layout is used to reduce the drain/source capacitance and the gate resistance of MOSFETs [12]. Other layout technique is the serpentine, which is attractive in designs with very long channels [12]. In addition, this layout technique can decrease the device-design size using polysilicon lines into a serpentine pattern [13]. This technique is widely used to improve the electrostatic-discharge (ESD) protection capabilities of a MOSFET [14].

The parasitic capacitances affect strongly the ICs performance. Due to this, they must be studied in the ICs design stage to decrease their negative effect on the ICs performance. These capacitances depend of the fabrication technology as well as the topology and distribution of the elements in the ICs design. In the metal oxide semiconductor (MOS) circuits, the capacitance in a determined signal node (C_L) can be obtained by the sum of three components: output capacitance (self-load) of the driver (C_{out}), interconnection capacitance (C_{int}) and input capacitance (load) of the driver circuit (C_{in}). Thus, C_L is obtained as [15]:

$$C_L = C_{in} + C_{int} + C_{out} \quad (1)$$

The input capacitance per unit area of a CMOS gate (C_{in}) and interconnection capacitance per unit length (C_{int}) can be determined as:

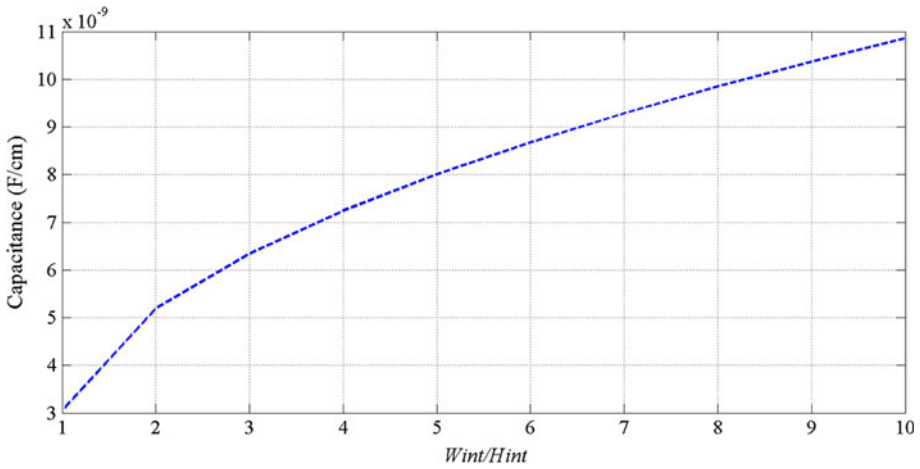

Fig. 2 Interconnection capacitance of a CMOS circuit

$$C_{in} = \left(\frac{\varepsilon_{ox}}{t_{ox}}\right)\left(\sum W_n + \sum W_p\right)L_{min} \tag{2}$$

$$C_{int} = \varepsilon_{ox}\left\{\frac{W_{int}}{t_{ox}} - \frac{H_{int}}{2t_{ox}} + \frac{2\pi}{\ln\left[1 + \frac{2t_{ox}}{H_{int}}\left(1 + \sqrt{1 + \frac{H_{int}}{t_{ox}}}\right)\right]}\right\} \tag{3}$$

where ε_{ox} and t_{ox} are the silicon dioxide permittivity and thickness, respectively; W_n and W_p are the overall width of all the connected transistors, which form the gate and the input node. $L_{mín}$ is the minimum length of the channel, H_{int} is the interconnection length and W_{int} is the interconnection width. Based on Eq. (2), the input capacitance of the gate is not a function of the layout style. Similarly, interconnection capacitance depends of the geometrical parameters W_{int}, H_{int} and t_{ox}. This interconnection capacitance decreases when these three parameters have the same magnitudes, as is shown in Fig. 2.

The output capacitance (C_{out}) of a MOS transistor is caused by diffusion capacitances (C_d) of the transistors, which depend of source and drain surface areas. This diffusion capacitance is given by [16]:

$$C_d = C_{jd}A_d + C_{jsw}P_d \tag{4}$$

where C_{jd} and C_{jsw} are the junction capacitances per unit area and periphery capacitances per unit length, respectively. The values of these capacitances depend by the proposed technology parameters. In addition, A_d and P_d are the drain area and perimeter, respectively.

Figure 3 shows the layout of a MOS transistor using the conventional technique. In this technique, λ is the scaling factor associated to the fabrication process. Generally, the scaling factor magnitude is the half of the minimum geometrical dimension that allows the fabrication process. The drain or source length and transistor width are defined by m and n, respectively. Based on Fig. 3, area ($A_{s,d}$) and perimeter ($P_{s,d}$) of source and drain are obtained as:

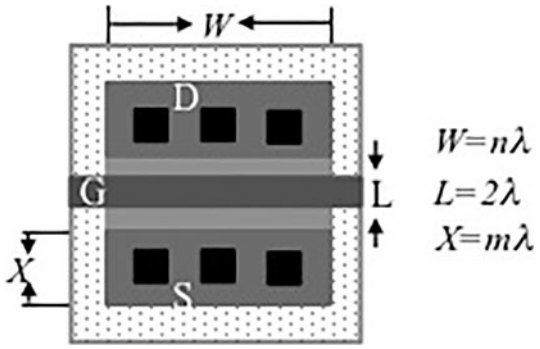

Fig. 3 Conventional layout style used as reference layout in this work

Table 1 Area and perimeter of the MOS transistor drain and source obtained with different layout techniques

Technique	W/L (μm)	A_d (μm^2)	A_s (μm^2)	P_d (μm)	P_s (μm)
Conventional	24/1.2	36	36	27	27
Concentric	24/1.2	22	33	35	48
Interdigitated	24/1.2	36	21.2	18	54
Serpentine	24/1.2	23.5	25	13	20

$$A_d = A_s = WX = \lambda^2(mn) \tag{5a}$$

$$P_d = P_s = 2(W + X) = 2\lambda(m + n) \tag{5b}$$

The designer can improve the circuit performance modifying the transistors area and perimeter, which changes the values of the parasitic capacitances. Table 1 shows the values of the areas and perimeters of the MOS transistor drain and source used in the proposed layout techniques.

In the submicrometric ICs design, an important parameter is the reduction of IC effective area, which allows a larger number of devices per chip. In addition, it decreases the parasitic capacitances of the devices. For this case, diffusion capacitance is the dominant capacitance at any node of the circuit.

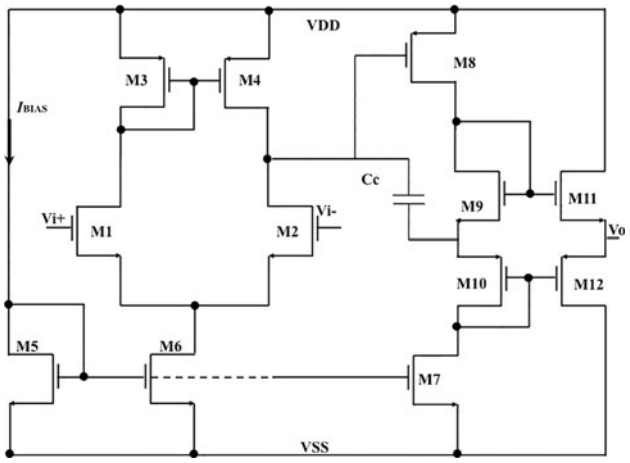

Fig. 4 Schematic diagram of a class AB CMOS amplifier

Table 2 Dimensions of a transistors used in the class AB CMOS amplifier

Transistor	*W/L* (μm)
M1-M2	7.2/1.2
M3-M4	16.8/1.2
M5-M7	4.8/1.2
M8	33.6/1.2
M9	24/1.2
M10	74/1.2
M11	360/1.2
M12	1,197/1.2

3 Amplifier layout design

In this section, we present the layout design of a class AB CMOS amplifier to evaluate the efficiency of the different layout techniques presented in this work.

3.1 Amplifier configuration

Figure 4 shows the schematic diagram of a class AB CMOS amplifier. The amplifier design details on the follows:

(a) All the amplifier geometric patterns have been generated using the minimum dimension that allows the design rules of ON Semiconductor technology [17]. Thus, parasitic capacitances in the relevant nodes can be reduced.

(b) For all the layout techniques were used the same transistors size and values for the load elements (capacitances and resistances) as well as the same input signal and operating frequency. The size of the transistors M11 and M12 were designed to handle the load and connect them to an output terminal (PAD). Table 2 indicates the transistors dimensions of the class AB amplifier.

(c) The parasitic elements of the circuits are extracted using the Virtuoso tool *Extracted* (CADENCE®). It can predict the transistors and circuits performance of the proposed amplifier before of its fabrication.

(d) The CMOS amplifier layout model uses the technological parameters of the 0.6 μm process of ON Semiconductor technology and the model of BSIM3v3.3 transistors [18, 19].

(e) The preliminary test of the electrical performance characteristics of the class AB CMOS amplifier is made to obtain some electrical parameters such as gain, offset, power consumption, SR, CMRR, PSRR.

4 Results

This section reports the electrical characteristics of the designed amplifiers using the serpentine, concentric, and interdigitated techniques.

Figure 5 shows the experimental setup for the electrical characterization of the designed CMOS amplifier.

Figures 6, 7, 8 show the layout and microphotograph of the fabricated op amps considering the serpentine, concentric, and interdigitated techniques. The complete area of the circuits includes the P-and N transistors surface area, as well as the input, output, and power supply lines. These microphotographs are obtained using a Leitz orthoplan microscope [20].

Table 3 indicates the main electrical characteristics of the designed amplifiers. The experimental electrical characteristics of the class AB CMOS amplifier circuit are made using an arbitrary waveform generator (Agilent® 33220A) and a digital oscilloscope (Tektronix® DPO2014). A sinusoidal excitation signal of 1 mV peak to peak at 1 kHz is supplied to the amplifier and its output signal is amplified more than 1,000 times (60 dB), as shown Fig. 8. In order to measure the cutoff frequency of the amplifier, a frequency sweep for the input signal from 0.5 Hz to 1.5 MHz were applied. Figure 9 shows the output signal of the three class AB CMOS amplifiers designed through the serpentine, concentric, and interdigitated techniques (Fig. 10).

Table 3 indicates the electrical characteristics of the CMOS amplifier designed with the three proposed layout techniques. The smallest area of the amplifier circuits is obtained using the serpentine technique. For the three layout techniques, the input capacitance is approximately equal in each designed circuit. However, the capacitance difference between the designed circuits is caused by the polysilicon lines out located to the active area of the transistors. Therefore, input capacitance of the amplifier circuits, determined by the width and length ratio of the

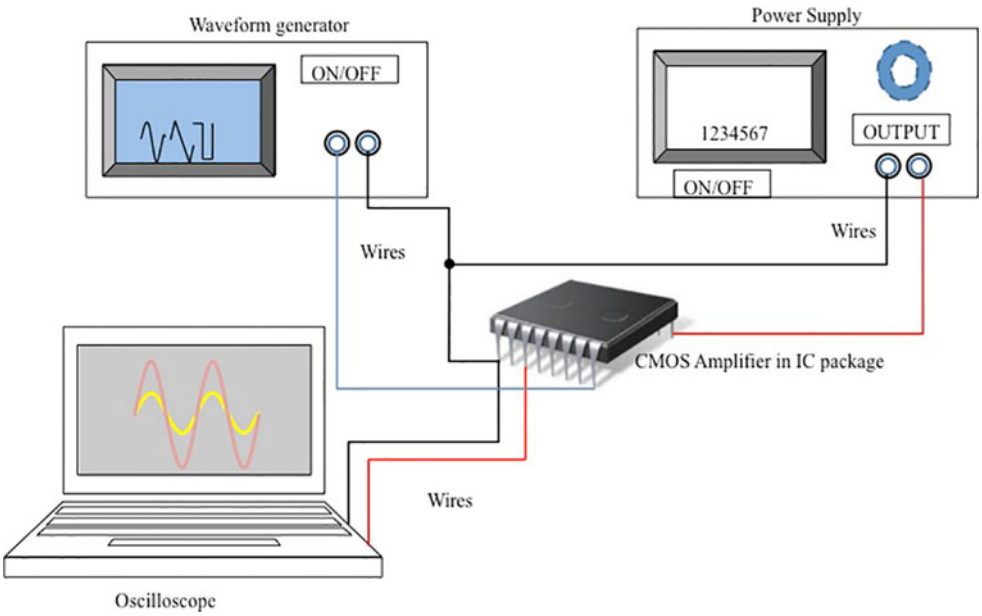

Fig. 5 Experimental setup for the electrical characterization of the class AB CMOS amplifier

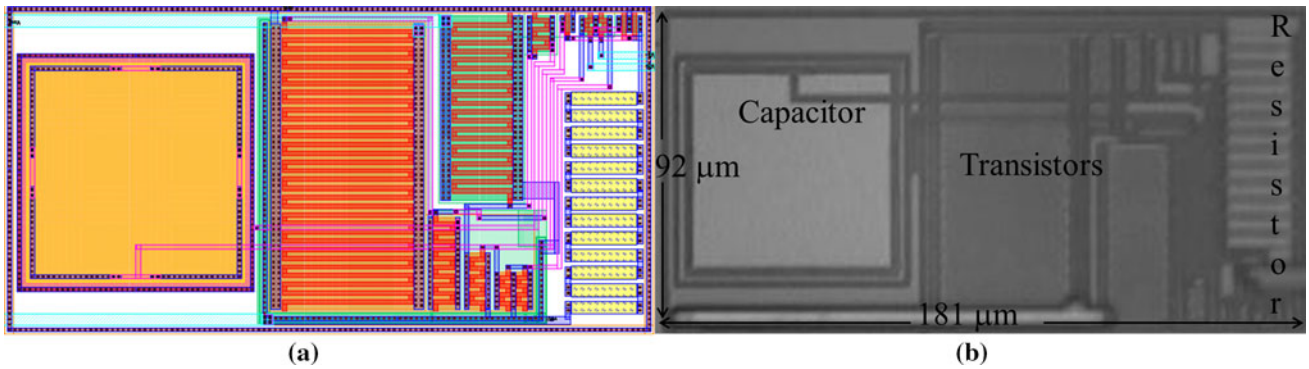

Fig. 6 **a** Amplifier layout designed with the serpentine technique and **b** microphotograph of the fabricated amplifier

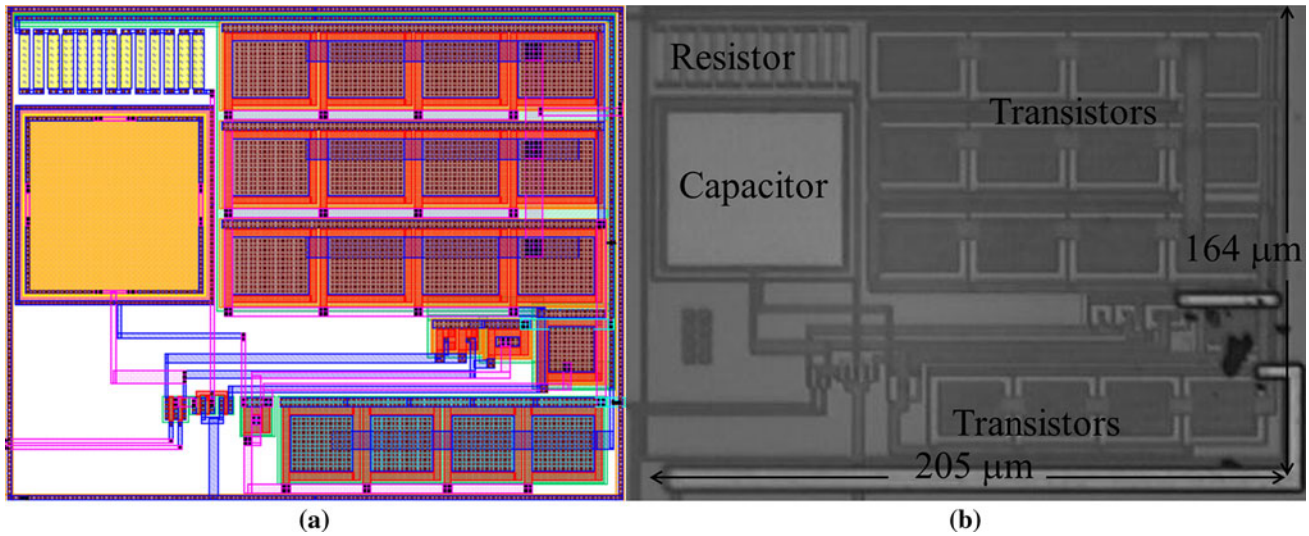

Fig. 7 **a** Amplifier layout designed with the concentric technique and **b** microphotograph of the fabricated amplifier

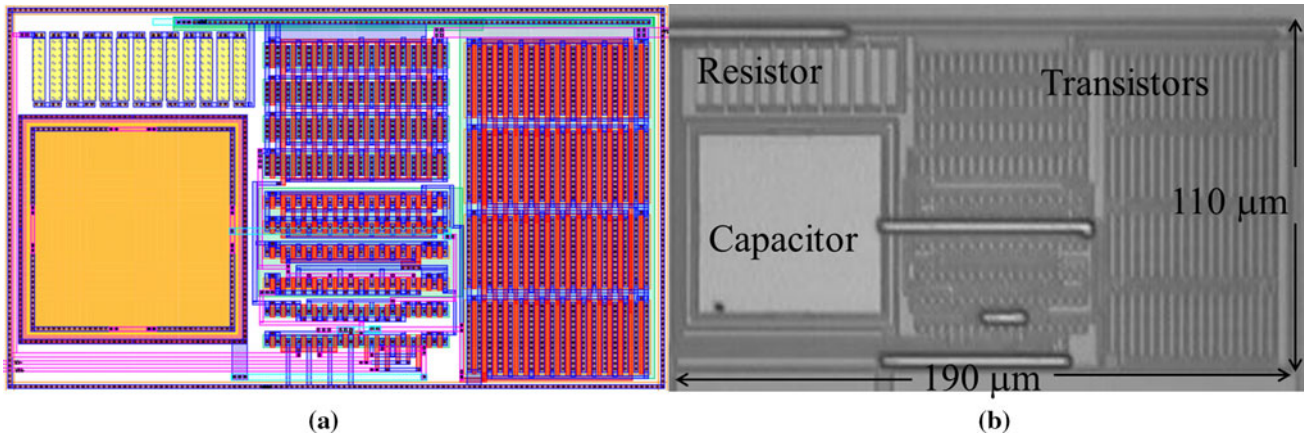

Fig. 8 **a** Amplifier layout designed with the interdigitated technique and **b** microphotograph of the fabricated amplifier

Table 3 Electrical characteristics of a class AB CMOS amplifier designed with different layout techniques

Parameters	Serpentine	Concentric	Interdigitated
Gain (dB)	58.79	58.76	55.10
CMRR (dB)	75	75	68
PSRR (dB)	64	60	57
Power (mW)	5.8	5.8	11
SR (V/µs)	20	19.5	14
Offset (mV)	30	45	15
C_{in} (fF)	8	8.3	8.4
C_{out} (fF)	19.38	20.41	103.76
Area (mm^2)	0.016	0.033	0.020

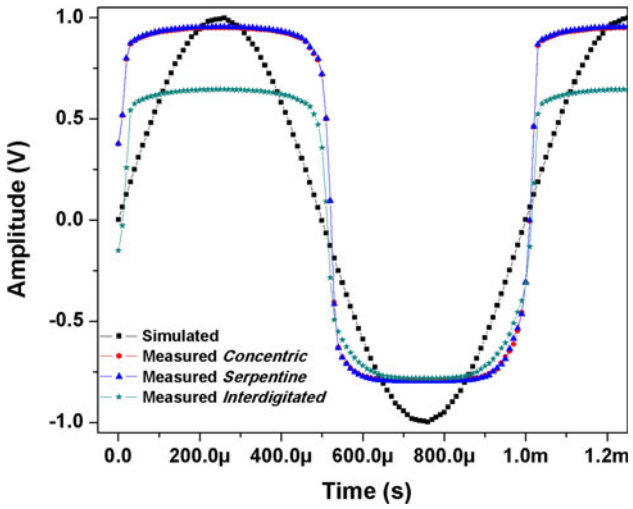

Fig. 9 Transient response of a class AB CMOS amplifier designed with the concentric, serpentine, and interdigitated techniques

transistor, does not depend on the used layout technique. The minimum output capacitances of the amplifier circuits were obtained using the concentric and serpentine technique. These techniques optimize the circuits-physical design due to the minimization of the source and drain

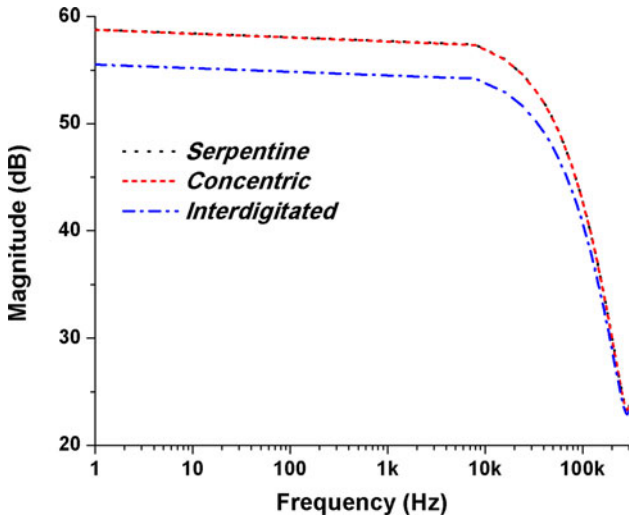

Fig. 10 Gain of a class AB CMOS amplifier designed with the concentric, serpentine, and interdigitated techniques

surface areas, which decrease the interconnection and parasitic capacitances between devices.

Based on results indicated on Table 3, the serpentine and concentric techniques generate speed circuits and improve the PSRR, respectively. In addition, these two techniques allow the amplifier design with the lower power consumption level. Considering the Power-Delay-Area Product, the serpentine technique leads to smaller product potency delay area product. This is most efficient for its application in IC design.

5 Conclusions

The serpentine, concentric, and interdigitated techniques were used in the class AB CMOS amplifier design to study their electrical performance. Based on electrical characterization, the serpentine technique decreases the amplifier surface area

close to 64 % and power consumption about 39 % with respect to the conventional technique. In addition, the serpentine technique increases the SR of the class AB CMOS amplifier. This is due to the reduction source and drain surface areas, which decreases the interconnection parasitic capacitances and the parasitic capacitances between devices. Considering the surface area, delay and consumption power parameters of the class AB CMOS amplifier, and its electrical performance is improved using the serpentine technique.

Further work will include the design and electrical characterization of different electronics devices using different layout techniques.

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