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Offset and gain calibration circuit for MIM-ISFET devices

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Abstract A programmable calibration circuit for sensors is proposed in this paper. It carries out gain and offset compensation by adding or subtracting appropriate correction factors to the transfer function of each sensor. Digital programmability makes it possible to automate calibration, paving the way for batch calibration. The circuit was designed for a specific sensor structure, a MIM-ISFET, which was modeled in HSpice. The proposed scheme reduces the offset and gain error due to process variations of both the sensor and the readout circuit. Offset error is reduced from 123 to 20 mV and gain error is reduced from 10.6 to 6.4 mV/pH. Relative error is reduced in the whole sensing range from 13 to 4 %. The circuit was designed in a 0.18 μm standard CMOS process, occupies an area of 115 × 100 μm^2 and consumes 2.3 mW.

Keywords Sensor calibration · ISFET · Signal conditioning

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1 Introduction

One of the most useful devices to measure the electrochemical activity of ionic solutions is the so-called ISFET: Ion-Sensitive Field-Effect Transistor. Widely used in biomedical applications, analytical chemistry and environmental monitoring [1–4], ISFETs are intrinsically sensitive to pH due to the nature of their gate oxide, which consists of surface reactive sites for the analyte of interest. Their compatibility with CMOS processes makes it possible to integrate them together with the electronic interface and signal processing circuitry on a single chip. In order to standardize their output signal, a calibration circuit can also be integrated with the sensors, thus enhancing their accuracy. If calibration is automatic, the costs are further reduced and calibration time is minimized [5].

In this paper a programmable circuit suitable for calibrating sensor transfer functions is proposed. Though the method is general and can be applied to many types of sensors, its functionality is demonstrated by calibrating an ISFET based on MIM (Metal-Insulator-Metal) capacitors in a useful range of pH level from 4 to 10.

Many of the calibration circuits found in literature are focused on linearization of the sensor transfer function [5–7]. The circuit proposed in this paper is instead focused on offset and gain correction. This is due to the fact that the MIM-ISFET was found to suffer high variations in offset and, to a lesser extent, in gain, because of process variability. Linearity errors, on the contrary, remain below 3 % and were not a concern by now. In [8] a digital correction of offset and gain is also realized but is mainly meant for continuous compensation of changes due to temperature variations.

Section 2 presents the operation principle and physical structure of the ISFET, as well as the ISFET based on MIM

capacitors that will be used. Section 3 shows the measured characteristic curves of the MIM-ISFET compared to the curves simulated with a model for HSpice. Section 4 shows the readout circuit employed and the transfer characteristic taking into account process variations for both the MIM-ISFET and the readout circuit. The calibration principle and the proposed digitally programmable offset and gain calibration circuit are presented in Sect. 5, as well as some post-layout simulation results. Section 6 shows the control algorithm for testing the offset calibration circuit and the experimental results. Finally, some conclusions are drawn in Sect. 7.

2 MIM-ISFET structure

Ion-Sensitive Field-Effect Transistors (ISFETs) are MOSFET-based devices. As shown in Fig. 1, the polysilicon gate of a MOS transistor is replaced by a reference electrode. The electrode is immersed in the aqueous solution (electrolyte) which in turn makes contact with the insulator (sensitive layer). The potential generated at the oxide-electrolyte interface depends on the concentration of the ions to which the insulator is sensitive, i.e., H^+ ions in the case of a pH-ISFET [9].

Due to their structural similarity, the same drain current equation is valid for both MOSFETs and ISFETs. For a MOSFET, the gate voltage V_G is set through a potential applied to the gate contact. In contrast, the gate voltage of an ISFET is the voltage at the reference electrode, usually 0 V.

The threshold voltage, V_T, is a function of the flat-band voltage V_{FB}, the silicon depletion charge Q_B and the Fermi potential ϕ_F, as described by the following equation:

$$V_T = V_{FB} - \frac{Q_B}{C_{ox}} + 2\phi_F \tag{1}$$

The threshold voltage of an ISFET contains terms which reflect the interfaces between the liquid and the gate oxide on the one side and the liquid and the reference electrode on the other. In fact, the flat-band voltage of an ISFET is given by [9]:

$$V_{FB} = E_{ref} - \Psi_0 + \chi_{sol} - \frac{\Phi_{Si}}{q} - \frac{Q_{ss} - Q_{ox}}{C_{ox}} \tag{2}$$

where E_{ref} is the reference electrode potential relative to vacuum, Φ_{Si}/q is the work function of silicon, Ψ_0 is the potential drop in the electrolyte at the oxide-electrolyte interface, Q_{ss} is the surface state density at the silicon surface, Q_{ox} is the fixed oxide charge and χ_{sol} is the surface dipole potential of the solution. All the terms in this equation are constant except for Ψ_0, which makes the ISFET sensitive to the electrolyte pH.

A new kind of ISFET based on MIM (Metal-Insulator-Metal) structures is now being developed [10]. For its fabrication on silicon, a low-voltage low-power (LVLP) 0.25 μm CMOS-based technology was used, namely the so-called M22W process, which is proprietary of *Freescale Semiconductor*. The MIM-ISFET consists of an NMOS transistor with two MIM capacitors coupled to its gate, as shown in Fig. 2. One of the MIM capacitors is connected to a Silicon Nitride (Si_3N_4) layer (sense plate), sensitive to pH and in direct contact with the aqueous solution. The other is connected to a pad for gate biasing. Additionally, another Si_3N_4 layer (sense plate) immersed in the solution is connected to another pad (RE), where a reference voltage can be applied. The MIM-ISFET structure and its symbol are shown in Fig. 2. The theory that describes the electrochemical phenomena at the liquid-oxide interface of a conventional ISFET can also be used to characterize the MIM-ISFET.

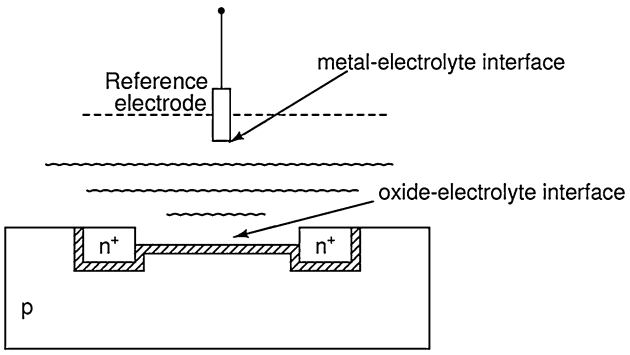

Fig. 1 Schematic representation of an ISFET device

3 MIM-ISFET characterization and modelling

The MIM-ISFET characterization was done by using a Semiconductor Parameter Analyzer. The process consisted in obtaining the $I_d - V_g$ curves by sweeping the gate voltage from 0 to 1.5 V and the reference voltage from −2 to 2 V, at $V_d = 0.1$ V. The process was repeated with the ISFET immersed in three different aqueous solutions with pH levels of 4, 7 and 10. The experimental setup for electrochemical characterization is shown in Fig. 3.

In order to design the conditioning circuit, a model of the MIM-ISFET suitable for standard simulation of electronic designs is necessary. In [11] Martinoia and Massobrio proposed a behavioural macromodel of the ISFET for Spice simulations. It is based on site-binding theory, which describes the charging mechanisms of an oxide as the equilibrium between surface groups and H^+ ions in the solution, the Gouy-Chapman-Stern model of the potential profile in the electrolyte, and the MOSFET physics.

This approach was adapted to model the MIM-ISFET by including the capacitive coupling and the electrical

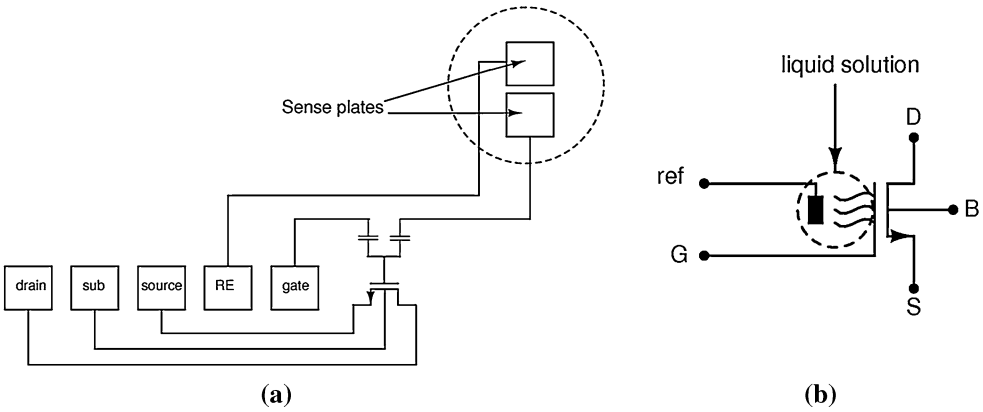

Fig. 2 MIM-ISFET **a** structure and **b** symbol

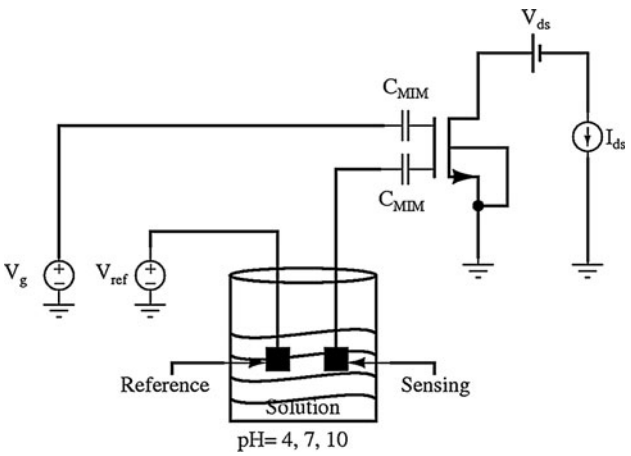

Fig. 3 Electrochemical characterization of the MIM-ISFET

resistivity of the solution, as shown in Fig. 4. E_{ref} represents the equilibrium potential between the reference electrode and the oxide-electrolyte interface, C_{SiO2} and C_{Si3N4} are the capacitances associated with the oxide and sensing layer, C_{eq} represents the electro-chemical stage at both electrodes, R and R' the equivalent solution resistances and C_{MIM} the MIM capacitors.

To validate the proposed model, simulation and experimental results were compared, as shown in Fig. 5. A good agreement was achieved for a reference voltage $V_{ref} = 0$ V. Further improvements are currently being made to the model in order to extend the results to other V_{ref} values. However, the model as it is proved to be very valuable as a starting point in the design of the readout and calibration circuit.

4 Readout circuit and process variability

Readout circuits are critical in the extraction of information from all kinds of sensors. As the purpose of this project was not the improvement of the readout itself but the standardization of the output response of sensors through calibration, the scheme proposed in [12] and shown in Fig. 6 was used. It consists of an operational amplifier which supplies a feedback signal from the drain to the gate of a PMOS transistor, thus compensating the changes in current of the ISFET due to changes in pH of the solution. This readout is simple and insensitive to body effect, and provides an output voltage, V_{sens}, proportional to the change in pH. The circuit was designed in a 1.8 V–0.18 µm CMOS process and a sensitivity of 80 mV/pH was achieved.

A problem encountered when developing the MIM-ISFET was process variability, which also affects the readout circuit. Figure 7 shows the variations generated by process variability taking into account both the MIM-ISFET and the readout circuit. Simulations correspond to the nominal and corner transistor parameter values (TT: typical transistors; SS: slow transistors; FF: fast transistors; FNSP: fast NMOS and slow PMOS; SNFP: slow NMOS and fast PMOS). According to these simulations, a maximum relative error in offset (output voltage at pH 4) of 24 % and a

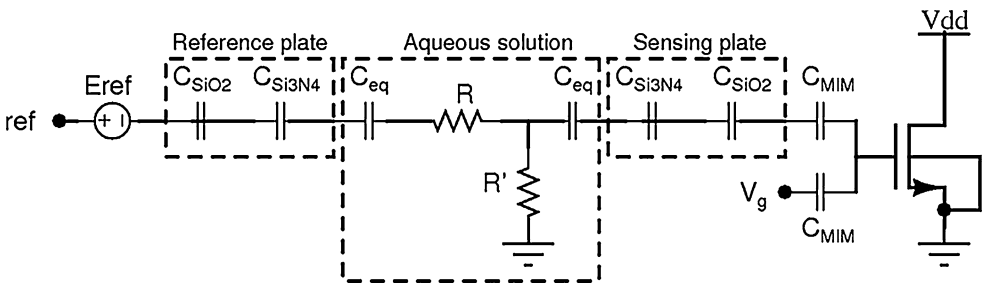

Fig. 4 Equivalent electric circuit of the MIM-ISFET

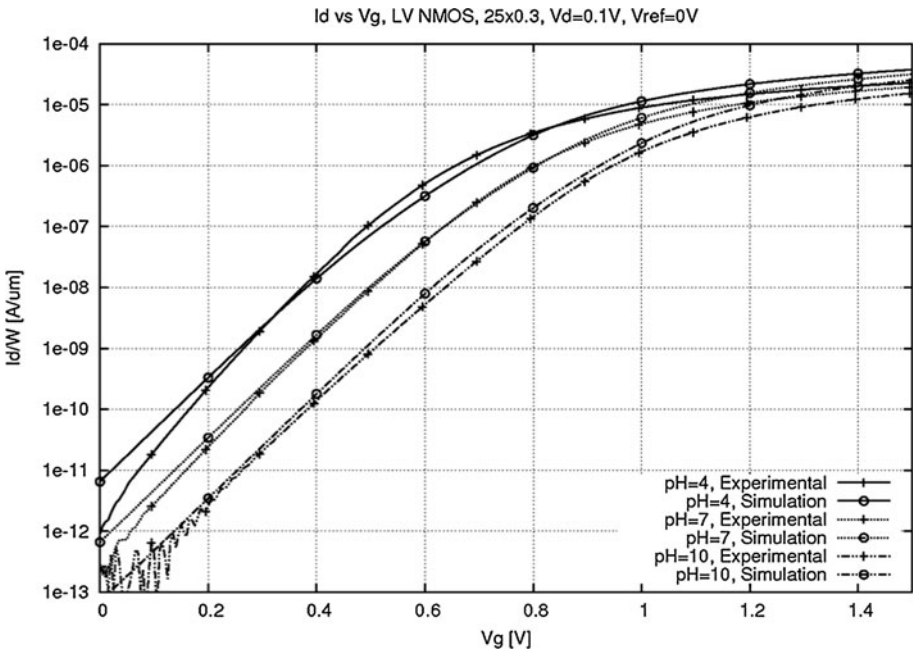

Fig. 5 Simulated versus experimental $I_d - V_g$ at $V_{ref} = 0$ V

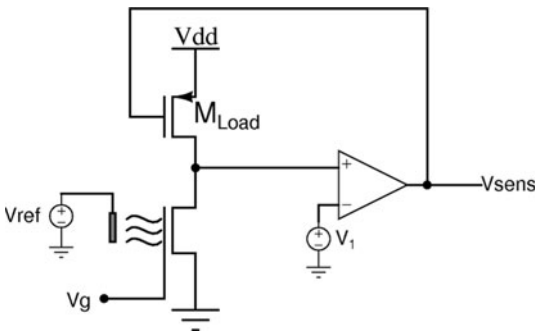

Fig. 6 Readout circuit

maximum relative error in sensitivity (change in mV per pH) of 11 % are to be expected. If reliable measurements of pH are intended, a calibration circuit able to standardize the output response of all fabricated devices is necessary. As already mentioned, the error in linearity remained below 3 %. Thus, calibration in offset and gain was the priority.

5 Digitally programmable calibration circuit

5.1 Offset calibration

The first step in the proposed calibration method consists of shifting the curves in Fig. 7 so that all of them intersect at the lowest input (pH 4). This is equivalent to carrying out an offset compensation by adding an appropriate correction factor to each curve. As it will be shown, this can be easily achieved in the current domain, as addition of currents is straightforward.

Mathematically, offset calibration can be explained as follows. The input of the sensor can be represented by a variable x and the output by a variable y; the uncalibrated response of the sensor can be denoted by the transfer function $y = f(x)$ whereas the desired transfer function is given by $y = g(x)$ and is assumed to be a linear function of the input signal $g(x) = K{\cdot}x$. A calibration measurement x_1 is taken for pH 4, which corresponds to the minimum input value. The sensor's output $f(x_1)$ is compared with the desired minimum output value, i.e. the point where the curves are desired to be translated to (y_1). Thus, a calibration coefficient a_1 is obtained, which is used to calculate the corrected transfer curve $h_1(x)$ of the sensor.

This process can be summarized in the following equation:

$$h_1(x) = f(x) + a_1 y_1 \tag{3}$$

with

$$a_1 = \frac{y_1 - f(x_1)}{y_1} \tag{4}$$

where $h_1(x)$ is the offset calibrated response and a_1 the offset calibration coefficient.

The proposed block diagram to implement offset calibration is shown in Fig. 8. An operational transconductance amplifier (OTA) converts V_{sens}, which is the output voltage of the readout circuit, into a current I_{sens}. A digitally programmable current $a_1 I_{ref}$ is added to or subtracted from I_{sens}. Finally, the resulting current is converted into a voltage by means of a transimpedance amplifier (TIA). The circuit was designed in a 0.18 μm CMOS process and biased with a 1.8 V supply voltage.

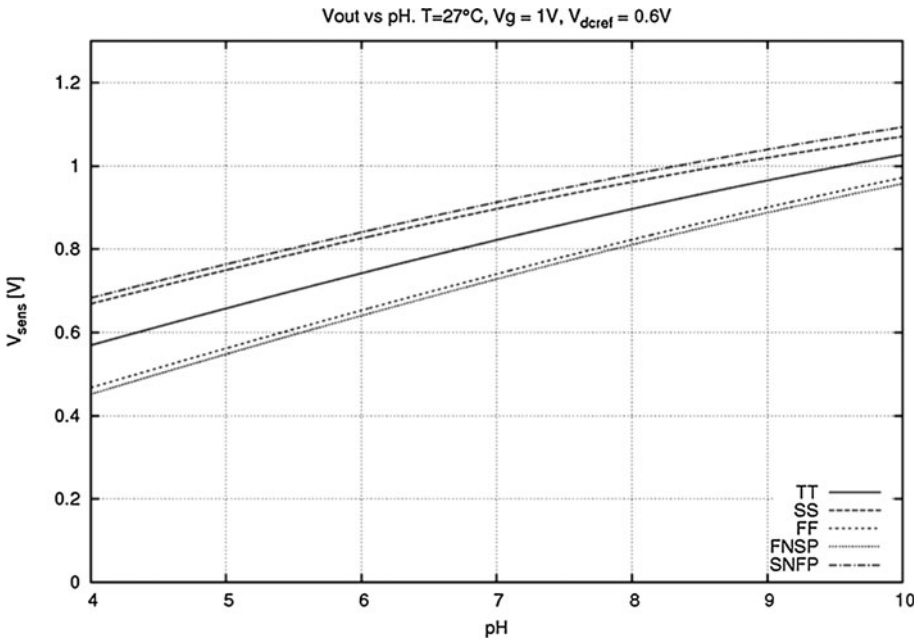

Fig. 7 Process variations for the ISFET and readout circuit

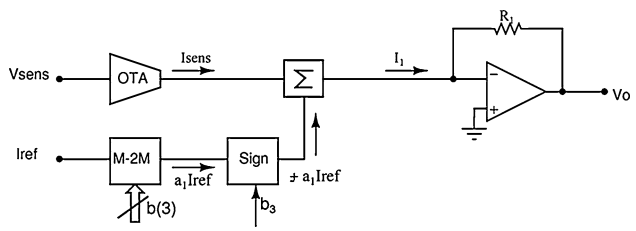

Fig. 8 Proposed offset calibration circuit

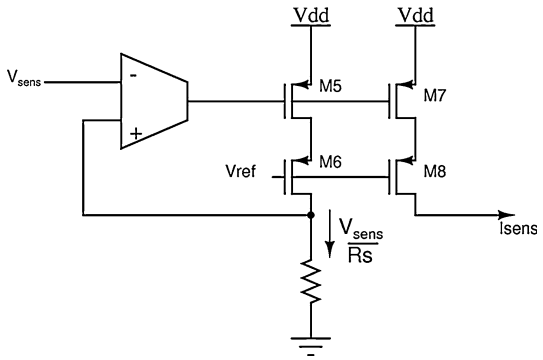

Fig. 9 OTA with output buffer and cascode mirrors

The OTA consists of a differential pair with a cascode PMOS output current mirror, as shown in Fig. 9. The negative feedback sets the output current equal to $I_{sens} = V_{sens}/R_s$, providing high linearity [13].

The 3-bit programmable M-2M network was implemented with PMOS transistors as shown in Fig. 10 [14, 15]. The reference input current, I_{ref}, is divided into two currents. The division factor, which determines the calibration step, is given by:

$$a_1 = \frac{1}{2^n}\sum_{j=0}^{n-1} b_j 2^j \quad \text{with } n = 3 \tag{5}$$

where $b(3) = \{b_2,b_1,b_0\}$ is the digital control word.

In order to determine how much current a_1I_{ref} is needed to cancel offset, another corner simulation was run to see how process variability affects the transimpedance amplifier input, I_1, including this time the effect not only of the MIM-ISFET and readout circuit variations, but also of the calibration circuit itself. Figure 11 shows the process variations for I_1, where it is found that the maximum correction current needed is $(a_1I_{ref})_{max} = 12$ μA. For this reason, a reference current $I_{ref} = 20$ μA was chosen, leading to a maximum available correction current of 17.5 μA, with a minimum current step of 2.5 μA.

To give the system the ability to correct deviations above and below the nominal value (TT), that is, to be able to add or subtract the current a_1I_{ref} from I_{sens}, the sign circuit shown in Fig. 12 was connected to the output of the M-2M network. A set of switching transistors controlled by a digital input, b_3, is used to drive the output of the M-2M either through an NMOS current mirror, inverting the current direction, or directly to the output node [16].

The current I_1 injected to the transimpedance amplifier in Fig. 8 is given by:

$$I_1 = I_{sens} \pm a_1 I_{ref} \tag{6}$$

where the current added to or subtracted from I_{sens} is, in summary, controlled by a 4-bit digital word, $b(4) = \{b_3,b_2,b_1,b_0\}$, with the most significant bit being used to select the direction of the current a_1I_{ref} .

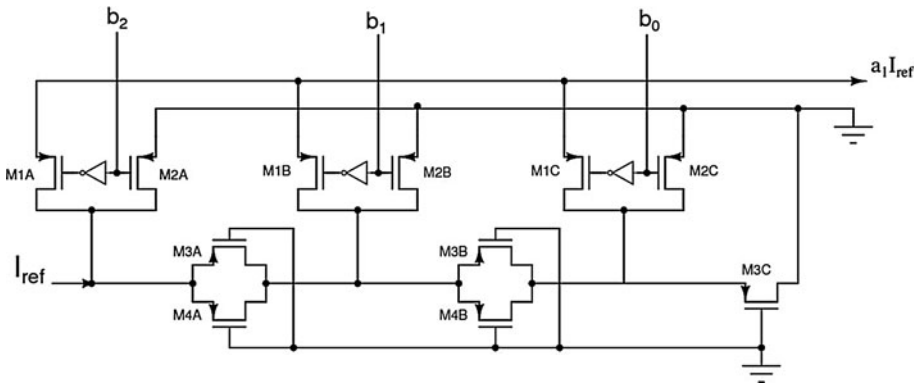

Fig. 10 M-2M network

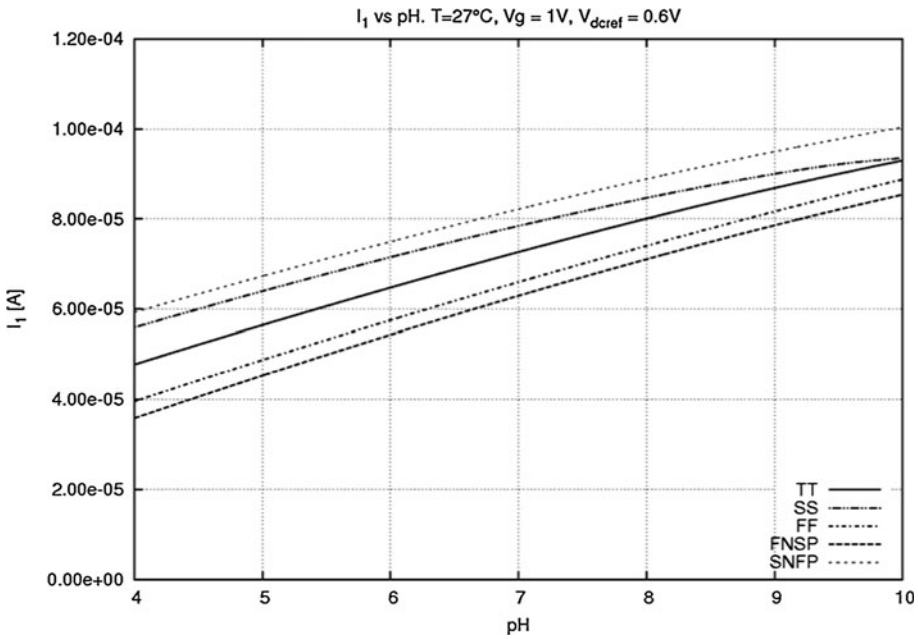

Fig. 11 Process variation for the current I_1

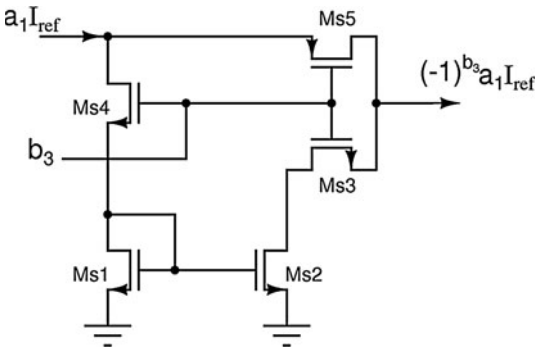

Fig. 12 Sign circuit

The transimpedance amplifier is a two stage operational amplifier with a feedback resistance R_1, as shown in Fig. 8, to transform the calibrated current I_1 into an output voltage $V_{out} = I_1R_1$. Finally, the reference current I_{ref} was generated with a Beta-multiplier reference.

Post-layout simulation results of the calibrated output signal are shown in Fig. 13. The effect of process variability is significantly reduced after applying calibration. Namely, the maximum error in offset was reduced from 123 mV before calibration (BC) to 20 mV after calibration (AC).

Corner simulations were carried out to determine the relative error with respect to the TT, BC and AC at different pH levels. The results are plotted in Fig. 14, where it can be seen that the maximum relative error due to process variations is reduced from 13 to 2 % for the lowest pH considered. Note that the relative error is lower than it was for the sensor and readout alone (see Sect. 4) even BC. This is only due to the fact that the offset value is now higher.

The offset calibration circuit, together with the readout, occupies an area of 115×64 μm^2 and consumes 1.6 mW. Although the explained calibration step is only intended for offset correction, it improves accuracy for the whole pH range, as can be seen in Fig. 14. After offset calibration, the highest relative error occurs for the highest input level (pH 10).

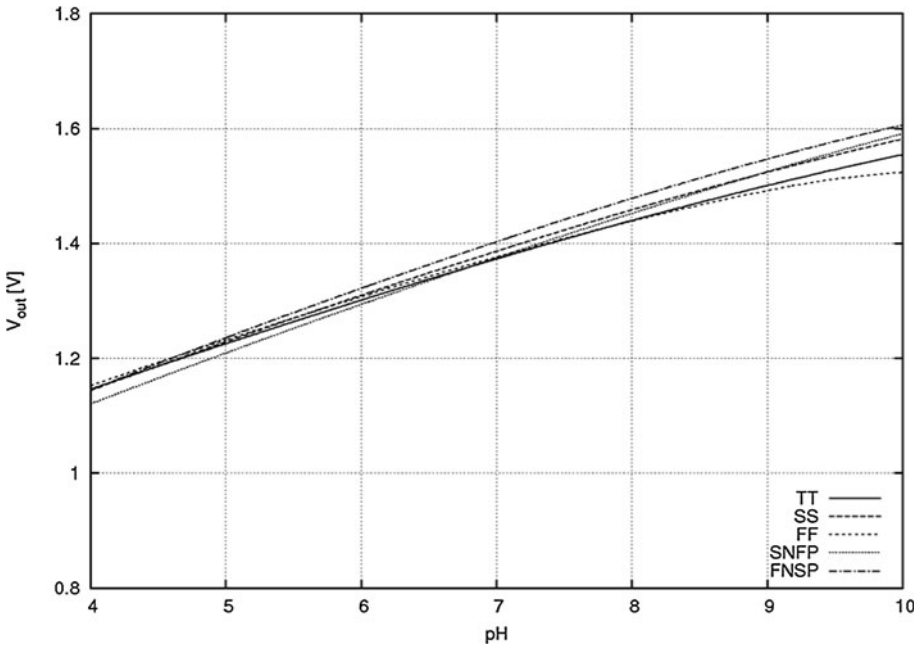

Fig. 13 Output responses after offset calibration

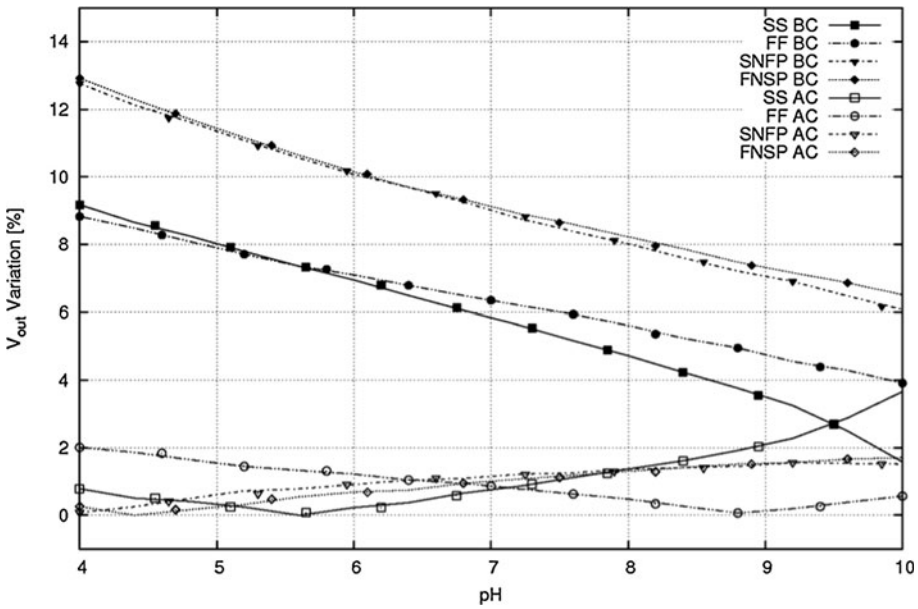

Fig. 14 Relative error before (*BC*) and after (*AC*) offset calibration

More bits can be added to the M-2M network if higher accuracy is still needed. However, if the error in sensitivity is to be reduced, the circuit must be modified for a second calibration step implementation, as explained in the next subsection.

5.2 Gain calibration

The gain or sensitivity calibration consists of rotating the curves in Fig. 13 (after offset calibration) so that all of them intersect at the highest input (pH 10). Mathematically, this operation can be represented by the following equation:

$$h_2(x) = h_1(x) + a_2\{h_1(x) - y_1\} \tag{7}$$

with

$$a_2 = \frac{y_2 - h_1(x_2)}{h_1(x_2) - y_1} \tag{8}$$

Here, $h_2(x)$ is the corrected transfer function, $h_1(x)$ is the offset calibrated response and y_1 the minimum output value determined by offset calibration (see Eqs. 3, 4), y_2 is the desired maximum value where the curves are to be rotated to and a_2 the gain calibration coefficient. Again, the rotation of the curves will be carried out in the current domain by adding or subtracting an appropriate correction current.

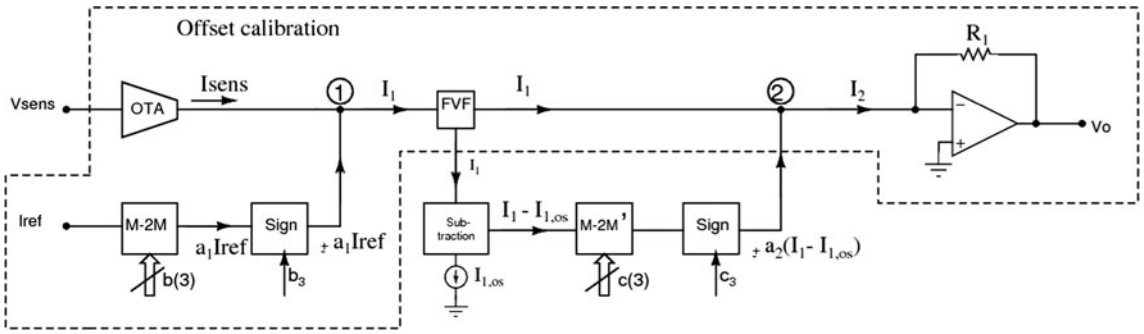

Fig. 15 Proposed offset and gain calibration circuit

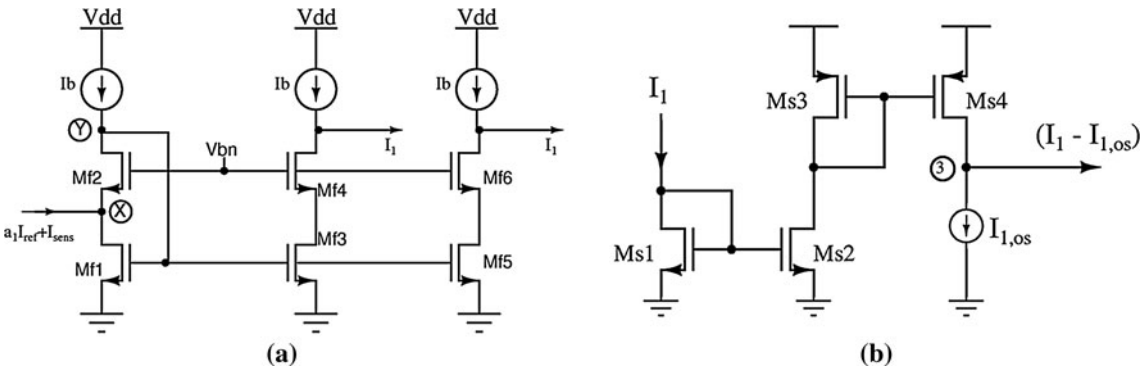

Fig. 16 **a** FVF current mirror and **b** subtraction block

The circuit proposed for offset and gain calibration is shown in Fig. 15. It consists of the offset calibration circuit (inside the dashed line) with an additional flipped-voltage follower (FVF) current mirror and some additional blocks to perform gain correction.

The input signal, V_{sens}, is converted into a current I_{sens} by the OTA. When gain calibration is to be carried out, storage of the offset-calibrated signal I_1 at minimum input is required (y_1 in Eq. 7). The storage block was emulated with a current source $I_{1,os}$. In this way, gain calibration will not degrade offset calibration, as every time the input signal is minimum ($V_{sens,\,min}$ corresponding to pH 4), $I_1 - I_{1,os} = 0$ and the only current injected into node 2 is I_1.

At any other input level, a portion of the current $I_1 - I_{1,os}$ is injected into or extracted from node 2. Thus, the current I_2 injected to the transimpedance amplifier in Fig. 15 is given by:

$$I_2 = I_1 \pm a_2(I_1 - I_{1,os}) \tag{9}$$

where

$$I_1 = I_{sens} \pm a_1 I_{ref} \tag{10}$$

Note the similarity between Eqs. (9) and (7), corresponding to rotation of the curves, and Eqs. (10) and (3), corresponding to translation of the curves.

Similarly to the circuit for offset calibration, the current added to or subtracted from I_1 at node 2 is controlled by a 4-bit digital word, $c(4) = \{c_3,c_2,c_1,c_0\}$. The most significant bit controls a sign circuit (as in Fig. 12) and therefore selects the direction of the current $a_2(I_1 - I_{1,os})$. The less significant bits control the amount of current (a_2) through a 3-bit M-2M current divider (M-2M′). Finally, the resulting current I_2 is converted into a voltage by means of the transimpedance amplifier. The FVF current mirror and the subtraction block are shown in Fig. 16.

Simulation results AC of both offset and gain are shown in Fig. 17. The effect of process variability in gain is reduced from 10.6 to 6.4 mV/pH. Figure 18 shows the relative error with respect to the TT, before gain calibration (BC) and after gain calibration (AC) at different pH levels. The results show a reduction in relative error at the highest pH level due to process variations from 3.2 to 2.4 %.

The complete calibration circuit, together with the readout, occupies an area of 115 × 100 μm^2 and consumes 2.3 mW. Note that calibration was done to standardize all output responses to match the nominal output signal. However, standardization in gain could also have been achieved by just adding a correction signal, not to match all curves with the TT but to increase gain for all of them and match them to a higher value, thus increasing the sensitivity of the whole system.

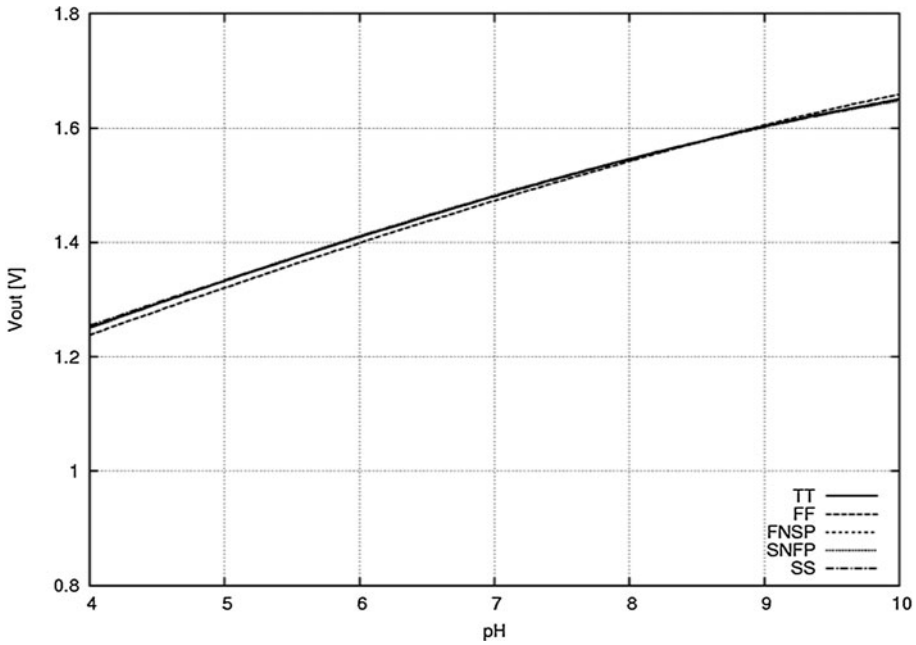

Fig. 17 Output responses after offset and gain calibration

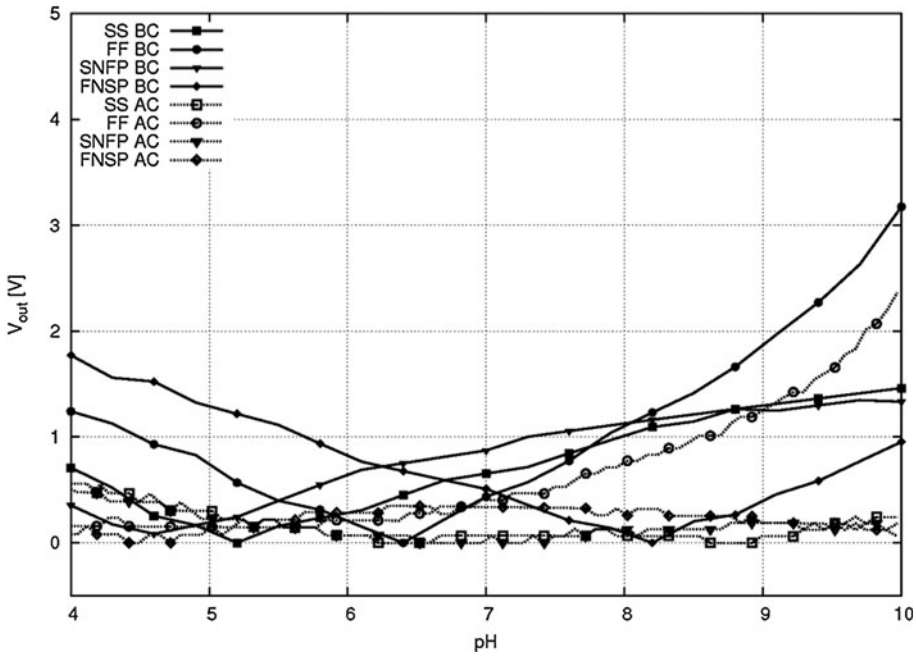

Fig. 18 Relative error before (*BC*) and after (*AC*) gain calibration

In the particular case of MIM-ISFET calibration, digitally controlled calibration in gain was not as effective as expected. To increase accuracy, the number of bits of the M-2M′ current divider should have been increased. However, it was decided by now to integrate a first prototype including only the offset calibration circuit.

6 Experimental results

A first prototype including readout and offset calibration was integrated in a 1.8 V–0.18 µm CMOS process. Figure 19 shows a microphotograph where the building blocks are highlighted.

To test the chip, a simple control circuit was implemented as shown in Fig. 20. It consists of an analog comparator, a 4-bit binary counter, a D flip-flop and some logic gates. The binary counter has a synchronous reset (SR, active low), a parallel enable input (PE, active low), 4 parallel inputs (P3, P2, P1, P0), two count enable inputs (CEP and CET, active high), a clock input (CLK) and 4 parallel outputs (Q3, Q2, Q1, Q0).

The output of the counter is used as the control word for the calibration circuit. A push button is used to start

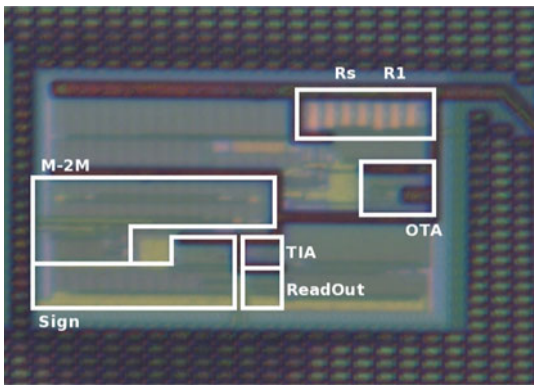

Fig. 19 Chip microphotograph

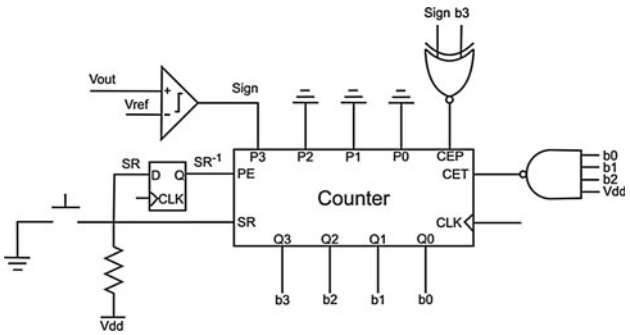

Fig. 20 Digital control circuit

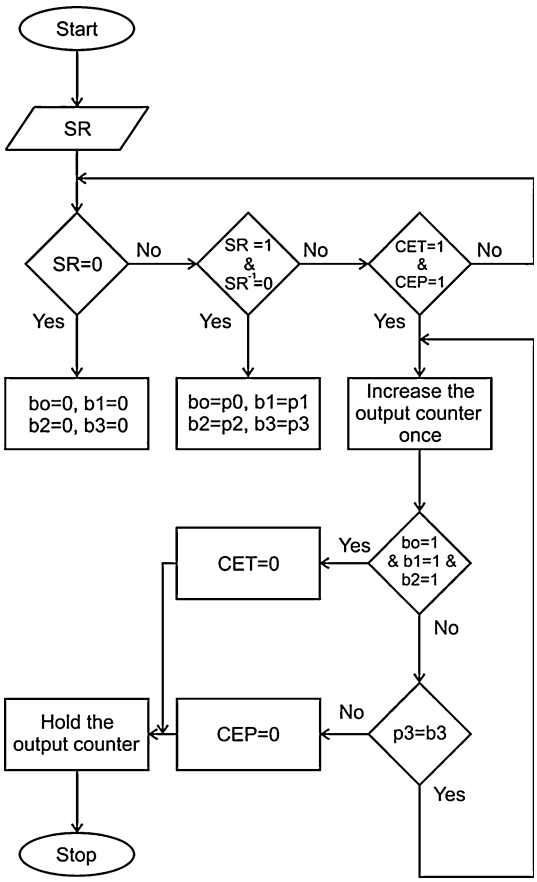

Fig. 21 Control algorithm flowchart

calibration. When the push button is pressed, the counter is reset so that the control word is 0000 and the output of the circuit, V_{out}, only depends on the sensor output signal. V_{out} is compared to the reference voltage V_{ref}. If $V_{out} < V_{ref}$, V_{out} should increase, so the most significant bit b_3 should be set to 1. If $V_{out} > V_{ref}$, V_{out} should decrease and b_3 set to 0. Thus, at the first active clock edge after releasing the switch, the parallel enable input PE is active and the output of the comparator is loaded to the most significant bit of the counter (1 if $V_{out} < V_{ref}$ and 0 if $V_{out} > V_{ref}$), whereas the 3 less significant bits are set to 0. PE is deactivated so that the counter starts up-counting at the next active clock edge, from X000 to X111, being X = 0 or 1. If V_{out} was higher than V_{ref} and turns lower, or viceversa, the output of the comparator changes. When this change is detected the counter is deactivated and the required calibration word is now stored in the counter. If the counter reaches X111 before V_{out} reaches V_{ref}, then the counter is deactivated and again the calibration word is the digital word stored in the counter. If this happens, it means that the offset was higher than the maximum offset that can be compensated for. The whole process is summarized in the flowchart of Fig. 21. Note that after releasing the push button no further action from the user is required.

Figure 22 shows how the output of the calibration circuit V_{out} changes at each active clock until reaching the value of the reference signal. Four cases can be distinguished, depending on whether the reference signal is higher or lower than V_{out}, and whether the difference between both signals is inside or outside the calibration range.

Table 1 shows the experimental calibration step and offset compensation range at different I_{ref} values. As already mentioned, I_{ref} was generated with a Beta-multiplier reference. The exact value of I_{ref} is set by an external resistor R_{ref}. On the one hand, offset deviations higher than $\pm$400 mV can be corrected by increasing the calibration step through I_{ref}. However, this also implies lower resolution and higher error. If such a high calibration range was needed, a better solution would be to increase both I_{ref} and the number of bits of the calibration word in the design phase. On the other hand, the calibration step can be lower than 24 mV, which determines the lowest achievable error in offset. Although the reference current I_{ref} and, therefore,

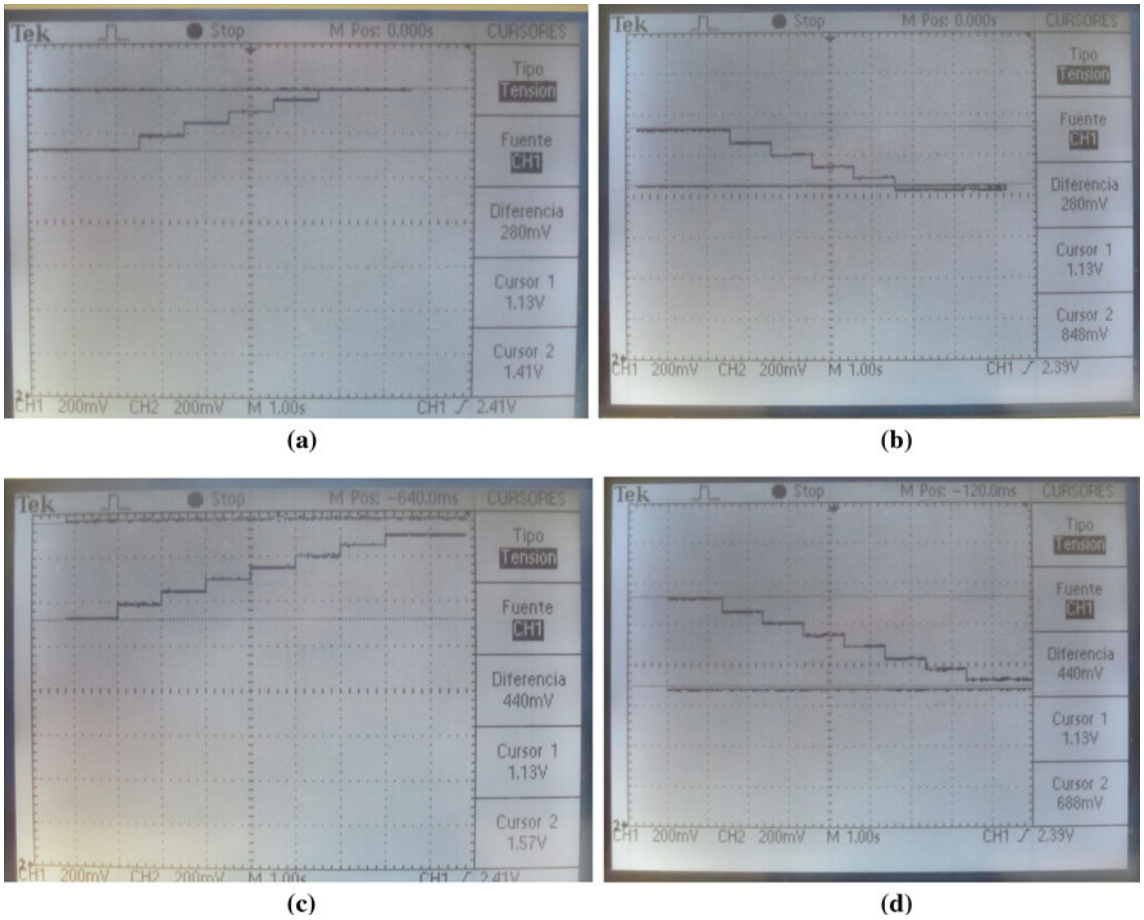

Fig. 22 Experimental offset calibration if **a** a negative offset deviation is corrected, **b** a positive offset deviation is corrected, **c** a negative offset deviation outside the calibration range is corrected and **d** a positive offset deviation outside the calibration range is corrected

Table 1 Calibration step tuning through I_{ref}

R_{ref} (kΩ)	I_{ref} (μA)	Calibration step (mV)	Calibration range (mV)
7	20.1	24.0	±168
6	22.7	26.3	±184
5	28.5	29.7	±208
4	35.1	37.7	±264
3	45.7	57.1	±400

Table 2 Calibration circuit characteristics

Parameter	Value
Technology	0.18 μm CMOS
Supply voltage	1.8 V
Minimum calibration step	24.0 mV
Maximum compensation range	±400 mV
Maximum calibration time[a]	$(2^{n-1} + 1)\ T_{CLK}$
Area consumption	115 × 64 μm^2
Power consumption	1.6 mW

[a] After releasing the push button, with n = number of bits of the calibration word

the calibration step can be somewhat further reduced, note that I_{ref} is saturating. In future implementations more care will be given to the design of the block generating I_{ref}. Table 2 summarizes the main characteristics of the integrated calibration circuit.

Comparison with other calibration circuits is not straightforward. Some of them were designed for linearity improvement [5, 7], some others for temperature compensation [6, 8]. In [8] a digital correction of offset and gain for continuous compensation of changes due to temperature variations is carried out. The calibration circuit proposed in our paper can also compensate for temperature changes, but it is meant for a single calibration before using the pH sensor. In fact, digital programmability allows for batch calibration. If the calibration word is stored in a memory integrated together with the sensor and the readout and calibration circuitry,

the result is a batch of high accuracy sensors. It is worth noting that this does not prevent the use of other compensation techniques to counteract drifts or temperature changes during operation.

In [17] a mixed signal integrated interface circuit for a gas monitoring system is presented. To increase resolution, the dynamic range was divided in 10 sub-intervals. A calibration technique to compensate offset and gain error mismatch between different scales was proposed. The relative error they achieve is lower than 0.1 % in almost every sub-interval, combining coarse and fine calibration at the cost of very high complexity and area consumption: a 13-bit analog-to-digital converter (ADC), two 8-bit digital-to-analog converters (DACs), two programmable resistors (made up of resistors arrays) and a digital control unit are necessary.

In our case, the programmable cells are made up of transistors, considerably reducing area, while maintaining linearity [18]. Higher accuracy can also be achieved with the proposed calibration circuit if the number of bits in the M-2M networks is increased. Furthermore, a finer adjustment could also be realized in our proposal through the reference current, as seen from experimental results (Table 1).

7 Conclusions

A new calibration circuit for offset and gain compensation was proposed for a specific ISFET based on MIM structures. A previous HSpice simulation model was adapted by introducing the physical parameters of the MIM-ISFET, in order to design and implement the readout and calibration circuit. The circuits were designed in a standard 0.18 μm CMOS process. Post-simulation results show that the maximum deviation due to process is reduced from 13 to 2 % for the minimum pH level and from 13 to 4 % in the whole pH range, significantly improving the reliability of the pH measurements. In absolute terms, offset error is reduced from 123 to 20 mV and gain error is reduced from 10.6 to 6.4 mV/pH. The offset calibration circuit was integrated and experimentally tested. A minimum calibration step of 24 mV was achieved with 1.6 mW power consumption at 1.8 V supply voltage. The control circuitry is simple and minimum action from the user is required for calibration.

The proposed calibration circuit does not deal with nonlinearity problems Nevertheless, if the operation range was split into several sub-ranges and the same operation principle was applied to each of them, nonlinearities could also be corrected. This would however result in higher complexity and power consumption.

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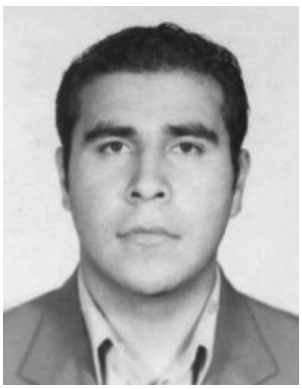

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