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Multiscroll floating gate–based integrated chaotic oscillator

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ABSTRACT

In this work, we proposed a voltage-to-current cell based on a Complementary metal-oxide-semiconductor (CMOS) inverter designed by using floating gate transistors. We demonstrate its usefulness for the design of stair-type and sawtooth functions to be used in the implementation of a multiscroll chaotic oscillator. The main advantage of using floating gate transistors to design the nonlinear functions is the elimination of external reference DC sources, as is typically done in most of the nonlinear functions that generate multiscroll attractors. The key guidelines for the design of our proposed voltage-to-current cell are given to provide good performances in the design of an integrated multiscroll chaotic oscillator. HSPICE simulations are presented to demonstrate the usefulness of the proposed cell to generate multiscroll attractors. Finally, simulation results before and after layout are presented to show the good agreement with respect to theoretical results. HSPICE simulations of the post-layout design are in accordance with the system behavior. Copyright © 2011 John Wiley & Sons, Ltd.

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KEY WORDS: multiscroll oscillator; floating gate MOSFET; chaotic oscillator; stair-type function; sawtooth function; integrated circuit

1. INTRODUCTION

In the area of continuous-time chaotic dynamics, the appearance of multiscroll chaotic behavior has been the subject of much research [1], mainly because of the complexity of the dynamics while allowing for the obtention of partial analytic solutions and some potential applications [2–11]. For instance, multiscroll chaotic oscillators can be designed using piecewise linear (PWL) functions that allow flexible schemes for the circuit implementation (e.g. [12–16]).

Although potential applications for multiscroll chaotic oscillators are still being investigated, some current applications lie in the areas of secure information encryption [2–5], random number generators [6], chaos-based control systems [7–9], and chaotic radars [10,11].

The main challenges in the design of chaotic attractors are related to the system complexity, where open issues like how to generate the higher number of scrolls [17,18], the reliable circuit implementation considering parasitic effects [19], the tradeoffs on frequency behavior [20], the reconstruction and modeling over noisy channels [21], or the Lyapunov exponents analysis [22]. This work discusses the previously mentioned issues by designing a multiscroll chaotic oscillator

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using a new voltage-to-current cell on the basis of a CMOS inverter and realized with floating gate transistors.

Traditionally, the design strategies of multiscroll chaotic attractors are based on the use of PWL functions to design the nonlinear part of the dynamical system [1,23]. Commonly used nonlinear functions are the stair function approach [12], the saturated approach [13,24], the sawtooth function [14–16], and others. Most of these designs use a switching component (sign function). On the other hand, the generation of chaotic attractors using integrated circuit designs has reported up to two-scroll attractors [25–29]. The use of the switching component is evident in the studies of Radwan *et al*. [28] and Gandhi and Roska [30].

Multiscroll exceptional designs are the floating gate CMOS (FGMOS)–based circuits presented by Fujiwara *et al*. [31], which were reported to generate up to three scroll-attractors (mostly due to the lack of regularity on the PWL function), and the multiscroll circuitry in [30], in which the author proposes to implement the switching mechanism on integrated circuit to achieve a larger amount of scrolls, both by using external increasing number of DC references.

A key point in all the design techniques mentioned is that the PWL function was designed using external reference DC voltage sources or external adjustable voltage dividers. Thus, to overcome the issues of integrated circuit realization of the PWL function and DC references over a highly flexible switching element required for the generation of multiscroll attractors, we recently proposed a new nonlinear voltage-to-current cell based on FGMOS inverters [16]. Basically, the inverter is designed with an internal input offset provided by the size relationships of the gate capacitors.

This work details the design procedure of a redefined and improved new switching cell that was able to perform multiscroll attractors according to HSPICE simulations using integrated CMOS technology with a feature size of 0.5 μm, and the results are given before and after layout. Particular advantages of our proposed design are the use of FGMOS transistors to generate input voltage offsets at the comparator, thus creating intern references, and the unique current-switching mechanism, which allows adjustments to the rest of the circuit.

2. PROPOSED VOLTAGE-TO-CURRENT CELL

A simplified schematic of the proposed switching element is shown in Figure 1a. It is a voltage-to-current cell embedding an inverter to perform voltage comparison. A FGMOS array provides a voltage shift to the inverter input. At the output, a cascode topology is in charge of the current transmission.

Basically, the proposed cell includes a current switch with a trigger in the floating input node. This node is precharged to voltage V_{DC} by the set of bias capacitors $C_b = C_2 \ldots C_n$. The other capacitor C_1 is used as the circuit input. When V_{in} is high enough to activate the inverter, the output current is I_{bias}; otherwise, the output current is I_{off}.

A more detailed schematic of Figure 1a is shown in Figure 1b. The first stage is the inverter designed with FGMOS (i.e. M1 and M2 transistors), which drives the gate of M3, allowing the bias current (branch M5 to M7) to be switched between M3 and M4. The output branch is conformed by transistors MS0–MS4. FGMOS transistors M6 and MS0 are used to control the amplitude and the offset of the output signal, respectively. V_A and V_B are playing the role of V_{bias} to preset adequate control voltages at the gates of M6 and MS0.

All bulk connections are made to the corresponding bias voltages V_{dd} or V_{ss}, where $V_{dd} = -V_{ss} = 2.5$ V unless specified. Voltages Vb1 to Vb4 are obtained by using the cascode biasing circuit shown in Figure 2, which was developed exclusively for this design. The transistor sizing of the voltage-to-current cell is shown in Table I.

The transient behavior can be analyzed using the simplified stages shown in Figures 1c–1e. The approximations used herein for roughly describing the circuit behavior are supported by the simulations. The transition time is divided into t_1 (Figure 1c), t_2 (Figure 1d), and t_3 (Figure 1e) for each stage. We call t_{HL} the total time required for the output current signal to fall from I_{off} to $-I_{bias}$ (similar to a digital circuit) and t_{LH}, the total time required to raise the output current from $-I_{bias}$ to I_{off}. Both cases are analyzed separately.

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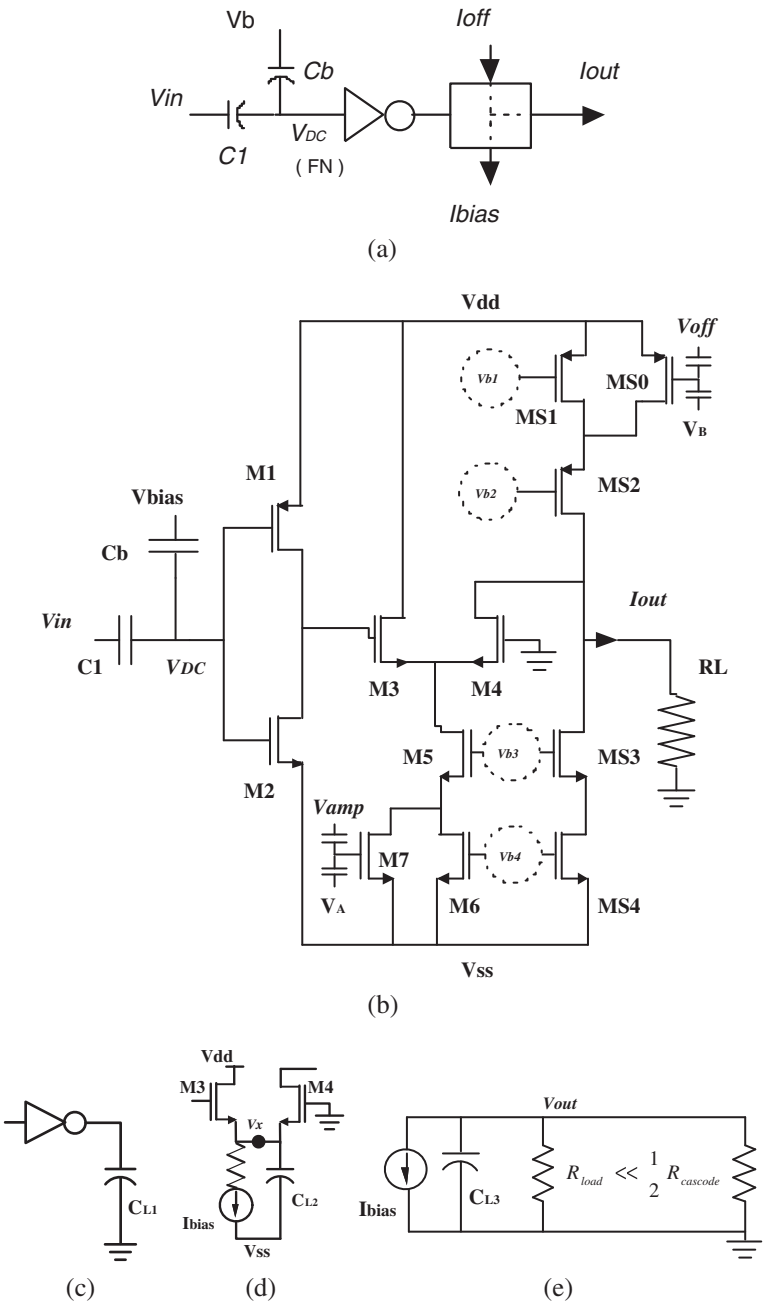

Figure 1. FGMOS-based voltage-to-current cell: (a) simplified schematic, (b) CMOS design, and simplified stages: (c) inverter stage, (d) comparator stage, and (e) output stage.

2.1. Transition t_{HL}

Figure 1c corresponds to the FGMOS inverter; its decreasing output controls transistor M3 (second stage) by turning it to cutoff when its value is below $V_{tN} + 2V_{dsat} - Vss$. For simplicity, we used a basic approximation for the inverter excursion time as t_1 because this transition is relatively fast [32]

$$t_1 = t_{pHL} = \frac{C_{L1}(V_{dd} - V_{ss})}{k_N(V_{dd} - V_{ss} - V_{thN})^2}, \tag{1}$$

where $k_N = c_{oxN}\mu_0$, $k_P = c_{oxP}\mu_0$, and C_{L1} is the parasitic capacitance formed by

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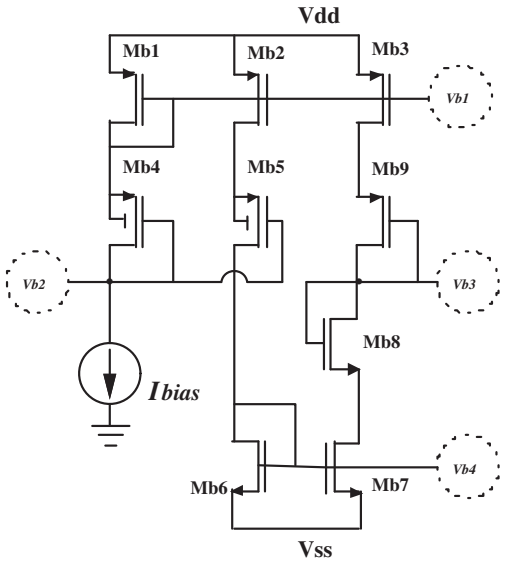

Figure 2. Cascode biasing of the proposed nonlinear cell.

$C_{L1} = C_{gdM1} + C_{gdM2} + C_{gsM3}$, in which the value is found to be around $C_{L1} \approx 14.4$ fF. Thus, one have $t_1 \approx 0.071$ ns.

In the second stage described by Figure 1d, M3 and M4 are both in cutoff because node V_x has been initially set by voltage V_{GS} of M3 to the cascode fixed current $I_{bias} = 2$ μA when only M3 is conducting, and now this current is simply discharging the node V_x until transistor M4 starts conducting this same current. The overall voltage change on the node is

$$\Delta V_x = V_x(t = t_2) - V_x(t = 0) = V_{dd} - V_{GS}(I_{bias}) - (0 - V_{GS}(I_{bias})) = V_{dd} \tag{2}$$

Thus, if both transistors are in cutoff, the time is found by integrating the constant current through $C_{L2} \approx 2C_{ovM3}W_{M3} = 1.56$ fF, then

$$t_2 \approx C_{L2}\frac{\Delta V_x}{I_{bias}} = 1.95 \text{ nF}. \tag{3}$$

According to the third stage described by Figure 1e, a current I_{bias} will suddenly discharge the output node from $V_{out}(t = 0) = 0.5I_{bias}R_{load}$ to $V_{out}(t = t_3) = 0$ (50% of excursion) through the parallel RC circuit given by the output load $R_{load} << R_{cascode}$ and $C_{L3} \approx C_{gdM4} + C_{gdS2} + C_{gdS3} = 6$ fF. Thus,

Table I. Transistor dimensions

Transistor	Width (μm)	Length (μm)
M1	12.6	3.9
M2	3.9	3.9
M3, M4	1.8	1.2
M5, M6, Ms3, Ms4	5.4	3.6
M7	3	4.2
Ms0	15	1.5
Ms1, Ms2	15	3.6
Mb1 to Mb5	15	1.2
Mb6 to Mb8	5.4	1.2
Mb9	5.4	6

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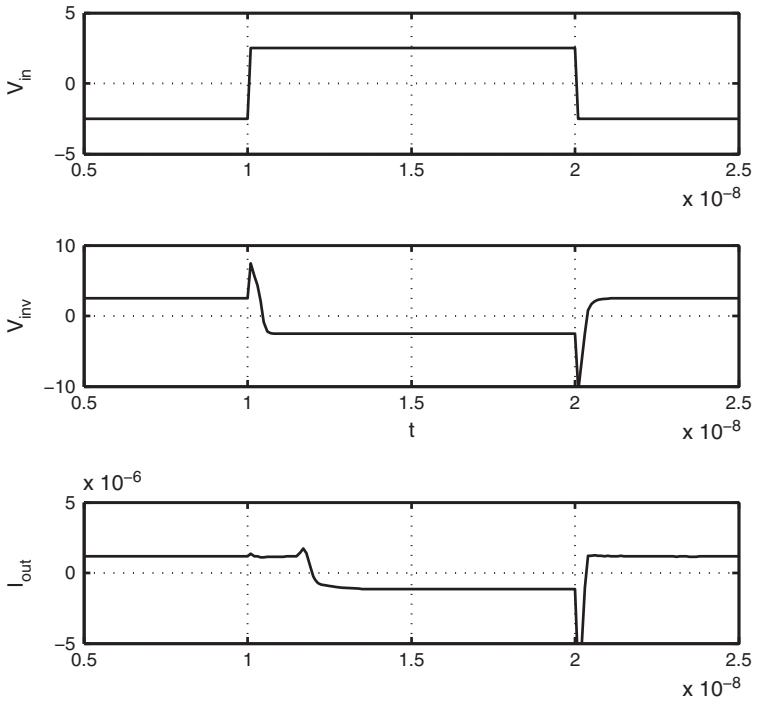

Figure 3. HSPICE transient simulation for the high to low transition t_{HL} at 10 ns and the low to high transition t_{LH} at 20 ns. Upper, middle, and lower windows show the inverter input (Figure 1c), the second stage input (1d), and the voltage-to-current cell output (1e), respectively.

$$t_3 \approx -R_{load}C_{L3}ln\left(\frac{V_{out}(t_3) - I_{bias}R_{load}}{V_{out}(0) - I_{bias}R_{load}}\right) = 0.005 \text{ ns} \tag{4}$$

This generates t_{HL} =2.026 ns, which is in close accordance with the simulation shown in Figure 3. It can be noticed that Equation (3) points to the highest delay. As a comment on optimization, we suggest to bias the drain terminal of transistor M3 to a voltage as low as ground to cancel Equation (2) and make t_2 negligible with respect to t_1. In this way, the comparator delay can be similar to a single inverter delay.

2.2. *Transition* t_{LH}

Following Figure 3, the close relation on this transition time to the inverter transition time, which is $t_1 \approx$0.242 ns [32], can be observed:

$$t_1 = t_{pLH} = \frac{C_L\left(V_{dd} - V_{ss}\right)}{k_P\left(V_{dd} - V_{ss} - |V_{thP}|\right)^2} \tag{5}$$

This is due to the second stage described by Figure 1d, as node V_x has a low voltage fixed by the saturated transistor M4. When M3 leaves the cutoff region, the current flows from M3 to M4, and the transfer is direct, the fast adjustment of V_x is due to the instant high transconductance of M3 (roughly $t_2 = 0$).

At the third stage described by Figure 1e, the calculation reaches the same value of transition t_{HL}. Thus, the total time is t_{LH} =0.250 ns, which is in accordance with the simulation.

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3. BUILDING PWL CHAOS-ORIENTED FUNCTIONS

If different combinations of the capacitor set C_b are used (Figure 1a), several voltage-to-current cells can be connected in parallel to produce a stair-like function, which is seen very often in the design of multiscroll oscillators [1,12–15,24].

To calculate the required bias capacitors, we set the internal DC reference V_{DC} given by Equation 6 at the floating node considering the total capacitance connected to it, $C_T = C_1 + C_2 + \ldots + C_n$, and the used bias voltages (V_2 to V_n). Because C_1 is the input capacitor, V_{in} will not contribute to the DC reference, but the overall input signal will be compressed by the ratio $k = \frac{C_1}{C_T}$ (see Figure 4).

$$V_{DC} = V_2 \frac{C_2}{C_T} + V_3 \frac{C_3}{C_T} + \ldots + V_n \frac{C_n}{C_T} \tag{6}$$

As the bulk capacitance C_n is taken into account, the bulk contribution given by Equation 7 has been obtained by the technology dependent parameter $f_{cpcb} = 0.14$, which is the ratio of the Poly1 to bulk capacitance to the Poly2 to Poly1 capacitance (for details on the 0.5-μm ON semiconductor process currently used in this work, see [33]).

$$C_n = f_{cpcb}(C_1 + C_2 + \ldots + C_{n-1}) \tag{7}$$

According to Figure 4, if the total capacitance C_T and the compression factor k $(1 > k > 0)$ are chosen, the other capacitors may be calculated using Equations 7 and 8,

$$\begin{aligned} C_1 &= kC_T \\ C_2 &= \left(C_T \frac{V_3 + V_b f_{cpcb}}{f_{cpcb} + 1} - C_1(V_3 - V_1) - C_T V_{DC} \right) \frac{1}{V_3 - V_2} \\ C_3 &= \left(C_T - C_1 - C_2 - f_{cpcb}(C_1 + C_2) \right) \frac{1}{f_{cpcb} + 1} \end{aligned} \tag{8}$$

It is desired to have a large factor k to have low compression. However, for the selection of the total capacitance C_T, two bounds will be considered. First, the capacitance C_b (and therefore C_T) must be sufficiently high to avoid the effects of the nonlinear parasitic capacitances of gate to source (M1, M2). As a rule of thumb, this means approximately 10 times the value of the higher parasitic capacitance (C_{GS}^{M1}). Roughly, for M1 saturated and M2 in cutoff,

$$C_{GS}^{M1} \approx (2/3) W^{M1} L^{M1} C_{OX} \tag{9}$$

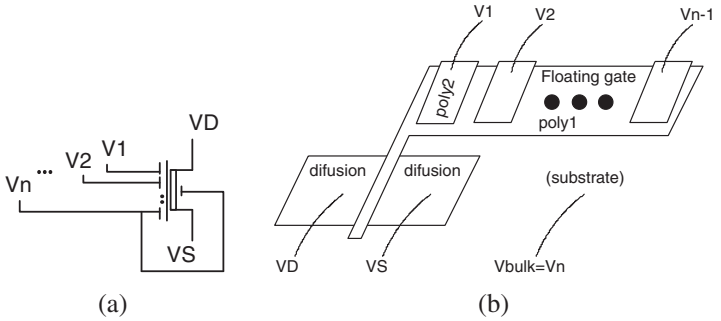

Figure 4. The used FGMOS transistor: (a) electrical diagram and (b) physical device.

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Second, C_b must be low enough to prevent the effect given by the parasitic pole formed by the equivalent input capacitance (say C_{in}) and the output resistance of the preceding buffer (R_{out})

$$f_p = \frac{1}{2\pi R_{out} C_{in}} \tag{10}$$

Given this considerations, we present two design examples of typical nonlinear functions. The function size will be defined by the dynamic range (DR). Besides, each breakpoint is generated by one voltage-to-current cell and has its own set of bias capacitors; for the rest of the document, we assume C_b as a single capacitor.

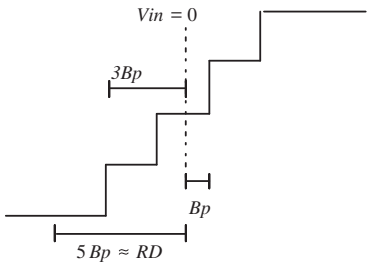
3.1. Stair-type n = 5 example

A symmetrical stair-type positive function with odd number of steps (see Figure 5a) can be described by

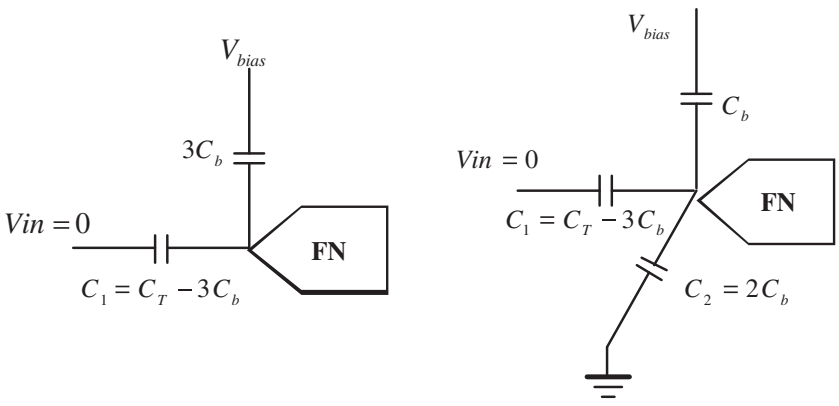
$$g(x) = \begin{cases} 0 & |x| \le B_p \\ 2ksgn(x) & |x| \le B_p(2k+1) \\ & |x| > B_p(2k-1) \end{cases}, \tag{11}$$

$$g(x) = (2k-1)sgn(x) \begin{matrix} |x| \le 2kB_p \\ |x| > 2B_p(k-1) \end{matrix}. \tag{12}$$

where $k = 1, 2 \ldots$ accounts for $n = 1 + 2k$ number of steps and spaced by B_p. Refer to Equation (12) for $n = 2k$ even number of steps.



(a)



(b)

Figure 5. Stair-type $n = 5$ function: (a) function basic relations and (b) bias capacitors connected to the floating input node.

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Assume only two capacitors connected to the floating node (C_1 and C_b). For $n=5$ steps, the break point (B_p) is settled below $\frac{DR}{n}$; the rest of the values are computed by Equations (13)–(15),

$$C_b^q = C_T^q\left(\frac{B_p^q}{V_{bias}}\right) \tag{13}$$

$$C_1^q = C_T^q - C_b^q \tag{14}$$

$$B_p^{q+1} = \frac{C_1^q}{C_T^q}B_p^q \tag{15}$$

Observe that it is actually iterated that because the signal compression changes the breakpoint, this process is followed for a few q steps until the value of B_p converges.

Thus, one have the values for the inner stairs where V_{bias} stands for the V_{dd} and V_{ss} connected C_b (see Figure 5b). In addition, two outer stairs are computed by replacing the value of B_p by $3B_p$ as can be inferred by Figure 5a in Equation (13). Note that having different values of C_b means a different compression of the received signal. To avoid these nonuniformities, a neutral capacitor C_n is connected between the floating node and the ground for the cells in charge of the inner slopes (see Figure 5b).

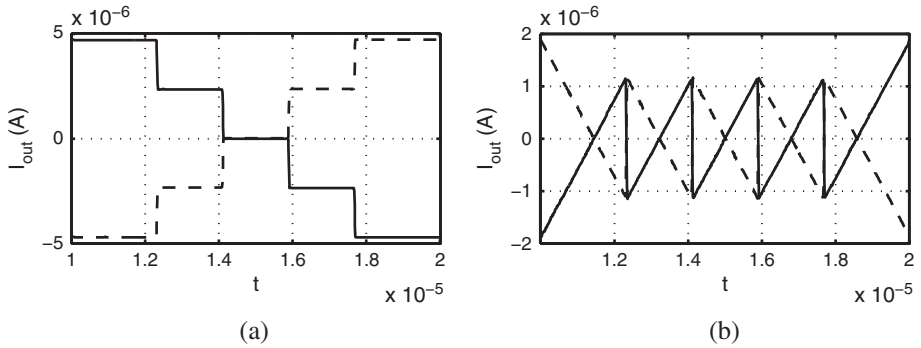
Observe that in practice, each step is set according to the circuit bias current I_{bias} (adjustable amplitude through M7); thus, Equations (11) and (12) are in fact scaled by the circuit factor I_{bias}. Figure 6a shows it with an extra scaling of ξ.

3.2. Sawtooth-type n = 5 example

A sawtooth-type nonlinear function with slope ξ can be generated by using a stair-type function with gain ξ connected in parallel (summing) with function $h(x) = -\xi x$ as described in Equation (16) for odd functions or Equation (17) for even functions,

$$f(x) = \begin{cases} -\xi x & |x| \le B_p \\ \xi(2ksgn(x) - x) & |x| \le B_p(2k+1) \\ & |x| > B_p(2k-1) \end{cases} \tag{16}$$

$$f(x) = \xi((2k-1)sgn(x) - x) \qquad \begin{matrix} |x| \le 2kB_p \\ |x| > 2B_p(k-1) \end{matrix} \tag{17}$$



(a) (b)

Figure 6. PWL V-I functions CMOS transient simulation, input signal is −1 to 1 V (dashed line), and 1 to −1 V (solid line): (a) stair-type function and (b) sawtooth-type function.

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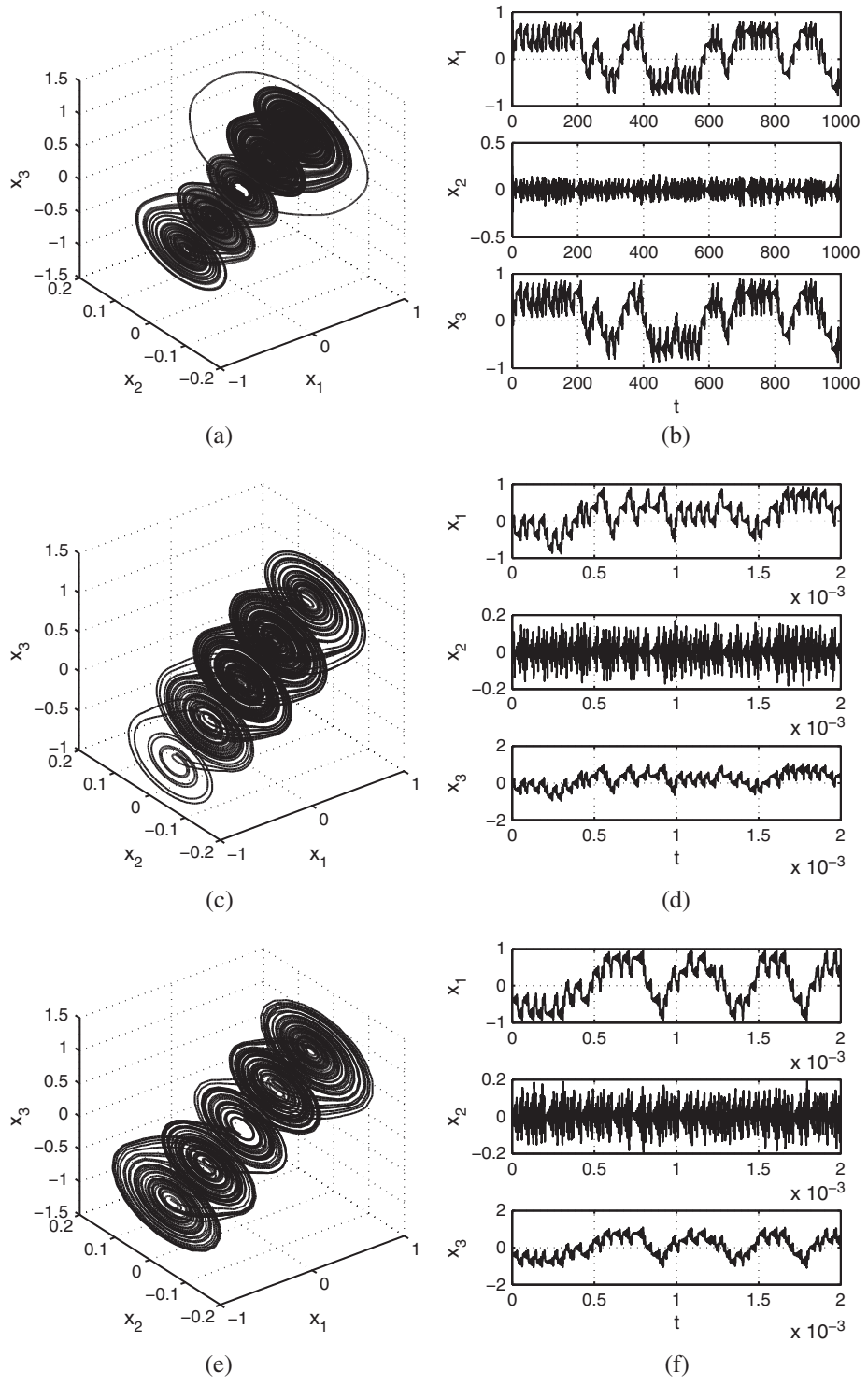

Figure 7. The five-scroll attractor in (a, c, e) phase and (b, d, f) time, (a, b) for the ideal system, (c, d) the HSPICE design, and (e, f) the post-layout simulation.

For the circuit implementation, the gain of $h(x)$ may be given by $-\frac{\xi}{R}$; in this case, it is required to fulfill the relation:

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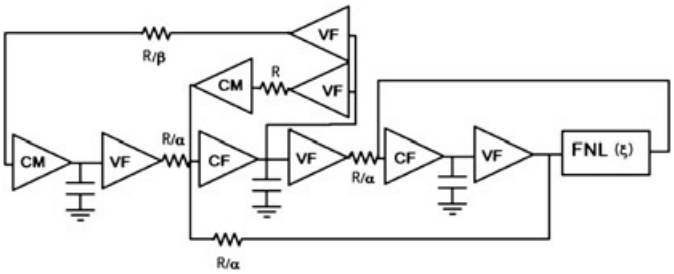

Figure 8. Circuit realization of multiscroll chaotic oscillator described by Equation ((19).

$$\frac{\xi}{R} = \frac{I_{\text{bias}}}{B_{\text{p}}} \tag{18}$$

where I_{bias} is the amplitude of the step current given by the voltage-to-current cell and $1/R$ stands for the linear circuit gains. To properly couple these values, the amplitude is tuned by M6. The circuit response is shown in Figure 6b.

4. MULTISCROLL CHAOTIC ATTRACTOR DESIGN

Our proposed voltage-to-current cell based on the FGMOS inverter can be very useful to implement many forms of multiscroll systems already published. In this section, we have chosen a recent sawtooth-based multiscroll design [16] to exemplify an application. Two main reasons motivate this selection:

The dynamical system properties have been analyzed before [34], where the coefficients have been optimized to deal with circuit tolerances while chaotic behavior has been kept.

For the system's particular nonlinear function, the Jacobian can be considered constant, which maintains mathematical simplicity, whereas the system complexity is the same for any number of scrolls in terms of the Lyapunov exponents [18].

Thus, the dynamical system given by Equation (19), with parameters $\alpha = 3$, $\beta = 4$, and $\gamma = 1$, and a sawtooth function (based on a parallel array of comparators and a negative amplifier) of Equations (16) or (17) will generate a multiscroll attractor. A Lyapunov analysis reveals $\lambda_1 = 0.222$ for the selection of the slope parameter $\xi = 0.8$. A typical five-scroll attractor may be seen in Figures 7a and 7b.

$$\begin{aligned} \dot{x}_1 &= \alpha x_2 + f(x_1) \\ \dot{x}_2 &= \alpha x_1 - \gamma x_2 - \alpha x_3 \\ \dot{x}_3 &= \beta x_2 \end{aligned} \tag{19}$$

The multiscroll chaotic system described by Equation (19) has been designed by unity gain cells [35] as shown in Figure 8. The electrical characteristics of the voltage follower, current follower,

Table II. Design electrical parameters

Parameter	Voltage follower	Current follower	Current mirror	Voltage-to-current cell	Units
DR	$>\pm 1$	$>\pm 100$	$>\pm 100$	$\pm V_{\text{bias}}$	V, μA
Gain	0.985	1.00	0.989	Adjustable	–
BW ($C_{\text{L}} = 1$pF)	100	70	55	400	MHz
R_{in} (1 MHz)	∞	1.4	1.4	∞	kΩ
R_{out} (1 MHz)	1.2	2470	290	550 (on/off)	kΩ
Offset	25	−90	<1	Adjustable	μV, pA
I_{bias}	60	60	60	5	μA

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Table III. Design requirements

	Linear circuit	PWL circuit
Required		Modularity
		Fast transition
	Swing	DC references
	Parameter relation	Adjustability
	Low offset	Low hysteresis
	High Z_{in}	
	High Z_{out}	
Not necessary	Area	
	High bandwidth	
	Exact gain	
	High linearity	

and current mirror for the ON 0.5-μm process are presented in Table II. These must be in accordance with Table III respecting the following criteria:

The circuit swing will be related to the ability to increase the number of scrolls by avoiding noise and circuit fault tolerances. The parameter relation is critical to sustain chaotic behavior. A prior analysis on the operation region[1] is useful in the parameter selection, where the devices DC gain is taken into account.

Because the offset is a big issue on either comparator design or chaotic autonomous systems, offset cancellation/adjusting techniques should be considered. The circuit topologies must be chosen to achieve good coupling among the different parts to avoid signal attenuation, which can affect the system operation parameters. In addition, hysteresis control is desirable to generate accurate nonlinear functions.

The frequency limitation of nonlinear devices is directly degrading the PWL function [20], thus changing critically the dynamical system properties. This motivates our selection for the simple inverter topology. In contrast, the linear circuit bandwidth can be much lower (depending on the PWL structure and the system time constant). Another relevant consideration is the omission of external DC references by the generation of the internal V_{DC} shift voltages (as explained earlier).

As a result, the nonlinear function block in Figure 8 is representing the parallel array of the nonlinear cell in Figure 1a as previously discussed in Section 2. The input capacitance of this block will grow as these arrays grow in number, that is, the number of scrolls grows. Then, Equation (10) can be rewritten for this multiscroll implementation as

$$f_p = \frac{1}{2\pi R_{outVF}(n-1)(C_1||(C_T - C1))} \tag{20}$$

where R_{outVF} stands for R_{out} and capacitors C_1 and C_T have been calculated by Equations (13)–(15) to conform the total input capacitance C_{in}. This pole will eventually limit the number $n \geq 2$ of scrolls with frequency.

The HSPICE simulation before layout is shown in Figures 7c and 7d. Finally, the Tanner post-layout simulation of the chaotic oscillator with five-scroll attractors is shown in Figures 7e and 7f. Thus, a good agreement with the presented considerations is obtained.

5. CONCLUSIONS

A new switching voltage-to-current cell based on an FGMOS inverter has been proposed and analyzed. In particular, a stair-like PWL function generation by sizing FGMOS transistor gates has been described. One of the main advantages in using the proposed cell for the design of multiscroll

[1]Sprott JC, Rowlands G. Chaos Data Analyzer (http://sprott.physics.wisc.edu/cda.htm); Hegger R, Kantz H, Schreiber T. Nonlinear Time Series Analysis TISEAN (http://www.mpipks-dresden.mpg.de/~tisean).

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chaotic oscillators is the elimination of external references, in which this circuit is, to the best knowledge of the authors, the first on its category.

The circuit performance has been also analyzed, and it has been found to fulfill a set of design requirements. This can also be considered as a contribution because there are few works dealing with the integrated design of chaotic oscillators. In this field, nonlinear functions are set apart from the rest because of their many degrees of freedom, which makes its design a critical challenge. In this case, we achieve technology simulations (both before and after layout), which resemble clearly the theoretic system behavior.

The main objective has been the CMOS integrated design of multiscroll chaotic oscillators. Finally, from the results shown in Figure 7, we can conclude that our proposed voltage-to-current cell on the basis of FGMOS transistors can be very useful in the implementation of several multiscroll schemes.

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