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Characterization of RF-MOSFETs in Common-Source Configuration at Different Source-to-Bulk Voltages From S-Parameters

Fabián Zárate-Rincón, Germán A. Álvarez-Botero, Reydezel Torres-Torres, *Member, IEEE*, Roberto S. Murphy-Arteaga, *Senior Member, IEEE*, and Stefaan Decoutere

Abstract—Using a new test fixture that allows us to bias the bulk terminal through an additional compensated DC probe, a two-port S-measurement-based methodology to characterize RF-MOSFETs in common-source configuration is herein presented. In addition to obtaining S-parameters at different bulk-to-source voltages using a single two-port configured test-fixture, the proposal allows the analysis of the electrical parameters of a MOSFET that are influenced by the substrate effect when the frequency rises. Physically expected results are obtained for device's model parameters, allowing to accurately reproduce S-parameters up to 20 GHz. Furthermore, extracted parameters, such as threshold voltage, are in agreement with those obtained using well-established DC methods. This method allows one to characterize a four-terminal MOSFET from two-port small-signal measurements.

Index Terms—DC methods, physical parameters of MOSFET, RF-MOSFET, two-port S-parameter measurements.

I. INTRODUCTION

CHARACTERIZING and modeling the RF-MOSFET as a four-terminal device is mandatory to accurately represent the corresponding features when performing IC-design-oriented simulations. Although three- and four-port pad configurations can be used for this purpose to obtain the small-signal S-parameters of an RF-MOSFET [1]–[3], the multiport vector network analyzer (VNA) required to perform the associated measurements is still not available in many microwave laboratories. Based on this, much recent research has been limited to exploring the small-signal characteristics of the MOSFET as a two-port device in common source and bulk configuration [4]–[7], however, the bulk bias dependence of the model parameters cannot be determined. Alternatively, experimental two-port S-parameters can be used for multiport characterization by either measuring several devices (DUTs) in different configurations [8], or by performing multiple combinations of measurements on a single DUT [9]. Unfortunately,

in addition to the die space required for the extra structures, the accuracy of the renormalization algorithms associated with these approaches is strongly dependent on the knowledge of the loads used to terminate the remaining ports (i.e., those which are not connected to the VNA ports), which are frequency dependent and difficult to determine. An interesting solution was proposed in [10], where three ground-signal-ground (GSG) coplanar RF probes were used to measure on-wafer RF-MOSFETs (i.e., two probes connected to the VNA ports and a third one to terminate the bulk-to-ground pads with a 50- Ω load). Designing additional external circuitry is, however, required to bias the device and achieving matching conditions.

To provide an efficient alternative to characterize bulk-bias dependent effects in RF-MOSFETs through a two-port VNA, common source devices with a separate bulk DC bias pad are fabricated and measured on the basis of the methodology herein proposed. Thus, conventional two-port S-parameters are obtained using GSG coplanar probes and an additional DC probe with a power bypass capacitor for the bulk contact, which minimizes the associated series inductance and any noise or oscillation due to the bulk supply. Using these measurements, in addition to the MOSFET's small-signal model parameters that allow the analysis of the device's input, output, and direct/reverse transmission characteristics as the bulk-to-source voltage changes, the built-in potential, the bulk potential, and the threshold voltage are found directly from S-parameter measurements in a simple fashion, without requiring further either DC or CV measurements. This represents an advantage because RF-MOSFETs are typically configured for testing using GSG probes, avoiding further experiments once the S-parameters are measured.

II. EXPERIMENTS

To develop and verify the modeling and parameter extraction methodology proposed in this paper, a test fixture to probe a multifingered n-channel RF-MOSFET with length, $L_m = 80$ nm, finger width, $W_f = 3$ μ m, and 64 gate fingers in a common-source configuration is fabricated using an RF-CMOS process featuring a shallow trench isolation scheme. The test fixture includes a ground shield using the bottom metal layer available (i.e., level-1 metal), which is connected to the ground pads to correctly establish the ground reference and to isolate the pads from the substrate. All these pads, as well as

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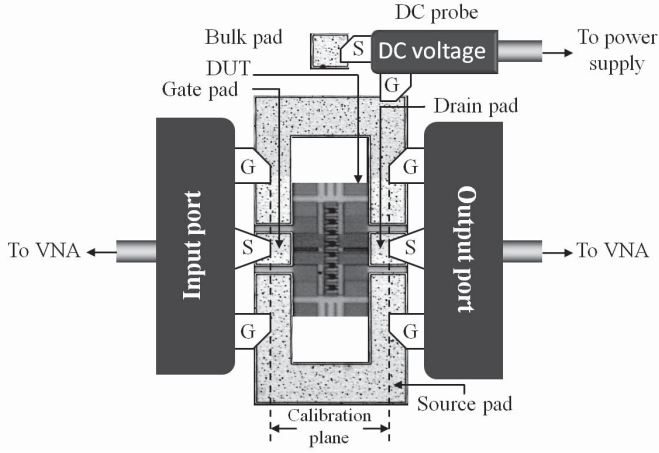


Fig. 1. Experimental assembly of the proposed test structure, illustrating the probes and the calibration plane.

the one used to bias the MOSFET bulk terminal, are made of aluminum at the level-3 metal. In addition, the device structure presents a separate bulk DC connection, a polysilicon/SiON gate, and a guard ring. Fig. 1 shows the fabricated structure illustrating that 150- μm pitch GSG probes can be used to collect two-port S-parameters using a VNA setup previously calibrated up to the RF-probe tips using an off-wafer line-reflect-match algorithm. The measurements are performed up to 20 GHz by applying a signal power of -20 dBm that guarantees small-signal operation while maintaining adequate signal-to-noise ratio for the applied RF measurement signals; the drain-to-source voltage (V_{ds}) was varied from 0.5 to 0.7 V, whereas the gate-to-source voltage (V_{gs}) from 0.55 to 0.65 V; these bias conditions cover the strong inversion and saturation regions. Nonetheless, for characterization purposes, measurements at $V_{ds} = V_{gs} = 0$ V (i.e., cold-FET conditions) are also performed.

The bulk-to-source voltage (V_{bs}) is varied from 0 V to -1.2 V using a DC quadrant needle probe from Cascade [11], whose design is based on a tungsten probe tip attached to a microstrip ceramic blade providing a minimized series inductance (L_{series}) of a few nanohenries, and including two bypass capacitors ($C_{bypass1} \approx 1$ μF and $C_{bypass2} \approx 100$ pF) to reduce the external parasitic impedance between the substrate and source terminals. Furthermore, the assumption that the DC probe does not affect the measurements is verified by observing no variations between two-port S-parameter measurements obtained when applying $V_{bs} = 0$ V, both using the DC probe and from a structure whose bulk and source are tied together (i.e., internally short-circuited), at least up to 20 GHz. On the other hand, it is also necessary to mention that the effect of the RF probing pads is de-embedded after measuring open and short dummy structures [12]. Using these measurements, the following methodology is developed and verified.

III. DETERMINATION OF THE SUBSTRATE PARAMETERS

Fig. 2 shows a simplified sketch of a MOSFET and its corresponding equivalent circuit model assuming the two-port configuration including the DC probe, used to measure the experimental S-parameters, where R_s and R_d are the series

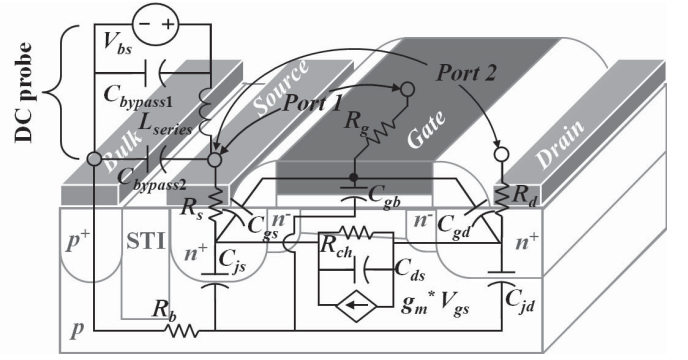


Fig. 2. Small-signal model for the RF-MOSFET, where $g_m^* = g_m e^{-j\omega\tau}$.

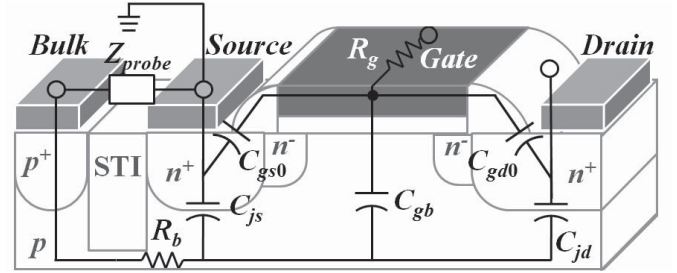


Fig. 3. Simplified model for the RF-MOSFET with $V_{gs} = V_{ds} = 0$ V, where Z_{probe} is the impedance of the DC probe tip.

parasitic resistances, R_{ch} is the channel resistance, R_g is the gate resistance, C_{ds} is the drain-source capacitance, C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, R_b is the substrate resistance, C_{js} and C_{jd} are the junction capacitances, and g_m is the transconductance. V_{bs} is considered to be applied by a simple voltage source, which is a reasonable assumption within the range of a few gigahertz, because the magnitude of the MOSFET substrate impedance is much higher than the parasitics introduced by the DC power supply, cables, and probe.

Firstly, the substrate elements are obtained at $V_{ds} = V_{gs} = 0$ V because this particular condition allows to simplify the equivalent circuit in Fig. 2 to that shown in Fig. 3. Here, the following expressions for the Y-parameters can be written [13], [14] as follows:

$$Y_{11} \approx \omega^2 R_g (2C_{gd0} + C_{gb})^2 + j\omega (2C_{gd0} + C_{gb}) \quad (1)$$

$$Y_{12} \approx -j\omega C_{gd0} \quad (2)$$

$$Y_{22} \approx \omega^2 R_b C_{jd}^2 + j\omega (C_{jd} + C_{gd0}). \quad (3)$$

The expressions (1) to (3) are obtained after considering that the effect of C_{js} is neglected by assuming $j/\omega C_{js} \parallel R_b \approx R_b$, which is valid up to some gigahertz as shown later in this paper, and $Z_{probe} \ll R_b$ was corroborated by means of the comparison of the experimental data between an RF-MOSFET with the DC probe tip placed on the bulk DC connection and one with tied source and bulk up to 20 GHz. Furthermore, in (1) the assumption $C_{gs0} \approx C_{gd0}$ is considered. Hence, at the frequencies at which (1)–(3) are valid, it is possible to obtain C_{jd} and C_{gd0} from the slopes of the linear regressions of the experimental $\text{Im}(Y_{22}) + \text{Im}(Y_{12})$ versus ω , and $-\text{Im}(Y_{12})$ versus ω , respectively; this procedure is illustrated in Fig. 4(a) and (b). Once C_{jd} and C_{gd0} are determined, linear regressions

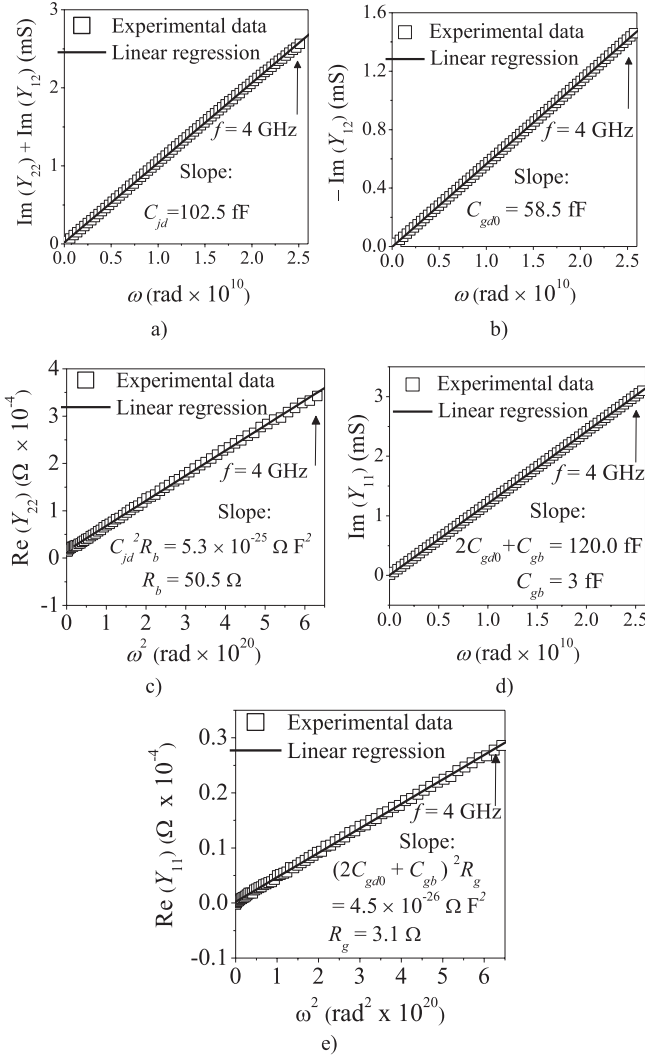


Fig. 4. Regressions to obtain. (a) C_{jd} , (b) C_{gd0} , (c) R_b , (d) C_{gb} , and (e) R_g at $V_{gs} = V_{bs} = V_{ds} = 0$ V.

of the $\text{Re}(Y_{22})$ versus ω^2 , $\text{Im}(Y_{11})$ versus ω , and $\text{Re}(Y_{11})$ versus ω^2 data are performed and then the values of R_b , C_{gb} , and R_g are extracted from the corresponding slopes; this is illustrated in Fig. 4(c)–(e). The good linearity observed in these data allows to verify the validity of (1)–(3) up to $f = 4$ GHz at $V_{gs} = V_{bs} = V_{ds} = 0$ V. Moreover, for the performed analysis, the extraction is repeated for different values of V_{bs} to observe the dependence of the substrate parameters on this voltage. If the substrate elements are obtained, then the corresponding effect is de-embedded from the experimental data, which allows for the determination of the remaining model parameters directly from Y -parameters.

As the frequency increases, the impedance associated with C_{js} becomes comparable with R_b , and (1) and (2) require including the corresponding effect. Thus, to express C_{js} in terms of two-port network parameters in a manageable way, the equivalent circuit associated with Y_{22} presented in Fig. 5 is used. In accordance with this circuit and considering

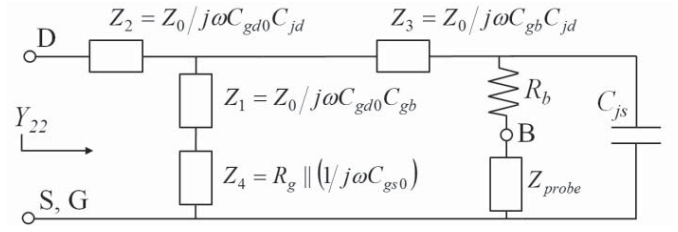


Fig. 5. Circuit for calculating Y_{22} at $V_{gs} = V_{ds} = 0$ V including C_{js} , where $Z_0 = (1/C_{gd0} + 1/C_{jd} + 1/C_{gb})^{-1}$, and Z_{probe} is the impedance of the DC probe tip.

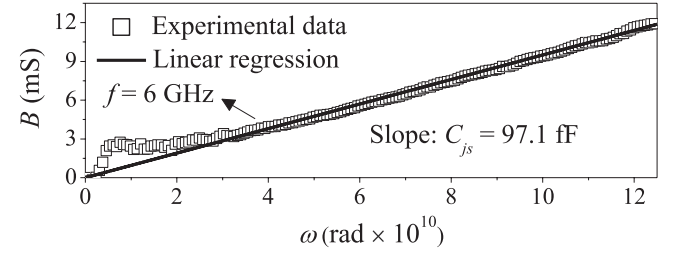


Fig. 6. Regression to obtain C_{js} at $V_{gs} = V_{bs} = V_{ds} = 0$ V.

$Z_{probe} \ll R_b$, the following parameter can be defined:

$$B = \text{Im} \left[\left(\left(\left(Y_{22}^{-1} + Z_2 \right)^{-1} - (Z_1 + Z_4)^{-1} \right)^{-1} - Z_3 \right)^{-1} \right] = \omega C_{js} \quad (4)$$

where B is the susceptance of C_{js} . Thus, while plotting B versus ω , C_{js} is obtained from the slope of the corresponding linear regression. Fig. 6 shows the excellent linearity of the experimentally determined data at $V_{bs} = V_{gs} = V_{ds} = 0$ V for frequencies > 6 GHz. Similar to the previously obtained parameters, C_{js} is extracted at different V_{bs} to analyze the corresponding dependence on this voltage.

After implementing the MOSFET equivalent circuit shown in Fig. 3, using the obtained parameters, SPICE simulations are performed and confronted with experimental data in Fig. 7. An additional simulation is performed removing C_{js} from the circuit. Fig. 7 shows the complex S_{22} , because this parameter is strongly influenced by the substrate components, which are of particular interest in the analysis presented here. Notice that a good model–experiment correlation is observed even ignoring C_{js} up to f around 8 GHz. This verifies the validity of the extractions performed in Fig. 4, where $f = 4$ GHz was the upper limit to perform the linear regressions. However, at higher frequencies the effect of C_{js} needs to be considered, and if incorporated into the model the simulation results are in better agreement with experimental data up to at least 20 GHz.

IV. DETERMINATION OF THE INTRINSIC CHANNEL RESISTANCE

Once the substrate parameters are determined as a function of V_{bs} , the intrinsic MOSFET parameters are to be obtained to establish correct small-signal models. R_{ch} is one of the most important MOSFET parameters of this type; thus, its corresponding extraction is shown hereafter.

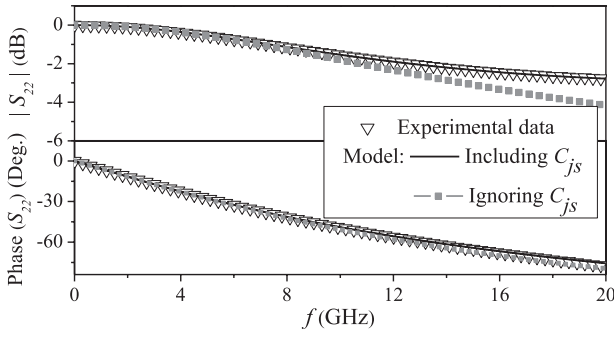


Fig. 7. Experiment-model correlation with and without C_{js} at $V_{gs} = V_{bs} = V_{ds} = 0$ V.

The small-signal channel resistance is strongly dependent on V_{bs} as it is closely related to the threshold voltage V_{th} . To determine the value of this resistance, the device is biased in strong inversion (i.e., the operation region where R_{ch} becomes apparent) and at $V_{ds} = 0$ V. Subsequently, the previously obtained substrate parameters R_b and C_{jd} are removed from the experimental data by means of the following equation that expresses the corrected Y -parameter matrix in strong inversion:

$$Y^* = Y - \begin{bmatrix} 0 & 0 \\ 0 & \frac{\omega^2 C_{jd}^2 R_b}{1 + \omega^2 C_{jd}^2 R_b^2} + j \frac{\omega C_{jd}}{1 + \omega^2 C_{jd}^2 R_b^2} \end{bmatrix} \quad (5)$$

where Y is the experimental Y -parameters in strong inversion including the substrate effects. Notice that (5) assumes that C_{jd} and R_b are independent of V_{gs} , which is a reasonable assumption even for multifingered devices [15]. In addition, C_{js} is not considered in this particular formulation because at $V_{gs} > V_{th}$ the source series resistance is much smaller than the reactance associated with this capacitance at the frequencies studied in this paper. When Y^* is transformed to Z -parameters, the following equation can be written [16]:

$$-\omega (\text{Im}(Z_{22}^*))^{-1} = C_x \omega^2 + (R_{ch}^2 C_x)^{-1} \quad (6)$$

with $C_x = C_{ds} + C_{gs} C_{gd} / (C_{gs} + C_{gd})$. From (6), C_x and R_{ch} can be extracted from the slope and intercept of a linear regression, as shown in Fig. 8.

Finally, the resistances R_s and R_d are given by

$$R_s = \text{Re}(Z_{12}^*) - \frac{1}{2} \frac{R_{ch}}{1 + (\omega R_{ch} C_x)^2} \quad (7)$$

$$R_d = \text{Re}(Z_{22}^*) - R_s - \frac{R_{ch}}{1 + (\omega R_{ch} C_x)^2}. \quad (8)$$

V. INFLUENCE OF V_{bs} ON MODEL PARAMETERS

Using the preceding procedure, several parameters were obtained as a function of V_{bs} . Fig. 9 shows the V_{bs} -dependent junction capacitances and substrate resistance. These curves present the physically expected form, as explained below. For R_b , as the magnitude of V_{bs} is increased, the effective volume is decreased (the effective volume refers to the volume of the substrate, in which the substrate current I_b flows, minus the volume of the depletion region). This behavior increases the

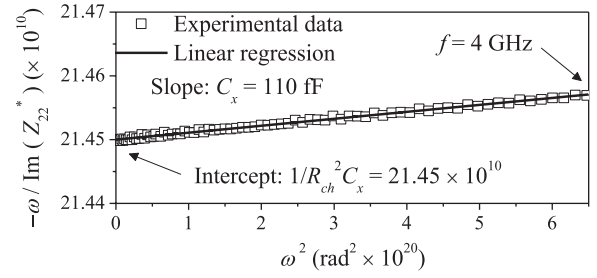


Fig. 8. Regression to obtain C_x and R_{ch} at $V_{gs} = 0.55$ V, $V_{bs} = -1$ V, and $V_{ds} = 0$ V.

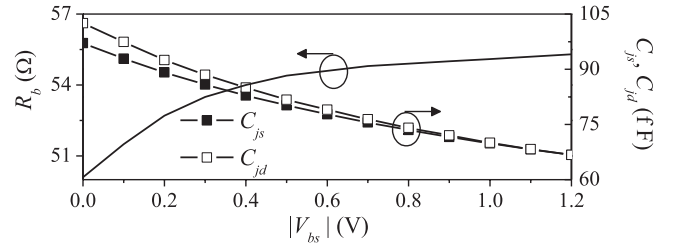


Fig. 9. Experimentally obtained R_b , C_{js} , and C_{jd} versus V_{bs} at $V_{gs} = V_{ds} = 0$ V.

value of the effective substrate resistance. R_b increases from 50.1 to 55.3 Ω while the magnitude of V_{bs} changes from 0 to -1.2 V. On the other hand, for C_{js} and C_{jd} , the variation with V_{bs} is that predicted by the equation for a junction capacitance, which is corroborated in the following way.

Because the source-to-substrate and the drain-to-substrate junctions are abrupt, C_{js} and C_{jd} vary with the inverse of the square root of the applied voltage (i.e., V_{bs}), which is the trend observed in Fig. 9. To verify this bias-dependence for the extracted capacitances, the well-known equation for an abrupt junction capacitance is written for C_{jd} (a similar equation can be written for C_{js}) as

$$1/C_{jd}^2 = 2(\psi_{bi,d} - 2V_T - V_{bs})/q\epsilon_s N_A A_d^2 \quad (9)$$

where q is the electron's charge, ϵ_s is the permittivity of silicon, N_A is the dopant concentration in the substrate, A_d is the junction area, V_T is the thermal voltage, and $\psi_{bi,d}$ is the built-in potential at the drain. In Fig. 10, the experimental $1/C_{jd}^2$ versus V_{bs} curve presents the linear trend that is in agreement with the theoretical variation of this parameter. Thus, ψ_{bi} can be found from a simple linear regression; for the drain junction $\psi_{bi,d} = 0.95$ V, whereas for the source junction $\psi_{bi,s} = 1.12$ V. It is noteworthy that the extraction of these parameters is completely determined from S-parameters and is equivalent to values obtained from DC measurements, as will be verified in the following.

On the other hand, the dependence of the resistances R_d and R_s with the bulk-source voltage V_{bs} for different values of V_{gs} is shown in Fig. 11. The resistances R_d and R_s decrease either when the magnitude of V_{bs} is made smaller or V_{gs} is made higher; similarly, this behavior occurs in the case of R_{ch} . This is due to the increase of the depletion region induced by V_{bs} and to the injection of minority carriers from the substrate to the LDD regions because of V_{gs} .

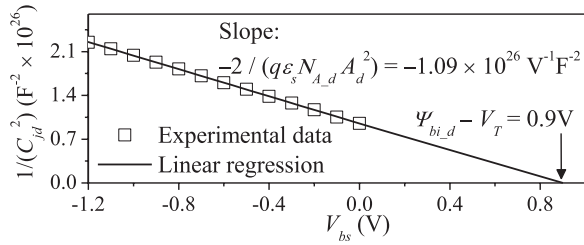
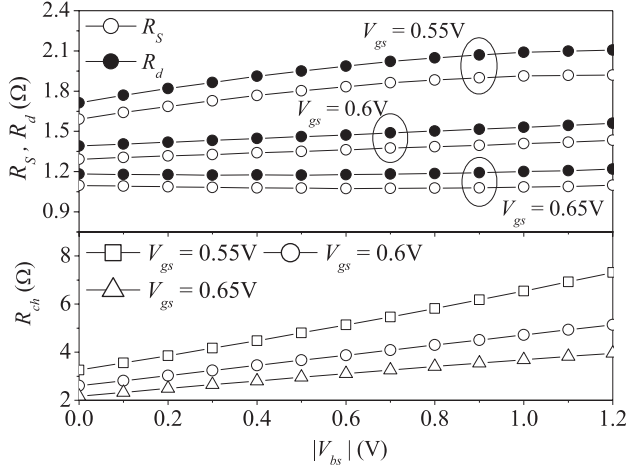


Fig. 10. Data linearization for the junction capacitance data.

Fig. 11. R_s , R_d , and R_{ch} against V_{bs} for different values of V_{gs} at $V_{ds} = 0$ V.

V_{th} is then found by performing a linear fitting of the inverse of R_{ch} obtained from RF measurements versus V_{gs} , as shown in Fig. 12; in this case, $1/R_{ch}$ can be estimated from

$$\begin{aligned} 1/R_{ch} &= \beta(V_{gs} - V_t) \\ &= (\mu_{\text{eff}} C_{OX} W_{\text{eff}}/L_{\text{eff}}) \times (V_{gs} - V_t) \end{aligned} \quad (10)$$

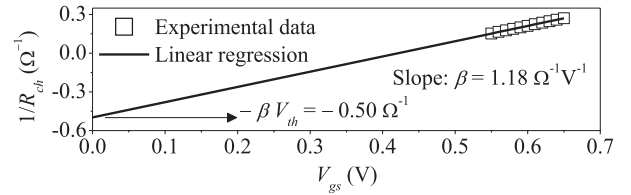
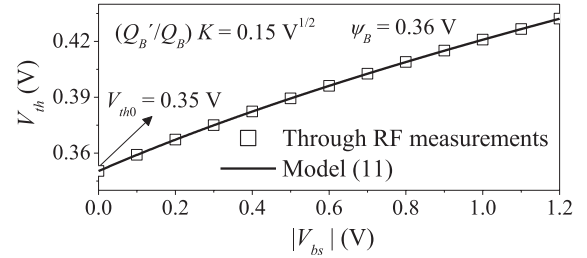
where μ_{eff} is the effective mobility, C_{OX} is the oxide capacitance per unit area, W_{eff} is the effective channel width, and L_{eff} is the effective channel length. Although μ_{eff} and L_{eff} depend on V_{gs} , these parameters can be assumed constant for small variations of gate bias. Fig. 12 shows the good linearity of the experimental $1/R_{ch}$ versus V_{gs} data. Subsequently, to implement a model for the threshold voltage, the following equation is used:

$$V_{th} = V_{th0} + (Q'_B/Q_B) \times K \left(\sqrt{2\psi_B - V_{bs}} - \sqrt{2\psi_B} \right) \quad (11)$$

$$K = \sqrt{2\epsilon_s q N_A}/C_{OX} \quad (12)$$

where V_{th0} is the threshold voltage when $V_{bs} = 0$ V, K is the body bias coefficient, Q'_B and Q_B are the depletion regions considering and neglecting the short channel effects. Thus, V_{th0} can be extracted from the intercept of the V_{th} versus V_{bs} curve shown in Fig. 13. Then, K and ψ_B are obtained by fitting this curve. Thus, the bulk potential ψ_B is found to be 0.36 V, whereas $V_{th0} = 0.35$ V.

After characterizing the RF-MOSFET with a separate terminal for the substrate through RF measurements, it is necessary to compare these results with those obtained from the classical DC methods. It should be noted, however, that the

Fig. 12. Determination of β and V_{th} at $V_{bs} = -1$ V; $V_{ds} = 0$ V.Fig. 13. Fitting of the V_{th} obtained from RF measurements.

V_{th} extraction methodology in RF is performed in the linear region with $V_{ds} = 0$ V, varying V_{bs} and injecting an RF signal of a given frequency in the output and input ports. Thus, the comparison should be made with DC methods that are valid in this operation region of the MOSFET, such as extrapolation in the linear region (ELR), second derivative (SD), and second derivative of the logarithm (SDL) of the drain current [17]. In the ELR method, a line tangent to the point of maximum slope of the I_d against V_g curve, corresponding to the maximum transconductance, is drawn; thus, V_{th} is the intercept in the abscissa. In SD, V_{th} is defined as the gate voltage when the derivative of the transconductance is a maximum. Furthermore, the SDL method determines V_{th} from the gate voltage at which the SDL of I_d presents a minimum value; this occurs when the drift and diffusion currents are equal to each other. In addition, SDL is developed to avoid the dependence on the parasitic series resistance [17]; this represents an advantage over the others.

Fig. 14 shows the comparison of the threshold voltage V_{th} as a function of substrate voltage V_{bs} between this RF method and some DC methods, which are ELR, SD, and SDL. It is evident that the threshold voltage values, obtained from RF measurements, are within the variation range of the considered DC extraction methods. It is important to note that the SDL method shows a similar behavior to that obtained from the RF method.

In the RF method, V_{th} is found by extrapolation of the graph of $1/R_{ch}$ as a function of V_{gs} . In turn, R_{ch} is determined from the Z-parameters of the imaginary part of the output port Z_{22}^* , in which the effects due to the parasitic series resistance that affects only the real part of Z_{22}^* are not apparent. In Z_{22}^* , substrate parasitic elements are removed from the experimental data. In contrast, SDL-based V_{th} extraction is less sensitive than others to changes in the parasitic series resistance. For this reason, both SDL and the RF method herein presented show a similar accuracy.

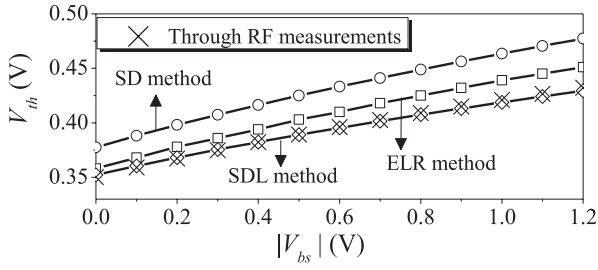


Fig. 14. Comparison of the threshold voltage V_{th} between the RF method and DC methods.

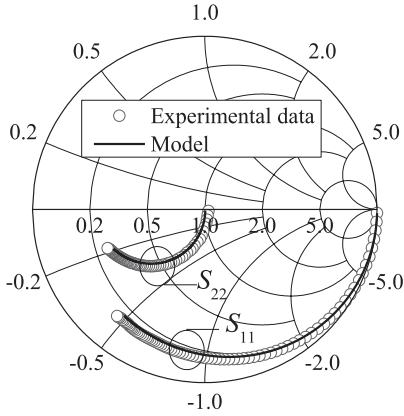


Fig. 15. Experiment-model correlation up to 20 GHz for S_{11} and S_{22} at $V_{gs} = 0.6$ V, $V_{bs} = -1$ V, and $V_{ds} = 0.7$ V.

VI. VALIDITY OF THE MODEL IN THE ACTIVE REGION

The operation of the transistor is discussed at $V_{ds} = 0$ V. Therefore, the effect associated with the transconductance g_m could be neglected. Accordingly, it is noted that S_{21} is equal to S_{12} . For practical applications, the transistor is, however, biased in strong inversion under different values of V_{ds} . Thus, the comparison between the experimental data and the model for the transistor in the active region is mandatory for which V_{ds} was fixed at three different values, 0.5, 0.6, and 0.7 V. In addition, a gate voltage V_{gs} of 0.6 V is considered to insure operation in strong inversion, varying V_{bs} from -1.2 V to 0 V in steps of 0.1 V. To extract the small-signal equivalent circuit elements, the procedure given in [18] is followed. Accordingly, the intrinsic parameters of the RF-MOSFET, C_{gs} , C_{gd} , C_{ds} , g_m , and R_{ch} , can be obtained through linear regressions up to 4 GHz, the range for which C_{js} can be neglected, after removing the effects of the parasitic substrate network and the parasitic resistances. This procedure, briefly described, is repeated for different V_{bs} and V_{ds} bias conditions. Figs. 15 and 16 show the comparison between simulated and measured S-parameters up to 20 GHz at $V_{gs} = 0.6$ V, $V_{bs} = -1$ V, and $V_{ds} = 0.7$ V, observing that the model fits very well the experimental data. Additionally, the phase delay τ , which is related to the reduction of the complex transconductance at high frequencies, is extracted from the regression of the experimental data, as shown in Fig. 17 [18].

Furthermore, the dependence of g_m with V_{bs} for different values of V_{ds} is shown in Fig. 18. Thus, g_m becomes smaller when the magnitude of V_{bs} increases or V_{ds} decreases. These behaviors are due to the increase of the depletion region at

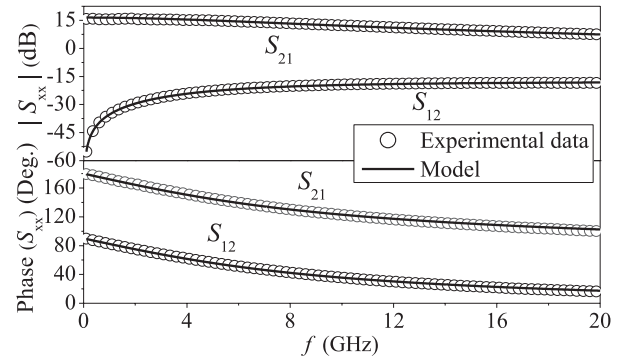


Fig. 16. Experiment-model correlation for S_{12} and S_{21} at $V_{gs} = 0.6$ V, $V_{bs} = -1$ V, and $V_{ds} = 0.7$ V.

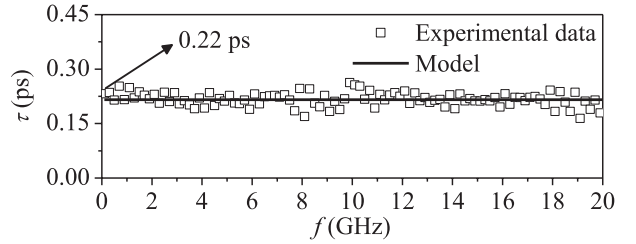


Fig. 17. Regression to obtain τ at $V_{gs} = 0.6$ V, $V_{bs} = -1$ V, and $V_{ds} = 0.7$ V.

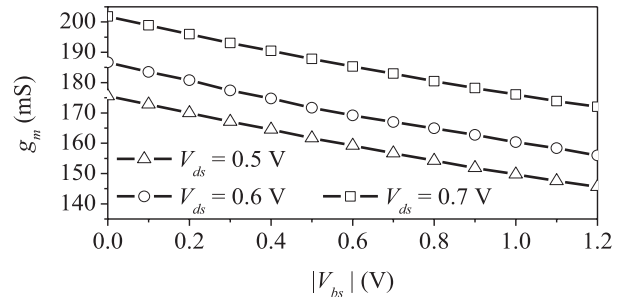


Fig. 18. g_m against $|V_{bs}|$ for different values of V_{ds} at $V_{gs} = 0.6$ V.

source and drain with V_{bs} and of the electric field in the horizontal direction because of V_{ds} .

VII. CONCLUSION

A method to extract physical MOSFET parameters from high-frequency measurements, and fully characterize the device for operation in this regime was outlined. The principal advantage of the method is that many important parameters, which are generally extracted from DC measurements, such as the built-in potential, the threshold voltage, the bulk potential, the body bias coefficient, and the transconductance, can also be determined using this procedure. The procedure requires that the device have an independent Bulk terminal, which can be biased arbitrarily. Thus, two-port S-parameter measurements were sufficient to extract the values for all the elements. This assertion was demonstrated by confronting the results with those obtained from DC methods. Furthermore, the proposed methodology was validated by the good fitting of the experimental data compared with simulations. Finally, it was shown that the parameters obtained using the proposed

method, can correctly reproduce not only experimental data at high frequency, but also at DC.

REFERENCES

- [1] J. Brinkhoff, S. C. Rustagi, J. Shi, and F. Lin, "MOSFET model extraction using 50GHz four-port measurements," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2007, pp. 647–650.
- [2] J. Brinkhoff, A. Issaoun, S. C. Rustagi, and F. Lin, "Multiport thru deembedding for MOSFET characterization," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 923–926, Aug. 2008.
- [3] U. Mahalingam, S. C. Rustagi, and G. S. Samudra, "Three-port RF characterization of MOS transistors," in *Proc. ARFTG Conf. Dig.*, Jun. 2005, pp. 56–61.
- [4] L. Negre, D. Roy, F. Cacho, S. Boret, P. Scheer, S. Jan, D. Gloria, and G. Ghibaudo, "Reliability characterization and modeling solution to predict aging of 40-nm MOSFET DC and RF performances induced by RF stresses," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1075–1083, May 2012.
- [5] J. Y. Kim, B. H. Ko, M. K. Choi, and S. Lee, "RF extraction method for source/drain overlap and depletion length of deep-submicron RF MOSFETs using intrinsic gate-bulk capacitance," *Electron. Lett.*, vol. 46, no. 23, pp. 1566–1568, Nov. 2010.
- [6] S. Lee and H. K. Yu, "A new technique to extract channel mobility in submicron MOSFETs using inversion charge slope obtained from measured S-parameters," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 784–788, Apr. 2001.
- [7] K. Bertling, A. D. Rakic, Y. T. Yeow, A. Brawley, H. Domyo, and F. M. Rotella, "Comparison of SOS MOSFET's equivalent circuit parameters extracted from LCR meter and VNA measurement," *IEEE Trans. Electron Devices*, vol. 59, no. 1, pp. 20–25, Jan. 2012.
- [8] A. Jha, J. M. Vasi, S. C. Rustagi, and M. B. Patil, "A novel method to obtain 3-port network parameters from 2-port measurements," in *Proc. IEEE Conf. Microelectron. Test Struct.*, vol. 17, Mar. 2004, pp. 57–62.
- [9] D. G. Kam and J. Kim, "Multiport measurement method using a two-port network analyzer with remaining ports unterminated," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 9, pp. 694–696, Sep. 2007.
- [10] M. T. Yang, Y. J. Wang, T. J. Yeh, P. C. Ho, Y. T. Chia, and K. L. Young, "Characterization and model of 4-terminal RF CMOS with bulk effect," in *Proc. IEEE Conf. Microelectron. Test Struct.*, vol. 17, Mar. 2004, pp. 189–193.
- [11] (2013). *Probe Selection Guide*, Cascade Microtech, Inc., Beaverton, OR, USA [Online]. Available: <http://www.cmicro.com/files/Probe-Selection-Guide.pdf>
- [12] R. Torres-Torres, R. S. Murphy-Arteaga, and J. A. Reynoso-Hernandez, "Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS," *Trans. Electron Devices*, vol. 52, no. 7, pp. 1335–1342, 2005.
- [13] J. Han, M. Je, and H. Shin, "A simple and accurate method for extracting substrate resistance of RF MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 434–436, Jul. 2002.
- [14] D. G. Kam and J. Kim, "Extraction of substrate resistance in bulk FinFETs through RF modeling," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 5, pp. 358–360, May 2007.
- [15] J. H. Jung and J. H. Lee, "Extraction of substrate resistance in multi-finger bulk FinFETs using shorted source/drain configuration," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 1335–1342, Sep. 2007.
- [16] E. Torres-Rios, R. Torres-Torres, G. Valdovinos-Fierro, and E. Gutiérrez, "A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from S-parameters," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 571–573, Mar. 2006.
- [17] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, A. Terán Barrios, J. J. Liou, and C. S. Ho, "Revisiting MOSFET threshold voltage extraction methods," *Microelectron. Rel.*, vol. 53, no. 1, pp. 90–104, Jan. 2013.
- [18] R. Torres-Torres and R. Murphy-Arteaga, "Straightforward determination of small-signal model parameters for bulk RF-MOSFETs," in *Proc. 5th IEEE Int. Caracas Conf. Devices, Circuits Syst.*, Nov. 2004, pp. 14–18.

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