# Fully-Integrated Low-Noise CMOS Chopper Amplifiers for Portable Sensor Systems.

by

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# Resumen

Los preamplificadores son bloques fundamentales en los sistemas de acondicionamiento de señal. En el caso particular del acondicionamiento de señales provenientes de sensores, la amplitud de las señales es usualmente del orden de $mV$ o incluso $\mu V$, de modo que el ruido del preamplificador es un factor crítico que puede limitar la resolución del sistema del sensor. Muchos sensores llevan información a baja frecuencias, incluso cerca del DC, por lo cual, el offset y el ruido de baja frecuencia (ruido flicker) de los preamplificadores limitan la precisión del sistema de acondicionamiento de la señal.

En esta Tesis se propusieron, fabricaron y caracterizaron sistemas de acondicionamiento de señal de bajo ruido flicker, basados en la técnica dinámica de cancelación chopping. Para ello, se propusieron amplificadores de voltaje de ganancia variable con baja contribución de ruido flicker y bajo consumo de potencia. Se propuso además un escalador de impedancia basado en la técnica de bootstrapping, el cual permite generar impedancias flotantes sin degradar la linealidad del circuito y con una contribución de ruido despreciable frente a la del resto del circuito. Adicionalmente, se propuso un circuito de reducción de transconductancia basado en la técnica de bootstrapping para la implementación de transconductores para filtros de tiempo-continuo con baja frecuencia de corte mediante la técnica Gm-C. Finalmente se implementaron amplificadores chopper para el acondicionamiento de señales empleando los preamplificadores propuestos como bloque central, modulación en la entrada y la salida, y filtrado mediante los filtros Gm-C de baja frecuencia.

Todas las topologías fueron diseñadas y fabricadas en una tecnología CMOS de $0.18\mu m$, y los resultados experimentales muestran un ruido referido a la entrada integrado por debajo de $1.5\mu V_{rms}$ con un ancho de banda de $1kHz$ y consumo de potencia en el orden de decenas de $\mu W$, alcanzando figuras de eficiencia de ruido y de potencia (NEF y PEF) por debajo de 5 y 45 V, respectivamente.

# List of Acronyms

$C_{ox}$ - Oxide Capacitance

$\eta$ - Enhancement gain

$f$ - Frequency

$G_m$ - Transconductance

$k$ - Boltzmann Constant

$K_f$ - Flicker Noise Constant

$\mu$ - Mobility

$L$ - Length

$T$ - Temperature

$W$ - Width

**ADC** - Analog to Digital Converter

**BW** - Bandwidth

**ChA** - Chopper Amplifier

**CLK** - Clock

**CMOS** - Complementary Metal-Oxide Semiconductor

**CMFB** - Common Mode Feedback

**CMRR** - Common Mode Rejection Ratio

**DR** - Dynamic Range

**DUT** - Device Under Test

**FOM** - Figure of Merit

**FVF** - Flipped Voltage Follower

**LIA** - Low-In Amplifier

**LGmOTA** - Low-Transconductance Operational Amplifier Transconductor

**LNP** - Low-Noise Preamplifier

**LPF** - Low-Pass Filter

**MOSFET** - Metal-Oxide Semiconductor Field Effect Transistor

**NA** - Normalized Area

**NP** - Normalized Power

**NAND** - Not-And Gate

**NEF** - Noise Efficiency Factor

**NMOS** - Negative-channel Metal-Oxide Semiconductor

**OTA** - Operational Amplifier Transconductance

**PR** - Pseudo-Resistor

**PPF** - Partial Positive Feedback

**PEF** - Power Efficiency Factor

**PMOS** - Positive-channel Metal-Oxide Semiconductor

**PSD** - Power Spectral Density

**PSRR** - Power Supply Rejection Ratio

**PSS** - Periodic Steady State

**RC** - Resistor-Capacitor

**SC** - Switched Capacitor

**SSF** - Super-Source Follower

**THD** - Total Harmonic Distortion

**VNA** - Vector Network Analyzer

**VGLNP** - Variable Gain Low-Noise Preamplifier

# Contents

# List of Figures

# List of Tables

# Chapter 1

# Introduction

The use of wireless sensors has opened countless applications in almost all fields, from industry and science, to entertainment, household and security. For example, some applications are infrastructure health monitoring, medical diagnosis or detection of environmental pollutants [1-9]. In infrastructure monitoring, wireless sensors make it possible to optimize energy distribution by establishing large occupancy patterns [4-5]. For medical diagnostics, it is possible to implant wireless sensors to monitor biological potentials, which contain physiological and pathological information [6-9]. All these applications are possible thanks to the development of sensors, i.e., devices which detect different types of signals (physical, chemical or biological) and respond in the form of an electrical signal, such as current or voltage. Sensors can be classified into different types according to their application, conversion mechanism or type of input signal [1-3, 10].

The arrival of low-cost portable sensors has made it possible to monitor almost any biological, physical or chemical variable. As a result, the realization of signal preprocessing systems has become a major challenge, as they must comply with strict requirements not to degrade the performance of the whole portable system. Low noise and high dynamic range amplifiers are required, which must furthermore be supplied with low voltage compatible with battery operation, low power consumption and reduced area to ensure portability [11-23]. Reducing the area reduces the size and weight of the sensing systems, whereas low power consumption is essential to increase the useful life of the battery. However, it is difficult to combine all these characteristics, as there are several trade-offs in the design of integrated circuits, specially between noise, area and power consumption [12,14,20].

## 1.1 Sensor Signal Conditioning

Figure 1.1 shows a typical signal acquisition system. Amplification is necessary to provide gain for low-range sensor outputs [25]. The analog front-end of an interface circuit connected directly to the sensing element has to transform the raw sensor signal into a signal suitable to be processed by the subsequent A/D converter. The preamplifier functions are normally limited to amplification and filtering, leaving more complex signal processing tasks to the digital section [26]. DC offset and flicker noise may degrade the dynamic range ($DR$) of the preamplifier, as they limit the resolution of the processing chain. Therefore, noise becomes a critical factor, determining the system performance [29], and the first stage at the front of the sensor node, after the sensor itself, must be a low intrinsic noise amplifier [27-28].

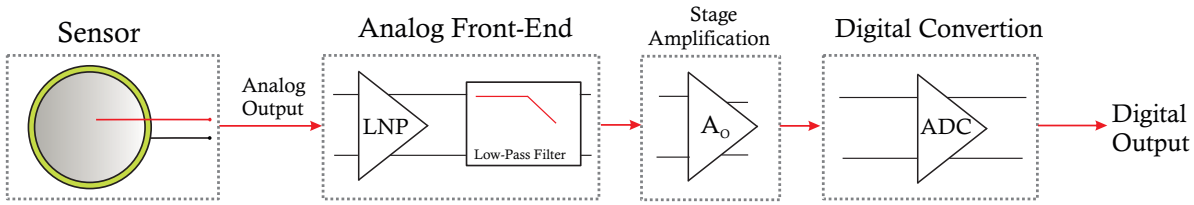


Figure 1.1: Block Diagram of a Signal Acquisition System.

As a first step to design low-noise signal conditioning circuits, it is necessary to know the sources of noise in integrated circuits, which will be presented in Chapter 2. Since the output of the sensors is normally a low frequency signal, the noise source that limits the dynamic range of the front-end amplifier is flicker noise. There are two different approaches to reduce flicker noise. The first approach is through circuit topology and transistor sizing, and can be to amplify signals of at least tens of microvolts. These amplifiers will be called low-noise preamplifiers (LNPs) in this Thesis. The second method is the use of dynamic offset cancellation techniques, which can be classified into two groups: auto-zero and chopping [30-32]. The auto-zero technique consists in first sampling and then subtracting the offset with low frequency components of the amplifier, but undersampling of the broadband noise results in an increased thermal noise contribution. The chopping technique, in turn, is a continuous time modulation technique in which the signal is translated to higher frequency, amplified and demodulated back to base-band, whereas the flicker noise is only modulated once and then filtered. As there is no noise undersampling, the residual noise is lower than with the auto-zero technique [33]. This

technique is used in analog front-ends, as shown in Figure 1.2, for input signals lower than tens of microvolts.

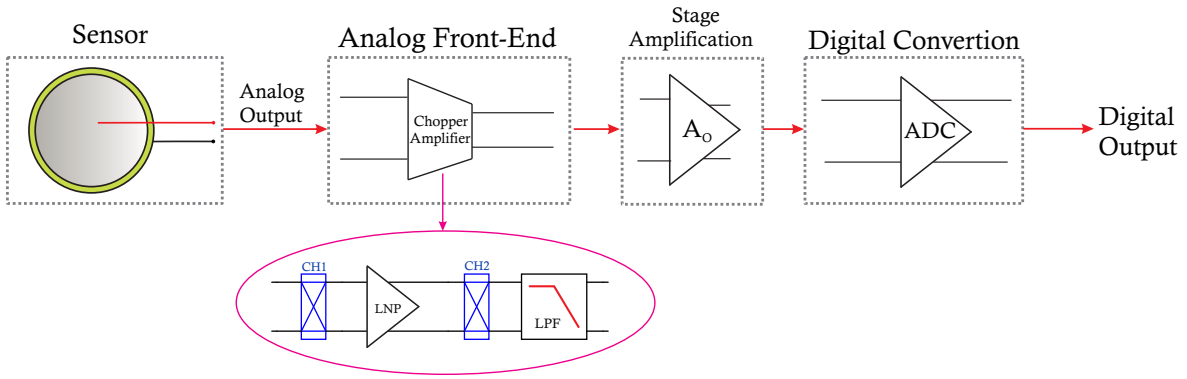


Figure 1.2: Block Diagram of a Signal Acquisition System with Chopper Amplifier.

The residual offset is a problem introduced by switches in chopping amplifiers due to charge injection and it is proportional to the chopping frequency ($f_{ch}$), so the residual offset can be decreased by reducing this frequency. However, to avoid aliasing in the signal, and to completely eliminate the low frequency noise, the chopping frequency can not be lower than the corner frequency $f_c$, i.e., the frequency at which the flicker noise is not predominant, and thermal noise becomes predominant. To further reduce the residual offset, the nested-chopper technique is proposed in [34], where the modulation-demodulation is applied twice at two different chopping frequencies, $f_{HIGH}$ and $f_{LOW}$. In this way, the residual offset can be reduced by a factor $f_{HIGH}/f_{LOW}$. As only an extra pair of modulators and a low-frequency control circuit are required, there is no significant increase in area and power consumption [34].

Another approach is the stabilized-chopper, which consists of two paths: a main signal path, that provides a large bandwidth, and an auxiliary path with high gain, where the chopping technique is applied to reduce flicker noise [35,38-39]. This technique provides high bandwidth and high gain at the cost of area and power consumption due to the use of the additional blocks.

This Thesis is devoted to the design of low-noise preamplifiers and low-frequency low-pass filters (LPFs) as the main blocks of the analog front-end, in particular of chopper amplifiers (Figure 1.2). Although the proposed LNPs and LPFs can be used in more complex chopping configurations to obtain higher resolution front-ends, such

as the above mentioned nested-chopper and stabilized-chopper, for the purpose of this Thesis the basic chopper amplifiers will be used as a proof of concept.

In order to characterize both the LNPs and the chopping amplifiers, there are two main figures of merit. The trade-off between the input-referred noise and the power consumption of the front-end amplifiers is usually expressed in terms of the noise efficiency factor ($NEF$) [42], defined as:

$$NEF = V_{ni,rms} \cdot \sqrt{\frac{2 \cdot I_{total}}{\pi \cdot 4kT \cdot V_t \cdot BW}} \tag{1.1.1}$$

where $V_{ni,rms}$ is the input-referred noise voltage integrated in the bandwidth $BW$ of the preamplifier, $I_{total}$ is the current consumption, $V_t$ is the thermal voltage, $k$ is the Boltzmann constant and $T$ is the temperature. Another figure of merit used to compare the design of amplifiers operating with different supply voltages is the power efficiency factor ($PEF$), defined as $NEF^2 \cdot V_{DD}$. The smaller the $NEF$ and $PEF$, the better the trade-off between noise and power consumption.

## 1.2 Objectives

The goal of this Thesis is to design low noise signal conditioning circuits in $0.18\mu m$ CMOS process standard technology. In particular, the main focus of this Thesis is the design of low-noise preamplifiers and low-frequency low-pass filters, as the main building blocks of analog-front ends with dynamic noise cancellation. The proposed chopping amplifiers will therefore be fully integrated, including the amplification stage, modulation/demodulation and filtering stage.

The particular objectives of this Thesis are:

- Design of voltage preamplifiers by analyzing and reducing the noise contribution of the devices not only through large sizing, but also through topology modifications.
- Implementation of fully integrated Gm-C low-pass filters with low cut-off frequency, in particular taking advantage of a novel proposed bootstrapping technique to reduce the cut-off frequency in a range from hundreds of $Hz$ to tens of $kHz$.
- Combination of the above presented blocks to design low-noise chopping amplifiers, with moderate power consumption to achieve competitive noise and power efficiency

factors.

## 1.3 Thesis Organization

This Thesis is organized in five chapters and two appendixes.

In this first Chapter a general overview of the signal acquisition circuits for portable sensing systems, as well as the objectives of the Thesis, are presented.

Chapter 2 is focused on the design of different low-noise preamplifiers that use transconductors as their core block. The first one, a flipped voltage follower (FVF) preamplifier, shows compactness with high linearity. Then, several Variable Gain Low-Noise Preamplifiers (VGLNPs) with low-power consumption, high-gain and low input-referred noise are proposed, using a novel impedance scaler based on the bootstrapping technique. All proposed architectures use source degeneration to improve linearity and achieve a well-defined gain. Simulation results are presented in order to validate every design in this Chapter, as well as experimental results of the integrated prototypes, which correspond to the best performance (low power-consumption with low-noise) proposals.

Chapter 3 treats with the implementation of low frequency Gm-C filters. First, a novel pseudo-differential low-transconductance amplifier is proposed based on the bootstrapping technique, which shows very low transconductance without the need for large passive components. Next, three low Gm transconductors are presented, which are then used to design three different Gm-C filters with low cut-off frequency and low power consumption. Finally, simulation results of all Low-Pass Filter are presented, as well as experimental results of the integrated prototypes, which were chosen to be the most power efficient with the lowest cut-off frequency.

In Chapter 4, three novel chopper amplifiers are implemented, using the circuits proposed in Chapter 2 and 3, as well as the modulator blocks and the non-overlapping clock signal generator. Simulation results are presented in order to validate every design in this Chapter, as well as experimental results of the integrated prototypes.

Chapter 5 provides a compilation of the results and conclusions of this Thesis, as well as some research directions that could be further studied in the future.

Appendix A shows the noise analysis carried out to determine the impact of intrinsic contributions of the preamplifiers proposed and it provides the information needed to perform periodic steady state (PSS) simulations. Finally, Appendix B details the experimental setup used for the characterization of the integrated prototypes.

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# Chapter 2

# Low-Noise Preamplifiers

Preamplifiers are fundamental building blocks in sensor signal conditioning, as they primarily determine the performance of the whole acquisition system. They are required to amplify, with a well-defined gain, very weak differential signals, with minimum power consumption. High common-mode rejection ratio (CMRR) and high power supply rejection ratio (PSRR) are also necessary to attenuate environmental interference [1-6]. In this Thesis, we will refer to preamplifiers as compact and moderately linear low-noise structures with low power consumption, which will be used as the constitutive building block for the implementation of chopping amplifiers to further reduce noise contribution and thus increase the resolution of the signal conditioning system [4-6]. The proposed low-noise preamplifiers have been designed using appropriate topologies and transistor sizing, so they are competitive in the current state of art.

Based on these considerations, the low-noise preamplifier design specifications can be summarized as follows:

- Fully Differential stage in order to increase noise immunity.
- $40dB$ gain or higher to ensure that the noise of the entire system is determined by this stage.
- Total harmonic distortion below $-40dB$ for $1mVpp$ input-voltage amplitude to ensure good linearity.
- A bias current in the order of a few tens of $\mu A$ to ensure low power consumption.

According to these requirements, this Chapter presents several low noise preamplifiers based on a voltage-current conversion at the input and current-voltage conversion at

the output. First, a summary of the main noise sources in an electronic system are presented. Next, a novel bootstrapping technique for the implementation of an impedance scaler, which will be used in most of the proposals, is presented. The proposed low-noise preamplifiers make use of PMOS transistors at the input, large area transistors and proper topologies to reduce flicker noise. Simulation results of each proposed preamplifier are presented and experimental measurements are shown in the case of the configurations that were fabricated, which showed the best trade-off between gain, noise and power consumption. Finally, the proposed topologies are compared with each other, and with other implementations found in the literature in order to highlight the advantages and disadvantages of each proposal. All proposed low-noise preamplifiers were designed and implemented in a $0.18\mu m$ CMOS standard process with $1.8V$ supply voltage.

## 2.1 Electronic Noise

Noise is an electrical disturbance that interferes in the transmission, acquisition or processing of signals, that is, it is a component of unwanted voltage or current. Noise limits the minimum signal level that a circuit can process with acceptable quality, and its study allows the development of mathematical models to determine its effects on the performance of circuits and/or electronic systems and to propose strategies to reduce such effects [7].

There are two types of noise: intrinsic and extrinsic. The first is generated in the devices as a consequence of their physical nature and is random; the second is generated as a result of the electrical or magnetic interaction between the circuit and the outside, or between different parts of the circuit itself, and can be periodic, intermittent or random in nature. The development of this work will focus on intrinsic noise reduction. It is possible to identify different fundamental noise mechanisms [7-9]:

- Thermal noise is generated by the random movement of charge carriers. It does not depend on the presence or absence of a direct current, so it is independent of biasing. Because it originates from the thermal excitation of the carriers, it is directly associated with absolute temperature. Thermal noise has a flat spectral density, so it is classified as white noise.

- Shot noise occurs in PN junctions. It also exhibits a flat spectral density and is caused by the individual flow of carriers when the bias current in DC experiences

current pulses, so it is completely dependent on the bias current.

- Burst noise is a type of low-frequency noise. The origin of this type of noise is not fully understood; however, it is related to the presence of impurity metal ions at the oxide interface in a semiconductor. In consists of sudden and staggered transitions between two or more voltage or current levels, in random and unpredictable times. It usually depends on the bias level.

- Flicker noise (or $1/f$ noise) is a type of noise found in all active devices. The origins of flicker noise are varied, but it is mainly caused by traps associated with impurities and crystal defects at the semiconductor-oxide interface. These traps randomly capture and release charge carriers, generating noise signals with concentrated energy at low frequencies. The spectral density of flicker noise is inversely proportional to the frequency.

### 2.1.1 Noise Associated with MOS Devices

The dominant sources of noise in a MOSFET are flicker and thermal noise, which are modeled, as shown in Figure 2.1, with a voltage source in series $V_G^2$ and with a current source in parallel $I_{th}^2$, respectively. The thermal noise power spectral density (PSD) is given by:

$$I_{th}^2 = 4kT\gamma g_m \tag{2.1.1}$$

where $k$ is the Boltzmann constant, $T$ the absolute temperature, $\gamma$ is a technology dependent constant and $g_m$ the transconductance of the device. The flicker noise PSD is given by:

$$V_G^2(f) = \frac{K_f}{WL \cdot C_{ox} f} \tag{2.1.2}$$

where $K_f$ represents the flicker noise constant for the particular device, $W$ and $L$ are the device dimensions, $C_{ox}$ is the oxide capacitance and $f$ the frequency. Constant $K_f$ can vary in a few orders of magnitude (according to technology), and depends on the manufacturing process of the device, so it is only possible to make a statistical calculation to approximate its value. $K_f$ parameter depends on the type of transistor, and is generally lower for PMOS transistors [7].

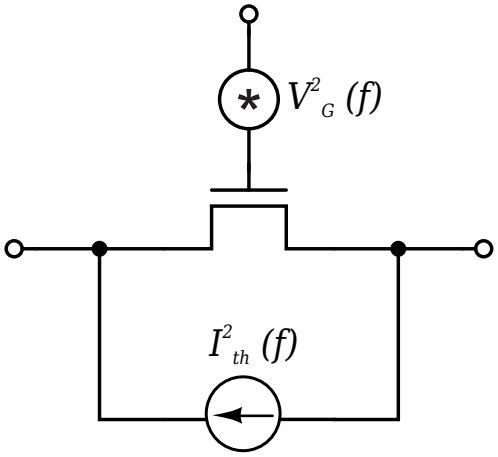



Figure 2.1: Modeling of flicker and thermal sources noise in a MOSFET.

Both noise sources can be combined in a single equivalent noise voltage source at the gate of the transistor, given by:

$$V_{n,in}^2(f) = \frac{4kT\gamma}{g_m} + \frac{K_f}{WL \cdot C_{ox} f} \tag{2.1.3}$$

Figure 2.2 shows noise PSD in a MOSFET device. It is possible to observe that at high frequencies the dominant source is thermal noise whereas at low frequencies it is flicker noise. The frequency at which the flicker noise ceases to be dominant is called corner frequency and is given by:

$$f_{corner} = \frac{K_f}{WLC_{ox}} \cdot \frac{g_m}{4KT\gamma} \tag{2.1.4}$$

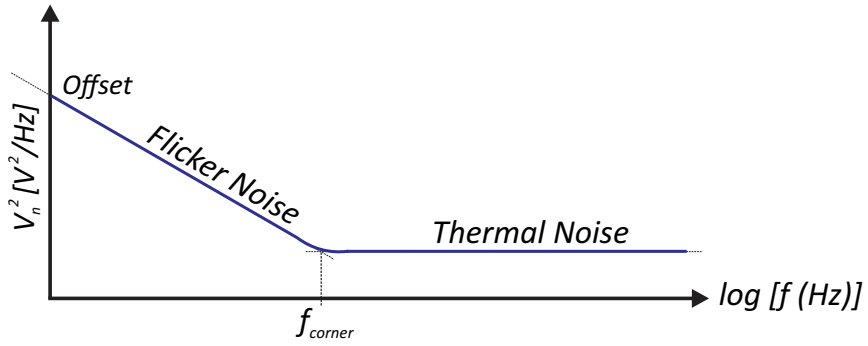



Figure 2.2: Noise PSD for a MOSFET.

Flicker noise therefore limits the overall performance of low-frequency signal processing circuits. According to equation (2.1.2), increasing the area of the transistors decreases the flicker noise contribution, because the probability that the charge carriers get trapped in the oxide interface decreases. However, if the amplitude levels of the input signal to be processed are very low, increasing the transistor dimensions is not sufficient to achieve a significant signal-to-noise ratio (6 dB). Noise analysis is an effective tool to study noise performance and design low noise configurations with the selection of topologies that minimize its contributions without increasing power and area consumption. However, noise analyses sometimes result in equations with many terms which are difficult to interpret, as presented in Appendix A. Therefore, the designer must also rely on simulation tools, which allow knowing which devices contribute the most to the total noise in a given topology.

## 2.2 Proposed Bootstrapping Resistors

The bootstrapping technique is often used to increase the input resistance of amplifiers or to act as a constant current to bias output stages [11]. In this Thesis it will be used to design high value resistors without the need for large area at low power cost. The bootstrapping technique is applied using a resistor $R_L$ connected between the input and output of a gain amplifier $K$, as shown in Figure 2.3a. Assuming the input impedance of $K$ is infinite, the current through $R_L$ is given by $I_{RL} = (1 - K)V_{in}/R_L$. Therefore, the equivalent input resistance of the circuit is $R_{Lb} = R_L/(1 - K)$, and can be very high if the gain of the amplifier is close to 1. The operation principle of the proposed resistance boosting technique, shown in Figure 2.3b, uses two voltage amplifiers $K_1$ and $K_2$ to set similar voltage levels at both terminals of $R_L$ and a current controlled current source to complete the design. In this case $R_{Lb} = R_L/(K_1 - K_2)$, and this proposal offers advantages regarding Figure 2.3a in terms of DC offset voltages.

### 2.2.1 Grounded Bootstrapping Resistor

Figure 2.4 shows a CMOS implementation of the grounded bootstrapping resistor based on the conceptual idea in Figure 2.3b. The two required amplifiers $K_1$ and $K_2$ are here source follower amplifiers $M_{RB1}$ and $M_{RB2}$. Note that $I_{b1} = I_{b2}$ and $M_{RB2}$ is connected as diode, so the input current is forced to be equal to the current through $R_L$. If both amplifiers are designed with similar gains the configuration results in a high value equivalent resistor, so this configuration is an impedance scaler. Next a small signal analysis

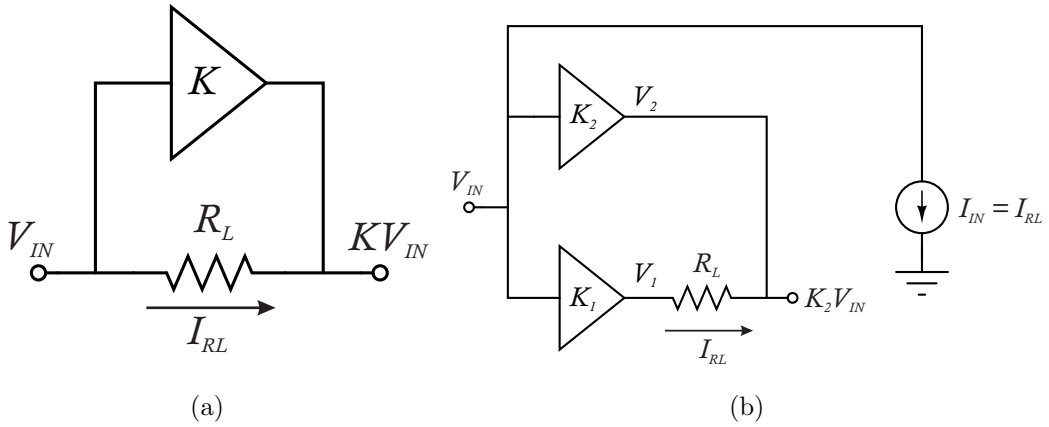



Figure 2.3: a) Bootstrapping technique and b) proposed resistance boosting.

is performed in order to provide more insight into how the technique works.

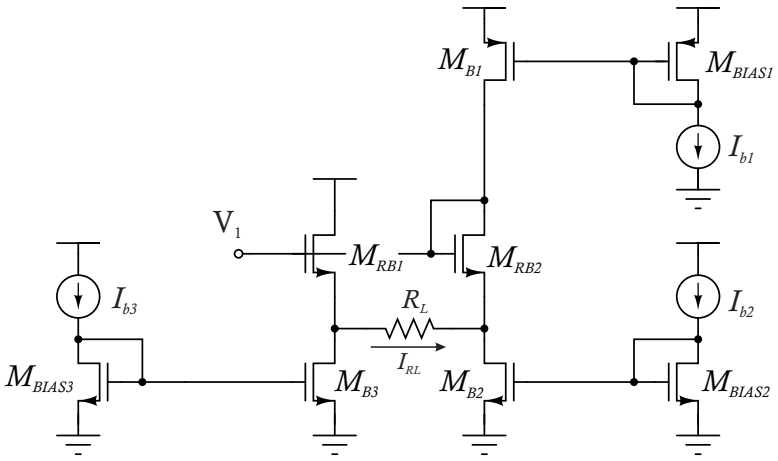



Figure 2.4: Proposed grounded bootstrapping resistor.

Let $r_{B1}$, $r_{B2}$ and $r_{B3}$ be the output resistance of the current source transistors $M_{B1}$, $M_{B2}$ and $M_{B3}$, respectively. If $r_{B1}r_{B2}r_{B3}R_L >> r_{B1}, r_{B2}, r_{B3}, R_L$, it can be shown that the small signal current $i_{RL}$ which flows through $R_L$ is given by:

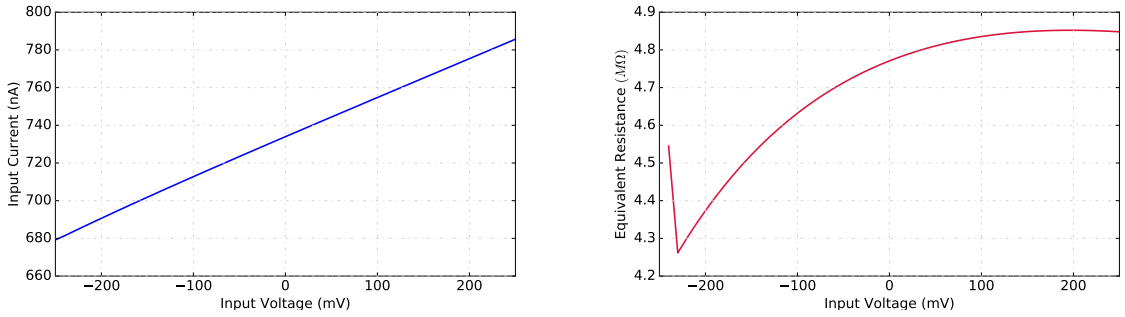
$$i_{RL} = \frac{(g_{m2}r_{B2} - g_{m1}r_{B3})V_{in}}{g_{m1}g_{m2}r_{B3}r_{B2}R_L + g_{m1}r_{B3}r_{B2} + g_{m2}r_{B3}r_{B2} + g_{m1}r_{B3}R_L + g_{m2}r_{B2}R_L} \tag{2.2.1}$$

where $g_{m1}$ is the transconductance of $M_{RB1}$ and $g_{m2}$ is the transconductance of $M_{RB2}$. Assuming that $g_{m1}r_{B3}$ and $g_{m2}r_{B2} >> 1$, the equivalent impedance is approximately given by:

$$R_{Lb} = \frac{g_{m1}g_{m2}r_{B3}r_{B2}R_L}{(g_{m2}r_{B2} - g_{m1}r_{B3})} \tag{2.2.2}$$

If $R_L$ increases, the equivalence impedance $R_{Lb}$ also increases. Besides, decreasing the difference between $g_{m2}r_{B2}$ and $g_{m1}r_{B3}$ ensures that the denominator in equation (2.2.2) decreases, which leads to a higher multiplying factor.

The impedance scaler was designed to operate in weak inversion in order to keep low power consumption. It uses a resistor $R_L = 100k\Omega$ and was biased with $I_{b1} = I_{b2} = 1\mu A$ and $I_{b3} = 500nA$, so it consumes $2.7\mu W$. Figure 2.5a shows the linear range of the proposed block under these bias conditions. According to the simulation results, the equivalent resistance is $4.3M\Omega$ for an input signal of $-240mV$ and changes to $4.85M\Omega$ for an input signal of $240mV$ (Figure 2.5b).




(a) (b)

Figure 2.5: a) Input current versus input voltage and b) equivalent grounded bootstrapping resistance.

### 2.2.2 Floating Bootstrapping Resistor

The floating bootstrapping resistor, shown in Figure 2.6, consists of two impedance scaler blocks with NMOS input transistors $M_{RB1}$ to $M_{RB4}$ acting as amplifiers. Bias current sources are implemented with single transistors $M_{Bi}$ with $i = 1, 2, 3$. The input transistors $M_{RB1}$ and $M_{RB3}$ are cross-coupled, as shown in the Figure in order to complete the design.

The proposed floating bootstrapping resistor uses two $100k\Omega$ resistors and was biased with $I_{b1} = I_{b2} = 1\mu A$, and $I_{b3} = 500nA$, so it consumes $5.4\mu W$. Figure 2.7a shows the linear range between $-200mV$ to $200mV$. Linear behavior is shown up to $200mVpp$ ($-100mV$-$100mV$).

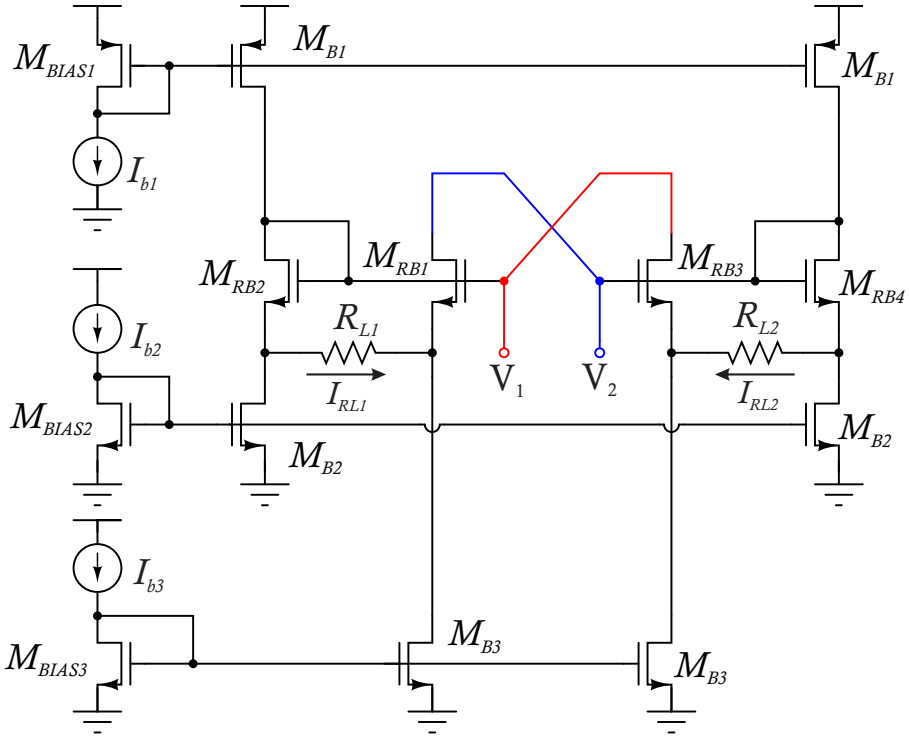
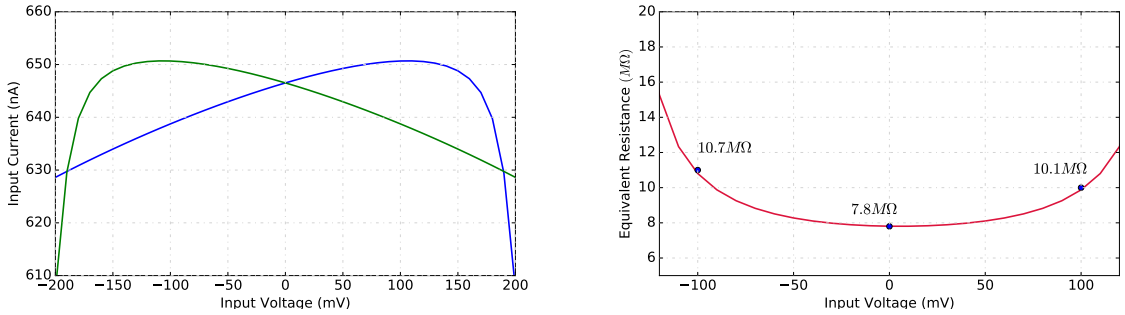



Figure 2.6: Proposed floating bootstrapping resistor.




(a) (b)

Figure 2.7: a) Input current versus input voltage and b) equivalent resistance for floating bootstrapping resistor.

The equivalent resistance is presented in Figure 2.7b, and it varies from $7.8M\Omega$ to $10.7M\Omega$, in a range from $-100mV$ to $100mV$ input voltage. As mentioned, the polysilicon resistors were $100k\Omega$ on each branch, so the equivalent resistance was increased by a factor of $\approxeq 45$.

### 2.2.3 Comparison with Other Implementations

The advantage of the proposed circuits is that high resistances can be implemented without the need for large area, as would be the case with passive components, and with low power consumption. Furthermore, linearity is not degraded in contrast to other techniques used to obtain high resistance with active components, as is the case of pseudo-resistors (PR) [12]. To corroborate this, a comparison between different high-resistance implementations is performed. The total harmonic distortion (THD) is obtained from simulations of a voltage divider, as shown in Figure 2.8 where a polysilicon resistor $R_c = 1M\Omega$ is connected in series with another polysilicon resistor (Figure 2.8a), a pseudo-resistor (Figure 2.8b) and the proposed floating resistor (Figure 2.8c). For a fair comparison, the equivalent resistance in all cases is $10M\Omega$.

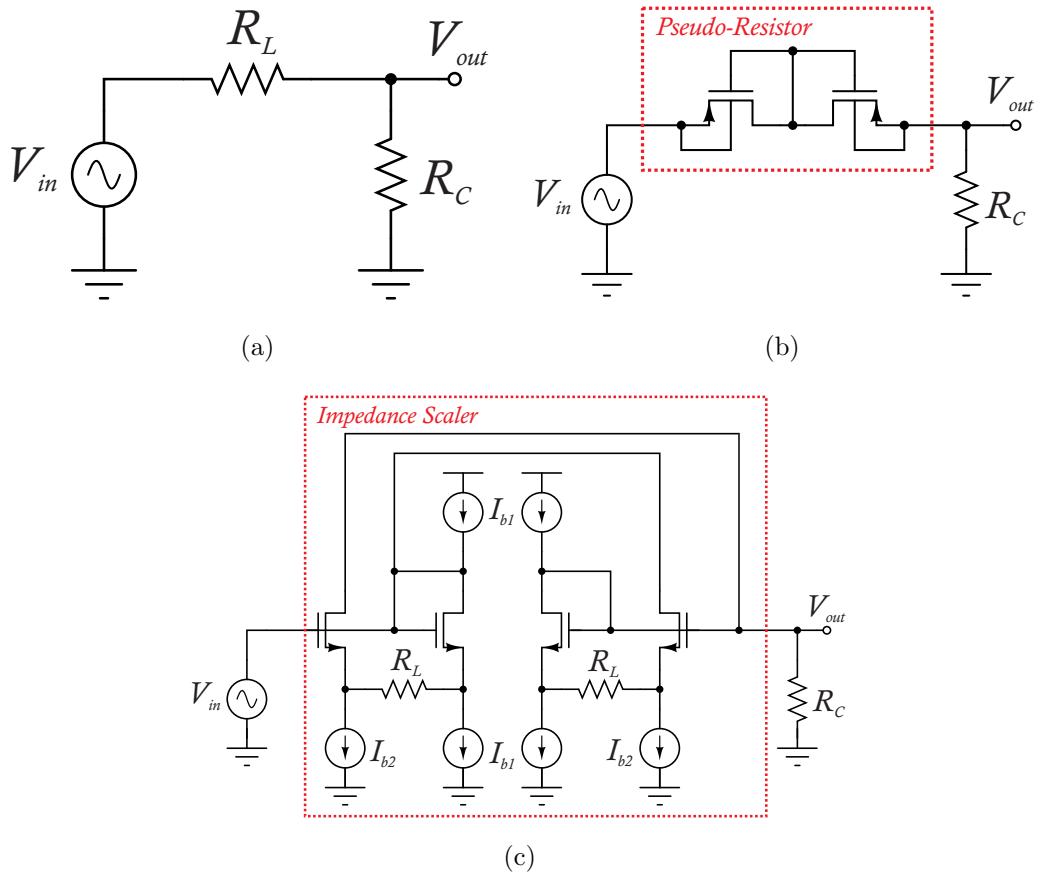



Figure 2.8: Voltage divider with a)Linear resistor, b)Pseudo-resistor, c)Floating bootstrapping resistor.

The THD for a sine input voltage at $50Hz$ with amplitude varying from $10mV$ to $250mV$ is shown in Figure 2.9 for the four different implementations. As expected, the polysilicon resistor provides the highest linearity, at the cost of area ($0.248mm^2$). In contrast, the pseudo-resistor consumes the least area, since only two PMOS transistors with $W/L = 3.5\mu m/36\mu m$ are required, but shows the highest distortion, with $-35dB$ THD at $250mV$ input amplitude. As for the proposed impedance scaler, it shows a THD $10dB$ lower than the pseudo-resistor for a $250mV$ input amplitude, with an area of $0.009mm^2$ and lower power consumption of $5.4\mu W$. A summary of the results is shown in Table 2.1.

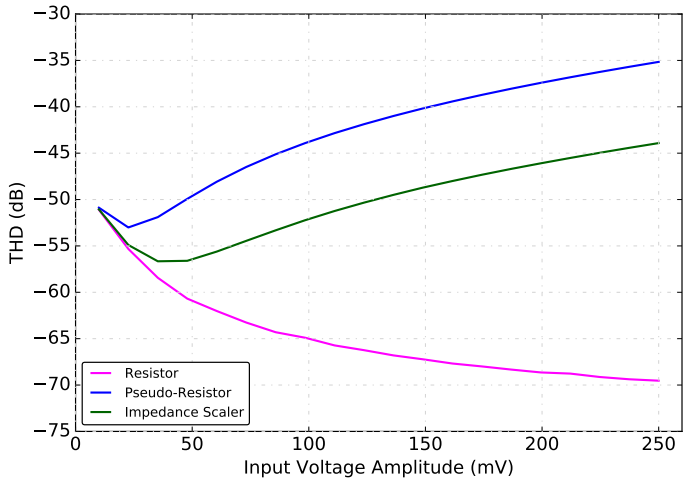
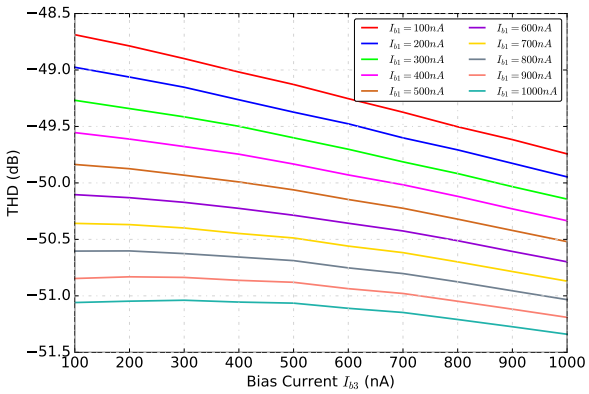



Figure 2.9: THD for different resistors implementations.

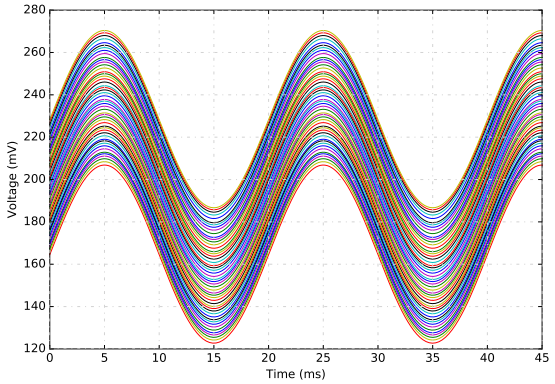
Table 2.1: Performance Comparison between Resistor Implementations.

| Parameters | Polysilicon resistor | Pseudo-resistor | Floating resistor |
|---|---|---|---|
| Power Consumption ($\mu W$) | NA | NA | 5.4 |
| THD ($dB$) @Input 100 mVpp | -65 | -41 | -52 |
| Area ($mm^2$) | 0.248 | >0.001 | 0.009 |

Finally, THD simulations were also performed by modifying the bias current in the proposed floating resistor, for a $20mVpp$ sine output voltage at $50Hz$. Figure 2.10a shows the THD for different values of $I_{b1}$, sweeping $I_{b3}$, from $100nA$ to $1\mu A$, which in turn results in a variations of $THD$ from $-48dB$ to $-51.2dB$. Figure 2.10b shows the time response at the output node ($V_{out}$) of the test circuit in Figure 2.8c.




(a)




(b)

Figure 2.10: a) THD for several $I_{b1}$ and $I_{b2}$ and b) Time response for proposed floating bootstrapped resistor.

## 2.3 Low-Noise Preamplifiers

This section presents several proposals of fully-differential low-noise preamplifiers. In the first two, LNP-0 and LNP-1, a polysilicon load resistor is used at the output to achieve high gain. In all the others, the impedance scaler is used as load resistance, which also adds the possibility of controlling the gain.

### 2.3.1 Flipped-Voltage Follower Low-Noise Preamplifier(LNP-0)

The first proposal, the LNP-0, consists of a flipped-voltage follower (FVF) based source degenerated transconductor, as shown in Figure 2.11. The DC current through the input transistors $M_1$ and $M_2$ is held constant which, together with the low impedance node established at their source terminals, results in unity voltage gain and high current sourcing capability [13]. The output current through $M_5$ and $M_6$ is therefore determined by the differential input voltage and the degeneration resistor $R_S$.The output current is copied through $M_7$ and $M_8$ and converted into a differential output voltage by means of resistor $R_L$, so the gain of the LNP-0 is $M \cdot R_L/R_S$, where $M$ is the gain of the current mirrors $M_5$ to $M_8$. The common mode feedback (CMFB) circuit consists of a differential difference amplifier.

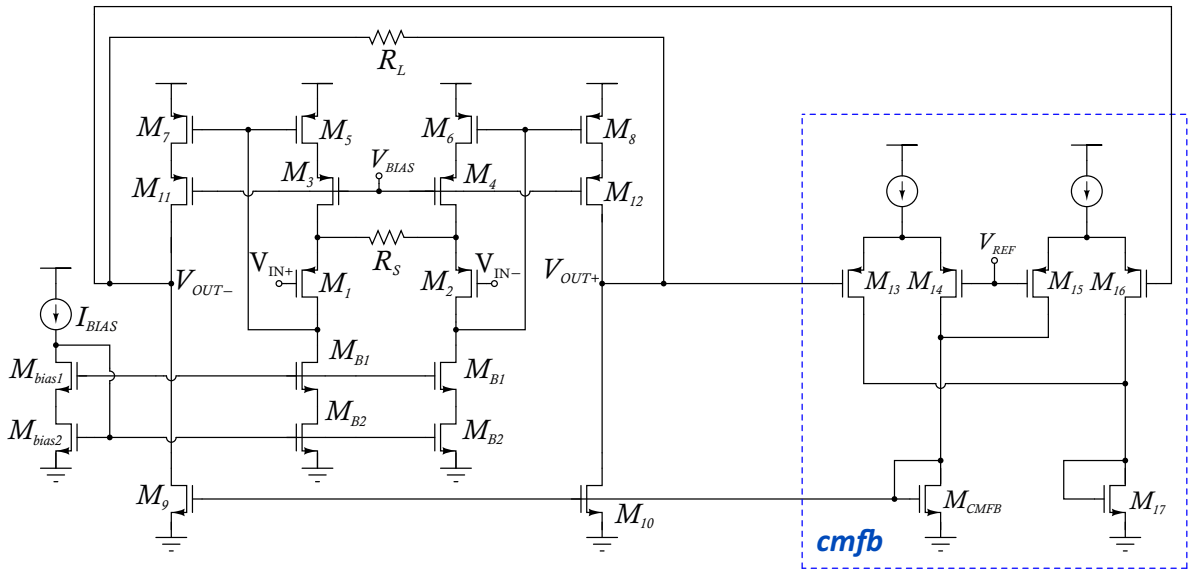



Figure 2.11: Flipped-voltage follower Low-noise preamplifier (LNP-0).

As shown in Appendix A, where the noise analysis of this circuit is presented, the current mirror gain M should be chosen higher than 1 to reduce flicker noise. However, there is a trade-off between the reduction in flicker noise and the increase in power consumption due to the increase in the current through the output branches. For this reason, $M = 1.5$ was chosen. It is preferable to use a PMOS FVF input because the flicker noise contribution in NMOS transistors is higher. In order to obtain the best noise-power trade-off, large area transistors operating in the weak inversion are used [14].

#### 2.3.1.1 Simulation Results

The proposed circuit was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage, and consumes $70\mu W$ total power. Table 2.2 summarizes the sizes of the transistors. The bias current is $I_{bias} = 5\mu A$, the degeneration resistance $R_S = 1k\Omega$, and the output resistance $R_L = 100k\Omega$. The preamplifier frequency response is shown in Figure 2.12. The circuit presents a differential gain of 41 dB and $560kHz$ bandwidth.

Table 2.2: Transistor Size of the Low-Noise Preamplifier 0.

| Transistors | $M_{1,2}$ | $M_{3,4}$ | $M_{5,6}$ | $M_{7,8}$ | $M_{9,10}$ | $M_{B1}$ | $M_{B2}$ |
|---|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 528/1 | 28/1 | 88/1 | 132/1 | 352/1 | 112/1 | 352/1 |

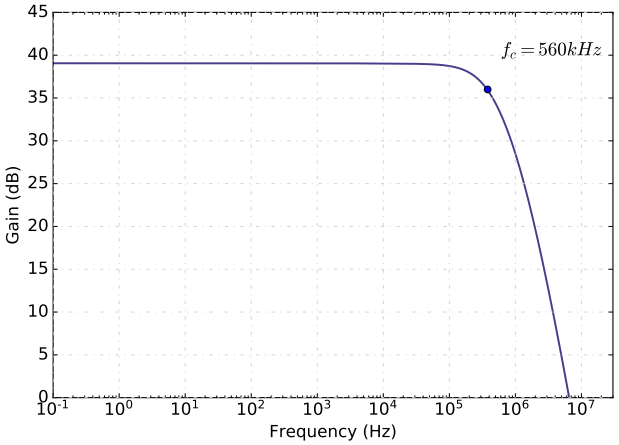



Figure 2.12: LNP-0 frequency response.

Figure 2.13 shows the time response for a $1mVpp$ amplitude signal at $250Hz$. Figure 2.14 presents the THD at several input voltage amplitudes, which is below $-40dB$ for sine input amplitudes up to $4mVpp$.

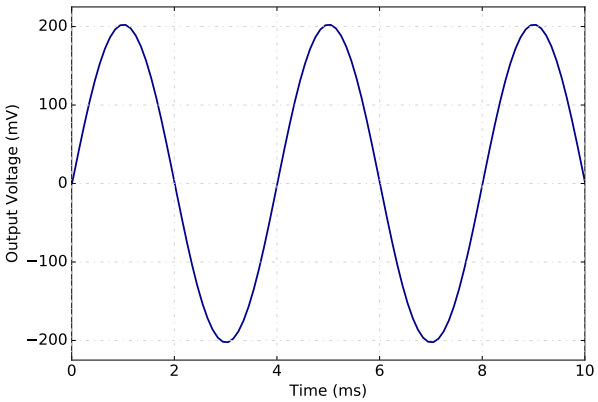



Figure 2.13: Output waveform at time response of the LNP-0.

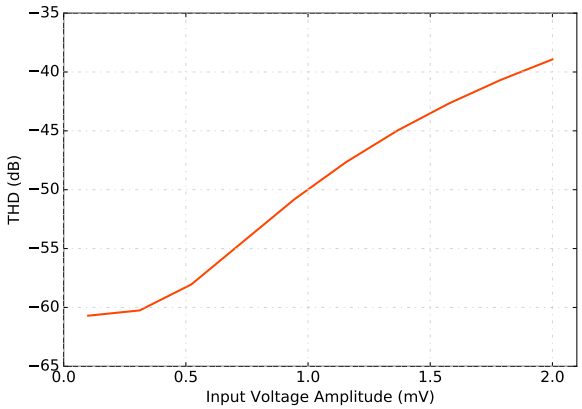



Figure 2.14: THD vs input amplitude of the LNP-0.

The equivalent input-referred noise power spectral density of the LNP-0 is shown in Figure 2.15. At $100Hz$ the input-referred noise is $28nV/\sqrt{Hz}$. When integrated from $0.1Hz$ to $1kHz$, the input referred noise is $1\mu V_{rms}$, and $9.7\mu V_{rms}$ when integrated in the whole-bandwidth (from 0.1 to $560kHz$).

The main characteristics of the preamplifier are summarized in Table 2.3.

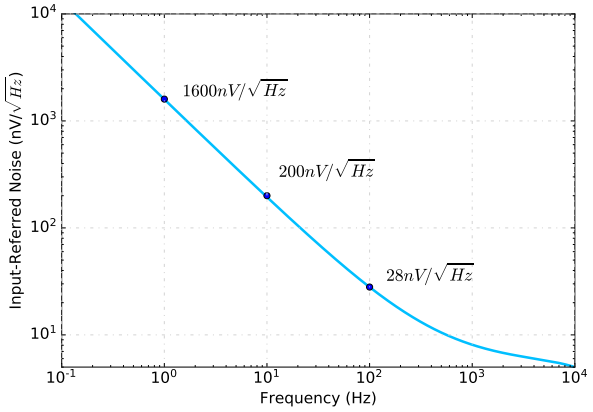



Figure 2.15: Input-referred Noise of LNP-0.

Table 2.3: Characteristics of the LNP-0.

| Parameters | Low-Noise Preamplifier 0 |
|---|---|
| Gain | 39.5 $dB$ |
| Bandwidth | 560 $kHz$ |
| Power | 70 $\mu W$ |
| CMRR | 74 $dB$@250$Hz$ |
| PSRR | 70 $dB$@250$Hz$ |
| Input Voltage @ THD=$-40dB$ | 4 mVpp @250$Hz$ |
| Input-Referred Noise ($0.1Hz - 560kHz$) | 9.7 $\mu V_{rms}$ |
| Offset | $\mu = 1.3mV$, $\sigma = 830\mu V$ |

### 2.3.2 Low-Noise Preamplifier 1 (LNP-1)

Figure 2.16 shows the schematic of the proposed LNP-1, which is based on a folded-cascode differential pair with a high-resistivity polysilicon resistor $R_S$ as source degeneration element. The current is carried to the output by means of transistors $M_7$ and $M_8$, where the conversion into a differential output voltage is carried out by means of another high resistivity polysilicon resistor $R_L$. The CMFB circuit, not shown in the Figure, consists of a differential difference amplifier.

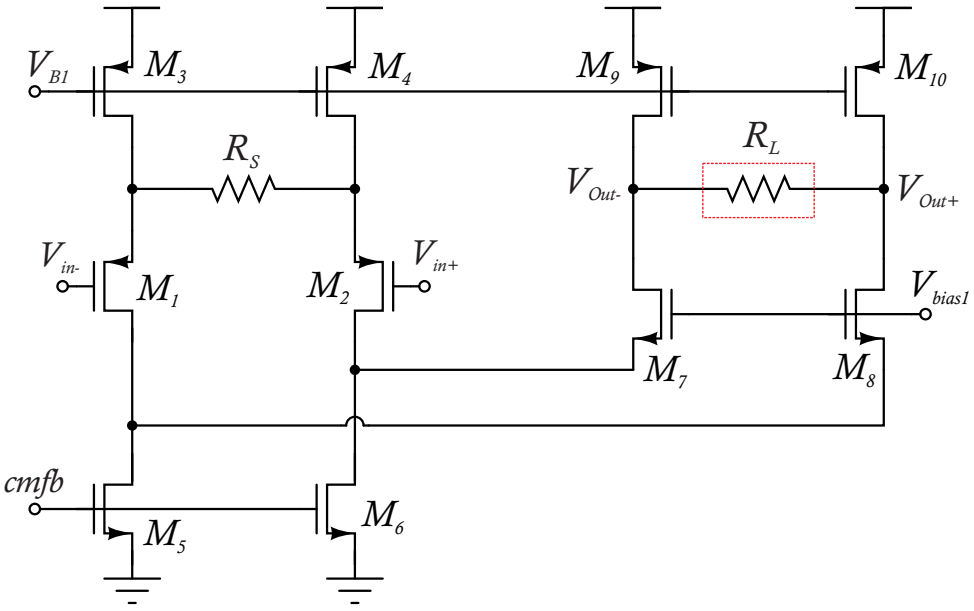



Figure 2.16: Low-Noise Preamplifier 1 with Polysilicon Resistor $R_L$.

The gain of the LNP-1 is given by:

$$A_0 = \frac{g_{m1} \cdot R_L}{g_{m1} R_S + 1} \tag{2.3.1}$$

where $g_{m1}$ is the input transconductance. In order to reduce the flicker noise contributions, the dimensions of the PMOS input pair and CMFB transistors were increased.

#### 2.3.2.1 Simulation Results

The proposed circuit was designed and simulated in a $0.18\mu m$ CMOS standard process. The sizing of transistors is shown in Table 2.4. The bias current was chosen to be $I_{B1} = 1\mu A$, to reduce the power consumption, and the amplifier was designed to operate in weak inversion. Under these bias conditions, to achieve a differential gain of $40dB$ according to equation 2.3.1, a relation $R_L/R_S = 100$ must be fulfilled. For this reason,the degeneration and load resistances were $100k\Omega$ and $10M\Omega$, respectively. Figure 2.17 shows the AC response. The gain of the preamplifier is $40.2dB$ and its cut-off frequency is $250kHz$.

Table 2.4: Transistor Size of the LNP-1.

| Transistors | $M_{1,2}$ | $M_{3,4}$ | $M_{5,6}$ | $M_{7,8}$ | $M_{9,10}$ |
|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 432/0.72 | 14.4/3.6 | 144/3.6 | 72/0.72 | 144/3.6 |

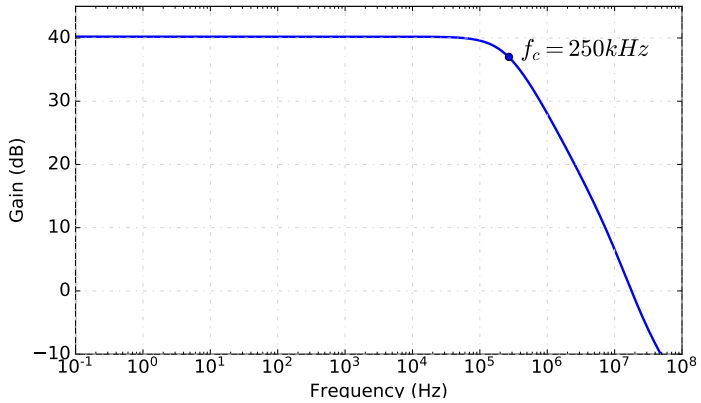
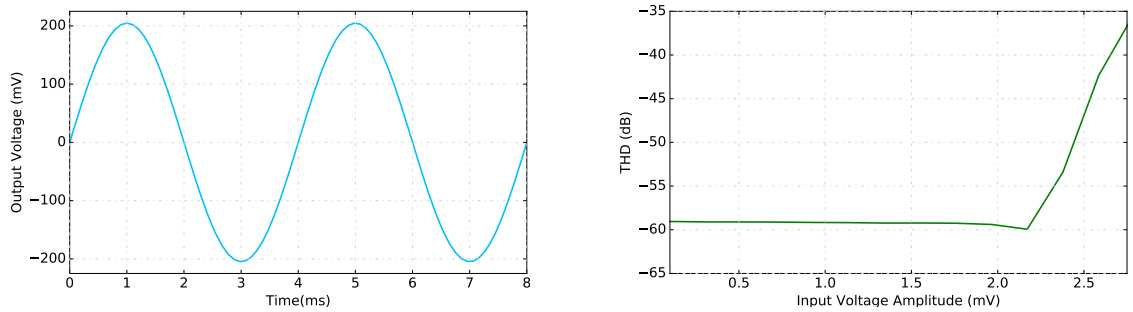



Figure 2.17: Frequency response of Low-Noise Preamplifier 1.

Transient simulation results of the LNP-1 for a $4mVpp$ sine input signal at $250Hz$ are shown in Figure 2.18a. for a $1mVpp$ sine input signal at $250Hz$. As shown in Figure 2.18b, the total harmonic distortion is $-60dB$ for a $4mVpp$ sine input signal, and remains below $-40dB$ at $5.2mVpp$ input. The equivalent input-referred-noise power spectral density of the proposed preamplifier is shown in Figure 2.19. The integrated input-referred noise of the LNP-1 from $0.1Hz$ to $1kHz$ and $0.1Hz$ to $250kHz$ is $2\mu V_{rms}$ and $13.2\mu V_{rms}$, respectively. Simulation results are summarized in Table 2.5.




(a) (b)

Figure 2.18: a) Transient simulation results and b)THD vs Input amplitude of the LNP-1.

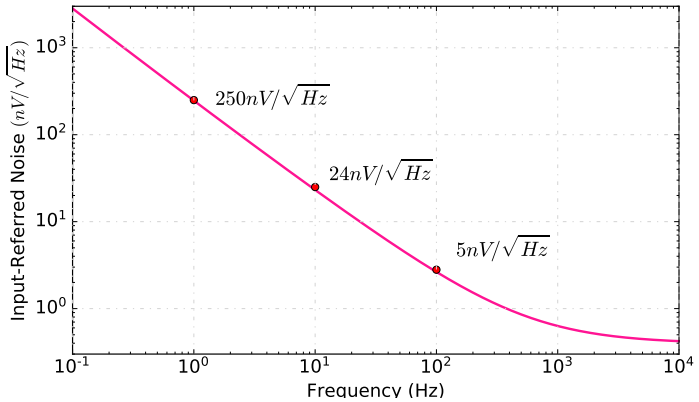



Figure 2.19: Input-Referred Noise of LNP-1 with $R_L$.

Table 2.5: Summary of Simulation Results of the LNP-1.

| Parameters | LNP-1 |
|---|---|
| Technology | 0.18 $\mu$m |
| Power Supply | 1.8 $V$ |
| Gain | 40.2 $dB$ |
| Bandwidth | 250 $kHz$ |
| Power | 15 $\mu W$ |
| CMRR | 81 @ 250Hz |
| PSRR | 84 @ 250Hz |
| Input Voltage @ THD=$-40dB$ | $5.2mVpp@250Hz$ |
| Input Referred Noise (0.1 Hz - 250 kHz) | 13.2 $\mu V_{rms}$ |
| Offset | $\mu = 1.6mV$, $\sigma = 750\mu V$ |

The main disadvantage of this circuit is the need for a very large polysilicon resistor, which causes a considerable increase in the area required for the physical implementation. In addition, due to the variations in the manufacturing process, mismatch between $R_L$ and $R_S$ causes an uncertainty in the final value of gain, which can not be adjusted after fabrication. For this reason, it is proposed to use the impedance scaler based on the bootstrapping technique to replace $R_L$ and provide gain tunability, as shown in the next Section.

### 2.3.3 Variable Gain LNP-1 (VGLNP-1)

Figure 2.20 shows the schematic of a LNP-1 where the load resistor is replaced by the proposed floating bootstrapping resistor. This configuration also allows for gain adjustment, so it is called Variable Gain Low Noise Preamplifier 1 (VGLNP-1).

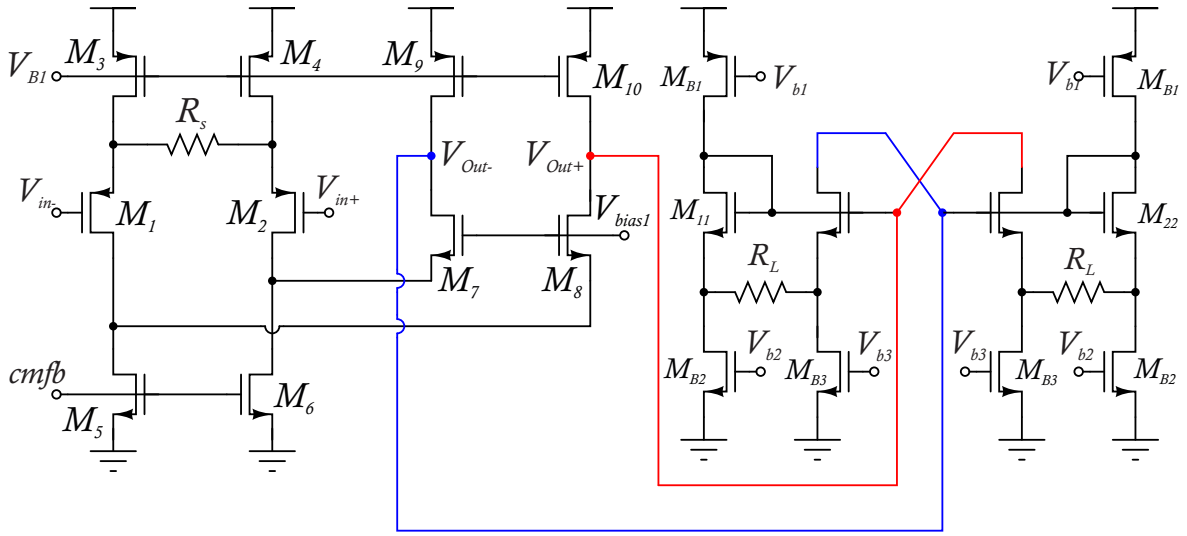
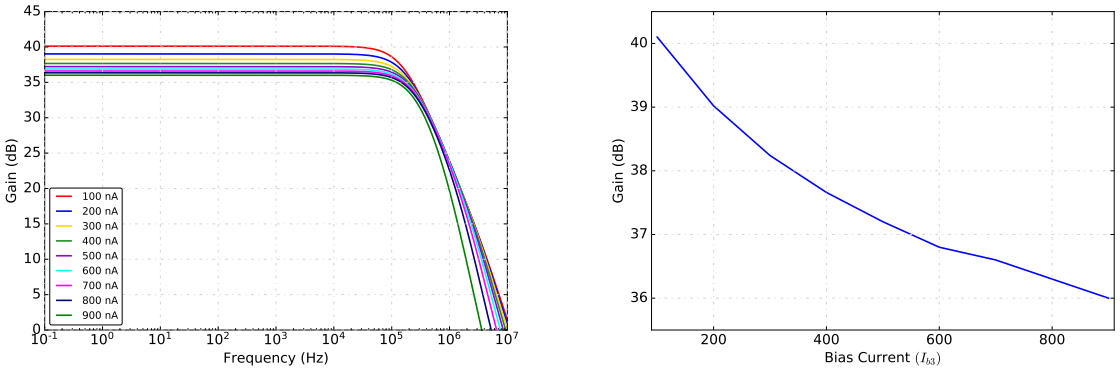



Figure 2.20: Proposed Variable Gain Low-Noise Preamplifier 1.

#### 2.3.3.1 Simulation Results

The VGLNP-1 was designed in a $0.18\mu m$ standard CMOS process with $1.8V$ supply voltage. The circuit was biased with $I_{B1} = 1\mu A$, $I_{b1}$=$I_{b2}$=$300nA$ and $I_{b3}$=$100nA$. To achieve an equivalent load resistance of $10M\Omega$, the impedance scaler requires two $100k\Omega$ resistors to which the bootstrapping technique is applied, so the area occupied by the passive resistors is reduced by a factor of 50. Furthermore, the use of a floating bootstrapping resistor provides the ability to change the equivalent load resistance ($R_{Lb}$ equivalent in the impedance scaler) through the bias currents $I_{b1}$, $I_{b2}$ and $I_{b3}$, resulting in a variable gain configuration.

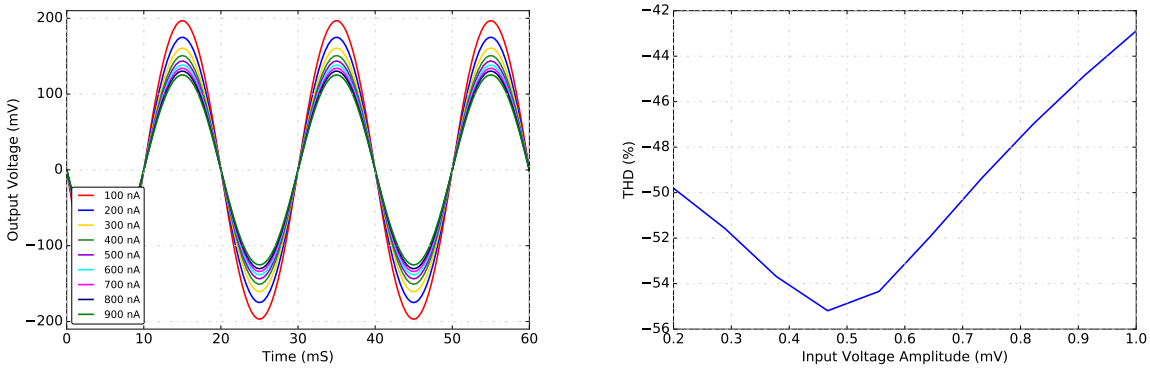
Figure 2.21 shows the frequency response and gain for several $I_{b3}$ values. When the bias current $I_{b3}$ changes from $100nA$ up to $900nA$, the differential gain varies from $36dB$ up to $40.2dB$ with almost constant bandwidth $f_c = 150kHz$.




(a) (b)

Figure 2.21: Frequency response for several $I_{b3}$ in the impedance scaler a) Programmability of the gain and b) Gain vs $I_{b3}$.

Figure 2.22a shows the time response also for several $I_{b3}$ values. The THD for a sine differential input voltage at $50Hz$ as a function of the input signal amplitude, at a gain setting of $40.2dB$ is shown in Figure 2.22b. It remains below $-40dB$ for input voltages up to $2mVpp$.




(a) (b)

Figure 2.22: a) Output Voltage for different gains and b) THD for different input voltages amplitudes

Finally, Figure 2.23 shows the input-referred noise power spectral density (PSD) of the proposed preamplifier. When integrated from $0.1Hz$ to $BW$ the input referred-noise is $11.6\mu V_{rms}$.

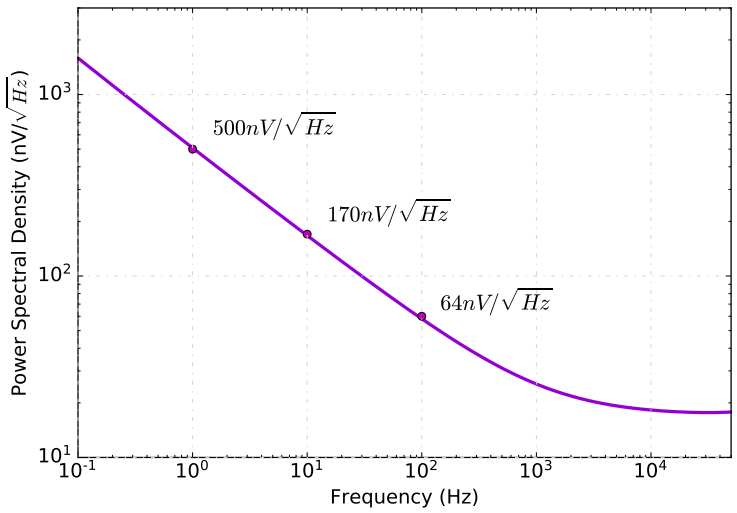



Figure 2.23: Input-referred Noise PSD of VGLNP-1.

#### 2.3.3.2 Experimental Results

The VGLNP-1 was fabricated in $0.18\mu m$ CMOS standard technology. The chip microphotograph and layout are shown in Figure 2.24. The area of the circuit is $450\mu m$x$90\mu m$, which includes the high resistivity polysilicon degeneration resistors ($R_S$ and $R_L$), designed to be $10k\Omega$ and $100k\Omega$, respectively, and the CMFB circuit. In order to reduce flicker noise, transistor lengths were set to $3.6\mu m$, which together with interdigitation in the layout, also improves matching.

For experimental characterization, the bias current $I_{B1}$ was set to $1\mu A$, whereas the bias currents in the impedance scaler block were $I_{b1} = I_{b2} = 600nA$ and $I_{b3}$ was varied from $170nA$ to $250nA$. Each current was generated via an external potentiometer. Under these conditions, the preamplifier, including the impedance scaler and CMFB block, consumes $22\mu W$, with $1.8V$ supply. It provides a variable gain from $34dB$ to $38dB$ as shown in Figure 2.25a, whereas the bandwidth varies from $13kHz$@$34dB$ to $100kHz$@$38dB$. Figure 2.25b shows the time domain output at different gain levels for $V_{in} = 2mVpp$ input signal at $1kHz$.

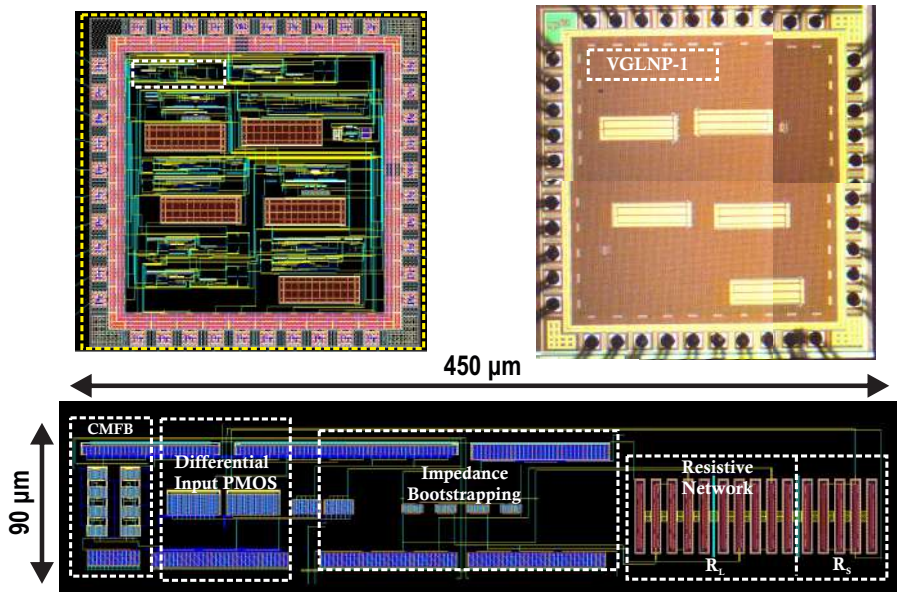
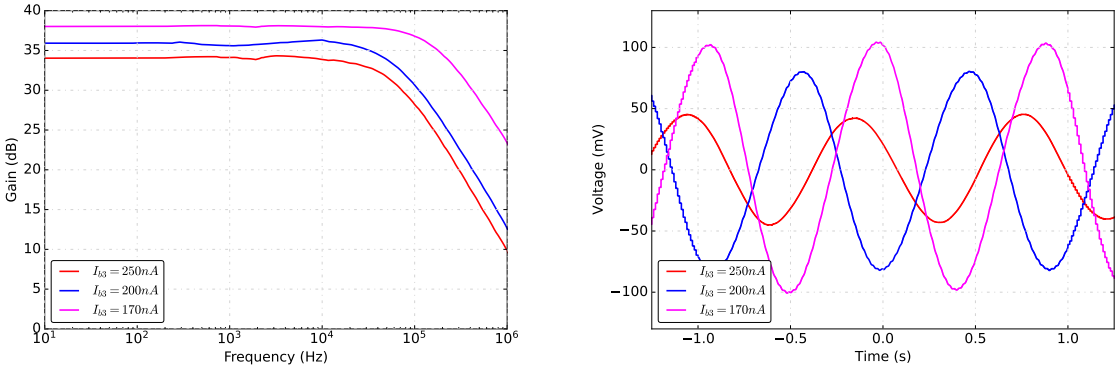



Figure 2.24: Microphotograph and layout of the VGLNP-1.




(a) (b)

Figure 2.25: a)Experimental frequency response for different $I_{b3}$ values and b) Experimental time response of the VGLNP-1.

The THD was measured using a Rohde & Schwartz FSV - Signal Analyzer ($10Hz$-$3.6GHz$). Figure 2.26 shows the THD for a sine differential input voltage at $1kHz$ and with amplitude varying from $1mV$ to $3mV$, at three different gain levels. In this case, the measured THD is below $-36dB$ for the minimum gain and increases to $-34dB$ at maximum gain. It remains below $-40dB$ with input amplitude voltage up to $2mV$ for the gain up to $36dB$. For maximum gain, the input voltage amplitude must be below $1mV$ to meet the stated specification.

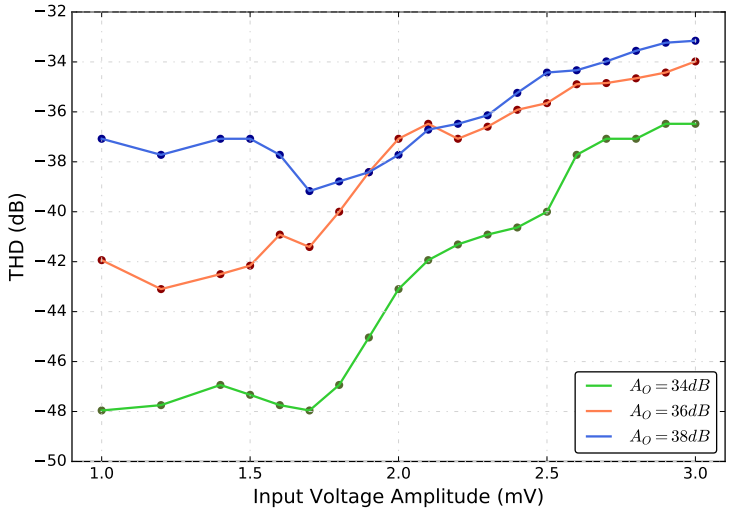



Figure 2.26: THD measurements at several gains.

Noise characterization was performed on three samples, using a SR530 Lock-in amplifier. The input-referred noise is shown in Figure 2.27. At $1kHz$ the power spectral density is $35nV/\sqrt{Hz}$. When integrated from $100Hz$ to $BW$ the input-referred noise is $11.8\mu V_{rms}$.

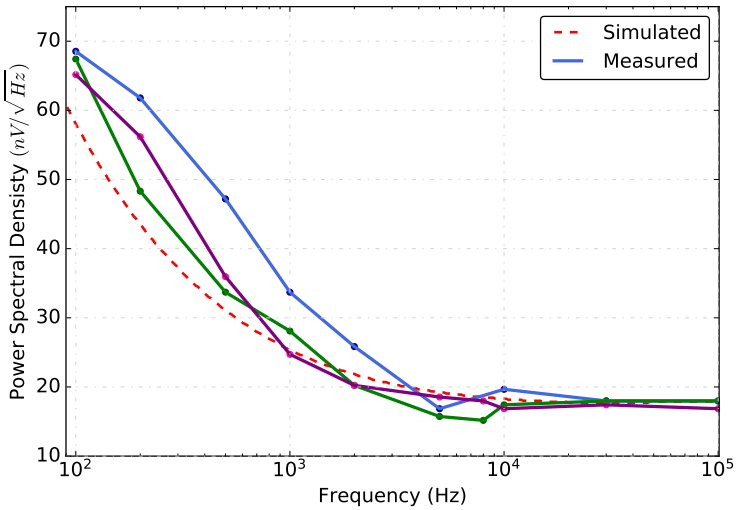



Figure 2.27: Input-referred noise PSD of the VGLNP-1.

#### 2.3.3.3 Comparative between the LNP-1 and the VGLNP-1

Table 2.6 shows a comparison between the proposed LNP-1 and VGLNP-1. The LNP-1 topology presents lower power consumption, lower input-referred noise, and higher linearity. However, the area required for the implementation of the resistor is 50 times higher than using the impedance scaler. In addition, the gain of the VGLNP-1 can be adjusted through the bias currents, which can also be used to counteract process variations, with a slight increase in power consumption.

Due to the versatility of the impedance scaler as output load resistor, the following low noise preamplifier proposals were also based on this alternative, aiming at lowering both the noise an power efficiency factors with respect to this first implementation.

Table 2.6: Performance Comparison of LNP-1 and VGLNP-1

| Parameters | LNP-1 | VGLNP-1 | |
|---|---|---|---|
| | Simulation | Simulation | Experimental |
| Technology ($\mu m$) | 0.18 | 0.18 | 0.18 |
| Supply ($V$) | 1.8 | 1.8 | 1.8 |
| Gain ($dB$) | 40.2 | 36 - 42 | 34 - 38 |
| Bandwidth ($kHz$) | 250 | 15 - 150 | 13 - 100 |
| Power ($\mu W$) | 15 | 16.2 | 22 |
| CMRR ($dB$) | 81 @ 250Hz | 76 @ 250Hz | - |
| PSRR ($dB$) | 84 @ 250Hz | 76 @ 250Hz | - |
| Input Voltage @ THD=$-40dB$ | 5.2 mVpp | 5.3 mVpp | 3 mVpp |
| Input-Referred Noise ($\mu V_{rms}$) | 13.2 | 11.6 | 11.8[1] |
| Mean Offset ($mV$) | 1.3 | 1.6 | - |
| Load Resistor $R_L$ ($M\Omega$) | 10 | 0.2 | 0.2 |
| Area ($mm^2$) | 0.2 | 0.004 | 0.004 |
| $NEF$ | 2.9 | 3.2 | 5 |
| $PEF(V)$ | 15.3 | 19.3 | 45.1 |

[1]Integrating from $100Hz$ to $100kHz$.

### 2.3.4 Variable Gain Low-Noise Preamplifier 2 (VGLNP-2)

Figure 2.28 shows the proposed VGLNP-2. The core transconductor consists of a super-source follower (SSF) based differential amplifier with source degeneration. Since the input transistors $M_1 - M_2$ are biased with a constant current, their source-gate voltages remain constant, so the differential input voltage is established between the terminals of $R_S$, and the generated current flows through $M_7$-$M_8$ and is converted back to a differential voltage by the floating bootstrapping resistor.

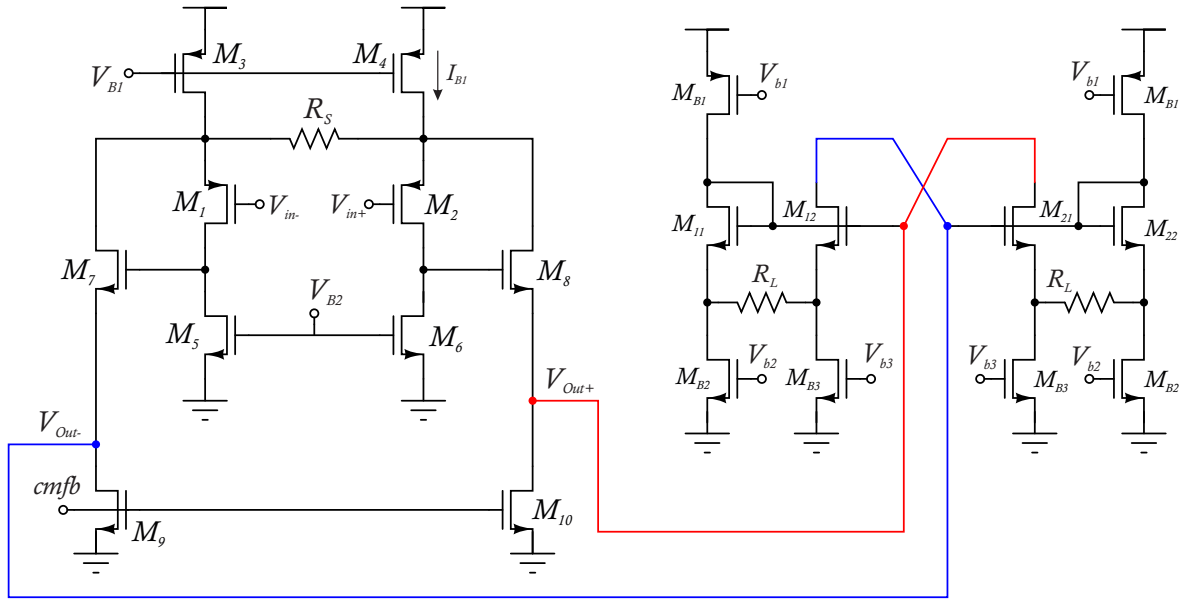



Figure 2.28: Proposed Variable Gain Low-Noise Preamplifier 2.

The super-source follower introduces a negative feedback loop via the transistors $M_{7,8}$, strongly reducing the output resistance. The gain of VGLNP-2 is given by:

$$A_O = \frac{g_{m1} r_{o1}}{1 + g_{m1} r_{o1}} \cdot \frac{R_{Lb}}{R_S} \tag{2.3.2}$$

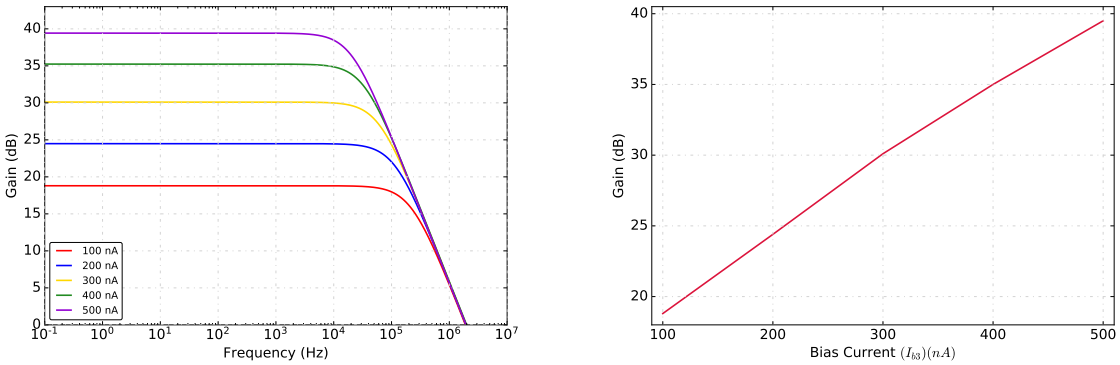
where $g_{m1}$ and $r_{o1}$ are the transconductance and output resistance of transistor $M_1$, and $R_{Lb}$ is the equivalent resistance of the load bootstrapping resistor. The degeneration resistor is $10k\Omega$ and the equivalent load resistor is $1.5M\Omega$, to set a gain of $40dB$.

### 2.3.4.1 Simulation Results

The VGLNP-2 was designed in a $0.18\mu m$ CMOS process with 1.8 V supply voltage, and consumes $15\mu W$ with the bias currents set to $I_{B1} = I_{B2} = 1\mu A$. In order to achieve an equivalent load resistance of $1.5M\Omega$, $R_L$ was set to $10k\Omega$ and the impedance scaler was biased with $I_{b1} = 2I_{b2} = 1\mu A$ and $I_{b3} = 500nA$. The sizing of transistors is shown in Table 2.7. In order to reduce flicker noise, the size of the PMOS input transistors and the PMOS biasing transistors $M_3$-$M_4$ were increased. The preamplifier frequency response for several values of $I_{b3}$ and the gain as a function of $I_{b3}$ are shown in Figure 2.29. The proposed circuit presents a variable differential gain from $19dB$ to $39.5dB$ when $I_{b3}$ is varied from $100nA$ to $500nA$, with $20kHz$ to $200kHz$ bandwidth.

Table 2.7: Transistor Size of the Variable Gain Low-Noise Preamplifier 2.

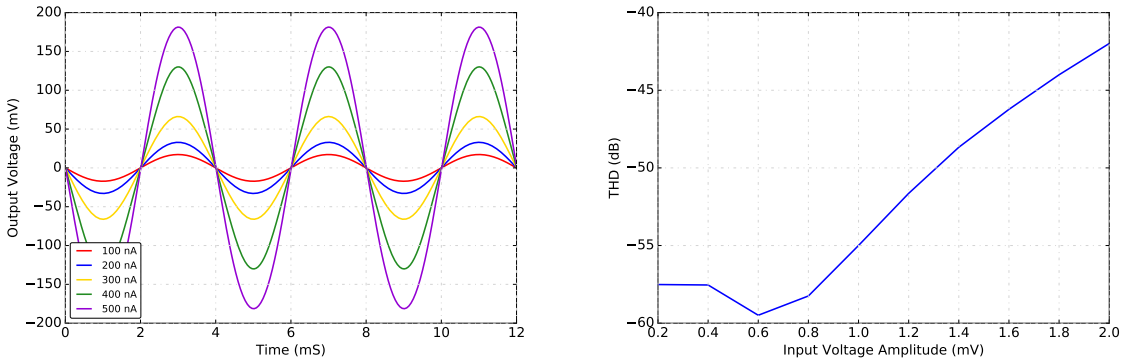
| Transistors | $M_{1,2}$ | $M_{3,4}$ | $M_{5,6}$ | $M_{7,8}$ | $M_{9,10}$ |
|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 90/1.8 | 72/3.6 | 36/3.6 | 36/3.6 | 72/1.8 |




(a) (b)

Figure 2.29: a) Frequency response for different $I_{b3}$ values and b) Gain vs $I_{b3}$ of the VGLNP-2.

Figure 2.30a shows the time response for a $1mV$ amplitude sine input signal at $250Hz$ at different gain settings. Figure 2.30b shows the total harmonic distortion as a function of the input voltage for $40dB$ gain. In particular, the THD is $-42dB$ for a $4mVpp$ sine input signal at $250kHz$ and decreases down to $-57dB$ for a $400\mu Vpp$ input.




(a) (b)

Figure 2.30: a)Output Voltage for different gains and b) THD simulation of the VGLNP-2.

Finally, Figure 2.31 shows the input-referred noise power spectral density. At $10Hz$ the input-referred noise is $28.5nV/\sqrt{Hz}$. Integrating from $0.1Hz$ to $20kHz$ the input referred-noise is $4.7\mu V_{rms}$.

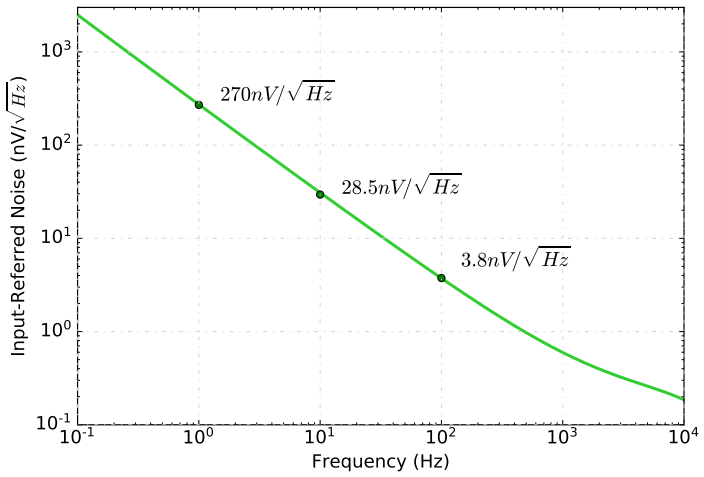



Figure 2.31: Input-referred Noise of the VGLNP-2.

### 2.3.5 Variable Gain Low-Noise Preamplifier 3 (VGLNP-3)

Figure 2.32 shows the VGLNP-3. It also consists of a super-source follower based on degenerated differential pair but the output currents are now copied to the output branches through mirrors in order to increase the output resistance. As in the former topology, the input pair is held at a constant bias current $I_{B1}$, which increases linearity. The CMFB circuit consist of a differential difference amplifier, not shown in Figure 2.32.

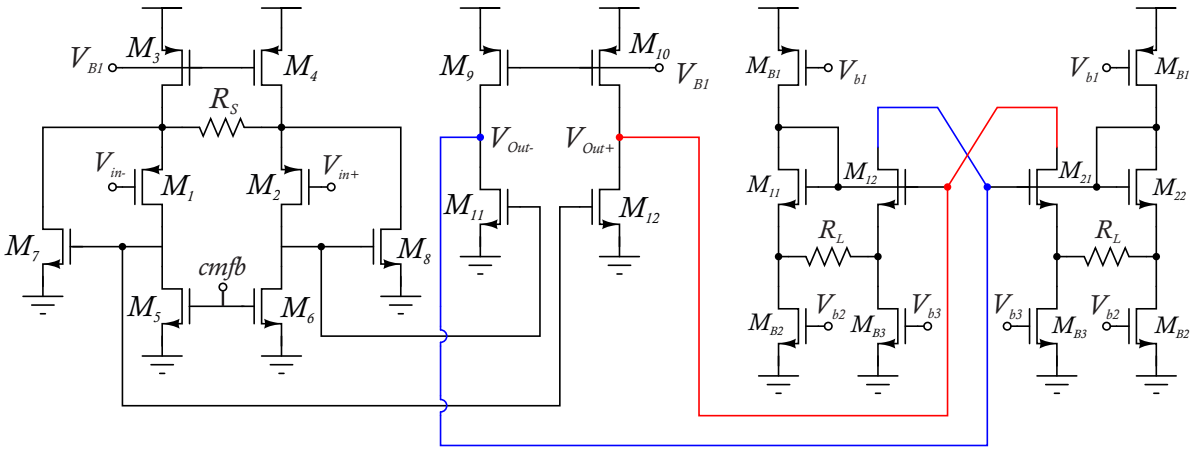



Figure 2.32: Variable Gain Low-Noise Preamplifier 3.

#### 2.3.5.1 Simulation Results

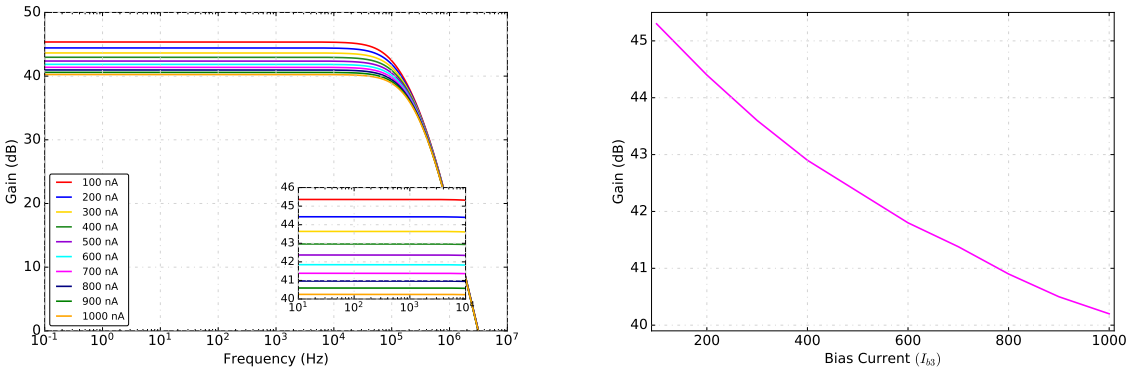
The VGLNP-3 circuit was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage. All transistors were biased in the weak inversion region. The total power consumption of the circuit is $17.1\mu W$. The sizing of transistors is shown in Table 2.8.

Table 2.8: Transistor Size of the Variable Gain Low-Noise Preamplifier 3.

| Transistors | $M_{1,2}$ | $M_{3,4}$ | $M_{5,6}$ | $M_{7,8}$ | $M_{9,10}$ | $M_{11,12}$ |
|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 180/1.8 | 72/3.6 | 72/1.8 | 36/3.6 | 72/3.6 | 36/3.6 |

As in all configurations, the area of the PMOS input transistors was increased to reduce the flicker noise contribution. A degeneration resistance $R_S = 25k\Omega$ and load resistors $R_L = 50k\Omega$ were used. The bias current was set to $I_{B1} = 1\mu A$, whereas, the impedance scaler was biased with $I_{b1} = I_{b2} = 1\mu A$ and $I_{b3} = 500nA$. Figure 2.33 shows

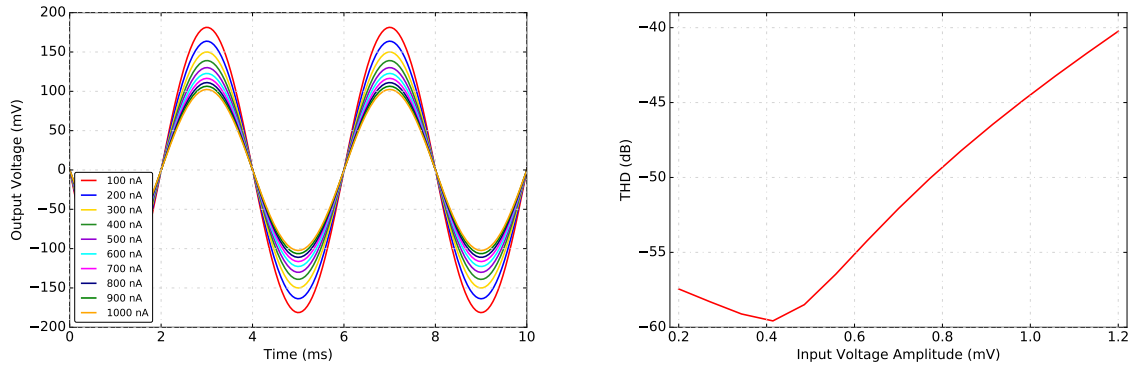
the frequency response at several $I_{b3}$ bias current values. The gain of the topology changes from $40dB$ to $45.5dB$ with almost constant $150kHz$ bandwidth.




(a) (b)

Figure 2.33: a) Frequency response for several $I_{b3}$ values in the impedance scaler and b) Gain vs $I_{b3}$ for the VGLNP-3.

Figure 2.34a shows the time domain for a $500\mu V$ amplitude input signal at $250Hz$, at different gain settings. For the Figure 2.34b shows the THD versus the input voltage amplitude at $250Hz$, at $40dB$ gain. As shown, the THD remains below $-40dB$ up to $1.2mV$ input voltage amplitude.




(a) (b)

Figure 2.34: a) Time response analysis for different bias currents $I_{b3}$ and b) THD simulation for different input voltages amplitude.

The input-referred noise power spectral density is shown in Figure 2.35. If integrated in a range from $0.1Hz$ to $150kHz$, the equivalent noise voltage is $5.4\mu V_{rms}$. Simulation results are summarized in Table 2.9.

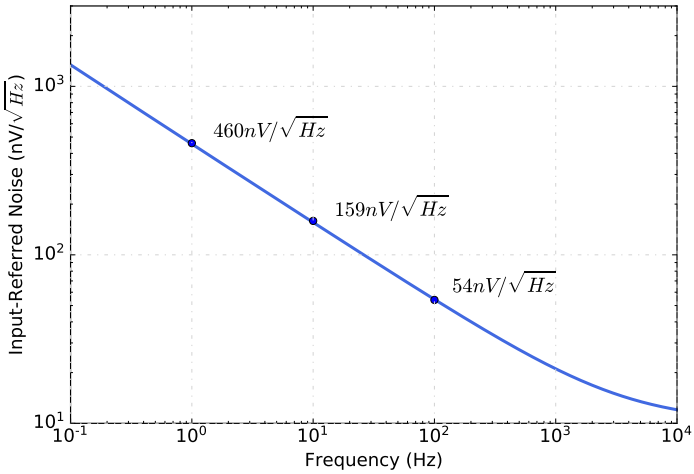



Figure 2.35: Input-referred noise of the VGLNP-3.

Table 2.9: Summary of Simulation Results of the VGLNP-3.

| Parameters | VGLNP-3 |
|---|---|
| Technology | 0.18 $\mu$m |
| Power Supply | 1.8 $V$ |
| Gain | 40 - 45.5 $dB$ |
| Bandwidth | 110 - 150 $kHz$ |
| Power | 17.1 $\mu W$ |
| CMRR | 75.5 @ 250Hz |
| PSRR | 76 @ 250Hz |
| Input Voltage @ THD=$-40dB$ | $2.4mVpp$@$250Hz$ |
| Input Referred Noise (0.1 Hz - 150 kHz) | 5.4 $\mu V_{rms}$ |
| Offset | $\mu = 1mV$, $\sigma = 280\mu V$ |

Since the objective in portable systems is low consumption, a topology with reduced power consumption is proposed next, keeping low the noise contribution with moderate area.

### 2.3.6 Variable Gain Low-Noise Preamplifier 4 (VGLNP-4)

Based on the complementary input stage, the architecture of the Variable Gain Low-Noise Preamplifier 4 is proposed, as shown in Figure 2.36. It combines an NMOS with a PMOS input differential pair, both with source degeneration. The source-degeneration complementary input amplifier allows the input range to be extended [15]. In this case, complementary input is used to double the effective transconductance without increasing the bias current [16].

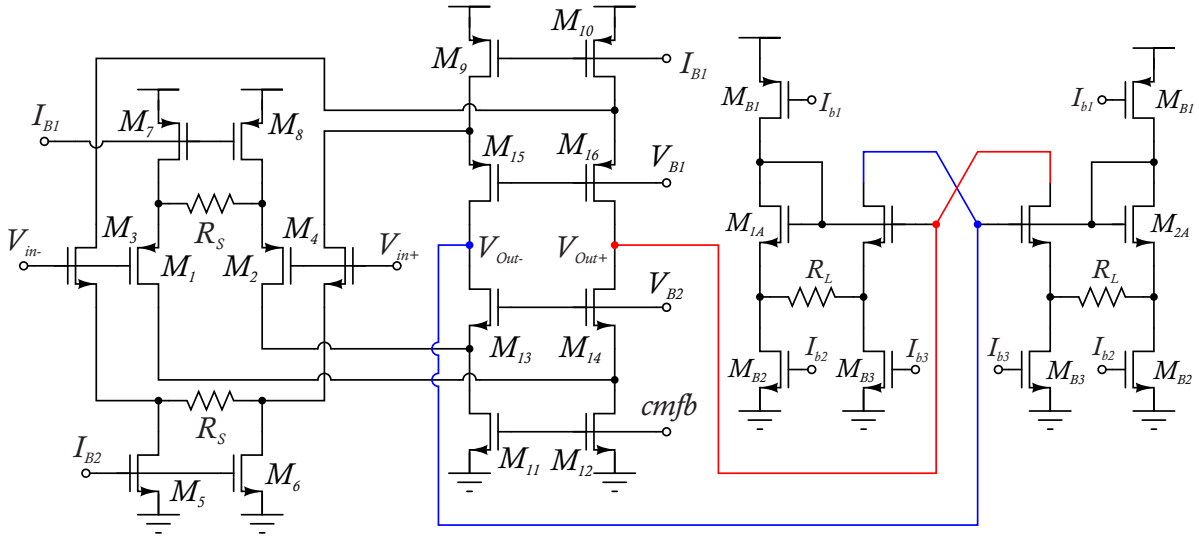


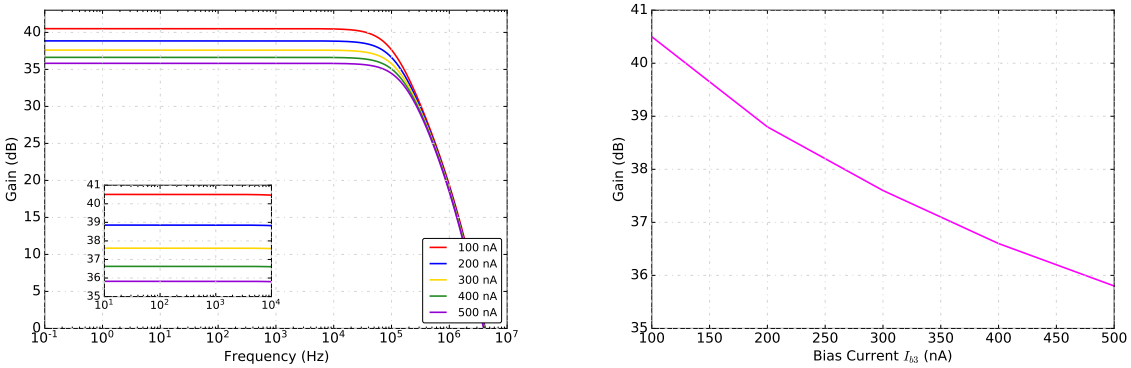

Figure 2.36: Proposed Variable-Gain Low-Noise Preamplifier 4.

#### 2.3.6.1 Simulation Results

The VGLNP-4 was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage and consumes $9.45\mu W$. All transistors were biased in the weak inversion region and their sizes are shown in Table 2.10. As in all cases, the width and length of the input transistors were increased to reduce the flicker noise contribution. Degeneration resistors $R_S = 10k\Omega$ were used in both differential pairs for source degeneration. Load resistors $R_L = 100k\Omega$ were used in the impedance scaler. Bias currents were set to $I_{B1} = 500nA$ and $I_{B2} = 250nA$, the impedance scaler was biased with $I_{b1} = I_{b2} = 300nA$ and $I_{b3} = 100nA$. Under these conditions, the VGLNP-4 shows a differential gain of $40.5dB$ with a bandwidth of $115kHz$. Figure 2.37a shows the simulated differential gain on the VGLNP-4 for several $I_{b3}$ values, from $100nA$ to $500nA$. In this range, the gain varies from $35.8dB$ to $40.5dB$, as shown in Figure 2.37b, with bandwidth constant of $115kHz$.

Table 2.10: Transistor Size of the Variable Gain Low-Noise Preamplifier 4.

| Transistors | $M_{1A,2A}$ | $M_{1B,2B}$ | $M_{3,4,9,10}$ | $M_{5,6,7,8}$ | $M_{11,12}$ | $M_{13,14}$ |
|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 216/0.72 | 72/0.72 | 14.4/3.6 | 72/0.72 | 14.4/3.6 | 72/0.72 |




(a) (b)

Figure 2.37: a) Frequency response for different $I_{b3}$ values and b) Gain vs $I_{b3}$ of the VGLNP-4.

Figure 2.38 shows the total harmonic distortion as a function of the input voltage for $40dB$ gain. The THD is $-49dB$ for a $400\mu Vpp$ sine input signal at $250Hz$ and increases up to $-40dB$ for a $2.2mVpp$.

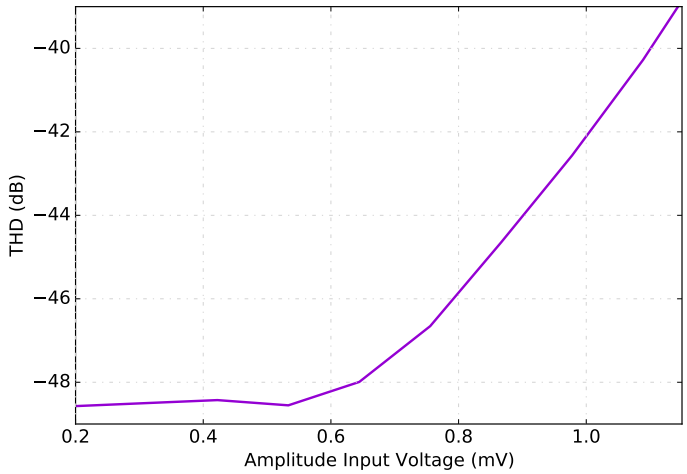
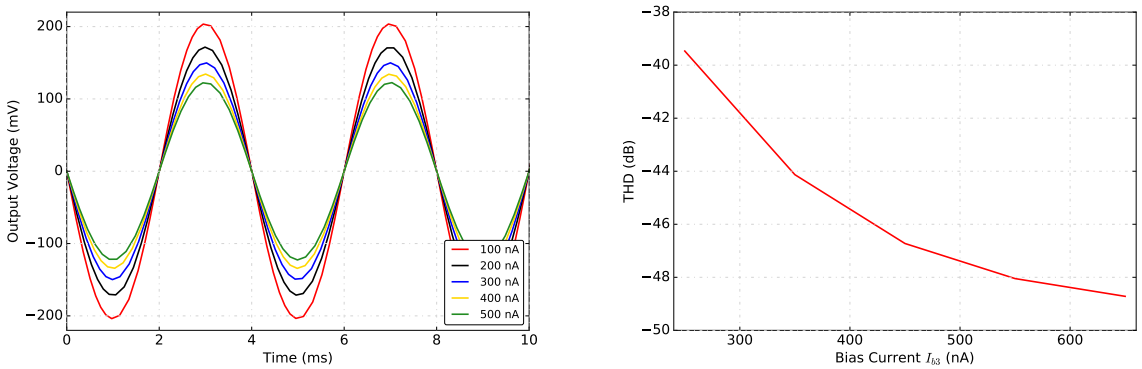



Figure 2.38: THD simulation for different input voltage amplitude of VGLNP-4.

Figure 2.39 shows the time response for a $1mV$ amplitude sine input signal at $250Hz$ at different gain settings. Figure 2.39 shows the THD versus the bias current $I_{b3}$ in the impedance scaler. The THD remains below $-40dB$ for maximum gain ($40.5dB$ @ $I_{b3} = 100nA$), and decreases down to $-49dB$ at minimum gain ($35.8dB$ @ $I_{b3} = 500nA$).




(a) (b)

Figure 2.39: a) Time response for different bias currents $I_{b3}$ and b) THD for a $1mV$ amplitude signal at $250Hz$ versus $I_{b3}$ at same input voltage amplitude.

The input-referred noise power spectral density of the VGLNP-4 is shown in Figure 2.40. The topology presents an integrated noise of $V_{n,rms} = 2.7\mu V_{rms}$, in a range frequency from $0.1Hz$ to $1kHz$, whereas from $0.1Hz$ to $115kHz$ the input noise is $8\mu V_{rms}$.

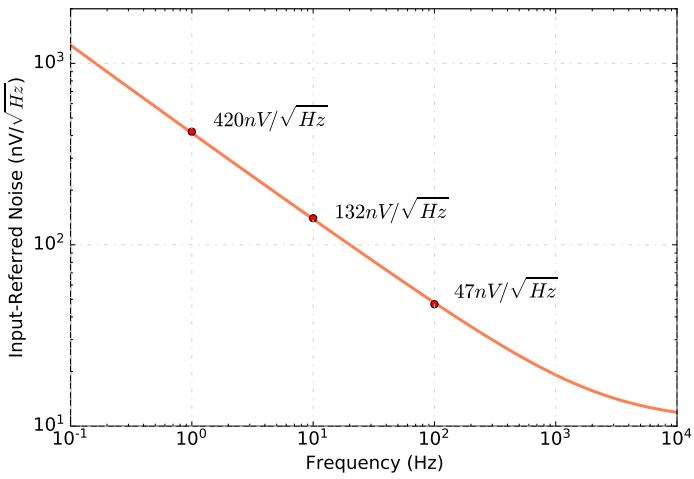



Figure 2.40: Input-referred noise of VGLNP-4.

Although the input-referred noise is higher than for the VGLNP-3 the VGLNP-4 was preferred because of its lower power consumption, more suitable for portable applications. For this reason, this configuration was chosen for integration.

### 2.3.6.2 Experimental Results

The VGLNP-4 was fabricated in 0.18$\mu m$ CMOS technology. The chip microphotograph and layout are shown in Figure 2.41. The area of the circuit is 450$\mu m$x100$\mu m$, which includes the high resistivity polysilicon resistors ($R_S$ and $R_L$), designed to be 10$k\Omega$ and 100$k\Omega$, respectively, as well as the CMFB circuit. In order to reduce flicker noise, transistor lengths were set to 3.6$\mu m$, which, together with interdigitation in the layout, also improves matching.

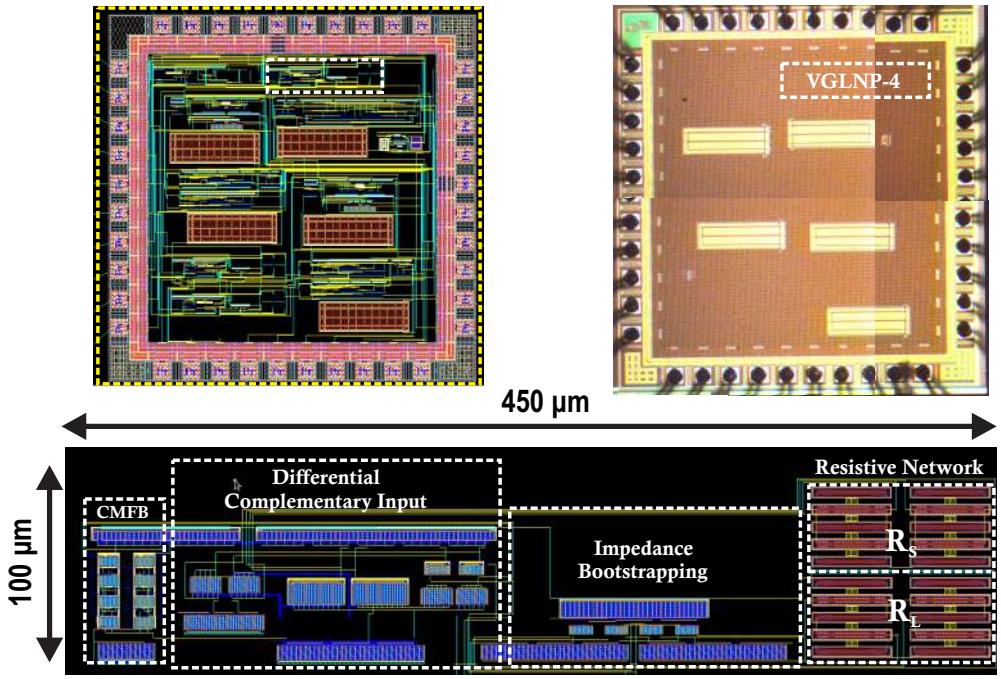
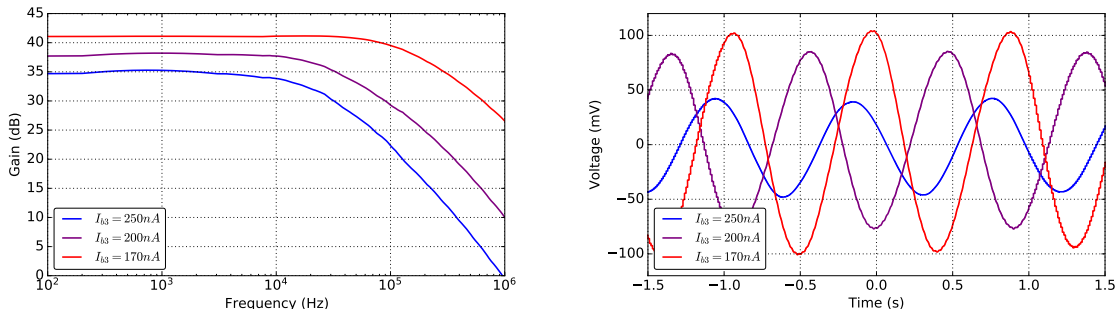



Figure 2.41: Microphotograph and layout of the VGLNP-4.

For experimental characterization the bias current $I_{B1}$ was set to 500$nA$, whereas $I_{B2}$ was set 250$nA$. The bias currents in the impedance scaler were $I_{b1} = I_{b2} = 600nA$ and $I_{b3}$ was varied from 170$nA$ to 250$nA$. The preamplifier provides a variable gain from 35$dB$ to 42$dB$, as shown in Figure 2.42a, where the bandwidth of the circuit varies from 11$kHz$ @ 35$dB$ to 100$kHz$ @ 42$dB$. Figure 2.42b shows the time response at different gain levels.




(a) (b)

Figure 2.42: Experimental characterization of the proposed VGLNP-4 a) Programmability of the gain and b) Time response taken from the oscilloscope.

The total harmonic distortion (THD) was also measured at several gain settings with a differential sine input voltage at $50Hz$. The measured THD is below $-40dB$ at $2mVpp$ for the three established gains, as shown in Figure 2.43. If the minimum gain is considered, the THD is below $-40dB$ up to an input amplitude voltage of $5mV$.

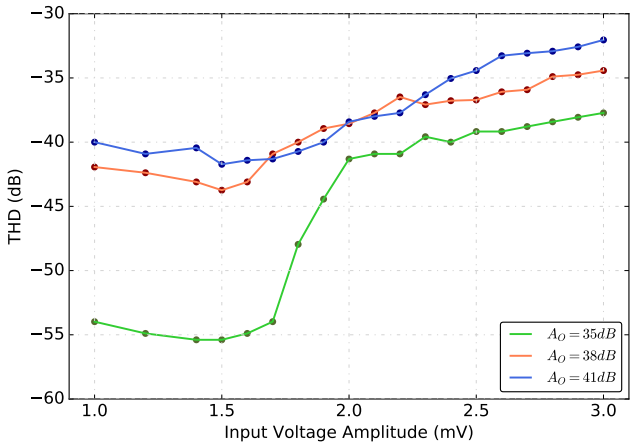



Figure 2.43: Output linearity measurements for several gains.

The input-referred noise power spectral density of the proposed preamplifier is shown in Figure 2.44. At $1kHz$ the input-referred noise is $18nV/\sqrt{Hz}$. When integrated from $100Hz$ to $100kHz$ the input-referred noise is $8.2\mu V_{rms}$. Simulation and experimental results are presented in Table 2.11.

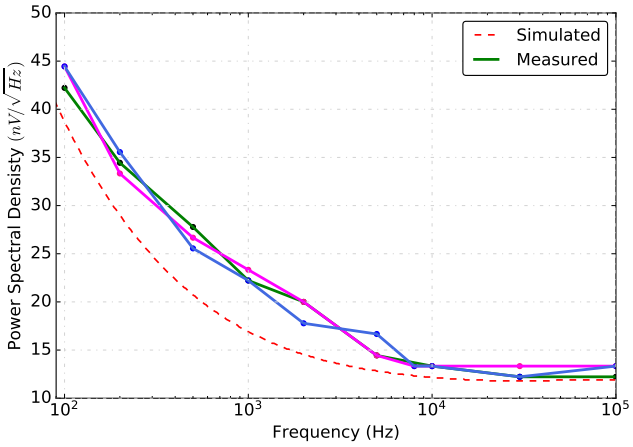



Figure 2.44: Input-referred noise power spectral density of VGLNP-4.

Table 2.11: Summary of Simulation and Experimental Results of VGLNP-4

| Parameters | VGLNP-4 | |
|---|---|---|
| | Simulation | Experimental |
| Technology ($\mu m$) | 0.18 | 0.18 |
| Power Supply ($V$) | 1.8 | 1.8 |
| Gain ($dB$) | 35.8 - 42.5 | 35 - 42 |
| Bandwidth ($kHz$) | 100 - 115 | 11 - 100 |
| Power ($\mu W$) | 9.45 | 12.3 |
| CMRR ($dB$) | 79 @ 250 Hz | - |
| PSRR ($dB$) | 80 @ 250 Hz | - |
| Input Voltage @ THD = $-40dB$ | 2.2 mVpp @ 250 Hz | 2 mVpp @ 50 Hz |
| Input-Referred Noise ($\mu V_{rms}$) | 8 | 8.2[1] |
| Mean Offset ($\mu V$) | 245 | - |

[1]Integrating from $100Hz$ to $100kHz$.

### 2.3.6.3 Comparative between the VGLNP-1 and the VGLNP-4

Table 2.12 shows a comparison between the experimental characterization of the proposed VGLNP-1 and VGLNP-4. The VGLNP-1 shows higher linearity, however, the gain is lower and the power consumption increases. In both cases, the gain can be adjusted though the bias currents. Under the same bias consideration in the impedance

scaler, the VGLNP-4 shows higher gain, even with lower bias current in the core transconductor. Furthermore the VGLNP-4 presents lower input-referred noise and lower power consumption, so it shows lower noise efficiency factors.

According to the experimental results, the VGLNP-4 presented a better performance, so it was used to implement two of the proposed chopping amplifiers in Chapter 4.

Table 2.12: Performance Comparison of VGLNP-1 and VGLNP-4

| Parameters | VGLNP-1 | VGLNP-4 |
|---|---|---|
| Technology ($\mu m$) | 0.18 | 0.18 |
| Supply ($V$) | 1.8 | 1.8 |
| Gain ($dB$) | 34 - 38 | 35 - 42 |
| Bandwidth ($kHz$) | 13 - 100 | 11 - 100 |
| Power ($\mu W$) | 22 | 12.3 |
| CMRR[1] @250 Hz ($dB$) | 76 | 79 |
| PSRR[1] @250 Hz ($dB$) | 76 | 80 |
| Input Voltage[2] @ THD= $-40dB$ | 3 mVpp | 2 mVpp |
| Input-Referred Noise[3] ($\mu V_{rms}$) | 11.8 | 8.2 |
| Mean Offset ($mV$) | 1.6 | 0.24 |
| Area ($mm^2$) | 0.004 | 0.0045 |
| $NEF$ | 5 | 2.6 |
| $PEF$ ($V$) | 45.1 | 12.2 |

[1]Simulation results, [2]At maximum gain, [3]Integrating from $100Hz$ to BW.

## 2.4 Comparison

In Table 2.13, the main characteristics of all the proposed LNPs and VGLNPs are presented. The LNP-0 shows low-noise and, due to the use of a polysilicon load resistor, good linearity, though at the cost of power consumption, which directly impacts its NEF. The LNP-1, in turn, presents low power consumption, with low input-referred noise and high linearity, but requires a $10M\Omega$ resistor to achieve high gain, which occupies a very large chip area, and makes it an unattractive option. To reduce the required area of the resistor at the output of the preamplifiers, the proposed low area and low power consumption bootstrapping resistor is used. As an additional feature, this block allows modifying the gain as a function of its bias currents. In this way, the VGLNP-2 presents the lowest noise power spectral density. Nevertheless, the output swing is limited and quickly saturates. As for the, VGLNP-4, it shows similar $NEF$ and $PEF$ values than the VGLNP-3, but with the lowest power consumption, so it was chosen for fabrication.

Finally, to better show the contribution of this chapter, the main characteristics of the VGLNP-4 prototype are summarized in Table 2.14 and compared to those of other integrated low-noise preamplifiers found in the literature.

VGLNP-4 presents a NEF of 2.6, very similar to that of [26] and only improved by [30]. However, [26] has a constant gain slightly lower than $40dB$. In addition, both [28] and [29] and [30] use a lower than nominal supply voltage ($1.8V$) to reduce the PEF. This implies that, to optimize the dynamic range of the conditioning circuit prior to converting the signal to digital, the following amplification stages will require a shift of the DC level.

Table 2.13: Performance Comparison with the Proposed Low-Noise Preamplifiers.

| Parameters | LNP-0 | LNP-1 | VGLNP-1 | | VGLNP-2 | VGLNP-3 | VGLNP-4 | |
|---|---|---|---|---|---|---|---|---|
| | Simulation | Simulation | Simulation | Experimental | Simulation | Simulation | Simulation | Experimental |
| Gain ($dB$) | 39.5 | 40.2 | 36 - 42 | 34 - 38 | 19 - 39.5 | 40 - 45.5 | 35.8 - 42.5 | 35 - 42 |
| Bandwidth ($kHz$) | 560 | 250 | 15 - 150 | 13 - 100 | 20 - 200 | 110 - 150 | 100 - 115 | 11 - 100 |
| Power ($\mu W$) | 70 | 15 | 16.2 | 22 | 15 | 17.1 | 9.45 | 12.3 |
| CMRR @250Hz ($dB$) | 74 | 81 | 76 | - | 65 | 75.5 | 79 | - |
| PSRR @250Hz ($dB$) | 70 | 84 | 76 | - | 69 | 76 | 80 | - |
| Input Voltage @ THD = $-40dB$ | 4 mVpp | 5.2 mVpp | 5.3 mVpp | 3 mVpp | 4.2 mVpp | 2.4 mVpp | 2.2 mVpp | 2 mVpp |
| Input-Referred Noise ($\mu V_{rms}$) | 9.7 | 13.2 | 11.6 | 11.8[1] | 4.7 | 5.4 | 8 | 8.2[1] |
| PSD ($nV/\sqrt{Hz}$) @ 100 Hz | 28 | 5 | 64 | 70 | 3.8 | 54 | 40 | 45 |
| Mean Offset ($mV$) | 1.3 | 1.3 | 1.6 | - | 1.5 | 1 | 0.24 | - |
| Load Resistor ($\Omega$) | 100 k | 10 M | 200 k | 200 k | 20 k | 100 k | 200k | 200k |
| Area ($mm^2$) | - | 0.2 | 0.004 | 0.004 | - | - | 0.0045 | 0.0045 |
| NEF | 3.1 | 2.9 | 3.2 | 5 | 3.7 | 1.65 | 2 | 2.6 |
| PEF ($V$) | 17.3 | 15.1 | 19.3 | 45.2 | 25 | 4.9 | 7.7 | 12.2 |

[1]Integrating from $100Hz$ to $BW$.

Table 2.14: Comparison with other LNPs in the Literature.

| Parameters | Wattanapanitch [26] 2007 | Zou [27] 2009 | Bidhendi [28] 2017 | Yu Wu [29] 2013 | Lee [30] 2018 | Ann-Ng [31] 2015 | **VGLNP-4** |
|---|---|---|---|---|---|---|---|
| Process ($nm$) | 500 | 350 | 180 | 180 | 180 | 65 | 180 |
| Supply ($V$) | 2.8 | 1 | 0.6 | 1 | 1.5 | 0.5 | 1.8 |
| Gain ($dB$) | 40.8 | 45.6 - 60 | 39 | 44.5 - 56 | 39.8 | 52.1 | 35-42 |
| Bandwidth ($kHz$) | 5.3 | 0.29 | 0.175 | 10 | 10 | 8.2 | 11 - 100 |
| Power ($\mu W$) | 7.5 | 0.89 | 0.69 | 13 | 3.28 | 2.8 | 12.3 |
| CMRR ($dB$) | 66 @5.3kHz | 71 @300Hz | 74 @- | - | 110 @1kHz | 80 @1kHz | 79[3] @250Hz |
| PSRR ($dB$) | 75 @5.3kHz | 84 @300Hz | 70 @- | - | 101 @1kHz | 78 @1kHz | 80[3] @250Hz |
| THD (%) @Input Voltage | 1@7.3mVpp | 0.6@- | 1@0.2mVpp | - | 0.4@4mVpp | 1@1.4mVpp | 1@2mVpp |
| Input-Referred Noise ($\mu V_{rms}$) | 3 (45Hz-5.3kHz) | 2.5 (0.05Hz-460Hz) | 2.3 (2Hz-175Hz) | 4.4 (0.1Hz-10kHz) | 3 (10Hz-10kHz) | 4.1 (1Hz-8.2kHz) | 8.2 (100Hz-100kHz) |
| Offset ($mV$) | - | - | - | - | - | - | 0.24[1] |
| Area ($mm^2$) | 0.16 | 1[2] | 0.0522 | 0.076 | 0.075 | 0.042 | 0.045 |
| NEF | 2.7 | 3.2 | 7.2 | 5.45 | 1.7 | 2.9 | 2.6 |
| PEF ($V$) | 19.9 | 10.6 | 31.3 | 29.7 | 4.3 | 8.6 | 12.2 |

[1]Mean value, [2]Area includes programmable gain amplifier, capacitor array and the digital comparator, [3]Simulation Results.

## 2.5 Conclusions

This chapter presents the proposal of an impedance scaler based on the bootstrapping technique suitable for the implementation of low noise preamplifiers. The advantage of this block is that the impedance programmability makes it possible to compensate for variations in the resistive value due to its manufacture, without a high impact on power consumption. Besides, the noise contributions are minimal, because the block is placed in the output nodes of the preamplifier. Six low-noise preamplifiers topologies were presented using different techniques, reducing noise at a topological level, analyzing the contributions of the topology itself. The proposed preamplifiers include a voltage-current conversion input stage, and a current-voltage output conversion stage, so a well-defined gain is achieved. The gain can be programmable, thanks to the use of the proposed impedance scaler. The preamplifiers were designed and simulated in a $0.18\mu m$ CMOS standard process. The VGLNP-1 and VGLNP-4 were fabricated in a $0.18\mu m$ CMOS standard process with $1.8V$ power supply. Experimental results show a low input-referred noise for the VGLNP-1 and VGLNP-4 with low power consumption. The proposed preamplifiers are a very competitive solution for the signal conditioning in portable applications.

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# Chapter 3

# Low Frequency Gm-C LPFs

The Gm-C technique, also called OTA-C, is the most popular technique used for the integration of continuous time filters in CMOS technologies due to its advantages in terms of tunability and simplicity [1-3]. The basic elements of Gm-C circuits are voltage-current converters (which in this Thesis will be interchangeably called Operational Transconductance Amplifiers, OTAs, or transconductors) and capacitors.

Gm-C filters, suffer from high variability to temperature, process and aging variations; thus, some tuning is needed to keep the frequency response within its specifications. Fortunately, the frequency response of the Gm-C can be controlled by the transconductance of the voltage-current converters and/or the capacitances. The usual way of tuning the transfer function of a filter is by adjusting the bias current of the transconductors.

The main block for continuous time filter implementation is the integrator, shown in Figure 3.1, whose transfer function is given by:

$$\frac{V_{out}}{V_{in}} = \frac{G_m}{sC} \tag{3.0.1}$$

Therefore, the output voltage is equal to the integration of the differential input voltage multiplied by the unity-gain frequency, which is given by:

$$f_u = \frac{G_m}{2\pi C} \tag{3.0.2}$$

where $G_m$ is the transconductance of the OTA and C is the capacitor value.

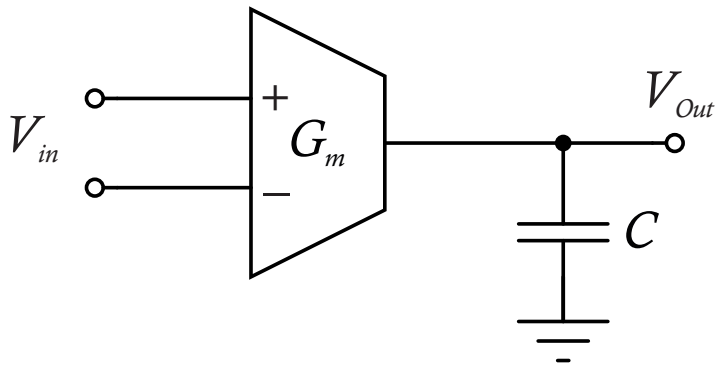



Figure 3.1: Single-ended Gm-C Integrator.

Low-pas filters are connected to the output of low-noise preamplifiers in order to limit the bandwidth of the conditioning system and thus reduce noise contribution [1-9]. In the case of chopping amplifiers, the output low-pass filter is responsible for removing the modulated low-frequency noise as well as undesired harmonics generated by the chopping technique, so the cut-off frequency is required to be as low as possible to filter out unwanted signals and eliminate the offset effectively.

To compare the performance of low-pass analog filters, several figures of merit (FOMs) are introduced [10-11]. These figures of merit involve the main parameters of filter performance: power consumption, dynamic range (DR), order of the filter (n), bandwidth (BW) and area consumption.

The dynamic range is defined as the ratio of the maximum and minimum level which the circuit can handle. The minimum signal level is determined by noise and the maximum level by total harmonic distortion. Dynamic range can be defined as:

$$DR = \frac{V_{signal,rms}}{V_{noise,rms}} \tag{3.0.3}$$

The first FoM is the relationship between the normalized power (NP), the order of the filter and the dynamic range, and is given by:

$$FoM_1 = \frac{NP}{n \cdot DR} \tag{3.0.4}$$

where the normalized power is defined as $NP = Power \cdot [0.5/(V_{DD} - V_{th})] \cdot (1/V_{DD})$. The second FoM takes into account the required area for the implementation on chip and the cut-off frequency. This FoM is given by:

$$FoM_2 = \frac{Power \cdot BW \cdot NA}{n \cdot DR} \tag{3.0.5}$$

where normalized area is defined as $NA = area/Tech^2$, $Power$ is the power consumption and $BW$ the bandwidth of the filter.

In order to achieve low cut-off frequencies, large capacitors and/or large resistors are required, which are impractical in fully integrated solutions. For this reason, other approaches to achieve large time-constants have been proposed in the literature, such as the use of capacitance multipliers or pseudo-resistors [12-13]. However, these techniques suffer from large area and high non-linearity, respectively, limiting their application. A popular approach to achieve low frequencies without sacrificing area or linearity is to use of $Gm$-$C$ filters based on very low $G_m$ OTAs [14-18]. CMOS OTAs designed in strong-inversion normally have a transconductance in the order of $\mu A/V$, whereas OTAs in weak inversion have a transconductance in the order hundreds of $nA/V$ [9]. To further reduce the transconductance, other approaches are necessary, as will be commented in the next Section.

This chapter presents four continuous time low-pass filters designed in a $0.18\mu m$ CMOS process with $1.8V$ power supply. First, the use of the bootstrapping technique presented in Section 2.1 to design low-Gm transconductors is showed, and then the low-frequency low-pass filters designs are shown. Simulation results are presented, and experimental measurements are shown in the case of the configurations that were fabricated. Finally, the proposed filters are compared with each order and with other implementations found in the literature in order to highlight the advantages and disadvantages of each proposal.

## 3.1 Proposed $Gm$-$C$ Reduction Technique

There are several techniques to design low $G_m$ transconductors. In the triode region, for example, it is possible to exploit the benefits of the smaller $g_m/I_D$ ratio, obtaining small transconductances without increasing the power consumption; however, the linearity is degraded [19]. Another way to reduce transconductance is to use the bulk-driven approach, as the bulk transconductance $g_{mb}$ is typically 0.2 to 0.4 times $g_m$. However, the input impedance depends in this case on the input signal value [20-22]. Current attenuation, consists in reducing the output current of the OTA by using current mirrors with large division factors. These current mirrors are sometimes based on series-parallel transistor structures to achieve a small copy factor, increasing the area of the circuit [4,23]. Another current attenuation technique is the so called current-steering approach, which provides programmability and current reduction using voltage-controlled current mirrors implemented via unbalanced differential pairs [24]. The main disadvantage of this technique is the control voltage range, which limits the transconductance range, and that some times the current of one of the branches is waisted. The current cancellation technique, in turn, reduces the equivalent $G_m$ of the OTA by splitting each input transistor in the differential pair into two parallel transistors, one of them carrying $N$ times the current through the other. When cross-coupling the drains of these split input transistors, the transconductance is reduced by a factor $(N-1)/(N+1)$. This configuration is sensitive to mismatch, so $N$ cannot be arbitrarily close to 1 and therefore the reduction in $G_m$ is limited [25-26]. Another alternative is the use of a capacitive network at the input of the OTA to reduce its transconductance [27]. The main disadvantages of this technique are the DC offset and the increased area due to the capacitors. Although the input voltage attenuator can also be implemented with an active cell to reduce the required area, this implies an increase in the noise contribution of the OTA. Finally, many authors use a combination of two or more of these techniques to further reduce $G_m$, without avoiding the trade-offs of each of them [4,26].

To avoid all these limitations, novel low-Gm transconductors based on the bootstrapping technique presented in Section 2.2 are proposed. To keep a high input impedance, the technique is applied as shown in Figure 3.2a [28]. As in the implementation of the impedance scaler in Chapter 2, the current $I_R$ through the resistor $R$ is copied to the output branch, but in this case that current is not supplied by the input. A possible practical implementation is the one shown in 3.2b, where the amplifiers $A_1$ and $A_2$ are

implemented with the source followers $M_{SF1}$ and $M_{SF2}$, and the $I_R$ current is copied to the output branch by the mirror $M_3$-$M_4$. In this way, low transconductance is achieved, which can be adjusted by means of the bias currents $I_{B1}$ and $I_{B2}$. A PMOS configuration was chosen to avoid body-effect by tying bulk and source together, and to reduce flicker noise.

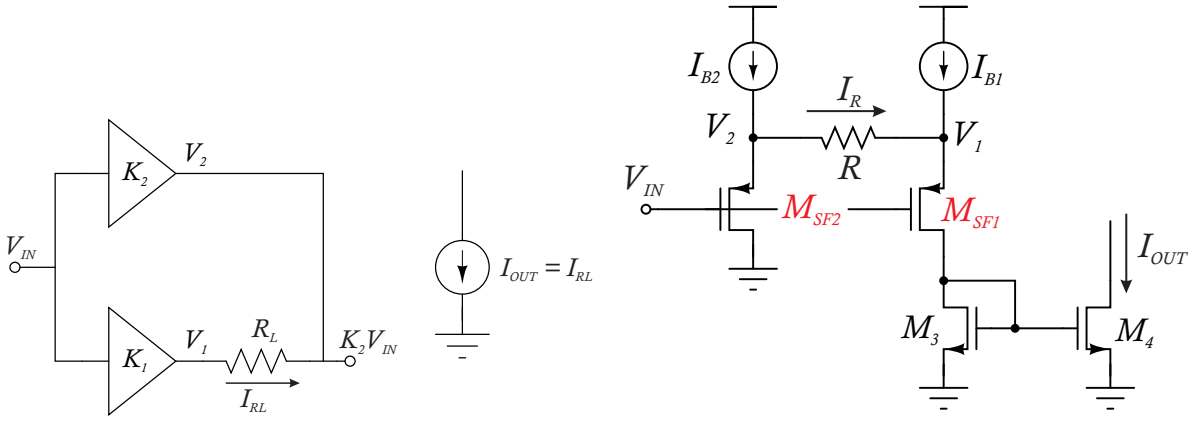



Figure 3.2: a) Block diagram of the proposed Gm reduction technique and b) Circuital implementation.

As transistors are biased in weak inversion, the voltages at nodes $V_1$ and $V_2$ are given by:

$$V_{1,2} = V_{in} - n_s V_t \cdot \ln\left[\frac{I_{SF1,2}}{I_S}\right] \tag{3.1.1}$$

where $I_{SF1} = I_{B1} + I_R$, $I_{SF2} = I_{B2} - I_R$, $V_t$ is the thermal voltage, $n_s$ is the slope factor and $I_S$ is the characteristic current. If $I_R << I_{B1}, I_{B2}$, as will be the case, a truncated Taylor expansion can be used to find the approximate value of $I_R$:

$$I_R \approx \frac{-n_s V_t I_{B1} I_{B2}}{R I_{B1} I_{B2} + n_s V_t (I_{B1} + I_{B2})} \cdot \ln\left[\frac{I_{B1}}{I_{B2}}\right] \tag{3.1.2}$$

From this equation, it is observed that a DC current is established through $R$ if the bias currents $I_{B1}$ and $I_{B2}$ are not equal. Furthermore, ideal current sources have been considered in this analysis and, as a result, the gain of both source followers is forced to be $A_1$=$A_2$=1, so the transconductance of the proposed circuit is $G_m = 0$, as expected.

Now let $r_{B1}$ and $r_{B2}$ be the output resistances of the current sources $I_{B1}$ and $I_{B2}$, respectively. If $r_{B1} r_{B2} R >> r_{B1}, r_{B2}$, $R$, it can be shown that the small signal current $i_R$ which flows through $R_S$ is given by:

$$i_R = \frac{(g_{m1}r_{B1} - g_{m2}r_{B2}) \cdot v_{in}}{R(g_{m1}r_{B1} + g_{m2}r_{B2}) + r_{B1}r_{B2}(g_{m1} + g_{m2} + g_{m1}g_{m2}R)} \tag{3.1.3}$$

where $g_{m1}$ is the transconductance of $M_{SF1}$ and $g_{m2}$ is the transconductance of $M_{SF2}$. Assuming $g_{m1}r_{B1} >> 1$ and $g_{m2}r_{B2} >> 1$, equation (3.1.3) can be approximated by:

$$G_m = \frac{\Delta(g_m \cdot r_B)}{g_{m1}g_{m2}r_{B1}r_{B2}R} \tag{3.1.4}$$

where $\Delta(g_m r_B)$ represents the difference between $g_{m1}r_{B1}$ and $g_{m2}r_{B2}$. If both branches are designed to be identical, with the same bias current $I_{B1}$=$I_{B2}$, the ideal transconductance is $G_m = 0$, since $A_1$=$A_2$, as expected. In practice, however, the actual transconductance under these conditions would be determined by mismatch, and it would not be possible to predict its polarity, resulting in potentially unstable systems if using the OTA in closed loop configurations. For this reason, it is not advised to use the same bias current in both branches. It can be noted, however, than even if $I_{B1} \neq I_{B2}$, $g_{m1}r_{B1}$ and $g_{m2}r_{B2}$ can still be similar, and the high-value resistance in the denominator in equation (3.1.4) still ensures a low equivalent transconductance. Note that the output resistance $r_{B1}$ of the bias current $I_{B1}$ sets a minimum transconductance limit, due to the fact that, if the signal current flowing through $R$ is much lower than the current through $r_{B1}$, the equivalent resistance seen at the source of $M_{SF1}$ is $r_{B1}$. This technique will be used for the design of several low Gm transconductors.

## 3.2 Proposed Low-Gm OTAs

In this Section several low-Gm OTAs are presented. Except for the first one, all of them are based on the technique proposed in the previous Section.

### 3.2.1 FVF-based Low-Gm OTA (LGmOTA-0)

Figure 3.3 shows the LGmOTA-0, which consists of a FVF-based source degenerated transconductor. The output current through $M_5$ and $M_6$ is determined by the differential input voltage and the degeneration pseudo-resistor $PR_S$. The output current is copied through $M_7$ and $M_8$. The CMFB circuit consists of a differential difference amplifier not shown in Figure 3.3.

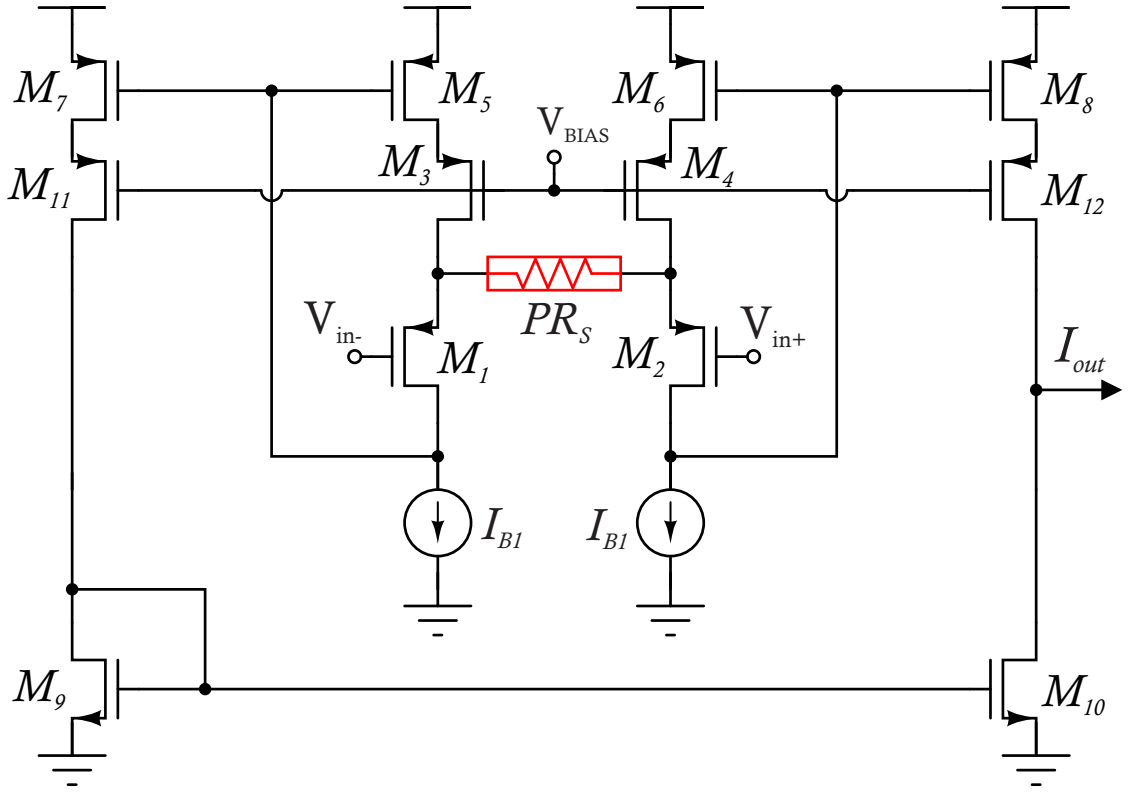



Figure 3.3: FVF-based low-Gm OTA (LGmOTA-0).

To achieve a low transconductance, a degeneration resistor in the order of tens of $M\Omega$ is required. In order no to increase the area, it is implemented with a pseudo-resistor instead of a polysilicon resistor. Figure 3.4 shows the implementation of the $PR_S$ [35].

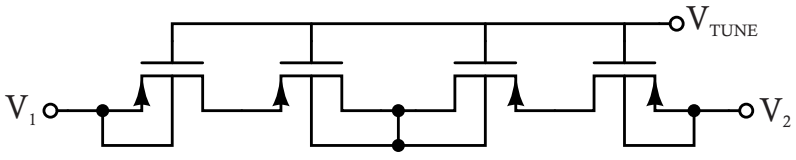



Figure 3.4: Pseudo-resistor implementation.

With this architecture, it is possible to achieve small transconductances as a function of the degenerated resistance without the need for additional Gm reduction techniques.

#### 3.2.1.1 Simulation Results

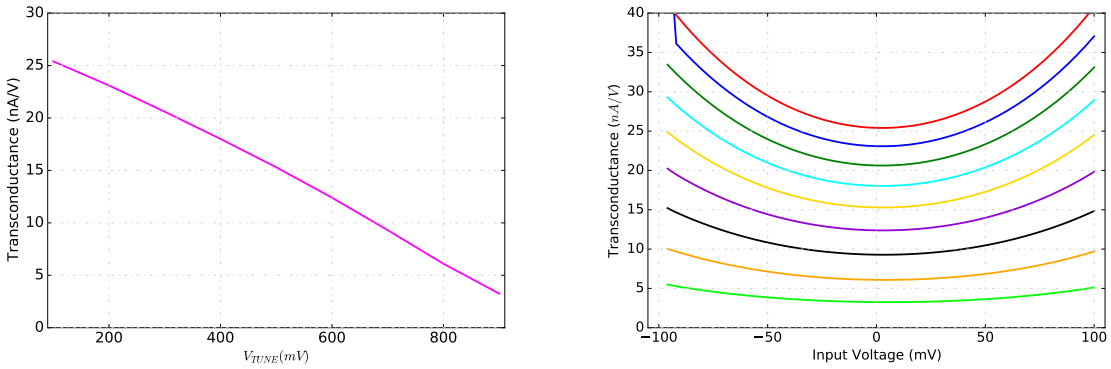
The LGmOTA-0 was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage, and consumes $9\mu W$ with the bias current set to $I_{B1} = 1\mu A$. The dimensioning of LGmOTA-0 is presented in Table 3.1.

Table 3.1: Transistor Size of Low-Gm OTA-0

| Transistor | $M_{1,2}$ | $M_{3,4}$ | $M_{5,6}$ | $M_{7,8}$ | $M_{9,10}$ | $M_{B1}$ | $M_{B2}$ |
|---|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 528/1 | 28/1 | 88/1 | 132/1 | 352/1 | 112/1 | 352/1 |

In the pseudo-resistor (Figure 3.4), the PMOS transistors are biased in weak-inversion and either their bulk-drain or their bulk-source terminals are short-circuited. Although high resistance values are achieved, the THD is degraded due to the non-linearity of the MOS transistors. The main advantage is that the equivalent resistance can be modified through $V_{TUNE}$ and, in this way, process variations can be compensated.

The LGmOTA-0 exhibits a variable $G_m$ from $3.25nA/V$ to $25nA/V$, when $V_{TUNE}$ is varied from $100mV$ to $900mV$, as shown in Figure 3.5a. Figure 3.5b shows the dependence of transconductance on the input voltage which results in signal distortion.

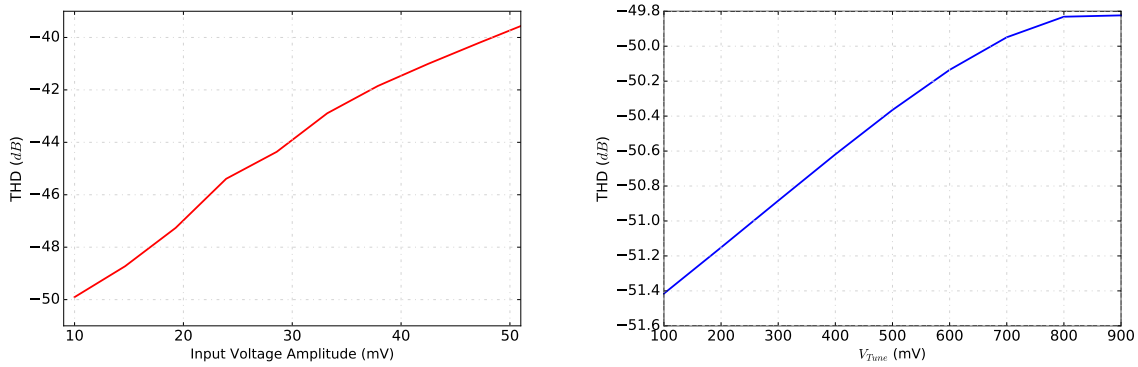



(a) (b)

Figure 3.5: a) Transconductance as a function of $V_{TUNE}$ and b) dependence of Gm on $V_{in}$ og the LGmOTA-0.

Figure 3.6a shows the total harmonic distortion for a sine differential input voltage at $1kHz$ with amplitude varying from $10mV$ to $50mV$ with $V_{TUNE} = 400mV$ and a transconductance $G_m = 10nA/V$. The THD remains below $-40dB$ for input voltages up to $100mVpp$. Figure 3.6b shows the THD when the transconductance changes due

to the change in $V_{TUNE}$, for a sine amplitude voltage of $10mV$. In this case, when the transconductance is reduced, the THD increases.




(a) (b)

Figure 3.6: a) THD for different input voltage amplitudes and b) THD by modifying $V_{TUNE}$ at same input voltage amplitude ($10mV$).

Finally, Figure 3.7 shows the input-referred noise power spectral density. At $10Hz$ the input-referred noise is $28\mu V/\sqrt{Hz}$. Integrating from $0.1Hz$ to the bandwidth the input-referred noise is $150\mu V_{rms}$. The main characteristics of the low transconductance LGmOTA-0 are summarized in Table 3.2.

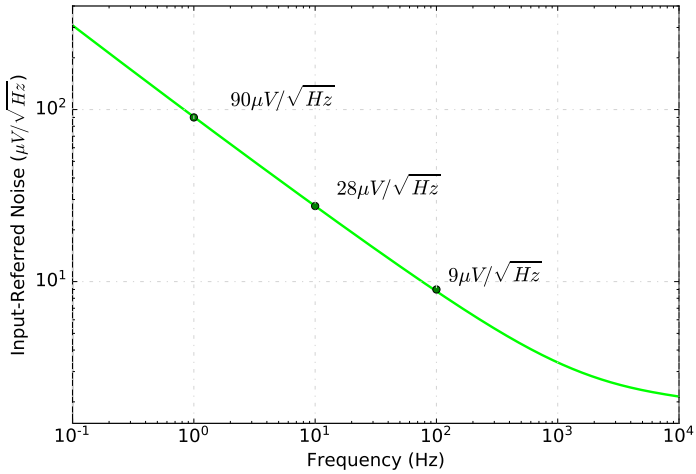



Figure 3.7: Input-Referred Noise of the LGmOTA-0.

Table 3.2: Characteristics of the Low-Gm OTA-0.

| Parameters | LGmOTA-0 |
|---|---|
| Process | 0.18 $\mu m$ |
| Supply | 1.8 $V$ |
| Gm | 3.25 - 25 $nS$ |
| Bandwidth | 560 $kHz$ |
| Power | 9 $\mu W$ |
| THD @ Input Voltage | 1% @ 100 $mVpp$ |
| Power Spectral Density | 9 $\mu V/\sqrt{Hz}$ @ 100$Hz$ |
| Input-Referred Noise | 150 $\mu V_{rms}$ (0.1$Hz$-$BW$) |

### 3.2.2 Low-Gm OTA-1 (LGmOTA-1)

The proposed LGmOTA-1, shown in Figure 3.8, is a pseudo-differential configuration. It consists of two $G_m$-reduction blocks with PMOS input transistors $M_1$ to $M_4$ acting as source followers (as proposed in Section 3.1) [28]. The bias current sources are implemented with single transistors $M_{11}$ to $M_{14}$, whose currents are set through $I_{B1}$ and $I_{B2}$. The output current of each block is copied to the output branch through simple current mirrors so that the DC component is ideally cancelled out. In order to validate the proposed technique, these current mirrors have no gain, though an attenuation factor could be added to further reduce $G_m$. The equivalent transconductance of the LGmOTA-1 can be written, based on equation (3.1.4), as:

$$G_m = \frac{2(g_{mSF1}r_{o13} - g_{mSF3}r_{o11})}{g_{mSF1}g_{mSF3}r_{o13}r_{o11}R} \tag{3.2.1}$$

where $r_{o11}$ is the output resistance of $M_{11}$-$M_{12}$, $r_{o13}$ the output resistance of $M_{13}$-$M_{14}$ and $g_{mSF1}$ and $g_{mSF3}$ the transconductance of $M_1$-$M_2$ and $M_3$-$M_4$, respectively.

#### 3.2.2.1 Experimental Results

The LGmOTA-1 was fabricated in a 0.18$\mu m$ standard CMOS process with 1.8$V$ supply voltage. The chip microphotograph and layout are shown in Figure 3.9. The area of the circuit is 110$\mu m$x90$\mu m$, which includes the high resistivity polysilicon degeneration resistors $R$, designed to be 100$k\Omega$ each. In order to achieve good matching, interdigitation was used in the layout and transistor lengths were set to 0.36$\mu m$.

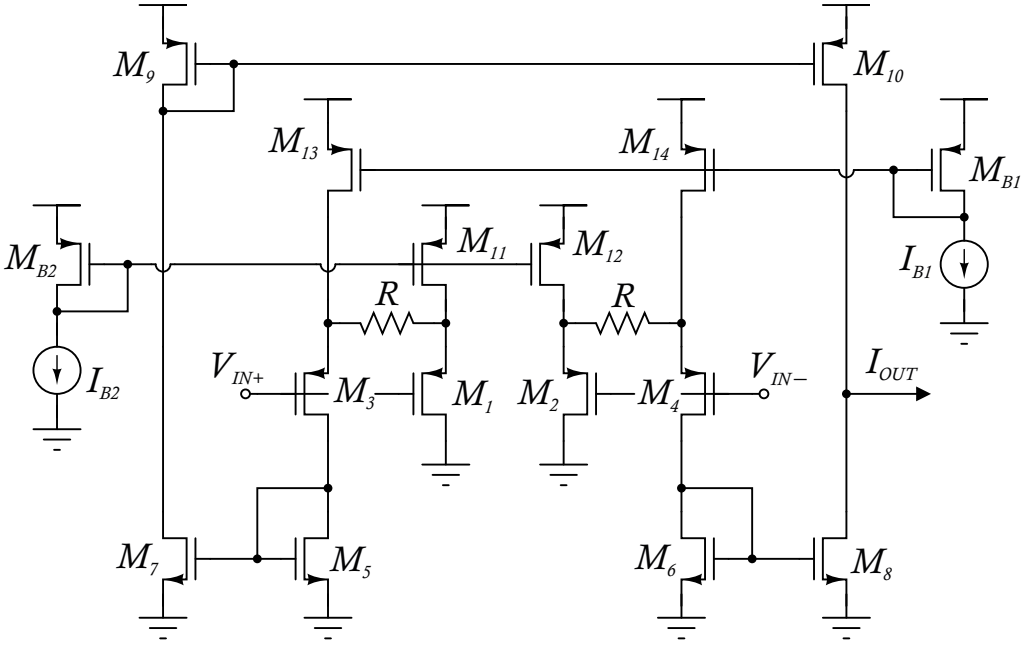



Figure 3.8: Proposed LGmOTA-1.

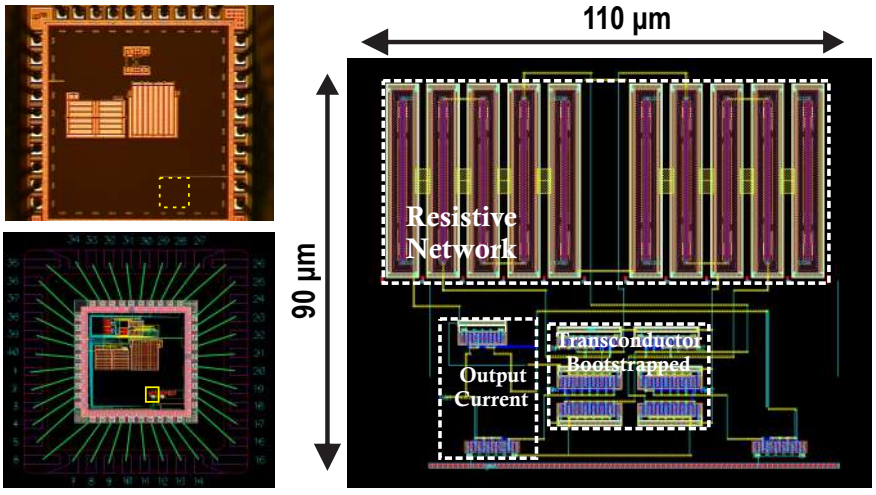



Figure 3.9: Microphotograph and layout of the LGmOTA-1.

For experimental characterization the bias current $I_{B2}$ was set to $1\mu A$, whereas $I_{B1}$ was varied from 20.5 to $72nA$. Each current was generated via an external potentiometer and a two channel signal generator was used to apply the differential input voltage. The

OTA exhibits a power consumption of $4\mu W$, and provides a variable $G_m$ from $15nA/V$ to $18.5nA/V$, as shown in Figure 3.10.

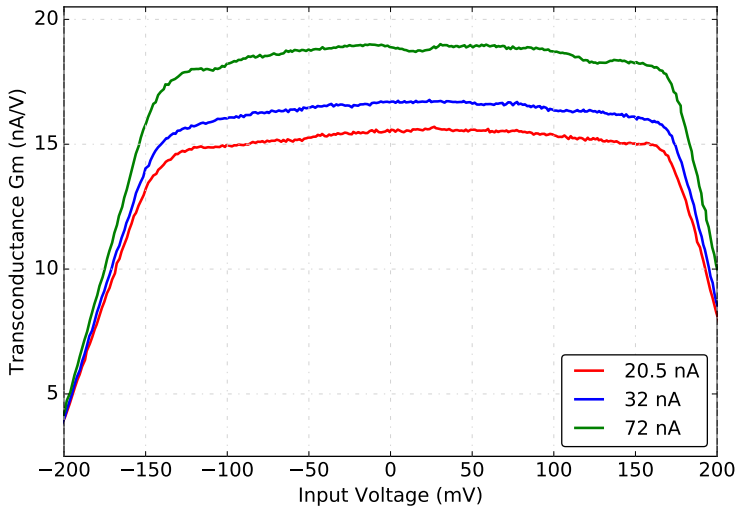



Figure 3.10: Measurement results of transconductance as a function of the differential input voltage, for several $I_{B1}$ values.

Figure 3.11 shows the total harmonic distortion (THD) for a sine differential input voltage at $1kHz$ varying from $50mVpp$ to $350mVpp$. The characterization was carried out at each $G_m$ setting and it shows that, in all cases, the THD remains below $-40dB$ for input voltages up to $340mVpp$. Experimental results of the proposed LGmOTA-1a are summarized in Table 3.3.

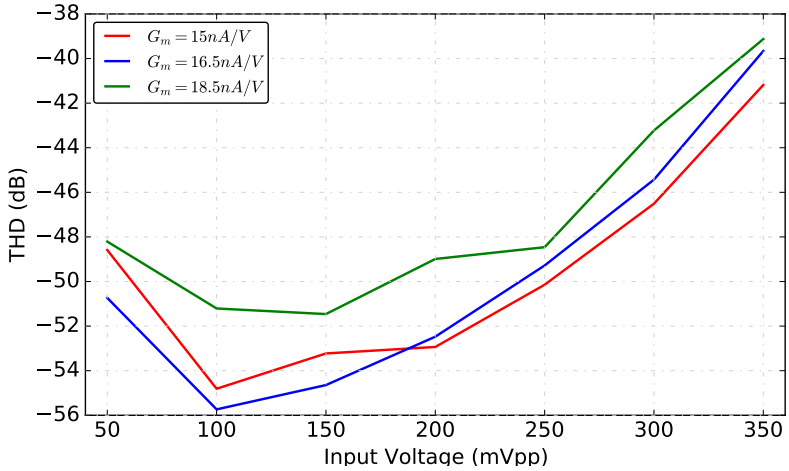



Figure 3.11: Measurement results of THD versus input voltage for several $I_{B1}$ values.

Table 3.3: Characteristics of the Low-Gm OTA-1.

| Parameters | LGmOTA-1 |
|---|---|
| Process | 0.18 $\mu m$ |
| Supply | 1.8 $V$ |
| Gm | 15 - 18.5 $nS$ |
| Bandwidth | 15 $kHz$ |
| Power | 4 $\mu W$ |
| THD @ Input Voltage | 1% @ 340 $mVpp$ |
| Power Spectral Density | 70.3 $\mu V/\sqrt{Hz}$ @ 100$Hz$ |
| Input-Referred Noise | 475 $\mu V_{rms}$ (0.1$Hz$-$BW$) |

#### 3.2.2.2 Second Order Effects

In order to gain more in-depth understanding of the proposed OTA operation, some simulations are provided that show the impact of the chosen current mirrors and mismatch on the characteristics.

#### 3.2.2.3 Impact of $r_{B1}$

The OTA shown in Figure 3.8 is the simplest implementation derived from the proposed Gm reduction technique, and was integrated to prove the effectiveness of this approach. However, in an extreme case, when the signal current flowing through R is much lower than the current through the output resistor $r_{B1}$ of the bias current source ($M_{13}$, $M_{14}$), $r_{B1}$ actually sets a minimum transconductance limit. To show the effect of this limitation, simulations were carried out to see the dependence of $G_m^{-1}$ on the value of R, both with simple current sources and when replacing $M_{13}$ and $M_{14}$ by cascode configurations. As shown in Figure 3.12, the value of $G_m^{-1}$ when using simple current sources tends to saturate as R increases, due to the limit established by $r_{B1}$. As for the case with cascode current sources, with an output resistance about 20 times higher, the value of $G_m$ was decreased (as predicted by equation (3.1.4)) and no saturation of $G_m^{-1}$ is observed in the considered range of R.

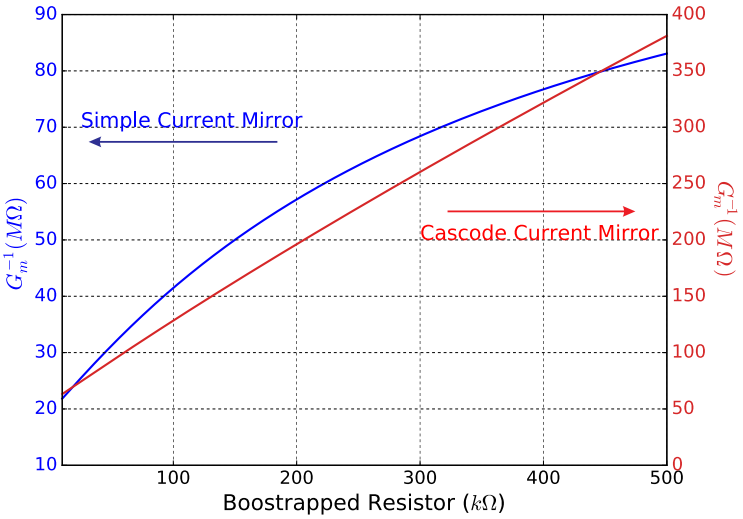



Figure 3.12: Equivalent resistance $G_m^{-1}$ using simple and cascode current mirrors.

#### 3.2.2.4 Current Mirror Effects

From the DC analysis in Section 3.1 it was shown that the proposed Gm reduction technique can provide very high linearity, as the output current is independent of the input voltage in a first order approximation. In practice, the linearity of the integrated OTA will be limited by the distortion introduced by the output current mirrors, $M_5$-$M_{10}$.

To prove this, simulations were carried out where these current mirrors were substituted by cascode current mirrors, which not only provide higher output resistance and accuracy in the copy, but also higher linearity. By doing so, the transconductance of the OTA with $I_{B1} = 72nA$ was decreased from $21nA/V$ to $16.5nA/V$, due to a more accurate current copy to the output. Figure 3.13 shows the THD in both cases, for sine input voltages ranging from $40mVpp$ to $350mVpp$ at $1kHz$. In order to compare the THD also at the same output levels, $I_{B1}$ was increased to $100nA$ in the cascode current mirror implementation to obtain the same $G_m = 21nA/V$ than in the simple case. As shown, the harmonic distortion in mainly determined by the current mirrors, and an improvement in their linearity highly impacts on the THD of the whole topology. In particular, the use of cascode current mirrors reduced the THD of the OTA around $6dB$.

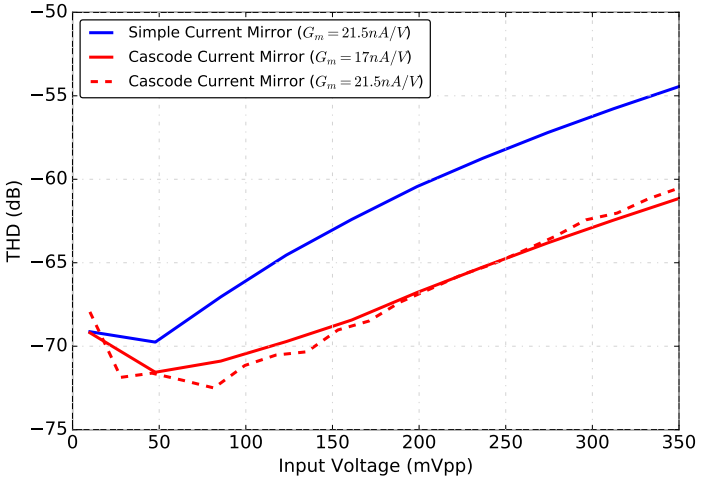
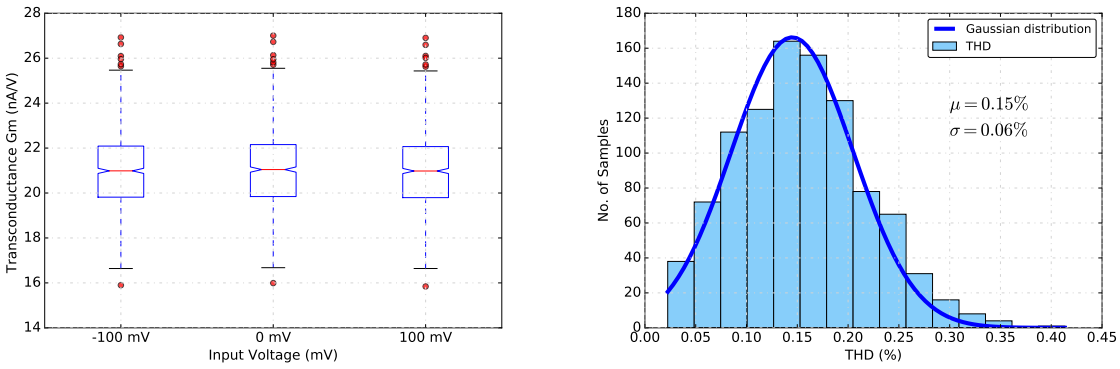



Figure 3.13: Simulation results of THD with different current mirrors.

#### 3.2.2.5 Mismatch Effects

In order to determine the impact of mismatch on $G_m$ and THD, Monte Carlo simulations (1000 runs each) of the LGmOTA-1 with $I_{B1} = 70nA$ and $I_{B2} = 1\mu A$ were carried out. Figure 3.14a shows the impact of mismatch on $G_m$, at three different input voltage amplitudes ($-100mV, 0mV$ and $100mV$). The red line in the box plot indicates the mean value of the transconductance, which is $21.5nA$ in all three cases with a standard deviation of $1.5nA/V$. As shown, the distribution is symmetric. The boxes cover the interquartile range of the distribution, i.e., 50% of the measurements lie in the range from $19.7nA/V$

to $22nA/V$. Figure 3.14b shows the THD histogram for an input voltage of $350mVpp$ at $1kHz$, which has a mean value of 0.15% and 0.06% standard deviation.




(a) (b)

Figure 3.14: Monte Carlo simulations for Mismatch a)Transconductance Box Plot and b)THD Histogram.

### 3.2.3 Comparison

Table 3.4 shows a comparison with previous low-$G_m$ OTAs found in the literature. The highest linearity is achieved in [31] and [34], at a cost of high voltage supply and high power consumption, in the first case, and, though not mentioned in the paper, at a cost of variable input impedance due to the rail-to-rail input operation in a bulk-driven configuration [22], in the second case. In contrast, the proposed LGmOTA-1 shows high linearity with moderate power consumption, low noise contribution and low area consumption. In particular, THD is 1% for a $350mVpp$ sine input signal at $1kHz$, and decreases down to 0.15% for a $100mVpp$ input. This THD would be even lower if simple current mirrors in the topology were replaced by cascode configurations, as will be shown in Section 3.2.2.4. It must also be noted that large bias currents were used during the characterization process due to experimental limitations. Even so, the power consumption is reduced when compared to OTAs based on current attenuation, such as [31] and [33], since there is no current waste. Furthermore, simulations show that the power consumption of the proposed topology can be decreased down to the order of hundreds of $nW$.

Table 3.4: Performance Comparison with other Low-$G_m$ Transconductors

| Parameter | [19]' 08* | [29]' 12 | [30]' 14 | [31]' 14 | [32]' 19 | [33]' 19 | [34]' 20 | **LGmOTA-1** |
|---|---|---|---|---|---|---|---|---|
| Process ($\mu m$) | 0.35 | 0.35 | 0.13 | 0.35 | 0.18 | 0.18 | 0.18 | 0.18 |
| Supply ($V$) | 1.5 | 0.8 | 0.25 | ±2.5 | 0.3 | 1.8 | 1 | 1.8 |
| Technique | Triode Region | Bulk Driven | Bulk Driven | Current Attenuation | Bulk Driven | Current Attenuation | Bulk Driven | Boots-trapping |
| Gm ($nA/V$) | 1 - 12 | 66 | 22 | 39.5 - 367 | 68 - 460 | 0.5 - 5000 | 0.62 - 6.28 | 15 - 18.5 |
| Power ($\mu W$) | <0.3 | 0.04 | 0.01 | 160 | 0.05 | 5.4 | 0.27 | 4 |
| BW ($Hz$) | 14.6 | 195 | - | - | 50 - 334 | 5.2 k | 100 | 15 k |
| THD (%) | 1 % @200 mVpp - | 1 @100 mVpp 10 Hz | 0.53 @100 mVpp - | 0.13 % @ 2 Vpp $1kHz$ | 0.47 @100 mVpp $100Hz$ | 1 @220 mVpp $5Hz$ | 0.18 @2 Vpp - | 1 @ 350 mVpp $1kHz$ |
| Input Referred Noise PSD ($\mu V/\sqrt{Hz}$) | 74 @10 Hz | - | - | - | 1.3 ** @10 Hz | - | - | 70.3 @100 Hz |
| Input Referred Noise $V_{rms}$ ($\mu V_{rms}$) | - | 80 (0.2 - 200) Hz | 100 (0.1 - 200) Hz | 332 (10 - 30k) Hz | - | 16.3 (0.06 - 5) Hz | 760 (1 - 100) Hz | 475 (1 - 1k) Hz |
| Area ($mm^2$) | - | 0.04 | 0.0053 | 0.006 | 0.035 | 0.014 | 0.027 | 0.0099 |

* Simulation results. ** Thermal Noise level, the corner frequency for $1/f$ noise was around $4Hz$ (stated in ref [32]).

### 3.2.4 Low-Gm OTA 2a (LGmOTA-2a)

Figure 3.15 shows the LGmOTA-2a, a pseudo-differential OTA which consists of two bootstrapped resistance blocks with NMOS/PMOS complementary input transistors ($M_1$ to $M_8$) acting as source followers. The transistors $M_9$ to $M_{16}$ are current mirrors, copying the bias current $I_{Bi}$ established by the gate voltage $V_{Bi}$, with $i = 1, 2, 3, 4$. The output current of each block is copied to the output branch through simple current mirrors. Finally, the LGmOTA-2a uses current cancellation in the output branches, in order to further reduce the transconductance $G_m$.

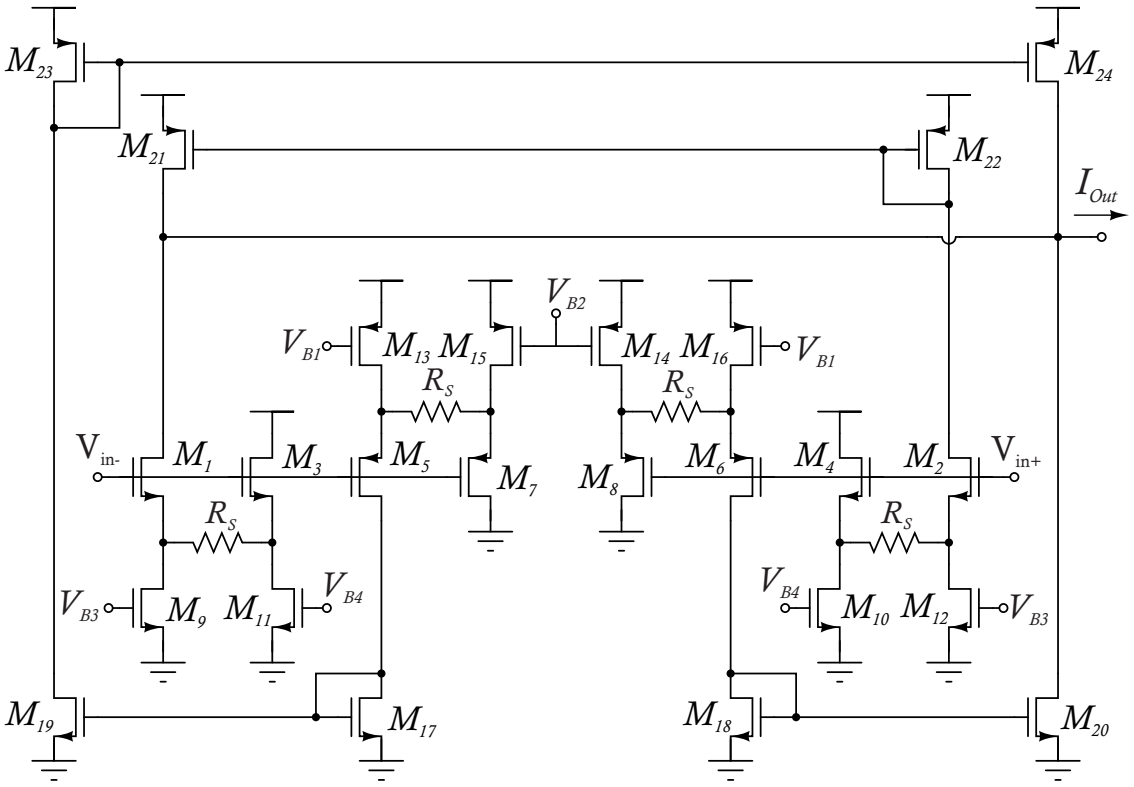



Figure 3.15: Bootstrapping Technique based LGmOTA-2a.

Assuming $g_{mpmos}r_{Bpmos}, g_{mnmos}r_{Bnmos} >> 1$, the transconductance can be approximated by:

$$G_m = \frac{\Delta(g_{mpmos}r_{Bpmos})}{g_{m3}r_{B3}g_{m7}r_{B7}R_S} - \frac{\Delta(g_{mnmos}r_{Bnmos})}{g_{m1}r_{B1}g_{m2}r_{B2}R_S} \tag{3.2.2}$$

where $\Delta(g_{mi}r_{Bi})$ represents the difference between $g_{m3}r_{B3}$ and $g_{m7}r_{B7}$ for $i = pmos$, and between $g_{m1}r_{B1}$ with $g_{m2}r_{B2}$ for $i = nmos$.

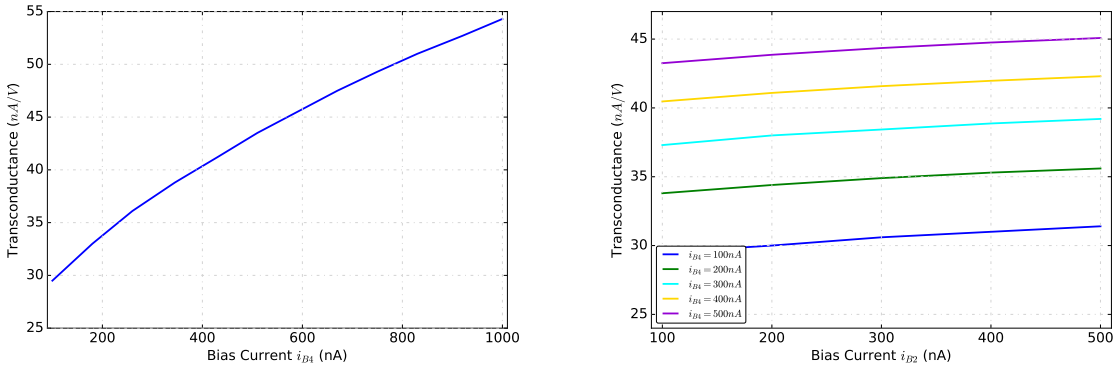
### 3.2.4.1 Simulation Results

The LGmOTA-2a was designed in a $0.18\mu m$ CMOS process with $1.8V$. The sizing of the transistors is shown in Table 3.5. The circuit was designed to operate in weak inversion.

Table 3.5: Transistor Size of Low-Gm OTA 2a

| Transistors | $M_{1,2,3,4}$ | $M_{5,6,7,8}$ | $M_{9,10,11,12}$ | $M_{13,14,15,16}$ | $M_{17,18,19,20}$ | $M_{21,22,23,24}$ |
|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 36/3.6 | 72/3.6 | 72/3.6 | 36/3.6 | 72/3.6 | 36/3.6 |

The OTA exhibits a power consumption of $5.2\mu W$, and provides a variable $G_m$ from $29nA/V$ to $54nA/V$ when $i_{B2}$ varies from $100nA$ to $1\mu A$, with $iB1$, $i_{B3}$ and $iB4$ set to $250nA$, $250nA$ and $500nA$, respectively, as shown in Figure 3.16a. Figure 3.16 shows the tunable transconductance, when $i_{B2}$ and $i_{B4}$ change from $100nA$ to $500nA$, simultaneously, with $iB1$ and $i_{B3}$ set to $250nA$. It is shown that the transconductance it is more sensitive to $i_{B4}$, i.e., the NMOS side transconductance is more sensitive to the bias current.

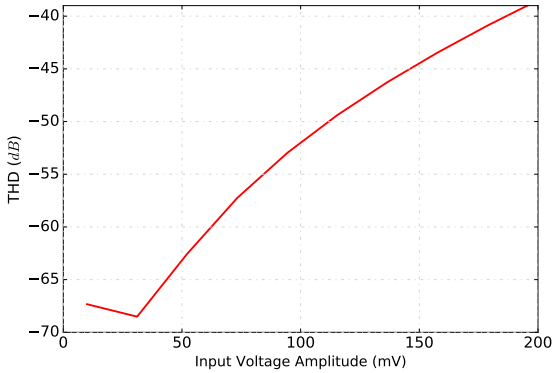



(a) (b)

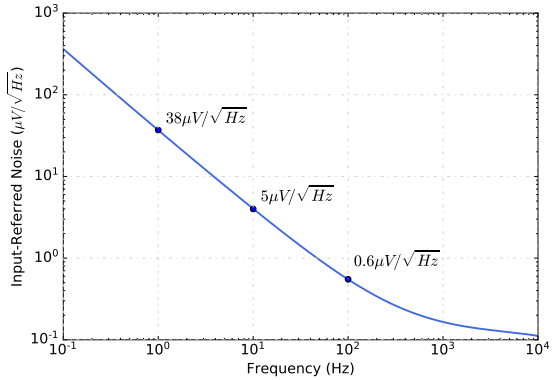
Figure 3.16: Transconductance a) as a function of the bias current $i_{B4}$ and b) as a function of $i_{B2}$ at different $i_{B4}$ values , for the LGmOTA-2a.

Figure 3.17a shows the total harmonic distortion for a sine differential input voltage at $1kHz$ with amplitude varying from $10mV$ to $200mV$. The THD remains below $-40dB$ for input voltages up to $380mVpp$.

The input-referred noise power spectral density of the LGmOTA-2a is shown in Figure 3.17b. The topology shows an integrated noise of $V_{n,rms} = 128\mu V_{rms}$ in a range frequency from $0.1Hz$ to bandwidth. The power spectral density at $10Hz$ is $5\mu V/\sqrt{Hz}$. Finally, simulations results are summarized in Table 3.6.




(a)




(b)

Figure 3.17: a) THD for different input voltage amplitudes and b) Input-Referred Noise of the LGmOTA-2a .

Table 3.6: Characteristics of the Low-Gm OTA-2a.

| Parameters | LGmOTA-2a |
|---|---|
| Process | 0.18 $\mu m$ |
| Supply | 1.8 $V$ |
| Gm | 29 - 54 $nS$ |
| Bandwidth | 390 $kHz$ |
| Power | 5.2 $\mu W$ |
| THD @ Input Voltage | 1% @ 380 $mVpp$ |
| Power Spectral Density | 0.6 $\mu V/\sqrt{Hz}$ @ 100$Hz$ |
| Input-Referred Noise | 128 $\mu V_{rms}$ (0.1$Hz$-$BW$) |

### 3.2.5 Low-Gm OTA 2b (LGmOTA-2b)

The proposed LGmOTA-2b is shown in Figure 3.18. It is very similar to the LGmOTA-2a, but in this case the value of resistor $R$ is zero, and the low transconductance is achieved by current division (through the input transistor $M_1$ to $M_8$) and current cancellation at the output.

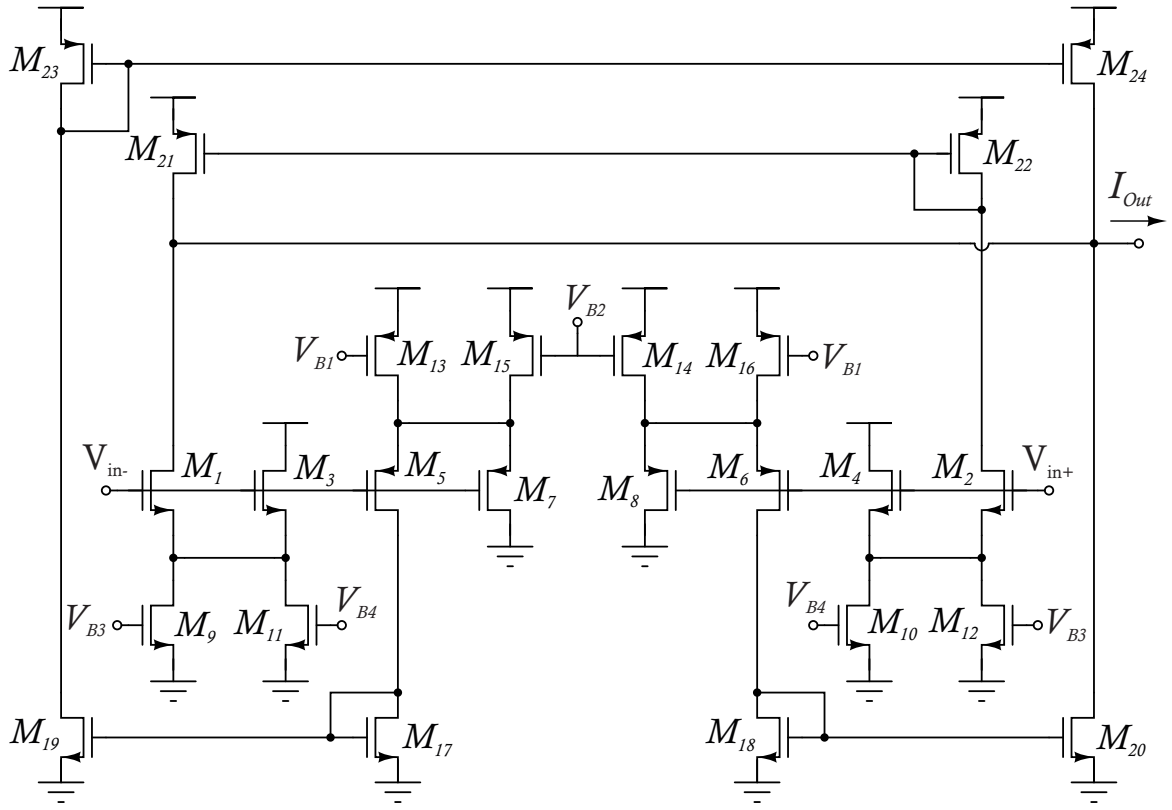



Figure 3.18: Schematic circuit of the proposed LGmOTA-2b.

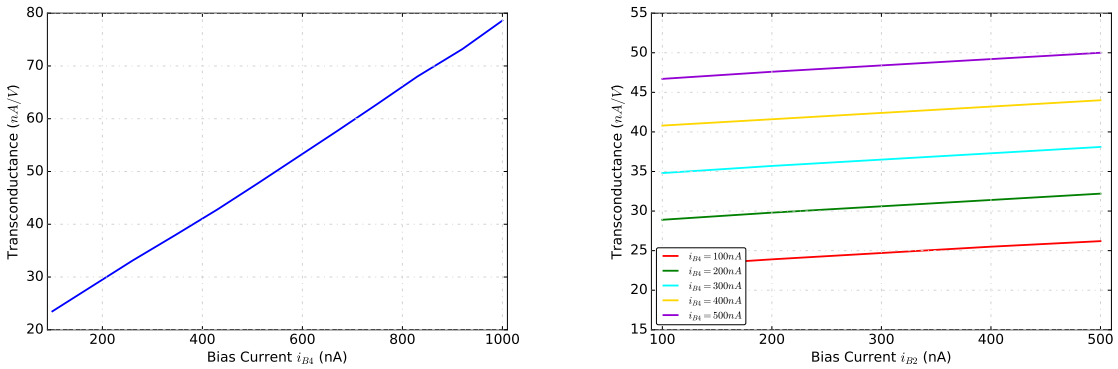
#### 3.2.5.1 Simulation Results

The LGmOTA-2b was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage and consumes $5.2\mu W$ with the bias currents set to $i_{B1} = 250nA$, $i_{B3} = 150nA$ and $i_{B2} = 150nA$, and $i_{B4} = 250nA$. Table 3.7 shows the dimensions of the transistors.

Table 3.7: Transistor Size of Low-Gm OTA 2b

| Transistors | $M_{1,2,3,4}$ | $M_{5,6,7,8}$ | $M_{9,10,11,12}$ | $M_{13,14,15,16}$ | $M_{17,18,19,20}$ | $M_{21,22,23,24}$ |
|---|---|---|---|---|---|---|
| W/L ($\mu m/\mu m$) | 36/3.6 | 72/3.6 | 72/3.6 | 36/3.6 | 72/3.6 | 36/3.6 |

The LGmOTA-2b exhibits a variable $G_m$ from $23nA/V$ to $79nA/V$, when the bias currents $i_{B4}$ varies from $100nA$ to $1\mu A$, as shown in Figure 3.19a. Figure 3.19b shows the variation of the transconductance, when $i_{B2}$ changes from $100nA$ to $500nA$, at different $i_{B4}$ values ($100nA$ to $500nA$).

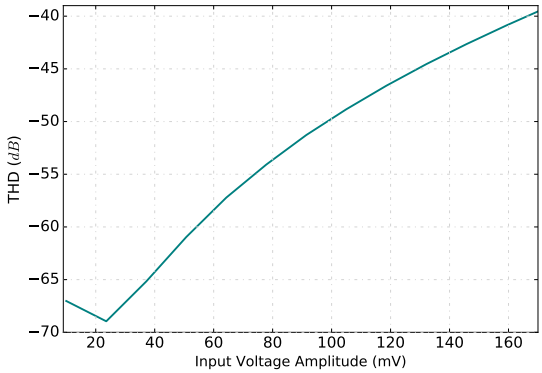



(a) (b)

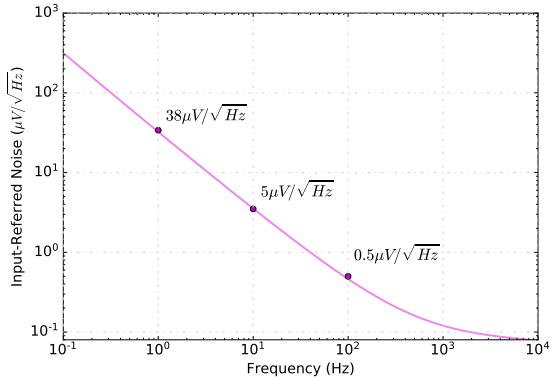
Figure 3.19: Transconductance a) as a function of the $i_{B4}$ and b) as a function of $i_{B2}$ at different $i_{B4}$ values, for the LGmOTA-2b.

Figure 3.20a shows the total harmonic distortion for a sine differential input voltage with amplitude varying from $10mV$ to $200mV$. The response shows that the THD remains below $-40dB$ for input voltages up to $340mVpp$.

The input-referred noise is shown in Figure 3.20b. At $10Hz$ the power spectral density is $5\mu V/\sqrt{Hz}$, while in $100Hz$ is $0.5\mu V/\sqrt{Hz}$. When integrated from $0.1Hz$ to bandwidth the input-referred noise is $125\mu V_{rms}$. Finally, simulations results are summarized in Table 3.8.




(a)




(b)

Figure 3.20: a) THD for different input voltage amplitudes and b) Input-Referred Noise of the LGmOTA-2b .

Table 3.8: Characteristics of the Low-Gm OTA-2b.

| Parameters | LGmOTA-2b |
|---|---|
| Process | 0.18 $\mu m$ |
| Supply | 1.8 $V$ |
| Gm | 24 - 79 $nS$ |
| Bandwidth | 390 $kHz$ |
| Power | 5.2 $\mu W$ |
| THD @ Input Voltage | 1% @ 340 $mVpp$ |
| Power Spectral Density | 0.5 $\mu V/\sqrt{Hz}$ @ 100$Hz$ |
| Input-Referred Noise | 125 $\mu V_{rms}$ (0.1$Hz$-$BW$) |

### 3.2.6 Comparison

Table 3.9 shows the main characteristics of all proposed LGmOTA. The LGmOTA-0 shows the lowest transconductance at a cost of an increased power consumption. Besides, due to the use a pseudo-resistor as degeneration element, its THD is high compared to the other proposals. The LGmOTA-1 presents low transconductance with the lowest power consumption. However, as the design was focused on the validation of the proposed bootstrapping technique to reduce Gm, and no special considerations were taken in terms of noise contribution, it also shows the highest input-referred noise. The LGmOTA-2a and LGmOTA-2b show similar results, with low power consumption, high linearity and the lowest input-referred noise.

Table 3.9: Performance Comparison of Proposed Low-$G_m$ Transconductors

| Parameters | LGmOTA-0* | LGmOTA-1 | LGmOTA-2a* | LGmOTA-2b* |
|---|---|---|---|---|
| Process ($\mu m$) | 0.18 | 0.18 | 0.18 | 0.18 |
| Supply ($V$) | 1.8 | 1.8 | 1.8 | 1.8 |
| Technique | source degeneration | bootstrapping | bootstrapping & current cancellation | division & current cancellation |
| Gm ($nA/V$) | 3.25 - 25 | 15 - 18.5 | 29 - 54 | 24 - 79 |
| Bandwidth ($kHz$) | 560 | 15 | 390 | 390 |
| Power ($\mu W$) | 9 | 4 | 5.2 | 5.2 |
| THD @ Input Voltage | 1 @ 100 mVpp | 1 @ 340 mVpp | 1 @ 380 mVpp | 1 @ 340 mVpp |
| PSD ($\mu V/\sqrt{Hz}$) @ 100 Hz | 9 | 70.3* | 0.6 | 0.5 |
| Input-Referred Noise** ($\mu V_{rms}$) | 150 | 997.5* | 128 | 125 |

*Simulation Results, **Integrating in the bandwidth.

## 3.3 Proposed Gm-C Low-Pass Filters

In this section the design, simulation and experimental measurements of different low-pass filters based on the above proposed low-Gm transconductors are presented. The proposed LPFs are: fully differential, first-order configurations, with cut-off frequencies in the order of units of $kHz$, with low power consumption in the order of tens of $\mu W$ and moderate area including the capacitor.

### 3.3.1 Low-Pass Filter (LPF-0)

The block diagram of the fully differential LPF-0 is shown in Figure 3.21.It consists of a low-Gm transconductor with resistive and capacitive load. Its transfer function is given by:

$$H(s) = \frac{G_m \cdot R_L}{(1 + sC_L R_L)} \tag{3.3.1}$$

where $R_L$ is the load resistor and $C_L$ is the load capacitor.

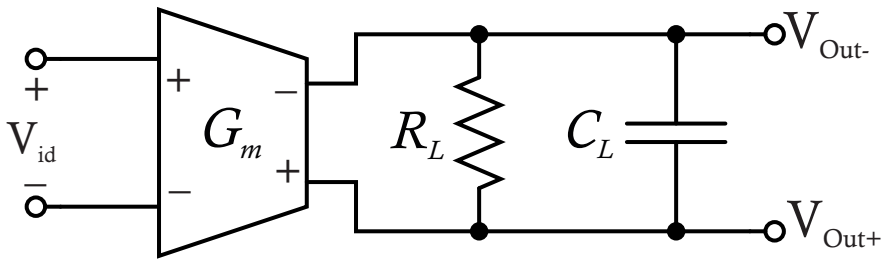



Figure 3.21: Gm-C implementation of the Low-pass Filter 0.

Figure 3.22a shows the circuit implementation of the proposed LPF-0, which is based on the LGmOTA-0 (FVF based source degenerated transconductor), with $G_m = 1/PR1$. The output current is therefore determined by the differential input voltage and the degeneration resistor $PR_1$, and is copied to the output branches through $M_7$ and $M_8$, and converted back into a differential output voltage by means of the load pseudo-resistor $R_L = PR_2$.

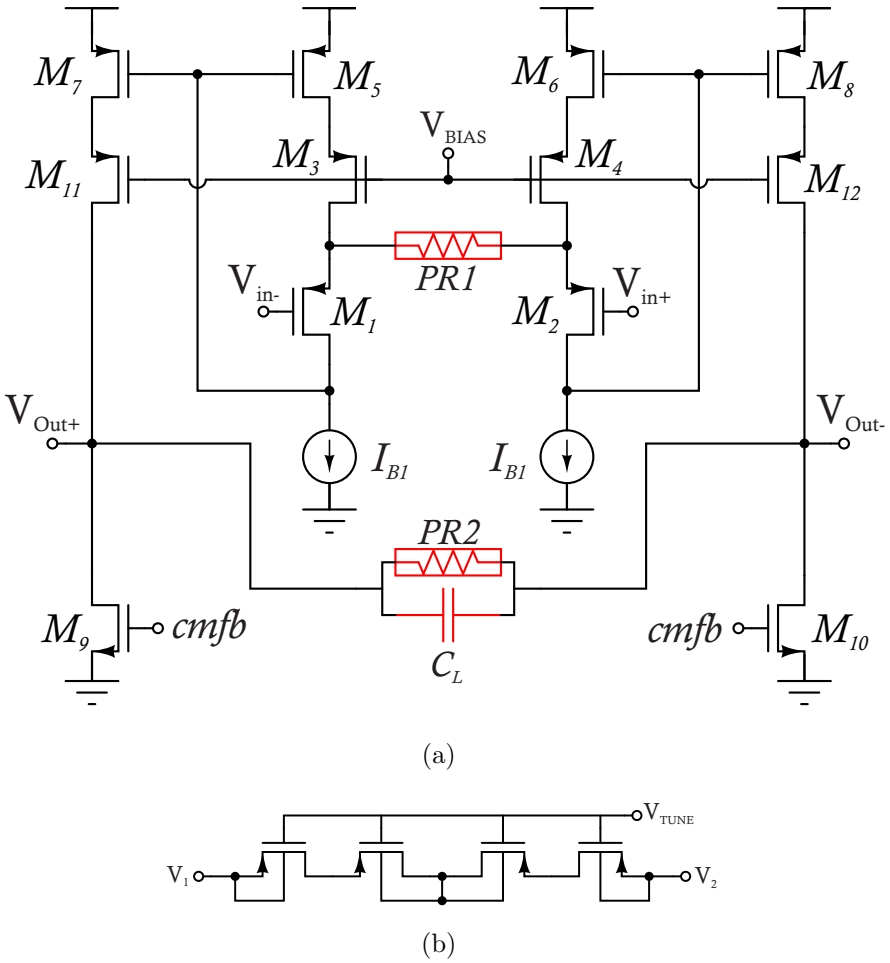



Figure 3.22: a) Proposed LPF-0 and b) pseudo-resistor.

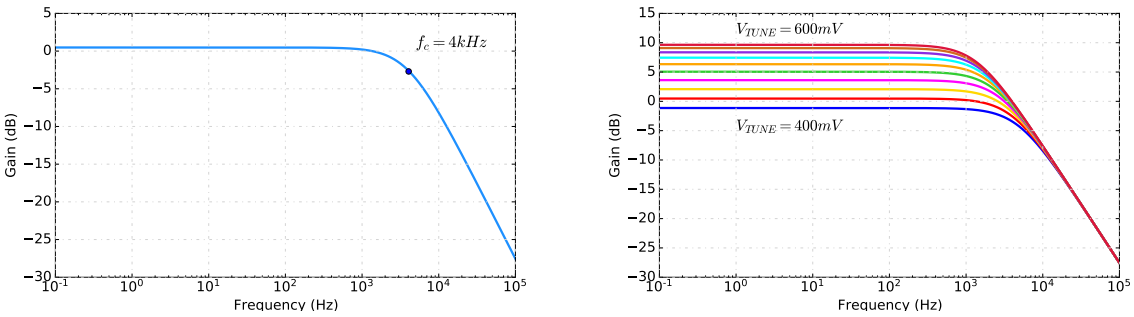
The pseudo-resistors are implemented with four PMOS transistors connected in series, as shown in Figure 3.22b. The pseudo-resistor exhibits a weak dependence on $V_{12}$, which results in a large resistance with moderate linearity [35].

The use of pseudo-resistors results in low cut-off frequency without increasing the required area, and allows modifying the gain and the cut-off frequency of the filter through the control voltage $V_{TUNE}$. In particular the cut-off frequency is modified through $PR_2$, whereas, the gain is adjusted through $PR_1$. Note that if $f_c$ needs to be changed while keeping constant the gain of the filter, both $PR_1$ and $PR_2$ must be simultaneously adjusted to keep their ratio constant.

The cut-off frequency was chosen $f_c = 4kHz$ to process input signals up to $400Hz$, so a capacitor $C_L = 35pF$and a pseudo-resistor $PR_2 = 4.5M\Omega$ were chosen. The $PR$ only takes $0.52\mu m^2$ active area, as each transistor is $W/L = 0.36\mu m/0.36\mu m$, whereas the capacitor, if implemented with a MIM configuration, requires $0.11mm^2$.

#### 3.3.1.1 Simulation Results

The proposed LPF-0 was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage and consumes $14\mu W$. As already mentioned, the DC gain of the filter can be programmable through the voltage $V_{TUNE}$. The frequency response for the LPF-0 is shown in Figure 3.23a. It exhibits a cut-off frequency $f_c = 4kHz$, and operates correctly in a tuning range from $400mV$ to $600mV$ at the gate of the pseudo-resistors. Under these conditions, the LPF-0 achieves a programmable gain from $-1dB$ to $10dB$ with cut-off frequencies from $1kHz$ to $4kHz$.

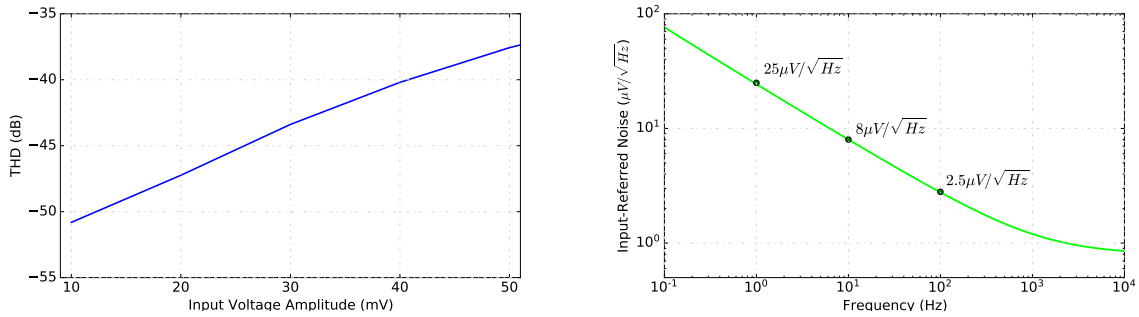



(a) (b)

Figure 3.23: a) Frequency response and b) Modifying $V_{TUNE}$ from $400mV$ to $600mV$ for the LPF-0.

Figure 3.24a shows the total harmonic distortion (THD) for a sine differential input voltage at $50Hz$ and with amplitude varying from $20mVpp$ to $100mVpp$. The THD remains below $-40dB$ for $80mVpp$ and decreases down to $-50dB$ for $20mVpp$.

Figure 3.24a shows the input-referred noise power spectral density. At $100Hz$ the input-referred noise is $2.5\mu V/\sqrt{Hz}$. Integrating from $0.1Hz$ to $1kHz$ the input referred noise is $40\mu V_{rms}$. Finally, Table 3.10 shows the main characteristics of the LPF-0.




(a) (b)

Figure 3.24: a) THD for several input voltage amplitudes and b) Input-referred noise of the LPF-0.

Table 3.10: Simulation Results for the LPF-0.

| Parameters | Simulation |
|---|---|
| Technology ($\mu m$) | 0.18 |
| Vsupply ($V$) | 1.8 |
| Power ($\mu W$) | 14 |
| Gain ($dB$) | -1 - 10 |
| fc ($kHz$) | 1 - 4 |
| Input-Referred Noise ($\mu V_{rms}$) | 40 ($0.1Hz - 1kHz$) |
| PSD ($\mu V/\sqrt{Hz}$) @100$Hz$ | 2.5 |
| THD (%) @Output mVpp | 1 @ 80 at 50$Hz$ |
| DR ($dB$) | 63 |
| NP ($\mu$) | 2.7 |
| NA | 4.6 |
| $FoM_1$ ($n$) | 1.96 |
| $FoM_2$ ($\mu$) | 183 |
| Area* ($mm^2$) | 0.15 |

*Estimated area including MIM capacitor.

### 3.3.2 Low-Pass Filter 1 (LPF-1)

The LPF-1 is based on the same configuration shown in Figure 3.21, but in this case the low-Gm transconductor is the bootstrapping-based LGmOTA-1, and the load resistor $R_L$ is implemented with the floating bootstrapped resistor proposed in Section 2.2.2, as shown in Figure 3.25 .

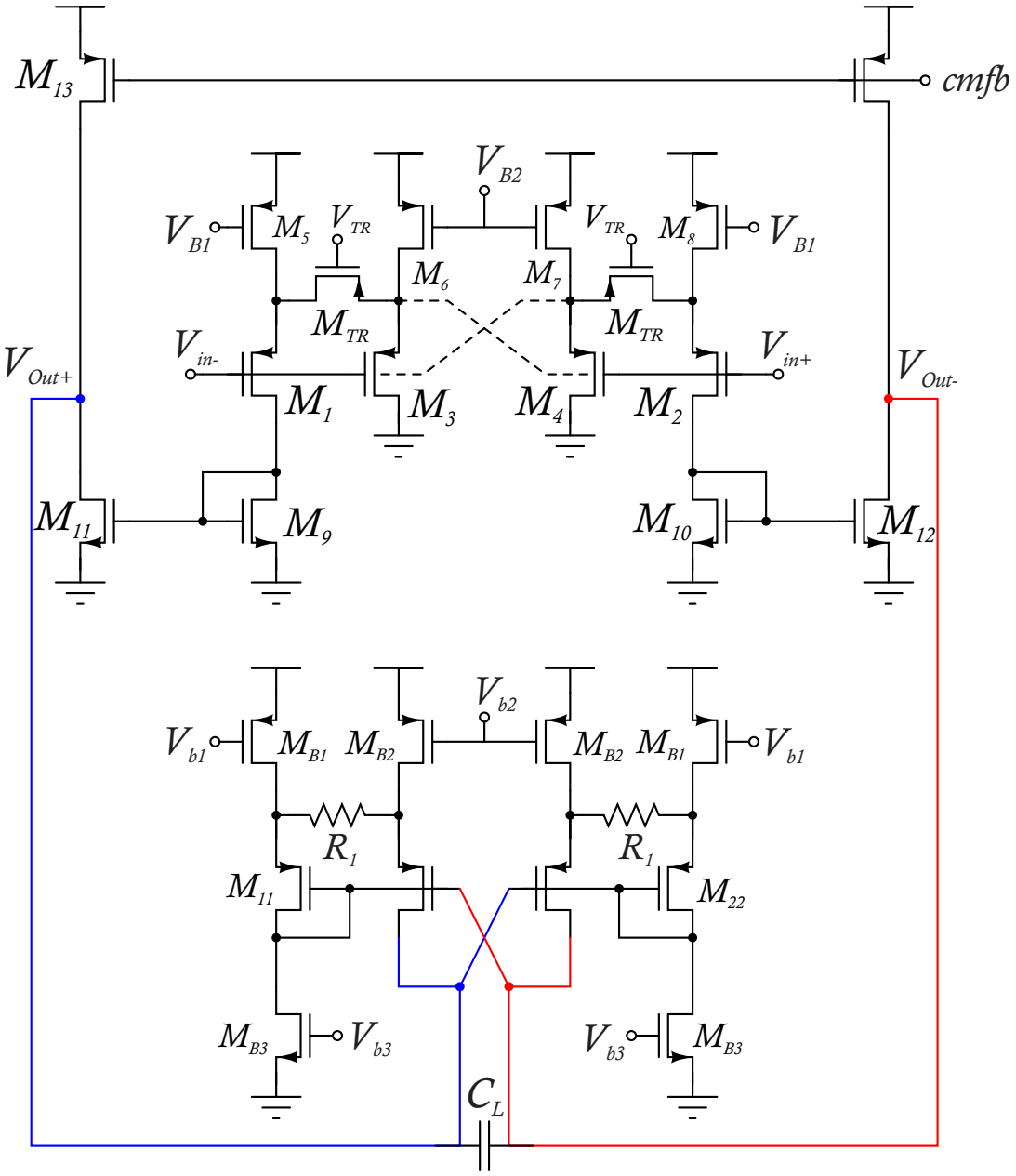



Figure 3.25: Schematic circuit of the LPF-1.

The transfer function of the LPF-1 is given by:

$$H(s) = \frac{\Delta(g_m \cdot r_B)}{g_{m1} g_{m3} r_{o5} r_{o6} R_{TR}} \cdot \frac{R_L}{1 + sC_L R_L} \tag{3.3.2}$$

where $R_{TR}$ is the equivalent resistance of the transistors ($M_{TR}$) in the triode region and $\Delta(g_m r_B)$ represents the difference between $g_{m1} r_{o5}$ and $g_{m3} r_{o6}$, while $R_L$ is the equivalent floating resistance.

#### 3.3.2.1 Simulation Results

The LPF-1 was designed in a $0.18\mu m$ CMOS standard process with $1.8V$ power supply and consumes $21.8\mu W$. The simulated frequency response is shown in Figure 3.26. The DC gain of the filter is $1dB$ with $1.5kHz$ cut-off frequency.

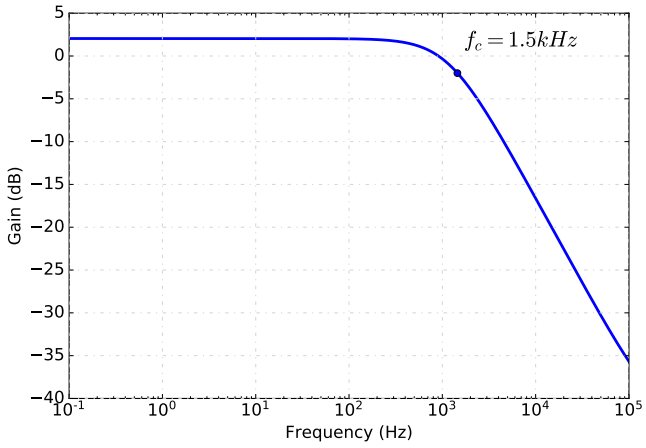
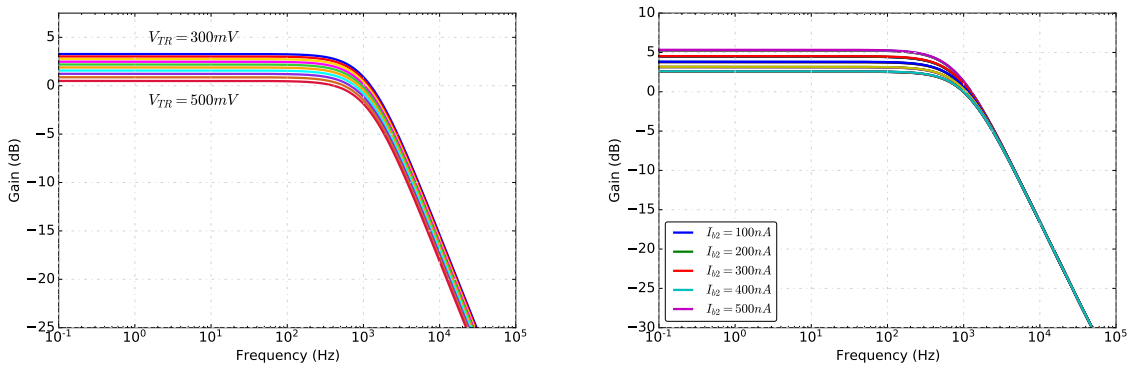



Figure 3.26: Frequency Response for LPF-1.

The gain and cut-off frequency of the configuration can be controlled either by modifying the bias voltage $V_{TR}$ of the triode transistors $M_{TR}$ in the LGmOTA-1 or by changing the output floating resistor $R_L$ through the bias current $I_{b1}$ of the bootstrapped floating resistor. Figure 3.27a shows the frequency response when $V_{TR}$ changes from $100mV$ to $500mV$. Note that under these conditions the transistors $M_{TR}$ do not leave the triode region to avoid linearity degradation. The LPF-1 shows a programmable gain from $0dB$ to $3.5dB$. Figure 3.27b presents the frequency response when $I_{b2}$ changes from $100nA$ to $500nA$. In this case, a gain variation from $1dB$ to $6dB$ is achieved, with an almost constant cut-off frequency $f_c = 1.5kHz$.




(a) (b)

Figure 3.27: Frequency response of the LPF-1: a)Modifying $V_{TR}$ and b)Modifying $R_L$ through $I_{b2}$.

Figure 3.28 shows the total harmonic distortion for a sine input voltage at $50Hz$ with amplitude varying from $1mV$ to $55mV$. The THD remains below $-40dB$ up to $100mVpp$.

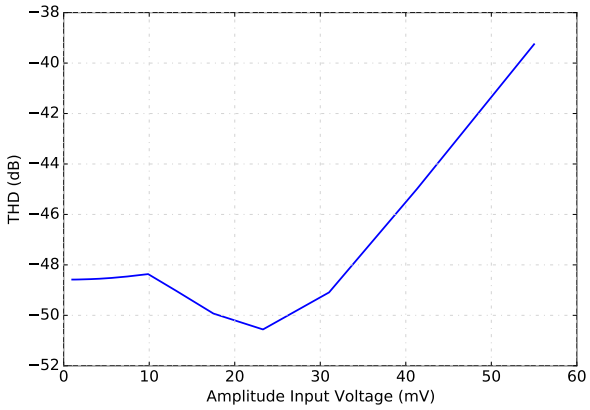



Figure 3.28: THD simulation for different input voltages amplitude.

Figure 3.29 presents the simulated input-referred noise power spectral density. The integrated noise from $0.1Hz$ to $1kHz$ is $40\mu V_{rms}$.

### 3.3.2.2 Experimental Results

The LPF-1 was fabricated in a $0.18\mu m$ CMOS process. The active area occupies $390\mu m$x$280\mu m$, as shown in Figure 3.30. The layout includes the high resistivity polysilicon degeneration resistors $R_1$ designed to be $100k\Omega$, and the load capacitor $C_L = 20pF$.

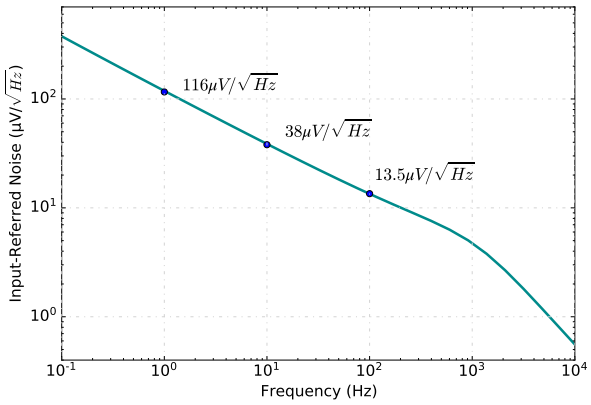



Figure 3.29: Input-referred Noise of the LPF-1.

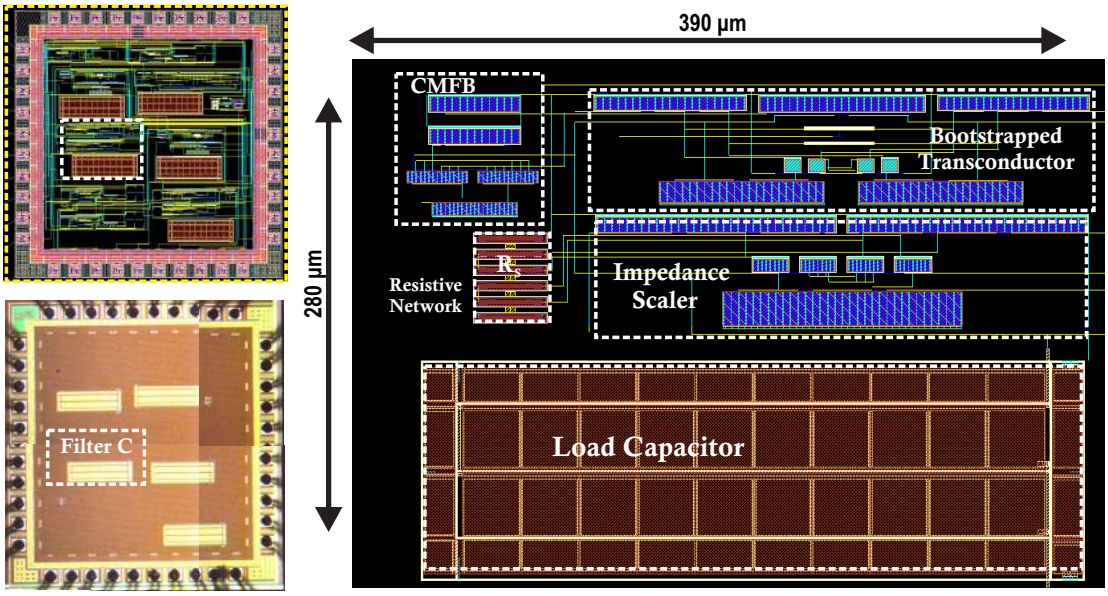



Figure 3.30: Microphotograph and layout of LPF-1.

The measured transfer function of the LPF-1 is shown in Figure 3.31. The filter gain is $0dB$, while the cut-off frequency varies from $490Hz$ to $7.1kHz$ when $I_{b1}$ changes from $350nA$ to $850nA$ in the bootstrapped resistor.

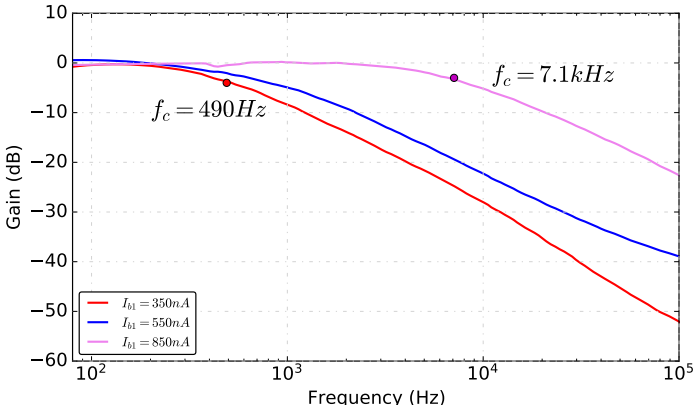
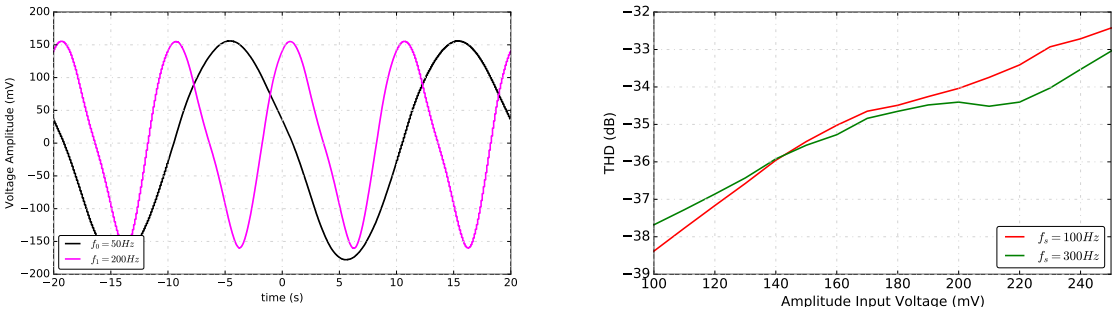



Figure 3.31: Experimental frequency response at several $I_{b1}$ values.

Figure 3.32a shows the time response for two different frequencies $f_0 = 50Hz$ and $f_1 = 200Hz$ with $300mVpp$ output voltage. Figure 3.32b shows the total harmonic distortion (THD) for a sine input differential voltage at several frequencies from $100Hz$ up to $500Hz$ and with amplitude varying from $100mVpp$ to $300mVpp$. The characterization was carried out at a cut-off frequency of $1.5kHz$ and in all cases, the THD remains below $-34dB$ for input voltages up to $200mVpp$. The THD is due to the use of the triode transistors $M_{TR}$, which degrade the linearity of the LGmOTA-1 when compared to the use of polysilicon resistors.




(a) (b)

Figure 3.32: Experimental a)Time response for $f_c = 1.5kHz$ and b)THD of the LPF-1.

Figure 3.33 shows the experimental input-referred noise PSD of the LPF-1, which is $16\mu V/\sqrt{Hz}$ at $100Hz$, and decreases down to $4.9\mu V/\sqrt{Hz}$ at $1kHz$. Integrating from $100Hz$ to $1kHz$ the input-referred noise voltage is $42\mu V_{rms}$. Finally both the simulation and experimental results of the LPF-1 circuit are summarized in Table 3.11.

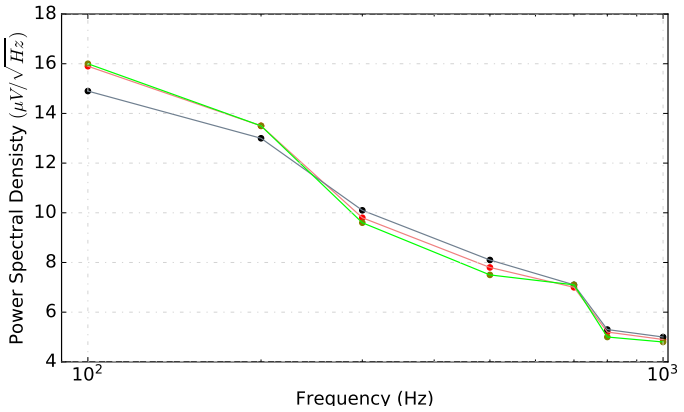



Figure 3.33: Experimental input-referred noise PSD of the LPF-1.

Table 3.11: Simulation and Experimental Results for the LPF-1.

| Parameters | Simulation | Experimental |
|---|---|---|
| Technology ($\mu m$) | 0.18 | 0.18 |
| Vsupply ($V$) | 1.8 | 1.8 |
| Power ($\mu W$) | 21.8 | 23.4 |
| Gain ($dB$) | 0 - 3 | 0 |
| fc ($kHz$) | 1.5 | 0.49 - 7.2 |
| Input-Referred Noise ($\mu V_{rms}$) | 40 (0.1Hz-1kHz) | 42 (100Hz-1kHz) |
| PSD ($\mu V/\sqrt{Hz}$) @$100Hz$ | 12.6 | 16 |
| THD (%) @Output mVpp | 1 400 @50 Hz | 1.1 200 @100 Hz |
| DR ($dB$) | 71 | 64.5 |
| NP ($\mu$) | 4.32 | 4.64 |
| NA | 3.3 | 3.3 |
| $FoM_1$ ($n$) | 1.22 | 2.75 |
| $FoM_2$ ($\mu$) | 31.1 | 22.9 |
| Area ($mm^2$) | 0.109 | 0.109 |

### 3.3.3 Low-Pass Filter 2a (LPF-2a)

The next low-pass filters are based on the fully differential first-order configuration shown in Figure 3.34. The transfer function of the filter is given by:

$$H(s) = \frac{G_{m1}}{G_{m2} + sC_L} \tag{3.3.3}$$

where $G_{m1}$ is the transconductance of the first OTA, and $G_{m2}$ the transconductance of the OTA in feedback loop, that emulates a load resistor. The cut-off frequency of the $G_m - C$ filter can be tuned by changing the $G_{m2}$ transconductance, whereas the gain can be adjusted by varying either $G_{m1}$ or $G_{m2}$. Note that if $G_{m2}$ changes, both gain and $f_c$ change.

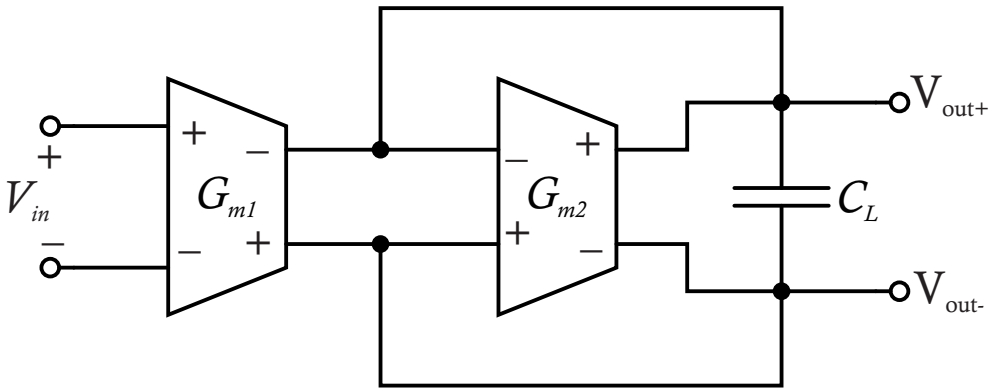



Figure 3.34: Block Diagram of the Low-pass Filter 2a.

The LPF-2a in particular consists of two LGmOTA-2a configurations and the load capacitor $C_L$. Both OTAs are designed with the same nominal transconductance $G_m = 30nA/V$, whereas $C_L = 20pF$.

Because the transconductance range of the transconductor is quite wide, the resultant filter also has a wide cut-off frequency range under suitable working conditions. In this case, the tunable cut-off frequency and gain can be controlled using $I_{b3}$ and $I_{b1}$, respectively.

#### 3.3.3.1 Simulation Results

The proposed LPF-2a was designed and simulated in a $0.18\mu m$ CMOS standard process with $1.8V$ power supply and consumes $2.9\mu W$. Figure 3.35 shows the AC response. The DC gain of the LPF-2a is $-1dB$ and its cut-off frequency is $1.5kHz$.

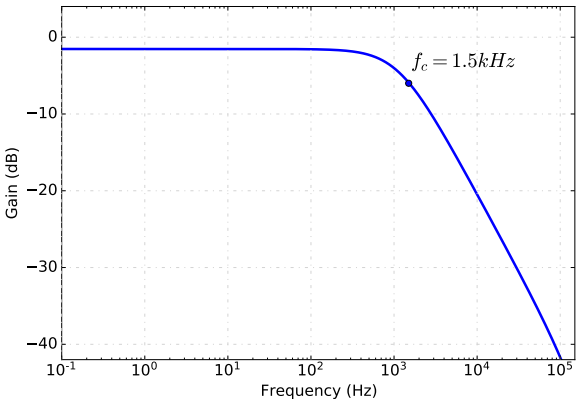
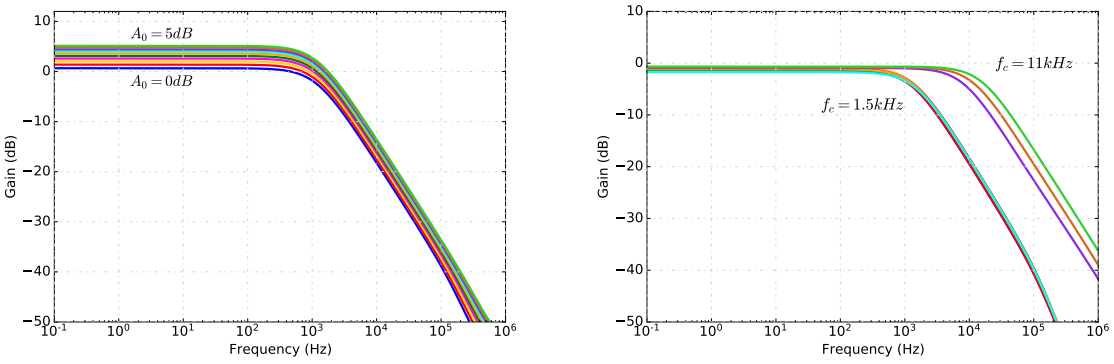



Figure 3.35: Frequency Response of LPF-2a.

Figure 3.36a shows the gain programmability from $0dB$ to $5dB$ when $I_{b3}$, which controls $G_{m1}$, changes from $100nA$ to $250nA$. Figure 3.36b presents the cut-off frequency when $I_{b1}$, which controls $G_{m2}$, varies from $100nA$ to $1\mu A$. Under these conditions, $f_c$ changes from $1.5kHz$ to $11kHz$.




(a) (b)

Figure 3.36: Frequency response of the LPF-2a when a)modifying $G_{m1}$ through $I_{B3}$ and b) modifying $G_{m2}$ through $I_{B1}$.

As shown in Figure 3.37, the total harmonic distortion remains below $-40dB$ up to $180mVpp$ input at $50Hz$.

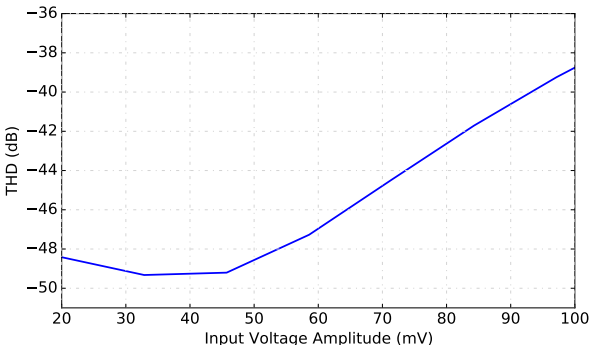



Figure 3.37: THD for different input voltages amplitudes of the LPF-2a.

Figure 3.38 shows the input-referred-noise power spectral density of the proposed LPF-2a. The input-referred noise is $10\mu V/\sqrt{Hz}$ at $100Hz$ and decreases down to $3.5\mu V/\sqrt{Hz}$ at $1kHz$. Integrating from $0.1Hz$ to $1.5kHz$ the input-referred noise voltage is $17.6\mu V_{rms}$.

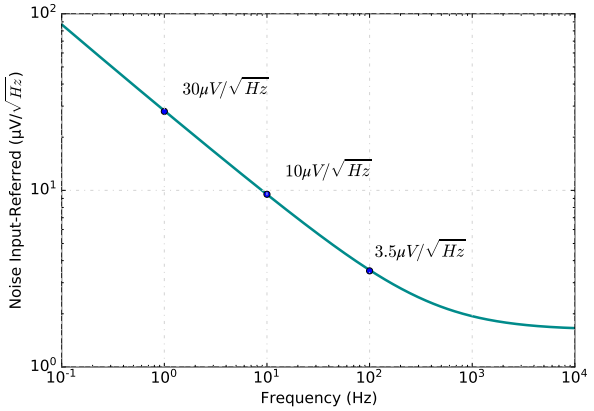



Figure 3.38: Input-Referred Noise of LPF-2a.

### 3.3.3.2 Experimental Characterization

The LPF-2a was fabricated in a $0.18\mu m$ standard CMOS process with $1.8V$ power supply. Figure 3.39 shows the microphotograph and layout of the fabricated chip, which includes the high resistivity polysilicon degeneration resistors $R$, designed to be $100k\Omega$ each, and the load capacitor. The silicon active area including two transconductors and the load capacitor is $470\mu m$x$300\mu m$.

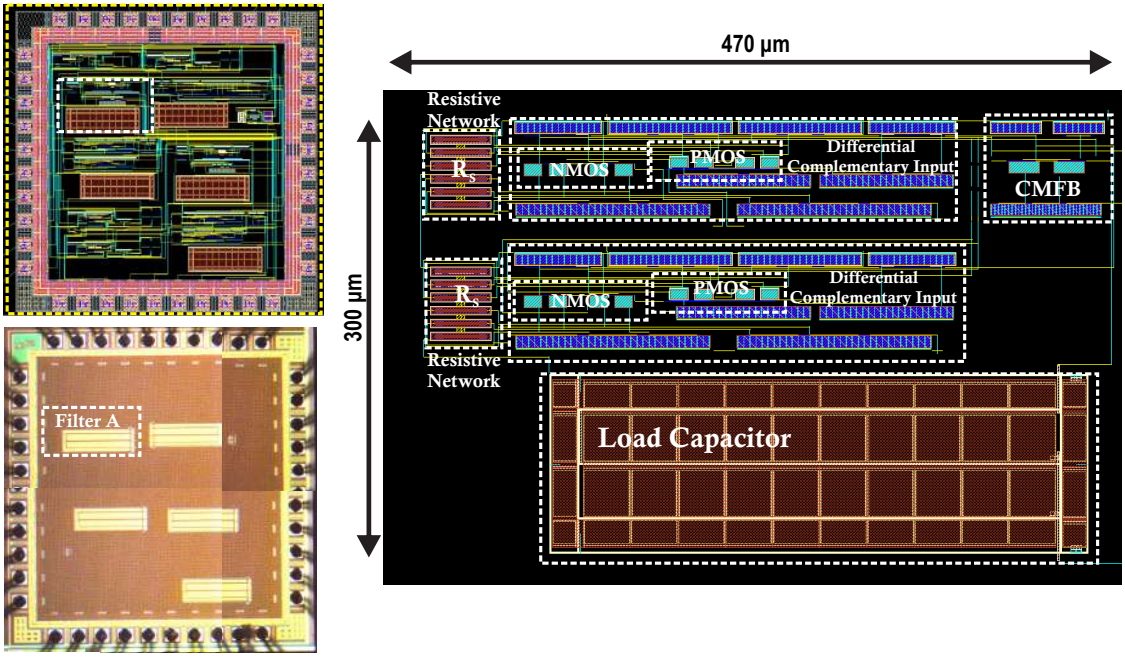



Figure 3.39: Microphotograph and layout of proposal LPF-2a.

The experimental frequency response of the LPF-2a is shown in Figure 3.40. The cut-off frequency varies from $2kHz$ (with $I_{b1} = 250nA$ and $I_{b3} = 520nA$) to $18kHz$ (with $I_{b1} = 1.2\mu A$ and $I_{b3} = 1.6\mu A$). The DC gain is about $-1dB$.

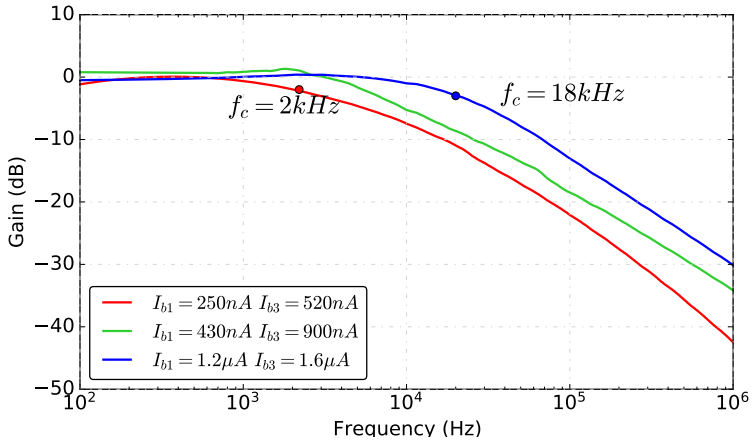
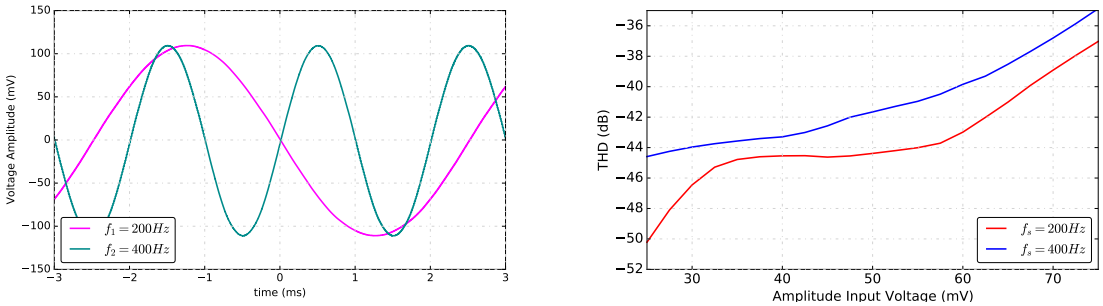



Figure 3.40: Experimental frequency response of the LPF-2a.

Figure 3.41a shows the time response. The graph shows the output signal at different frequencies with $I_{b1} = 250nA$ and $I_{b3} = 520nA$ and $f_c = 2kHz$. Figure 3.41b shows the total harmonic distortion for a differential sine input voltage at frequencies $200Hz$ and $400Hz$ with amplitude varying from $40mVpp$ to $150mVpp$. The characterization was carried out at a cut-off frequency of $2kHz$. In all cases, the THD remains below $-40dB$ for input voltages up to $120mVpp$.




(a) (b)

Figure 3.41: a) Time Response for several frequencies and b) THD measurements for LPF-2a.

The input-referred noise density is shown in Figure 3.42. The PSD of the input-referred noise is $5.2\mu V/\sqrt{Hz}$ at $100Hz$, and decreases down to $2.3\mu V/\sqrt{Hz}$ at $1kHz$. Integrating the passband noise from $100Hz$ to $1kHz$ results in an input-referred noise voltage $V_{rms} = 27.7\mu V_{rms}$. The simulation and experimental results are summarized in Table 3.12.

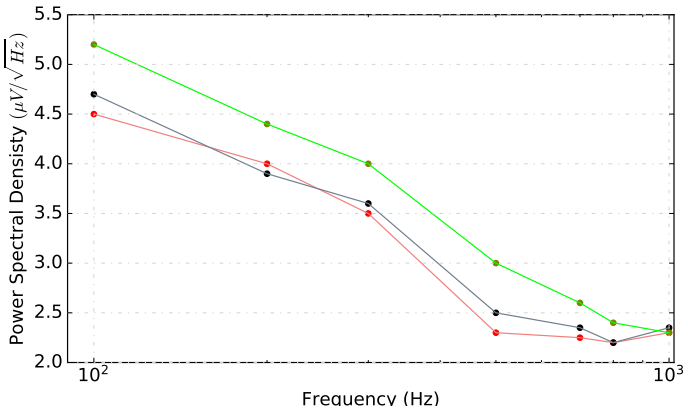



Figure 3.42: Input-Referred Noise PSD of the LPF-2a.

Table 3.12: Simulation and Experimental Results for the LPF-2a.

| Parameters | Simulation | Experimental |
|---|---|---|
| Technology ($\mu m$) | 0.18 | 0.18 |
| Vsupply ($V$) | 1.8 | 1.8 |
| Power ($\mu W$) | 2.6 | 5.3 |
| Gain ($dB$) | 0 - 5 | -1 |
| fc ($kHz$) | 1.5 - 11 | 2 - 18 |
| Input-Referred Noise ($\mu V_{rms}$) | 17.7 (0.1Hz - 1kHz) | 27.7 (100Hz - 1 kHz) |
| PSD ($\mu V/\sqrt{HZ}$) @ 100 Hz | 3.5 | 5.1 |
| THD (%) @ Output ($mVpp$) | 1 200 @ 50 Hz | 1 150 @ 200 Hz |
| DR ($dB$) | 72 | 68 |
| NP ($\mu$) | 0.515 | 1.05 |
| NA | 4.35 | 4.35 |
| $FoM_1$ ($n$) | 0.09 | 0.32 |
| $FoM_2$ ($\mu$) | 18.8 | 14.4 |
| Area ($mm^2$) | 0.141 | 0.141 |

### 3.3.4 Low-Pass Filter 2b (LPF-2b)

The LPF-2b is based on the same fully differential configuration (Figure 3.34), but in this case, the OTAs are the LGmOTA-2b presented in Section 3.2.4. Again, both the gain and the cut-off frequency can be adjusted through the bias currents $I_{b1}$-$I_{b4}$.

#### 3.3.4.1 Simulation Results

The LPF-2b was designed in a $0.18\mu m$ CMOS standard process. The simulated transfer function is presented in Figure 3.43. The DC gain is $0dB$ with a cut-off frequency of $1.9kHz$.

In the same way as the LPF-2a, the gain and cut-off frequency can be tuned through the transconductances $G_{m1}$ and $G_{m2}$. Figure 3.36a shows how the gain varies from $0dB$ to $6.5dB$ when $I_{b3}$ changes from $100nA$ to $250nA$, i.e., when the transconductance $G_{m1}$ is changed. Figure 3.36b shows the variation of the cut-off frequency when $I_{b3}$ varies from $100nA$ to $2.5\mu A$. Under these conditions, $f_c$ changes from $2kHz$ up to $45kHz$.

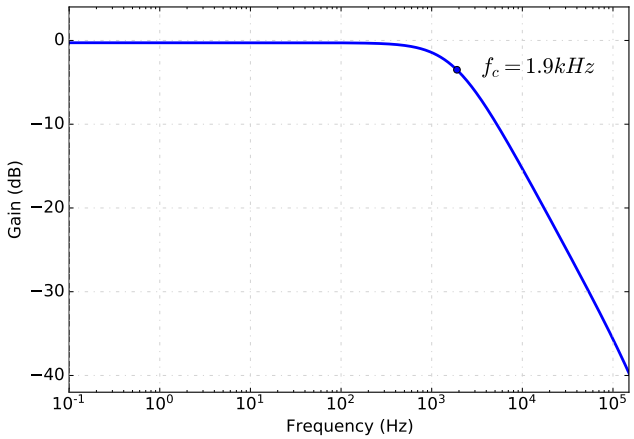
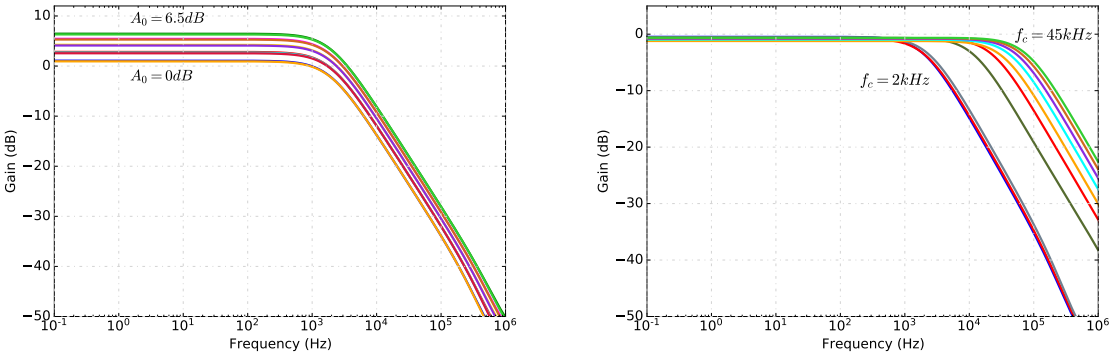



Figure 3.43: Simulated transfer function for LPF-2b.

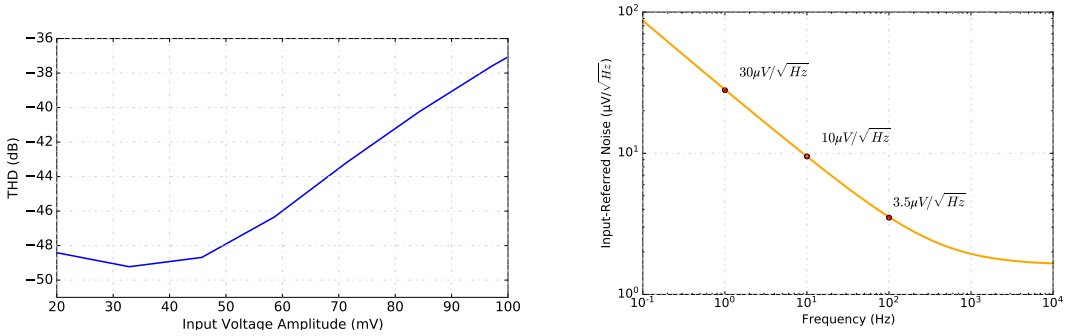



(a) (b)

Figure 3.44: Frequency response a)Modifying the gain by $G_{m1}$ and b)Modifying $f_c$ through $G_{m2}$ of the LPF-2b.

Figure 3.45a shows the total harmonic distortion as a function of the input voltage for $0dB$ gain. The THD is $-49dB$ for a $60mVpp$ sine input voltage and increases up to $-40dB$ for $170mVpp$.

Figure 3.45b shows the simulated input-referred-noise power spectral density of the proposed LPF-2b, which is $10\mu V/\sqrt{Hz}$ at $100Hz$ and decreases down to $3.5\mu V/\sqrt{Hz}$ at $1kHz$. Integrating from $0.1Hz$ to $1.9kHz$ the input-referred noise voltage is $17.9\mu V_{rms}$.




(a) (b)

Figure 3.45: a)THD for different input voltages amplitudes and b)Input-referred noise PSD of the LPF-2b.

### 3.3.4.2 Experimental Results

The proposed LPF-2b was fabricated in a $0.18\mu m$ standard CMOS process and operates with $1.8V$ supply voltage. Figure 3.46 shows the microphotograph and layout of the fabricated chip. The silicon active area for LPF-2b (shown inside the rectangular frame) is $600\mu m$x$240\mu m$.

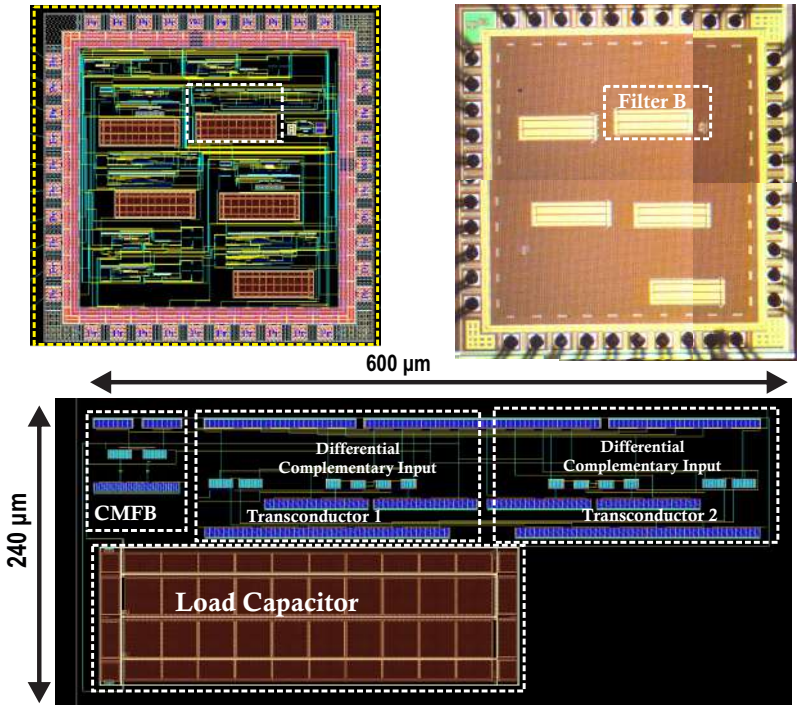



Figure 3.46: Microphotograph and layout of proposal LPF-2b

The circuit was biased with $I_{b1} = 250nA$, $I_{b2} = 500nA$ and $I_{b3} = 520nA$, $I_{b4} = 690nA$. The frequency response is shown in Figure 3.47. It can be noted that the cut-off frequency varies from $1.6kHz$ to $15kHz$. The DC gain is around $0dB$.

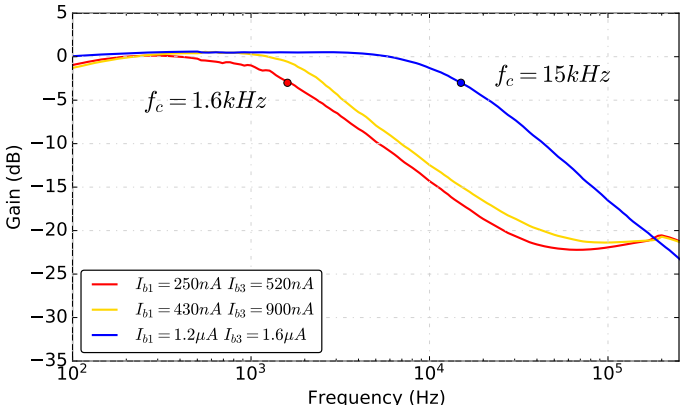
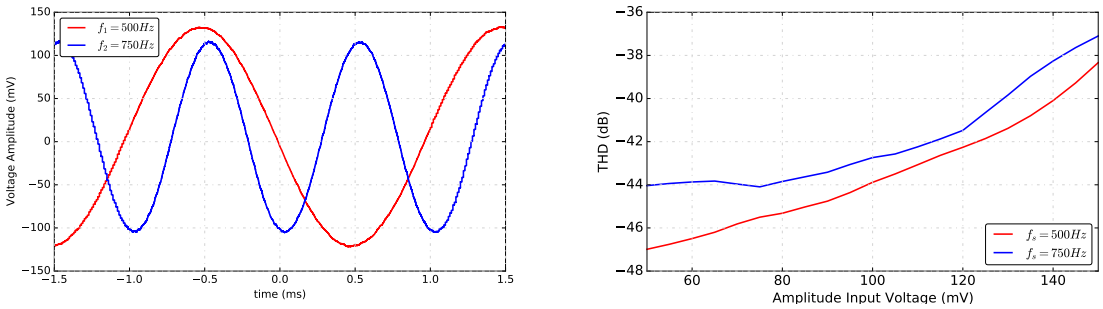



Figure 3.47: Measured frequency responses over the tuning range.

Figure 3.48a presents the time response for two different signal frequencies $f_s = 500Hz$ and $f_s = 750Hz$. Figure 3.48 shows the THD for a sine differential input voltage at the same frequencies and with amplitude varying from $50mV$ to $150mV$. The characterization was carried out at a cut-off frequency of $1.6kHz$, and in all cases the THD remains below $-40dB$ for input voltages up to $250mVpp$.




(a) (b)

Figure 3.48: Experimental a) Time response and b) THD for different amplitude input voltages for the LPF-2b.

The input-referred noise density is shown in Figure 3.49. The power spectral density of the input-referred noise is $4\mu V/\sqrt{Hz}$ at $100Hz$, and decreases down to $1.95\mu V/\sqrt{Hz}$ at $1kHz$. Integrating the input-referred noise from $100Hz$ to $1kHz$ gives an input-referred

noise voltage $V_{rms} = 24\mu V_{rms}$. Simulation and experimental results of the LPF-2b circuit are summarized in Table 3.13.

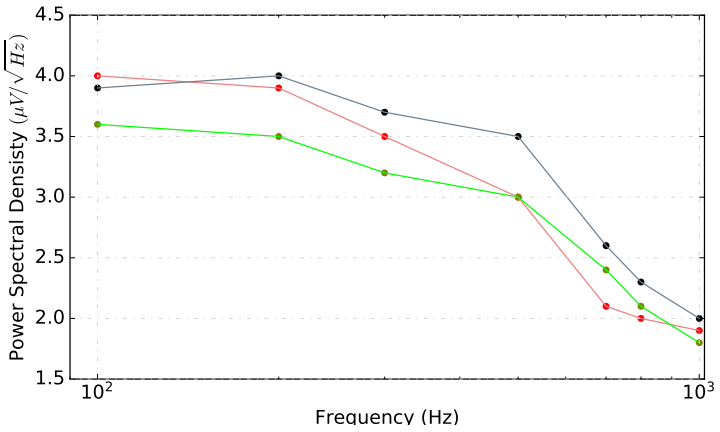



Figure 3.49: Input-Referred Noise of LPF-2b.

Table 3.13: Simulation and Experimental Results for the LPF-2b.

| Parameters | Simulation | Experimental |
|---|---|---|
| Technology ($\mu m$) | 0.18 | 0.18 |
| Vsupply ($V$) | 1.8 | 1.8 |
| Power ($\mu W$) | 2.7 | 5.4 |
| Gain ($dB$) | 0 - 6 | 0 |
| fc ($kHz$) | 1.9 - 45 | 1.6 - 15 |
| Input-Referred Noise ($\mu V_{rms}$) | 17.9 (0.1Hz-1kHz) | 24 (100Hz-1kHz) |
| PSD ($\mu V/\sqrt{Hz}$) @ 100 Hz | 2.7 | 4 |
| THD (%) @Output mVpp | 1<br>170 @50 Hz | 1<br>140 @500Hz |
| DR ($dB$) | 73 | 69.4 |
| NP ($\mu$) | 0.535 | 1 |
| NA | 4.4 | 4.4 |
| $FoM_1$ ($n$) | 0.08 | 0.29 |
| $FoM_2$ ($\mu$) | 3 | 10.4 |
| Area ($mm^2$) | 0.144 | 0.144 |

### 3.3.5 Performance Comparison of LPF

The summary and performance comparison of the proposed Gm-C filters designed and tested are shown in Table 3.14. The LPF-0 is a very compact configuration which provides a variable gain from $-1$ to $10dB$, and cut-off frequency as low as $1kHz$. However, the linearity is degraded due to the use of pseudo-resistors. The LPF-1, based on the LGmOTA-1, provides a variable gain from 0 to $3dB$, and variable cut-off frequency from $490Hz$ to $7.1kHz$. It achieves the lowest cut-off frequency at a cost of an increased power consumption, due to the boosting resistance block used at the output. Finally, both the LPF-2a and LPF-2b show the lowest $\text{FoM}_1$, i.e., the best trade-off between power consumption and dynamic range. The LPF-2a provides a variable gain from 0 to $5dB$, and variable $f_c$ from $2kHz$ to $18kHz$. The LPF-2b provides a variable gain from 0 to $6dB$, and variable $f_c$ from $1.6kHz$ to $15kHz$, and shows the lowest $\text{FoM}_2$, i.e., the best trade-off between power consumption, bandwidth, area and dynamic range.

To better show the contribution, the main characteristics of the fabricated filters are summarized in Table 3.15 and compared with other Gm-C filters found in the literature. When compared with other topologies, the proposed LPFs do not achieve such low frequencies as some of them. The LPF-2a shows the second lowest power consumption, after [39], which also achieves lower cut-off frequencies, at a cost of a decreased gain (i.e., at a cost of attenuating the signal, which in a chopper amplifier is already low), and with lower dynamic range. In terms of dynamic range, the proposed LPFs are second best after [33]. The proposed LPFs, however, provide not only tunable cut-off frequency but also tunable gain, which can be increased as required. The nominal gain of [33], in contrast, is $0dB$ and cannot be tuned.

Table 3.14: Performance Comparison with the Proposed Gm-C Filters.

| Parameters | LPF-0 | LPF-1 | | LPF-2a | | LPF-2b | |
|---|---|---|---|---|---|---|---|
| | Simulation | Simulation | Experimental | Simulation | Experimental | Simulation | Experimental |
| Technology ($\mu m$) | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 |
| Vsupply ($V$) | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| Power ($\mu W$) | 14 | 21.8 | 23.4 | 2.6 | 5.3 | 2.7 | 5.4 |
| Gain ($dB$) | -1 - 10 | 0 - 3 | 0 | 0 - 5 | -1 | 0 - 6 | 0 |
| fc ($kHz$) | 1 - 4 | 1.5 | 0.49 - 7.1 | 1.5 - 11 | 2 - 18 | 1.9 - 45 | 1.6 - 15 |
| Input-Referred Noise* ($\mu V_{rms}$) | 40 | 40 | 42 | 17.7 | 27.7 | 17.9 | 24 |
| PSD ($\mu V/\sqrt{Hz}$) @ 100 Hz | 2.5 | 12.6 | 16 | 3.5 | 5.1 | 2.7 | 4 |
| THD (%) @ Output mVpp | 1 80 @ 50 Hz | 1 100 @ 50 Hz | 1 >100 @ 100 Hz | 1 200 @ 50 Hz | 1 150 @ 250 Hz | 1 170 @ 50 Hz | 1 140 @ 500 Hz |
| DR ($dB$) | 63 | 71 | 64.5 | 72 | 68 | 73 | 69.4 |
| NP ($\mu$) | 2.7 | 4.32 | 4.64 | 0.515 | 1.05 | 0.535 | 1 |
| NA | 4.6 | 3.3 | 3.3 | 4.35 | 4.35 | 4.4 | 4.4 |
| $\text{FoM}_1$ ($n$) | 1.96 | 1.22 | 2.75 | 0.09 | 0.32 | 0.08 | 0.29 |
| $\text{FoM}_2$ ($\mu$) | 183 | 31.1 | 22.9 | 18.8 | 14.4 | 3 | 10.4 |
| Area ($mm^2$) | 0.15 | 0.109 | 0.109 | 0.141 | 0.141 | 0.144 | 0.144 |

*Integrating from $0.1Hz$ to $1kHz$ (simulation), and integrating from $100Hz$ to $1kHz$ (experimental).

Table 3.15: Performance comparison with other Topologies Filters.

| Parameters | Sanchez [39] 2015 | Wang [36] 2015 | Sawigun [37] 2018 | Sun [38] 2018 | Perez [33] 2019 | LPF-1 | LPF-2a |
|---|---|---|---|---|---|---|---|
| Technology ($\mu m$) | 0.13 | 0.35 | 0.35 | 0.18 | 0.18 | 0.18 | 0.18 |
| Vsupply ($V$) | 1.2 | 3.3 | 0.6 | 1 | 1.8 | 1.8 | 1.8 |
| Order | 3 | 9 | 4 | 5 | 2 | 1 | 1 |
| Power ($\mu W$) | 450 | 59.5 - 90 | 9.27x$10^{-4}$ | 0.35 | 9.9 | 23.4 | 5.3 |
| Gain ($dB$) | 10 | 18.8 - 21.1 | -2.7 | -6 / -8 | $< 0.5$ | 0 | -1 |
| fc ($kHz$) | 375 - 590 | 0.03 - 8 | 0.1 - 0.27 | 0.05 | 0.00157 - 5.2 | 0.49 - 7.1 | 2 - 18 |
| Input-Referred Noise ($\mu V_{rms}$) | 342 | 93.3, 34.3[3] | 46.8 | 100 | 19.9[2] | 42 | 27.7 |
| PSD ($\mu V/\sqrt{Hz}$) @ 100 Hz | - | - | - | - | - | 16 | 5.1 |
| THD (%) @ Output mVpp | 1 450 | 1 82 - 31 | - | - | 1 345 @ 0.5 Hz | 1 >100 @ 100 Hz | 1 150 @ 250 Hz |
| DR ($dB$) | 53.35 | 49.8 - 52 | 47 | 49.9 | 75.7[1] | 64.5 | 68 |
| NP ($\mu$) | - | 3.34 - 5.05 | - | 0.29 | 1.96 | 4.64 | 1.05 |
| NA | 4.73 | 7.34 | 1.37 | 3.7 | 0.815 | 3.3 | 4.35 |
| $FoM_1$ ($n$) | - | 1.2 - 1.7 | - | 0.186 | 0.16 | 2.75 | 0.32 |
| $FoM_2$ ($\mu$) | 0.573x$10^6$ | 4870 - 1816 | 1.39x$10^{-4}$ | 0.041 | 3.44 | 22.9 | 14.4 |
| Area ($mm^2$) | 0.08 | 0.9 | 0.168 | 0.12 | 0.0264 | 0.109 | 0.141 |

[1]For $f_c = 0.5Hz$, [2]For $f_c = 5Hz$, [3]Minimum value noises reported.

## 3.4 Conclusions

This chapter presented several novel low-Gm transconductors with tuning capability and high linearity to implement low-pass filters with low cut-off frequency. The first proposal, the LGmOTA-0, is based on a FVF transconductor and relies on a pseudo-resistor to achieve low Gm without the need for large area polysilicon resistors. It achieves a transconductance ranging from $3.25nA$ to $25nA/V$, but linearity is degraded by the pseudo-resistor. The LGmOTA-1 is a novel topology which applies the bootstrapping technique to increase the equivalent resistance of polysilicon resistors, and thus achieve low Gm. It was fabricated in a $0.18\mu m$ CMOS process and experimental results show a transconductance range from $15nA/V$ to $18.5nA/V$, with good linearity, thus validating the proposed technique. Finally, the LGmOTA-2a and LGmOTA-2b are proposed, based on similar topologies. The first one relies on bootstrapping and current cancellation to achieve low Gm, whereas the second one only relies on current and division cancellation. Both show similar results, with a variable Gm from $29nA/V$ to $54nA/V$ in the first case, and $24nA$ to $79nA$ in the second case, very low input-referred noise of approximately $600nV/\sqrt{Hz}$, and good linearity.

Furthermore, three filters were designed and fabricated using the proposed core transconductors. The LPF-1 and LPF-2 were implemented using a complementary differential input combined with bootstrapping and applying current cancellation to achieve low-transconductance. Finally, a comparison between the proposed filters and recently integrated LPF found in the literature is presented. The proposed filters show high programmability of gain and cutoff frequency and, depending on the equivalent transconductance of the core OTA have a wide operating range with moderate THD and cut-off frequencies in the order of tens of $kHZ$.

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# Chapter 4

# Chopper Amplifiers

The chopping technique is a continuous time modulation technique used to reduce the offset and flicker noise, in which the low-frequency signal is translated to higher frequencies, amplified and demodulated back to baseband, whereas the flicker noise is modulated at high frequencies and then filtered out. To avoid aliasing due to the unwanted mixing of the input signals and the switching signals, the switching frequency must be appropriately selected [1-10].

Figure 4.1a shows the block diagram of the chopping technique and Figure 4.1b the spectrum of a low frequency signal. After the first chopper modulator ($CH1$), the signal is translated at higher frequencies than the flicker noise (Figure 4.1c). After amplification and the second chopper block ($CH2$), the amplified signal is demodulated back to low frequency, while the noise content is modulated once, so its frequency components are now around the odd harmonics of the chopping frequency (Figure 4.1d). Finally, the signal passes through a low-pass filter (LPF) to eliminate the noise contribution (Figure 4.1e). To completely remove the residual noise, the chopping frequency must be higher than the noise corner frequency.

The noise power spectrum of a chopper amplifier is shown in Figure 4.2 [2]. It shows a flat spectral density, with a peak at the chopping frequency due to the commutation of the switches. The superior noise performance of the continuous-time chopper technique over the sampled auto-zero technique makes it the best choice to realize low-noise sensor interfaces with low-power consumption [2].

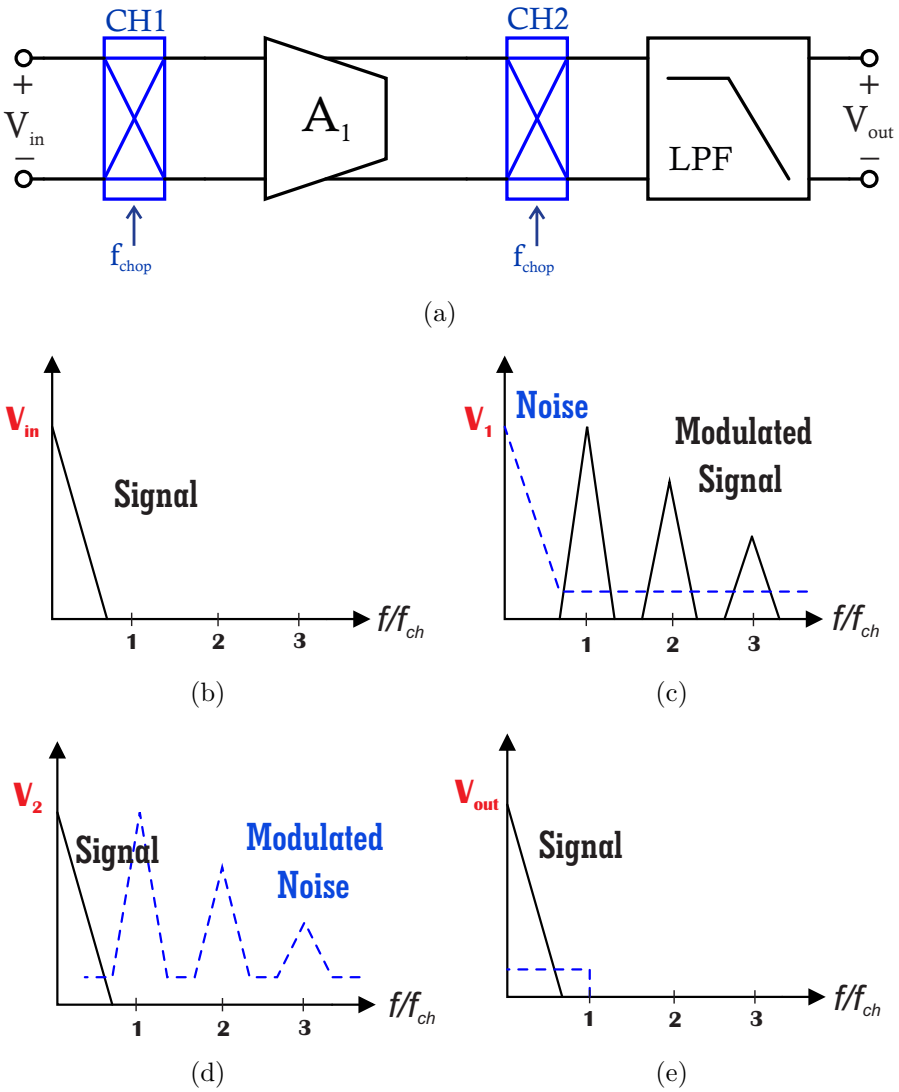



Figure 4.1: Principle of the Chopping Technique.

The chopping technique usually does not introduce extra noise, especially when the modulators are positioned at low impedance nodes. However, there is still residual offset due to the modulators commutations[7-10]. Furthermore, as already mentioned, the chopper frequency must be higher than the noise corner frequency of the amplifier, and at least 10 times the bandwidth of the amplifier to avoid residual noise contributions due to switching [7].

The proposed chopper amplifiers are designed to process input signals from $500\mu V$ to $1mV$ with frequencies from $0.1Hz$ to $100Hz$. The amplifier must have at least $40dB$ gain, to ensure that it determines the overall noise of the acquisition system with power

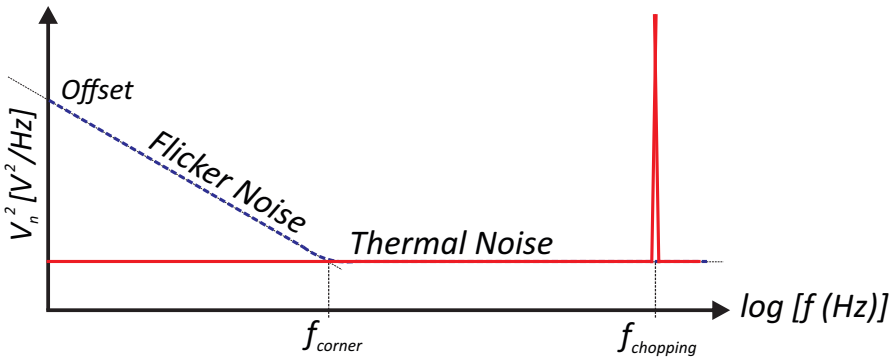



Figure 4.2: Noise power spectrum of Chopper Technique.

consumption in the order of tens of $\mu W$.

This Chapter presents the implementation of three fully differential chopping amplifiers based on the building blocks proposed in the former Chapters. First, the implementation of the modulators and their control circuitry are presented. Then, the first chopper amplifier (ChA-0) is proposed, based on the LNP-0 and the LPF-0. The chopper amplifier 1 (ChA-1), in turn, consists of the VGLNP-4 in conjunction with the LPF-1. Finally, the chopper amplifier 2 (ChA-2) is proposed also based on the VGLNP-4 but with the LPF-2a, which has lower power consumption and higher linearity than the LPF-1.

## 4.1 Modulators and Clock Signal Generation

The chopping technique involves the use of two modulation blocks controlled by a clock ($clk$) signal with complementary phases, i.e. in counter-phase. Each modulator consists of four switches, as shown in Figure 4.3a, which, in CMOS technology can be implemented with MOSFETs, as shown in Figure 4.3b.

A MOS transistor switch has a non-infinite impedance when it is off and non-zero impedance when it is on. The on resistance can be as high as $10k\Omega$ for minimum size switches, and the off resistance is typically about $10M\Omega$. A voltage drop thus occurs when current is flowing through the open switch. Additionally, there is a small delay between the signal controlling the MOSFET switch gates and the switching action. The main cause of delay is the relatively high capacitance of the clock line [1].

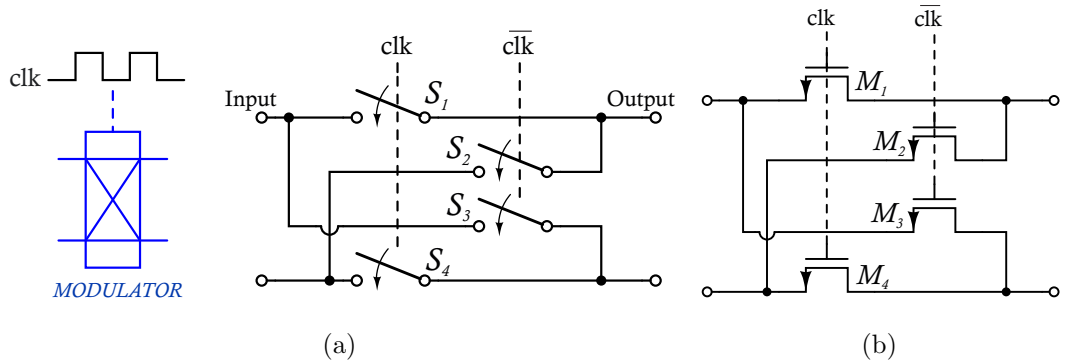



Figure 4.3: a) Schematic of a Modulator and b) its implementation with MOSFET.

The main problem introduced by switches in a chopping amplifier is the charge injection, as it produces an unwanted ripple at the output of the amplifier (glitches). This inconvenient is caused by two phenomena: redistribution of channel charge and clock feed-through. Several techniques for reducing charge injection can be applied [7-8]:

- Dummy Switches: Charge injection can be reduced by adding dummy switches driven by a complementary clock, which inject an amount of charge that compensates for the charge injected by the main switch. The dummy switch can be connected in series, as shown in Figure 4.4a, or in parallel.

- Complementary Switches: Another way to reduce the charge injection is to use a transmission gate, as shown in Figure 4.4b, so that the PMOS and the NMOS transistors inject opposite charge and cancel each order.

- Fully Differential Circuit: Another way to compensate charge injection is to use fully differential configurations. If the charge injection in the two half circuits matches, the charge injection only results in a change in the common-mode voltage, which is finally cancelled out at the output.

For the design of the proposed chopper amplifiers and in order to reduce the charge injection, the modulator blocks in this Thesis were implemented with complementary devices, as shown in Figure 4.5. When *clk* goes to GND, the transistors $M_{N1}$ and $M_{P1}$ are turned on, allowing the signal to pass, whereas the transistor $M_{N2}$ and $M_{P2}$ are in the cut-off region. When *clk* changes its logic state, the transistors $M_{N1}$ and $M_{P1}$ enter the cut-off region, whereas $M_{N2}$ and $M_{P2}$ are turned on. In this way, the signal is modulated with chopping frequency $f_{chop}$ defined by the clock frequency.

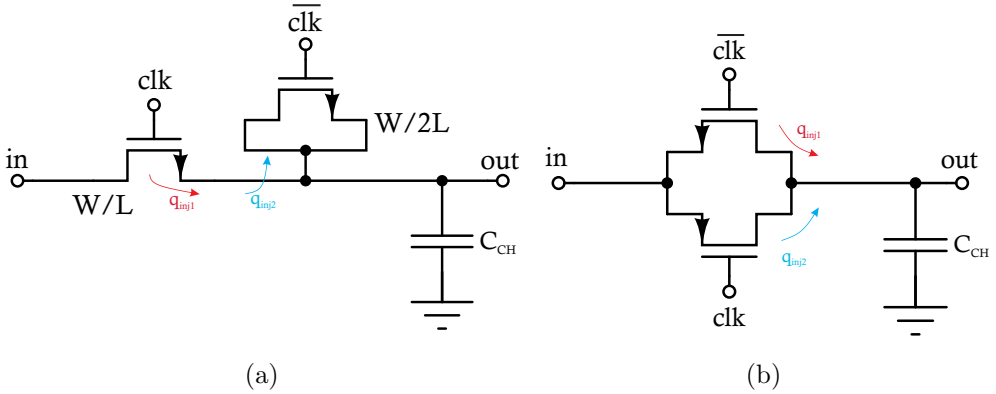



Figure 4.4: Charge Injection Compensation with: a) a dummy switch, and b) a transmission gate.

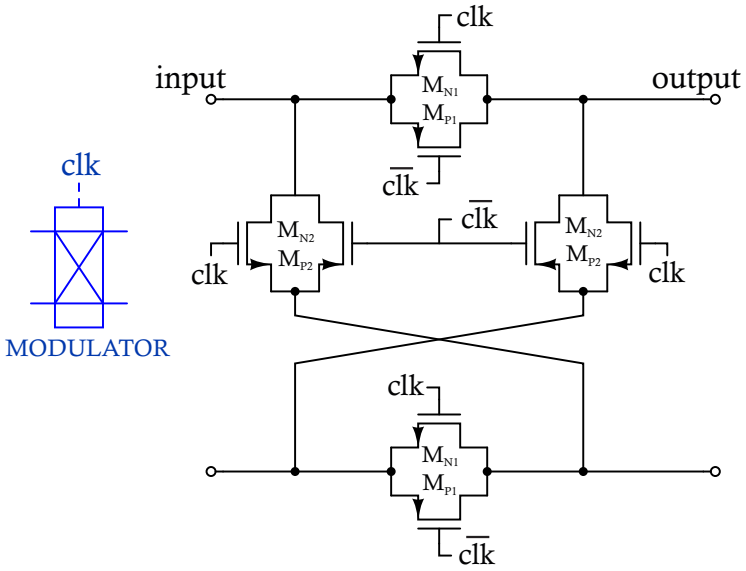



Figure 4.5: Schematic Circuit of the Implemented Chopper.

The modulator block was designed in a $0.18\mu m$ CMOS standard process, with $(W/L)_N = 2(W/L)_P$ so that the charge injections are compensated, and with minimum PMOS transistor dimensions, in order to reduce the parasitic capacitances. Figure 4.6 shows the layout of the modulator block. The active area of the circuit is $10\mu m$x$6\mu m$.

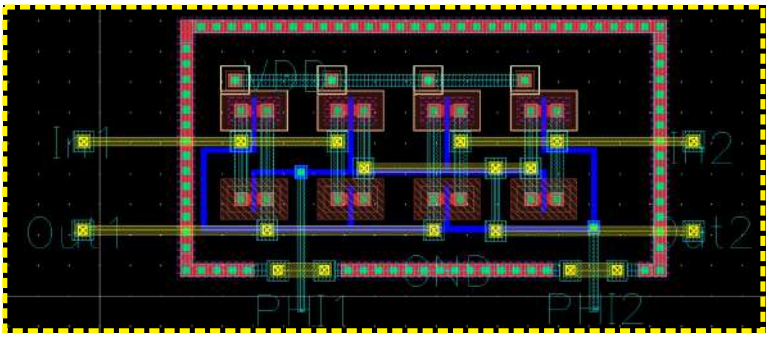



Figure 4.6: Layout of the chopper modulator.

Non idealities in clock timing, such as clock skew and overlapping, introduce residual offset. Clock skew is a phenomenon in which the clock signals change at different transitions times. Overlapping, in turn, occurs when there is a time lag and both clocks are high/low at the same time for a short period, causing a short circuit between the differential signal paths. This causes a low input impedance, so, the effective gain of the amplifier is reduced, resulting in increased noise and offset [7].

To avoid this effect, a non-overlapping circuit is required. In synchronous circuits, a two-phase clock refers to clock signals distributed on two wires, each with non-overlapping pulses. Figure 4.7 shows the non-overlapping clock generator using NAND and inverters gates with feedback.

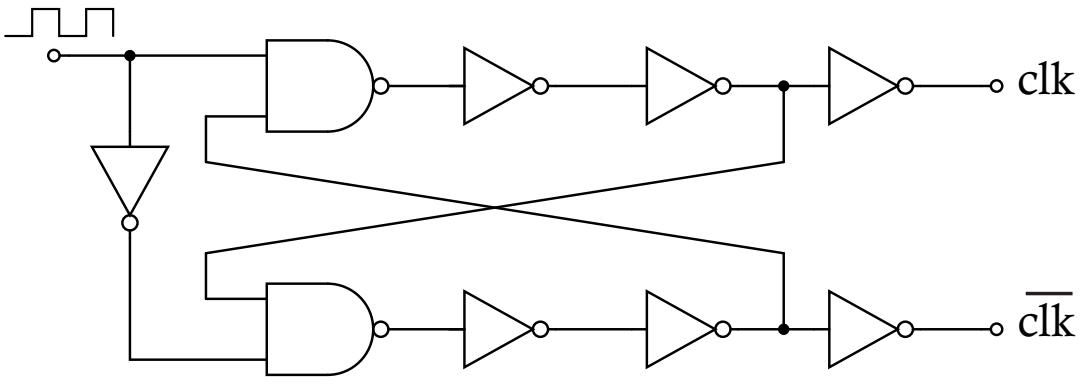



Figure 4.7: Two-Phase Non-overlapping Clock Generator.

The non-overlapping clock generator was designed in the same $0.18\mu m$ CMOS standard process. The dimensions of the transistors were designed so that the logic gates switch at $V_{DD}/2$. Figure 4.8 shows the layout, with an active area of $75\mu m$x$10\mu m$.

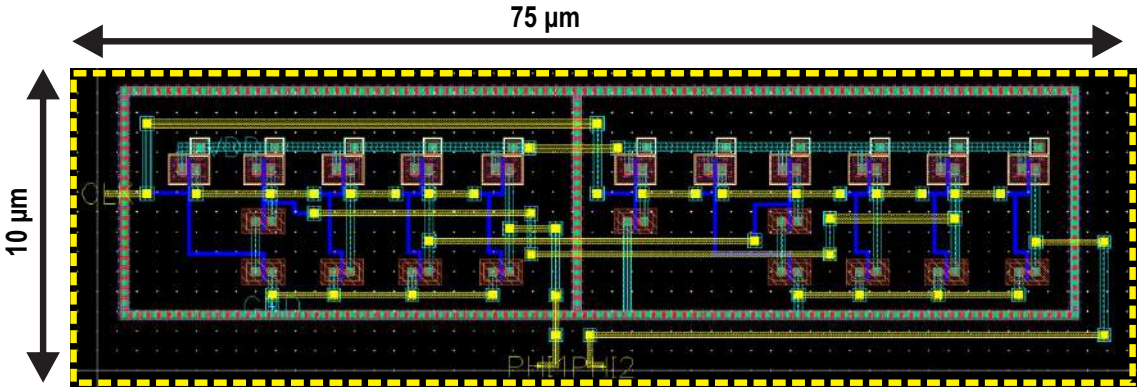
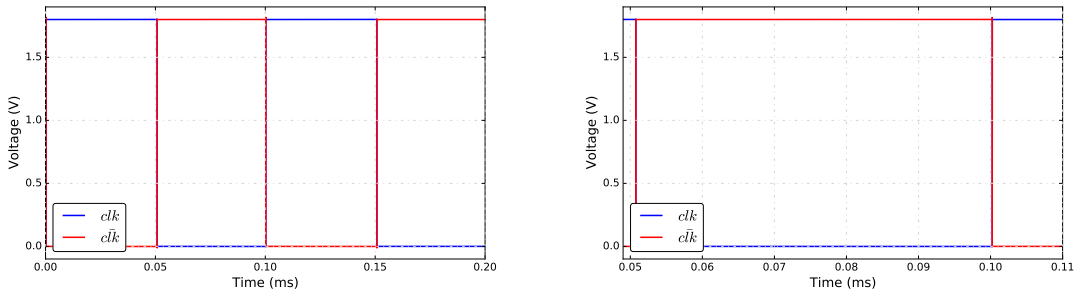



Figure 4.8: Layout of the Non-Overlapping Clock Generator.

Figure 4.9 shows the time response of the two-phase clock generator, when, injecting a square signal with $f_{clk} = 10kHz$. The simulation shows both non-overlapping output signals.




(a) (b)

Figure 4.9: Simulation of the two-phase clock.

## 4.2 Chopper Amplifier 0 (ChA-0)

Figure 4.10 shows the block diagram of the first proposed chopper amplifier, which will be called ChA-0. The chopper technique is applied to the voltage amplifier LNP-0 by means of an external chopper modulator $CH1$, an embedded chopper modulator $CH2$, and the output filter LPF-0.

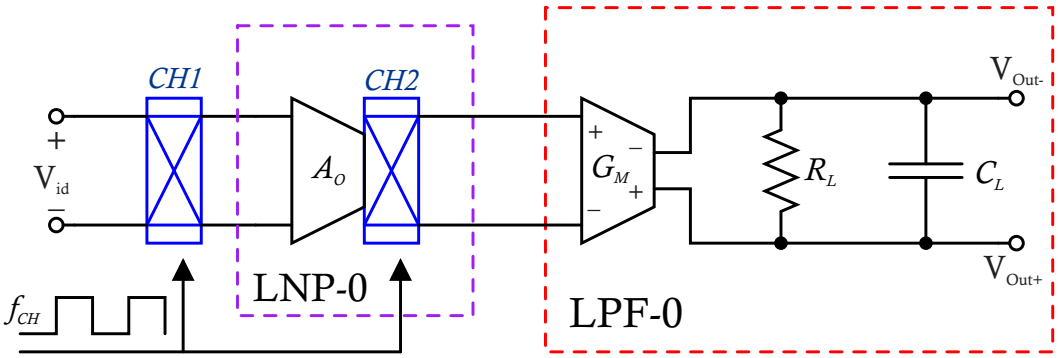



Figure 4.10: Block Diagram of Chopper Amplifier 0.

Figure 4.11 shows the complete schematic circuit. The LNP-0 was chosen for its low noise contribution ($9.7\mu V_{rms}$) and high linearity ($THD = 1\%$ for input signals up to $4mVpp$). Cascode transistors $M_{SW1}$ and $M_{SW2}$ in the output branches are used to implement the output modulator $CH2$, making use of the generated low impedance nodes, thus reducing glitches and resulting in a more compact solution [12]. The LPF-0 is based on the same transconductance cell as the LNP-0, with reduced power consumption ($14\mu W$ versus the $70\mu W$ consumed by the LNP-0 presented in Section 3.3.1) and a cut-off frequency of $1kHz$ to eliminate the modulated noise components. It also features a programmable gain through the control voltage of the pseudo-resistor $PR2$ without degrading noise performance.

### 4.2.1 Simulation Results

The proposed circuit was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage, and consumes $84\mu W$ total power. The frequency response is shown in Figure 4.12. The circuit presents a differential gain of $41dB$ and $1kHz$ bandwidth. Figure 4.13 shows the time response for a $500\mu V$ amplitude sine input signal at $250Hz$. The demodulated and amplified input signal is shown before filtering the modulated noise (Figure 4.13a), and

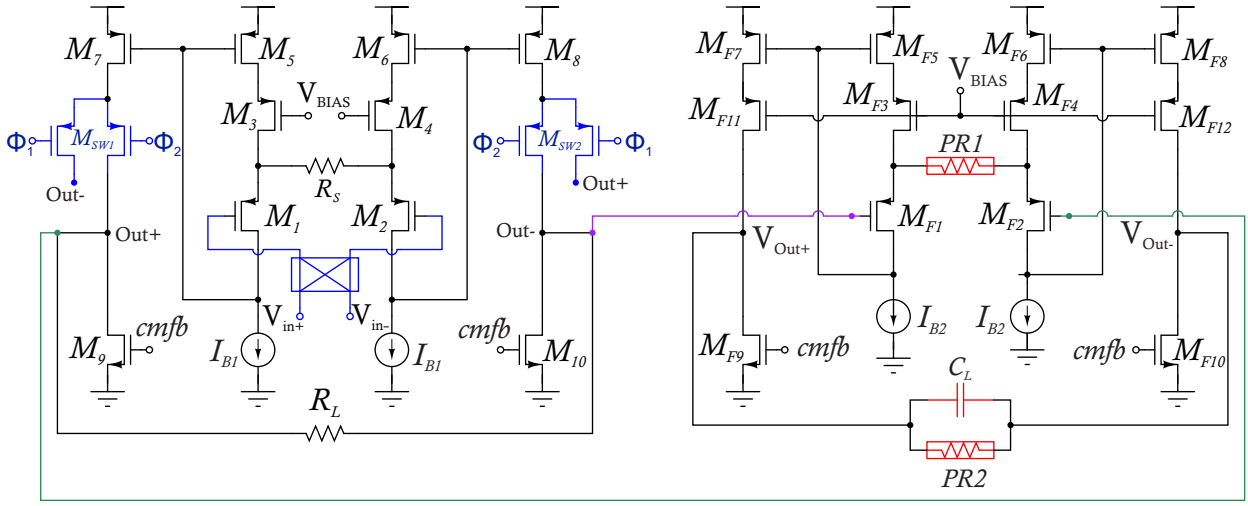



Figure 4.11: Proposed Chopper Amplifier 0.

at the output of the LPF (Figure 4.13b). The total harmonic distortion of the output signal under these conditions is 1.5%. The simulated CMRR and PSRR is $75dB$ and $72dB$, respectively, at $50Hz$.

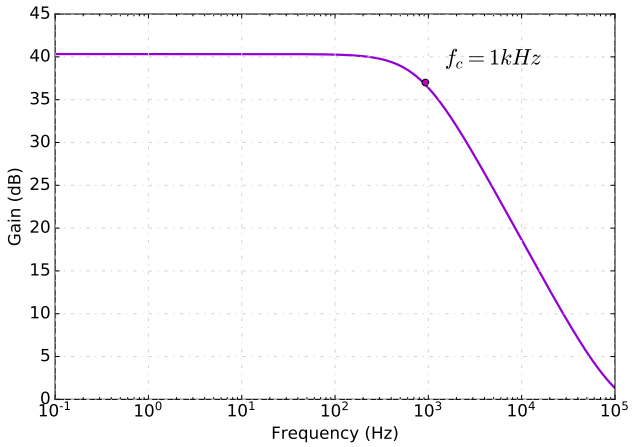
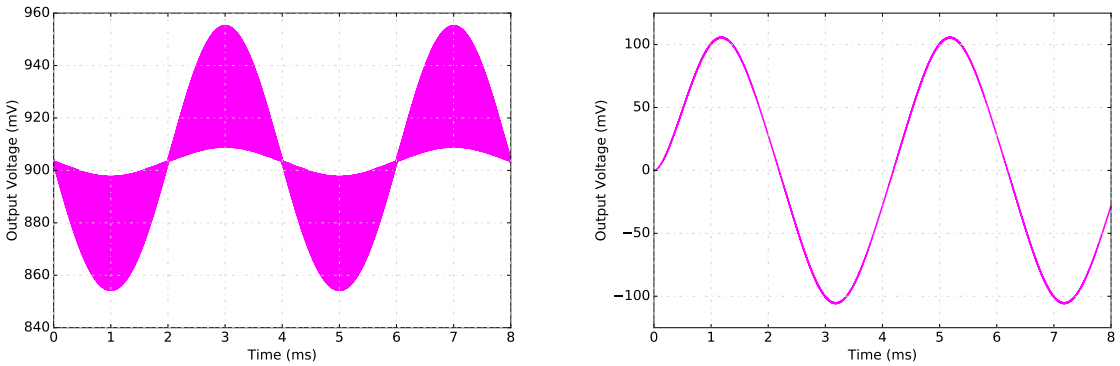



Figure 4.12: Frequency Response of Chopper Amplifier 0.

After running the PSS simulation in conjunction with PNoise, the input-referred noise power spectral density of both the LNP-0 and the proposed ChA-0 is shown in Figure 4.14 for comparison. At $250Hz$ the input-referred noise decreases from $24.5nV/\sqrt{Hz}$ without the chopping technique, to $14.5nV/\sqrt{Hz}$ with the chopping technique. When integrated




(a) (b)

Figure 4.13: Waveforms at the a) input and b) output of the Low-Pass Filter.

from $0.1Hz$ to $1kHz$ the input referred noise is $1\mu V_{rms}$ for the LNP-0, and $0.56\mu V_{rms}$ for the whole configuration. The efficiency factors of the ChA-0 are $NEF = 4.6$ and $PEF = 38V$.

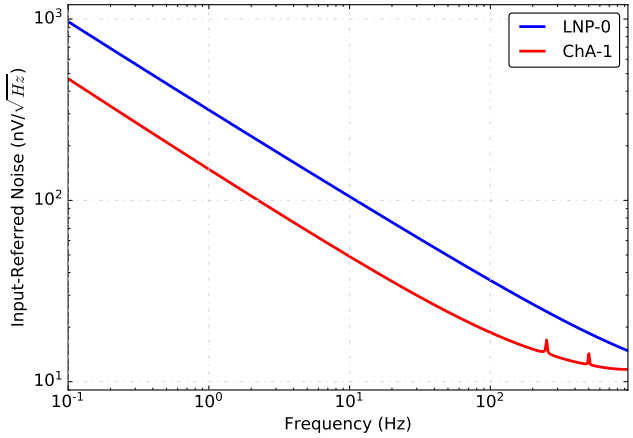



Figure 4.14: Comparison of Input-Referred Noise between the LNP-0 and the ChA-0.

## 4.3 Chopper Amplifier 1 (ChA-1)

The block diagram of the proposed Chopper Amplifier 1 is shown in Figure 4.15. It consists of the VGLNP-4, based on bootstrapping technique, and the LPF-1. The VGLNP-4 was selected as the main preamplifier as it featured the lowest power consumption ($12.3\mu W$) with $NEF = 2.6$, $PEF = 12.2V$ and programmable gain. The LPF-1 was used in this configuration due to the low cut-off frequency ($f_c = 1kHz$ with $C_L = 20pF$) and the ability to adjust both the gain and frequency.

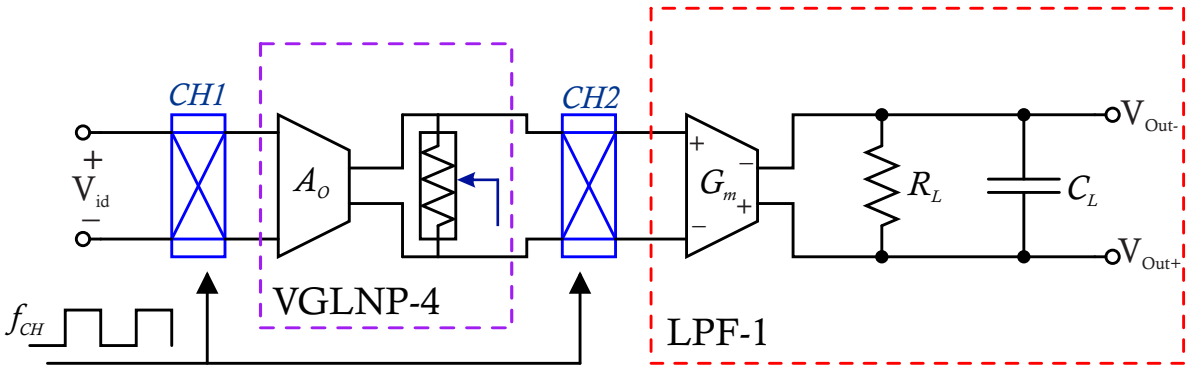



Figure 4.15: Block Diagram of the Chopper Amplifier 1.

The transistor level circuit of the ChA-1 is shown in Figure 4.16. In contrast with the LPF-1 in Chapter 3, here the polysilicon resistors $R_S$ were replaced by MOS transistor $M_{Rs}$ in order to reduce the required area. To ensure linearity, transistors $M_{Rs}$ were biased in deep triode. Besides, the gain can be modified through $V_{tune}$. Ultimately, the load floating bootstrapping resistor makes it possible to modify the cut-off frequency of the filter when the bias current $I_{B4}$ is modified.

### 4.3.1 Simulation Results

The proposed circuit was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage, and consumes $31\mu W$ total power. All transistors in the preamplifier and filter were biased in the weak inversion region. The bias currents were set to $I_{BIAS1} = 500nA$ and $I_{BIAS2} = 250nA$ for the VGLNP-4, whereas the output load bootstrapping resistor was biased with $I_{b1} = I_{b2} = 1\mu A$ and $I_{b3} = 500nA$. The bias currents in the LPF-1 were set to $I_{B1} = 500nA$ and $I_{B2} = 250nA$. The frequency response of the ChA-1 under these conditions is shown in Figure 4.17. The circuit presents a differential gain

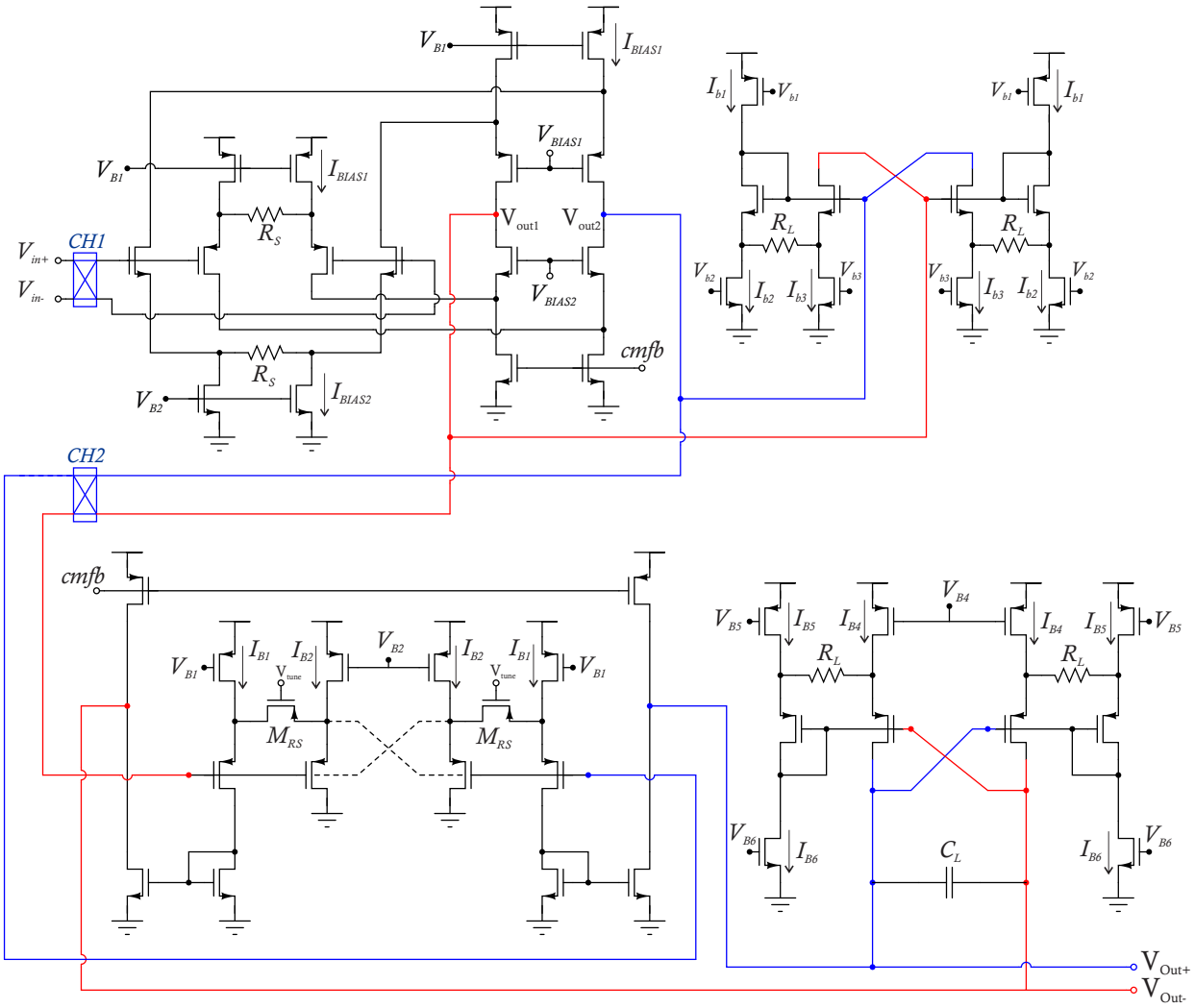



Figure 4.16: Schematic Proposed Chopper Amplifier 1.

of $41.5dB$ and $800Hz$ bandwidth. Figure 4.18 shows the time response for a $600\mu Vpp$ sine input signal at $50Hz$. The demodulated and amplified input signal is shown before filtering the modulated noise (Figure 4.18a), and at the output of the LPF (Figure 4.18b).

The input-referred noise power spectral density of the VGLNP-4 and ChA-1 is shown in Figure 4.19a. At $250Hz$ the input-referred noise decreases from $30nV/\sqrt{Hz}$ without the chopping technique, to $16nV/\sqrt{Hz}$ with the chopping technique. When integrated from $0.1Hz$ to $1kHz$ the input referred noise is $2.7\mu V_{rms}$ for the VGLNP-4, and $1\mu V_{rms}$ for the whole configuration. In order to determine the offset voltage, Monte Carlo simulations (1000 runs) were carried out. Figure 4.19b shows the histogram of the

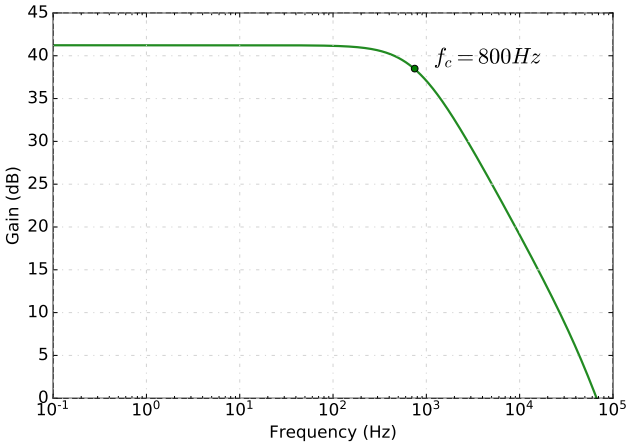
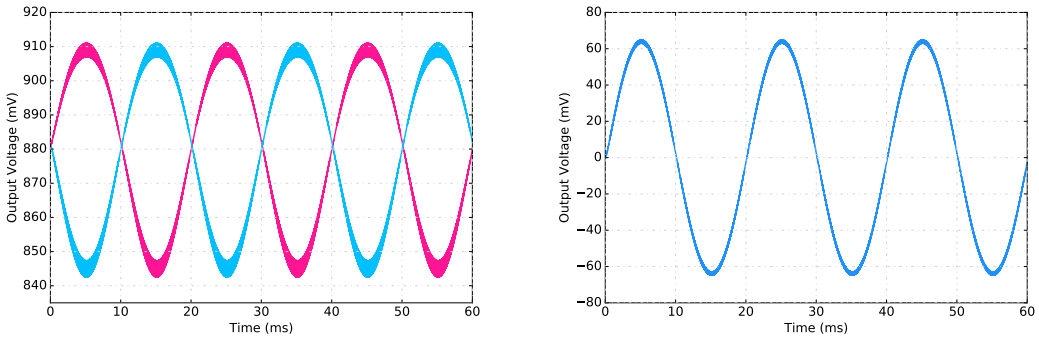



Figure 4.17: Simulated frequency response of the ChA-1.



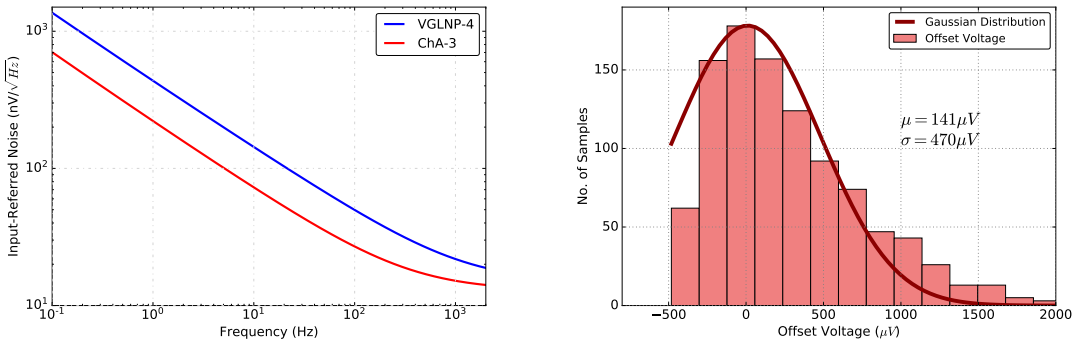

(a) (b)

Figure 4.18: Waveforms at the a) input and b) output of the Low-Pass Filter.

input-offset voltage, which has a mean value of $141\mu V$ and $470\mu V$ standard deviation, whereas the VGLNP-4 presented an input-offset voltage with mean value of $243\mu V$ and $364.5\mu V$ standard deviation.

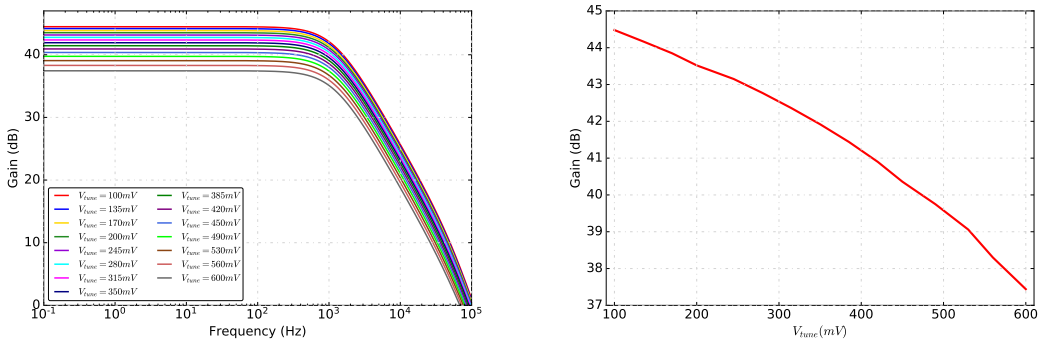
As already mentioned, the filter gain is programmable through the control voltage $V_{tune}$. When this voltage is varied from $100mV$ to $600mV$, the gain changes from $37dB$ to $45dB$ with constant cut-off frequency of $800Hz$. Figure 4.20a shows the frequency response for several $V_{tune}$ values, and Figure 4.20b presents the $dB$ gain versus the $V_{tune}$ values.

Finally, the Chopper Amplifier 1 presents a $NEF = 5$ and a $PEF = 46.2V$ for a




(a) (b)

Figure 4.19: Simulation of a) input-referred noise and b) Input Offset Histogram from Monte Carlo Analysis.




(a) (b) Gain vs $V_{tune}$

Figure 4.20: Simulated a) Frequency Response for several $V_{tune}$ at $M_{Rs}$ and b) Gain vs $V_{tune}$ of the ChA-1.

noise integration bandwidth from $0.1Hz$ to $1kHz$.

### 4.3.2 Experimental Results

The ChA-1 was integrated in $0.18\mu m$ CMOS standard technology with $1.8V$ power supply. A microphotograph and layout of the ChA-1 are shown in Figure 4.21. The frequency response is shown in Figure 4.22. The measured gain is $39dB$ with $1.3kHz$ bandwidth. Figure 4.23 shows the response in the time domain.

Figure 4.24 shows the measured input-referred noise power spectral density of both the VGLNP-4 and the ChA-1. The input low-frequency noise level measured at $200Hz$ is $35nV/\sqrt{Hz}$, for the VGLNP-4, and is reduced down to $16nV/\sqrt{Hz}$ for the whole

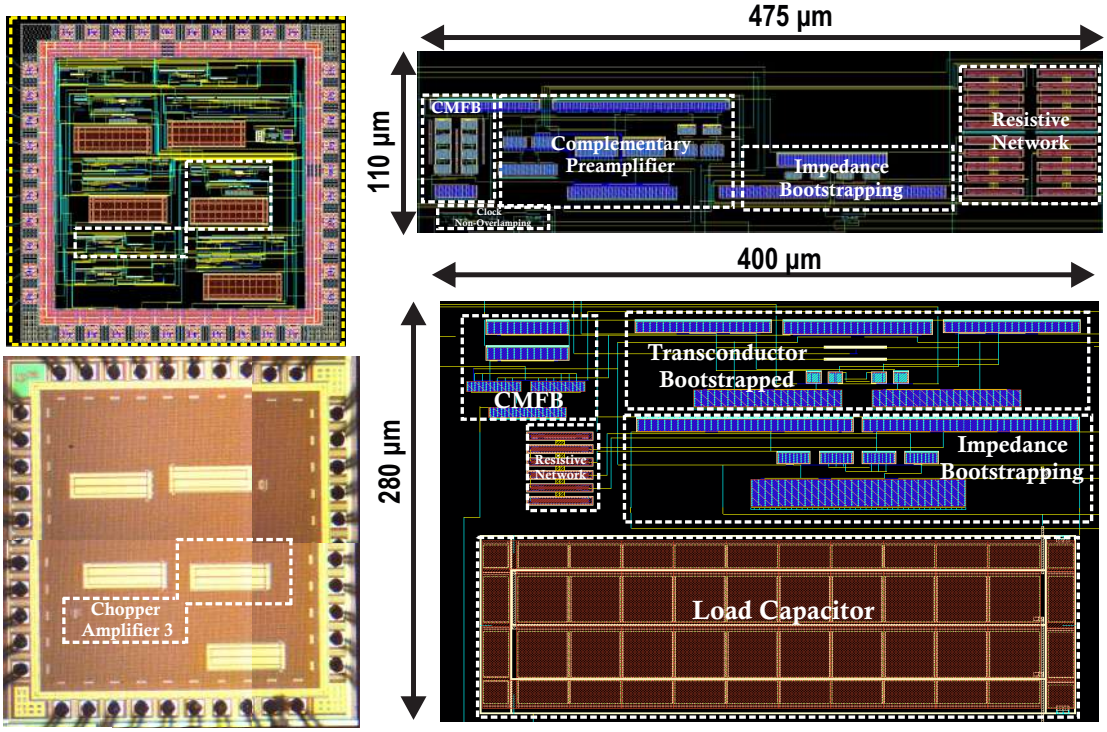



Figure 4.21: Microphotograph and Layout of the Proposed Chopper Amplifier 1.

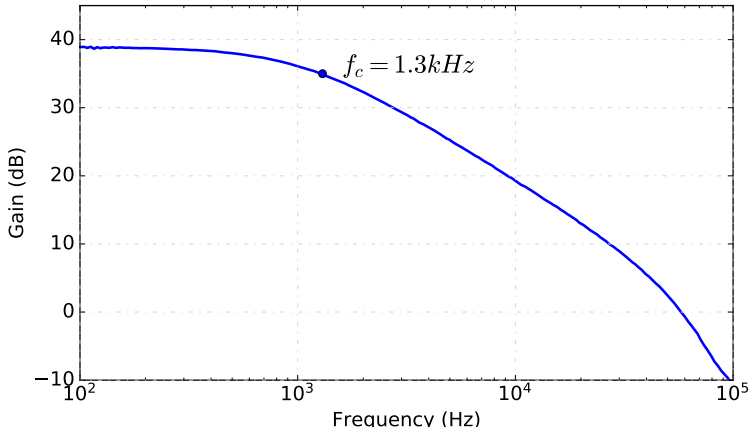



Figure 4.22: Experimental frequency response of the ChA-1.

configuration. When integrated from $100Hz$ to $1kHz$, the experimental input-referred noise is reduced from $8.2\mu V_{rms}$ for the VGLNP-4 to $1.2\mu V_{rms}$. The efficiency factors of the ChA-1 are $NEF = 8.9$ and $PEF = 144V$.

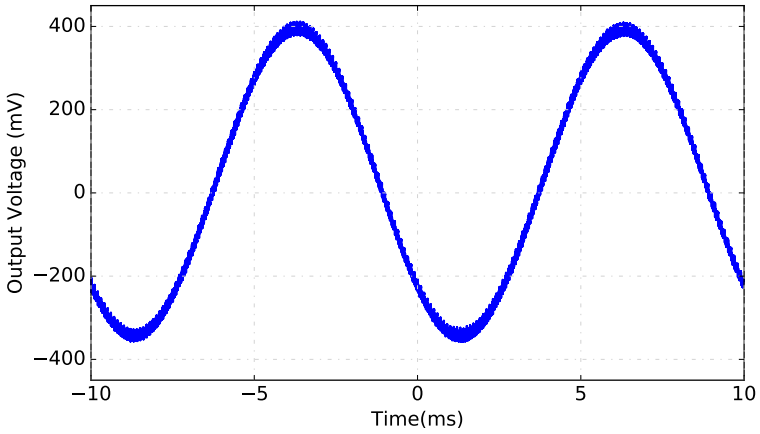



Figure 4.23: Experimental time response of the ChA-1.

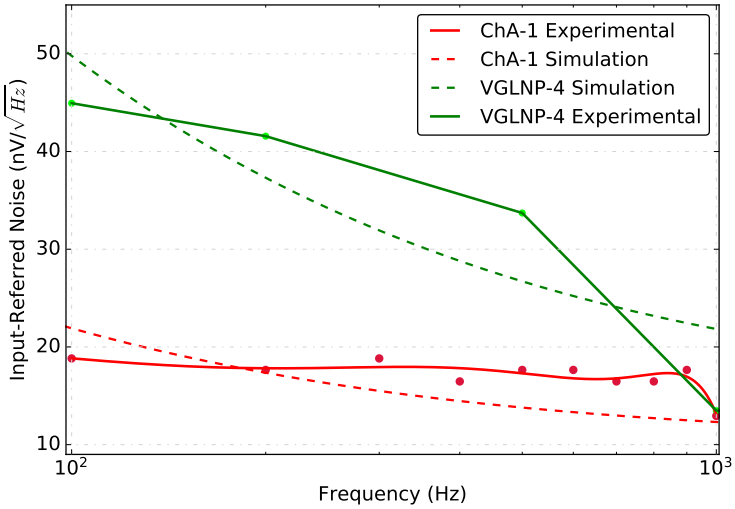



Figure 4.24: Comparative between measured and simulated input-referred noise of the VGLNP-4 and the ChA-1.

## 4.4 Chopper Amplifier 2 (ChA-2)

Figure 4.25 shows the block diagram of the chopper amplifier 2 (ChA-2). It consists of the VGLNP-4, input and output chopper modulators (ChA-1 and ChA-2) and the output filter LPF-2a. The detailed schematic of the ChA-2 is shown in Figure 4.26. As for the ChA-1, the VGLNP-4 was chosen because of its low power consumption ($9.45\mu W$) with good efficiency factors and programmable gain (from $35dB$ to $42dB$). The LPF-2a is

used because of its low power consumption ($5.3\mu W$), a tunable low cut-off frequency from $2kHz$ to $18kHz$ with $C_L = 20pF$ and moderate area consumption ($0.144mm^2$). The chopper modulators and the clock signal generator were implemented as shown in Section 4.1.

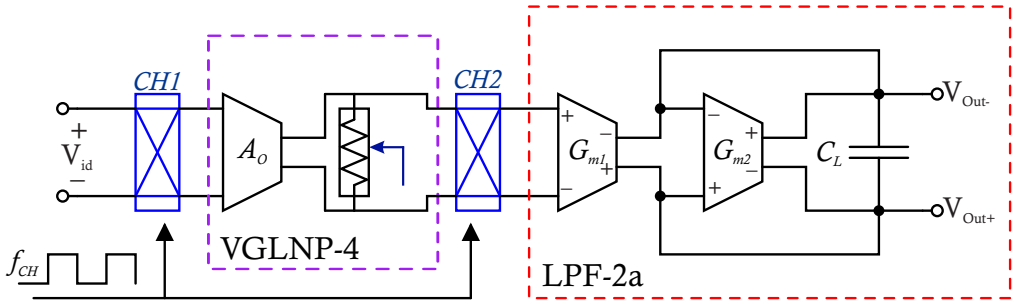



Figure 4.25: Block Diagram of the Chopper Amplifier 2.

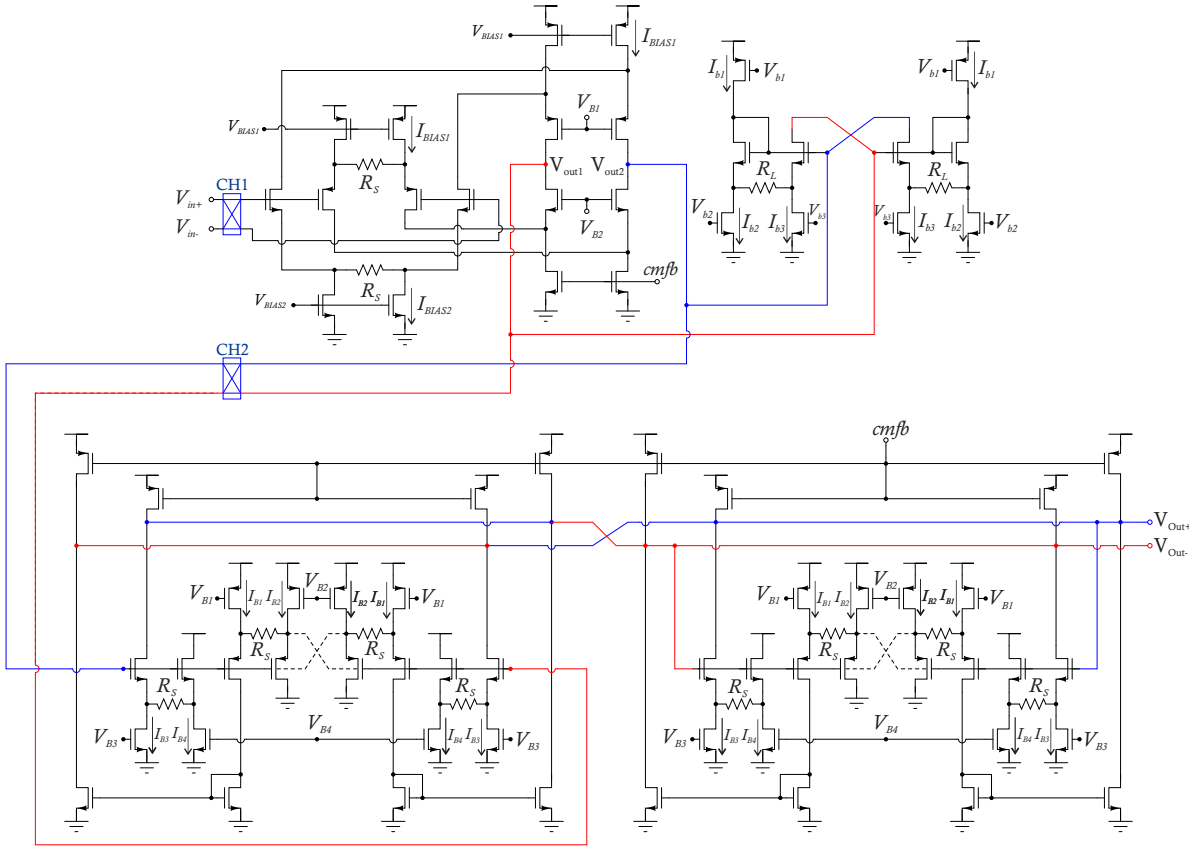



Figure 4.26: Schematic-Proposed of the Chopper Amplifier 2.

### 4.4.1 Simulation Results

The ChA-2 was designed in a $0.18\mu m$ CMOS process with $1.8V$ supply voltage. All transistors in the preamplifier and filter were biased in weak inversion. The total power consumption of the circuit is $12.2\mu W$. The bias currents were set to $I_{BIAS1} = 500nA$ and $I_{BIAS2} = 250nA$ for the VGLNP-4, whereas the load bootstrapping resistor was biased with $I_{b1} = I_{b2} = 1\mu A$ and $I_{b3} = 500nA$. The frequency response is shown in Figure 4.27. The chopper amplifier provides a differential gain of $39.2dB$ and $1.6kHz$ bandwidth. Figure 4.28 shows the time response for a $1mVpp$ sine input signal at $50Hz$ before filtering and at the output of the low-pass filter.

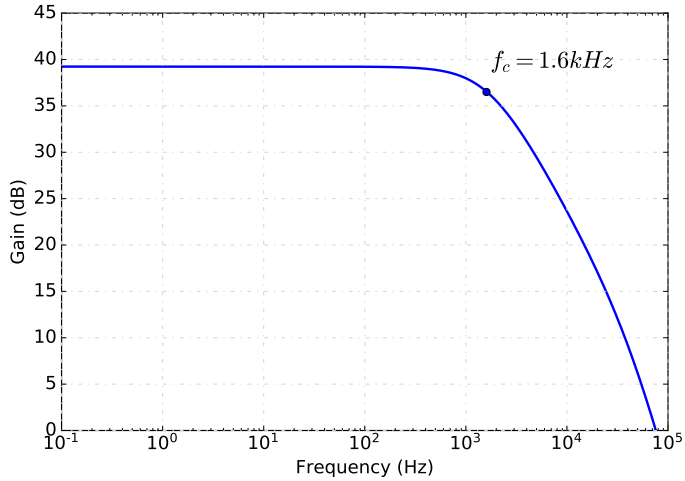
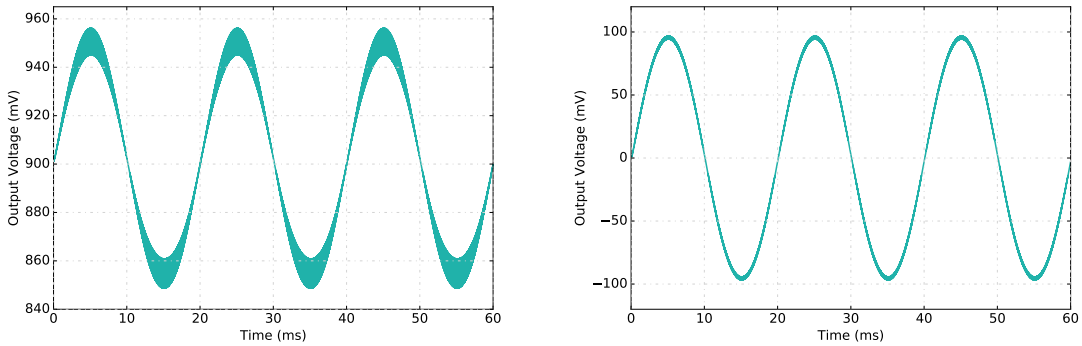


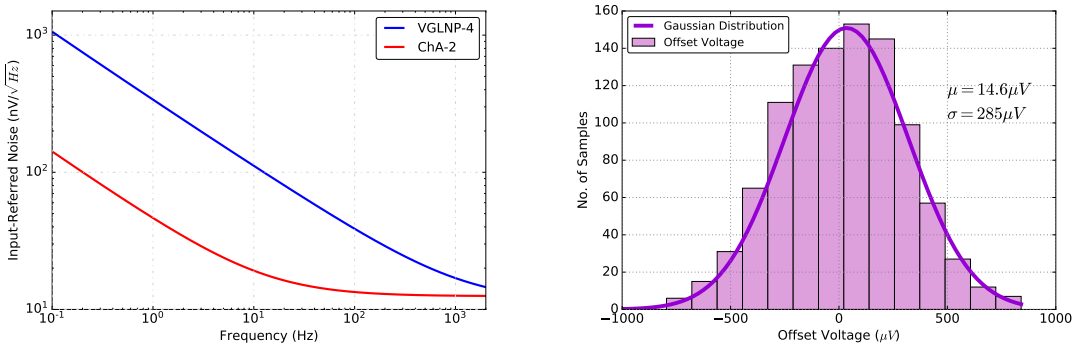

Figure 4.27: Frequency Response of the Chopper Amplifier 2.




(a) (b)

Figure 4.28: Waveforms at the a) input and b) output of the LPF.

The input-referred noise power spectral density of both the VGLNP-4 and the Chopper Amplifier 2 are shown in Figure 4.29a. When integrated from $0.1Hz$ to $1kHz$, the input-referred noise is $2.7\mu V_{rms}$ without chopping technique and decreases to $0.42\mu V_{rms}$ for the whole configuration. In order to determine the offset voltage, Monte Carlo simulations (1000 runs) were carried out. Figure 4.29b shows the histogram of the input-offset voltage, which has a mean value of $14.5\mu V$ and $285\mu V$ standard deviation. The input-offset voltage without chopping was $202\mu V$ with $364.5\mu V$ standard deviation.




(a) (b)

Figure 4.29: a) Input-referred Noise PSD and b) Input Offset Histogram from Monte Carlo Analysis of ChA-2.

Figure 4.30 shows the THD for a sine differential input voltage at $50Hz$ and with input amplitude varying from $500\mu V$ to $2mV$. The simulation carried out shows that, the THD remains below $-40dB$ up to $3.6mVpp$.

It is possible to change the gain of the ChA-2 from $28dB$ to $43dB$ when the bias currents $I_{B1}$ and $I_{B2}$ of the LPF-2a change from $100nA$ to $500nA$ without modifying the cut-off frequency ($f_c = 1.6kHz$). Figure 4.31 shows the frequency response when $I_{B1}$ and $I_{B2}$ change from $100nA$ to $500nA$, and from $100nA$ to $200nA$ respectively.

The input-referred noise is reduced from $8\mu V_{rms}$ for the VGLNP-4 to $420nV_{rms}$ in a range frequency from $0.1Hz$ to $1.6kHz$. The efficiency factors are $NEF = 1.5$ y $PEF = 3.7V$.

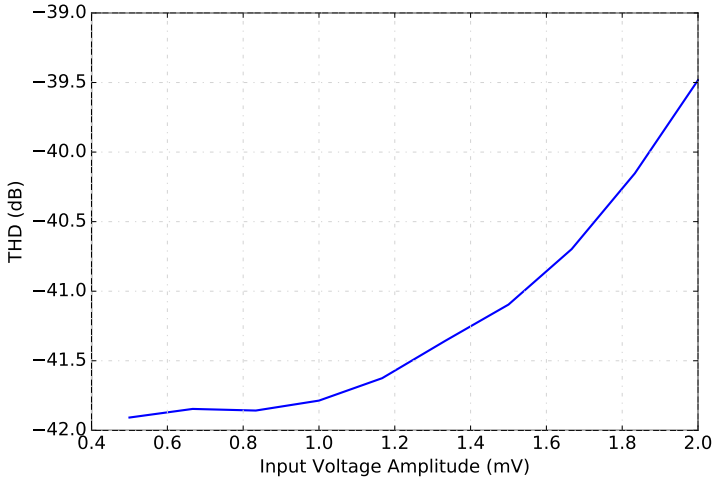



Figure 4.30: THD for several Input Voltages.

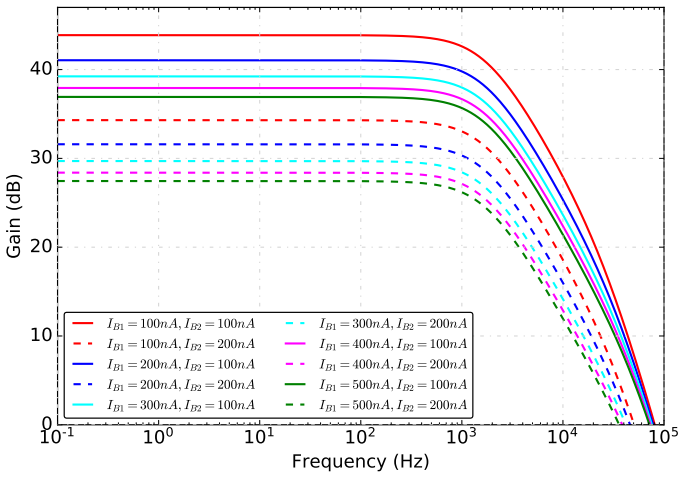



Figure 4.31: Gain programmability for several bias currents in the impedance scaler.

### 4.4.2 Experimental Results

The ChA-2 was integrated in $0.18\mu m$ CMOS standard technology. A chip microphotograph is shown in Figure 4.32. For experimental characterization, the bias current $I_{BIAS1}$ was set to $500nA$, whereas $I_{BIAS2}$ was set to $250nA$. The bias currents in the impedance scaler were $I_{b1} = I_{b2} = 500nA$ and $I_{b3} = 170nA$. Finally, the bias currents in the low-pass filter were $I_{B1} = I_{B3} = 150nA$, $I_{B2} = I_{B4} = 100nA$.

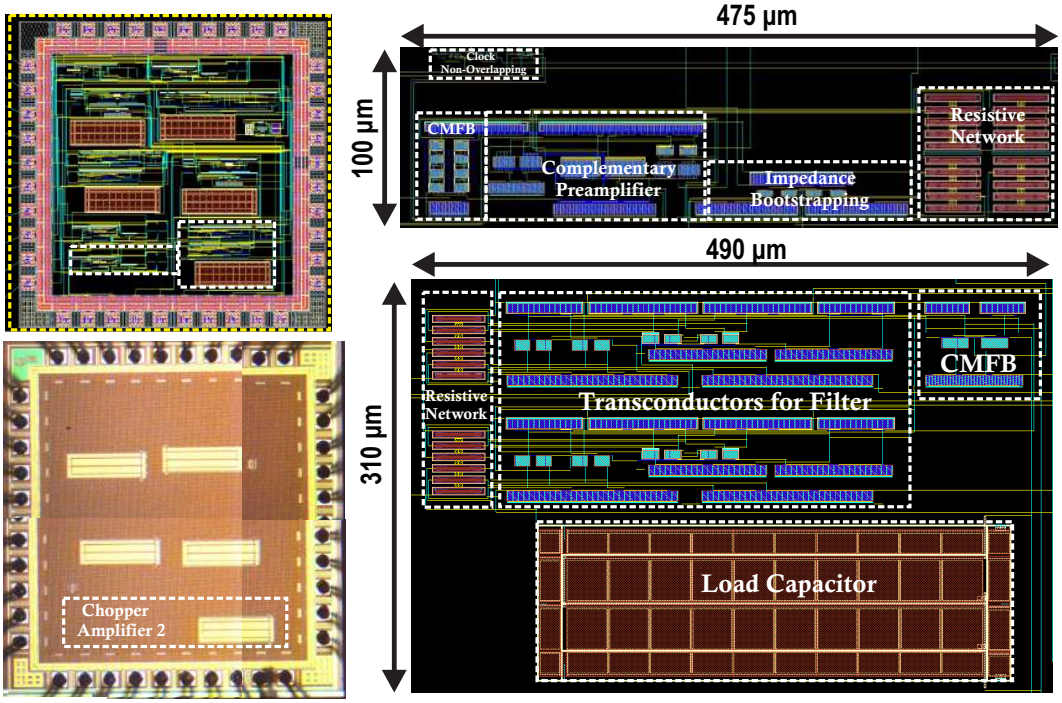



Figure 4.32: Microphotograph and Layout of the Proposed Second Chopper Amplifier

Figure 4.33 shows the experimental frequency response at the highest gain, i.e. $38.5dB$, and it shows a bandwidth of $1kHz$. Figure 4.34 shows the response in the time domain.

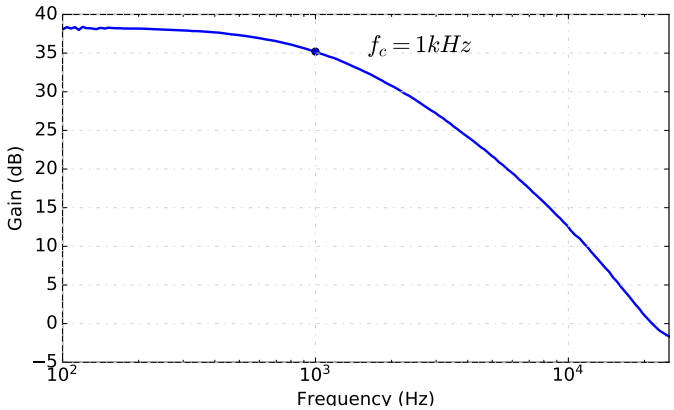



Figure 4.33: Experimental frequency response of the ChA-2.

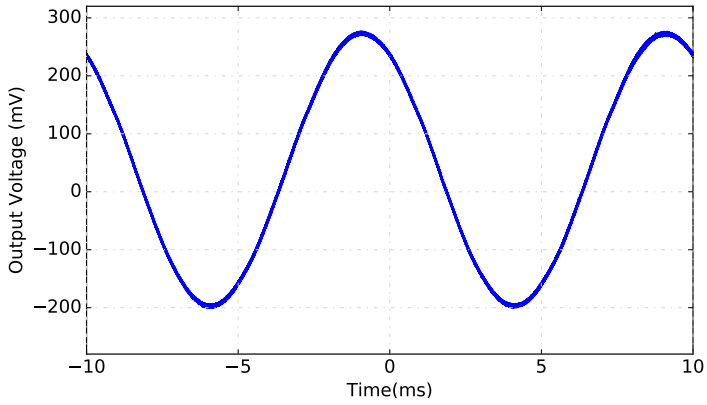



Figure 4.34: Experimental time response of the ChA-2.

Figure 4.35 shows the measured input-referred noise power spectral density of both the VGLNP-4 and the ChA-2. The input low-frequency noise level measured at $200Hz$ is $35nV/\sqrt{Hz}$, for the VGLNP-4, and is reduced down to $20nV/\sqrt{Hz}$ at $200Hz$ for the ChA-2. Integrating from $100Hz$ to $1kHz$, the experimental-referred noise is reduced from $8.2\mu V_{rms}$ for the VGLNP-4 to $0.65\mu V_{rms}$. The efficiency factors are $NEF = 3.6$ y $PEF = 24.2V$.

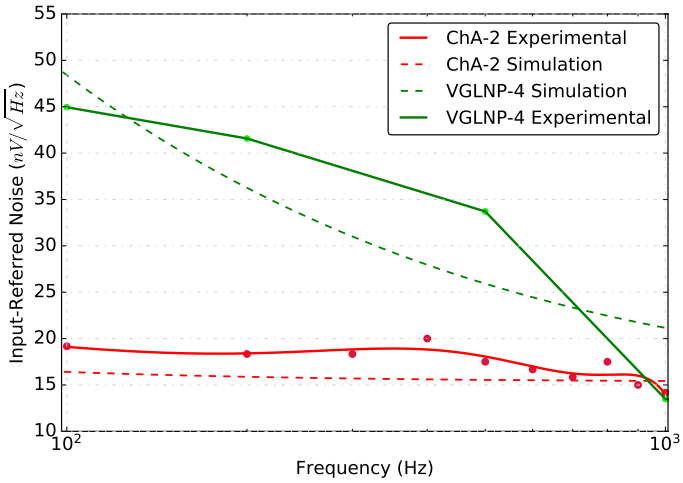



Figure 4.35: Comparative between measured and simulated input-referred noise of the VGLNP-4 and the ChA-2.

According to the experimental results, the ChA-2 shows a NEF of 3.6 and a $PEF$ of $24.2V$ with a noise integration bandwidth from $100Hz$ to $1kHz$.

### 4.4.3 Comparison

Table 4.1 shows the simulated and measured performance of the three proposed chopper amplifiers. The ChA-0 shows low input-referred noise and a good trade-off between noise, power consumption and bandwidth. However, the high power consumption makes it an unattractive solution for portable applications. The ChA-1 in contrast, reduces the power consumption, but at a cost of increasing the input-referred noise, which leads to a slight increase in the noise efficiency factor. Finally, the ChA-2 presents the lowest consumption, the lowest input-referred noise and, therefore, the best NEF and PEF.

In Table 4.2 the ChA-2 is compared with other chopping amplifiers found in the literature. Together with [17], the ChA-2 shows the lowest input-referred noise, which is only $650nV_{rms}$. In terms of NEF, the lowest value is achieved by [17], as the ChA-2 is penalized by the power consumption. Even so, it achieves a good noise efficiency factor of 3.6. Furthermore, the proposed configuration is the only one which provides control of both the gain and the cut-off frequency, so the amplifier can be adapted according to the range of signals to be handled.

Table 4.1: Performance Comparison between the Proposed Chopper Amplifiers.

| Parameters | ChA-0 | ChA-1 | | ChA-2 | |
|---|---|---|---|---|---|
| | Simulation | Simulation | Experimental | Simulation | Experimental |
| Technology ($\mu m$) | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 |
| Supply ($V$) | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| Gain ($dB$) | 39 - 42 | 37 - 44 | 39 | 28 - 42 | 38.5 |
| Bandwidth ($kHz$) | 1 | 0.8 | 1.3 | 1.6 | 1 |
| Power ($\mu W$) | 84 | 31 | 68 | 12.2 | 35 |
| Input-Referred Noise ($\mu V_{rms}$) | 0.56 (0.1Hz-1kHz) | 1 (0.1Hz-1kHz) | 1.2 (100Hz-1kHz) | 0.42 (0.1Hz-1kHz) | 0.65 (100Hz-1kHz) |
| CMRR ($dB$) | 75 @250 Hz | 68 @50 Hz | - | 70 @50 Hz | - |
| PSRR ($dB$) | 70 @250 Hz | 70 @ 50 Hz | - | 70 @50 Hz | - |
| Mean Offset ($\mu V$) | 650 | 141 | - | 14.6 | - |
| Chopper Freq ($kHz$) | 50 | 20 | 20 | 20 | 20 |
| THD (%) @Output Voltage (mVpp) | 1 200 @250 Hz | 1.5 260 @50 Hz | 2.5 200 @100 Hz | 1 190 @50 Hz | 2 200 @100 Hz |
| Area ($mm^2$) | - | - | 0.154 | - | 0.186 |
| NEF | 4.6 | 5 | 8.9 | 1.5 | 3.6 |
| PEF ($V$) | 38 | 46.2 | 142.5 | 3.7 | 24.2 |
| Gain/Frequency Programmability | Yes/No | Yes/Yes | Yes/Yes | Yes/Yes | Yes/Yes |

Table 4.2: Performance Comparison of the Chopper Amplifier 2 with other Works.

| Parameters | Jiawei [13] 2017 | Hui Wang [14] 2018 | Chung-Yu Wu [15] 2018 | Zheng [16] 2018 | Deng-Luo [17] 2018 | Chung-Jae [18] 2019 | Deng-Luo [19] 2020 | ChA-2 Measure |
|---|---|---|---|---|---|---|---|---|
| Technology ($\mu m$) | 0.13 | 0.18 | 0.18 | 0.18 | 0.18 | 0.13 | 0.18 | 0.18 |
| Vsupply ($V$) | 1.2 | 0.8 | 1.8 | 1.2 | 1.8 | 1 | 0.8 | 1.8 |
| Gain ($dB$) | 40 | 56 | 49 - 68 | 58 | 40 | 55 | 43.4 | 38 |
| Bandwidth ($kHz$) | 5 | 0.13 | 0.117 | 0.5 | 5.4 | 1.1 | 0.65 | 1 |
| Power ($\mu W$) | 3.5 | 4 | 3.26 | 9.24 | 3.25 | 2.3 | 2.3 | 35 |
| Input-Referred Noise ($\mu V_{rms}$) | - - | - - | 2 (0.6Hz-117Hz) | 1.3 (0.5Hz-500Hz) | 0.65 (0.3Hz-200Hz) | 2.18 (0.01Hz-1kHz) | 1.2 (1Hz-650Hz) | 0.65 (100Hz-1kHz) |
| CMRR ($dB$) | 85 | - | 67 | >100 | >100 @50 Hz | 125 | >100 @50 Hz | 70[1] @ 50 Hz |
| PSRR ($dB$) | - | - | 69 | - | >70 @1 kHz | - | - | 70[1] @ 50 Hz |
| Offset ($\mu V$) | - | 620 | - | 6000 | - | - | - | 14.6[1] |
| Chopper Freq ($kHz$) | 2.5 | 2 | 0.3 | 20 | 20 | - | 30 | 20 |
| THD (%) @Input (mVpp) | - - | - - | 0.82 5 @70 Hz | 0.08 2 @ - | 0.1 5 @ - | - - | 0.1 4 @ - | 2 2 @100 Hz |
| Area ($mm^2$) | 0.3 | 0.03 | 0.22 | 1.2 | 0.2 | - | 0.25 | 0.186 |
| NEF | 3.9 | 13.7 | 3.4 | 6.15 | 2.4 | 3.8 | 3 | 3.6 |
| PEF ($V$) | 18.2 | 187.7 | 20.1 | 45.4 | 10.4 | 14.4 | 7.5 | 24.2 |
| Gain/Frequency Programmability | No/Yes | No/No | Yes/No | No/No | No/No | No/No | No/Yes | Yes/Yes |

[1]Simulation Results.

## 4.5 Conclusions

This Chapter presented the design of three chopper amplifiers in a $1.8V$ - $0.18\mu m$ CMOS process.

The ChA-0 shows a modular design employing the same core transconductor in the preamplifier and in the output low-pass filter. The structure of the transconductor allows the output demodulator block to be embedded in the output branches of the circuit, which reduces the glitches generated by the chopping technique. However, the increased power consumption is an inconvenient for portable applications. The use of pseudo-resistors allows modifying then gain and cut-off frequency of the ChA-0 through a tuning voltage.

The ChA-1 was implemented using the VGLNP-4 as core preamplifier and the LPF-1. The structure allows achieving high programmable gain, which can be adjusted through the load bootstrapped resistor in the VGLNP-4. The ChA-1 showed low noise with moderate area and power consumption. However, the NEF and PEF values were not as low as expected due to power consumption. Furthermore, the ChA-1 showed the highest distortion due to the use of triode transistors in the output LPF-1.

Finally, the ChA-2 achieved the best efficiency factors, with $NEF = 3.6$ and $PEF = 23.3V$, and with only $14.6\mu V$ input-offset. It also provides programmability for both the gain and cut-off frequency through the bias current of the LPF and the bias currents in the load bootstrapped resistor of the VGLNP-4.

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# Chapter 5

# Conclusions and Future Work

In this final Chapter the conclusions obtained during this Thesis are presented. Also some ideas derived of the results obtained from this Thesis are discussed as future work.

## 5.1 General Conclusions

In this Thesis, the simulation, design and experimental verification of chopper amplifiers in $0.18\mu m$ CMOS standard process has been presented, which are an essential building block in the front-end circuitry for signal conditioning.

First, a novel implementation, based on the bootstrapping technique, of high-value resistors with low power and area consumption, is proposed. The presented configurations, both grounded and floating topologies, are able to provide equivalent resistance values about 40 to 50 times the integrated polysilicon resistor values. Furthermore, the equivalent resistance is adjustable through the bias current of the impedance scaler, so when used as load resistor in a preamplifier, it provides a way of tuning the equivalent gain of the circuit.

Several low noise preamplifiers are proposed in this Thesis. All of them are designed to reduce noise contributions at a topological level, and are based on a voltage-current conversion input stage and a current-voltage output conversion stage, to obtain a well-defined gain. The LNP-0 is based on a flipped-voltage-follower (FVF) transconductor with a polysilicon resistor ($R_S = 1k\Omega$) as degeneration element and another polysilicon resistor ($R_L = 100k\Omega$) as output load, i.e., as current-voltage conversion element. This amplifier is very compact, and shows good linearity. Although it also shows a good

noise-power-bandwidth trade-off, with a noise efficiency factor $NEF = 3.1$, the relatively high power consumption may be a handicap in portable systems. The LNP-1 is based on a folded-cascode configuration with a polysilicon resistor $R_L = 10M\Omega$ as output load to achieve the current-voltage conversion. The LNP-1 is highly linear and shows a noise efficiency factor $NEF = 2.7$, which indicates a good trade-off between noise, power consumption. The VGLNP-1 is also based on a folded-cascode configuration, with the polysilicon resistor at the output replaced by a floating bootstrapped resistor for current-voltage conversion. The floating resistor allows to reduce the area required to achieve high gain, and provides gain tunability. Experimental results show a noise efficiency factor $NEF = 5$, i.e., the proposal exhibits a trade-off between power and area. The VGLNP-2 is based on a super-source-follower with a polysilicon resistor as source degeneration element. Again, the current-voltage conversion is done through a floating bootstrapped resistor at the output. The VGLNP-2 shows low noise and low power consumption, and a noise efficiency factor $NEF = 3.7$. However, the output swing is limited. A modification of proposal VGLNP-2 is the VGLNP-3, which is based on the super-source follower with degeneration source, but the output currents are copied though current mirrors to increase the output resistance. The VGLNP-3 uses the load floating bootstrapped resistor to achieve high gain with moderate power consumption. It shows the lowest noise efficiency factor $NEF = 1.65$. Finally, to complete the low-noise preamplifiers Section, the VGLNP-4 is described. It is based on a complementary NMOS/PMOS input differential pair with source degeneration, which allows doubling the effective transconductance without increasing the bias currents. VGLNP-4 shows the lowest power consumption with high linearity. The preamplifier is compact and presents a good noise-power-bandwidth trade-off with a noise efficiency factor $NEF = 2.6$. These characteristics make it attractive for signal conditioning in portable applications.

The VGLNP-1 and the VGLNP-4 were fabricated and verified experimentally. The VGLNP-1 achieved a tunable gain from $34dB$ to $38dB$, with $100kHz$ bandwidth and $11.8\mu V_{rms}$ input-referred noise, achieving a NEF of 5 and PEF of 45 with moderate power consumption. Finally, the VGLNP-4 presents a tunable gain from $35dB$ up to $42dB$ with $100kHz$ bandwidth and $8.2\mu V_{rms}$ input-referred noise and low power consumption. The efficiency factors are 2.6 and $12.2V$ for noise and power respectively, which shows that it is a suitable topology for low power applications.

Next, several low transconductance amplifiers are proposed for the design of low cut-off frequency filters. The LGmOTA-0 is a flipped voltage-follower transconductor with a pseudo-resistor as degeneration element. The topology achieves low transconductance in the order of units to tens of $nA/V$, but linearity is degraded due to the distortion introduced by the pseudo-resistor. This issue is circumvented in the LGmOTA-1 by applying the bootstrapping technique to reduce the equivalent transconductance. Experimental results show a Gm range from $15nA/V$ to $18.5nA/V$ with $4\mu W$ power consumption and THD lower than $-40dB$ for input voltages up to $340mVpp$. The LGmOTA-2a combines the bootstrapping technique applied to two low-Gm transconductors in parallel with current cancellation at the output, resulting in a tunable low transconductance from $29nA/V$ to $54nA/V$, with $5.2\mu A$ power consumption, a THD lower than $-40dB$ for input voltages up to $380mVpp$, and with only $600nV/\sqrt{Hz}$ input noise at $100Hz$. Finally, the LGmOTA-2b is based on a similar topology without the need for polysilicon resistors. It achieves similar results, with a variable transconductance from $24nA/V$ to $79nA/V$, $5.2\mu W$ power consumption, THD lower than $-40dB$ for input voltages up to $340mVpp$, and with $500nV/\sqrt{Hz}$ input noise at $100Hz$.

The low Gm transconductors were used to implement four different low cut-off frequency LPFs. All of them have the capability to modify both the cut-off frequency and the gain through a given bias current. The LPF-0 is a very compact configuration which provides a variable gain from -1 to $10dB$, and cut-off frequency as low as $1kHz$. However, the linearity is degraded due to the use of pseudo-resistors. The LPF-1, based on the LGmOTA-1, provides a variable gain from 0 to $3dB$, and variable cut-off frequency from $490Hz$ to $7.1kHz$. The dynamic range of this configuration is improved, even though the configuration is still limited by the distortion level, as shown in the experimental results. Finally, both the LPF-2a and LPF-2b show the lowest $\text{FoM}_1$, i.e., the best trade-off between power consumption and dynamic range. The LPF-2a provides a variable gain from 0 to $5dB$, and variable cut-off frequency from $2kHz$ to $18kHz$. The LPF-2b provides a variable gain from 0 to $6dB$, and variable cut-off frequency from $1.6kHz$ to $15kHz$, and shows the lowest $\text{FoM}_2$, i.e., the best trade-off between power consumption, bandwidth, area and dynamic range.

Finally, the three chopper amplifiers implemented using previously designed blocks were presented. First, the ChA-0 was implemented with a modular design, employing the same core transconductor in the preamplifier and in the LPF. The structure of the pream-

plifier makes it possible to use a demodulator block embedded in the output branches of the circuit, which reduces the glitches generated by the chopping technique. The ChA-0 achieves good efficiency factors ($NEF = 4.6$ and $PEF = 38V$.), but the increased power consumption ($84\mu W$) is not suitable for portable applications. The ChA-1 was implemented using a VGLNP-4 as core preamplifier, and the LPF-1. It shows lower power consumption ($31\mu W$) but the input-referred noise is increased ($1\mu V_{rms}$), resulting in similar noise efficiency factors than the LNP-0, with $NEF = 5$ and $PEF = 46.2V$. As for the ChA-2, it used the VGLNP-4 as core preamplifier with the LPF-2a. Experimental results showed the best noise-power trade-off, and therefore the best efficiency factors. It presented an input-referred noise of $0.65\mu V_{rms}$ in an integration bandwidth of $100Hz$ to $1kHz$, and a power consumption of $35\mu W$. The efficiency factors are $NEF = 3.6$ and $PEF = 24.2V$, which makes it an attractive option for signal conditioning in portable applications.

## 5.2 Future Work

In this Thesis, the proposed bootstrapping technique to achieve high resistance or low transconductance has been applied using the simplest topology as voltage amplifiers. In particular, source followers are used as the main building block. As future work, other buffer configurations can be used instead, leading to novel low-Gm transconductors which may result in even lower transconductance values.

Other research line could be the design of alternative filter topologies by taking advantage of the multiple outputs that can be made easily available in the proposed low-Gm OTAs. In particular, if the output of each source follower in the low-Gm cell is copied to an output branch, OTAs with two differential outputs can be obtained. If this fact is conveniently exploited, it could lead to fully differential filters with compact structures saving power and chip area.

Another line of work to be explored in the future is the design of other chopping amplifier configurations employing the building blocks proposed in this Thesis, in order to further reduce the residual offset. In particular, the nested chopper amplifier is a promising configuration, as it reduces the residual low-frequency noise without increasing circuit complexity and power consumption.

# Appendices

# Appendix A

# Noise Analysis and Simulation

## A.1 Noise Analysis

The input-referred flicker noise of the LNP-0 is given by:

$$\begin{aligned} V_{n,1/f}^2 = & \frac{2}{C_{ox}f}\left[\frac{K_p}{(WL)_1} + g_{m5}^2 R_S^2\left[\frac{K_p}{(WL)_5} + \frac{K_p}{(WL_7)}\right]\right] \\ & + \frac{2}{C_{ox}f}\cdot\frac{g_{mB2}^2(1+g_{m1}R_S)^2}{g_{m1}^2}\cdot\frac{K_n}{(WL)_{B2}} \\ & + \frac{2}{C_{ox}f}\cdot\frac{g_{m9}^2}{g_{m7}^2}\cdot g_{m5}^2 R_S^2\cdot\frac{K_n}{(WL)_9} \end{aligned} \tag{A.1.1}$$

where $K_n$ and $K_p$ are technology dependent constants, $C_{ox}$ is the oxide capacitance, $f$ is the frequency, and $g_{mi}$ and $(WL)_i$ are the transconductance and area of transistor $M_i$ respectively. As $R_S$ and $R_L$ are linear polysilicon resistors, they only contribute with thermal noise, which is not taken into account in equation A.1.1. If transistors $M_7 - M_8$ are designed $M$ times wider than $M_5 - M_6$ to provide some gain to the current mirror, their area and transconductance are also $M$ times higher. Therefore, assuming $g_{m1}R_S >> 1$, equation A.1.1 can be rewritten as:

$$\begin{aligned} V_{n,1/f}^2 = & \frac{2\cdot K_p}{C_{ox}f}\left[\frac{1}{(WL)_1} + \frac{g_{m5}^2 R_S^2(1+M)}{M(WL)_5}\right] \\ & + \frac{2\cdot K_n}{C_{ox}f}\left[\frac{g_{mB2}^2 R_S^2}{(WL)_{B2}} + \frac{g_{m9}^2 R_S^2}{M^2(WL)_9}\right] \end{aligned} \tag{A.1.2}$$

The gain $M$ of the current mirror should be chosen higher than 1 to reduce flicker noise. However, there is a trade-off between the reduction in flicker noise and the increase in power consumption due to the increase in the current through the output branches. For this reason, $M = 1.5$ was chosen.

The input-referred noise flicker or the LNP-3 is given by:

$$\begin{aligned} V_{n,1/f}^2 &= \frac{2 \cdot K_p}{C_{ox}(WL)_1 \cdot f} \\ &+ \frac{2 \cdot K_n}{C_{ox}(WL)_2 \cdot f \cdot g_{m2}^2} \cdot \frac{(g_{m5}g_{m1}R_{eq1}R_{eq2}r_{01}r_{o4} + R_{eq1}R_{eq2}r_{o4}g_{m5})^2}{(g_{m5}g_{m1}R_{eq1}r_{o1}r_{o4})^2} \\ &+ \frac{2 \cdot K_p}{C_{ox}(WL)_3 \cdot f \cdot g_{m3}^2} \cdot \frac{(g_{m2}g_{m1}R_{eq1}R_{eq2}r_{o1}r_{o4} + g_{m5}R_{eq1}R_{eq2}r_{o4})^2}{(g_{m5}g_{m1}R_{eq1}r_{o1}r_{o4})^2} \\ &+ \frac{2 \cdot K_n}{C_{ox}(WL)_4 \cdot f \cdot g_{m4}^2} \cdot \frac{(g_{m1}g_{m5}R_{eq1}R_{eq2}r_{o1}r_{o4} + g_{m5}R_{eq1}R_{eq2}r_{o4})^2}{(g_{m5}g_{m1}R_{eq1}r_{o1}r_{o4})^2} \\ &+ \left[\frac{2 \cdot K_n}{C_{ox}(WL)_5 \cdot f \cdot g_{m5}^2} + \frac{2 \cdot K_p}{C_{ox}(WL)_6 \cdot f \cdot g_{m6}^2}\right] \\ &\cdot \left[\frac{(g_{m2}g_{m1}R_{eq1}R_{eq2}r_{o1}r_{o4} + g_{m1}R_{eq1}R_{eq2}r_{o1} + R_{eq1}R_{eq2}r_{o4}g_{m2})^2}{(g_{m5}g_{m1}R_{eq1}r_{o1}r_{o4})^2}\right] \end{aligned} \tag{A.1.3}$$

where $R_{eq1} = r_{o6}||R_L$ and $R_{eq2} = R_S||r_{o3}||r_{o2}$. $K_n$ and $K_p$ are technology dependent constant, $C_{ox}$ is the oxide capacitance, $f$ is the frequency, and $g_{mi}$ and $(WL)_i$ are the transconductance and area of transistor $M_i$ respectively. To reduce flicker noise, it is required to increase the transconductance of transistors $M_1$ and $M_5$, however, increasing $g_{m1}$ and $g_{m5}$ generates an increase in power consumption, so, there is a trade-off between flicker noise and power consumption. The main advantage of the technique is that the impedance scaler does not generate additional flicker noise to the preamplifier, since the noise is determined by the differential input and bias stages.

## A.2 PNoise Simulation

Chopper amplifiers use modulation to reduce the low frequency noise. The modulator is implemented with four MOSFET switches, as shown in Figure 4.3. Noise calculations in conventional simulators (like SPICE) are based on a small-signal linearized model of the circuit at its DC operating point [1]. Because of the linearization, frequency translation of noise due to the switch modulation cannot be directly determined in these

simulations [1]. For example, SPICE can calculate the noise of a circuit based on the DC operating point when $clk1$ and $clk2$ are fixed but can not calculate when it $clk1$ and $clk2$ are constantly changing.

Spectre simulator extends the traditional time-domain algorithms to handle RF simulation. It uses the Newton shooting method to calculate the periodic steady-state (PSS) response of those circuits. The period of chopper amplifier is the time when a modulation switch is opened once an closed once. The first step to simulate a chopper amplifier is to calculate the periodic steady-state (PSS) response of the circuit to determine the periodical operating point. With the PSS analysis, the input of a circuit is biased to a common input voltage with only the chopper clock applied. The chopper clock will help to determine the period of the PSS response of the circuit [2].

The circuit is linearized around the periodic operating point, and the steady-state response of the periodically varying linear circuit is calculated by superimposing the signal that it is driven by a small sinusoidal signal at an arbitrary frequency.

To complete the noise analysis, a type of analysis known as PNOISE is required. Pnoise analysis is similar to conventional noise analysis, except that it includes the effects of frequency conversion. PNOISE analysis is a two-step process, where the PSS is used to calculate the response to a large periodic signal such as a clock. In the second step, which is the actual PNOISE analysis, the resulting noise performance is calculated [3].

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# Appendix B

# Experimental Characterization

In this Appendix the experimental setup used to characterize the designed integrated circuits in this Thesis is presented. The setup equipment used in the laboratory and the way each circuit of the Thesis was connected to be tested are shown.

Figure B.1 shows the Test Bench for experimental measurements of the transconductor (output current). Each current ($I_{B1}$ and $I_{B2}$) was generated via an external potentiometer, and a two signal generator was used to apply the differential input voltage. A transimpedance amplifier, implemented with the general purpose amplifier TL081 and a feedback resistor $R_F = 2.2M\Omega$, was connected to the output of the transconductor in order to convert the output current into an output voltage.

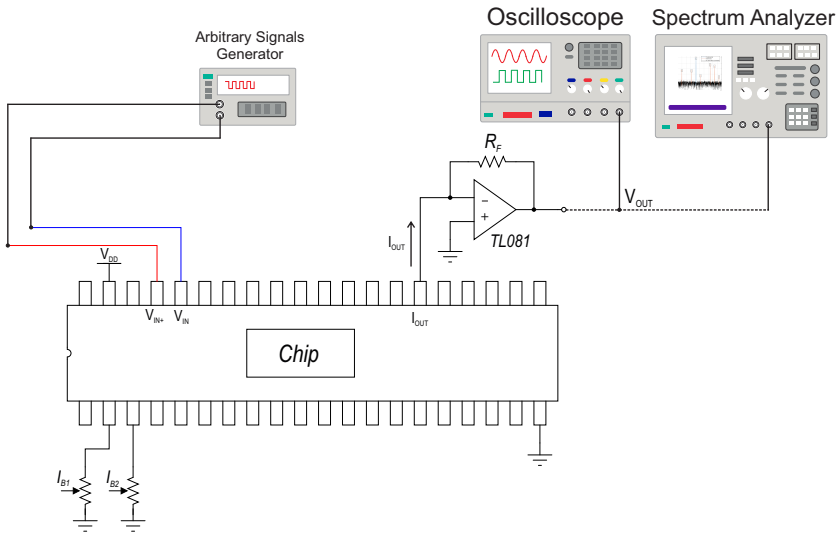


Figure B.1: Setup Experimental to Gm Measure and THD.

The transconductance was measured by applying a $100Hz$ triangle wave to the input from 0 to $V_{DD}$ and obtaining the derivative of the output voltage with respect to the input voltage, $G_m = (1/R_f)(dV_{out}/dV_{id})$, with a digital oscilloscope. Finally, for the THD measurements, they were carried out with the dynamic signal analyzer HP89440A.

Figure B.2 shows the Test bench for experimental characterization of the Variable Gain Low-Noise Preamplifiers. Measurements of the time response was carried out using the Tektronix DPO7104 Digital Phosphor Oscilloscope, whereas for the THD measurements, the signal analyzer Rohde & Schwarz FSV 10Hz-3.6GHz was used.

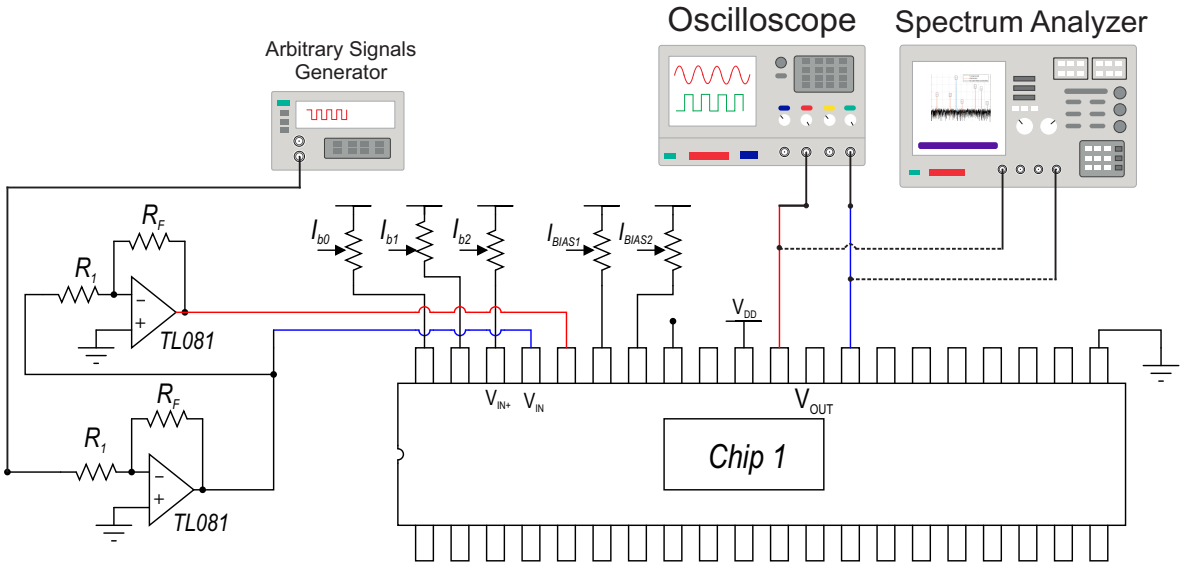


Figure B.2: Setup Experimental for Time Response and THD.

The input signal was applied using a single output signal generator HP33120A. However, it was necessary to convert the input signal $V_{in}$ into a differential signal ($V_{in-}$ and $V_{in+}$) by means of two operational amplifiers, implemented with the general purpose amplifier TL081, connected in an inverter configuration. Resistors $R_1$ an $R_F$ in Figure B.2 were used to attenuate the input signal and avoid saturating the output. The input signal was attenuated with the inverters down to $1mV$. Figure B.3 shows the protoboard used to measure the Variable Gain Low-noise Preamplifiers. Each current was generated via an external potentiometer as shown in Figure B.3. Finally, Figure B.4 shows the complete measurement setup.

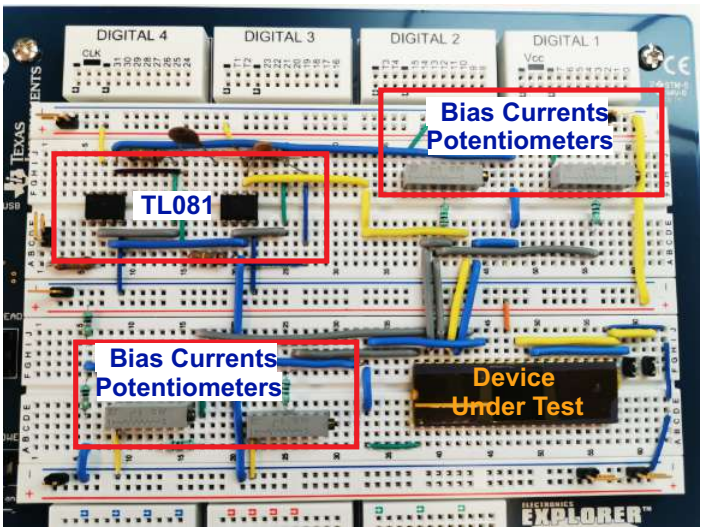


Figure B.3: Photograph of Test Protoboard.

Figure B.4: Photograph of the whole setup.

To analyze the frequency response of the VGLNP, the same protoboard arrange was used. Figure B.5 shows the diagram of the Test bench for experimental measurement of the frequency domain. A Keysight E5061B Network Analyzer was used for this characterization. The equipment was calibrated along with the measuring wires connected to the power splitter. Calibration ensures proper measurement of the frequency response of the device under test (DUT). Resistors were used to attenuate the signal and generate

$V_{in}$. A $V_{in}$ signal of $-30dBm$ was used and attenuated down to $1mV$ amplitude. Figure B.6 shows the complete measurement setup for the frequency response.

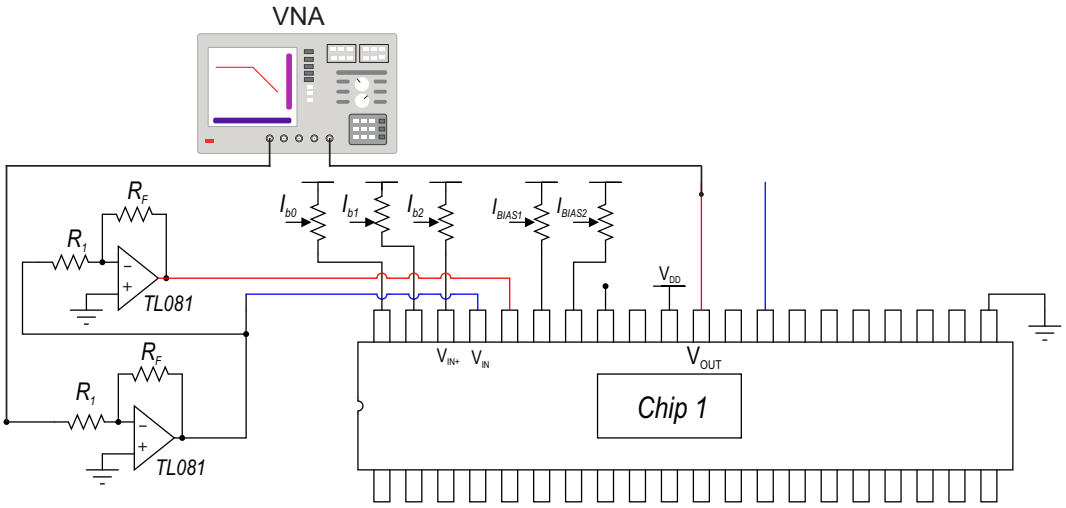


Figure B.5: Setup Experimental for Frequency Response.

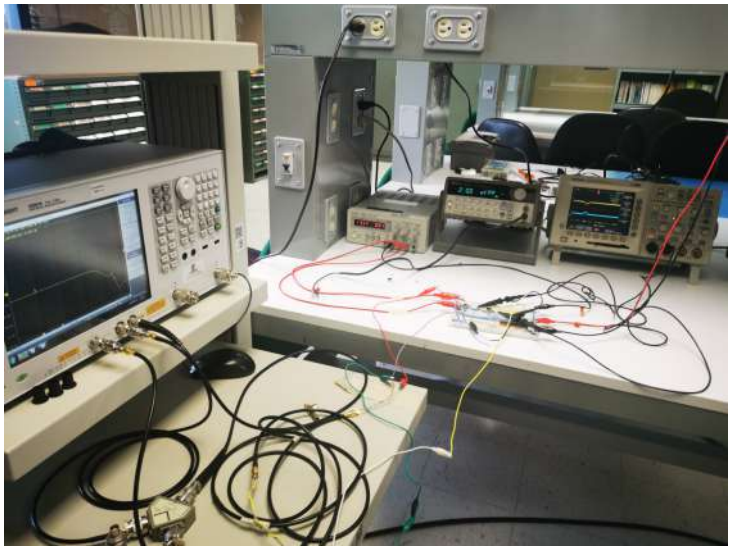

Figure B.6: Photograph of whole setup.

Finally, the experimental noise characterization was carried out using a SR530 Lock-In Amplifier (LIA). Figure B.7 shows the schematic diagram for noise measurements. The LIA provides a voltage mode differential output signal, which is fed directly to the input of the circuit under test. The signal from the sample under test is amplified by an AC-

packed high-gain amplifier. The output of this amplifier is multiplied by the outputs of the internal PLL in two phase-sensitive detectors (PSD1 and PSD2). This multiplication shifts each frequency component of the input signal by the reference frequency [1].

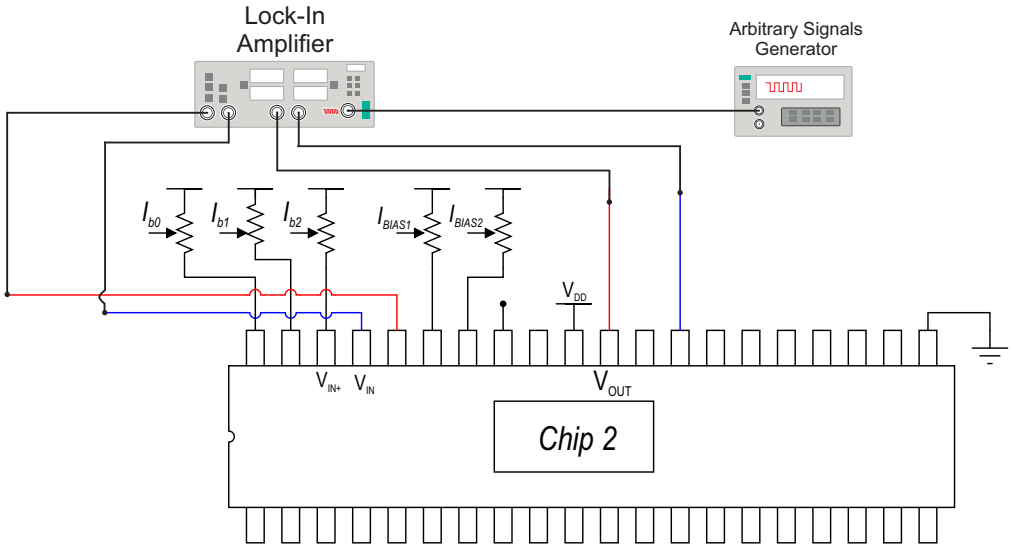


Figure B.7: Setup Experimental for Noise Measurement.

The external signal generator allows defining the frequency at which the power spectral density measurement is taken. Table B.1 shows the main parameters of the LIA. In order to ensure a reliable measurement, three samples from each circuit were measured.

Table B.1: Specifications of the LIA.

| Parameters | Specifications |
|---|---|
| Full-Scale Sensitivity | 100 nV - 5 mV |
| Dynamic Response | High - 60 dB |
| Offset | Off |
| Equivalent-Noise Bandwidth (EnBW) | 1 Hz |
| Active Filters | Bandpass - Line Notch |

The same characterization was carried out for the low-pass filters (LPF) and the chopper amplifiers.

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