VCO Optimization in CMOS Technology Applying Metaheuristics

by

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Resumen

Esta tesis se centra en la optimización del desempeño de dos topologías de osciladores controlados por voltaje (VCOs) en estructura de anillo, mediante el uso de metaheurísticas. Debido a que los objetivos y restricciones de optimización varían de acuerdo a la aplicación en la que el VCO pueda ser usado, se eligió como caso de estudio la optimización de un VCO cuyo propósito es ser adecuado para uso en sistemas de banda ultra amplia (UWB). De acuerdo a las características necesarias para la operación en UWB, se selecciono entonces la maximización de la frecuencia de oscilación como el objetivo a alcanzar, con la restricción de que el VCO opere en el rango de frecuencia de 3.1 a 10.6 GHz, así como que su consumo de potencia y su ruido de fase se encuentre por debajo de los límites establecidos por el diseñador.

Para llevar a cabo la optimización del VCO por medio de metaheurísticas primero es necesario identificar tanto los objetivos como las restricciones que el diseño debe cumplir, así como las variables de este que al ser ajustadas a través del algoritmo brindan la posibilidad de alcanzar el desempeño deseado. Las restricciones pueden estar relacionadas a mantener ciertas características de operación dentro de valores predefinidos como aceptables para cada aplicación en particular, por ejemplo que la frecuencia de oscilación se encuentre por encima de cierto valor o que el consumo de potencia del circuito no sobrepase un valor establecido, por otro lado también es importante considerar aquellas restricciones inherentes al diseño del circuito que son necesarias para que este opere adecuadamente, por ejemplo que ambos transistores en un par diferencial tengan las mismas dimensiones entre sí y que ambos funcionen en determinada región de operación. Una vez identificados todos estos detalles, es necesario adaptar el algoritmo para resolver el problema de optimización especifico que se define a través de los objetivos y restricciones ya identificados.

Como parte del proceso de optimización el algoritmo genera de manera aleatoria un conjunto de valores de las variables de diseño y los sustituye en el circuito, realiza las simulaciones correspondientes y evalúa la función objetivo y las restricciones, este proceso es repetido durante una cantidad definida de iteraciones. Como resultado de este proceso, el algoritmo brinda una solución al problema de optimización que, de acuerdo a lo codificado en este, es la mejor. En este caso de estudio, se evalúa que las soluciones

brindadas por el algoritmo de optimización cumplen con los criterios necesarios para que el VCO sea adecuado para uso en la aplicación establecida y también se evalúa su desempeño en término de otros parámetros como potencia, ruido de fase y a través de una figura de mérito (FoM). Con el propósito de maximizar más allá la frecuencia de oscilación, una de las dos topologías seleccionadas para ser optimizadas inicialmente fue modificada en número de etapas y sometida a optimización de nueva cuenta. Con el objetivo de observar las diferencias en el desempeño de un mismo diseño de VCOs dimensionado a través de metaheurísticas al cambiar el problema de optimización, se agregó un caso de estudio en el que el objetivo consta de la minimización del ruido de fase de las dos topologías de VCO, ambos casos de estudio son comparados y analizados.

Abstract

This thesis focuses on the performance optimization of two ring voltage controlled oscillators (ring VCOs) topologies, through the use of metaheuristics. Since the optimization objectives and constraints vary according to the application in which the VCO is meant to be used, thus the optimization of a VCO whose purpose is to be suitable for use in ultra-wide band (UWB) systems is selected herein as a case study. According to the requirements necessary for UWB operation, the maximization of the oscillation frequency is then selected as the objective, with the restriction that the VCO must operate within the frequency tuning range of 3.1 to 10.6 GHz, as well as that its power consumption and phase noise are below the limits established by the designer.

To carry out the optimization of a VCO through metaheuristics, firstly it is necessary to identify both the objectives and restrictions that the design must meet, as well as the design variables that when adjusted through the algorithm, provide the possibility of achieving the desired performance. The restrictions may be related to maintaining certain characteristics within predefined values that are acceptable for each particular application, i.e. the oscillation frequency having to be above a certain value or the power consumption of the circuit not exceeding a fixed value. On the other hand, it is also important to consider those restrictions inherent to the design of the circuit that are necessary for it to operate properly, i.e. that both transistors in a differential pair have the same dimensions or work in a given operation region, etc. Once all these details are identified, it is necessary to modify the algorithm to solve the specific optimization problem that is defined through the objectives and constraints already identified.

As part of the optimization process, the algorithm randomly generates a set of values of the design variables and replaces them in the circuit, performs the corresponding simulations and evaluates the objective function and the restrictions, this process is repeated for a defined amount of iterations. As a result of this process, the algorithm provides a solution to the optimization problem that, according to what is coded in it, is the best. In this case study, it is evaluated if the solutions provided by the optimization algorithm meet the necessary criteria so that the VCO is suitable for use in the established application and its performance is also be evaluated in terms of other parameters such as power, phase noise and through a figure of merit (FoM). In order to

further maximize oscillation frequency, one of the two topologies that were selected for optimization initially was modified in number of stages and subjected to optimization again. Intending to observe the performance differences that take place among the same VCO designs sized through metaheuristics when changing the optimization problem, a case study is added, in which the objective consists of phase noise minimization of the two VCO topologies, both case studies are compared and analyzed.

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Chapter 1
Introduction

Voltage controlled oscillators (VCOs) are electrical circuits that produce a periodic oscillatory output $V(t)$ whose frequency is proportional to a control voltage V_{ctrl} [10], which tunes the oscillation frequency accordingly to the respective voltage variation. The interval of values among which the oscillation frequency can be set by adjusting the control voltage is called tuning range (TR), and is defined for both frequency and voltage. The block diagram of a VCO is depicted in Fig.1.1. The relation of output frequency to input voltage is given by both the transfer function and the VCO gain (K_{VCO}). The ideal tuning characteristics are depicted in Fig.1.2, ideally there must be a linear relation between the oscillation frequency and the control voltage values through all the tuning range, however in most cases this doesn't occur and the relation f_{osc} vs V_{ctrl} tends to be rather nonlinear. VCOs are commonly employed to perform voltage to frequency conversion. Its implementation in integrated circuits (ICs) began with the use of bipolar junction transistors (BJTs) [11] to later be carried out using CMOS and BiCMOS processes, sometimes reaching higher oscillation frequencies [12].

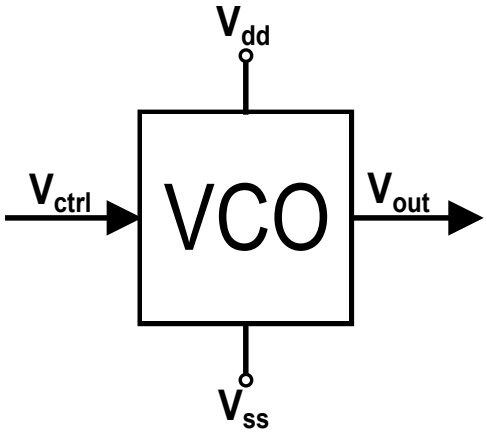


Figure 1.1: VCO block

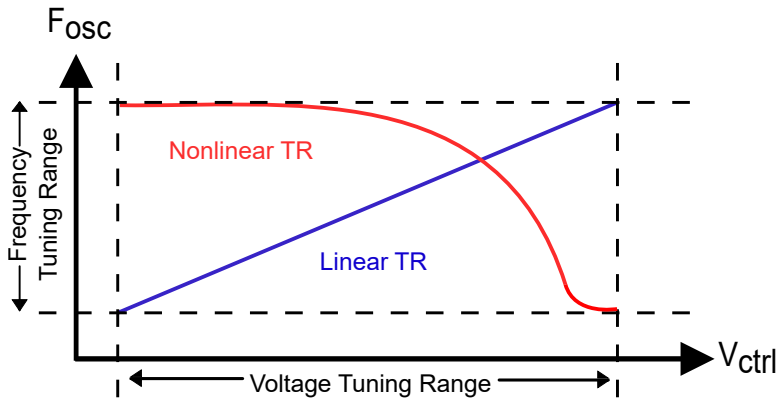


Figure 1.2: Ideal tuning characteristics

For a system to oscillate it must satisfy Barkhausen's criterion, since it is a necessary condition for oscillation to occur, however is not sufficient for the oscillation to take place. Barkhausen's criterion applies to linear circuits with a feedback loop, such as the block diagram depicted in Figure 1.3. It states that, the circuit will sustain steady-state oscillations only at frequencies for which:

- The absolute magnitude of the loop gain equals the unity: $|kH| = 1$.
- The phase shift around the loop is zero or an integer multiple of 2π: $\angle kH = 2\pi n$.

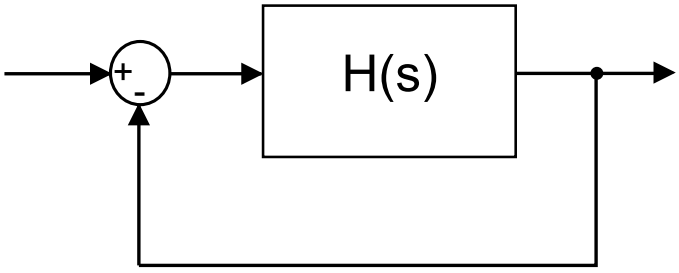


Figure 1.3: Negative feedback system [1]

Where, k is the feedback factor in the circuit and $H(j\omega)$ is the transfer function of the amplifier, so kH is the loop gain around the feedback loop. From the first Barkhausen criterion, the design may be set up to achieve a unity loop gain at the desired oscillation frequency, ω. This is also known as the oscillation startup condition. However, this could set the circuit to be very vulnerable since any circuit variation could produce a gain reduction below 1. Therefore, the loop gain must preferably be set up to be larger than unity [1].

1.1. VCO Classification

VCOs can be implemented through a variety of architectures, some of them are summarized next as well as their main features that can be more or less favorable depending on the application the VCO will be used in. CMOS VCO designs can be classified by their hardware characteristics in LC tanks and ring structures, which in turn can be classified according to the type of signal in the delay stage into: single-ended, differential and pseudo differential.

1.1.1. LC VCOs

LC VCO architectures characteristically are able to tune transistors to operate at higher frequencies than ring VCOs, also are relatively immune to power supply noise [13], and their phase noise (PN) and jitter characteristics are exceptional [14]. However, they usually occupy a much larger area due to its passive elements, suffer from magnetic coupling and require careful calibration to overcome their limited tuning range [5]. Capacitor arrays are often used to extend the tuning range, however its performance is affected due to mismatches in passive devices. There is a trade off between phase noise performance and power consumption [15]. Thus, an approach to achieve phase noise reduction while maintaining a low power consumption is by using multi-objective circuit optimization tools, such as in [16] where the sizing of an LC-tank VCO is performed, however, the frequency TR is quite narrow and due to the trade-off between objectives, the optimization takes several hours.

A differential architecture is more appropriate for implementing LC VCOs, particularly when the aim is to decrease the noise coupling impact. The LC VCO conventional topology is composed by a cross-coupled NMOS differential pair loaded by inductors [17], where the losses of the passive components are compensated through the negative resistance of the cross-coupled transistors to avoid the oscillation from stopping. Transistors T3 and T4 can tune the oscillation frequency through the control voltage variation, which in turn varies its capacitances. By reducing parasitic resistances in both inductors and MOS varactors and performing an adequate transistor sizing, an appropriate phase noise performance can be maintained. The complementary LC VCO topology compensates for losses in the passive devices with both NMOS and PMOS cross-coupled transistors. Owing to the addition of the PMOS transistors the symmetry of the output waveform increases, propitiating a better phase noise performance for a given tail current than that of the topology solely constituted by NMOS.

Compensation of the different features that degrade LC VCO's performance is an important task. A technique to compensate for power supply noise (PSN) in a LC VCO is proposed in [18]. Since varactors offer a positive sensitivity to noise induced by the power supply, placing a reversed connected MOS varactor at the output node could cancel the negative sensitivity to noise induced by the power supply. The noise performance improvement of a LC VCO is proposed in [19]. Table 1.1 shows some of the

most relevant characteristics in LC VCO design. As one can see the best values of PN, power and figure of merit (FoM) are achieved in [16], however this is also the LC VCO with the smallest frequency tuning range. The widest tuning range is reached by [20] while maintaining acceptable power, PN and FoM values. The FoM evaluated in [19] is different from the rest of FoMs reported in table 1.1.

Table 1.1: LC VCO characteristics.

$Work$	$Tech.(nm)$	$Power(mW)$	$PN(\frac{dBc}{Hz})$	$\|FoM\|\ (\frac{dBc}{Hz})$	$Freq.TR(GHz)$	$\|Volt.TR\|\ (V)$	$K_{VCO}(\frac{GHz}{V})$
[16]	130	@P2 0.349	@P2 -119.9	-192.1	2.46 to 2.3	1.1	-
[20]	65	7.4	-107.2 @10MHz	-172.6	54.1	0.4	max=10
[19]	65	1.6	-118.2	184 dB	-	-	0.05
[21]	40	All: 81.8	All: -91.8	-166.75	46.2 to 55.2	1.8	-

1.1.2. Ring VCOs

In VCOs based on single-ended delay cells the signal in the ring is defined with respect to V_{SS} or ground, full rail-to-rail signal swing can be achieved, however they are restricted to be integrated by an odd number of stages for the oscillation to occur. A true differential signal is defined by a differential gate circuit, differential stage based VCOs feature the prospect of a high common mode rejection, leading to both better frequency stability and phase noise, also in this case the number of stages isn't restricted given that both signal's phases are available; by simply inverting a connection the oscillation criteria can be satisfied and an even number of stages can be used. In a pseudo differential cell the signal is defined differentially and the delay cell doesn't have as much common mode rejection as a differential cell. Some important characteristics are [6]:

- Power efficiency: is higher in single-ended delay cells, since the delay stage solely consumes power when a signal transition occurs, unlike differential stages where a bias current is always flowing.
- Jitter: The impact of amplitude coupling in differential circuits is limited due to common mode rejection, whereas in single-ended based VCOs any variation in supply or substrate voltage can lead to jitter, in pseudo differential cells this can be decreased through symmetric layout and good matching. This is not the case for delay modulation where a differential or pseudo differential topology doesn't mean jitter reduction, given that when both paths are affected in the same way the outcome is the same amount of jitter.
- Signal swing: In contrast to single-ended cells, the differential topology requires a smaller signal swing since maintaining all the devices in the active region of operation requires the signal amplitude to be quite lower than the supply voltage. Generally, in pseudo differential cells the signals have a full range swing enhancing jitter performance.

The conventional single-ended delay cell performance isn't as suitable for ultrahigh-speed ICsímplementation due to some of its characteristics, such as its high sensitivity to environmental noise, which in turn results in noise margin reduction and a larger propagation delay [22]. Also its performance isn't enhanced with technology scaling as other CMOS circuits, conventional inverter based VCOs don't accomplish both the speed and power requirements at the same time [23]. In [24] a variation of the conventional single-ended delay cell is used in a technique that inhibits process variations of the center frequency without increasing power consumption through the addition of an extra feedback loop. The delay cell is composed by two cross-coupled NOR gates, this architecture incorporates an extra port that powers down the VCO and through the two cascaded PMOS transistors enhances the output impedance [24]. However, the addition of performance's measures such as phase noise, FoM and VCO'gain could provide a better insight to the VCO's performance.

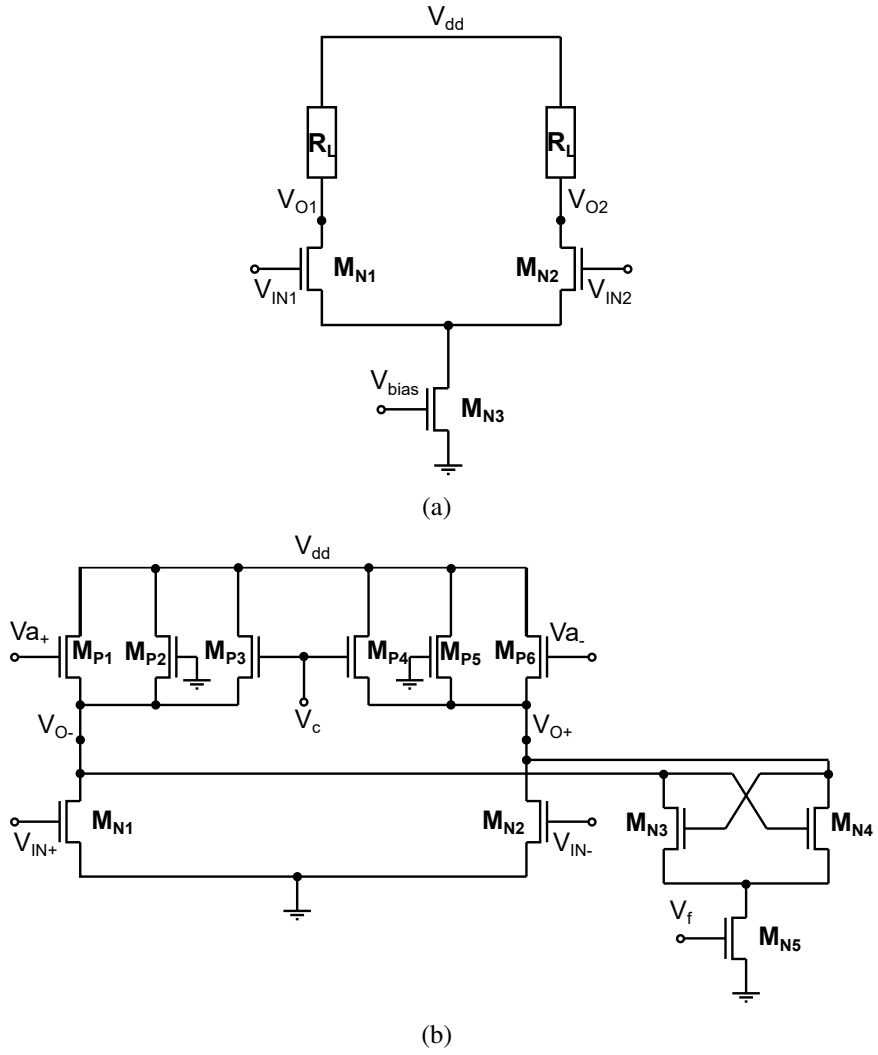
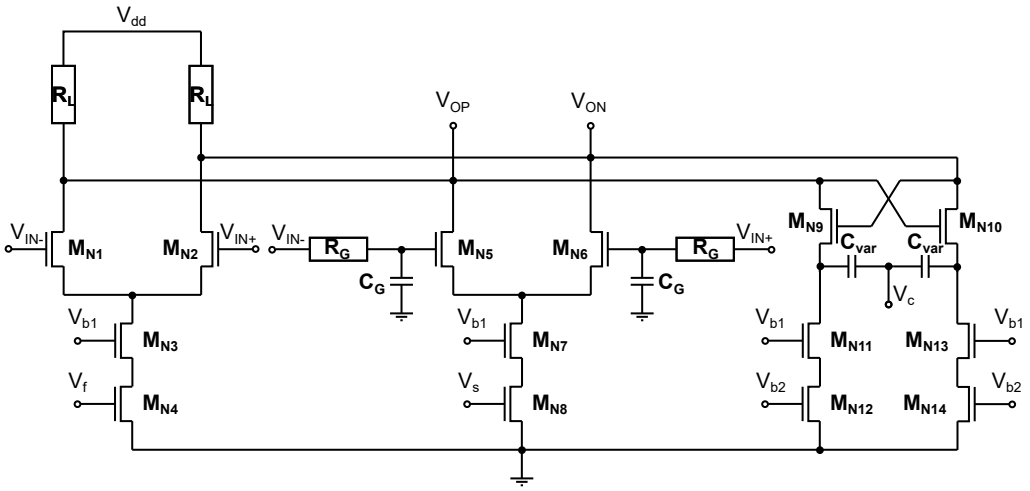
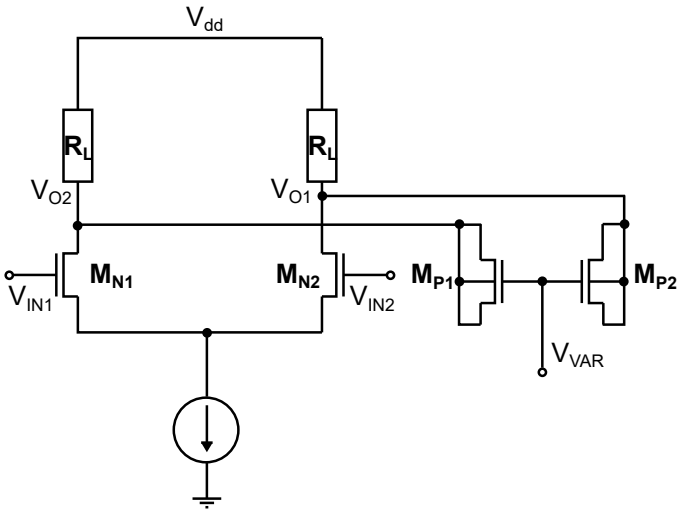


Figure 1.4: (a) Conventional differential delay cell [2], (b) Delay cell for multi-loop RVCO [3].

Fig.1.4 (a) shows a commonly used differential VCO stage architecture. In contrast to CMOS inverters, differential delay cells allow to get symmetrical even-phase outputs and are ideal to achieve higher operating frequencies in low-voltage IC design due to its low output swing voltages. Some of the challenges in designing with a differential topology is to reduce the effect of supply noise and maintain a constant current consumption for farther frequencies [2, 22, 23]. In this conventional topology the load is commonly realized using PMOS transistors operating in triode region. The differential delay cell shown in Fig.1.4 (b) allows to perform coarse and fine frequency control, which leads to both frequency boosting and to a lower tuning gain while avoiding a TR reduction.



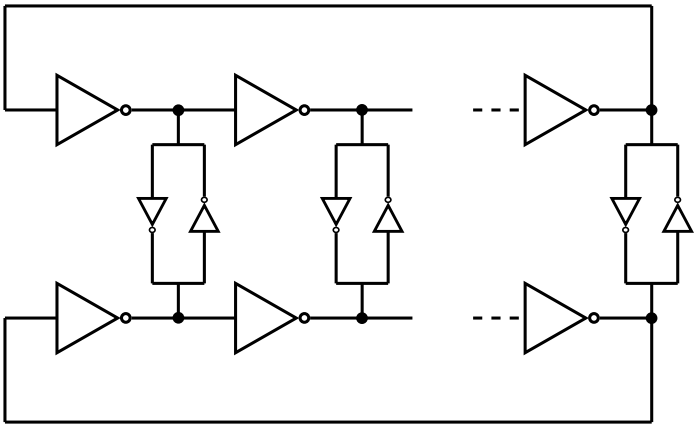
(a)



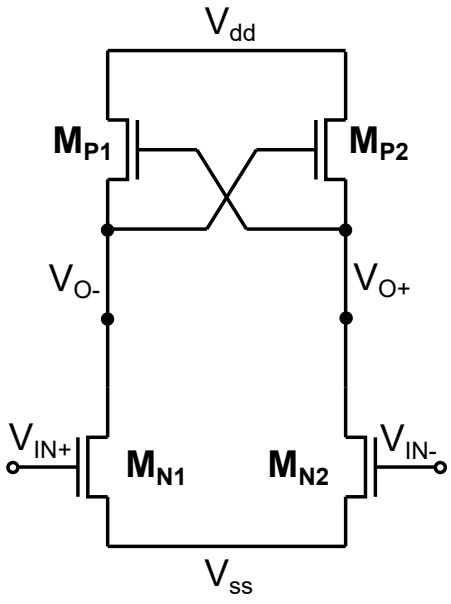
(b)

Figure 1.5: (a) Differential delay cell for K_{VCO} non-linearity compensation [4], (b) Delay cell in differential structure [5].

Whereas the delay cell in Fig.1.5 (a) is designed to compensate for the VCO's gain non-linearity. Similarly, Fig.1.5 (b) shows another variation of a differential delay cell, proposed in [5] to compensate the power supply noise of a ring VCO based PLL. This architecture has a PMOS transistor connected to the output nodes, where its capacitances C_{gs} and C_{gd} are used as varactors and are positively correlated with V_{DD}. When V_{DD} rises, the varactor's capacitance grows leading to a negative supply sensitivity and thus counteracts the conventional topology positive supply sensitivity. Two pseudo-differential topologies are shown in Fig.1.6, in (a) two single ended ring structures are coupled so that they oscillate 180 degrees out of phase. Whereas in (b) the delay cell is integrated of two cross-coupled inverters that are referenced to V_{SS} [6, 25].



(a)



(b)

Figure 1.6: Pseudo-differential ring oscillator [6].

The improvement of the non-linearity of a VCO, is carried out through the single-ended delay cell shown in Fig.1.7, while the real implementation is pseudo-differential. However, this work lacks of phase noise and FoM measurements which are important indicatives of VCO performance.

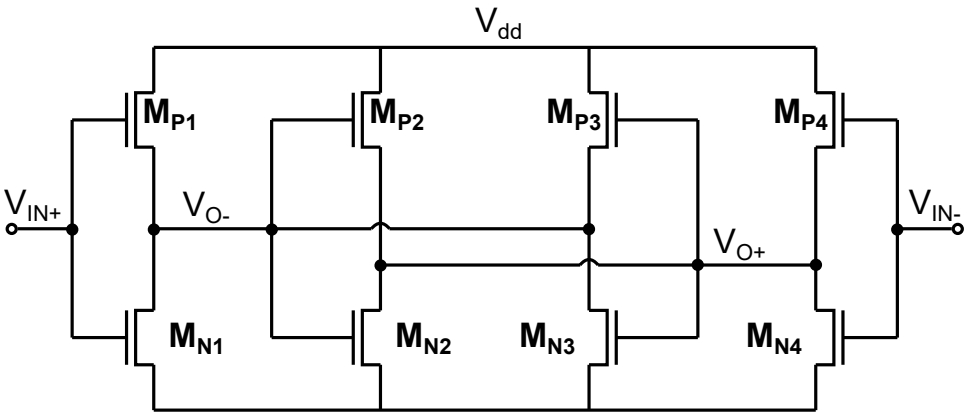


Figure 1.7: Delay cell in pseudo-differential structure [7]

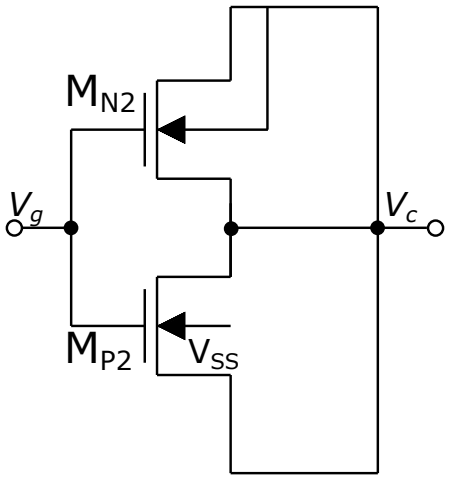


Figure 1.8: Inverter-cap [8]

Similarly, in [8] a ring VCO is implemented using conventional inverters and inverter-caps (shown in Fig.1.8) connected in a pseudo differential architecture to achieve a desirable phase noise performance and high frequency operation, however its TR could be further extended. The gate capacitance of an inverter is denominated inverter-cap, whose value is fixed throughout PVT variations to prevent delay variations, which in turn influence jitter. Inverter-caps are employed as variable capacitors since its capacitance varies in a relatively more linear manner, being also used to adjust the VCO's

frequency. The analog ring VCO implemented in the aforementioned work is part of an all digital phase locked loop architecture (ADPLL). Another pseudo-differential structure is used in [26] to reduce power consumption which is an important feature in VCO based ADCs, for this purpose a current-reuse architecture is used. However, the achieved frequency TR isn't quite wide. Therefore is important to maintain an equilibrium between frequency and power consumption.

Table 4.12 shows some of the most relevant characteristics in ring VCO design. As one can see, the RO in [27] has the best figure of merit, while the lowest phase noise is achieved in [8], on the other hand the smallest power consumption is attained in [28]; moreover the widest frequency TR is accomplished in [29], however is worthy to note that a 45 nm technology is employed in the aforementioned work, whereas the widest TR in 180 nm technology is reached in [4].

Table 1.2: Ring VCO characteristics.

$Work$	$Tech.(nm)$	$Topology$	$Power(mW)$	$PN(\frac{dBc}{Hz})$	$\lvert FoM\rvert\ (\frac{dBc}{Hz})$	$Freq.TR(GHz)$	$\lvert Volt.TR\rvert\ (V)$	$K_{VCO}(\frac{GHz}{V})$
[8]	180	PD	1.06	-138.5	-	1.66 to 1.57	0.4	0.023
[28]	180	SE	0.19	-138	-	1 ± 14 %	-	-
[27]	180	SE	1.2	-106	165.1	0.8 to 1.3	1.1	-
[4]	180	D	28	-92.68	-	1.78 to 2.53	0.2	7 %
[30]	65	PD	20	-90.08	157.34	11 to 2.4	0.65	4.6
[29]	45	SE	0.357	-88.54	-	41.75 to 0.308	0.5	-
[31]	40	D	1.1	-98.05	160.4	0.86 to 1.38	1.1	-
[25]	28	PD	1.1	-95.7	160.7	0.7 to 2.78	-	0.25

1.2. Performances

Some of the main VCOs desirable features are related to achieve: low power consumption, minimal layout area, high frequency capacity, low phase noise, gain linearity over frequency, wide tuning range and robustness to process, voltage and temperature (PVT) variations.

One of the approaches explored to accomplish low power dissipation in a VCO, has been designing with a low supply voltage, nevertheless this compromises the achievable frequency tuning range and the sensitivity to the supply noise. Getting a constant voltage to frequency gain is another of the desirable VCO characteristics, which has been tackled through the use of multiple varactors or voltage to current converters. However, this is at the expense of phase noise performance degeneration, increased design complexity and a raise in power dissipation for the same frequency. Thus, although one can find guidelines to address modern design issues produced by the downscaling of CMOS technologies [32], it is still difficult to achieve the simultaneous enhancement

of two or more performances that's often required for the VCO to optimally operate in a particular application [20, 32–34].

VCOs are commonly used in applications such as analog to digital converters (ADC) [24,26,35–37], PLLs [19,21,38,39], comparators [40,41], among others. Each application has a different set of performances (see table 1.3) that must be enhanced to achieve an appropriate overall operation [4, 30]. Taking this into account, an optimization process requires defining the objective functions in accordance with the given application, and the corresponding design issues must be approached without compromising VCO's desirable characteristics [31].

Table 1.3: VCO characteristics associated to its application in comparators, PLLs, ADCs, etc.

$Work$	$Tech.(nm)$	$Application$	$Power(mW)$	$PN(\frac{dBc}{Hz})$	$Freq.TR(GHz)$	$\|Volt.TR\|\,(V)$	$K_{VCO}(\frac{GHz}{V})$
[40]	350	Comp	0.021	-	0.012 to 0.0000001	2	-
[5]	180	PLL	12.6	-95	1.5 to 2.5	-	1.389
[42]	180	Conv	19.1	-92.25	10.92 to 1.561	1.8	-
[43]	180	ADC	34.5	-88.9	0.4 to 3.49	0.36	-
[44]	90	ADC	-	-130dB	1 to 7.2	0.3	-
[24]	65	ADC	3	-	0.002 to 0.044	-	-
[36]	65	ADC	-	-	0.083 @ 0.6	VDD	$6.4V^{-1}$

The FoM given by (1.1), depends on some of the VCO main features, and is employed to quantify a VCO's performance, where f_{osc} is the oscillation frequency, $L\{f_{offset}\}$ represents the phase noise at an offset frequency f_{offset} and P_{diss} is the power dissipation measured at the oscillation frequency [30].

$$FoM_{dB} = L\{f_{offset}\} - 20log\left(\frac{f_{osc}}{f_{offset}}\right) + 10log\left(\frac{P_{diss}}{1mW}\right) \tag{1.1}$$

1.2.1. Oscillation Frequency

Boosting the achievable VCO's oscillation frequency may seem simple but it requires a good design methodology to achieve it, for example, reducing the number of stages of a ring VCO could be considered to increase the frequency of oscillation. Nonetheless, by reducing the number of stages a higher gain would be required of the delay cell to satisfy the oscillation condition, increasing accordingly the power consumption.

In [3] a multi-loop technique to achieve frequency boosting is applied to a ring VCO, which consists of a primary loop that operates as a regular ring VCO, and a secondary loop that contributes an extra input to the transfer function, reducing the output nodes slew time. The delay cell used for this purpose (Fig.1.4 (b)) allows to perform coarse and fine frequency control, however the power consumption of this oscillator is somewhat higher than other VCOs found in the state of the art.

1.2.2. Tuning Range (TR)

VCO's tuning range is the interval of oscillation frequencies reached through the control voltage changes. The broadening of the linear voltage tuning range is carried out in [31], where the tuning range is effective rail-to-rail. The delay cell proposed in the aforementioned work features added resistors between inputs and outputs to accelerate the output transitions and enhance the phase noise by increasing the current that flows through the load capacitance. The rail-to-rail voltage TR is achieved by means of simultaneously controlling the added elements which are a NMOS transistor in parallel with the tail current source and two PMOS switches connected to a PMOS cross-coupled latch, also through proper sizing of these elements the tuning characteristics can be more linear. However, even though this work manages to maintain a low power consumption, low phase noise and a good FoM while broadening the voltage TR in comparison with the conventional topology, the frequency TR resulting from the implementation of the proposed delay cell isn't as wide as TRs reported in similar works.

According to the desired application, the VCO's TR may need to be widened, e.g., ultra-wide band (UWB) systems operate in the 3.1 to 10.6 GHz frequency range [45]. On the other hand, the requirements of operating frequency and phase noise for Bluetooth applications are 2.4–$2.4835GHz$ and $-81dBc/Hz \quad @1MHz$, respectively [46]. Applications that may need to operate according to the bluetooth standards are receivers, transmitters, transponders and frequency synthesizers, among others. As expected the VCO has to be designed to operate at around 2.4GHz, but alongside this is necessary to consider desirable characteristics, such as phase noise and low power consumption. For example, a differential topology is frequently used for the ring VCO implementation in bluetooth applications due to its superior noise performance [47].

The achievable TR can be restricted by tuning variations that may conduct to common mode voltage deviation and signal fading, which in turn can lead to the oscillation stopping. In [42], the ring VCO's TR extension procedure used in a data converter is focused in the use of an active load consisting of a pair of PMOS current sources connected in parallel to a pair of cross coupled PMOS transistors. The addition of the active elements allows to reduce power consumption at high frequencies besides widening the TR, however this VCO could benefit from reducing the power consumption, which is large in comparison to other works implemented in the same technology, also the evaluation of a FoM could help to quantify the overall VCO's performance. Similarly, the current boosting (CB) technique can be used to approach the enhancement of the ring VCO's tuning range [29], however it leads to a rise in power consumption. The CB technique is carried out by employing extra MOS transistors connected in parallel to the load, these additional transistors are biased to operate in the saturation region at all times. Other works mostly focus on broadening the characteristically narrow tuning range of LC tank VCOs, as it is essential in some applications such as transceivers. The TR broadening, while maintaining an acceptable phase noise, can be achieved by

topologies consisting of switchable decoupled VCO cores [20].

1.2.3. Voltage-frequency transfer function linearity

K_{VCO} is expressed as the ratio of the VCO output frequency to the control voltage and should be intended to have a small variation amongst the tuning range as shown in Fig.1.2 (b), to achieve low jitter, low noise, fast settling time and good stability, among other desirable characteristics. The linearity enhancement of K_{VCO} is important for VCOs in both ring and LC-tank structures. Some techniques that are intended to attain a low K_{VCO} variation accomplish it at the cost of a narrower frequency tuning range or output swing degradation and accordingly the phase noise. This matter is approached in [4] by the introduction of a differential cross-coupled pair, as shown in Fig.1.5 (a), with capacitive degeneration that due to its reversed K_{VCO} non linearity acts as a compensation mechanism and reduces the VCO's gain non linearity without debilitating the phase noise performance, the tuning range, or the output amplitude, however the VCO could be further improved by establishing the power consumption reduction as an objective.

The VCO gain non-linearity is one of the main reasons for performance degradation of VCO based ADCs, since it produces a modulation of the quantization noise's high frequency components to the in-band frequency range. To avoid the effects of non-linearity on the ADC performance, two pseudo-differential VCOs (that diminish even order harmonics and improve PSN) are employed in [7]. Given that there's no difference between the two VCOs, the impact of PVT variations don't affect the ADC performance (Fig.1.7 (a)). Additionally, it has been found that the degradation, product of the VCO nonlinear characteristics considerably decreases through the rising of the number of stages. Frequently applications such as ADCs are affected by the degradation of more than one performance and ADCs aren't the exception, both PN and gain non-linearity can be overcome by the addition of a feedback loop. The compensation of both of these performances, proposed in [36], is carried through a time-varying switched capacitor circuit, where the conversion is carried out through a non-sampling loop with a single bit feedback signal. However, the achieved TR is narrow in comparison to similar works. Comparators are also affected by gain non-linearity, they are a fundamental block in many designs since the comparator precision directly impacts the design's operation. In [40] is proposed a low power, large bandwidth, small area and high speed time domain comparator constituted by two improved linearity VCOs that display a linear low power consumption, however this is achieved at the expense of a reduced frequency TR.

1.2.4. Phase Noise and Jitter

Phase noise is commonly described in the frequency domain. In an ideal oscillator, operating at a given frequency ω, its frequency spectrum is in the form of a pulse.

However, in a real oscillator the energy is distributed within a reduced band around ω since there are both passive and active devices and external noise sources that insert noise into the system. The phase and amplitude of the output is disturbed causing the spectrum to present skirts around the carrier frequency ω [48] (Fig.1.9). Fluctuations in amplitude are mostly attenuated by an amplitude limiting mechanism present in most practical oscillators [49]. On the other hand, fluctuations in the output frequency of the VCOs have a direct impact on the signal to noise ratio (SNR) and time synchronization, in which phase alignment is necessary [9]. The phase noise spectrum is defined by the noise sources present in it, such as resistors and active devices. Other passive devices such as inductors and capacitors produce a filtering action that shapes noise but does not contribute to it [48].

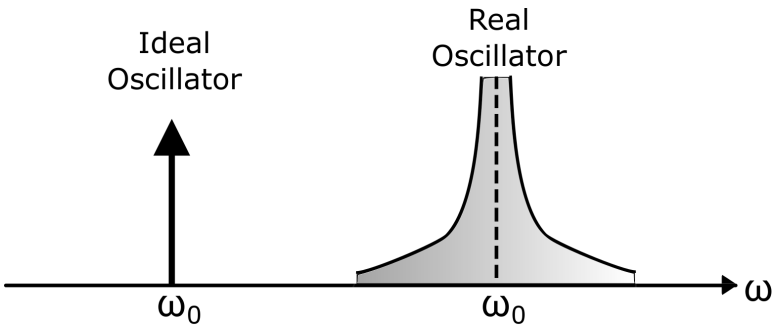


Figure 1.9: Oscillator spectrum [9].

According to [49], a single-ended delay cell with a single current source that supplies a current impulse in one of the nodes causes an instantaneous change in the node's voltage; producing in turn a variation in the transition time. This produces fluctuations in amplitude and phase. Unlike amplitude alterations, phase variations are maintained indefinitely, since subsequent transitions are shifted by the same amount. An impulse sensitivity function that represents the sensitivity at each point of a waveform to an impulse or disturbance is defined. When the impulse occurs during a transition the phase variation is large, on the contrary when the impulse occurs while the output is saturated this has a minimal impact on the oscillator's phase.

Considering a differential stage with passive load, the noise of the tail current source that's close to the oscillation frequency has no influence on PN. However, both low frequency noise and noise that is close to even multiples of the oscillation frequency do affect it. Taking this into consideration, the phase noise and jitter expressions of a CMOS differential ring oscillator are given by (1.2) and (1.3), respectively. Unlike the single-ended RO, the phase noise in the differential oscillator does depend on the number of stages, with PN performance degenerating as N increases for a given frequency and power dissipation. Where η is a proportionality constant whose value is around 1, N is the number of stages, k is the Boltzmann constant, T is the period, P is the to-

tal power dissipation, V_{char} is the device's characteristic voltage, f_o is the oscillation frequency and Δf is a frequency offset.

$$L_{min}\{\Delta f\} = \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right) \cdot \frac{f_o^2}{\Delta f^2} \tag{1.2}$$

$$\kappa_{min} = \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right)}, \tag{1.3}$$

In ring VCOs the enhancement of PN performance while maintaining gain linearity, has been approached through the use of inductive load [50] and dynamic current sources coupled to the input [27], however the former improves PN at the expense of both TR reduction and greater area, while the latter achieves desirable FoM and PN values but the frequency TR can be further widened. Due to its PN features a ring VCO cannot be used in applications that demand high frequency resolution, however phase noise can be diminished through some techniques, such as the sub-sampling loops used in PLLs [39, 51]. Even though LC tank VCOs characteristically have a much lower PN than that present in ring VCOs, some works have focused on further reducing this characteristic through techniques such as body-bias [52] which in turn has the advantage of reduced power consumption. Some other techniques used to reduce PN and power consumption of a quadrature VCO are superharmonic injection and current reuse [33, 53], however the former achieves a reduced TR. Tail filtering technique [15] is used to reduce PN, consists of placing a large inductor between ground and the common source of the differential pair, thus producing a high impedance in series with the differential pair, however this noise filtering produces a drastic increase in the already large area consumed by LC VCOs.

1.2.5. Power Supply Noise (PSN)

The noise induced by the power supply contributes to jitter and can cause frequency variations, this effect in LC VCOs can be compensated through the use of complementary varactors without producing a degradation in PN or an increase in power consumption as been studied in [18], however the TR widening, which is one of the main drawbacks in LC VCO topologies, isn't achieved in this work in contrast to other similar VCOs. On the other hand, ring VCO based ADCs display a high sensitivity to power supply noise, which in turn results in poor ADC performance. Thus, in [35] a technique based in injection locking oscillation is employed to achieve immunity against PSN, however this is at the expense of a narrow TR. Due to the technology scaling-down and its desirable characteristics, ring VCO based PLLs became more relevant; nonetheless switching noise affects its supply rejection performance [38, 51]. A wide bandwidth is required to accomplish low phase noise in a ring VCO based PLL; nevertheless, the PLL reference frequency, its stability and the ripple amplitude on the ring VCO restrict the loop bandwidth [39]. In [5] a ring VCO based supply-insensitive PLL is proposed to

compensate for supply variations through the use of two differential ring VCOs (Fig.1.5 (b)) and an on-chip calibration system, however its phase noise performance which is of great relevance in PLLs could be further improved.

1.2.6. Process, Voltage and Temperature (PVT) Sensitivity

The three main causes of alteration on a circuit's performance are the variations in: the fabrication process, power supply and operation temperature. These constitute PVT variations and their impact is increased with the devices'downscaling [54]. Process variations include wafer defects or may be produced by certain chemical procedures causing some circuit's parameters to change, voltage fluctuations in the circuit take place for a variety of reasons such as supply noise and can be compensated with a voltage regulator to prevent the transistor's operating point from being affected, last but not least temperature variations can be caused by external sources or by the circuit's own power dissipation. PVT variations can be minimized by a proper design as well as through layout placement and routing.

The variation of the VCO center frequency with process causes a detriment in the ADC performance, thus a calibration technique that compensates for process variations with almost no increase in power consumption is proposed in [24] (Fig.1.4 (a)), however a narrow TR is achieved. Similarly, the inaccurate VCO center frequency yield by PVT variations produces a drift in the injection instants which affects the PLL's phase noise. This is approached through an open loop technique for PN canceling, attaining wide-band filtering and PVT stabilization [38]. Time domain comparators also experience issues with PVT variations. Thereby, VCO based closed loop comparators are an alternative, given that the delay difference in each cycle is accumulated during oscillation an improved noise performance and robustness is achieved [41].

1.3. Optimization Algorithms

From the discussion given above and tables 1.1, 1.2 and 1.3, it is noticeable that the simultaneously enhancement of more than one or two VCO performances isn't a trivial task. In addition, and as described in section 1.2, every application hast its own trade-offs and specifications that must be fulfilled for the sake of reaching an optimal operation. Therefore, achieving the optimization of a particular objective additionally to an equilibrium between performances is a matter of interest in IC's design. An option to carry out an appropriately optimized VCO design for a given application that involves multiple specifications and takes into account conflicts among objectives, is the application of metaheuristics.

Mono-objective metaheuristics feature a higher optimization potential since, as its name suggest, they're oriented to the enhancement of one unique objective rather than two or more conflicting objectives. This allows the algorithm to focus its resources in

either maximizing or minimizing the objective itself instead of finding the solutions that best handle a comprise between objectives. Thus, due to its advantages mono-objective algorithms have been widely used as a mean to achieve IC's design and optimization. The mono-objective optimization through DE of a CMOS inverter is carried out in [55], where three different case studies are defined to optimized the switching characteristics of the inverter, these case studies are related to the fall time, the difference between rise and fall times and the symmetry of the inverter's output voltage, also the results given by DE are compared to the designs given by real coded genetic algorithm (RGA) and PSO. Design optimization of analog IC's through both genetic algorithms and PSO is explored in [56], where two case studies are analyzed the first one being a two-stage amplifier and the second is a folded cascode amplifier, the reported tests shown that the best results are given by the combination of the two algorithms. In [57] DE algorithm is used to optimize VLSI routing in an effort to minimize the wire's length, the results are also compared to that obtained through other algorithms such as PSO, artificial bee colony (ABC) and first lookup table estimation (FLUTE), resulting in performance superiority of DE. A variation of DE, named average DE (ADE) that features a different mutation strategy, is used in [58] to optimize the component values of analog filter circuits, which highly affect the circuit's response. Furthermore, a comparison of the results obtained through DE to those of PSO and genetic algorithms for the objective of impedance matching in microstrip antennas is reported in [59], here DE finds the antenna widths and lengths, as well as transmission line position with the aim to reach the expected matching optimization.

On the other hand, multi-objective algorithms can simultaneously optimize two or three conflicting objectives. Thus, they don't have as much optimization capacity as mono-objective algorithms, its performance is better suited to obtain diverse solutions and to improve the trade-offs among objectives, however they generate a variety of solutions. In multi-objective optimization, the optimality of a solution is based on dominance, meaning that the set of optimal results (non dominated or Pareto optimal) is given by the group of feasible solutions that aren't dominated with respect to each other [60]. Two well-known multi-objective optimization algorithms are NSGA-II and MOEA/D. The simultaneous minimization of both phase noise and power consumption through a variety of metaheuristics has been carried out in [28, 43]. In [28] the operation improvement of a ring VCO based on single-ended delay cells is performed through two algorithms, particle swam optimization (PSO) and non-dominated sorting genetic algorithm (NSGA-II), to minimize both the phase noise and power consumption. This is carried out through the use of symbolic modeling techniques to obtain the total output noise density and VCO's phase noise expressions, by doing this the run time is reduced and the noise expression is simplified. Achieving also an improvement in tuning range without being an objective and also performing both Monte Carlo and process corners analyses to the final design. However, given that the widening of the frequency TR isn't an objective, this remains quite narrow, and also no FoM is evaluated. Similarly, in [43] the optimal sizing of a differential ring VCO used as a part of

an ADC, is carried out through multi-objective particle swam optimization (MOPSO) and infeasibility-driven evolutionary algorithm (IDEA) to improve its performances by minimizing both the phase noise and the power consumption while maintaining a given oscillation frequency. Noise modeling is also carried out. To obtain the simplified noise expressions and solve the equations'system, the determinate decision diagram (DDD) symbolic technique is used. Also, Monte Carlo and PVT variations analyses were performed to guarantee the design robustness. Even though a desirable TR value is achieved in the aforementioned work, both the power consumption and phase noise achieved with optimization aren't as low in contrast to similar works, therefore these objectives can be further improved. Also measuring a FoM would provide a better insight in comparing its performance to other similar works.

Mono-objective algorithms use all of its capacity in the enhancement of a particular objective instead of purposing its power for the improvement of multiple objectives; and provide only one solution. To achieve good results with this kind of algorithms the objective function must be properly defined [60]. Some of the mainly used mono-objective algorithms for IC's design optimization are differential evolution and particle swarm optimization.

1.3.1. Differential Evolution

Differential evolution (DE) is a mono-objective algorithm that performs an iterative optimization based on an individuals population's evolution under the concept of competition. Each individual of the initial population, is randomly generated, and constitutes a tentative solution that is associated to a fitness value through an objective function to indicate the individual's suitability to a particular problem. The individuals with better fitness are more likely to be selected as parents, the chosen ones are reproduced using genetic operators such as crossover and mutation, to produce new offsprings, which are also evaluated to determine its survival. This represents a generation and this process is repeated until a stop criteria is met [61,62]. The DE algorithm is suitable for continuous optimization problems, like sizing analog CMOS ICs.

In the DE algorithm a population vector is altered through a vector of differences, which translates to a recombination operator and a self-referential mutation operator that leads the algorithm towards finding suitable solutions. Each individual is encoded as a vector of real numbers that are within the limits given for each design variable. If a variable's magnitude is out of range, the recombination and mutation operators can be used to reset the value. The crossover operator defines the offspring-associated variable to be a a linear combination of three randomly selected individuals or an inheritance of its parents value while guaranteeing that at least one of the offspring's variable will be different from its parent. A scaling factor is employed to prevent stagnation of the search process [61, 63].

Some guidelines to tune the DE algorithm may include to set the population number to ten times the amount of decision variables and initialize the weighting factor, P_f to 0.8 and the crossover constant, P_c to 0.9. If no convergence is achieved an increase in population may be necessary, however frequently the weighting factor is the one that has to be modified to be a little lower or higher than 0.8. The relation between convergence speed and robustness features is a trade-off, if the amount of population increments and the weighting factor decrements then convergence is more likely to occur but within a longer period of time. The DE algorithm's performance is more sensitive to the value of the weighting factor than it is to the value of the crossover constant, and the range of both is generally in [0.5, 1]. A faster convergence may occur with higher values of the crossover constant [61]. If a variable's magnitude is out of range, the recombination and mutation operators can be used to reset the value. For instance, the value can be set to the limit it exceeds, however this comes at the cost of a decrement in the population's diversity. Other approaches reset it to a random value or initialize this value to a mid point between its previous value and the violated bound. In the latter the limits are approached asymptotically leading to a reduction in the amount of disruption [61].

In the process of DE optimization each individual is mutated to generate an adaptive solution v_{ij} from three randomly selected parents, as given in (1.4). Afterwards, the crossover takes place creating a trial solution, through the recombination of a mutated solution v_{ij} with an individual x_{ij}, given by (1.5). Finally, the replacement is carried out employing an elitist selection, where the new individual will replace its parent if its objective function value is better or equal to the parent, as given in (1.6) [61].

$$v_{ij} = x_{r3j} + P_f(x_{r1j} - x_{r2j}) \tag{1.4}$$

$$u_{ij} = \begin{cases} v_{ij} & \text{if} \quad rand_j[0,1] < P_c \quad \text{or} \quad j = j_{rand} \\ x_{ij} & \text{otherwise} \end{cases} \tag{1.5}$$

$$x_i(t+1) = \begin{cases} u_i(t+1) & \text{if} \quad f(u_i(t+1)) \leq f(x_i(t)) \\ x_i(t) & \text{otherwise} \end{cases} \tag{1.6}$$

1.3.2. Particle Swarm Optimization

PSO is another mono-objective metaheuristic, it can be applied to perform high-level synthesis for field-programmable gate array (FPGA) devices, CMOS integrated circuit design [28, 64], analog active filter design, among others. The algorithm is initialized from an arrangement of randomly generated particles within a defined search space, where each of them is described by its position and velocity. Both particles'position and velocity can be represented through mathematical expressions that represent the

best global position and the particle's individual evolution into the best position [65]. The particles'position changes among iterations from an initial velocity vector and its speed is set to different values according to random parameters. Since every particle identifies its best position and is also able to spot whether or not its actual position is the global best, both the particles'position and speed determine if a particle has to be updated [64].

The updating mathematical expressions are given by (1.7) and (1.8), where $p_i(t+1)$ and $v_i(t+1)$ are the particle's position and velocity at the i_{th} iteration, respectively. p_{best} and g_{best} are the particle's best position and best global position, respectively. c_1 and c_2 act as the reliability of the particle in itself and in the swarm, respectively. While r_1 and r_2 are two real randomly generated numbers with a uniform distribution ranging within 0 and 1.

$$v_i(t+1) = v_i(t) + c_1 r_1(p_{best}(t) - p_i(t)) + c_2 r_2(g_{best}(t) - p_i(t)) \tag{1.7}$$

$$p_i(t+1) = p_i(t) + v_i(t+1) \tag{1.8}$$

c_1 and c_2 are very important parameters in the algorithm's performance since they control the equilibrium among exploration and exploration tendencies, meaning that increasing the value of c_1 leads to particles shifting unto their local best experiences while a crescent c_2 value conducts to a quicker convergence to the global best position. Also by setting $c_1 = c_2 = 2$ the particles surpass the goal in a reduced time [65]. Both the selection of the best solutions and randomization are some of the main factors that guarantee global optimality to be reached by a mono-objective metaheuristic. Where the selection of the best solutions ensures that the solution meets an optimum value while the randomization prevents the solution from being stopped at local optima [66]. The constraint handling is performed as follows: if two feasible particles are being compared, the particle with the best cost is chosen, however when only one of the particles is feasible, the feasible is the one to be chosen. Lastly, if neither of the particles are feasible then the particle that fulfills more constraints is selected [64].

1.4. Problem Formulation

VCOs main characteristics are associated to: phase noise, tuning range, power consumption, gain linearity and silicon area, among others. VCOs are commonly used in a variety of applications such as, PLLs, ADCs, DACs, comparators and transmitters, among others. Thus, it is important that their characteristics be optimal for the specific application. In the state of the art there are several delay cells topologies and design techniques that fulfill certain application requirements, however due to the comprises between objectives it's difficult to achieve a better performance of various VCO's features, e.g., phase noise reduction may be achieved but at the cost of both TR reduction

and greater area.

Improving a VCO's performance includes the simultaneous enhancement of features that are in conflict, thus metaheuristics represent a viable option to carry out the design, since they allow to improve a variety of designs just by defining the objective function and restrictions based on the characteristics to be improved for each specific design. Therefore, achieving an optimized design that takes into account all of the features that may affect a specific circuit's operation is still an open problem. For these reasons, this thesis proposes to carry out the design optimization of two VCO topologies through mono-objective optimization, aiming for both VCO designs to be suitable for use in UWB systems, while also having desirable features such as low power consumption and phase noise.

1.5. Objectives

1.5.1. General objective

The objective of this thesis is to carry out the performance optimization of two VCO topologies that aim to be suitable for use in UWB systems, by applying metaheuristics. The desired improvements include: increasing the ranges of both control voltage and tuning frequency, so that the VCO operates within the frequency range designated for UWB systems, improving the phase noise performance and reducing power consumption. A FoM that comprises some of the aforementioned features will be evaluated. At the end, it will be demonstrated the usefulness of applying different metaheuristics to enhance the performances of different VCO designs.

1.5.2. Specific objectives

- Establish the main features to be enhanced (objectives) and the characteristics that are meant to be maintained within an acceptable range of values (restrictions). Identify the available means to improve the required performances to propose an adequate technique.

- Select among the available topologies and techniques the ones that are best suited to carry out the VCOs' performance enhancement.

- Perform mono-objective optimization of the selected topologies.

- Evaluate the VCO performance through FoM evaluations.

1.6. Thesis Organization

This thesis is organized as follows:

Chapter 1 introduces a VCO classification and sub-classification according to its hardware and to the type of signals present in them, respectively. A description of the most important features in VCO performance, and the trade offs among them. Finally, a brief description of some of the most used optimization algorithms is presented.

Chapter 2 focuses on the design of VCOs using a delay cell in single and differential output, and provides a description of the characterization of two case study that will be optimized through metaheuristics in the following chapters.

Chapters 3 consists of the description of the optimization process including specific design considerations to take into account for the sizing of each VCO to be adequate. The description of the algorithms adaptation to the optimization problem is also shown.

Chapter 4 summarizes the results obtained from the VCO optimization through metaheuristics. A case study for a different objective is also presented.

Chapter 5 sums up the conclusions derived from the analysis and characterizations performed on each one of the previous chapters.

Chapter 2
Design Features of CMOS VCOs

Section 2.1 explains the operation principles of ring VCOs, it deepens on the construction of VCOs by the use of two types of delay stages: single-ended and differential. A description of the design process and considerations of both ring VCOs whose performance is to be optimized through mono-objective metaheuristics is displayed next. The characterization of the four-stage differential and six-stage pseudo-differential topologies is provided in 2.2 and 2.3, respectively.

2.1. Design of VCOS Using Delay Cells

As previously stated throughout the previous chapter and in section 1.1, oscillators can be mainly classified in two categories: LC and ring oscillators. In this section the discussion is directed towards the description of both the operation mode as well as the design of ring oscillators.

In the previous chapter was provided a brief description of the Barkhausen criterion, which has to be satisfied for oscillation to occur. Ring oscillatorsóperation can be explained through the negative feedback system depicted in Figure 1.3, which was used to explain the criterion. The oscillating system is represented by the block, it reaches oscillation with no input applied to it due to the delay introduced by what is inside of the block, which in a ring oscillator would be the delay stages. More specifically, if there's enough delay introduced, then the phase shift that the signal undergoes on its path through the loop reaches a point were the feedback signal is amplified instead of being subtracted. This amplification keeps going on when there's enough loop gain until saturation occurs, which in a ring oscillator is also determined by its delay stages. Even though there's no input applied to the oscillator the noise of the devices that form the delay stages and hence the oscillator is what is amplified through the loop allowing for the oscillation to occur [1].

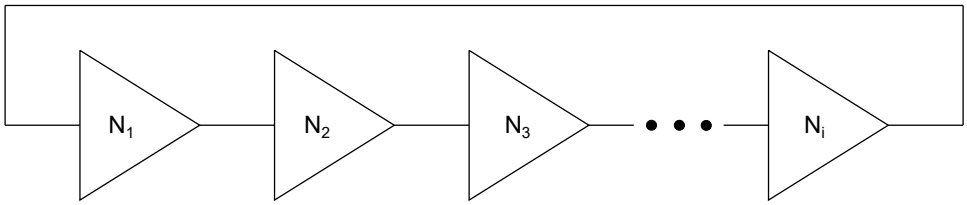


Figure 2.1: Single-ended delay stage VCO block diagram

In ring oscillators constructed with single-ended delay cells the minimum amount of stages N necessary to comply with the aforementioned oscillation requirements is three-stages, through each stage the signal is amplified and inverted reaching the first input with a delay, were the process keeps going. As explained in section 1.1.2 they are limited to be composed of an odd number of stages. Given that they only dispose of a single input/output, if N is even then the output of the last delay stage would be equal to the input of the first one. Figure 2.1 shows the block diagram of a VCO composed by i single-ended stages, were i is odd, it can clearly be seen that the oscillators implemented with this kind of delay stage can only be connected in the form that has been shown. An increase in the amount of stages leads to a frequency reduction since the delay is increased with N this delay is also produced by the impossibility of MOS devices'gate to change states instantaneously since gate capacitance must accumulate charge for I_{DS} to be able to flow [67].

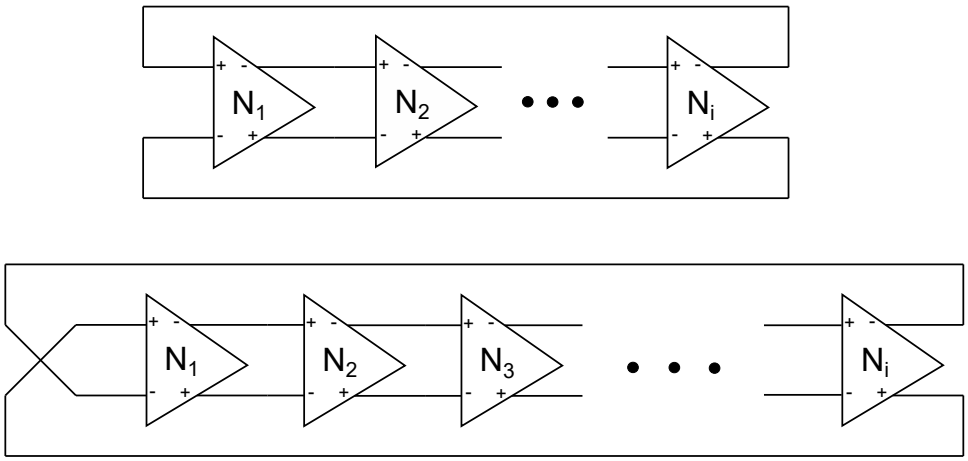


Figure 2.2: Differential delay stage VCO block diagram of: odd (top) and even (bottom) stages

Similarly to that of single-ended stages, in the differential VCOs constructed with an odd number of stages the minimum value of N is three. Whereas in a even-stage VCOs the minimum number of stages is two, however to be able to achieve the required oscillation conditions it would be necessary to guarantee an extra phase shift in each stage, leading to an increment in power consumption [68]. Figure 2.2 depicts the type of connections required for a i stage VCO were i is odd (top) and i is even (bottom). The

same explanation provided for the implementation of VCOs with single-ended delay cells applies for differential oscillators, from Figure 2.2 is evident that if an even-stage VCO was to be connected as one with N odd, the last output wouldn't be inverted in regards of the first input, which wouldn't allow for oscillation to occur. The same can be said for an even-stage VCO, if the change in the feedback connections isn't applied then the output would be the same to the input were is being connected to, instead of being inverted as it should be. The subject of ensuring that the oscillation conditions will be met in circuits with a small number of stages is approached in [69], by making a circuit more instable with the addition of phase degeneration nets and thus aiming to improve its performance.

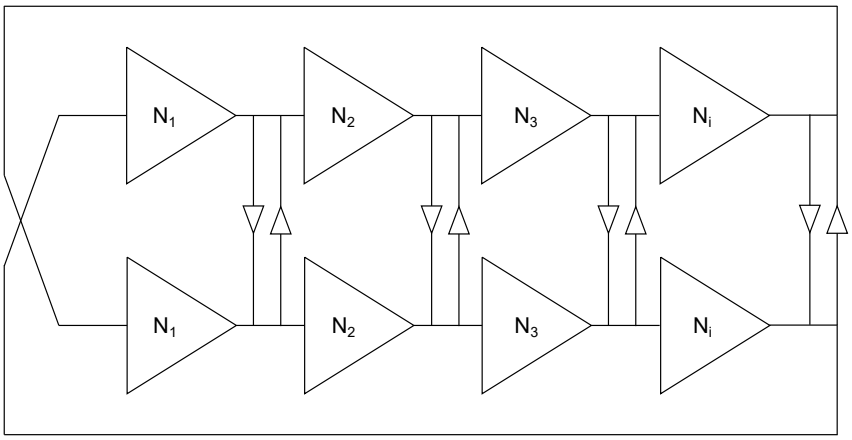


Figure 2.3: Pseudo-Differential VCO block diagram even stages

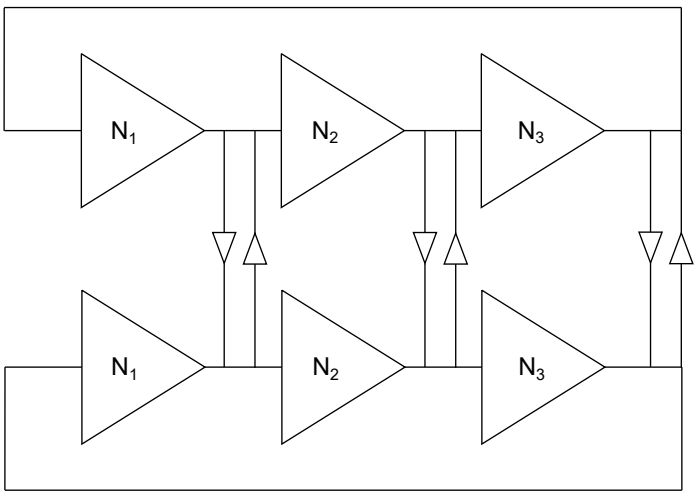


Figure 2.4: Pseudo-Differential VCO block diagram odd stages

Figure 2.3 show an example of a pseudo-differential VCO constructed with an even number of stages, as one can see its stages are single-ended, the pseudo-differential operation is given by the latches connected between the two rings, and given that i is even the feedback connection is inverted to satisfy oscillation conditions. If i were to be odd it will only be required to change the input connections of the first inverter of each ring as in Figure 2.4.

2.2. Four-Stage Differential Ring VCO

2.2.1. VCO Design

Figure 2.5 shows the differential delay stage selected herein to design the four-stage ring VCO.

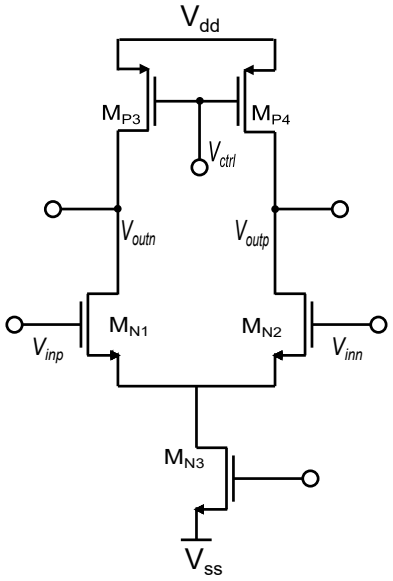


Figure 2.5: Differential delay stage

The topology in Figure 2.5 has been previously employed in [70], [2] and [71] to implement VCOs. In this topology the buffer's load is implemented by PMOS transistors $MP3$ and $MP4$ operating in triode region, where a control voltage variation in $MP3$ and $MP4$ gates produces a variation of the load transistors'resistance. Thus, the oscillation frequency tuning of a VCO using the delay stage in Figure 2.5 can be carried out through the variation of the control voltage V_{ctrl}. PMOS resistance is given by equation (2.1).

$$R_L = \frac{1}{\mu C_{ox}(|V_{ctrl} - V_s| - |V_{th}|)} \tag{2.1}$$

The transistor's sizing of this cell is carried out taking into account that to achieve a good design all the transistors must operate in the saturation region, except for the load transistors which must operate in triode region [2]. To work in saturation region transistors must satisfy equations (2.2) and (2.3); while for triode operation transistors have to met the criteria set by equations (2.3) and (2.5). Other considerations are that to achieve a symmetrical operation the differential pair transistors sizes are equal M_{N1} = M_{N2}, as well as the load transistors M_{P3} = M_{P4}.

$$|V_{DS}| > |V_{GS}| - |V_{TH}| \tag{2.2}$$

$$|V_{GS}| > |V_{TH}| \tag{2.3}$$

$$(\frac{W}{L}) = \frac{2I_D}{\mu_n C_{ox}(|V_{GS}| - |V_{TH}|)^2} \tag{2.4}$$

$$|V_{DS}| < |V_{GS}| - |V_{TH}| \tag{2.5}$$

$$I_D = \mu C_{ox} \frac{W}{L}[(|V_{GS} - V_{TH}|)\,|V_{DS}| - \frac{1}{2}\,|V_{DS}|^2] \tag{2.6}$$

The following dimension ratios are obtained from equation (2.4), $(\frac{W}{L})_{MN1} = (\frac{W}{L})_{MN2} = 339$, $(\frac{W}{L})_{MN3} = 2778$, $(\frac{W}{L})_{Mbn} = 1111$. Proposing $L_{MN1} = L_{MN2} = L_{MN3} = L_{Mbn} = 0.18\mu m$, $W_{MN1} = W_{MN2} = 61\mu m$, $W_{MN3} = 500\mu m$ and $W_{bn} = 200\mu m$, are obtained, the sizing of the bias transistor was carried out with the intention to achieve a tail current of 4mA, with $I_{bias} = 2mA$. For the PMOS load transistors the dimension ratios are obtained through equation (2.6) [72], $(\frac{W}{L})_{MP3} = (\frac{W}{L})_{MP4} = 144$, proposing $L_{MP3} = L_{MP4} = 0.18\mu m$, $W_{MP3} = W_{MP4} = 26\mu m$ are obtained. The load capacitor's value is computed from the HSPICE .lis file, under the consideration of driving one buffer at its output, which resulted in $C_L = 54.7fF$. The sizing is performed using 180 nanometers (nm) from United Microelectronics Corporation (UMC).

As briefly described in section 1.1.2, differential VCO topologies can be integrated by either an odd or an even number of stages, given that the oscillation criteria can be satisfied through inverting the feedback connections. Figure 2.6 exemplifies what was described above with two block diagrams, one represents the necessary connection for a VCO conformed by an odd number of stages to oscillate (for the sake of the example a three-stage VCO is depicted), while the other shows how the feedback connection must be for an even-stage ring VCO (the example depicts a four-stage VCO).

For this case study the VCO number of stages is selected to be four. Thus, the circuit representation of the four-stage ring VCO block diagram depicted in Figure 2.6 (bot-

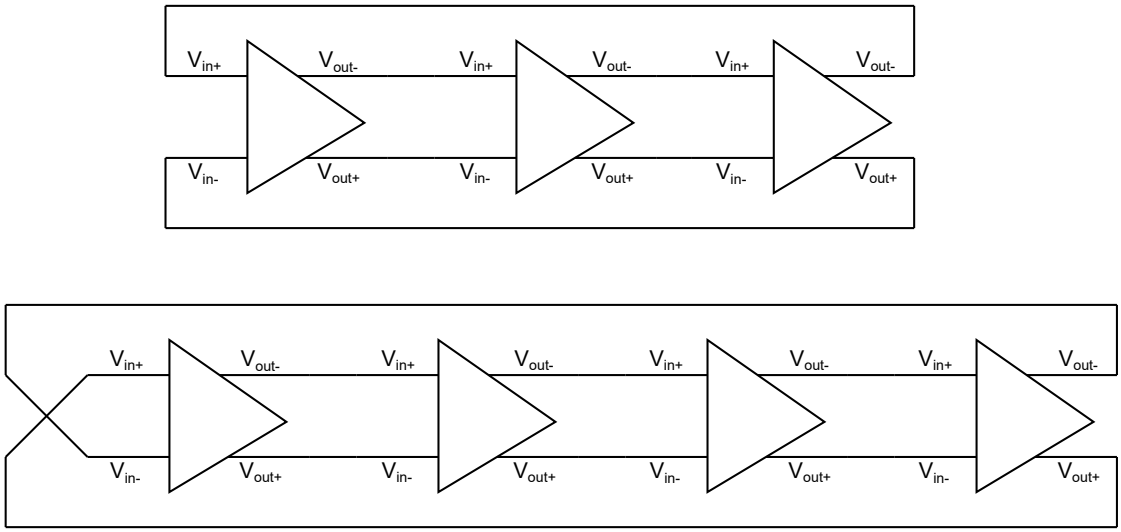


Figure 2.6: Block diagram of three-stage (top) and four-stage(bottom) VCOs

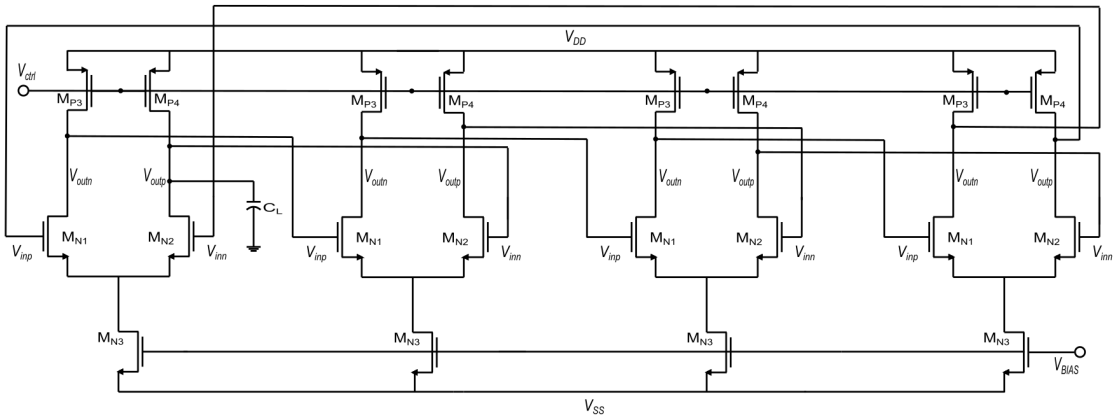


Figure 2.7: Four stage ring VCO.

tom) is shown in Fig.2.7. This VCO is implemented using the CMOS differential stage shown in Figure 2.5. The oscillation frequency, f_{osc}, of a VCO can be evaluated by (2.7), where N represents the number of stages and τ is a time constant which depends on the resistance associated to the active load and the load capacitor. The oscillation frequency varies in a range determined by the control voltage (V_{ctrl}), applied to the M_{P3} and M_{P4} gates and depends on the number of differential CMOS stages [2].

$$f_{osc} = \frac{1}{2N \cdot \tau} \quad where \quad \tau = \frac{C_L R_L}{1 + g_{ds} R_L} \tag{2.7}$$

2.2.2. VCO Characterization

The characterization results of a VCO manually designed based in this topology are reported in [34], which includes the outcome of a symbolic analysis that aims to identify the circuit parameters that influence the most the achievable oscillation frequency, as well as its tuning characteristics, robustness analyses such as PVT, its layout, among others.

The design carried out in section 2.2.1 resulted in oscillation frequencies between 3.08GHz and 5.44GHz, for control voltages between $-0.29V$ and $-0.9V$, respectively. Figure 2.8 depicts the waveform of the 5.44GHz output signal. On the other hand, the VCO tuning range is depicted in Figure 2.9, the data for the tuning range is obtained through the simulation of the VCO for each control voltage value (considering the V_{ctrl} range to be from -0.9 to 0.9 V, in 0.1 V steps), and getting the oscillation frequency value for each of this executions.

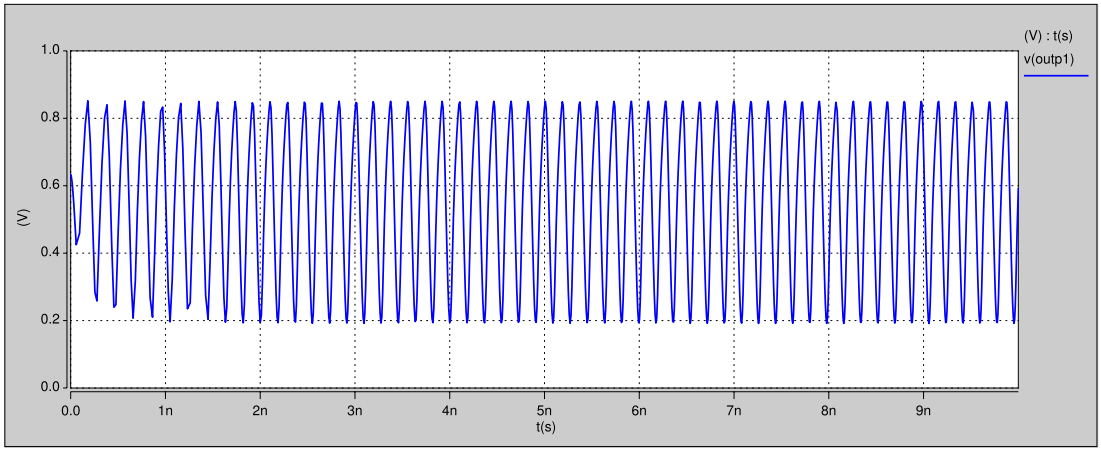


Figure 2.8: Four-stage VCO's output waveform.

The average power consumption of this oscillator is measured at the highest frequency value through HSPICE, resulting in around 41.2 mW. On the other hand, phase noise is measured through the use of HSPICE command .phasenoise, the theory behind how this command works and a deeper insight on the requirements to obatin results through its use are summarized in section 3.4. Phase noise performance results are shown in Fig.2.10, resulting in a phase noise value of -87.89 dBc/Hz @1MHz. Finally, the FoM is easily calculated from equation 1.1, resulting in a magnitude of 146.45 dBc/Hz.

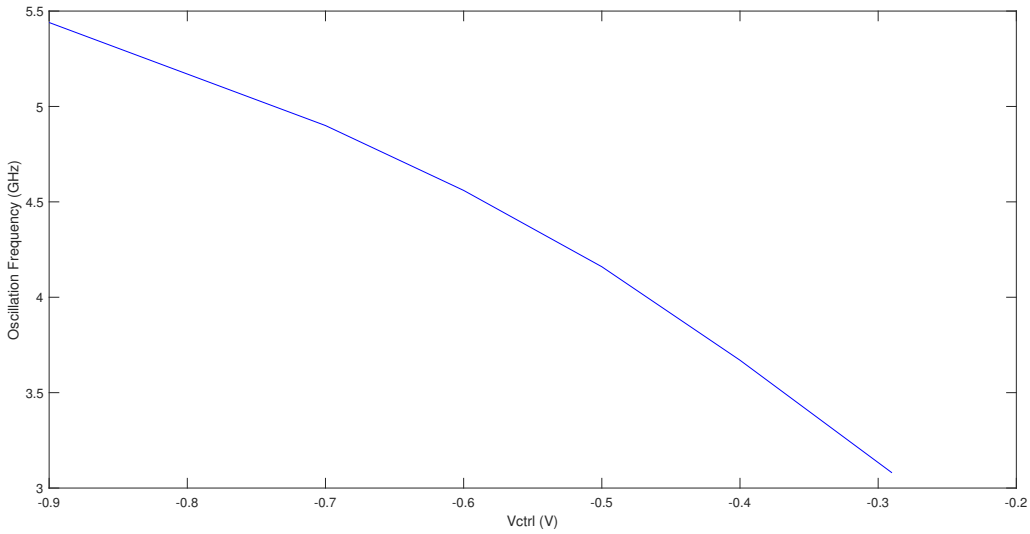


Figure 2.9: Four-stage ring VCO Tunning Characteristics.

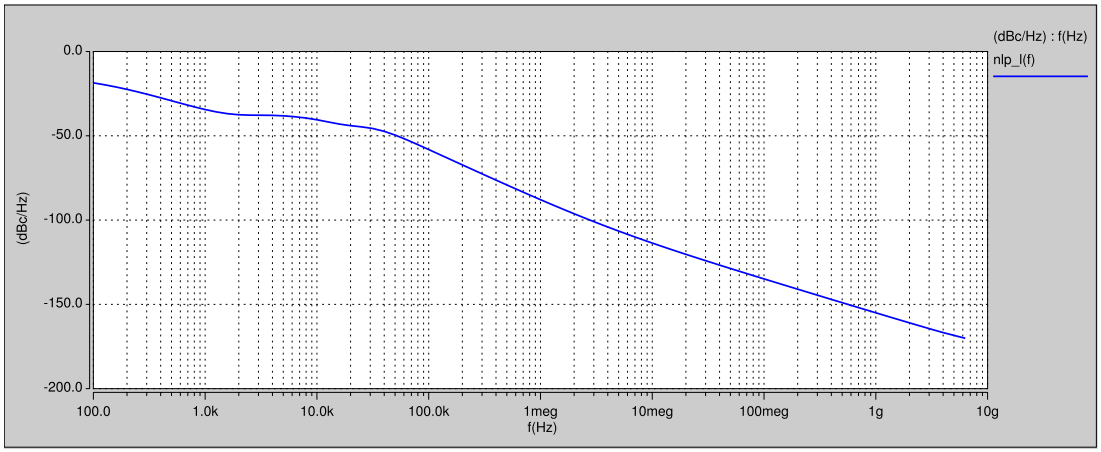


Figure 2.10: Four-stage VCO's phase noise.

2.3. Six-Stage Pseudo-differential Ring VCO

2.3.1. VCO Design

The block diagram of the six-stage ring VCO is shown in Fig.2.11 [8]. The delay stage of this VCO is a single-ended inverter, from section 1.1.2 it is mentioned that ring VCOs implemented with single-ended delay stages can only be constituted by an odd number of stages, however the aforementioned section also alludes to the fact that pseudo-differential structures can be implemented with both odd and even number of stages using single-ended delay stages, which is the case for this VCO. This VCO is implemented with a pseudo differential architecture with the intent of achieving an improved

noise performance. This VCO is composed by eight inverters as the one shown in Fig. 2.12 (b), the inverters from one through six, are used as delay stages, while the purpose of the inverters seven and eight is to generate the 180° phase difference required for oscillation. As one can see inverters one through three and four through six are each connected as a single-ended three-stage oscillator, whereas inverters seven and eight achieve a coupling between these two blocks to produce the pseudo-differential operation. The tuning of the oscillation frequency is carried out through the four inverter caps located in between rings, the inverter cap topology is shown in Figure 2.12 (a). Inverter caps are used to adjust the VCO's oscillation frequency by tuning the variable capacitance of the inverter's gate through V_{ctrl} variation.

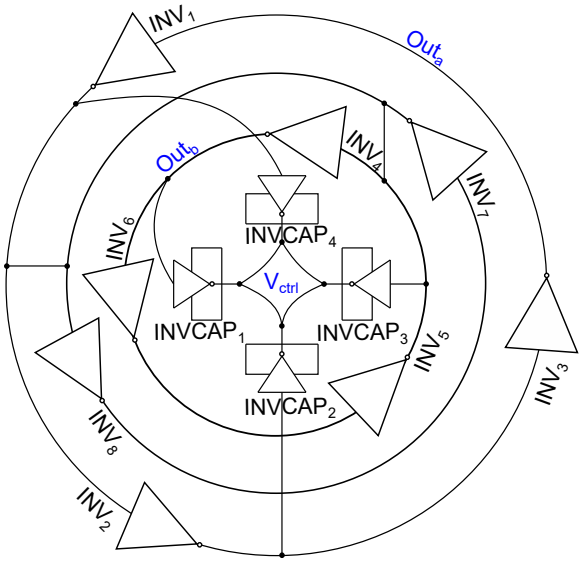


Figure 2.11: Six-stage VCO block diagram.

Inverter caps display a more desirable jitter performance in regards to MOS capacitors, since the former keep a fixed capacitance value through PVT variations [8], whereas deviations on PVT highly impact the operation of the latter. On the other hand, the enhancement in Inverter cap's noise performance is due to the highly linear relation between total capacitance variation and control voltage that features, when comparing it to the relation between variable capacitance and V_{ctrl} of MOS capacitors. This high linearity in capacitance variation is a consequence of its construction, given that the inverter cap's total capacitance is defined by both the NMOS and PMOS transistors in the inverter, M_{N1} and M_{P1}, respectively. Thus, the combination of the two transistor's contributions results in an enhanced linearity in the capacitance change for the same variation in V_{ctrl} [73].

The transistor's sizing of this cell is carried out taking into account that to achieve a good design both of the devices that are part of the inverter, M_{N1} and M_{P1}, have to

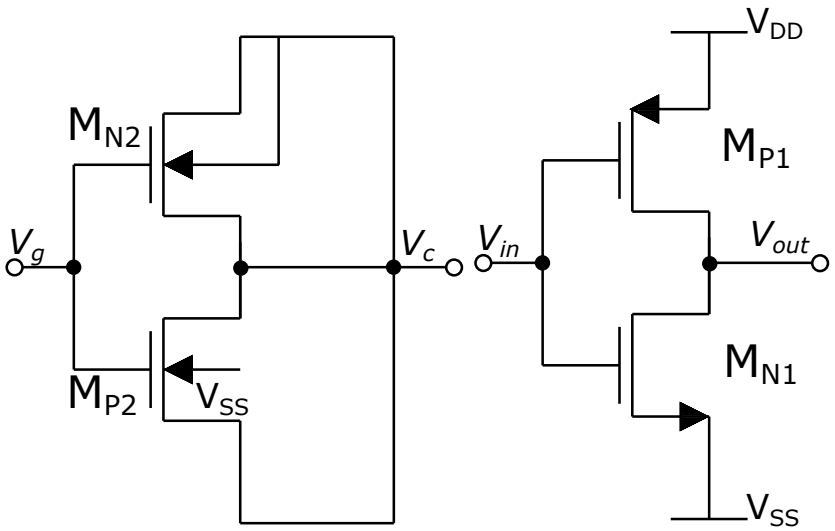


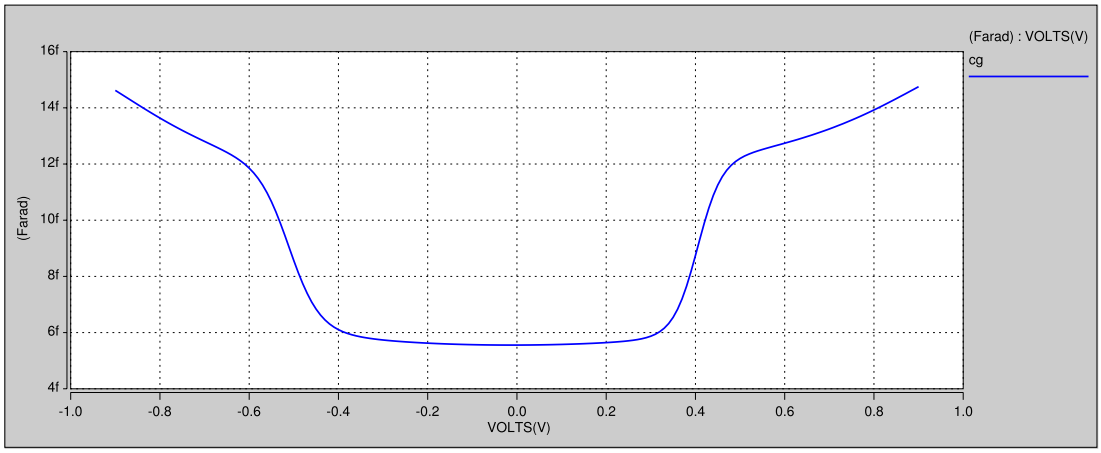
Figure 2.12: (a) Inverter cap (b) Inverter.

operate in the saturation region. Meaning that to work in saturation region transistors must satisfy the relations in equations (2.2) and (2.3).Some consideration to take into account is that for an adequate inverter cap sizing, the widhts and lenghts of both of its devices, M_{N2} and M_{P2}, must be equal: $W_{MN2} = W_{MP2} = L_{MN2} = L_{MP2}$.

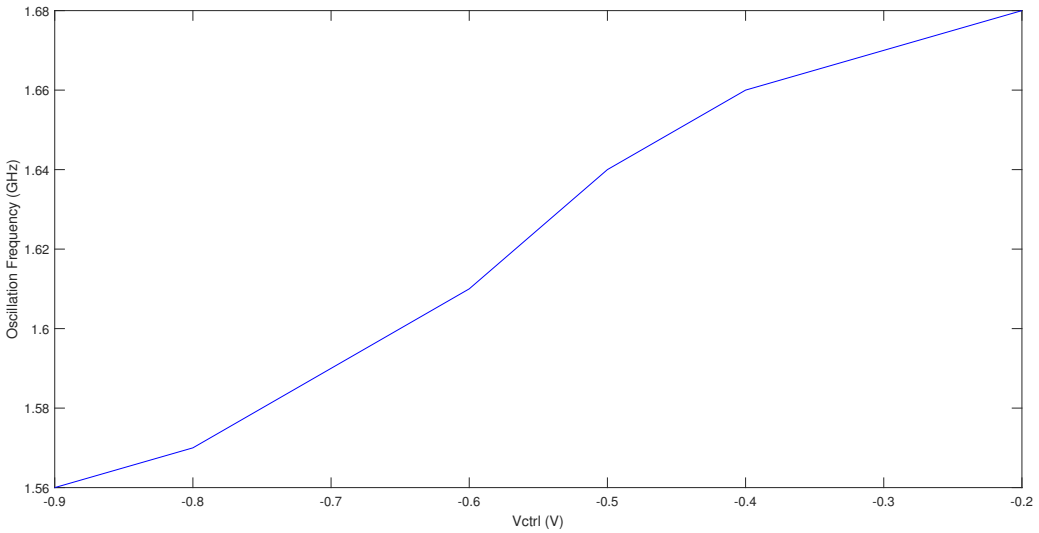
Taking this into consideration a manually sized preliminary design was carried out, the following dimension ratios are obtained from equation (2.4), $(\frac{W}{L})_{MN1}) = 35$ $(\frac{W}{L})_{MP1}) = 87$, $(\frac{W}{L})_{MP2}) = (\frac{W}{L})_{MN2}) = 1$. Proposing $L_{MN1} = L_{MP1} = 0.27\mu m$ and $L_{MN2} = L_{MP2} = 2.7\mu m$, then $W_{MN1} = 9.45\mu m$, $W_{MP1} = 23.4\mu m$ and $W_{MN2} = W_{MP2} = 2.7\mu m$, are obtained. The sizing is performed using 180 nanometers (nm) from United Microelectronics Corporation (UMC).

2.3.2. VCO Characterization

The characterization results of the design developed in 2.3.1, are described herein. In regards to the tuning range, the process followed to obtain the tuning characteristics of this VCO is exactly the same described in the previous section for the four-stage oscillator. However in this case, the control voltage variation produces a change in the inverter caps'capacitance which in turn is traduced to the variation of the oscillation frequency, which differs from the mechanism followed in the four-stage VCO where V_{ctrl} variation produce an alteration in the resistance of the active load transistors. Fig. 2.13 (a) shows the capacitance offered by the inverter cap circuit through V_{gc} variation.



(a)



(b)

Figure 2.13: Six-Stage VCO (a) Capacitance vs V_g (b) Tunning Characteristics.

This six-stage oscillator resulted in oscillation frequencies between 1.68GHz and 1.56GHz, for control voltages between $-0.2V$ and $-0.9V$, respectively. As one can see from the tuning characteristics depicted in Figure 2.13 (b), the tuning range of this VCO is quite narrower than the TR obtained with the four-stage VCO design. The VCO's output waveform is shown in Figure2.14, oscillating at 1.68GHz with a -0.2V control voltage.

The average power consumption for this oscillator is measured with HSPICE, being around 11.34 mW at its highest frequency which is lower than what is obtained for the four-stage VCO. Furthermore, as described in section 2.2 phase noise is measure through HSPICE command .phasenoise. Phase noise results are shown in Fig.2.15,

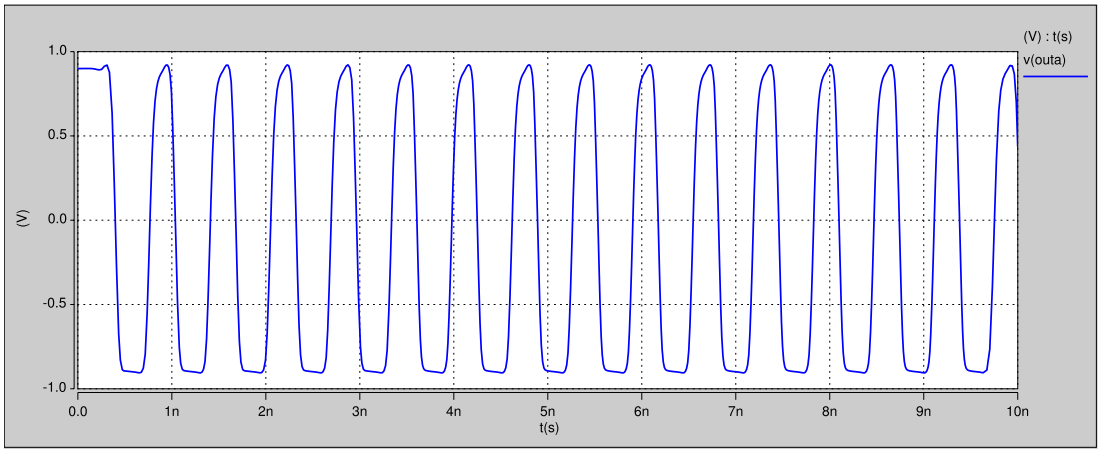


Figure 2.14: Six-stage VCO's output waveform.

where a phase noise value of -93.1dBc/Hz @1MHz is obtained, which is lower than that of the four-stage VCO. FoM is calculated from equation 1.1, which resulted in a magnitude of 147.08 dBc/Hz, which is also greater than that of the four-stage VCO.

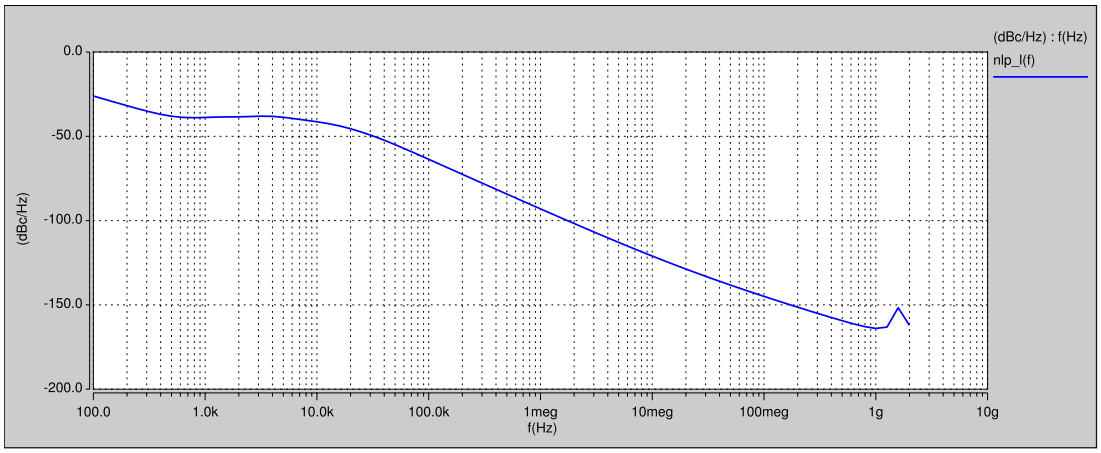


Figure 2.15: Six-stage VCO phase noise.

Chapter 3
Optimization of CMOS VCOs

When designing a VCO a number of considerations must be taken into account to assure the requirements of the particular application will be met, meaning that a VCO used in a PLL will mainly need an enhanced phase noise performance, such as in [38, 39] where sub-sampling and open loop techniques are used for this purpose in ring VCO based PLLs. This may not be the case for ADC implementation which is affected also by power supply noise [35], tunning characteristics non linearity [36] and PVT variations [24] among others [26, 37].

Some of the most common desirable VCO features are low power consumption, minimal layout area, high frequency capacity, low phase noise, gain linearity over frequency, wide tuning range as well as robustness to process voltage and temperature (PVT) variations [34]. The relevance of these characteristics in VCO performance vary amongst applications, therefore VCO optimization can imply a variety of objectives or restrictions combinations according to the application where the VCO will be used making it very useful to use an optimization method that can be easily adapted to specific cases.

For example, among these characteristics phase noise has proven to be a crucial feature in the performance of several circuits that involve VCOs. However, oftentimes there's a trade off between the phase noise minimization and the enhancement of other important features such as power consumption in both ring VCOs [74] and LC VCOs [32, 33] where area is also a concern to take into account [20]. Considering that LC VCOs tend to have a superior phase noise performance than ring VCOs, there has been a lot of effort put towards the analysis and improvement of this feature to obtain results comparable to that of the LC VCOs but using ring structures, adding more to all of its advantages such as its low area requirements [75].

3.1. Optimization Case Study

The objective of this thesis is to optimize the performance of a CMOS VCO intended to be adequate for use in UWB systems. Hence, oscillation frequency is selected herein as the optimization objective aiming for the VCO to operate in the oscillation frequency tuning range necessary for UWB operation.

Ultra-wideband (UWB) systems involve the generation and transmission of large amounts of data over the 3.1 to 10.6 GHz frequency range, as defined by the Federal Communications Commission (FCC). UWB signals must have either a fractional bandwidth larger than $20\,\%$ or a bandwidth of at least 500 MHz, measured at -10dB from its center frequency [45, 76]. The use of this short-range radio communication technology requires high-speed operation, both low power consumption and low noise, besides large tuning faculties [77]. Given that UWB systems operate in a frequency range that is also used by other short-range protocols, UWB signals must be transmitted at a low power, so that when distributed over the large bandwidth the power spectral density is low, which in turn prevents interference with other signals in the same band whose systems operate with higher power values [78].

UWB is also known as Impulse Radio UWB (IR-UWB) since it transmits the data in the frequency range of radio signals throughout a large bandwidth [79]. UWB technology has some inherent advantages over other short-range communication protocols. For example, in UWB communications the data is transmitted as impulses that are non continuous in time. Given that the impulses are very short time signals the bandwidth available is quite wide, this results in low power consumption, and both of this features lead to secure data transmission and reception of the information in UWB systems. Similarly, given its frequency range UWB signals can penetrate objects, walls, etc. Other characteristics related to UWB systems are high data rates and high precision at short distances.

Due to its capabilities UWB is used in communication devices, vehicular radars, ground and object penetrating radars, ,medical tracking and security systems, among others [80]. Ring VCOs are an effective power solution in applications that require an UWB operation, due to both their flexible phase noise requirements and to the possibility of acquiring quadrature signals [81]. A LC VCO that uses variable inductors and switched capacitors to achieve an ultra-wide band operation in proposed in [20], where the compensation of the LC-tank losses is performed through the augmentation of the switching transistors'sizes. Thus, leading to a power dissipation, phase noise and parasitic capacitances increment which in turn limits the achievable oscillation frequency and TR.

3.2. Optimization Method Selection

As widely noted above VCO optimization isn't a trivial task, considering all the information analyzed throughout this work one can imply that besides oscillation frequency, both phase noise and power consumption are also important features that can heavily affect the performance of a circuit that includes a VCO. Fortunately, metaheuristics represent an approach that would allow to maximize oscillation frequency while maintaining some specifications that are in conflict (such as low power consumption, low phase noise, wide control voltage range or reduced silicon area) at desirable values. It is important to mention that the use of metaheuristics for VCO optimization, aims to offer the designer the possibility to redefine the algorithm's objective and constraints to the ones that are relevant to a particular application, without having to implement further design changes.

VCO optimization has been previously carried out through the use of metaheuristics, in [28] PSO and NSGA-II are used to minimize phase noise and both of them consider frequency either as a restriction or as an objective to be maximized, respectively, the mentioned ring VCO's delay stage is an inverter, in this case NSGA-II algorithm obtained slightly better results for phase noise and frequency. Whereas in [82] the phase noise and power consumption optimization of a LC-VCO is performed through the use of electronic design automation (EDA) tools, more specifically a multi-objective heuristics algorithm (MOHA) is used to carry out the optimization. Similarly, in [83] a multi-objective metaheuristic named multi-objective gravitational search algorithm (MOGSA)is introduced to optimize the power consumption and phase noise of an cross-coupled LC-VCO. On the other hand, in [84] the phase noise and power consumption optimization of a LC-VCO is carried out by the use of three metaheuristics, genetic algorithm (GA), PSO and simulated annealing (SA), from the comparison is highlighted that SA shows the most accurate results, however the time of execution is greater, while GA and PSO both result in good design solutions GA has a lower execution time, but PSO represents a better option in terms of the trade-off between the optimization solutions and execution time.

Considering that the objective of achieving such high frequencies for UWB operation is quite defying, and that mono-objective algorithms are suitable for continuous optimization problems, such as the sizing of analog CMOS ICs [28, 64]. Then, mono-objective metaheuristics are selected herein to carry out the VCO optimization aiming to be able to maximize the oscillation frequency to its full potential, this happens due to the fact that this kind of metaheuristics use all of its capacity in the enhancement of a particular objective instead of purposing its power for the improvement of multiple objectives, meaning that such optimization couldn't be reached at such level through the use of multi-objective metaheuristics since the algorithm will have to consider all the objective or objectives simultaneously, interfering with its optimization capacity [85].

Mono-objective algorithms have been widely used in analog integrated circuit optimization. In [86] DE, PSO and variations of them are used to carry out the optimization of switched capacitor biquadratic filters, from the results of the case study presented is concluded that the variants of the PSO algorithm were most suitable for the optimization problem of minimizing the difference between the real and ideal circuit response. Similarly, in [87] the sizing of a buffer chain through PSO and DE and some DE variants is carried out. Some of the parameters checked to determine the algorithms effectiveness are symmetry, power consumption, as well as rise and fall times. From the results, it's concluded that a variation of DE yields the best results. Moreover, in [64] PSO is used for the sizing of two different OTAs, one of them being the RFC-OTA and the other being the Miller. The objective of the OTAsóptimization is to maximize the GBW, while guaranteeing that their DC operation conditions are appropriate through the introduction of a constraint management criteria. On the other hand, in [88] the sizing of three CMOS operational amplifiers is performed by applying mono, multi and many objective optimization; carrying out a comparison an analysis of the results. Some of the parameters considered to measure the op-amp enhancement are power consumption, area, FoM, among others. From the resultsánalysis is remarkable that many-objective metaheuristics gave the best solutions, furthermore it's also remarkable that according to these results mono-objective metaheuristics were more effective than the multi-objective ones for that design problem. In [89] the sizing ot a two-stage operational amplifier is implemented through a variant of PSO which aims to remove the limitations of PSO, named Craziness based PSO (CRPSO) with the aim to minimize the amount of silicon area required by the circuit.

Two of the most widely used mono-objective algorithms are DE and PSO. According to [90] some of the advantages of PSO algorithm are related to its robustness, ease of implementation and tuning, high efficiency, fast convergence, among others, While the main disadvantage is its susceptibility to getting trapped in local minima and premature convergence. On the other hand, [91] resumes quite a lot information of DE, it describes some of the DE advantages such as its ease of implementation, high capacity for solving optimization problems that can be more demanding such as nonlinear ones, among others. Also DE can easily manage large-scale optimization problems, and also its variants have proven to be efficient for optimization. Henceforth, two mono-objective algorithms, DE and PSO, are used herein with the objective to maximize oscillation frequency in a ring VCO [74], which also accounts for trade offs, thus maintaining important features, such as minimum power consumption and low phase noise performance at acceptable values. Thus, resulting in an optimization problem that when solved would satisfy the needs of UWB applications and improve the overall performance of the VCO by tackling other of its important features, while also featuring the ease of adaptation required for VCO optimization.

3.3. Optimization process

The performance optimization of two different ring VCOs is carried out herein with both DE and PSO algorithms. Taking into account the requirements of operation and features described in 2.2 and 2.3, for the four-stage and the six-stage ring VCOs, respectively. Some optimization considerations and results of the four-stage oscillator are summarized in [92] for the DE algorithm, whereas optimization of the six-stage ring VCO are presented in [93] for both the DE and PSO algorithms. As previously established the maximization of oscillation frequency is the optimization objective, herein the frequency range is a part of the optimization process as a constraint as well as the power consumption of the VCO, the VCO's phase noise performance and the operation region of the transistors.

The optimization works by checking whether or not the restrictions are fulfilled, if the value of frequency that's being evaluated is among the range of desired values, then the particle is feasible. Conversely, if the frequency restriction isn't fulfilled, the algorithm establishes that particle as a non feasible one. On the other hand the compliance of the rest of the constraints is also checked by the algorithm and a constraint management is carried out to take them into account in the optimization process. From the information about each VCO's required performance provided throughout this work, the optimization problems are formulated accordingly in 3.3.1 and 3.3.2 for the four-stage and six-stage oscillators, respectively. The adaptation of both algorithms for the defined sizing optimization problem is described in 3.4.

3.3.1. Four-Stage Differential Ring VCO

The sizing optimization problem will search for the sizes of the design variables within the search spaces defined by the designer while taking into account the fulfillment of the defined constraints. The optimization problem of the four-stage ring VCO is defined by (3.2), where the design variables, x, are the dimensions of the differential pair and the load transistors, in this case the control voltage isn't a variable since each VCO design is simulated for every value of the control voltage range (-0.9 to 0.9 V) in steps of 0.1 V. The constraints are given by the operation region in which the transistors must operate, the minimum magnitude of the frequency tuning range as well as the limits the latter must be within, the maximum value of phase noise and the maximum power consumption. Both the bias current and the the polarization transistors (M_{N3} and M_{bn}) sizes were kept at fixed values. For the DE algorithm the objective function $g(x)$ is expressed by (3.1), where μ represents a tunable constant established to one in this case, $r(x)$ stands for the constraints and $f(x)$ equals the oscillation frequency. A flag assigns 0 to a fulfilled constraint and 1 to a non satisfied one, so when all constraints are fulfilled the second term of the function equals 0 and thus the objective function is solely given by the oscillation frequency $g(x) = f(x)$. For the PSO algorithm the objective function is also defined by $g(x) = f(x)$.

$$g(x) = f(x) + \mu \sum r^2(x) \tag{3.1}$$

$$\begin{aligned}
&\text{Search} : x = [W_1, W_3, L_1, L_3] \\
&Maximize : g(x) \\
&\text{Subject to} : 2.5GHz \geq f_{oscmin} \leq f_{min}, \\
&f_{oscmax} \geq f_{max}, \\
&f_{TR} \geq f_{TRmin}, \\
&L\{f_{offset}\} \leq L\{f_{offsetmax}\}, \\
&P_{cons} \leq P_{max}, \\
&V_{DS} \leq V_{GS} - V_{TH} \quad \text{for} \quad M_{P3} \quad \text{and} \quad M_{P4}, \\
&V_{DS} \geq V_{GS} - V_{TH} \quad \text{otherwise}, \\
&W_{min} < W < W_{max}, \\
&L_{min} < L < L_{max}
\end{aligned} \tag{3.2}$$

The values of the oscillation frequency, frequency tuning range, power consumption and phase noise constraints are established as variables f_{min}, f_{max}, f_{TRmin}, P_{max} and $L\{f_{offsetmax}\}$, respectively, since they aren't totally defined. To achieve the operation in the desired range f_{min} and f_{max} are set to 3 GHz and 10.7 GHz, respectively. Whereas the TR, power and phase noise constraints are defined as $f_{TRmin} = 7.5GHz$, $P_{max} = 60mW$ and $L\{f_{offsetmax}\} = -80\frac{dBc}{Hz}$. The constraints related to operation region are to maintain the PMOS load transistors (M_{P3} and M_{P4}) and the remaining NMOS transistors, working in the triode region and in the saturation region, respectively. The limits of the widths and lengths for both oscillators are: $2\lambda \leq W \leq 1000\lambda$ and $2\lambda \leq L \leq 10\lambda$, respectively, where λ= 90 nm. These limits remain unchanged for both algorithms. The V_{BIAS} remains the same from the preliminary design through the results yield by both algorithms for the four-stage VCO.

Next are described some of the considerations that must be taken into account in the optimization of this oscillator both through DE and PSO. It's worth mentioning that contrary to the optimization of this VCOs described in previous works, herein each design is simulated for each control voltage value in the range of -0.9 to 0.9 V, in 0.1 V steps. According to the constraints the operation region of the delay cell must be checked, this is done with a subcircuit of just the delay cell in the same netlist file that the VCO (both have the same design variable values). From this executions the algorithm obtains the operation region of the transistors, oscillation frequency and power consumption values for each V_{ctrl} to get both the voltage and frequency tunning

ranges (it checks if the latter is greater or equal than the constraint), it identifies the maximum and minimum values of the frequency TR and determines if both of those values are within the ranges described above, and locates the center frequency value f_o. Once identified the center frequency it gets the power value that corresponds to it and checks it against its constraint. If the center frequency of the design is greater than 3 GHz, then phase noise simulation is performed, this is done to shorten the execution time by not having to simulate phase noise for each design, just for the ones where it is likely to achieve the desired operation.

3.3.2. Six-Stage Pseudo-Differential Ring VCO

The optimization problem associated with the oscillation frequency optimization of the six-stage ring VCO, is defined by (3.3) for the DE algorithm as in the four-stage ring VCO described previously, thus all the explanation provided above about this topic applies to this oscillator as well. For the PSO algorithm the objective function is also solely defined by the phase noise ($g(x) = f(x)$). Whereas the design variables, x, are constituted by the dimensions of both the inverter (W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}) and the inverter cap (in which case $W_{M2} = W_{MN2} = W_{MP2} = L_{MN2} = L_{MP2}$). The constraints are given by the operation region of the inverter transistors where both of them must be operating in saturation region, the frequency tuning range being at least as wide as defined, the maximum and minimum oscillation frequency values matching spscific values, maximum power consumption and maximum phase noise. As in the previous oscillator, the sizing optimization problem finds the most suitable sizes of the design variables that are within the defined search ranges, considering the restrictions'compliance. The variables'search spaces remain the same for the optimization of both oscillators.

$$
\begin{aligned}
&\text{Search} : x = [W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}, W_{M2}] \\
&Maximize : g(x) \\
&\text{Subject to} : 2.5GHz \geq f_{oscmin} \leq f_{min}, \\
&f_{oscmax} \geq f_{max}, \\
&f_{TR} \geq f_{TRmin}, \\
&L\{f_{offset}\} \leq L\{f_{offsetmax}\}, \\
&P_{cons} \leq P_{max}, \\
&V_{DS} \geq V_{GS} - V_{TH} \quad \text{for} \quad M_{N1} \quad \text{and} \quad M_{P1}, \\
&W_{min} < W < W_{max}, \\
&L_{min} < L < L_{max}
\end{aligned}
\tag{3.3}
$$

3.4. Algorithm Adaptation to the Optimization Problem

Since the optimization problem remains fairly similar for the two oscillators (given that the main difference between the two of them is in the restriction checking part) and that the adaptation of both algorithms is very general, then the pseudo codes for each algorithm is equivalent for both oscillators. The optimization with both DE and PSO algorithms requires to define a population of I_n individuals or particles, a maximum number of generations $maxGen$ and an objective function $g(x)$. The SPICE simulator is linked within the optimization loop to evaluate some delay cell's parameters in both algorithms.

Phase noise measurement is carried out just for the center frequency of each design to avoid slowing down the algorithm run time. Given that some data such as the VCO's oscillation frequency is required to properly set the phase noise simulation, then this step is added as a part of the optimization process after the simulation of the VCO, in an effort to reduce the execution time of the algorithm a condition is added to specify that phase noise simulation will only be carried if the central oscillation frequency is equal or greater than fo_{min} which is set to 3 GHz for the four stage oscillator and to 1GHz for the six-stage VCO. The impact of noise in the oscillator's output is measured in HSPICE RF through ".phasenoiseçommand.

To carry out phase noise measurement of a VCO through this command it is necessary to use the Harmonic Balance (HB) technique in conjunction with it. The latter is called upon with ".HBOSCçommand and it aims to obtain the steady state solutions of the circuit in the frequency domain through a set of finite Fourier series that correspond to the voltage/current waveforms of the oscillator, where the oscillation frequency itself isn't defined and has yet to be determined by the algorithm. HBOSC works without the need of any voltage/current inputs, it does so by formulating the circuit equations in the frequency domain, this formulation is reached by assigning a set of phasor equivalents to the unknown waveforms for a variety of frequency components. The unknown phasors are meant to be found through the application of HB, while satisfying the Kirchoff laws. The circuit components are evaluated either in the frequency or in the time domain, depending on its linearity, thus for non linear components the proceeding is to convert its response to the frequency domain to then be incorporated to that of the linear components'response (that is already on the frequency domain) which produces a final response generated from the combination of both, which complies with voltage/current Kirchoff laws. To start the HB analysis it's required to establish an approximate value of the oscillation frequency, number of harmonics, a pair of oscillating nodes and an estimation of the output waveform's amplitude voltage (it is suggested that this value is set to half of the supply voltage value).

The sizing optimization process to maximize oscillation frequency briefly described above, is adjusted in the Algorithm 3.1 to use DE as the optimization method. For

Algorithm 3.1 DE pseudocode

```
1: procedure DE(I_n, maxGen, g(x))
2:     Generate the SPICE netlist of the ring VCO
3:     for i = 1 : I_n do
4:         for V_ctrl = −0.9 : 0.1 : 0.9 do
5:             Initialize the population randomly and replace the initial individuals (Ws, Ls)
   into the netlist
6:             Evaluate the VCO and check the constraints
7:             Evaluate the objective function
8:         end for
9:         if fo(i) ≥ fo_min then
10:            Simulate the VCO again and evaluate phase noise
11:        end if
12:    end for
13:    while j < maxGen do
14:        for i = 1 : I_n do
15:            for V_ctrl = −0.9 : 0.1 : 0.9 do
16:                Create a trial solution from 3 randomly selected parents using (1.4)
17:                Apply crossover using (1.5)
18:                Replace the new individual into the netlist
19:                Simulate the VCO and count the constraints
20:                Evaluate the objective function
21:            end for
22:            if fo(i) ≥ 3GHz then
23:                Simulate the VCO again and evaluate phase noise
24:            end if
25:            if the individual's objective function is less than that of the parent then
26:                The new individual replaces the parent using (1.6)
27:            end if
28:        end for
29:    end while
30: end procedure
```

DE, the individuals from the randomly generated population are added to the VCO netlist and each one of them is simulated. The SPICE simulator is linked within the optimization loop to evaluate the VCO electrical characteristics. From the output .lis file the electrical characteristics are extracted to monitor the constraint values, if the center oscillation frequency happens to be equal or greater than 3 GHz then the VCO is simulated again with the same individuals, this new simulation features the addition of the necessary commands to execute phase noise simulation to the VCO netlist.

Algorithm 3.2 [64], shows the transformation of the PSO algorithm for the specific optimization problem of maximizing a ring VCO's oscillation frequency, which means that $g(x) = f_{osc}$. Similarly to the process followed with the DE algorithm, with PSO the

particles of the randomly generated population are replaced into the VCO netlist, when the oscillator operates within the maximum and minimum frequency values the solution is considered feasible, whereas if it isn't the solution isn't feasible.The updating mathematical expressions are given by (1.7) and (1.8).

Algorithm 3.2 PSO pseudocode

```
1: procedure PSO(I_n, maxGen)
2:     Generate the SPICE netlist of the ring VCO
3:     for i = 1 : I_n do
4:         for V_ctrl = −0.9 : 0.1 : 0.9 do
5:             Initialize randomly the particles and replace them (Ws, Ls) into the netlist
6:             Evaluate the VCO and check the constraints
7:             Evaluate the objective function
8:         end for
9:         if fo(i) ≥ fo_min then
10:            Simulate the VCO's phase noise
11:        end if
12:        Update the p_best particle considering the constraints and the objective function
13:        Update the g_best particle considering the constraints and the objective function
14:    end for
15:    for j = 1 : maxGen do
16:        for i = 1 : I_n do
17:            for V_ctrl = −0.9 : 0.1 : 0.9 do
18:                Copy particle i to p
19:                Update the particle p velocity using (1.7)
20:                Update the particle p position using (1.8)
21:                Replace the new particles into the netlist
22:                Simulate the VCO and count the constraints
23:                Evaluate the objective function
24:            end for
25:            if fo(i) ≥ 3GHz then
26:                Simulate the VCO's phase noise
27:            end if
28:            Compare particles i and p
29:            Update the p_best particle considering the constraints and the objective function
30:            Update the g_best particle considering the constraints and the objective function
31:        end for
32:    end for
33: end procedure
```

In PSO the constraint management considers that: when two feasible particles are compared, the particle with the lowest phase noise is selected, if only one of the particles is feasible, then the feasible one is chosen. Lastly, when both particles aren't feasible then the particle that complies with more constraints is selected [64].

Chapter 4
Analysis and Discussion of Optimization Results

4.1. Oscillation Frequency Optimization

For oscillation frequency optimization of both the four-stage and three-stage ring VCO, DE algorithm executions are carried out setting the number of individuals I_n and amount of generations max_{gen} to 60 and 30 respectively. For the PSO algorithm a population of 60 individuals and a maximum number of generations of 60 are used.

On the other hand for six-stage VCO optimization, I_n and max_{gen} for DE algorithm are set to 30 and 30 respectively. For PSO a population of 60 individuals and a maximum number of generations of 40 are used. For both of this tests: $PN_{max} = -80dBc/Hz$ and $P_{max} = 60mW$.

4.1.1. Four-Stage Differential Ring VCO

The design variables of each of the 5 best feasible sized solutions are summarized in Table 4.1, for both algorithms. On the other hand, the results of some of the design constraints such as phase noise (PN), frequency tuning range and power of the VCO, as well as some other relevant features as voltage tuning range and FoM, are summarized in Table 4.2. For this purpose, the best solutions are considered to be the ones that are closer to the desired frequency tuning range for UWB operation.

The phase noise simulation results of the non-optimized design (-87.89 dBc/Hz@1MHz) against the best solution given by the DE (-89.05 dBc/Hz@1MHz) and the PSO (-85.18 dBc/Hz@1MHz) algorithms are shown in Figure 4.1. The blue signal depicts the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively.

Table 4.1: Best 5 feasible sized solution design variables.

Solution	$W_{MN1}(\mu m)$		$W_{MP3}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP3}(\mu m)$		$C_L(fF)$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	26.19	12.06	32.58	17.19	0.18	0.18	0.18	0.18	31	14
2	16.56	25.02	24.93	15.39	0.18	0.18	0.18	0.18	20	30
3	8.73	62.46	18.72	31.77	0.18	0.18	0.27	0.18	10	74
4	21.78	58.77	22.59	44.64	0.18	0.18	0.27	0.18	26	70
5	21.78	16.29	32.94	53.46	0.18	0.18	0.27	0.18	26	19

Table 4.2: Best 5 feasible sized solution constraints.

Solution	$Power(mW)$		$Freq.TR(GHz)$		$\|Volt.TR\|\,(V)$		$PN(dBc/Hz@1MHz)$		$\|FoM\|\,(\frac{dBc}{Hz})$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	12.22	28.6	7.9 to 0.047	7.31 to 1.46	0.8	1.3	-89.05	-85.18	148	147.44
2	9.48	31	7.89 to 0.05	6.34 to 0.61	0.8	0.4	-87.17	-87.13	147.88	147.19
3	8.8	40.4	7.64 to 0.05	5.6 to 2.94	1.3	0.7	-85.67	-88.39	149.19	145.69
4	13.4	38.7	7.42 to 0.07	5.4 to 3.13	1.4	0.4	-88.34	-87.37	149.34	143.34
5	11.84	30.3	6.7 to 0.01	7.44 to 6.31	1.2	0.4	-90.1	-85.3	149.58	147.05

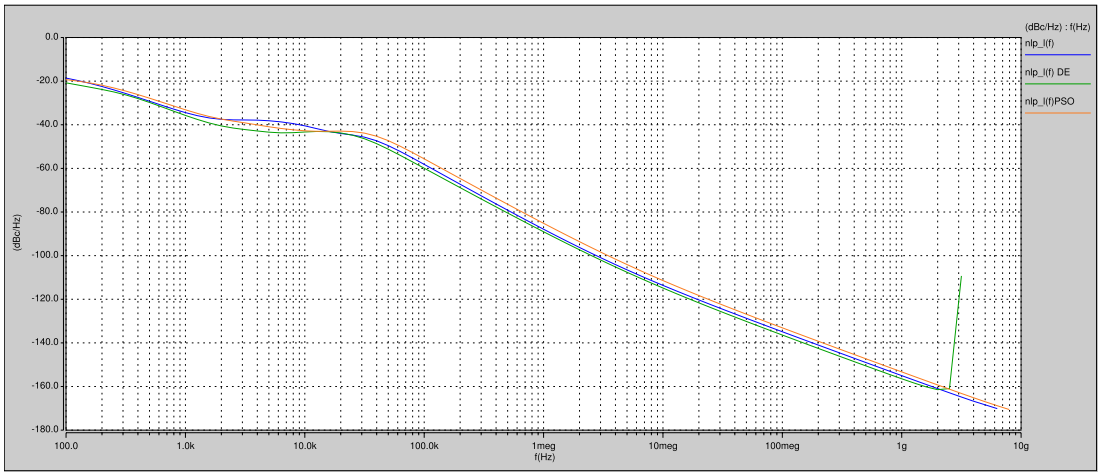


Figure 4.1: Phase noise of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

Figure 4.2 depicts the tuning characteristics of both the original and the two designs optimized for oscillation frequency. The DE optimized design, shows wider tuning ranges (both in frequency and voltage), whereas the design optimized through PSO has

a wider frequency tuning range but a narrower voltage tuning range. From Table 4.1 and Figures 4.1 and 4.2 it is noticeable a slight improvement of 1.16 and increment of 2.74 dBc/Hz@1MHz, in regards to the original design phase noise, for DE and PSO algorithms, respectively.

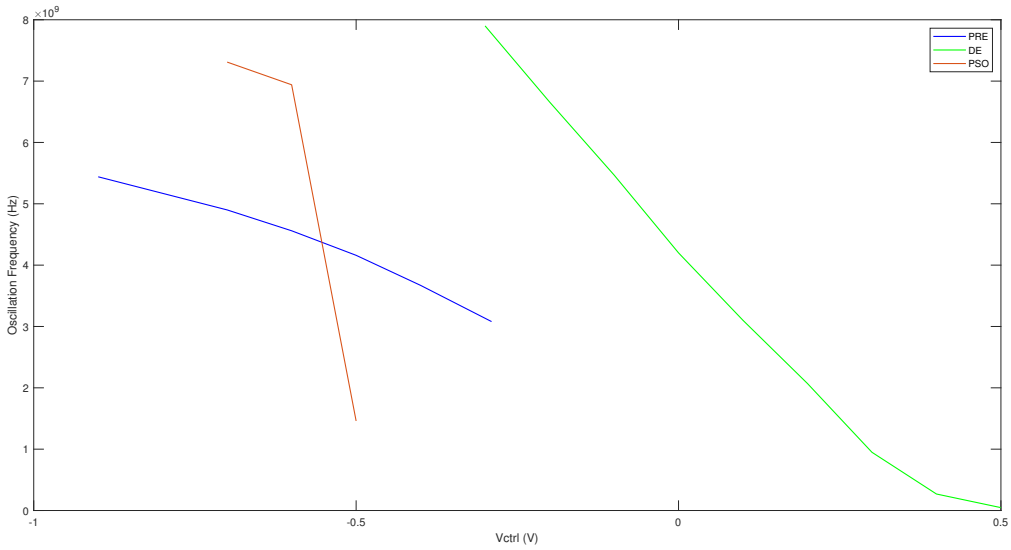


Figure 4.2: Tuning range of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

As one can see none of this designs achieved the desired frequency tuning range to operate in the complete range of UWB systems. Thus, another test will be carried out using the same two algorithms for oscillation frequency optimization but changing the number of stages to three.

Three-Stage Differential Ring VCO

The original four-stage VCO, changes to the three-stage ring VCO topology depicted in Figure 4.3. The inputs of the first stage has to be interchanged as in odd stage VCOs. This change in the SPICE netlist is the only edition required to carry out this tests, the rest of the values are maintained as in the four-stage VCO.

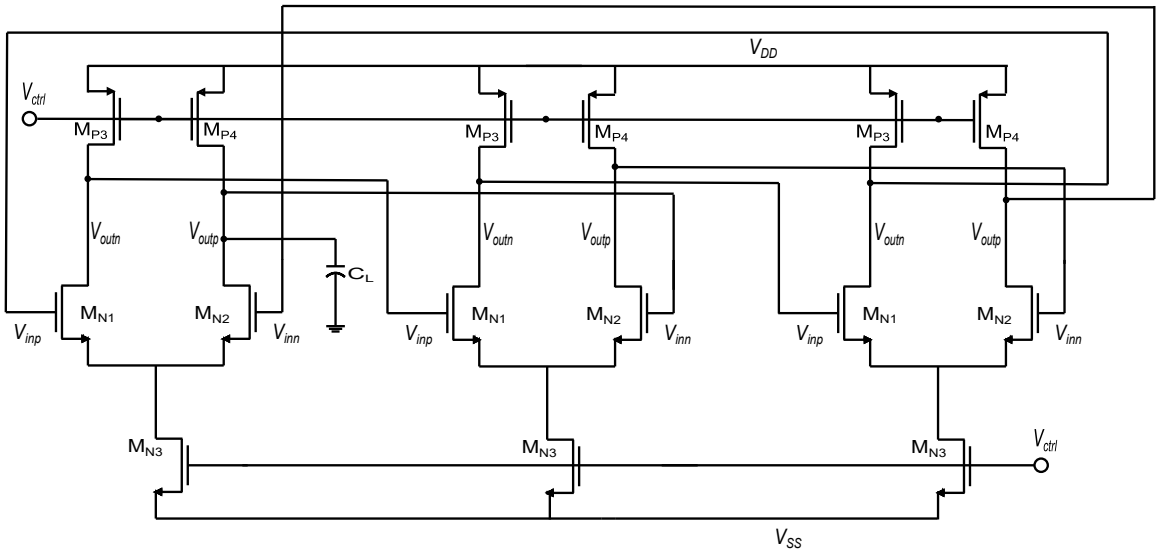


Figure 4.3: Three-Stage ring VCO

Table 4.3 shows the sizes of the 5 best feasible solutions, given by both DE and PSO. Whereas in Table 4.4 are summarized some of the more relevant constraint values. Analogously, the solutions considered to be the best are those more suitable for use in UWB systems.

Table 4.3: Best 5 feasible sized solution design variables.

$Solution$	$W_{MN1}(\mu m)$		$W_{MP3}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP3}(\mu m)$		$C_L(fF)$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	27.99	20.7	20.88	15.93	0.18	0.18	0.18	0.18	33	13
2	42.3	54.9	20.88	27.72	0.18	0.18	0.18	0.18	50	65
3	31.23	16.83	24.39	19.8	0.18	0.18	0.18	0.18	37	8
4	46.62	18.99	23.85	14.94	0.18	0.18	0.18	0.18	55	23
5	7.38	44.64	17.01	19.89	0.18	0.18	0.27	0.18	9	53

Table 4.4: Best 5 feasible sized solution constraints.

$Solution$	$Power(mW)$		$Freq.TR(GHz)$		$\|Volt.TR\|\,(V)$		$PN(dBc/Hz@1MHz)$		$\|FoM\|\,(\frac{dBc}{Hz})$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	15.4	14.7	8.49 to 0.0316	9.95 to 0.192	1.2	1.25	-87.31	-85.3	147.85	147.8
2	19.4	20.3	8.21 to 0.0236	9.6 to 0.148	1.4	1.1	-85.73	-87.16	145.09	144.9
3	17.8	14.3	8.08 to 0.0336	9.11 to 0.261	1.1	1	-86.42	-85.45	146.62	148.25
4	17.8	11.3	7.71 to 0.0249	8.94 to 0.18	1.3	1.2	-87.9	-86.2	146.11	148.24
5	17.8	18.6	7.5 to 0.105	8.79 to 0.129	1.2	1.4	-85.87	-86.24	149.07	145.19

The phase noise simulation results of the non-optimized design (-87.89 dBc/Hz@1MHz) against the best solution given by the DE (-87.31 dBc/Hz@1MHz) and the PSO (-85.3 dBc/Hz@1MHz) algorithms are shown in Figure 4.4. The blue signal depicts the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively. In this case, none of the optimized designs presents a minimization in phase noise.

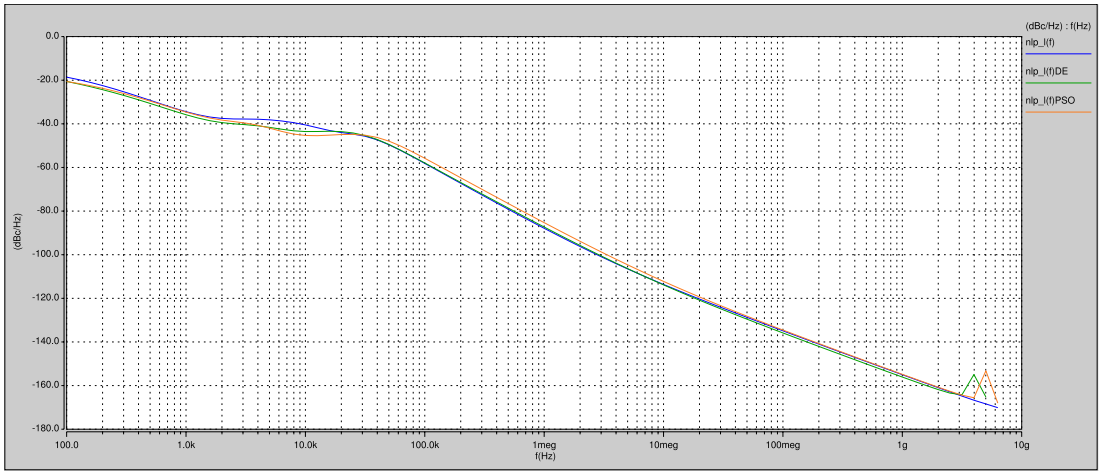


Figure 4.4: Phase noise of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

Figure 4.5 depicts the tuning characteristics of both the original and the two designs optimized for oscillation frequency. Both the DE and PSO optimized designs, have wider tuning ranges both in frequency and voltage.

4.1.2. Six-Stage Pseudo-Differential Ring VCO

The design variables of each of the 5 best feasible sized solutions for both algorithms, are summarized in Table 4.5. The simulated phase noise, frequency/voltage tuning ranges and power of the VCO, are summarized in Table 4.6. As in both the four and three stage ring VCOs the best solutions are considered to be the ones that are more suitable for UWB applications.

PN simulation results of the non-optimized design (-93.1 dBc/Hz@1MHz) against the best solutions given by DE (-109.97 dBc/Hz@1MHz) and PSO (-91.69 dBc/Hz@1MHz) are shown in Figure 4.6. The blue signal depicts the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively. In this

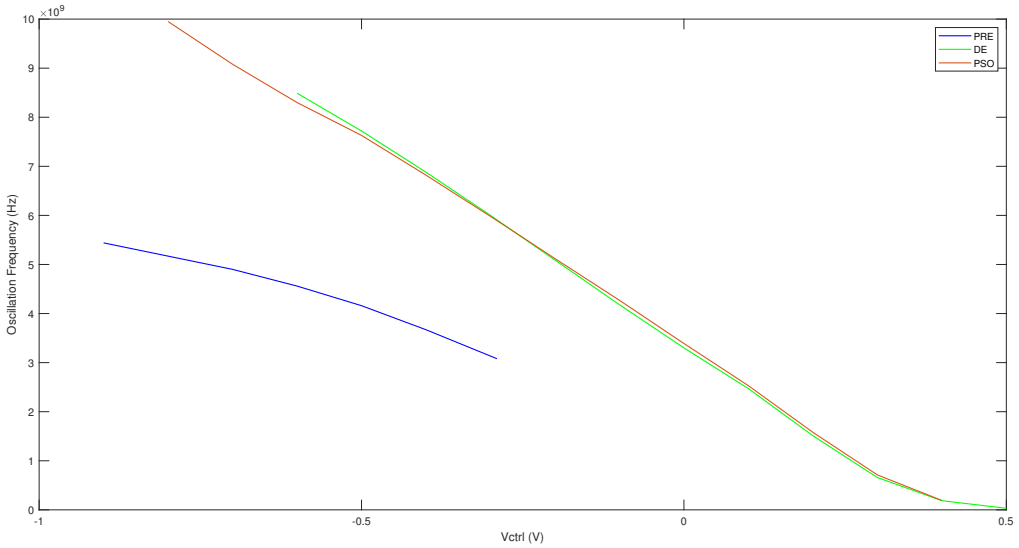


Figure 4.5: Tuning range of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

Table 4.5: Best 5 feasible sized solution design variables.

Solution	$W_{MN1}(\mu m)$		$W_{MP1}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP1}(\mu m)$		$W_{M2}(\mu m)$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	53.1	13.95	74.61	46.44	0.45	0.18	0.18	0.18	20.43	5.94
2	52.02	24.3	74.25	79.47	0.45	0.27	0.18	0.18	20.7	4.68
3	63	31.95	81.63	87.12	0.45	0.36	0.18	0.18	23.04	4.68
4	63.72	21.78	85.95	55.44	0.72	0.18	0.18	0.27	21.87	6.21
5	51.3	49.86	71.73	55.71	0.45	0.9	0.18	0.18	25.92	4.23

Table 4.6: Best 5 feasible sized solution constraints.

Solution	$Power(mW)$		$Freq.TR(GHz)$		$\|Volt.TR\|\,(V)$		$PN(dBc/Hz@1MHz)$		$\|FoM\|\,(\frac{dBc}{Hz})$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	57.94	32.79	0.685 to 0.515	2.2 to 1.82	1.2	1.4	-109.97	-91.69	138.41	142.94
2	57.2	47.3	0.668 to 0.493	2.44 to 2.16	1.3	1.5	-110.17	-93.1	148.45	143.7
3	59.4	50.7	0.63 to 0.469	2.29 to 2.06	1.3	1.3	-110.75	-95.99	148.06	145.67
4	55.9	15.9	0.562 to 0.402	1.59 to 1.3	1.4	0.9	-114.07	-90.68	150.34	141.6
5	56.5	37.9	0.48 to 0.342	1.31 to 1.24	1.3	1.2	-112.46	-105.25	148.56	151.65

case the best solution obtained through DE represents an enhancement in PN performance, which is not the case for the solution given by PSO.

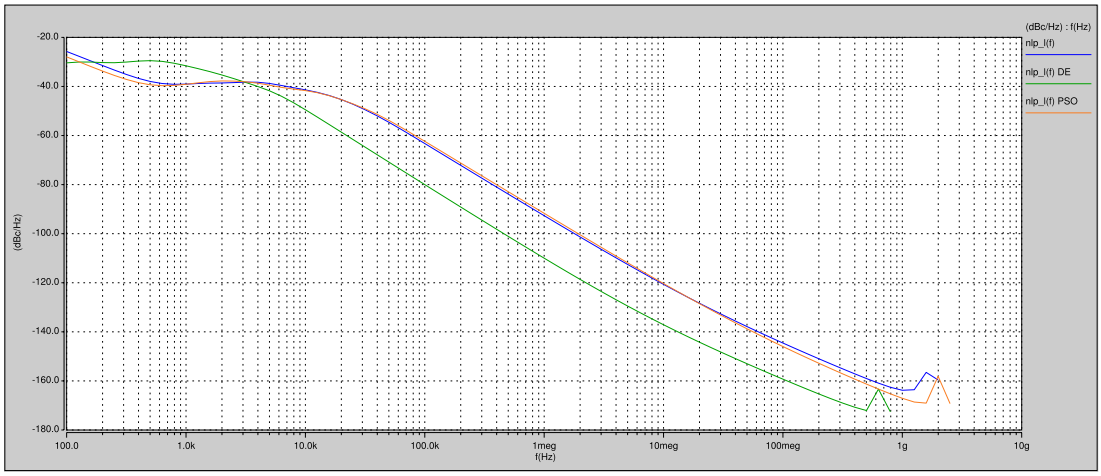


Figure 4.6: Phase noise of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

Tuning ranges of both the original and optimized designs are shown in Figure 4.7, in this case the tuning range of the solution given by the PSO algorithm is wider than in the original design, however this is not the case for the frequency tuning range of the DE algorithm solution since this is reduced in regards to that of the preliminary design.

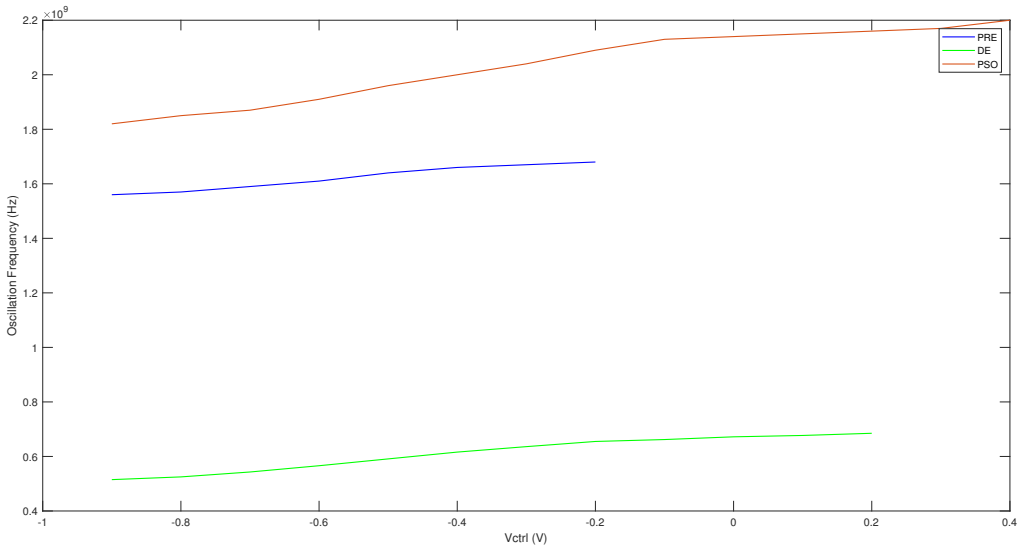


Figure 4.7: Tuning range of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

4.2. Phase Noise Optimization

Phase noise is one of the most important features in VCO performance. Given that there's a conflict between phase noise minimization and oscillation frequency maximization, phase noise optimization is used herein as a case study to appreciate and compare the effects on the different features of optimized designs when the objective function changes. For this case study, the oscillation frequency value is maintained as part of the optimization process as a constraint instead of an objective in contrast to what's reported in section 4.1, the details on how the optimization process is modified for phase noise optimization is described in 4.2.1.

For the four-stage VCO DE algorithm executions are carried out setting the number of individuals I_n and amount of generations max_{gen} to 50 and 30 respectively. For the PSO algorithm a population of 60 individuals and a maximum number of generations of 60 are used. Whereas for the six-stage VCO DE algorithm executions are carried out setting I_n and max_{gen} to 30 and 30 respectively. For the PSO algorithm a population of 60 individuals and a maximum number of generations of 40 are used. For both VCOs $f_{min} = 100MHz$ and $P_{max} = 30mW$.

4.2.1. Optimization Process

As previously stated the phase noise minimization is the optimization objective, in this case study the oscillation frequency is part of the optimization process as a constraint as well as the power consumption of the VCO and the operation region of the transistors. In this case study, the optimization algorithm checks whether or not the restrictions are fulfilled, if the constraints are met then phase noise is evaluated through HSPICE command .phasenoise, if phase noise simulation doesn't fail, then the particle is feasible. Conversely, if the constraints aren't fulfilled, or if the phase noise simulation fails then the algorithm establishes that particle as a non feasible one. Both optimization problems, as well as the adaptation of both algorithms for the defined sizing optimization problems are formulated and described accordingly below.

The optimization problem of the four-stage ring VCO for phase noise minization is defined by (4.1). Similarly, the design variables are the dimensions of the differential pair and the load transistors, but in this case the control voltage is also taken as a variable. The constraints are given by the operation region of the transistors, the minimum oscillation frequency and maximum power consumption. The objective function equation doesn't change from the oscillation frequency optimization, just with the difference that $f(x)$ stands for phase noise. The constraints related to the transistorsóperation region and the variables limits are the same as described in the oscillation frequency optimization. Similarly to the process followed to optimize oscillation frequency, firstly the operation region of the devices is checked from the HSPICE results of the delay cell

itself, and from the whole VCO oscillation frequency and power consumption values are extracted. If the constraints are fulfilled, then phase noise simulation is carried out.

$$
\begin{aligned}
&\text{Search} : x = [W_1, W_3, L_1, L_3, V_{ctrl}] \\
&Maximize : g(x) \\
&\text{Subject to} : f_{osc} \geq f_{oscmin} \\
&P_{cons} \leq P_{max}, \\
&V_{DS} \leq V_{GS} - V_{TH} \quad \text{for} \quad M_{P3} \quad \text{and} \quad M_{P4}, \\
&V_{DS} \geq V_{GS} - V_{TH} \quad \text{otherwise}, \\
&W_{min} < W < W_{max}, \\
&L_{min} < L < L_{max}, \\
&V_{SS} < V_{ctrl} < V_{DD}
\end{aligned}
\tag{4.1}
$$

The optimization problem associated with the phase noise optimization of the six-stage ring VCO, is defined by (4.2) for the DE algorithm. For the PSO algorithm the objective function is also solely defined by the phase noise. Whereas the design variables, x, are constituted by the control voltage and the dimensions of both the inverter (W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}) and the inverter cap (in which case $W_{M2} = W_{MN2} = W_{MP2} = L_{MN2} = L_{MP2}$). The constraints related to the transistorsóperation region are the same as specified for the oscillation frequency optimization problem, the rest are associated to the minimum oscillation frequency values and maximum power consumption. As in the previous oscillator, the sizing optimization problem finds the most suitable sizes of the design variables that are within the defined search ranges, considering the restrictions'compliance. The variables'search spaces remain the same for the optimization of both oscillators.

$$
\begin{aligned}
&\text{Search} : x = [W_{MP1}, W_{MN1}, L_{MN1}, L_{MP1}, W_{M2}, V_{ctrl}] \\
&Maximize : g(x) \\
&\text{Subject to} : f_{osc} \geq f_{min}, \\
&P_{cons} \leq P_{max}, \\
&V_{DS} \geq V_{GS} - V_{TH} \quad \text{for} \quad M_{N1} \quad \text{and} \quad M_{P1}, \\
&W_{min} < W < W_{max}, \\
&L_{min} < L < L_{max}, \\
&V_{SS} < V_{ctrl} < V_{DD}
\end{aligned}
\tag{4.2}
$$

The optimization problem remains fairly similar for the two oscillators, thus the pseudo codes for each algorithm are equivalent for both oscillators. The SPICE simulator

is linked within the optimization loop to evaluate some delay cell's parameters in both algorithms. Given that some data such as the VCO's oscillation frequency is required to properly set the phase noise simulation, then this step is added as a part of the optimization process after the simulation of the VCO, the only difference when setting phase noise simulations among the two oscillators is that in the differential topologies the designer has a variety of outputs that can be established as the oscillating node required to carry out the analysis, whereas in the pseudo-differential topology there are only two outputs available to establish as the oscillating node, this is maintained through all the algorithms and for both optimization objectives.

Algorithm 4.1 DE pseudocode

```
1: procedure DE(I_n, maxGen, g(x))
2:     Generate the SPICE netlist of the ring VCO
3:     for i = 1 : I_n do
4:         Initialize the population randomly and replace the initial individuals (Ws, Ls) into
   the netlist
5:         Evaluate the VCO and check the constraints
6:         if constraints = 0 then
7:             Simulate the VCO again and evaluate phase noise
8:         end if
9:     end for
10:    while j < maxGen do
11:        for i = 1 : I_n do
12:            Create a trial solution from 3 randomly selected parents using (1.4)
13:            Apply crossover using (1.5)
14:            Replace the new individual into the netlist
15:            Simulate the VCO and count the constraints
16:            if constraints = 0 then
17:                Simulate the VCO again and evaluate phase noise
18:            end if
19:            if the individual's objective function is less than that of the parent then
20:                The new individual replaces the parent using (1.6)
21:            end if
22:        end for
23:    end while
24: end procedure
```

The sizing optimization process to minimize phase noise, is summarized in the Algorithm 4.1 to use DE as the optimization method. As explained previously, for DE, the individuals from the randomly generated population are added to the VCO netlist and each one of them is simulated, the VCO electrical characteristics are extracted from HSPICE output file. If the constraints are satisfied, then the VCO is simulated again

with the same individuals, this new simulation features the addition of the necessary commands to execute phase noise simulation to the VCO netlist.

On the other hand, algorithm 4.2, summarizes the transformation of the PSO algorithm for the specific optimization problem of phase noise minimization, thus $g(x) = L\{f_{offset}\}$. Similarly to the process followed with the DE algorithm, with PSO the particles of the randomly generated population are replaced into the VCO netlist, when phase noise simulation doesn't fail the solution is considered feasible, whereas if it does fail or the constraints aren't matched the solution isn't feasible. The updating mathematical expressions are given by (1.7) and (1.8).

Algorithm 4.2 PSO pseudocode

```
1: procedure PSO(I_n, maxGen)
2:     Generate the SPICE netlist of the ring VCO
3:     for i = 1 : I_n do
4:         Initialize randomly the particles and replace them (Ws, Ls) into the netlist
5:         Evaluate the VCO and check the constraints
6:         if constraints = 0 then
7:             Simulate the VCO's phase noise
8:         end if
9:         Update the p_best particle considering the constraints and the objective function
10:        Update the g_best particle considering the constraints and the objective function
11:    end for
12:    for j = 1 : maxGen do
13:        for i = 1 : I_n do
14:            Copy particle i to p
15:            Update the particle p velocity using (1.7)
16:            Update the particle p position using (1.8)
17:            Replace the new particles into the netlist
18:            Simulate the VCO and count the constraints
19:            if constraints = 0 then
20:                Simulate the VCO's phase noise
21:            end if
22:            Compare particles i and p
23:            Update the p_best particle considering the constraints and the objective function
24:            Update the g_best particle considering the constraints and the objective function
25:        end for
26:    end for
27: end procedure
```

The process followed to carry out the constraint management has been previously detailed in section 3.4.

4.2.2. Four-Stage Differential Ring VCO

The design variables of each of the 5 best feasible sized solutions for both algorithms, are summarized in Table 4.7.

Table 4.7: Best 5 feasible sized solution design variables.

$Solution$	$W_{MN1}(\mu m)$		$W_{MP3}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP3}(\mu m)$		$V_{ctrl}(V)$		$C_L(fF)$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	84.69	75.33	75.42	60.21	0.72	0.72	0.9	0.81	-0.8	-0.9	370	330
2	71.82	76.23	61.47	66.24	0.72	0.72	0.81	0.9	-0.9	-0.9	314	333
3	76.5	67.86	61.83	59.31	0.72	0.63	0.81	0.81	-0.9	-0.9	335	260
4	88.74	78.3	63.72	66.15	0.72	0.63	0.81	0.9	-0.9	-0.9	388	299
5	89.91	77.67	53.64	60.57	0.9	0.54	0.72	0.81	-0.9	-0.9	492	254

Whereas the simulated phase noise (PN), frequency and power of the VCO, are summarized in Table 4.8. For this purpose, the best solutions are considered to be the ones with the lower phase noise.

Table 4.8: Best 5 feasible sized solution design constraints.

$Solution$	$Power(mW)$		$Frequency(MHz)$		$PN(dBc/Hz@1MHz)$		$\|FoM\|$ $(\frac{dBc}{Hz})$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	29.45	29.1	622.87	706.78	-113.79	-112.66	155.71	155.01
2	28.72	29	713.97	669.22	-113.04	-112.64	155.53	154.53
3	29.2	28.9	699.46	828.18	-112.51	-111.49	154.75	155.24
4	29.7	29.4	645.84	739.44	-111.47	-110.68	152.94	153.37
5	28.9	29.9	540.62	888.64	-110.81	-110.94	150.86	155.16

The phase noise simulation results of the non-optimized design (-87.89 dBc/Hz@1MHz) against the best solution given by the DE (-113.79 dBc/Hz@1MHz) and the PSO (-112.66 dBc/Hz@1MHz) algorithms are shown in Figure 4.8. The blue signal depicts the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively. From Table 4.7 and Figure 2.10 it is noticeable the improvement of 25.9 and 24.77 dBc/Hz@1MHz, in regards to the original design phase noise, for DE and PSO algorithms, respectively.

It can be seen that DE algorithm achieved lower phase noise compared to PSO, while requiring less resources to achieve slightly better results. Compared to DE, PSO required to increase both the population size and the maximum number of generations to 60.

Additionally, PSO algorithm required approximately two to three times the execution time of DE to generate quite similar feasible solutions.

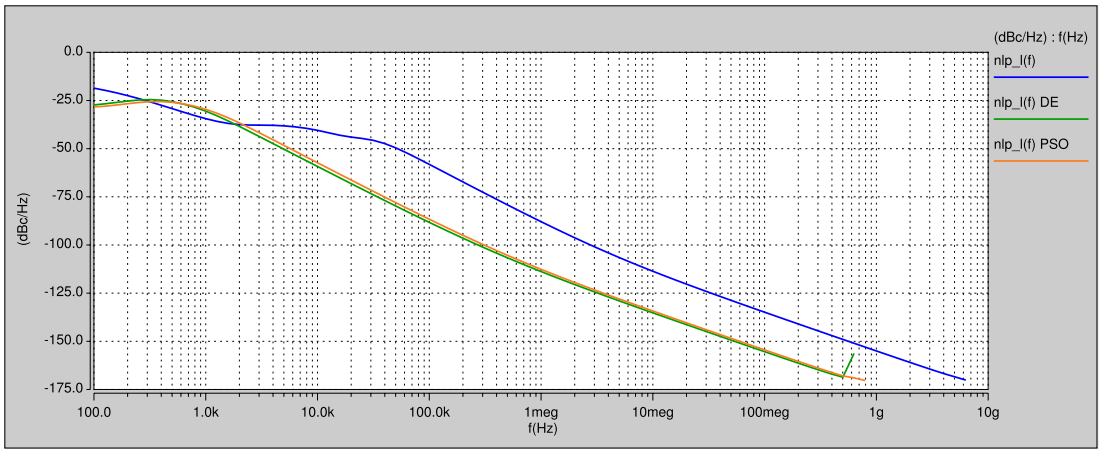


Figure 4.8: Phase noise of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

Similarly, Figure 4.9 depicts the tuning characteristics of both the original and the two designs optimized for PN, it is quite noticeable that both the tuning range and the achievable oscillation frequencies are reduced when the optimization objective is changed to be phase noise. For the DE optimized design the TR is defined from 669.46 to 622.87 MHz for control voltages of -0.9 to -0.8 V. Whereas for the PSO optimized design the TR is defined from 706.78 to 669.31 MHz for control voltages of -0.9 to -0.8 V. Reasserting the point that achieving the simultaneous performance improvement of multiple IC features isn't a trivial task.

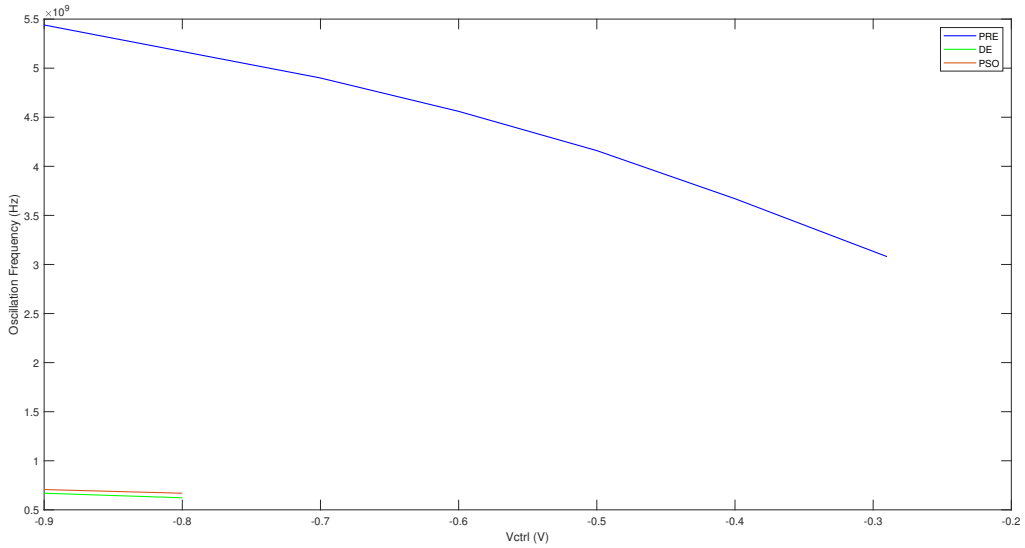


Figure 4.9: Tuning range of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

4.2.3. Six-Stage Pseudo-Differential Ring VCO

The design variables of each of the 5 best feasible sized solutions for both algorithms, are summarized in Table 4.9. On the other hand, the simulated phase noise (PN), frequency and power of the VCO, are summarized in Table 4.10. For this purpose, the best solutions are considered to be the ones with the lower phase noise.

Table 4.9: Best 5 feasible sized solution design variables.

$Solution$	$W_{MN1}(\mu m)$		$W_{MP1}(\mu m)$		$L_{MN1}(\mu m)$		$L_{MP1}(\mu m)$		$W_{M2}(\mu m)$		$V_{ctrl}(V)$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	39.42	20.43	89.1	60.12	0.9	0.72	0.39	0.54	33.3	24.93	-0.9	-0.64
2	40.2	13.14	89.95	58.86	0.9	0.54	0.44	0.72	30.79	19.53	-0.88	-0.86
3	33.88	7.02	89.25	46.35	0.86	0.81	0.48	0.9	29.37	13.05	-0.7	-0.43
4	30.74	31.5	89.4	78.39	0.86	0.63	0.51	0.36	26.88	22.41	-0.69	-0.83
5	33.72	23.67	89.27	80.91	0.86	0.81	0.58	0.81	27.41	13.23	-0.77	-0.37

The phase noise simulation results of the non-optimized design (-93.1 dBc/Hz@1MHz) against the best solution given by the DE (-129.01 dBc/Hz@1MHz) and the PSO (-124.67 dBc/Hz@1MHz) algorithms are shown in Figure 4.10. The blue signal depicts

Table 4.10: Best 5 feasible sized solution design constraints.

$Solution$	$Power(mW)$		$Frequency(MHz)$		$PN(dBc/Hz@1MHz)$		$\|FoM\|$ $(\frac{dBc}{Hz})$	
	DE	PSO	DE	PSO	DE	PSO	DE	PSO
1	26.41	13.38	101.17	104.58	-129.01	-124.67	154.89	153.79
2	23.52	10.06	100.85	100.69	-128.85	-122.46	155.21	152.49
3	21.57	5.01	100.56	100.38	-128.82	-122.38	155.53	155.41
4	18.47	24.9	100.13	200.87	-128.77	-121.36	156.12	153.46
5	19.32	12.67	100.13	194.4	-128.65	-120.79	155.8	155.54

the original phase noise, whereas the green and orange signals depict the DE and the PSO phase noise, respectively. From Table 4.9 and Figure 2.15 it is noticeable the improvement of 35.91 and 31.57 dBc/Hz@1MHz, in regards to the original design phase noise, for DE and PSO algorithms, respectively.

It can be seen that DE algorithm achieved lower phase noise compared to PSO, while requiring less resources to achieve better results. Another point is that compared to DE, PSO required to increase both the population size and the maximum number of generations to 60 and 40, respectively. Additionally, PSO algorithm required approximately two to three times the execution time of DE to generate similar feasible solutions.

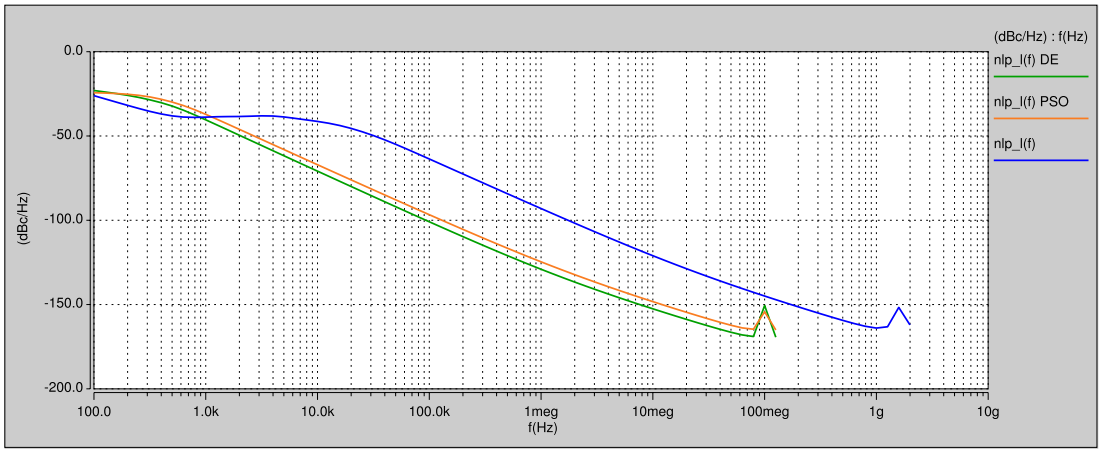


Figure 4.10: Phase noise of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

On the other hand, the tuning ranges of both the original and optimized designs are shown in Figure 4.11, in this case the voltage tuning range is wider than in the original design, however this is not the case for the frequency tuning range since this is reduced in regards to that of the preliminary design (comparing to the results given by both algorithms).

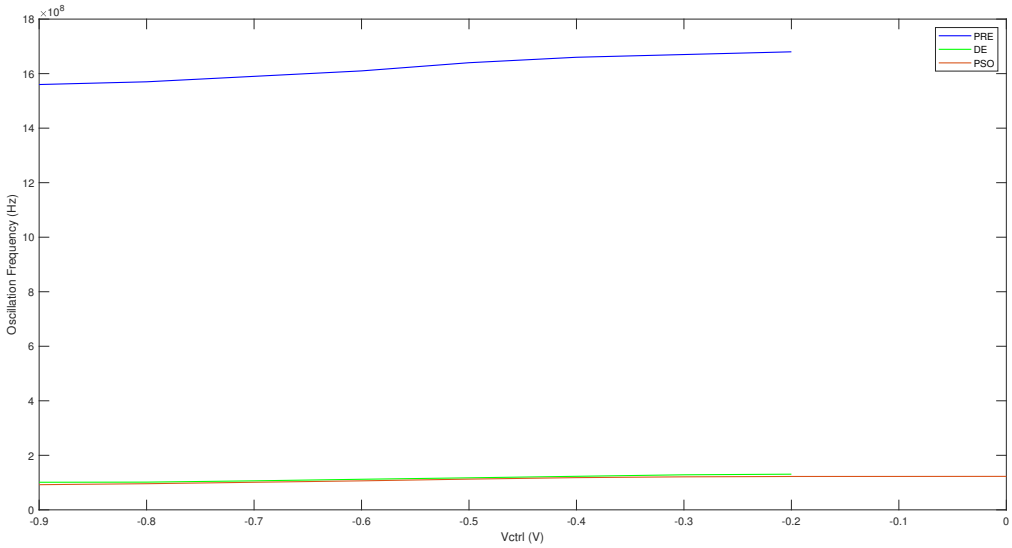


Figure 4.11: Tuning range of the best sized solutions provided by the DE (blue) and PSO (green) algorithms

4.3. Results Comparison

4.3.1. Oscillation Frequency Optimization

Table 4.11 sums up the features of some VCOs used in UWB systems. Here in the best design obtained from oscillation frequency optimization, which is a result of the optimization of the three-stage ring VCO by PSO algorithm, is compared to other VCOs used in UWB systems. As one can see, the frequency tuning range of the design obtained herein is one of the largest and covers almost all the frequency interval assigned to UWB systems to operate in, while maintaining other parameters such as phase noise and power within acceptable values, also the FoM is comparable to that of other designs in the state of the art. Furthermore, it is worth mentioning that the approach of reducing the number of delay stages, N, to three with the aim to increase the oscillation frequency was reasonable since it comply with the intention of having a design with higher f_{osc}.

Among the works designed in 180nm none of them is enhanced through any optimization method. The oscillator designed in [80] uses a symmetric load differential delay stage to construct a four-stage ring VCO, with the intention to be used in an UWB transmitter, it achieves a TR magnitude of 2.2GHz that is required for its application but is narrower than the TR reached in this work. It also has a better PN performance and FoM

Table 4.11: Characteristics of VCOs used in UWB systems

$Work$	$Tech.(nm)$	$Power(mW)$	$PN(\frac{dBc}{Hz})$	$\lvert FoM\rvert\ (\frac{dBc}{Hz})$	$Freq.TR(GHz)$	$\lvert Volt.TR\rvert\ (V)$
This Work	180	14.7	-85.3 @1MHz	147.8	9.95 to 0.192	1.25
[80]	180	41.36	-91.71 @ 1MHz	150.8	3.98 to 6.18	0.85
[77]	130	5	-88.4 @1MHz	156.5	1.82 to 10.18	
[94]	180	18.4	-95 @ 1MHz	-	2.7 to 5.4	1.6
[95]	180	3.42	-120.1 @1MHz	-	3.77 to 4.27	1.8
[96]	90	8.26	-75.2 @1MHz	137.03	2.1 to 5	0.64
[97]	130	300	-106 @1MHz	-	3.2 to 22.7	8.5

in regards to this work, however the power consumption is one of the highest among the works compared in Table 4.11. In [94] the design of a LC-VCO to work in the UWB low-frequency band (3.1 to 5 GHz), in this topology the passive spiral inductor is replaced by a tunable active inductor. The TR magnitude is 2.7GHz which is sufficient to satisfy the objective of working in the low frequency band, and the PN reported is around the values obtained in similar works, in regards to this work the design of [94] features a higher power consumption, lower phase noise and a narrower TR. Similarly, in [95] a LC-VCO with a complementary cross-coupled topology with the aim to be used as a part of a multi-band UWB frequency synthesizer. Its TR is 0.5GHz, which is the narrower among the ones compared, in contrast the PN and power consumption featured in this design are the lowest from Table 4.11.

From the works implemented in 130nm technology, none of them is enhanced through any optimization method. In [77] a two-stage ring VCO meant to be used in UWB applications is carried out. This design features a 8.36GHz TR, which is smaller than the 9.76GHz TR achieved in this work but the maximum frequency is higher than the one reached in this work. Among the works compared, this one features the best FoM, its power consumption and its phase noise are lower to that of what's obtained in this work. A LC-VCO used to implement an UWB signal source for radar applications, which is composed by three VCO blocks is reported in [97]. The entire TR (of the three VCOs) is 19.5GHz, however 10GHz is the maximum continuous TR which is slightly higher than the one featured in this work, however it features the highest power consumption which is around 20 times higher of that reported in this work. The PN obtained through this design is one of the lowest from the ones reported. In [96] a VCO that aims to be adequate for UWB-FM applications and use in an UWB-FM transmitter, is designed in 90nm technology. Its TR is 2.9GHz, which is in the narrower side, similarly to its PN and FoM which are both the worst values among the works reported, on the other hand, its power consumption is on the lower side, being lower than that of the reported in this work.

As one can see from the analysis presented above and as highlighted throughout this thesis, metaheuristics allow the user to achieve an overall performance enhancement. Taking the results presented above, one can notice that only one of the referred works

reached a wider tuning range, having a f_{max} which is also higher than the f_{max} of this work, but this same design has the highest power consumption among all of them. Whereas as one may notice the best phase noise performance is obtained from the design that has the narrowest TR. Thus, metaheuristics allow the designer carrying out a circuit design sizing, whose response can be satisfactory in more than one aspect and without surpassing certain limits that could affect in a negative way the circuit performance or make it inadequate for applications that have certain power or phase noise requirements, among all of the other design requirements that are critical for some circuit's efficiency.

Figure 4.12 shows the tuning range comparison of each of the best solution obtained with each topology for oscillation frequency optimization. As one can see the three and four stage VCOs have quite a wider tuning range than that of the six-stage VCO. On the other hand, Figure 4.13 depicts the phase noise performance comparison for the three VCO topologies optimized for oscillation frequency, it can be seen that the lower phase noise is achieved by the six-stage VCO design solution, being the three-stage VCO the one with the highest PN value.

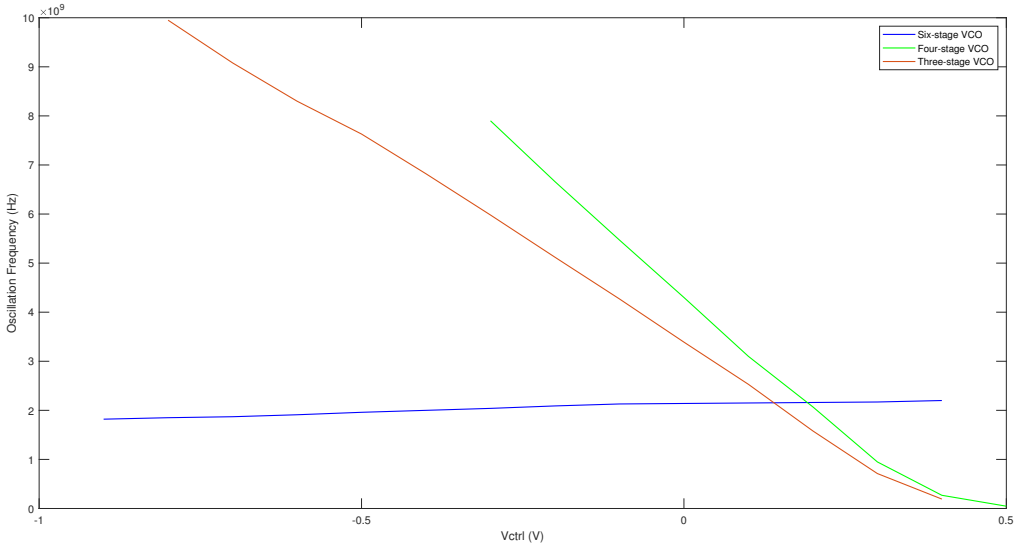


Figure 4.12: Tuning range of the best sized solutions resulting from the six-stage (blue), four-stage (green) and three-stage (red) VCO oscillation frequency optimization

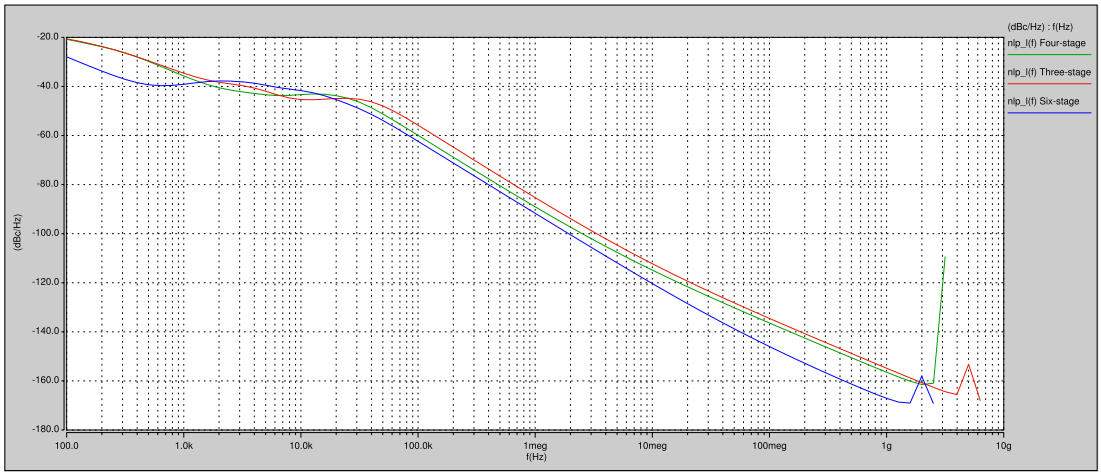


Figure 4.13: Phase noise of the best sized solutions resulting from the six-stage (blue), four-stage (green) and three-stage (red) VCO oscillation frequency optimization

4.3.2. Phase Noise Optimization

Table 4.12 shows a comparison of some relevant parameters in VCO performance of the best sizing result considering PN optimization with other ring VCO topology results in the literature. As one can see, the PN performance of the pseudo-differential design obtained through optimization with the DE algorithm is comparable to what is already reported in the literature for designs implemented in the same technology and measured at the same offset frequency, while also represents an improvement from the PN performance of the non-optimized design.

The same can be said for the differential topology where a better PN performance was obtained in regards to other oscillators reported that are implemented with the same type of topology and also when comparing it to the design before optimization. On the other hand, the power consumption of the VCOs designed herein is on the higher side and the tunning range of the ring VCO implemented with a differential topology is narrower than it used to be before optimization, however is comparable to what's reported in similar works.

Taking into account the results obtained from the oscillation frequency optimization analyzed in 4.3.1, one can notice the big results difference when the objective to optimize is changed, for example here is noticeable that the TR achieved in this case is narrower to that of when the optimization was the oscillation frequency, but as expected the PN performance is improved being one of the best ones at that offset frequency. It also can be noted that the six-stage VCO topology is better suited for phase noise minimization since it gave better phase noise results regardless of the optimization objective. Whereas among the three and four stage VCOs, is noticeable that the four-stage

Table 4.12: Ring VCO characteristics.

$Work$	$Tech.(nm)$	$Topology$	$Power(mW)$	$PN(\frac{dBc}{Hz})$	$\|FoM\|\ (\frac{dBc}{Hz})$	$Freq.TR(GHz)$	$\|Volt.TR\|\ (V)$	$K_{VCO}(\frac{GHz}{V})$
This Work	180	PD	26.41	-129.01@1MHz	154.89	0.1 to 0.13	0.7	-
This Work	180	D	28.9	-113.79@1MHz	155.01	0.669 to 0.623	0.2	-
[8]	180	PD	1.06	-138.5@100MHz	-	1.66 to 1.57	0.4	0.023
[28]	180	SE	0.19	-138@1MHz	-	1 ± 14 %	-	-
[27]	180	SE var.	1.2	-106@1MHz	165.1	0.8 to 1.3	1.1	-
[4]	180	D	28	-92.68@1MHz	-	1.78 to 2.53	0.2	7 %
[30]	65	PD	20	-90.08@10.3125GHz	157.34	11 to 2.4	0.65	4.6
[29]	45	SE var.	0.357	-88.54@10MHz	-	41.75 to 0.308	0.5	-
[31]	40	D	1.1	-98.05@1MHz	160.4	0.86 to 1.38	1.1	-
[25]	28	PD	1.1	-95.7@1MHz	160.7	0.7 to 2.78	-	0.25

ring VCO resulted in better phase noise performance than that of the three-stage VCO design solutions.

Figure 4.14 shows the tuning range comparison of each of the best solution obtained with each topology for phase noise optimization. As one can see the four stage VCOs has a wider tuning range than that of the six-stage VCO. Whereas, Figure 4.15 depicts the phase noise performance comparison for the two VCO topologies optimized for phase noise minimization, it can be seen that the lower phase noise is achieved by the six-stage VCO design solution.

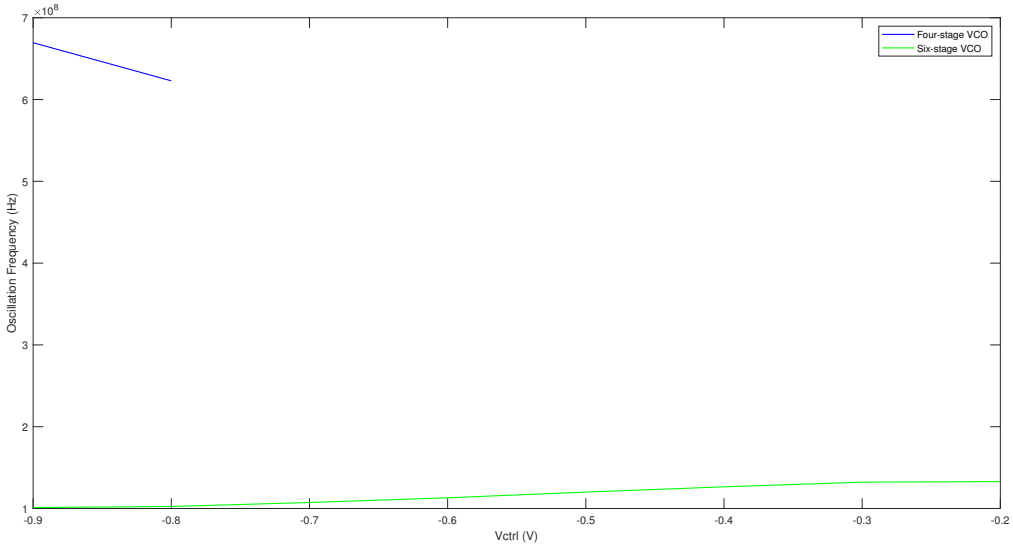


Figure 4.14: Tuning range of the best sized solutions resulting from the four-stage (blue) and six-stage (green) VCO phase noise optimization

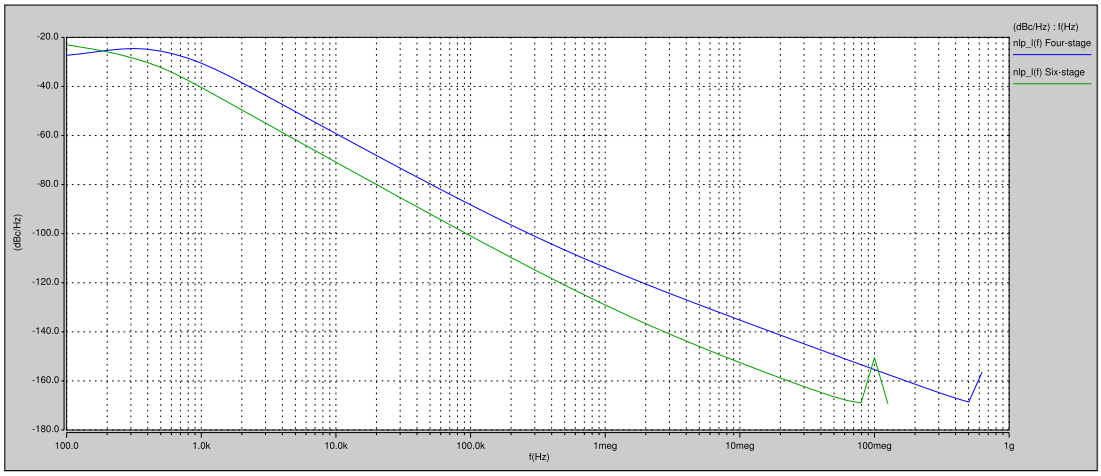


Figure 4.15: Phase noise of the best sized solutions resulting from the four-stage (blue) and six-stage (green) VCO phase noise optimization

Figure 4.16 shows the tuning range comparison of each of the best solution obtained through oscillation frequency and phase noise optimization, for the four-stage VCO. It is noticeable the big difference in tuning range magnitude within the design resulting from the oscillation frequency optimization and the one optimized for phase noise, with the latter being a lot narrower in comparison. On the other hand, Figure 4.17 depicts the comparison in phase noise performance of the two best four-stage VCO designs optimized for oscillation frequency and for phase noise, respectively. As one can see, from the two VCO designs the one that shows better phase noise performance is the one that is optimized for phase noise as expected.

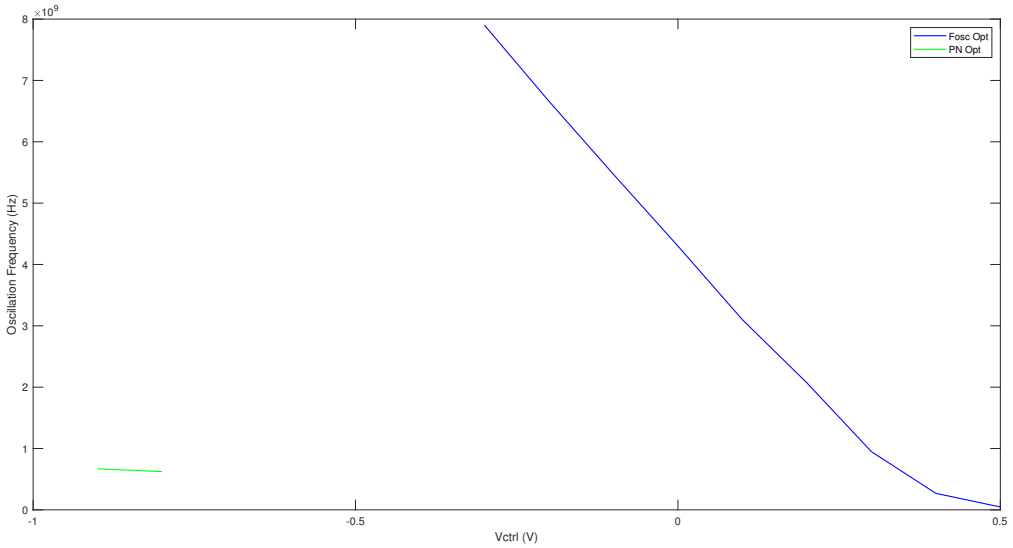


Figure 4.16: Tuning range of the best sized solutions of the four-stage VCO resulting from oscillation frequency (blue) and phase noise (green) optimization

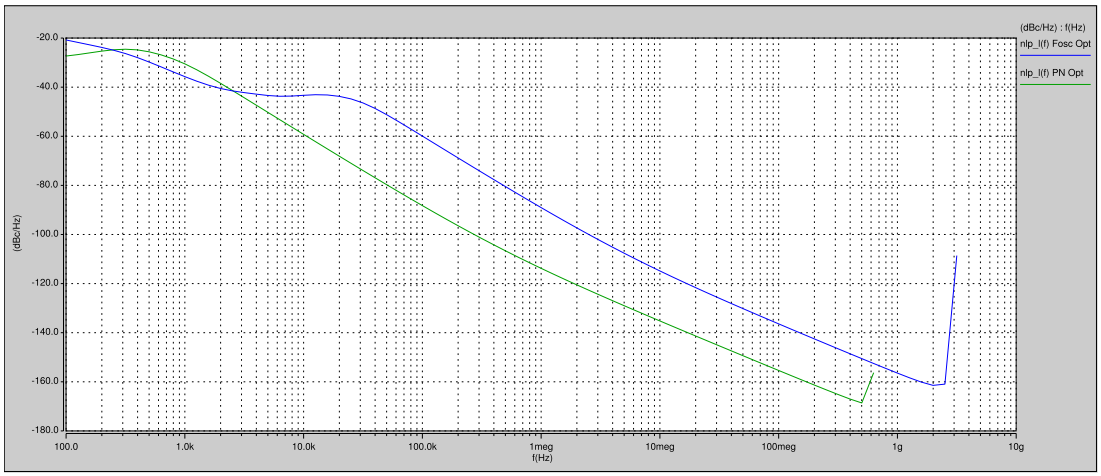


Figure 4.17: Phase noise of the best sized solutions of the four-stage VCO resulting from oscillation frequency (blue) and phase noise (green) optimization

Figure 4.18 shows the tuning range comparison of each of the best solution obtained through oscillation frequency and phase noise optimization, for the four-stage VCO. Similarly to the four-stage VCO the design optimized for oscillation frequency features a wider tuning range than that of the phase noise optimized one, but in this case is not such an extreme magnitude difference. Moreover, Figure 4.19 shows the comparison

in phase noise performance of the two best six-stage VCO designs optimized for oscillation frequency and for phase noise, respectively. As one can see, from the two VCO designs the one that shows better phase noise performance is the one that is optimized for phase noise as expected, for this topology there's a bigger and more noticeable difference between the two optimization results.

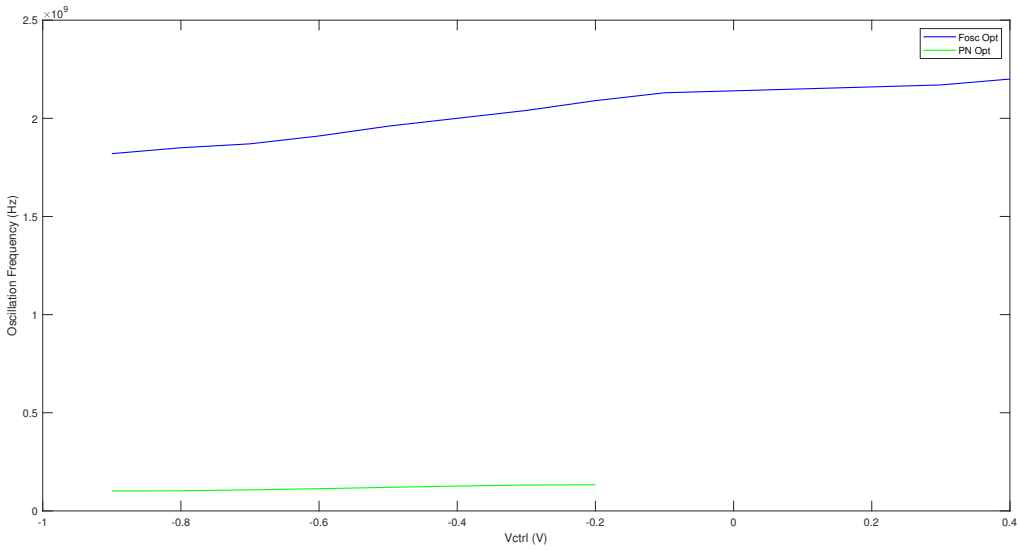


Figure 4.18: Tuning range of the best sized solutions of the six-stage VCO resulting from oscillation frequency (blue) and phase noise (green) optimization

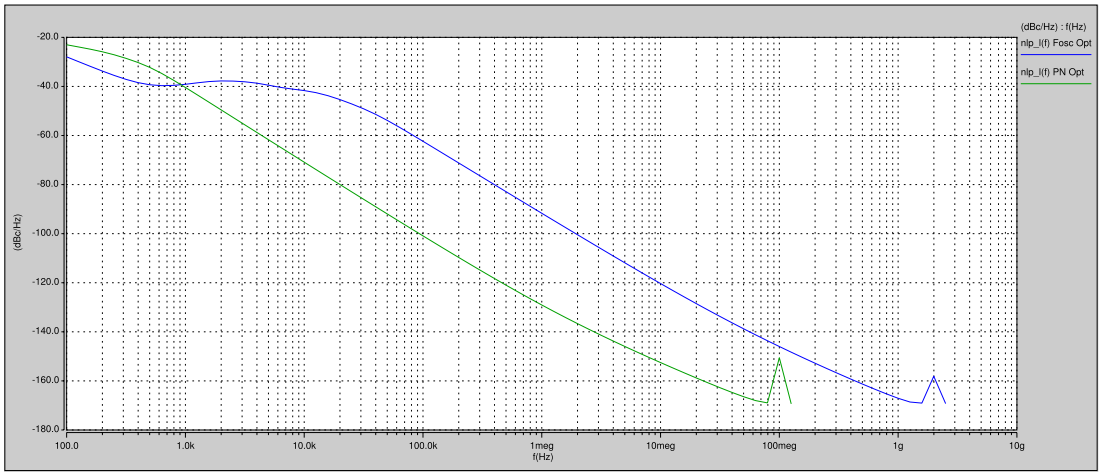


Figure 4.19: Phase noise of the best sized solutions of the six-stage VCO resulting from oscillation frequency (blue) and phase noise (green) optimization

Chapter 5
Conclusions and Future Work

5.1. Conclusions

Throughout the investigation developed in this thesis has been clear that the relevance of VCO features such as power consumption, phase noise, oscillation frequency, tuning range and VCO gain, among others, is directly related to the requirements of the application the VCO is meant to be used in. This is due to the fact that not all the applications require from the VCO block to have the same behavior, some applications require a low power VCO while in other the power consumption isn't a concern to take into account, and this applies for all of the features that characterize a VCO. In this case study, the ring VCO is meant to be used in UWB systems, which determined the optimization objective as well as the constraints that were codified in the optimization algorithm. Both the objective and constraints can change drastically from one case study to another, e.g. a different case study may require to add a lot more constraints to be able to guarantee a good performance.

Through the oscillation frequency optimization of three different VCO topologies for oscillation frequency maximization, the three and four stage ring VCOs resulted in better designs in terms of suitability for use in UWB systems due to the wide TR achieved, while also maintaining acceptable values of power consumption and phase noise. Initially the VCOs to optimize were only the four and six-stage topologies, however a test with three-stage topology was carried out with the aim to reach higher oscillation frequencies than what was obtained through the four-stage designs, which proved to be a valid approach since this reduction in the number of stages allowed a further enhancement of the oscillation frequency, with the best design being one obtained through the optimization of the three-stage VCO. In terms of power consumption the best design is on the lower end, whereas its FoM is quite similar to that of the works compared, however in terms of phase noise this design is in the higher end in regards to the works with which is being compared. Otherwise, the six-stage topology provided oscillation frequencies less than half of that obtained with both three and four stage oscillators, at the same time the power consumption also increased from the other two VCO designs,

however contrary to the other parameters phase noise performance was better in the six-stage VCO designs.

To better explore the performance differences of both topologies and the contrast in results when changing the optimization objective other test was performed but this time for phase noise optimization. In the phase noise optimization test the six-stage VCO turned out to result in designs that feature a lower phase noise, in regards to the four-stage ring VCO. When optimizing phase noise the six-stage oscillator featured one of the lowest phase noise values among the works that measure it at the same offset frequency, however the power consumption and FoM could be further improved, when it comes to the TR, it's quite comparable to that of the other designs that are being compared but is noticeable that the TR achieved with this topology is very reduced in regards to the TR obtained with both the three and four stage ring VCOs. On the other hand, when using the four-stage VCO topology to optimize phase noise the achievable oscillation frequency was drastically reduced whereas the power consumption is increased overall in comparison to the oscillation frequency optimized designs.

This results reinforce the point that different topologies are more or less suitable for specific applications, in this case the six-stage VCO is more adequate for those applications that require low phase noise performance but that not necessarily need a wide tuning range. Whereas in the contrary, both the four and three stage ring VCOs are more fitting to be used in applications where a wide tuning range is a requirement. It's remarkable that one topology can result in a very different performance if the optimization objective changes, which is very noticeably exemplified with the two case studies and the two different optimizations carried out herein. The achievement of even wider tuning ranges requires the use of other VCO topologies. With that being said each of the topologies selected for optimization through metaheuristics, were enhanced in regards to the preliminary designs and its results are comparable to that of other VCO designs used in UWB systems.

From the application of two different metaheuristics it is evident that in all executions, PSO requires more resources than DE to be able to generate adequate designs. However, as one can appreciate the best designs for oscillation frequency optimization of both the three and six-stage VCOs were obtained through PSO, in contrast the best design of the four-stage VCO was obtained through DE. Whereas in phase noise optimization, DE algorithm provided the best solutions in the two oscillators that were optimized. Given that these two metaheuristics feature differences on the constraint management criteria and taking into consideration that in the oscillation frequency optimization process there was a higher amount of constraints involved, it may be inferred that the DE optimization results could be benefited of adjusting the before mentioned criteria to be more adequate for the specific objective established in this work.

5.2. Future Work

The possible future work related to this thesis could be:

- Carry out multi-objective optimization of both VCO designs.
- Extend the optimization to other VCO topologies.
- Use machine learning for the optimization.
- Perform VCO optimization for a different application that features a distinct objective and restrictions than the ones described in this work.

Appendix A
Published Works

- Perla Rubi Castañeda-Aviña, Esteban Tlelo-Cuautle, Luis Gerardo De La Fraga, Phase Noise Optimization of Integrated Ring Voltage-Controlled Oscillators by Metaheuristics, AIMS Mathematics, vol. 7, no. 1, pp. 14826-14839, eISSN 24736988, June 9, 2022. DOI: 10.3934/math.2022

- MA Valencia-Ponce, PR Castañeda-Aviña, E Tlelo-Cuautle, VH Carbajal-Gómez, VR González-Díaz, Y Sandoval-Ibarra, JC Nuñez-Perez, CMOS OTA-based filters for designing fractional-order chaotic oscillators, Fractal and fractional, vol. 5, no. 3, Art 122, pp 1-16, eISSN 25043110, September 2021. DOI: 10.3390/fractalfract5030122

- Perla Rubi Castañeda-Aviña, Esteban Tlelo-Cuautle, Luis Gerardo de la Fraga, Single-objective Optimization of a CMOS VCO Considering PVT and Monte Carlo Simulations, Mathematical and Computational Applications, vol. 25, no. 4, article 76, pp. 1-14, ISSN 1300686X e 22978747, 2020. DOI: 10.3390/mca25040076

- E Tlelo-Cuautle, PR Castañeda-Aviña, R Trejo-Guerra, VH Carbajal-Gómez, Design of a Wide-Band Voltage-Controlled Ring Oscillator Implemented in 180nm CMOS Technology, Electronics, vol. 8, no. 10, Art 1156, pp. 17, eISSN: 2079-9292, 2019. DOI: 10.3390/electronics8101156 Q3

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