CMOS Circuit Design for Bio-Impedance Spectroscopy Applications

by

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The deeper I get the less that I know
That's the way that it go
The less that I know the deeper I go

The Strokes

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Abstract

The analysis of bioimpedance spectroscopy (BIS) is based on measuring the passive electrical properties of biological tissues and their frequency-dependent response to alternating current. This non-invasive characterization technique has become a fundamental tool for obtaining diagnostic information about the physiological properties of the human body.
The non-invasiveness, continuous monitoring capability, portability, and versatility of BIS systems have become increasingly relevant in the development of new healthy applications and measurement techniques. Additionally, the advancements in CMOS technology, these factors highlight the need to optimize analog and digital blocks to enable precise voltage measurements across a broad frequency range while meeting requirements for noise, power consumption, and area efficiency in both front-end and back-end stages.
This work presents proposed analog and digital blocks for BIS applications designed using UMC 180nm technology. For signal generation in the backend stage, a QFGT-modified ring oscillator topology operating in weak inversion is proposed to generate kilohertz-range signals. The oscillator incorporates dual control mechanisms: one based on a feedback factor, β, and other based on a tuning voltage, V_{Tune} . As an digital alternative, a Direct Digital Synthesizer (DDS) with signal compression is introduced, reducing the memory consumption of the ROM used to store the discretized sine wave. Finally, the design of a front-end signal conditioning circuit is presented, comprising and high-performance instrumentation amplifier with a gain range of 26–76 dB and an associated CMRR of 130–189 dB.

Keywords: Bio-Impedance Spectroscopy Analysis, QFGT-modified ring oscillators, Direct Digital Synthesizer, Instrumentation Amplifier.

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CHAPTER 1

Introduction

This chapter outlines this work's specific goals and objectives, providing a clear structure for the study. Moreover, it introduces tissue behavior and the appropriate techniques for bio-impedance measurements. It begins by focusing on the impedance response in the frequency domain. Finally, it briefly describes the biological phenomena involved in measuring tissue impedance, highlighting the frequency ranges of each biological mechanism.

1.1 Motivation

In recent years, Bio-Impedance Spectroscopy (BIS) analysis is a non-invasive method that has positioned itself as an alternative to continuous monitoring and early detection of diseases, even as a novel tool to generate tomographic type images, therefore, to exploit the full potential of Bioimpedance Spectroscopy measurements it is essential using front-end and back-end systems that require high accuracy and a wide bandwidth range. These systems are usually implemented as application-specific integrated circuits (ASICs) in CMOS technology that allow the integration of analog and digital blocks on a single chip at a reasonable cost.
Typically, BIS architectures comprise a back-end consisting of a signal generator over the frequency range of interest and a transconductor stage to convert the voltage signal into a current to be injected into the Tissue Under Test (TUT). On the other hand, the front-end stage allows the voltage reading of the generated response to subsequently calculate the magnitude and phase of the associated, or the real and imaginary component.
However, the integration of this type of systems involves designing robust systems to artifacts due to the electrodes, high dynamic range (1 m Ω - 10 kΩ), high skin-electrode impedances (10 kΩ - 10 MΩ)). Similarly, the need for low-power consumption and safety compliance to medical standards (IEC) requires customized approaches that take advantage of the benefits offered by analog and digital design.
Although many publications address specific components such as internal amplifiers, signal generators, and a voltage-controlled current source (VCCS), the implementation of the front-end and back-end of the system represents a challenge in the design of the

BIS ASIC due to the wide frequency range over which it must work, raising the need to improve designs or include topologies that allow an accurate measurement considering the abovementioned aspects.
Using BIS analysis as a non-invasive continuous monitoring tool represents an opportunity for optimizing ASICs that perform these measurements. The wide range of frequencies over which it works, as well as the power consumed by the system, represents a tradeoff in the design of each of the blocks that make up the ASIC; on the other hand, implementing a back-end stage that meets the specifications of medical standards represents a necessity not only in a structured design but in a complete integration of a high-performance BIS system.

1.1.1 Objectives

To conduct a comprehensive study of the requirements for various applications of Bio-Impedance Spectroscopy (BIS) analysis, aiming to provide an overview of the architectures capable of performing these measurements. That includes developing a macro-modeling methodology for blocks comprising an impedance measurement system and proposing analog signal generators based on QFGT-modified Ring Oscillators and digital signal generators using a Direct Digital Synthesizer (DDS) approach. Additionally, the research aims to design an initial signal conditioning front-end to facilitate accurate impedance measurements.

Specific objectives

- Study the principles of Bio-Impedance measurement, including excitation signal generation, impedance modeling and equivalent electrical representation of the measurement system.

- Investigate the fundamental building blocks of a bioimpedance front-end system, including their interdependencies and the critical parameters used to assess their performance.

- Analyze the theoretical performance of existing architectures for Bio-Impedance front-end electronics and correlate these findings with the state of the art to identify limitations and opportunities for improvement.

- Propose a novel design approach to signal generator using a QFGT-modified Maneatis Cell Ring Oscillator to generate a signal over a wide frequency range.

- Design and optimize the proposed architecture and validate through process variations and Monte Carlo analysis to verify the robustness of the design, making each block relevant to Bio-Impedance applications.

1.2 Theoretical Fundamentals

1.2.1 Electrical Impedance

The electrical impedance of a two-terminal system is a complex quantity equal to the ratio between the voltage signal applied to the two-terminal element and the corresponding current flowing through it, according to Ohm's law, impedance (Z) is frequency dependent and equal to the complex ratio of the AC voltage (V) over the current (I), as is described in Equation 1.1.

$$Z(f) = \frac{1}{Y(f)} = \frac{V_O sin(2\omega t + \phi)}{I_O sin(2\omega t)} = Re(Z) + jIm(Z) = R + jX \tag{1.1}$$

In Equation 1.1, the I_O and V_O are the injected current and recorded voltage signal amplitudes, as shown in Figure 1.1, t is time, ϕ is the phase difference between current and voltage (positive or negative, depending if an inductive or capacitive), Y is the admittance, $Re(Z)$ is the real part of the impedance, which is the resistance (R) and $Im(Z)$ is the imaginary part of the impedance, known as the reactance (X).

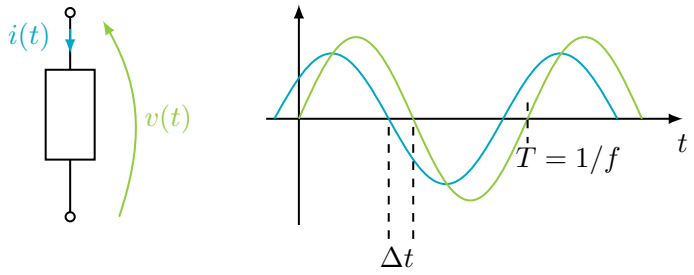
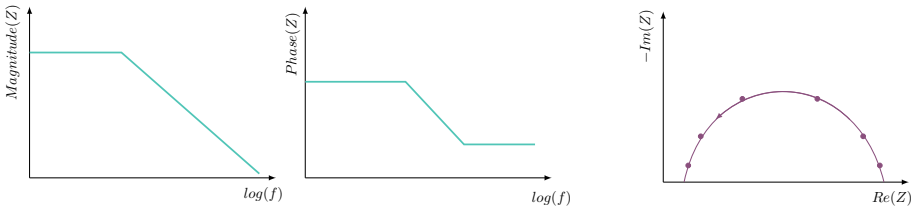


Figure 1.1: Definition of the impedance Z(f) of a two-terminal system

The Bode Plot and the Cole-Cole Plot are two standard tools for analyzing impedance in the frequency domain. The Bode plot (shown in Figure 1.2a) is graphical representation of the polar form of the frequency response of the analyzed system. This representation provides information on essential parameters such as cut-off frequency, resonance frequency, and system stability.



(a) (b)

Figure 1.2: Graphical representations of an impedance response. a) Bode Plot b) Cole-Cole Plot

The Cole-Cole Plot is a particular case of the Nyquist plot that decomposes the impedance value into its real and imaginary parts (calculated or measured over a range of frequencies), representing them as a set of points on a complex plane as is shown in Figure 1.2b). This representation helps to describe the behavior of nonlinear systems or those whose changes vary significantly with frequency. Additionally, it allows for showing the behavior of the time constants in the impedance, which correspond to semicircles in the complex plane.

1.2.2 Electrical Properties of Living Tissues

A specific conductivity σ and a relative permittivity ϵ_r can characterize every material. To incorporate the losses due to the dielectric and the frequency dependence of the material, the conductivity and permittivity are defined as complex quantities in the time domain, as shown in 1.2 - 1.5. [2] [10] Where $\hat{\sigma}(\omega)$ and $\hat{\epsilon}(\omega)$ are the complex conductivity and permittivity respectively.

$$\hat{\sigma}(\omega) = \sigma' + j\sigma'' \tag{1.2}$$

$$\hat{\epsilon}(\omega) = \epsilon' - j\epsilon'' = (\epsilon'_r - j\epsilon''_r)\epsilon_0 \tag{1.3}$$

where

$$\sigma'' = \omega\epsilon' \tag{1.4}$$

and

$$\epsilon'' = \frac{\sigma'}{\omega} \tag{1.5}$$

All living tissues are wet biological materials with DC conductivity because the ions are free and can migrate. [11] Polarization and the displacement of charges do not occur instantaneously when an electric field is applied, as shown in Figure 1.3. When the frequency is low enough, all charges in the tissue have the necessary time to change their position and then the polarization is maxima. While when the frequency increases the polarization and the permittivity decrease.[11] [12]

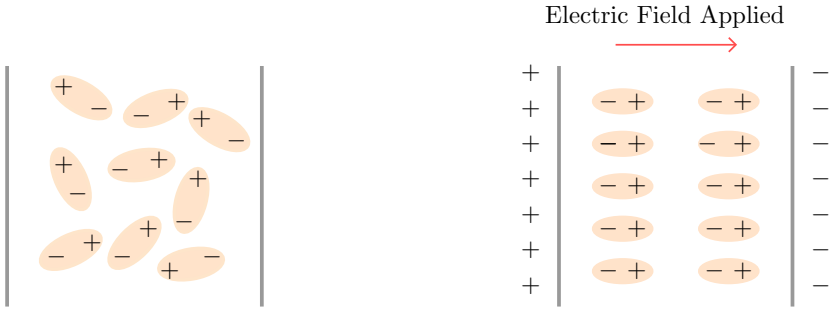


Figure 1.3: Polarization mechanism under the influence of an electric field

The time it takes for charges to change their position due to an increase or decrease in an induced electric field is known as **relaxation time**. [2] The dispersion mechanism can also be analyzed in frequency domain as a function of the permittivity of the material.

1.2.2.1 Dispersion and Dielectric Phenomena

In general, the tissue is an anisotropic medium due to the orientation of cells, macromembranes, and organs. A first approximation to the frequency behavior of biological tissues can be observed in [1], which proposed a distribution of time constants (DRT) for different tissues and biological fluids based on real measurements.
Equation 1.6 allows us to describe the frequency behavior of the tissue as a sum of the contributions of each variations in permittivity associated with the time constant, where α is the distribution parameter, τ is the relaxation time constant of the polarization mechanism, ϵ_∞ is the high frequency dielectric constant, σ is the static ionic conductivity. [1]

$$\hat{\epsilon}(\omega) = \epsilon_\infty + \sum_n \frac{\Delta\epsilon_n}{1 + (j\omega\tau_n)^{(1-\alpha)}} + \frac{\sigma}{j\omega\epsilon_0} \tag{1.6}$$

With the permittivity response, the complex conductivity and the tissue impedance can be calculated using Equations 1.7 and 1.8, respectively.

$$\hat{\sigma}(\omega) = j\omega\epsilon_0\hat{\epsilon}(\omega) \tag{1.7}$$

$$\hat{z}(\omega) = \frac{1}{\hat{\sigma}}(\omega) \tag{1.8}$$

The frequency response of permittivity for any tissue can be plotted using Equation 1.6 and the time constants defined in [1]. Figure 1.4 shows the MATLAB simulation of the frequency response for the permittivity and conductivity of muscle tissue (transversal).
In this response, as frequency increases, permittivity decreases nonlinearly. These changes occur primarily in three steps associated with dispersions defined in [13]: α defined in the range of Hz to kHz, β established in the range of hundreds of kHz to MHz, and finally γ at frequencies on the order of GHz. Table 1.1 details the biological

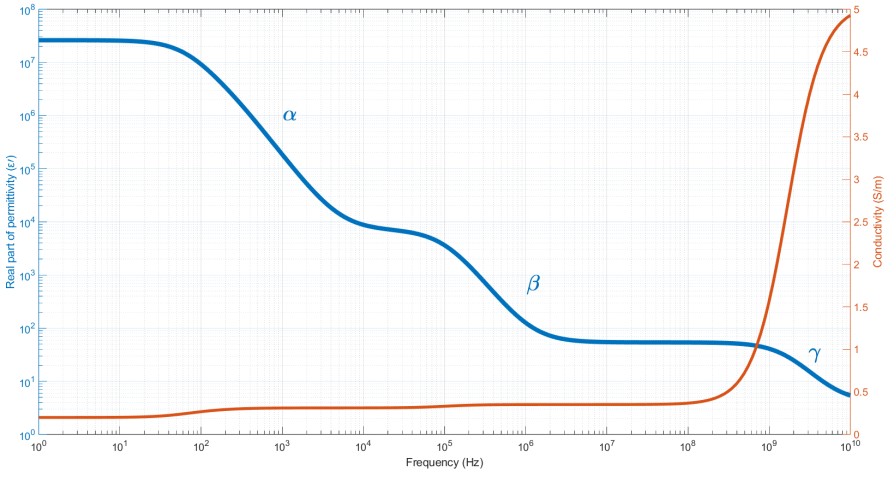


Figure 1.4: Dispersions illustrated in conductivity and permittivity spectra for muscle.[1]

mechanisms involved in each frequency range corresponding to the dispersions indicated in Figure 1.4. This information allows to define the frequency range within the characteristics of the tissue can be analysed.

Table 1.1: Biological mechanisms in dispersion regions [10]

Type	Characteristic Freq.	Mechanism
α	mHz - kHz	The dispersion is related with ionic diffusion gated cell membrane channels and cell membrane effects.
β	0.1 - 100M Hz	Protein molecule response, cell membrane polarizations relaxations and Maxwell-Wagner effects.
γ	0.1 - 100 GHz	Dipolar polarization mechanisms in polar media and the abundant tissue water.

1.2.2.2 Frequency Response of the Tissue

The effect of applying an external electric field (usually through a known current) is known as the **exogenic method** according to [10]. This method primarily involves the induced electric field displacing charges, forming dipoles, and polarizing the material [11]. Due to the anisotropy of biological tissues, the response to an induced electric field varies non-linearly depending on the frequency of the injected signal. Figure 1.5 shows two pathways through which the current can flow.

- **DC and Low Frequencies (green path)**: The medium where the cells are located acts as a resistance due to intracellular and extracellular fluids, causing current to flow around the cells.
- **High Frequencies (blue path)**: The capacitances associated with the cell membranes contribute a slight conductance, allowing for some conduction within the cells due to local conductivity.

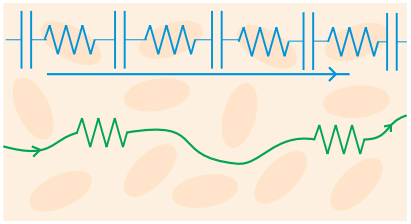


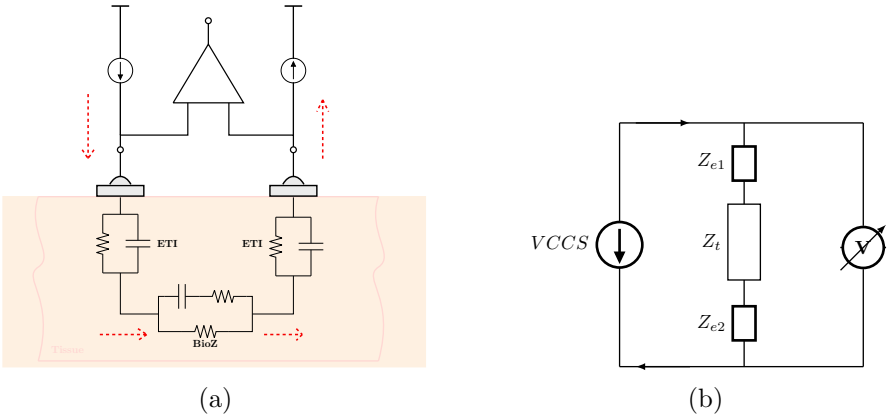
Figure 1.5: Low- and high-frequency current paths in tissue. [2]

1.2.3 Techniques for Measuring Tissue Impedance

Most impedance spectroscopy systems inject a constant current at different frequencies and measure the resulting voltage. Voltage measurement techniques are classified into bipolar and tetrapolar, the primary difference being the number of electrodes used.

1.2.3.1 Bipolar Technique

In this type of configuration, the current is injected through a pair of electrodes, and the resulting voltages are measured across the same pair of electrodes, as shown in Figure 1.6a, the equivalent circuit associated to the measurement system is shown in figure 1.6b.



(a) (b)

Figure 1.6: Bipolar Technique. a) Representation b) Equivalent circuit

In this configuration, the total measured impedance can be expressed as the sum of the impedance due to the tissue-electrode interface (denoted as Z_{e1} and Z_{e2}) and the impedance of the tissue under test as is expressed in Equation 1.9.

$$Z_{meas} = Z_{e1} + Z_T + Z_{e2} \tag{1.9}$$

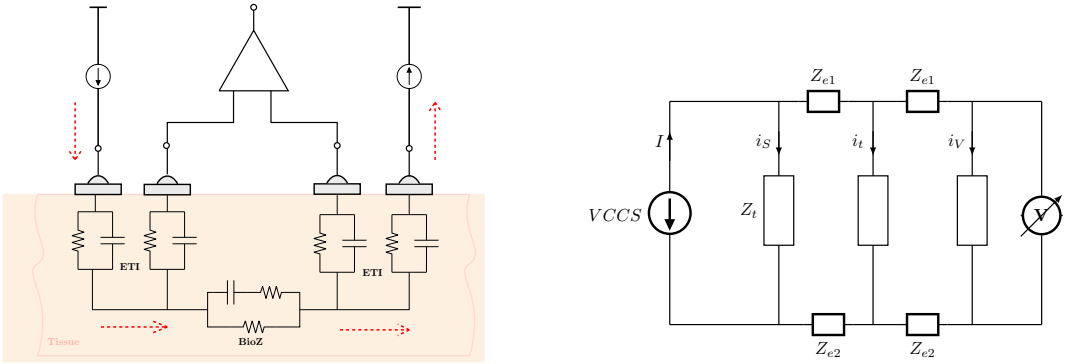
Assuming both electrodes are identical, then the measured impedance (Z_{meas}) can be expressed according to Equation 1.10

$$Z_{meas} = Z_T + 2Z_e \tag{1.10}$$

From expressions 1.9 and 1.10, it is evident that the influence of the electrodes is the main disadvantage in the measurement process because it is not possible to determine whether the measured variations in the voltage response are due to the tissue response (Z_t) itself or changes in the electrode impedance (Z_{e1}, Z_{e2}). Moreover, any noise signal originating from the current source directly affects the load, leading to undesired signals or measurement errors. [14]

1.2.3.2 Tetrapolar Technique

The tetrapolar technique involves using a different pair of electrodes for each stage, with two electrodes for current injection and two for measuring the voltage response, as shown in Figure 1.7.



(a) (b)

Figure 1.7: Tetrapolar Technique a) Representation b) Equivalent circuit

The equivalent circuit is shown in Figure 1.7b, and its impact on tissue measurement has been thoroughly analyzed and detailed in [14]. This analysis defines the concept of transfer impedance as the ratio of the resulting potential between the injection and measurement electrodes. As in shown in Equation 1.11, assuming that all electrode impedances are equal ($Z_{e1} = Z_{e2} = Z_{e3} = Z_{e4} = Z$).

$$T_Z = \frac{Z_t}{1 + Z_t \left[\frac{4Z + Z_V + Z_S}{Z_V Z_S}\right] + 2Z \left[\frac{2Z + Z_V + Z_S}{Z_V Z_S}\right]} \tag{1.11}$$

Ideally, it is possible to consider that the impedance due to the source Z_S and the impedance due to the voltage measurement Z_V tend to infinity; however, the design is limited by the parasitic capacitances connected to ground, particularly at very high frequencies. [14]

1.2.4 Electrode-Tissue Interface

The connection of the electrode to the tissue involves adding an impedance associated with both the electrode and the tissue interface, commonly referred to as ETI. In [15] and [3], an equivalent circuit model for the skin-electrode interface is proposed, associating resistance and capacitance with each tissue layer involved in the measurement process, as shown in Figure 1.8.

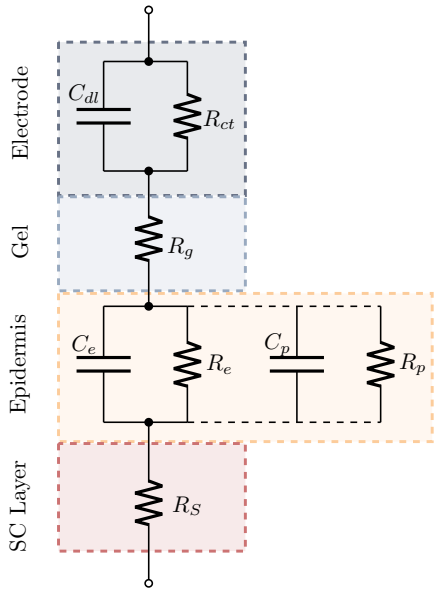


Figure 1.8: Complex circuit model for the skin-electrode interface considering electrode, electrode/skin contact, epidermis, and subcutaneous layers.[3]

For general purposes, it is possible to simplify the model in Figure 1.8 according to [16] to a simpler model, considering the half-cell potential of the electrode due to the charge distribution between the electrode material and its surface electrolytes caused by oxidation (V_{hc}). The electrical charges between the skin and the electrode are represented by the capacitance C_D, and the charge transfer in the conductive medium between the skin and the electrode is represented by R_D. The under-skin tissue resistance is represented by R_S.

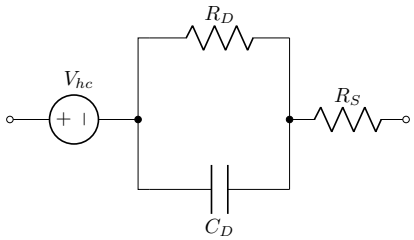


Figure 1.9: Equivalent circuit model for electrode-skin interface.

Therefore, the simplified impedance of the ETI results in the Equation 1.12.

$$Z_e = R_S + \frac{R_D}{1 + sC_D R_D} \tag{1.12}$$

This simplification allows for the characterization of the different types of electrodes that are clinically used. The Table 1.2 shows the mean values for Ag/AgCl, Orbital, and Stainless Steel electrodes according to [16].

Table 1.2: Mean values for typical electrodes used in medical applications

Electrode Type	R_D [kΩ]	C_D [nF]	R_S [Ω]
Ag/AgCl	215.82	18.9	399.7
Orbital	299.4	9.3	626.8
Stainless Steel	3289.4	4.9	856.4

Figure 1.10 shows the Cole-Cole plots simulated in MATLAB using the data from Table 1.2 for the electrodes analyzed in [16]. It can be observed that the electrode type with the highest impedance is Stainless Steel, whose response is at least 10 times greater compared to Ag/AgCl and Orbital electrodes.

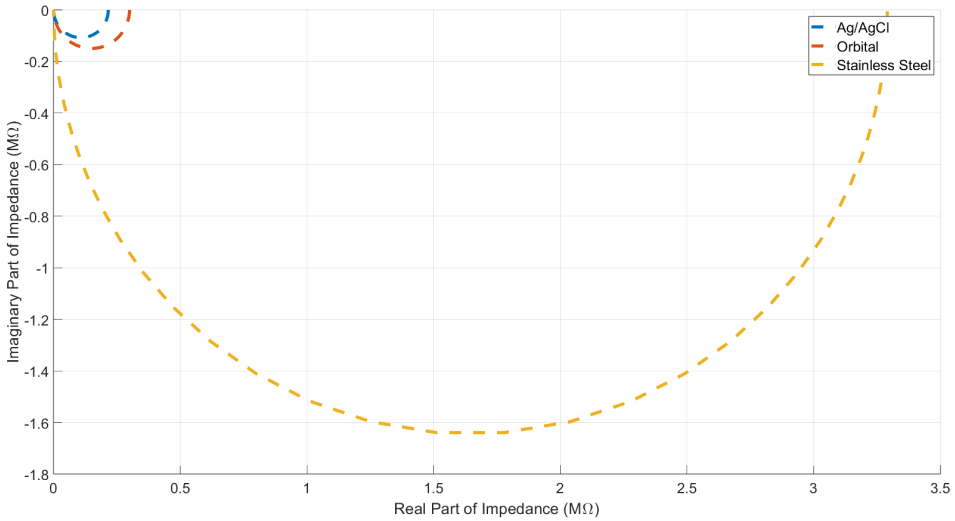


Figure 1.10: Comparison of the impedance response for each electrode type

The correct choice of electrodes improves the acquisition of the biological signal to be measured. Otherwise, a high electrode-skin impedance would result in poor biological signal quality, low signal amplitude, and low signal-to-noise ratio. [16]

1.2.5 Applications of Bio-Impedance in Biomedical Monitoring

In recent years, non-invasive monitoring techniques have gained clinical relevance for accurately detecting diseases. In this context, Bio-Impedance measurement has emerged as a prominent approach.[17] It has been demonstrated that Bio-Impedance monitoring through various methods holds significant clinical applications as is detailed shown in Figure 1.11. [4]

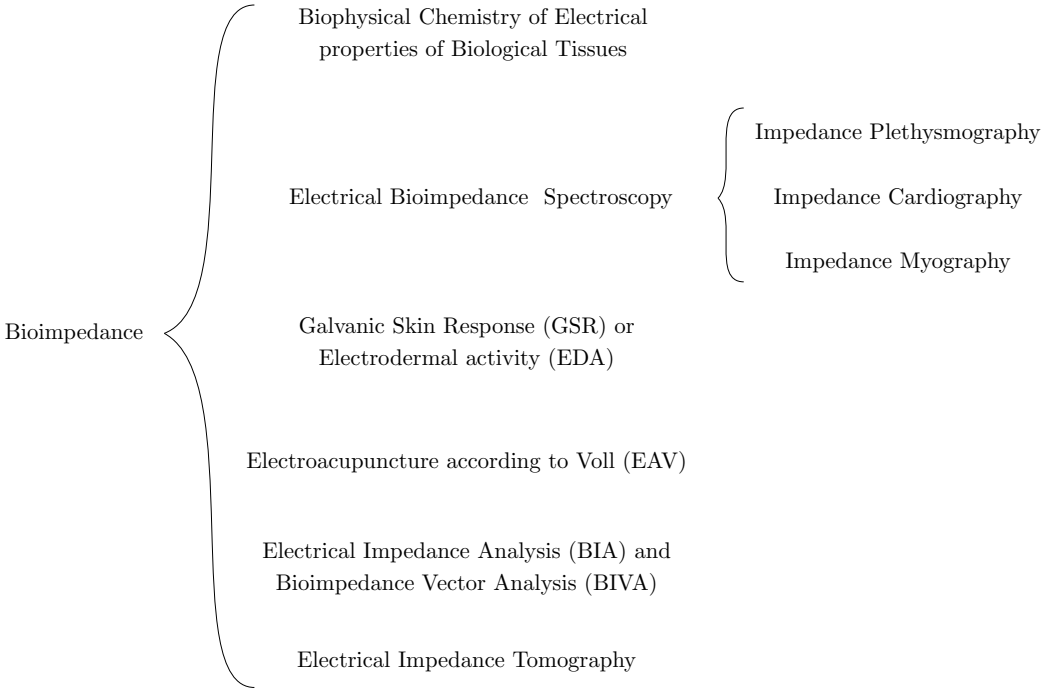


Figure 1.11: Different branches of Bio-Impedance Anaysis in human clinical studies. [4]

According to Table 1.3, body composition analysis typically utilizes frequency ranges from 50 kHz to 1 MHz in Bio-Impedance spectroscopy (BIS) applications. This frequency range is selected because, at these frequencies, the impedance of the cell membrane predominates, enabling precise measurements of intracellular and extracellular fluid volumes.
Although the amplitude of the applied current is generally very low (typically ranging from μA to mA) [18] recommends a current value of 800 μA. Furthermore, studies have demonstrated a strong correlation between BIS and multiple dilution techniques for assessing total body water (TBW).
In [19], a measurement technique operating at specific frequencies: 5, 50, and 250 kHz, this was proposed to analyze segmental phase angles for diagnosing diabetes-mellitus in individuals. On the other hand, other studies have focused on narrower frequency ranges, such as 455.5 kHz for electrical measurements [20]. Additionally, [21] explored a broader frequency range, from 10 kHz to 100 kHz, for bio-impedance measurement

applications. For heart rate applications, the frequency operations region in this study refers to the use of a 30 kHz frequency to inject a current of 1 mA for Bio-Impedance measurements on the participants. [22] Other authors [23] validate the use of BIS to heart rate applications using commercial devices.
In [24], the frequency range analysis focused on applying an alternating signal with frequencies ranging from 100 Hz to 0.1 MHz to measure the impedance parameters of subjects' skin. This study demonstrated significant differences in resistance, capacitance, and phase measurements between hydrated and dehydrated states, highlighting the potential of bio-impedance analysis to classify hydration status. A commercial bio-impedance analysis device was utilized for the measurements, and the summarized data in Table 1.3 was extracted from the manufacturer's datasheet.
Besides, [25] suggests that for accurate hydration parameter measurements, it is advisable to operate within a frequency range of 1 kHz to 1 MHz, as noted in [10]. This analysis typically applies a current in the range of 500–800 μA and emphasizes that the distance between the signal and detection electrodes should be at least 5 cm to minimize measurement errors.
Advanced applications employ bio-impedance as an alternative method to tomography or as an imaging tool by using an array of electrodes placed over the region of interest. These systems map the measured impedance values to associated colors, enabling visual representation. The selection of the operating frequency range depends on the specific application within the human body and the desired trade-off between spatial resolution and penetration depth.
In general, Electrical Impedance Tomography (EIT) systems tailor their operating frequency range to the specific tissue being imaged, considering factors like the impedance of the tissue, size of the region of interest, and the desired imaging depth. [26] [27] In EIT systems, the number of electrodes used for data collection is critical for image resolution. Common configurations include systems with 8, 16, 32, 64, or even 128 electrodes.

Table 1.3: Summary of monitoring applications of Bio-Impedance with key parameters and references.

Analysis	**Frequency Range**	**Current Applied**	**Electrode Distance**	**References**
Body Composition	50 kHz - 1 MHz	800 μA	4 - 7 cm (S.A.)	[28], [18], [29]
Glucose Analysis	Multi-frequency	Not mentioned	5 cm (S.A.)	[19], [20], [21]
Heart Rate	30 kHz - 50 kHz	1 mA	Variable ($\leq$ 10 cm)	[22], [23]
Hydration Assessment	5 kHz a 100 kHz	620 μA, 500 - 800 μA	5 cm	[24], [25], [30]
EIT	10 Hz a 10 MHz	10 μ - 1 mA	Circular matrix	[27], [26]

S.A.: Segmental Analysis
Commercial Device (Bodystat Multiscan 5000 ©)

1.3 Adquisition System Proposal

The impedance behavior can be described in terms of magnitude and phase using topologies such as Peak Detector or Rectification and low-pass filter (LPF) applied to the signals acquired by the instrumentation amplifiers [31], [32]. Other topologies propose Synchronous Sampling at points where the injected signal is at its zero and maximum values, allowing the calculation of the real and imaginary parts of the impedance within a single channel [33], [34], [35]. Additional structures suggest a bridge-based method, consisting of the unknown impedance (typically the Tissue Under Test) in series with a known impedance, which can be adjusted to balance the response of the current applied to the load [36], [37], [38].
The topology considered for signal measurement is the one proposed in [5] due to the simplicity. This topology allows for reading and recording data on current, voltage, and phase difference throughout the measurement process. The reference resistor (R_{REF}) is used to ensure that the current measured by the data acquisition system accurately reflects the current injected into the sample.

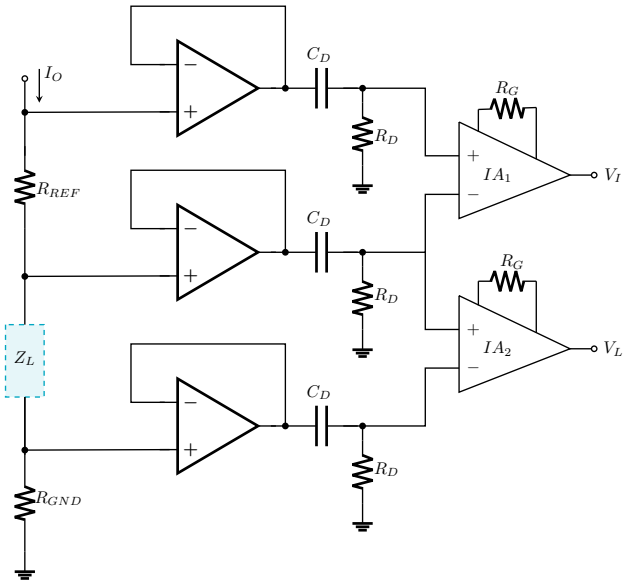


Figure 1.12: Signal Conditioning System for Bio-Impedance Measurement. [5]

The structure of the Bio-Impedance spectroscopy measuring system shown in Figure 1.12 can be explained as follows:

- The buffer is an isolation circuit, it serves to ensure that the current and voltage signals are not affected by the circuit afterwards.
- The RC circuit after buffer forms a high pass filter (HPF) set at 10 Hz cut-off frequency to eliminate DC-offset voltage.
- The IA is used to convert the differential signal to single ended, by amplifying the signals (G_1 and G_2) through R_G selection.

- The value of the actual current I_Z is the voltage on the reference resistor divided by the value of the reference resistor R_{REF}.

The output signals correspond to the reference voltage signals (the voltage generated by the resistance R_{REF} and the input current I_Z) and the voltage generated by the load impedance (Z_L), thus input current I_Z indirectly through V_I using the Equation 1.13

$$|I_Z| = \frac{|V_I|}{G_1 * R_{REF}} \tag{1.13}$$

Where G_1 corresponds to the gain of the instrumentation amplifier (IA_1), and the voltage measured across the load is across V_L using the Equation 1.14

$$|V_Z| = \frac{|V_L|}{G_2} \tag{1.14}$$

Similarly, G_2 is the gain of the instrumentation amplifier (IA_2), so that the impedance of the load can be calculated as shown in Equation 1.15.

$$|Z_L| = \frac{|V_L|}{|I_Z|} \tag{1.15}$$

And therefore, the phase shift of the signals is measured through V_I and V_L as is explained in Equation 1.16.

$$\theta_L = \theta_{VL} - \theta_{VI} = 360^\circ \frac{\tau}{T} \tag{1.16}$$

Where τ is the time delay between the signals V_L and V_I, T is the period of the I_Z signal.
The resistive part (associated with $Z_{L,Re}$) and the reactive part (associated with $Z_{L,Im}$) of the load impedance can be calculated using the Equations 1.17 and 1.18.

$$Z_{L,Re} = |Z_L| \cos(\theta_L) \tag{1.17}$$

$$Z_{L,Im} = |Z_L| \sin(\theta_L) \tag{1.18}$$

To verify the considered system and the macromodelling, 2 different loads are considered and shown in Figure 1.13. For the first case (Fig. 1.13a)), the analysis focuses on the combination of resistive and capacitive elements, with proposed values of $R_{L2} = 4.7$ kΩ and $C_{L2} = 2.2$ nF, the second case (Figure 1.13b)), an equivalent electrical tissue model is employed, as detailed in [39].
The expression of the characteristic impedance in each case of Fig. 1.13 is described through Equations 1.19 - 1.20.

$$Z_A(f) = \frac{R_{L2}}{1 + (2\pi f R_{L2} C_{L2})^2} - j \frac{2\pi f R_{L2}^2 C_{L2}}{1 + (2\pi f R_{L2} C_{L2})^2} \tag{1.19}$$

$$Z_B(f) = R_{L3} + \frac{R_{L2}}{1 + (2\pi f R_{L4} C_{L3})^2} - j \frac{2\pi f R_{L4}^2 C_{L3}}{1 + (2\pi f R_{L4} C_{L3})^2} \tag{1.20}$$

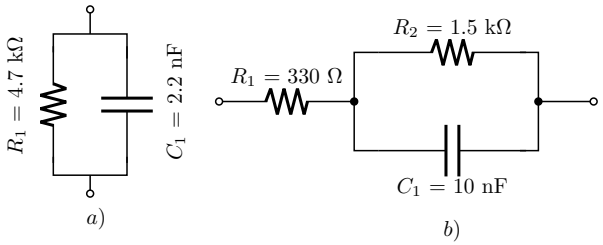


Figure 1.13: Devices Under Test

In this way, the magnitude and phase of each load, can be calculated using the rectangular form expressed in Equations 1.17 - 1.18.

$$|Z_L| = \sqrt{Z_{L,Re}^2 + Z_{L,Im}^2} \tag{1.21}$$

$$\theta_L = \arctan\left(\frac{Z_{L,Im}}{Z_{L,Re}}\right) \tag{1.22}$$

The response is compared against the measurements obtained from the proposed system to validate the model defined by Equations 1.19 and 1.19 for each case. Figure 1.14 presents the Cole-Cole plot of the simulated results for each scenario.

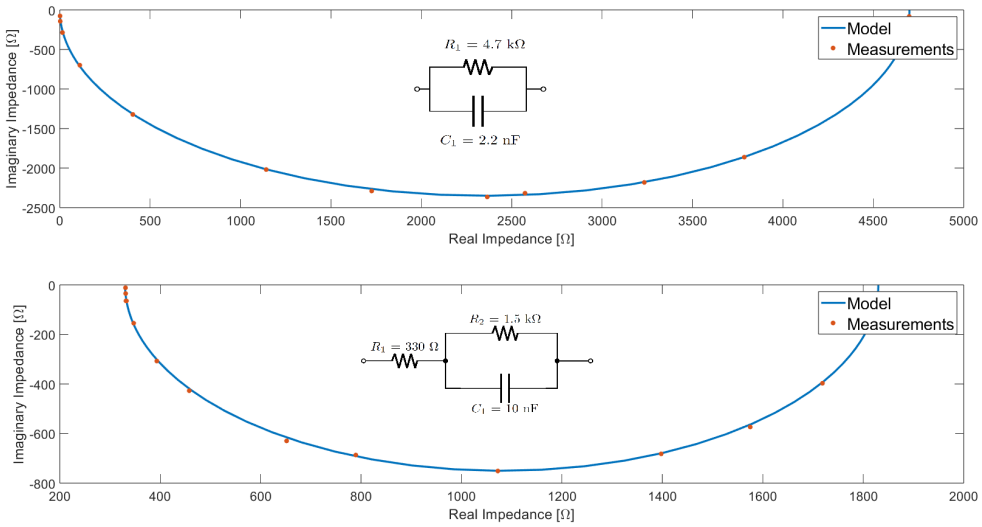


Figure 1.14: Cole-Cole Plot Response of model and measurement for DUT in Figure 1.13

1.4 Conclusions

Bio-Impedance Spectroscopy (BIS) systems are specialized devices developed to measure and extract the electrical properties of biological tissues, subsequently converting these properties into digital data for further analysis. The importance of BIS systems lies in their expanding role within the growing field of non-invasive medical monitoring, which offers significant potential for real-time health assessment and management.
Throughout this chapter, the relevance of BIS systems has been evaluated and detailed, highlighting their application as a wearable alternative for various body measurement. This analysis not only underscores the advantages of BIS technology but also delineates the current landscape of its applications, offering insights into the specific measurement parameters considered in each use case.
The responsible for generating signals within the frequency range of interest is the Back-End stage which poses a significant challenge due to the wide range it must cover, requiring a robust and versatile design. On the other hand, the Front-End stage is an essential component in the measurement process, as it ensures the accurate acquisition of the signal response. For both stages, it is crucial to perform macromodeling to define the necessary specifications and validate the integrated operation of all blocks, ensuring system coherence and reliability.
Specifically, the performance of the instrumentation amplifier (IA) plays a decisive role in the overall accuracy and reliability of the Bio-Impedance System. Parameters such as adjustable gain range, bandwidth, and common-mode rejection are critical to achieving high-fidelity measurements under varying physiological conditions. Similarly, other essential blocks, such as signal generators, play a key role in enabling precise system operation and characterization, ensuring that the design and performance requirements are met.

CHAPTER 2

Signal Generation Proposals

This chapter propose two solutions to signal generation within the dispersion range β. The first employs a QFGT-modified Ring Oscillator operating in Weak Inversion region offering kilohertz-range signals with a dual control via feedback factor β and the tuning voltage V_{Tune}. The second approaches the advantages of digital synthesis using a DDS with signal compression, reducing the sizing of the memory due to the discretization. Both methods ensure a compact design and reliable signal generation.

2.1 Oscillators

Oscillators are essential components in every electronic system and are responsible for generating periodic signals autonomously. They can be classified into non-resonant and resonant types. Non-resonant oscillators, such as delay lines and ring oscillators, do not rely on resonant elements, which are widely used in CMOS digital applications due to their simplicity [7]. Resonant oscillators, including crystal-based and LC tank types, leverage resonant circuits to ensure frequency stability, making them ideal for high-precision applications like telecommunications [40]. The choice between these oscillators depends on factors such as frequency stability and application-specific requirements.

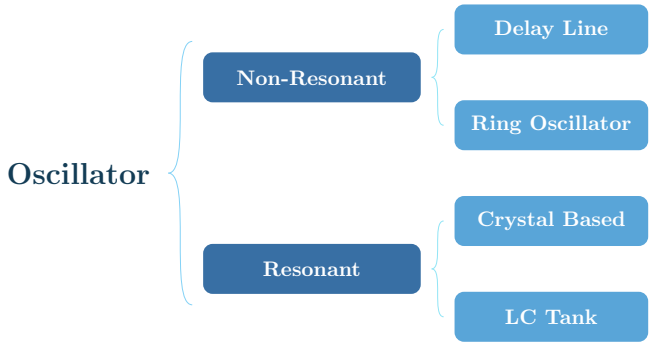


Figure 2.1: Classification of the different types of oscillators

2.1.1 Ring Oscillators

A ring oscillator is composed of an odd and even number (N) of open loop inverting amplifiers or delay cells (or stages) coupled in a positive feedback loop [6]. When an initial condition excites the Ring Oscillator, the propagation signal passes through the chain of N delay cells, resulting in a total delay of $2Nt_p$ to complete one period (T_{osc}), where t_p is the propagation time of a single delay cell, as shown in Equation 2.1.

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{2Nt_p} \tag{2.1}$$

From the Equation 2.1, it is possible to denote that the oscillation frequency is determined by the propagation time t_p of each stage and the number of stages of the Ring Oscillator (denoted as N).

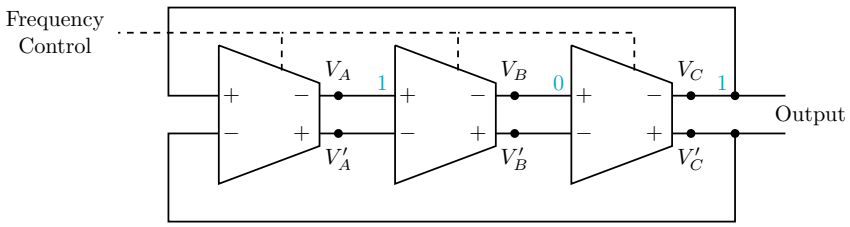


Figure 2.2: Basic topology of a three-stage ring oscillator

For every single cycle, there are downward and upward transition, and each delay cell's intrinsic propagation delay times, high-to-low (t_{PHL}) and low-to-high (t_{PHL}), are associated with those transitions. Figure 2.3 shows the corresponding waveform of the 3-stages Ring Oscillator shown in Figure 2.2. V_A represents a differential signal oscillating between high and low logic levels and shows the three key points associated to each transition in time domain, denoted as **Edge** X_1, **Edge** X_2, and **Edge** X_3.

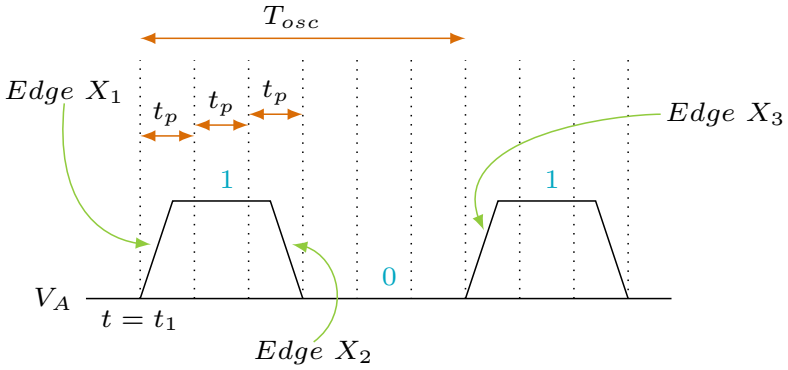


Figure 2.3: Time domain response of 3-stages RO of Figure 2.2. [6]

The total oscillation period, denoted as T_{osc}, is the time required for the signal to return to its original state after propagating through the three stages. In figure 2.3, T_{osc} is defined as the interval between two equivalent edges, for example, between **Edge** X_1 and the subsequent edge after the signal has passed through the three stages.

2.1.2 Delay Cell Types

When comparing and classifying types of delay cells used in ring oscillators, several approaches are highlighted in recent research, focusing on key factors such as power consumption, phase noise, tuning range, and robustness against process variations.

- **Inverter-based Delay Cells:** Inverter-based delay cells are the most used in ROs due to their simplicity and efficiency in area. These cells introduce a delay through each inverter, determined by the load capacitance and channel resistance. These cells are well-suited for CMOS integration and are preferred in low-power applications where simplicity and cost-efficiency are critical [41] [42].
- **Dual-Delay-Path Cells:** These cells provide better control over the oscillation frequency by utilizing two separate delay paths. This architecture allows for more precise tuning of the oscillation frequency and offers improvements in phase noise performance. They are particularly useful in high-frequency applications where linearity and frequency stability are required [42].
- **Differential Delay Cells:** Differential delay cells are designed to minimize noise and increase frequency range. These cells are often used in high-performance RF circuits and systems due to their superior noise immunity and wide frequency tuning capabilities. Additionally, they offer better control over phase noise, making them ideal for communication systems [43] [41].
- **Voltage-Controlled Delay Cells:** Voltage-controlled delay cells are used in voltage-controlled oscillators (VCOs), where the oscillation frequency is adjusted by an external voltage. These cells are common in phase-locked loops (PLLs) and data converters, where a precise control of frequency is necessary. They are also advantageous in low-power designs requiring wide frequency tunability [41]

2.1.2.1 Maneatis Cell

The Maneatis cell was first introduced in 1993 [44]. It is a delay cell consisting of an nMOS differential amplifier ($M_{1,2}$) with pMOS triode loads ($M_{3,4}$) in parallel with a current source ($M_{5,6}$). By adjusting the control voltage (V_{Tune}), transistors $M_{5,6}$ modify the total current through the differential pair, thereby allowing the oscillation frequency to increase or decrease.
A detailed description of the function of each stage indicated in Figure 2.4 is provided below:

- M_B **Transistor**: operates as the bias transistor of the delay cell (also known as the Tail Current).
- M_1 **and** M_2 **Transistors**: these transistors function as the input differential pair.
- M_3 **and** M_4 **Transistors**: they serve as the load for one of the output branches, where M_3 is a transistor connected as a diode, and M_4 acts as a voltage-controlled current source regulated by V_{Tune}.

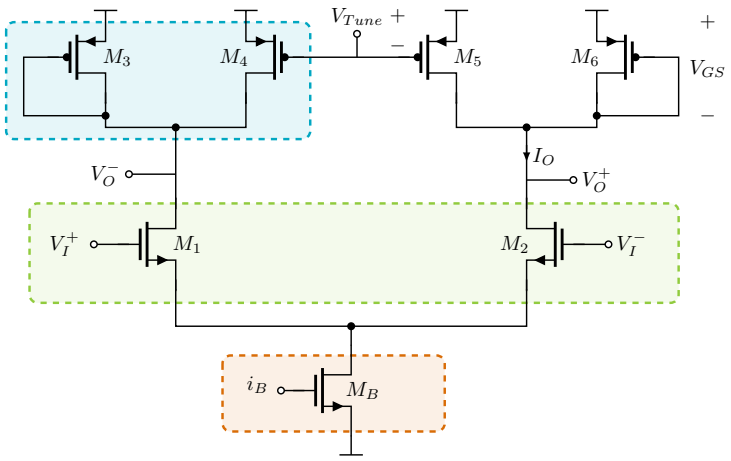


Figure 2.4: Basic structure of the Maneatis Cell (**Topology A**)

This cell is referred to as symmetric load because the current-to-control voltage relationship is symmetric with respect to the midpoint of the voltage excursion, as shown in Figure 2.5. Figure 2.5 illustrates the ideal I-V characteristics of symmetric loads at low (labeled as I in Figure 2.5b) and mid-range (labeled as II) bias voltages. With the upper supply acting as the maximum swing limit, the lower swing limit is symmetrically positioned at the bias level of the pMOS transistor, V_{Tune}. The dashed lines represent the effective resistance of the load and highlight the symmetry of their I-V characteristics.

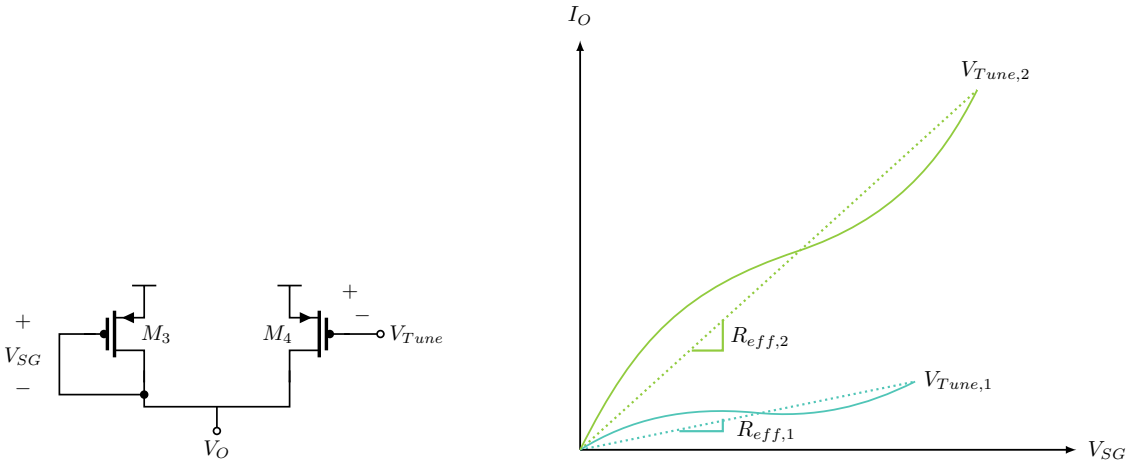


Figure 2.5: DC characterization of the Maneatis Cell. a) Load structure b) Characteristic I-V curve

The delay time generated by the Maneatis Cell is primarily determined by the capacitive and resistive elements of the load. Thus, the delay of the cell is given by expression 2.2.

$$\tau = R_{eff} \cdot C_{eff} \tag{2.2}$$

Where R_{eff} is the inverse of the transconductance and can be easily obtained from its definition, as shown in expression 2.3

$$g_m = \frac{\partial i_D}{\partial V_{GS}} \tag{2.3}$$

Due to the applications of ring oscillators involve high frequencies, it is very common for the transistors in the delay cells to operate in strong inversion (also known as the saturation region). Therefore, the Drain Current (I_D) is expressed as

$$I_D = \frac{1}{2}\mu_{n,p}C_{OX}\frac{W}{L}(V_{GS} - V_{Th})^2 \tag{2.4}$$

Therefore, the transconductance is obtained by applying 2.3 to 2.4, and specifically for the pMOS load transistors, it results in Equation 2.5

$$g_m = \mu_p C_{OX}\frac{W}{L}(V_{GS} - V_{Th}) \tag{2.5}$$

The AC gain of the cell is given by the Equation

$$A_V = \frac{g_{m1}}{g_{m3} + g_{DS1} + g_{DS3} + g_{DS4}} \tag{2.6}$$

The ring oscillator configuration implies that the delay cell uses a load with these characteristics. Therefore, the circuit bandwidth will be determined by

$$\omega_O = \frac{g_{m3} + g_{DS1} + g_{DS3} + g_{DS4}}{C_{GS1} + C_{GS3} + C_{DB1} + C_{DB3} + C_{DB4}} \tag{2.7}$$

From expressions 2.6 and 2.7, it is possible to obtain the gain-bandwidth product, as shown in the equation

$$\omega_T = \frac{g_{m1}}{C_{GS1} + C_{GS3} + C_{DB1} + C_{DB3} + C_{DB4}} \tag{2.8}$$

2.1.3 DPI/SFG Analysis

The systematic method of circuit and system analysis, Driving Point Impedance / Signal Flow Graph, proposed by [45], allows using signal flow graphs as a visual and mathematical tool to model their interaction, enabling the decomposition and simplification of complex circuit analysis. The driving-point impedance methodology was first introduced by [46]. This method addresses the problem by dividing it into two more manageable sub-circuits, which are later synthesized to construct the complete solution of the original system.

- **Short Circuit Current:** An AC ground short is imposed at the desired output node "x", and the current that flows through this short is calculated, commonly referred to as the short-circuit current, I_{scx}.

- **Driving Point Impedance:** In this sub-circuit, the equivalent impedance (known as the "Driving Point Impedance") seen from the node of interest "x" (DPI_x) is calculated.

Therefore, the voltage seen at node "x" can be easily calculated as

$$V_X = I_{SC,x} \cdot DPI_x \tag{2.9}$$

In this work, the DPI/SFG method has been applied to the analysis of the Maneatis delay cell. To simplify the analysis, the output resistances involved in each of the transistors composing the topology described in Figure 2.6 are considered.

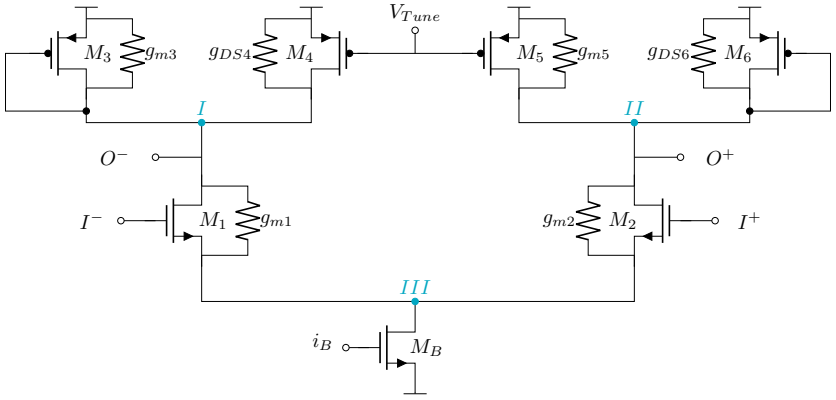


Figure 2.6: Resistances associated with the transistors for the DPI/SFG analysis

The impedance seen at node I is described as detailed in Equation 2.10, by considering that the contribution due to g_{DS3} and g_{DS1} is negligible.

$$DPI_1 = (g_{m3} + g_{DS4})^{-1} = r_{O1} \tag{2.10}$$

The short-circuit current at the same node is given by the transconductance of the input differential pair as is shown in 2.11.

$$I_{SC,1} = V_{III}(g_{DS1} + g_{m1}) - V_{I^+} g_{m1} \tag{2.11}$$

Due to the symmetry of the topology, the short-circuit current (and impedance) seen at node II is analogous to Equations 2.11 and 2.10, respectively.

$$DPI_2 = (g_{m6} + g_{DS5})^{-1} = r_{O2} \tag{2.12}$$

$$I_{SC,2} = V_{III}(g_{DS2} + g_{m2}) - V_{I^-} g_{m2} \tag{2.13}$$

Finally, the total short-circuit current at node III is the sum of the contributions from both branches; thus, the total current is given by Equation 2.14.

$$I_{SC,3} = V_{I^+} g_{m1} + V_{I^-} g_{m2} \tag{2.14}$$

The impedance at node III is described in Equation 2.15.

$$DPI_3 = (g_{DS1} + r_O^{-1})^{-1} \tag{2.15}$$

Expressions 2.10 - 2.15 establish the corresponding Signal Flow Graph (SFG) shown in Figure 2.7. To illustrate the relationship between the equations and the SFG, each current (or voltage) generation is marked by its respective expression: for instance, $V_{I^+}g_{m1}$ and $V_{I^-}g_{m2}$ are indicated in blue, and according to Equation 2.14, both are represented as a summation point whose result is I_{SC3}.

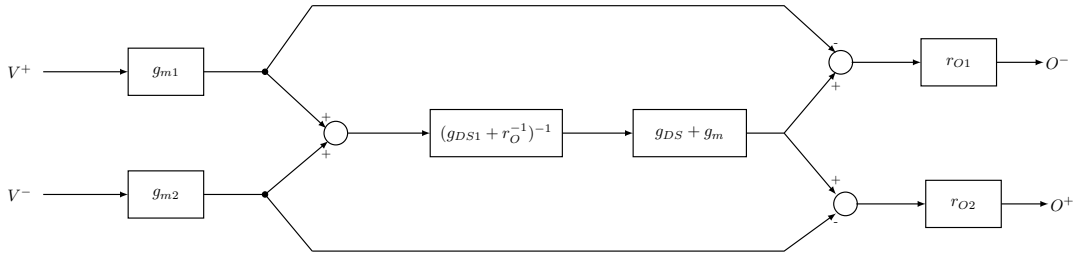


Figure 2.7: Resulting SFG from the DPI analysis of the Maneatis Cell (**Topology A**)

The SFG allows to describe the following points:

- **Differential Input (V^+, V^-):** The signals V^+ and V^- pass through transistors M_1 and M_2 with transconductance gains of g_{m1} and g_{m2}, respectively.
- **Short-Circuit Current (I_{SC}):** A short-circuit current is generated at node I, which is influenced by the transconductance terms and the g_{DS} conductances, in addition to the output resistance r_o.
- **Impedance Z_{III}:** Node III demonstrates how the circuit combines differential conductance and the impedances $g_{DS} + g_m$. This node is crucial for determining the frequency response of the circuit.
- **Differential Output (V_O^+, V_O^-):** The signals O^+ and O^- are obtained through the load resistances r_{o1} and r_{o2}, which help stabilize the signals and minimize distortion.

2.1.4 Quasi-Floating Gate Transistors

The structure of the Quasi-Floating Gate Transistor (QFGT) is shown in Figure 2.8. In this modification, the gate of the transistor functions as a weighted summation point, dependent on the weighting of the gate capacitors. This topology is called with the prefix "Quasi" because there is an nMOS (or pMOS) transistor connected to V_{DD} (or V_{SS}) through a reverse-biased diode-connected transistor, which acts as a large-value resistor, thus maintaining the operating point.

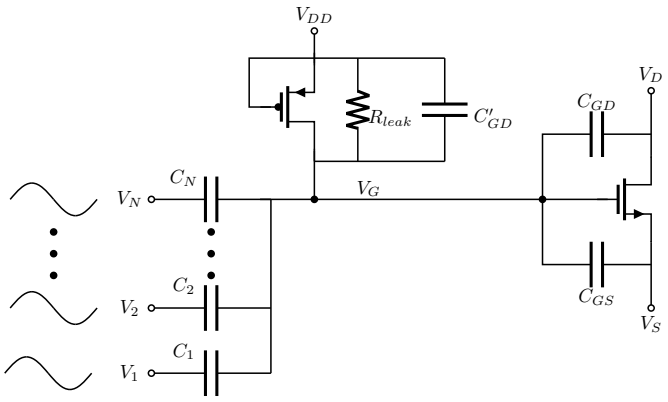


Figure 2.8: Structure of a Quasi-Floating Gate Transistor (QFGT) capacitively coupled

The voltage at the gate of the QFGT (V_G) is described in Equation 2.16, where C_{Total} is the total capacitance seen at the gate, primarily composed of the parasitic capacitances of the QFGT and the capacitances associated with the signals as shown in Equation 2.17.

$$V_G = \frac{sR_{leak}C_{Total}}{1 + sR_{leak}C_{Total}} \tag{2.16}$$

$$C_{Total} = \sum_{i=1}^{N+1} C_i + C_{GS} + C_{GD} + C'_{GD} \tag{2.17}$$

Therefore, the voltage seen at the input will correspond to the sum of the capacitive divider of the input signals (weighted by C_i) and the contributions from the voltages V_D and V_S, resulting in the following expression as shown in Equation 2.18.

$$V_{in} = \frac{1}{C_{Total}} \left(\sum_{i=1}^{N+1} C_i V_i + C_{GS} V_S + C_{GD} V_D \right) \tag{2.18}$$

The weighted sum of the signals through the QFGT can be either capacitive or resistive. In this design proposal, resistors were chosen (as shown in Figure 2.9); however, the analysis is similar to the capacitive case.

The voltage at the gate V_G is determined by the voltage divider formed by R_{leak} and R_{Total}, as shown in Equation 2.19.

$$V_G = \frac{R_{Total}}{R_{leak} + R_{Total}} \tag{2.19}$$

Where R_{Total} is given by Equation 2.20

$$\frac{1}{R_{Total}} = \sum_{i=1}^{N} \frac{1}{R_i} \tag{2.20}$$

Thus, the input voltage V_{in} will be the sum of the voltages across each resistor, with each signal weighted by the conductance of each individual resistance:

$$V_{in} = R_{Total} \cdot \left(\sum_{i=1}^{N} \frac{V_i}{R_i} \right) \tag{2.21}$$

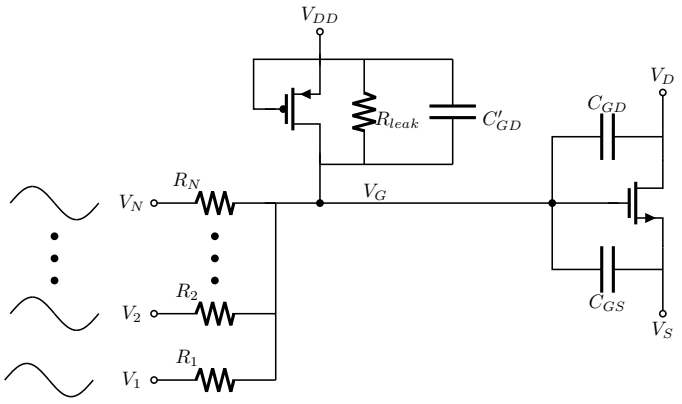


Figure 2.9: Structure of a quasi-floating gate transistor (QFGT) resistively coupled

2.1.5 Voltaje Follower Structure

The source-coupled differential pair configuration offers a significant reduction in output resistance, making it ideal for driving capacitive loads and ensuring stable voltage outputs across varying input conditions. As illustrated in Figure 2.10, the topology demonstrates a high gain-bandwidth product, enabling rapid response to changing input signals while maintaining low output impedance. These attributes highlight the effectiveness of the voltage follower in applications requiring signal buffering, impedance matching, and reliable isolation between circuit components.

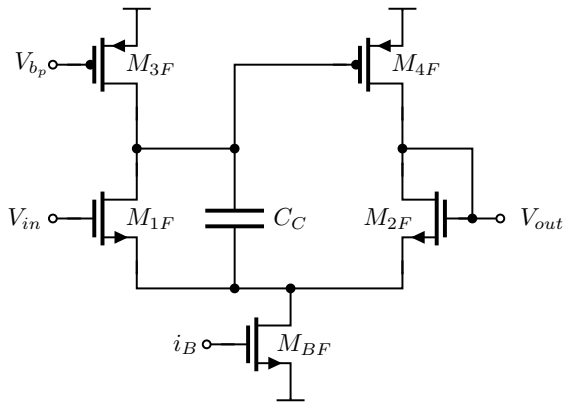


Figure 2.10: Structure of the Voltage Follower Block

Due to its follower topology, the voltage transfer gain (A_0) is affected by a small error ϵ [47] denoted by the Equation 2.22

$$A_0 = \frac{1}{1+\epsilon} \tag{2.22}$$

Assuming that transistors M_{1F} and M_{2F} are well-matched, the gain error for the unity-gain amplifier is mainly function of the input transistor (M_{1F}) and the load pMOS

transistor M_{2F} as detailed in Equation 2.23.

$$\epsilon \approx \frac{g_{DS3F,4F} + g_{DS1F,2F}}{g_{m1F,2F}} \tag{2.23}$$

The amplifier's frequency performance depends on its damping factor and the pole frequency ω_O, as shown in the Equations 2.24 - 2.25 respectively.

$$\xi = \frac{1}{2}\sqrt{\frac{C_C}{C_L}\frac{g_{m4}}{g_{m1}}} \tag{2.24}$$

$$\omega_O = \sqrt{\frac{g_{m1,2}g_{m4}}{C_C C_L}} \tag{2.25}$$

The compensation capacitor can be calculated from the expression in Equation 2.24, as shown in Equation 2.26, where primarily depends on the transconductance of the input/output transistors and the damping factor ξ.

$$C_C = 2\xi^2 \frac{g_{m1,2}}{g_{m4}} C_L \tag{2.26}$$

2.1.6 Voltage Follower-modified Maneatis Cell

Phase degeneration was previously mentioned in [48] and [49]; however, the proposal is revisited in this work as an alternative for generating signals that enable the analysis of Bio-Impedance Spectroscopy over the broadest possible frequency range. For this purpose, a pseudo-diode configuration is considered, now taking into account that the Gate-Drain connection includes a voltage follower element, as shown in the topology of Figure 2.10.

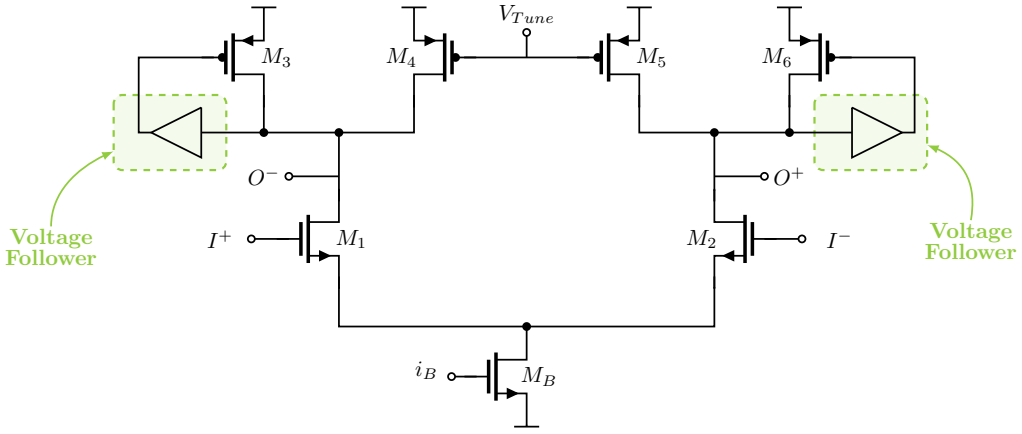


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Figure 2.11: Structure modified Maneatis Cell using Voltage Follower (**Topology B**)

Although ideally V_{SG} remains constant (due to the DC response of the Voltage Follower) this modification allow to decouple the drain of the M_3 transistor and its gate terminal for further modifications.

2.1.7 Maneatis Cell with Phase Degeneration using Internal Feedback Networks

The Phase degeneration networks constitute feedback pathways that alter the phase of the system. Their operation within the circuit can be described as follows:

- **Feedback Pathways**: In the circuit, two feedback pathways directed toward the load are established, facilitated by the implementation of quasi-floating gate transistors.
- **Feedback Weighting**: The feedback signals can be weighted, allowing for greater significance to be assigned to one feedback pathway over the other, depending on the stability requirements of the system. This weighting is crucial for adjusting the dynamic behavior of the system.
- **Impact on the Transfer Function**: Depending on the weighting of the feedback signals, the location of the poles in the transfer function can be modified, which in turn causes a change in the phase of the system and, consequently, in the stability of the cell delay.

As previously mentioned, this work addresses Phase Degeneration through the positive feedback of weighted signals via a Quasi-Floating Gate Transistor (QFGT) using resistors. The proposed topology is illustrated in Figure 2.12, where the feedback resistive network is used to implement the signal weighting. Distinct color blocks are used to differentiate the feedback pathways, highlighting the two outputs labeled V_O^+ and V_O^-.

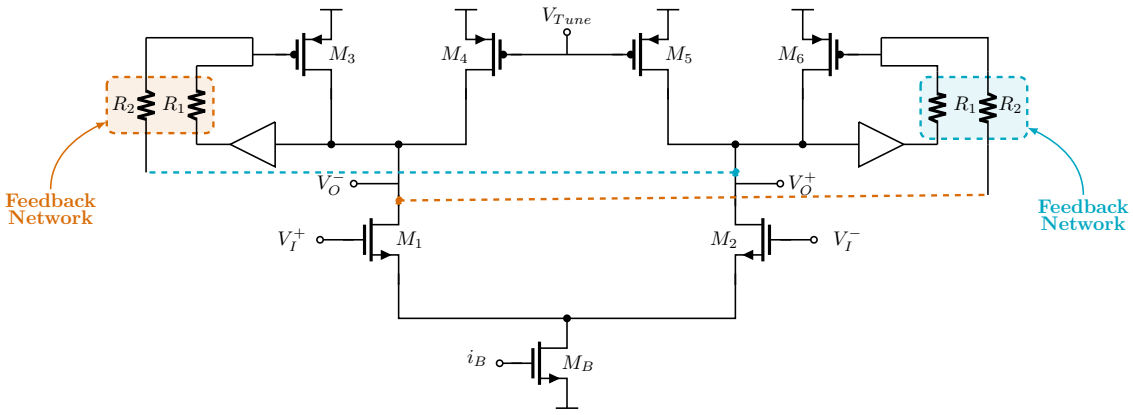


Figure 2.12: Structure of the QFGT-based modified Maneatis Cell (**Topology C**)

To analyze the effect of the resistor ratio R_1 and R_2 on the feedback, the voltage V_G across M_3 will be examined, with the understanding that the analysis for M_6 is identical due to the symmetry of the cell. Furthermore, given the topology, it is valid to assume that $R_1 \gg 1/g_{m2F}$. The modification of both outputs can be represented using the model of Figure 2.13.

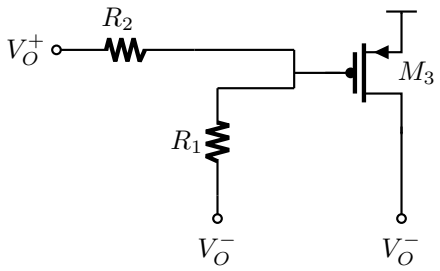


Figure 2.13: Analysis of the load of the QFGT based-modified Maneatis Cell.

Due to the decoupling of the voltage follower cell, its possible to represent the terminals of the pseudo-diode transistor as shown in Figure 2.13. This allow to define the feedback factor as a function of the relation of the resistances R_1 and R_2. The voltage seen at the gate of M_3 is β times the voltage of the complementary output as shown in Equation 2.28.

$$V_G = -\beta V_O^+ \tag{2.27}$$

Where, the feedback factor is function of R_1 and R_2 according to Equation 2.28, and therefore, the output resistance can be expressed as shown in Equation 2.29.

$$\beta = \frac{R_1 - R_2}{R_1 + R_2} \tag{2.28}$$

$$R_{OUT} = \frac{1}{\frac{1}{r_O} - g_m\beta} \tag{2.29}$$

This factor gives three cases that modify the stability of the modification of the cell delay:

- $R_1 = R_2$: this condition nullifies the effect of the feedback in the cell.
- $R_1 \gg R_2$: this case must be avoided because causes that the cell act as a latch.
- $R_2 \gg R_1$: the feedback factor β is positive and allow the modification of the frequency response.

The effect to use this modification is seen in the response of the output resistance denoted as a negative resistance dependent on the effect of β.
The transfer function $H(s) = V_o(s)/V_i(s)$ of the QFGT-modified Maneatis cell is computed by considering a load capacitance $C_L = C_{GS1}+C_{GD1}+C_{GS3}+C_{DB3}+C_{DB4}+C_{GD4}$ attached to the $V_o^{\pm}$ node in Figure 2.12.
The Equation 2.30, the ω_O and the Gain-Bandwidth product (GBW) can be computed as shown in Equations 2.31 and 2.32.

$$H(s) = -A_O \cdot \frac{\frac{1}{C_L R_{out}}}{s + \frac{1}{C_L R_{out}}} \tag{2.30}$$

$$\omega_O = \frac{1}{C_L R_{out}} = \frac{1}{C_L} \cdot \left(\frac{1}{r_{O_{4,5}}} - g_{m_{3,6}} \beta \right) \tag{2.31}$$

$$GBW = \frac{g_{m_{1,2}}}{C_L} \tag{2.32}$$

Three significant remarks can be established based on Equations 2.31 and 2.32:

- The GBW remains constant despite the β factor variation.
- The bandwidth of the cell can be reduced by increasing the β, leading to a phase shift (also called phase degeneration).
- An increment in the β factor enhances the A_O gain.

2.1.8 Design and Verification of the different Ring Oscillators

To verify the operation of the cell, a 5-stage ring oscillator topology was proposed, as illustrated in Figure 2.14. In this work, the simulations consider the three types of delay cells previously analyzed:

- Basic Maneatis Cell: Figure 2.4
- Voltage Follower-modified Maneatis Cell: Figure 2.11
- QFGT-based modified Maneatis Cell: Figure 2.12

As shown in Figure 2.14, the parasitic interconnection capacitance between each of the cells is labeled as C_ω. In this work, a value of $C_\omega = 50\,\text{fF}$ was considered.

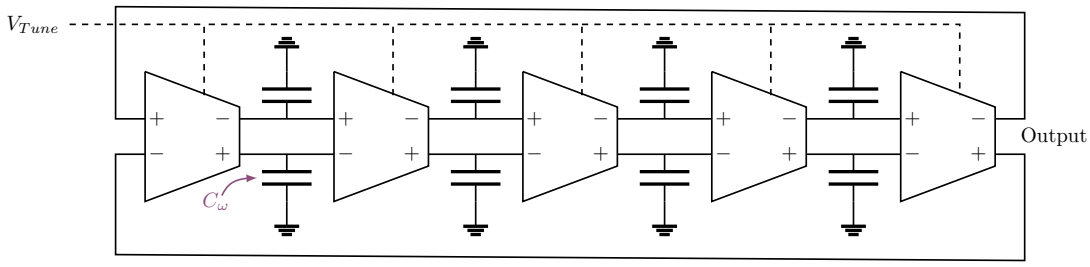


Figure 2.14: Topology of the 5-stage ring oscillator proposed

The sizing process of the delay cells begins with the generation of the bias voltages for the transistors that constitute the delay cell. The generated bias voltages utilize simple current mirrors, as illustrated in Figure 2.15.

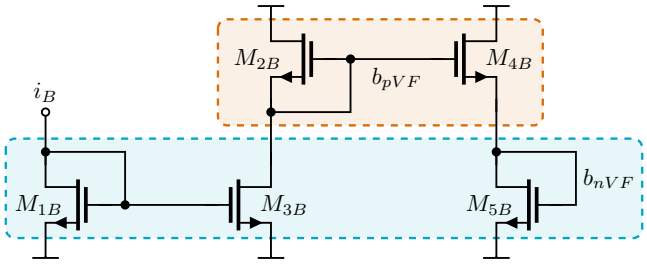


Figure 2.15: Biasing block for the Voltage Follower blocks

For the sizing of the biasing stage, the specifications shown in Table 2.1 are taken into account. In this design, as in the blocks presented in the following chapters, the restrictions imposed by the UMC 180nm technology in terms of **electromigration**, as well as the specific requirements for the analog layout design, are also considered.

Table 2.1: Design specifications of biasing circuit cell of 10 μA

Parameter	Value
$\|V_{D,sat}\|$	65 mV
I_B	10 μA
$\|V_{bp}\|$	≈382 mV
V_{bn}	≈323 mV

In this work, a minimum transistor length (L) of 420 nm is set as a restriction. This parameter was determined by considering the minimum spacing between Metal 1 and Metal 2 (denoted in the PDK as ME1 and ME2), as well as the minimum width to ensure at least two contacts. Considering the lenght restriction and the specifications in the Table 2.1, the dimensions of the biasing block are summarized in Table 2.2.

Table 2.2: Dimensions corresponding to Voltage Follower Bias Cell

Transitor	W_F [m]	L [nm]	NF
M_{1B}	12.44μ	540	4
M_{2B}	19.91μ	550	10
M_{3B}	12.44μ	440	4
M_{4B}	19.91μ	560	10
M_{5B}	12.44μ	540	4

Considering that the geometric pattern of the cell must be square, the resulting width of the transistors in the biasing cell is taken into account. Thus, symmetry in the design optimizes the mismatch effect between the designed cells. The final sizing of the voltage follower cell is presented in Table 2.3; it is important to mention that the dimensions of M_{3F} (particularly the length of the transistor) were adjusted to minimize the offset level at the output.

Table 2.3: Dimensions corresponding to Voltage Follower

Transitor	W_F [m]	L [nm]	NF
M_{BF}	12.44μ	720	4
M_{1F}	12.44μ	800	4
M_{2F}	12.44μ	800	4
M_{3F}	19.91μ	420	4
M_{4F}	19.91μ	540	4

2.1.8.1 Simulation and verification

The DC characterization is illustrated in Figure 2.16. In this figure, the voltage characteristic curve is presented. Due to its nature as a follower, it is expected that ideally, the output signal (identified as the dashed orange curve) will follow the input signal (identified as the blue curve) across the entire voltage range. In this simulation, for an input range of 400 mV to 860 mV, the slope is nearly unity.

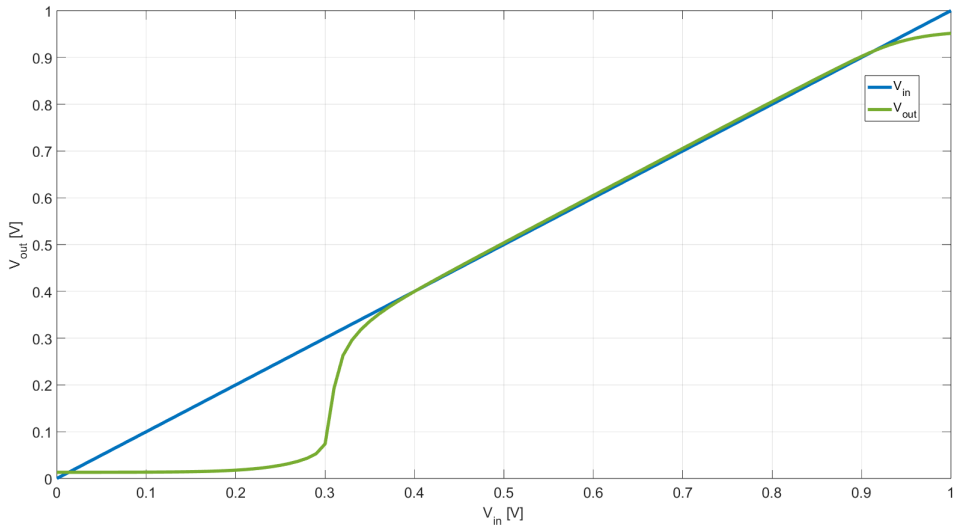


Figure 2.16: Characteristic DC transfer curve of the Voltage Follower.

Figure 2.17 shows the AC response of the voltage follower. The compensation of this block considers a Voltage Follower block of the same dimensions in its load and a C_ω = 50 fF, resulting in a C_C ≈850 fF and a f_{UG} = 18.62 MHz. The curve marked in blue corresponds to the gain of the cell, while the dashed green curve represents the frequency response of the phase of the block.

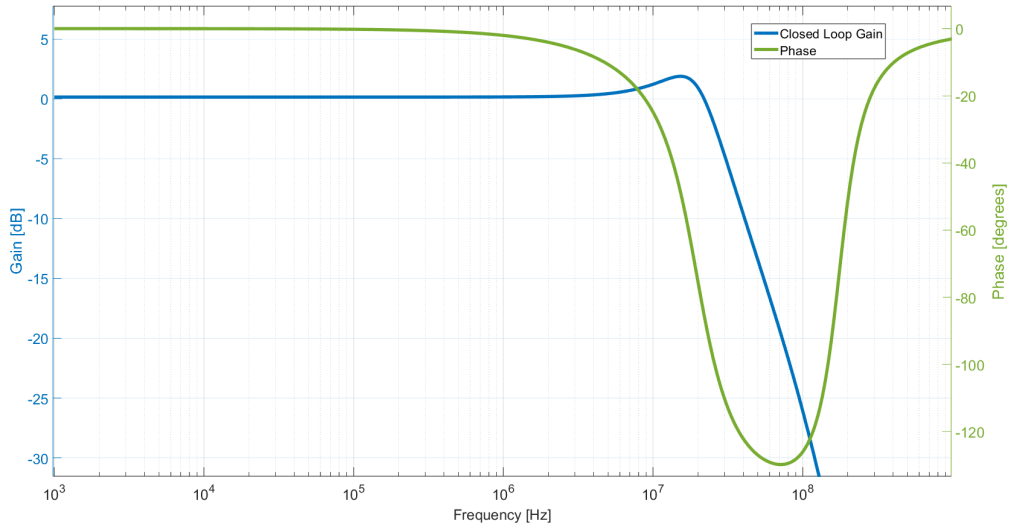


Figure 2.17: AC analysis of the voltage follower.

The sizing of the Maneatis Cell considers that each of the regions denoted by blocks, as shown in Figure 2.4, will be located within the same active region in the layout. Thus, taking into account the criteria explained earlier, the resulting dimensions are summarized in Table 2.4.

Table 2.4: Dimensions corresponding to Basic Maneatis Cell Delay

Transitor	W_F [m]	L [nm]	NF
M_B	6μ	760	8
M_1, M_2	6μ	720	8
M_3, M_6	6.45μ	720	4
M_4, M_5	6.45μ	720	16

To verify the symmetry in the load transistors, a DC analysis of the cell was performed considering the dimensions corresponding to transistors M_3 and M_4, taking into account the conditions of V_{SG} and plotting the output current (through V_O indicated in Figure 2.5a). Figure 2.18 shows two curves; the blue curve corresponds to a V_{Tune} = 650 mV, and the orange curve represents the curve for a V_{Tune} = 1 V. Thus, it is confirmed that for each value of V_{Tune}, there exists an effective resistance whose approximate value is the slope of the curve obtained from the load.

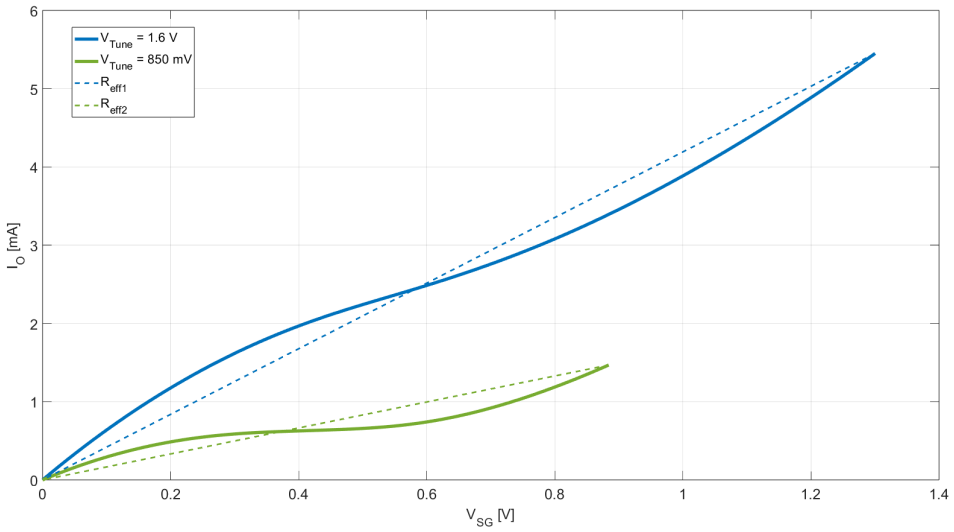


Figure 2.18: I-V curve of the load transistors (M_3 and M_4) considering different biases.

To compare the performance of the different designed cells, Figure 2.19 shows the frequency response of each cell. The green curve corresponds to the basic Maneatis cell, the orange curve represents the response of the cell with phase degeneration using the Voltage Follower, and finally, the blue curve is associated to the cell with the internal feedback network.

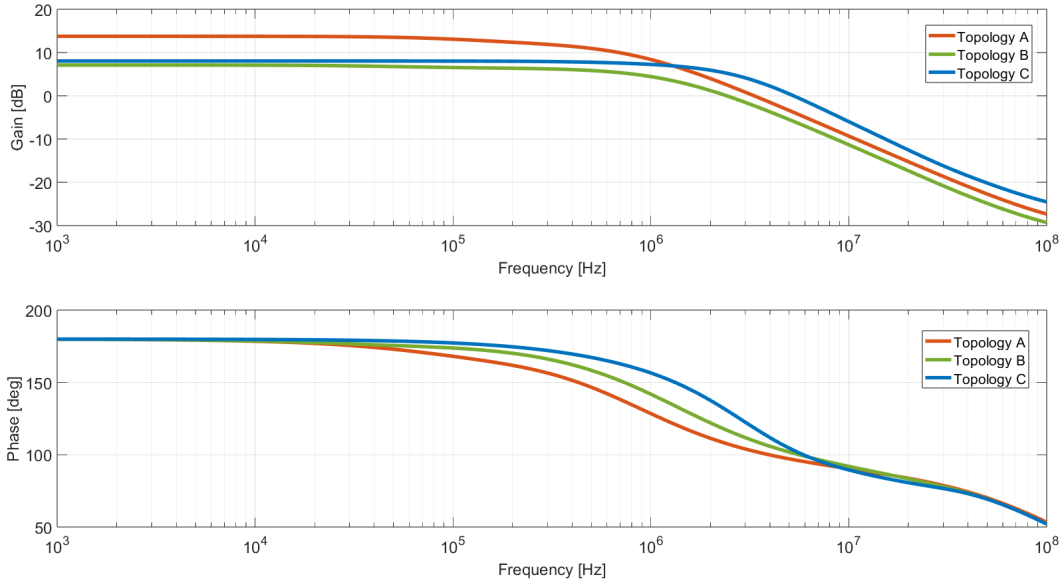


Figure 2.19: Gain and Phase frequency responses of each topology considered.

From the obtained simulations, it was observed that the modification of the pseudo-diode using the voltage follower altered the bandwidth of the cell, which in turn will be reflected as a decrease in the oscillation frequency of the ring. In contrast, the cell with internal feedback was simulated considering an $\beta = 0.5$, with $R_1 = 200$ kΩ, and the

response showed a reduction in gain. Table 2.5 summarizes the gain and bandwidth measurements for each compared delay cell.

Table 2.5: Comparison of the frequency response of the different delay cells.

Cell	Gain [dB]	Bandwidth [Hz]
Basic Maneatis Cell	13.27	539 k
Maneatis Cell with Voltage Follower	13.76	428.2 k
Maneatis Cell with Local Feedback	3.466	637.9 k

The analysis of the effect of the feedback factor β on the gain and bandwidth of the modified delay cell is conducted by considering the three possible scenarios (defining a $R_2 = 100$ kΩ):

- $\beta > 0$: Resistor condition in feedback network $R_1 < R_2$
- $\beta = 1$: Resistor condition in feedback network $R_1 = R_2$
- $\beta < 0$: Resistor condition in feedback network $R_1 > R_2$

To consider the three possible scenarios for β, the parametric simulation was performed using the Cadence simulator, taking a minimum value of R_1 from 10 kΩ to 600 kΩ, with the feedback factor ranging from 20 to 0.3. The obtained results are shown in Figure 2.20.
In Figure 2.20, the condition of β demonstrates a decrease in the gain of the cell of up to -7 dB. The attenuation of the gain is also reflected in the condition $\beta = 1$; for a gain of at least 2 dB, the feedback factor must be at least 0.75.

Table 2.6: Comparison of the time response of the Ring Oscillators based on the different topologies.

Ring Oscillator Type	f_{Osc} [kHz]	Amplitude [mV]
Maneatis Cell - Based	868.1	411.54
Maneatis Cell with Voltage Follower - Based	841.3	408.3
Maneatis Cell with QFGT - Based	727.3	84.65

Table 2.6 summarizes the transient response to a $V_{Tune} = 650$ mV for the three ring oscillators of the three different analyzed cells. Figure 2.21 shows the characteristic curve of the oscillation frequency as a function of β; in this work, the selected operating range spans from 150 kΩ to 800 kΩ.

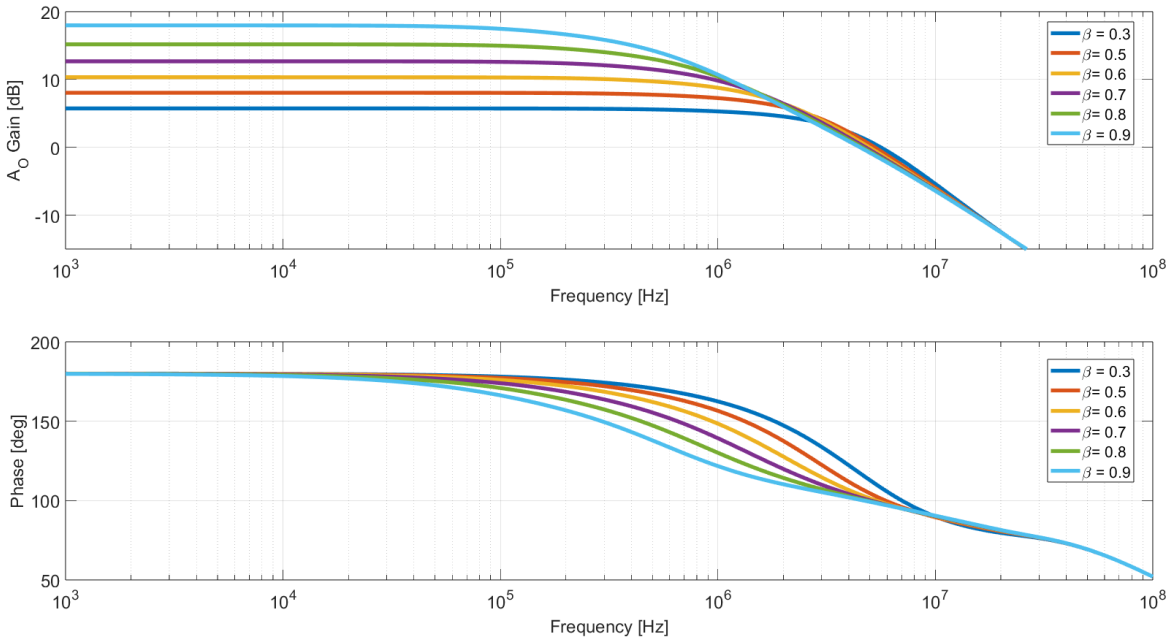


Figure 2.20: Gain and Phase frequency response of Topology C, as a function of the feedback factor β

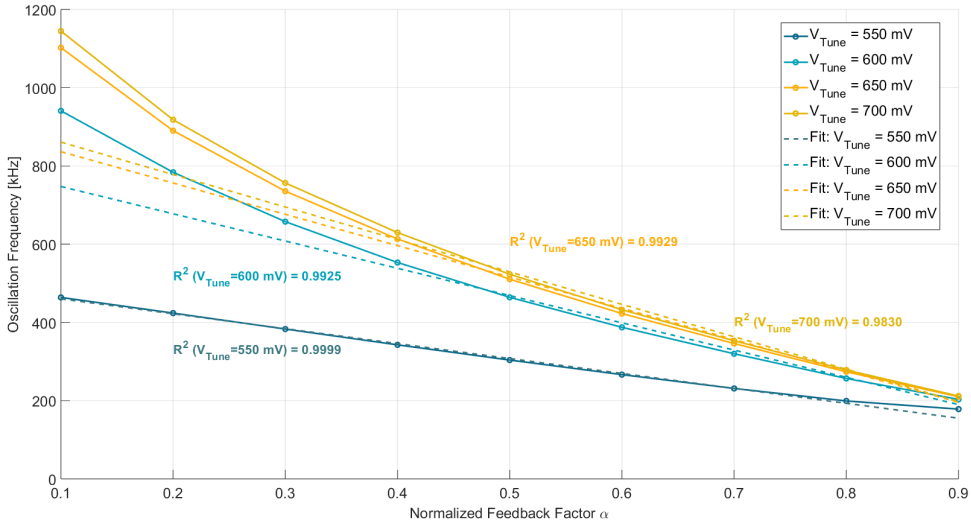


Figure 2.21: Characteristic frequency curve as a function of R_1 considering the 5-Stages Ring Oscillator based on Topology C

2.1.8.2 Monte Carlo Analysis and Process Variations Analysis

Process variations are inevitable deviations that occur during the fabrication of integrated circuits, which can affect the electrical characteristics of devices and, consequently, the circuit's performance. Process corners represent the most extreme variations of parameters that affect the strength or speed of the MOSFET, considering the contribution of pMOS and nMOS transistors separately. By combining them, we get the following combinations:

- FF Corner: Refers to the Fast-Fast corner (for both pMOS and nMOS transistors).
- SS Corner: Refers to the Slow-Slow corner (for both pMOS and nMOS transistors).
- FPSN Corner: Refers to the Slow corner for the nMOS and Fast for the pMOS transistors.
- FNSP Corner: Refers to the Slow corner for the pMOS and Fast for the nMOS transistors.

To validate the design of each of the designed cells, simulations were conducted regarding the process variations of the technology. Table 2.7 summarizes the results of the simulations of the effect of process variations on the frequency response of the individual cells, particularly gain and bandwidth.

Table 2.7: Summary of the results obtained from the process variation analysis.

Cell Delay	Parameter	Nominal	SS	FF	FNSP	SNFP
Topology A	Gain [dB]	13.76	2.182	11.17	7.136	5.94
	BW [Hz]	539k	2.455M	12.55M	1.35M	6.593M
Topology B	Gain [dB]	13.77	2.21	11.18	7.231	5.94
	BW [Hz]	478k	2.521M	9.66M	1.346M	5.426M
Topology C	Gain [dB]	3.466	5.336	3.007	4.843	1.351
	BW [Hz]	637.9k	471.3k	1.54M	525k	852.2k

NOTE: The maximum and minimum values obtained in each simulation are indicated with the colors blue and green, respectively.

The validation of the ring oscillators is also performed in the time domain, considering a $V_{Tune} = 650$ mV. In Table 2.8, these simulations characterized the frequency variation due to the different corners of the manufacturing process. It was observed that the maximum and minimum frequency values are associated with the FF and SS corners, respectively.

Table 2.8: Results of the process variation analysis for the different ring oscillators.

Ring Oscillator Based	Nominal	SS	FF	FNSP	SNFP
Topology A	868.1k	718.7k	1.31M	772.5k	1.089M
Topology B	841.3k	693.6k	1.26M	737.7k	1.031M
Topology C	727.3k	648.1k	986.2k	686.3k	828.7k

NOTE: The maximum and minimum values obtained in each simulation are indicated with the colors blue and green, respectively.

Table 2.9 summarizes the performance of the ring oscillators considered in this work under Monte Carlo analysis. These simulations were conducted with 1000 runs, accounting for statistical variations in both mismatch and process. This analysis allows for the validation of the operation of the internal local feedback networks applied to the modified structure, achieving a reduction of more than 50% in the standard deviation, considering two cases of oscillation frequency (denoted as Case I and II). This leads us to the conclusion that implementing dual feedback improves the performance of the cell in terms of frequency; moreover, it provides a means of frequency control (in addition to V_{Tune}), which is suitable for bio-impedance spectroscopy applications due to the range of frequencies over which tissue must be analyzed.

Table 2.9: Summary of Monte Carlo simulation results for the different Ring Oscillators.

Topology	Mean [μ]	Standard Deviation [σ]
Topology A	894.445 kHz	143.429 kHz
Topology B	850.921 kHz	113.996 kHz
Topology C: Case I	1.114 MHz	10.94 kHz
Topology C: Case II	176.828 kHz	32.58 kHz

2.2 Direct Digital Frequency Synthesizer (DDS)

First proposed by Tierney in 1971 [50], the Direct Digital Frequency Synthesizer (DDS) consists of three basic building blocks: a phase accumulator, a phase-to-amplitude converter, and finally, a linear digital-to-analog converter to produce a fully analog output signal, as shown in Figure 2.22.

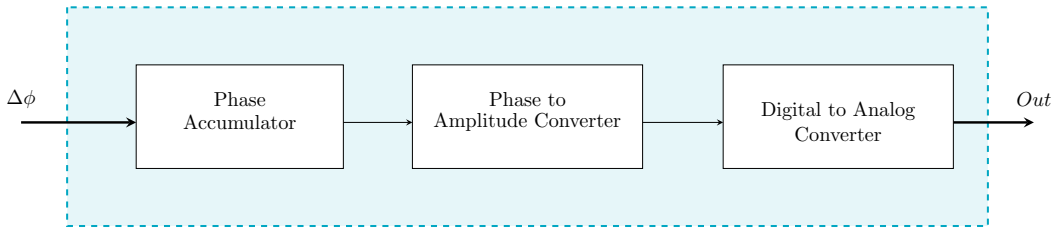


Figure 2.22: Block diagram of DDS

The input parameter (in addition to a clock signal) is a digital word known as the *phase increment* $\Delta\phi$. During each clock cycle, $\Delta\phi$ is added to the previously stored value in the Phase Accumulator (PA). In other words, it functions as an adder with a memory register that stores the resulting sum. Consequently, the output signal's operating frequency depends on the principle of overflow arithmetic. [51] In this way, for a given input clock frequency f_{clk}, the output frequency f_{out} is given by

$$f_{out} = \frac{f_{clk}}{2^j} \tag{2.33}$$

Where j is the number of bits of the accumulator, and therefore $\Delta\phi$ must be less than or equal to 2^{j-1}. The phase accumulator generates a digital word that functions as a pointer address to a Phase-to-Amplitude Converter, which consists of a discretized sinusoidal signal over a range of 2π and stored in a ROM look-up table. Finally, the DAC is used to convert the quantized sine wave into an analog signal.
In this type of architecture, signal storage involves significant memory elements, which, when synthesized, can result in the following:

- Higher power consumption
- Lower reliability
- Slower access time
- Larger die area, which reduces the performance of the DDS.

These limitations lead to implementing a design that either requires less die area in synthesis or, alternatively, uses signal approximation algorithms (such as the CORDIC algorithm [52]) to eliminate the need for a ROM.

2.2.1 Proposed 8-bit DDS

The proposed DDS signal generation approaches the symmetry of the sinusoidal signal as the main optimization point for the ROM block, as shown in Figure 2.23. The 4-bit digital word (Step Frequency) is added to the 8-bit PA register during each clock cycle. However, the most significant bits (MSB and 2nd MSB in Figure 2.23) are control elements for the Complementor blocks.

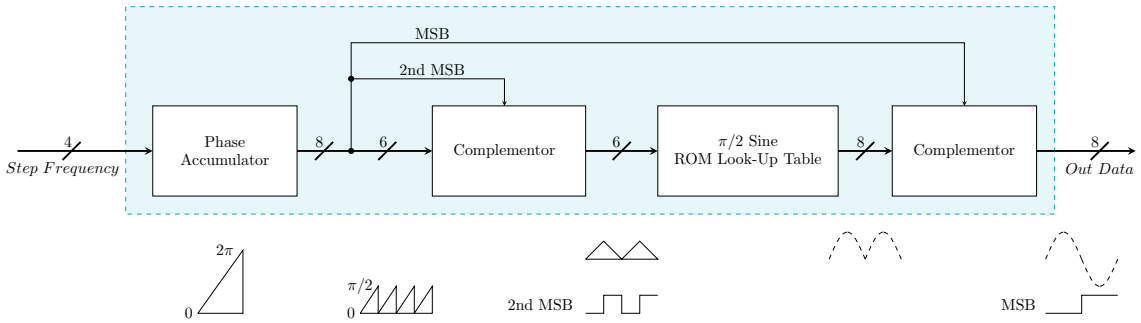


Figure 2.23: ROM-based DDS with signal compresion

Figure 2.23 shows the operational algorithm:

- In each clock cycle, the 4-bit digital word (*Step Frequency*) is added to the 8-bit PA Register.
- The first six bits of the output vector from the PA [5:0] are complemented if the 2nd MSB = 1, generating a triangular waveform corresponding to the half-cycles of the output wave.
- The second half-cycle of the signal is complemented when the MSB = 1 to convert the rectified signal into a sinusoidal signal.

However, a 4-bit control word only allows the generation of sixteen different frequency waveforms, which is limiting for the frequency range required by Bio-Impedance Spectroscopy applications. Figure 2.24 shows a 2-bit frequency divider block added to overcome this limitation.

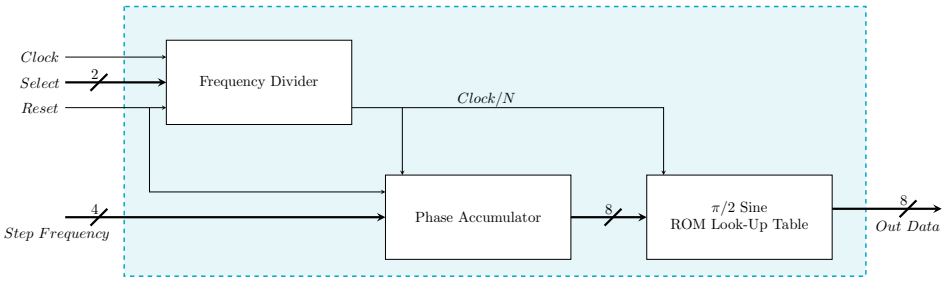


Figure 2.24: Top Design of DDS proposed

The selection conditions of the Frequency Divider follow the logic of the Phase Accumulator: **if the input word increases, then the operating frequency also increases.** Thus, the output of the Frequency Divider results in the following cases:

- *Select* = 0'b00 → N = 8
- *Select* = 0'b01 → N = 6
- *Select* = 0'b10 → N = 4
- *Select* = 0'b11 → N = 2

Considering the above, the generalized expression for the frequency (considering 8 bits) of the block in Figure 2.24 can be expressed in function of the clock frequency and the input data of the Step Frequency, as shown in Equation 2.34.

$$f_{Out} = \frac{f_{CLK}}{N \times 2^{(9-j)}} \tag{2.34}$$

where j corresponds to the input data of Step Frequency.
Following the expression 2.34 and considering a clock frequency $f_{CLK} = 100$ MHz, it is possible to obtain transfer curves that relate the output signal frequency to the digital input word (*Step Frequency*) for the different *Select* cases, as shown in Figure 2.25.

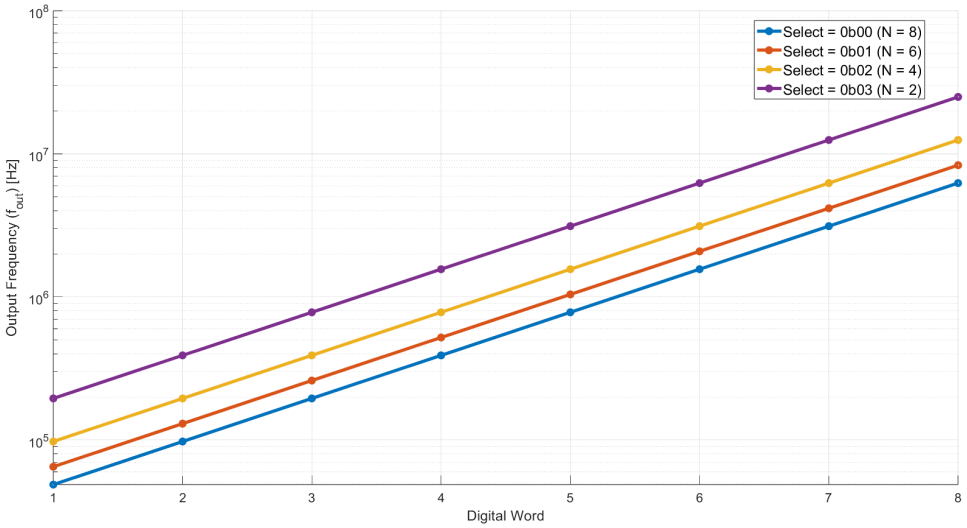


Figure 2.25: Output frequency values obtained for different input words.

As shown in Figure 2.25, the system can generate signals with frequencies spanning three orders of magnitude. Theoretically, the minimum frequency is achieved under the conditions *Select* = 0'b00 and *Step Frequency* = 0'b0001, resulting in $f_{Out} = 48.8$ kHz. On the other hand, the maximum output frequency is obtained with *Select* = 0'b11 and *Step Frequency* = 0'b1111, reaching $f_{Out} = 25$ MHz.

2.2.2 Simulation and verification in Aldec-HDL

The first step in the synthesis of digital circuits in 180 nm technology is the simulation and verification of each of the modules shown in Figure 2.22. Each of these modules is designed using hardware description languages, specifically Verilog. The simulations presented below were conducted using Aldec-HDL software.

2.2.2.1 Frequency Divider Module

The operation of this module primarily consists of a counter that depends on the input word which defines a parameter of the module Max. Counter Control instantiated in Verilog, as shown in Figure 2.26. In each clock cycle, a register counts from zero up to the parameter value; at this point, the output bit is complemented to generate a lower-frequency clock signal. This newly generated frequency will then serve as the clock for the subsequent blocks.

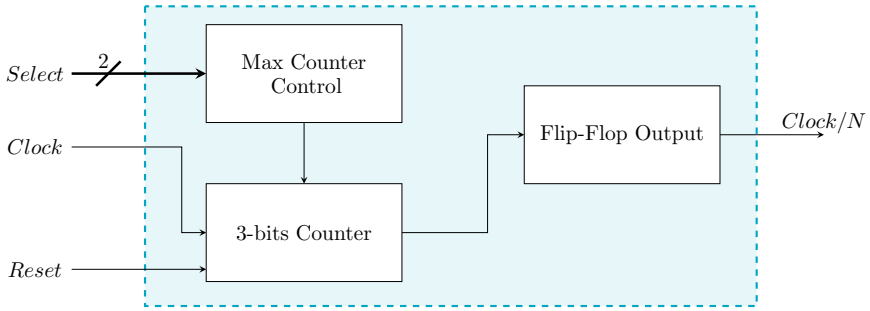


Figure 2.26: Block Diagram of Frequency Divider Verilog Module

Figure 2.27 shows the waveform of the Frequency Divider output for input words *Select* = 0 and *Select* = 1, considering a clock frequency f_{CLK} = 100 MHz. For the first 2200 ns, it can be observed that **clkOutput** changes state every 4 clock cycles. On the other hand, when *Select* = 2, the control register changes its value, and the state change occurs every 3 clock cycles of *clkMaster*. Figure 2.28 shows the waveform of *clkOutput*

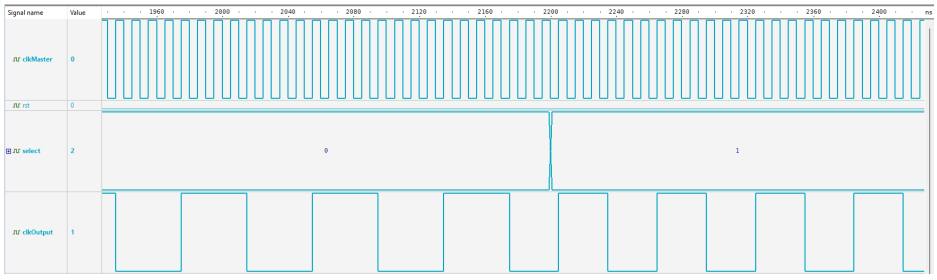


Figure 2.27: Simulation of the **Clock Divider** module for Select = 0 (up to 2200 ns) and Select = 1.

when the digital input word is *Select* = 2 and 3. In the first case, the *clkOutput* signal changes every 2 clock cycles, in the second case, the output signal changes state in each

defined cycle. These simulations allow us to verify the functionality of the *Frequency Divider* module for each input word scenario.

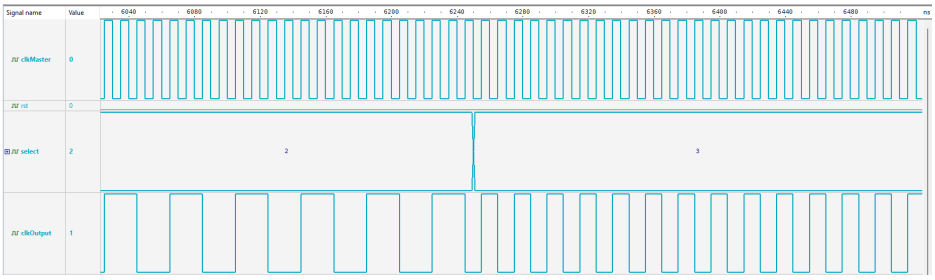


Figure 2.28: Simulations of the **Clock Divider** module for different Select configurations.

2.2.2.2 Phase Accumulator Module

The phase accumulator is a modulo-N counter with 2^N digital states that increment with each input clock pulse of the system. The magnitude of the increment depends on the value of the tuning word, M, applied to the adder stage of the accumulator. The tuning word sets the size of the increment for the counter, determining the frequency of the output waveform. As shown in Figure 2.29, each word corresponds to a discretized value of the sinusoidal signal stored in the ROM Look-Up Table.

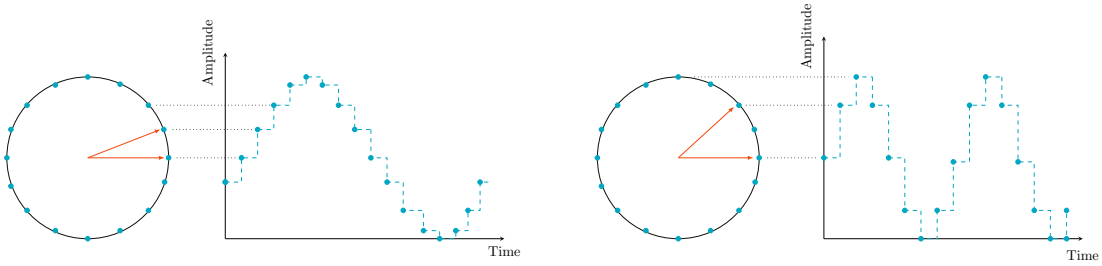


Figure 2.29: View of a 16-state phase accumulator operation using a phase wheel to visualize how the tuning word affects the output frequency of the DDS

Figure 2.30 shows the waveform corresponding to the 6-bit output vector of the *Phase Accumulator*. As noted, the triangular signal corresponds to each half-cycle reflected in the DAC output during the simulation. It is important to note that the corresponding analog signals of the output vector are shown for the cases considered for the digital input word *stepA*, .

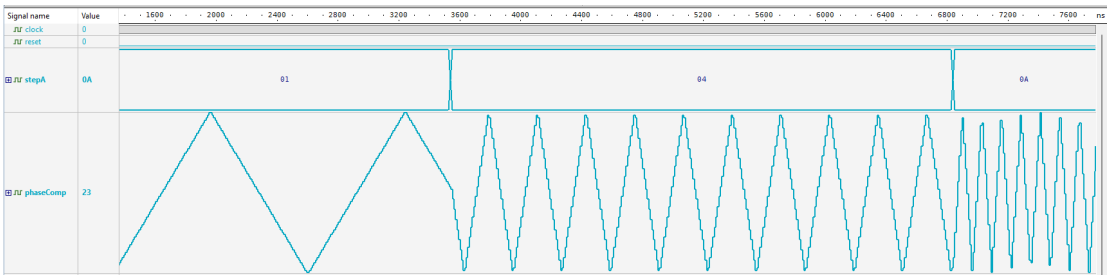


Figure 2.30: Analog signal corresponding to the output of the phaseComp register considering stepA = 01, 04, and 0A.

2.2.2.3 Sine Look-Up Table Module

The designed ROM is 8x64, where each register stores data corresponding to the discretized sinusoidal wave previously obtained in Matlab. Figure 2.31 shows the internal structure of the module. As can be seen, the designed module includes a complement stage that depends on the flags (or most significant bits) to generate the sinusoidal signal over 2π. In the module's testbench, the simulation only considers a count from 0 to 63 (i.e., a 6-bit counter) in the address to verify that the stored data corresponds to the discretization obtained in Matlab.

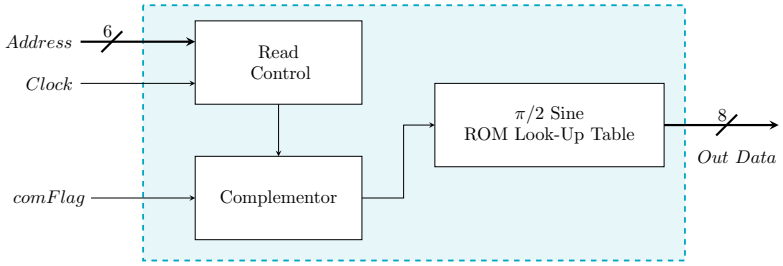


Figure 2.31: Block Diagram of Sine Look-Up Table Verilog Module

Figure 2.32 shows the result of the module verification and the analog waveform associated with the digital word obtained at the *data* port. For this scenario, the step size of the *address* is unitary to achieve the highest resolution in the output signal.

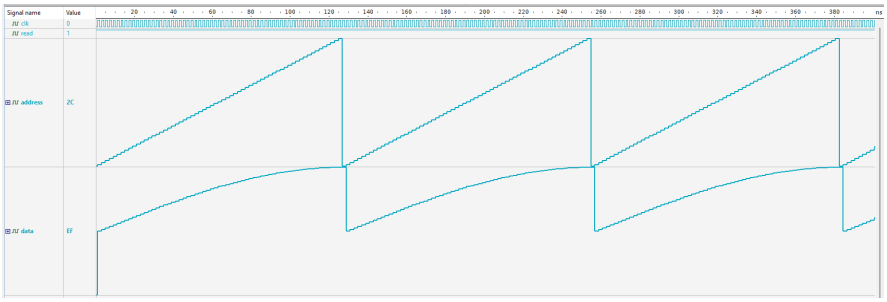


Figure 2.32: Simulation of the output register for each of the 64 addresses of the LUT

2.2.2.4 Top DDS Design

Finally, the DDS comprises the internal instantiation of each previously presented module, and Figure 2.22 shows their interconnections. Figure 2.33 depicts the waveform obtained in the simulation results.

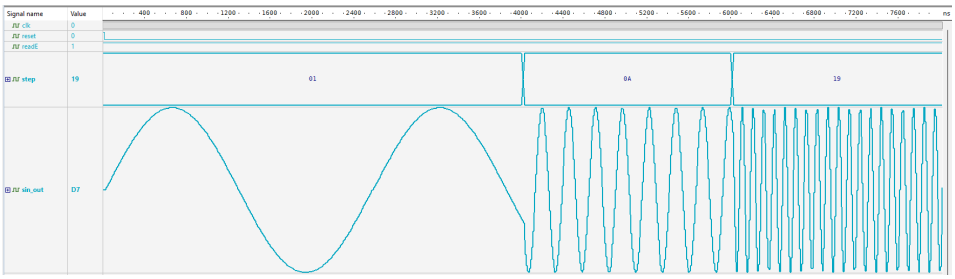


Figure 2.33: Final simulation of the Top design described in Figure 2.24

We can observe that during the first 4000 ns, the control word defined in *step* is 01, resulting in a very low operating frequency but with the advantage of minimal distortion due to quantization levels. Conversely, when the *step* takes the value 0A, there is an increase in frequency, although this comes with the drawback of more significant distortion in the output signal (*sin_out*).

2.2.3 Synthesis using 180 nm technology

Once the design was verified in Aldec-HDL, logic synthesis to 180 nm technology was carried out using Cadence's Genus tool. This tool allows for instantiating of all components from the loaded Verilog files. Additionally, timing analysis was performed, where the constraints were defined to analyze the slack across all datapaths of the resulting design.

2.2.3.1 Timing analysis

Slack is defined as the difference between the actual or achieved time and the desired time for a timing path [53], for example, the case shown in Figure 2.34.

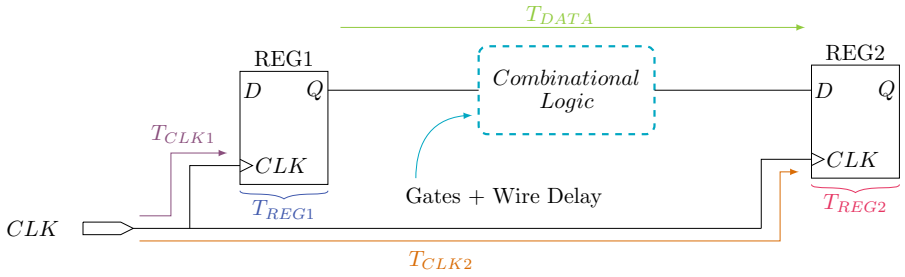


Figure 2.34: Illustration of slack definition between two synchronous blocks.

The representation of each of the digital signals involved in 2.34 is shown in Figure 2.35. In the diagram, the slack is the time remaining after the data signal becomes valid and before the next clock edge, which performs the latch operation, captures the signal in the second register (REG2).

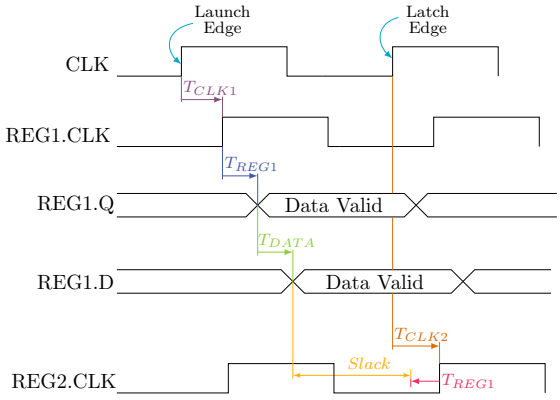


Figure 2.35: Timing diagram of signals presented in 2.34.

In this way, the following signals can be explained:

- $\mathbf{T}_{CLK1}$: This is the launch clock time (Launch Edge), meaning when the first register (REG1) launches the data signal.

- $\mathbf{T}_{DATA}$: This is the time when the data signal becomes valid after being launched from REG1.
- $\mathbf{T}_{CLK2}$: This is the second clock edge time (Latch Edge), when the REG2 register captures the data signal.
- The **slack** is the time margin between $\mathbf{T}_{DATA}$ (when the data is valid) and the capture edge of REG2 ($\mathbf{T}_{CLK2}$).

Thus, slack is a critical parameter in signal timing, as it indicates whether the design operates at the specified frequency. This parameter can be analyzed under the following scenarios:

- A **positive slack** means that the design is operating at the specified frequency with some margin.
- **Zero slack** indicates that the design is working exactly at the specified frequency with no margin available.
- A **negative slack** implies that the design does not meet the constrained frequency and timing, resulting in a setup violation.

During the synthesis process using the Genus tool, the constraints were defined to obtain the histogram of slack associated with the critical paths of the synthesized design. Figure 2.36 shows the count of the six critical logic paths with positive slack values.

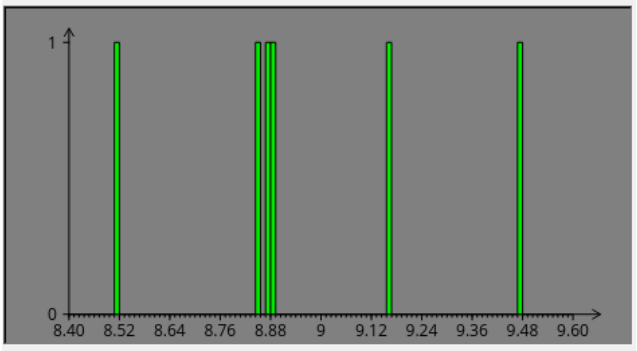


Figure 2.36: Histogram of the slack associated with the critical logic paths of the synthesized design obtained with Genus tool.

2.2.3.2 Power Analysis

Table 2.10 reports the results of the power analysis conducted by Genus. This table provides a detailed summary of power consumption and describes the contributors to the total power, with switching power being the most significant contributor.

Table 2.10: Power Detail Report

Instance	Cells	Leakage [nW]	Internal [μW]	Net [mW]	Switching [mW]
DDS/U2	112	9.392	132.871	1.183	1.316
DDS	166	17.788	664.138	1.264	1.928

2.2.4 Logic Equivalence and Layout

The objective of the Conformal tool is to compare the original Verilog code with the cells associated with the digital library. That enables verification that the synthesized blocks meet the instantiated modules, identifying and eliminating redundant registers or blocks if necessary. It also helps ensure that no modules were omitted due to non-synthesizable instructions. Table 2.11 shows the comparison results generated by Conformal, where modules U2 and U3, corresponding to *phaseAcc* and *freqDiv*, respectively, were fully synthesized into cells associated with the technology. In contrast, module U2, corresponding to the LUT, was generated as a separate module.

Table 2.11: Logic Equivalence Check

Golden	Revised
8 primitives	54 library cells
U1(phaseAccm)	U2(LUT)
U2(LUT)	
U3(freqDiv)	

Figure 2.37 shows the schematic resulting from the digital synthesis. The final report from Genus indicated that the total cell area is 5173.459 μm^2, and the net area reported in the program is 2165.659 μm^2, resulting in a total area of 7339.118 μm^2 (Cell + Net).

Finally, using Innovus, a floorplan was created specifying the power supplies as well as the input and output ports. For the layout, Metal I and II were used for power supplies, and the input and output pins were connected via Metal III. Additionally, it was defined that even-numbered metals are used for vertical connections, while odd-numbered metals are used for horizontal interconnections. Considering the above, the final layout design is shown in Figure B.3, with final dimensions of 190 μm $\times$ 41 μm.

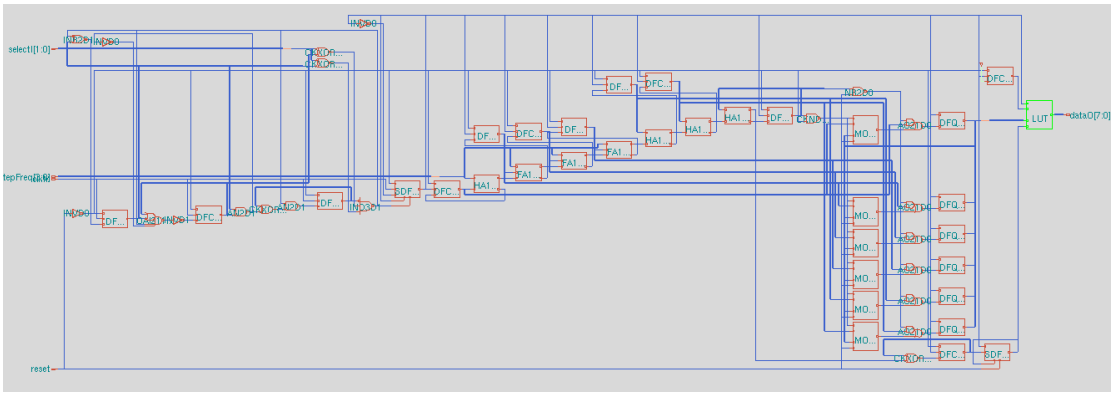


Figure 2.37: Resulting schematic from the association of the design with the digital cells from the library.

2.3 Conclusions

The DPI analysis provides valuable insights into the behavior of complex systems by modeling their components with idealized assumptions. This approach facilitates understanding how an applied signal propagates through the system and interacts with circuit features like feedback mechanisms. The QFGT-based feedback network, acting as the summation node, effectively regulates the system's frequency response based on the feedback factor, β, illustrating how feedback influences the control and stability of the oscillator's performance across different operating ranges.
Additionally, the use of transistors in Weak Inversion, combined with the internal degeneration networks, further refines the oscillator's frequency control. These networks not only reduce the operating frequency but also enhance the overall tunability and stability of the ring oscillator. The results emphasize the importance of careful circuit design in achieving the desired frequency range, particularly when internal feedback elements and degeneration techniques are employed to modulate the oscillator's performance.
The implementation of the DDS through digital synthesis leverages the advantages of using a standardized hardware description language, enabling synthesis across different technologies with the same code. This approach facilitates the modularity of functional blocks. However, there is a tradeoff between the oscillation frequency (f_{out}) and signal distortion. Specifically, the maximum operating frequency exhibits the highest waveform distortion. For instance, signals generated with the digital word *Step Frequency* = 0'b0001 have minimal distortion due to the small step size within the phase accumulator, whereas cases with the maximum step size result in a fully distorted output signal.

CHAPTER 3

Instrumentation Amplifier Design

The key component enabling the measurement of characteristic current and voltage signals for Bio-Impedance analysis is the Instrumentation Amplifier (IA). Due to its ability to amplify low-amplitude signals while maintaining stability, even in the presence of contact resistance between the electrodes and the skin, which it is critical for ensuring accurate measurements. This chapter begins by analyzing the internal blocks of the proposed IA, followed by an evaluation of the IA's overall performance. The design's robustness is then verified through process corner variations and Monte Carlo analysis and finally a comparison with the state of the art.

3.0.1 Folded Cascode Operational Transconductance Amplifier (FC-OTA)

The structure of the conventional single-ended Folded-Cascode OTA is shown in Figure 3.1. In this configuration, the principal objective of using PMOS transistors at the input (M_1 and M_2) is to achieve a lower input common-mode voltage, reduced input-referred flicker noise, and a higher non-dominant pole, thus resulting in a larger unity-gain bandwidth. [7] [54] [55]

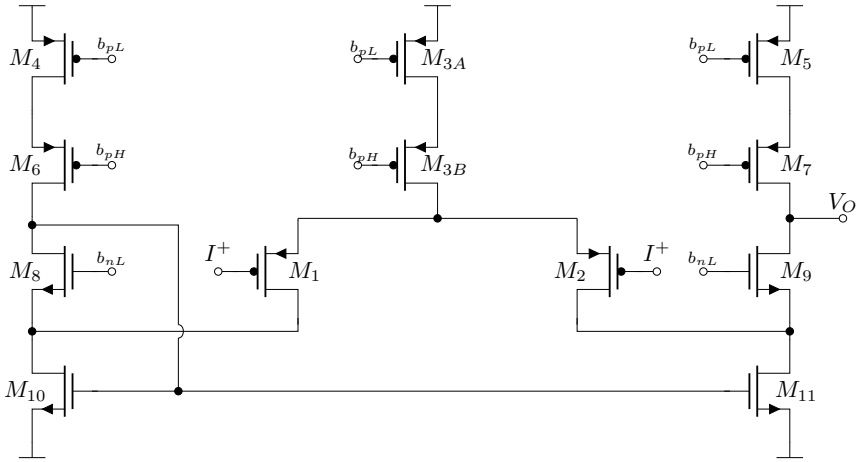


Figure 3.1: Folded Cascode OTA Topology

3.0.1.1 DC Analysis

Conventional FC-OTA topologies are typically biased with a basic current mirror; however, this design proposes that the bias current be supplied using a cascode current mirror, as shown in Figure 3.1.
To ensure that the OTA operates in the saturation region, the input signal range must be defined. This range is determined by the parameters $V_{in,min}$ and $V_{in,max}$, which vary depending on the amplifier topology used. Specifically, for the OTA in Figure 3.1, the minimum and maximum input ranges are defined by expressions 3.1 and 3.2, respectively.

$$V_{in,min} = V_{DD} - 2|V_{DSsat3A,3B}| - V_{GS1,2} \tag{3.1}$$

$$V_{in,max} = V_{SS} + 2|V_{DSsat3A,3B}| + |V_{DSsat1,2}| + V_{DSsat10,11} \tag{3.2}$$

Analyzing expressions 3.1 and 3.2, it is evident that using the cascode mirror for biasing represents a limitation in the input signal headroom of the FC-OTA. However, at node A, there is higher resistance due to transistors M_{3A} and M_{3B}, which enhances the virtual ground node and is reflected as an improvement in the amplifier CMRR response.

$$V_{out,min} = V_{SS} + V_{DSsat8,9} + V_{DSsat6,7} \tag{3.3}$$

$$V_{out,max} = V_{DD} - |V_{DSsat4,5}| - |V_{DSsat6,7}| \tag{3.4}$$

Expressions 3.3 and 3.4 allow us to conclude that the output signal will be limited by at least $2V_{DSsat}$ to maintain saturation and avoid distortion in the output signal.

3.0.1.2 AC Analysis

The advantage of using this topology is the higher gain. The folding of the input differential pair achieves a better input common-mode range. The gain of a Folded-Cascode configuration is obtained from its small signal model, using the expression

$$A_O = g_m R_{out} \tag{3.5}$$

Where g_m is the transconductance associated with the input differential pair and R_{out} is the resistance associated with the cascode stage at the output node. Intuitively, R_{out} can be calculated as follows

$$R_{out} = R_{on}||R_{op} \tag{3.6}$$

The small signal model associated with the FC-OTA topology, shown in Figure 3.2, allows for calculating the output resistance and, thus, the DC gain (AO) using expression 3.5.
As shown in Figure 3.2, the input pair is connected to the virtual ground. The output resistance is equal to the equivalent resistance of both cascodes, denoted as nMOS and pMOS, resulting in the expression 3.7.

$$R_{out} = \{(g_{m9} r_{O11}) r_{ds9}\}||\{r_{O7}[g_{m7}(r_{O5}||r_{O7})]\} \tag{3.7}$$

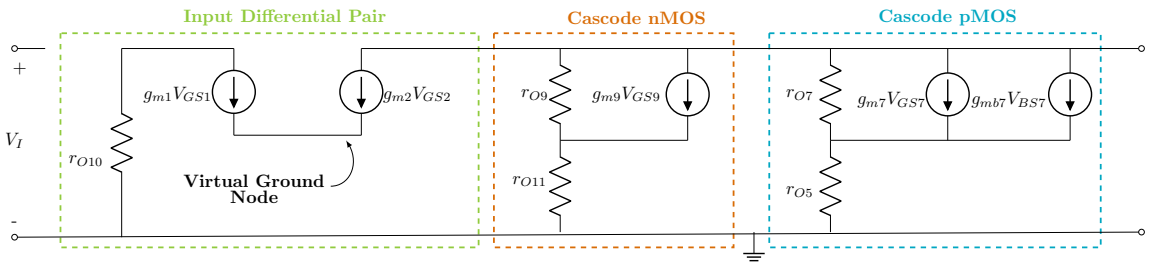


Figure 3.2: Small Signal Model of the FC-OTA shown in Figure 3.1

Finally, the DC Gain of the topology is obtained by substituting 3.7 into 3.5, as expressed in Equation 3.8.

$$A_O = -g_{m1,2}\{(g_{m9}r_{O11})r_{ds9}\}||\{r_{O7}[g_{m7}(r_{O5}||r_{O7})]\} \tag{3.8}$$

An approximation can be made by associating a pole with each node [7] to analyze the frequency response of the FC-OTA, as indicated in Figure 3.1. Consequently, the poles and the zero of the transfer function are described in Equations 3.8 to 3.12.

$$\omega_L = \frac{1}{R_{out}C_L} \tag{3.9}$$

$$\omega_A \approx \frac{g_{m9}}{C_{DB9} + C_{GS9} + C_{DB11}} \tag{3.10}$$

$$\omega_B \approx \frac{g_{m8}}{C_{BS8} + C_{GS8} + C_{DB10}} \tag{3.11}$$

$$\omega_C \approx \frac{g_{m10}}{C_{GS10} + C_{GS11} + C_{DB6} + C_{DB8}} \tag{3.12}$$

Finally, the transfer function can be described as:

$$A(s) = A_O \cdot \frac{(1 + s/2\omega_C)}{(1 + s/\omega_L)(1 + s/\omega_A)(1 + s/\omega_B)} \tag{3.13}$$

From Equation 3.13, it is evident that the FC-OTA exhibits one dominant pole, two non-dominant poles, and one Left-Half Plane (LHP) Zero.

3.0.1.3 Noise Analysis

The noise in CMOS circuits consists of random fluctuations that exist whether external signals are present or not, potentially distorting weak signals when transistors are part of an analog circuit. Due to its variability, the instantaneous value of I_n (or even voltage) at any given time t is unpredictable. Therefore, noise is characterized by its mean square value denoted as $\overline{I_n^2}$ and its root mean square $\sqrt{\overline{I_n^2}}$. [7]
White noise in CMOS transistors, often referred to as thermal noise or Johnson-Nyquist noise [56], originates from the random thermal motion of carriers in the channel when the transistor is in strong inversion. A current source between the drain and source

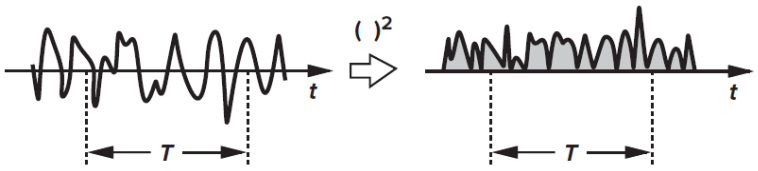


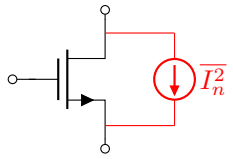
Figure 3.3: Average noise power. [7]

terminals can model this behavior. The drain current per unit bandwidth is described in equation 3.14 and illustrated in Figure 3.4a.

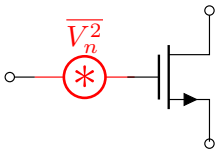
$$\overline{I_n^2} = 4kT\gamma g_m \tag{3.14}$$

Where, $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, and the coefficient γ is the white noise gamma factor. According to [7], this factor is derived to be equal to 2/3 for long-channel transistors. However, it is important to emphasize that this parameter is technology-dependent and varies for submicron MOSFETs. [7]
Additionally, the flicker noise (also known as "1/f" noise due to its behavior at low frequencies) can be modeled by a voltage source $\overline{V_n^2}$ in series with the gate [57] as shown in Figure 3.4 and is approximately given by Equation 3.15, where κ is a process-dependent constant on the order of 10^{-25} V^2F.

$$\overline{V_n^2} = \frac{\kappa}{C_{OX}WL}\frac{1}{f} \tag{3.15}$$



(a) Thermal noise modeled as a current source.



(b) Flicker noise modeled as a voltage source.

Figure 3.4: MOSFET noise modeled as spectral density functions.

The power spectral density of the contributions from both noise sources is shown in Figure 3.5. Two regions can be identified, divided by the 1/f Corner point:

- At low frequencies ($f \leqslant 1/f$ Corner), the power spectral density is dominated by 1/f noise, which decreases with increasing frequency. This is observed as a negative slope on the graph.
- At higher frequencies ($f \geqslant 1/f$ Corner), thermal noise predominates. This is represented as a horizontal line on the graph, indicating that its power spectral density remains ideally constant with respect to frequency.

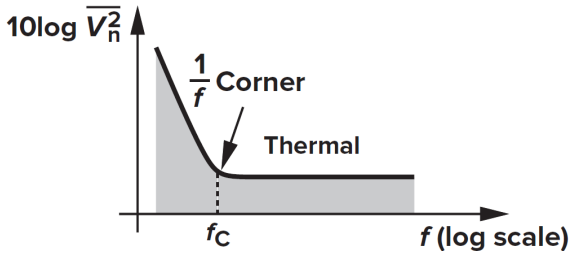


Figure 3.5: Concept of flicker noise corner frequency. [7]

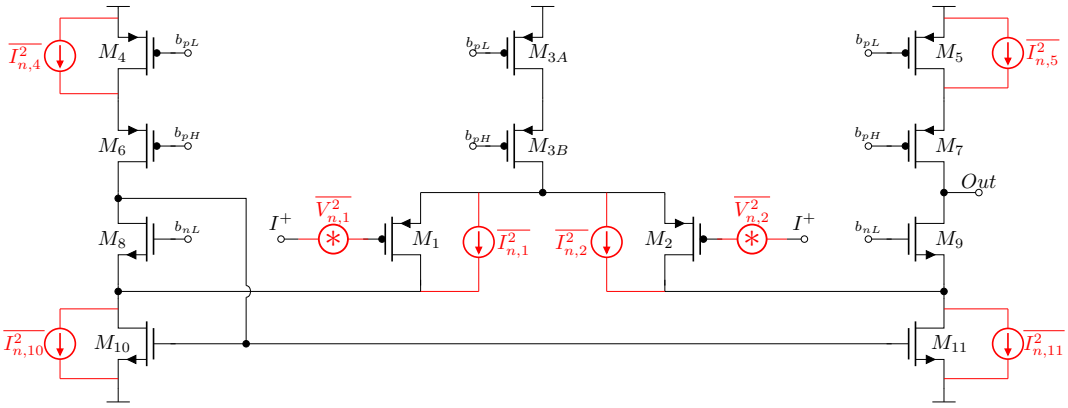


Figure 3.6: FC-OTA Topology with significant noise contributions

Based on the previous information and considering the models shown in Figures 3.4a and 3.4b, it is possible to assign the noise sources associated with the transistors that, according to [58] and [59], contribute to a greater extent, as illustrated in Figure 3.6. Before proceeding with the analysis, according to [7], it is important to assume the following points in order to simplify the analysis:

- The thermal noise (modeled as current sources) is uncorrelated.
- The noise of cascode devices is almost negligible at low frequencies.
- The coefficient γ is equal for all transistors.

The contribution of thermal noise due to the input differential pair M_1 and M_2 is

$$\overline{V_{n,out}^2}\,|_{M_1,M_2} = 2(4kT\gamma g_{m1,2}R_{out}^2) \tag{3.16}$$

In Equation 3.16, the factor 2 accounts for the noise due to M_1 and M_2. Similarly, for the other transistors, we have:

$$\overline{V_{n,out}^2}\,|_{M_4,M_5} = 2\left(4kT\gamma g_{m4,5}R_{out}^2\right) \tag{3.17}$$

$$\overline{V_{n,out}^2}\,|_{M_{10},M_{11}} = 2\left(4kT\gamma g_{m10,11}R_{out}^2\right) \tag{3.18}$$

Thus, the total input-referred noise is the sum of the contributions shown in Equations 3.16 to 3.18, divided by the square of the amplifier's overall gain (A_O).

$$\overline{V_{n,in}^2} = \frac{8kT\gamma}{A_O^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m4,5}}{g_{m1,2}^2} + \frac{g_{m10,11}}{g_{m1,2}^2}\right) \tag{3.19}$$

The flicker noise due to the transistors shown in figure 3.6 is

$$\overline{V_{n,out}^2}\,|_{M_1,M_2} = 2\left(\frac{\kappa_p}{(WL)_{1,2}C_{OX}f}g_{m1,2}^2R_{out}^2\right) \tag{3.20}$$

$$\overline{V_{n,out}^2}\,|_{M_4,M_5} = 2\left(\frac{\kappa_p}{(WL)_{4,5}C_{OX}f}g_{m4,5}^2R_{out}^2\right) \tag{3.21}$$

Similarly, it is possible to determine the total input-referred flicker noise, resulting in the following equation:

$$\overline{V_{n,in}^2} = \frac{2\kappa_p}{C_{OX}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{4,5}}\frac{g_{m4,5}^2}{g_{m1,2}^2}\right) \tag{3.22}$$

The overall input-referred noise (considering both thermal and flicker noise) is the sum of each contribution calculated previously (Equations 3.19 and 3.22).

$$\overline{V_{n,in}^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m4,5}}{g_{m1,2}^2} + \frac{g_{m10,11}}{g_{m1,2}^2}\right) + \frac{2\kappa_p}{C_{OX}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{4,5}}\frac{g_{m4,5}^2}{g_{m1,2}^2}\right) \tag{3.23}$$

3.0.2 Common-Source Amplifier

The common-source amplifier primarily consists of an input transistor (specifically an nMOS in this case) and a load transistor that serves as the bias for the amplifier. The operation of the common-source amplifier relies on the transistor operating in the saturation region. The implementation of this block allows for greater output headroom due to the presence of only two connected transistors. Although this output stage may not provide the highest gain, it offers the advantage of a wider dynamic range at the output.

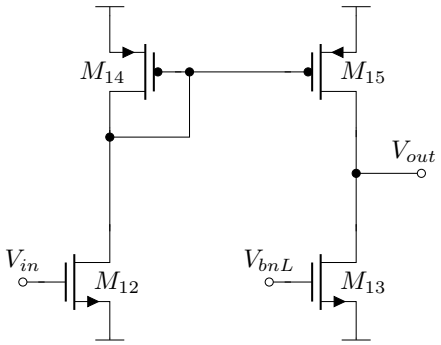


Figure 3.7: Common-Source Amplifier Topology

3.0.2.1 DC Analysis

For a CMOS common-source amplifier, the DC input and output range are constrained by the operating conditions of the MOSFET transistor in the common-source configuration. These ranges depend on the saturation voltage V_{DSat} (the minimum V_{DS} required

to keep the transistor in saturation) and the threshold voltage V_{TH}. The input range is limited by the conditions that ensure the transistor remains in the saturation region.

$$V_{in,min} = V_{GS12} \tag{3.24}$$

To turn on the transistor in saturation region, the input voltage must be greater than the threshold voltage V_{TH}.

$$V_{in,max} = V_{DD} - V_{DSsat14} \tag{3.25}$$

The output range is defined by the operation of the transistor and the load connected to the drain. In the common-source configuration:

$$V_{out,min} = V_{DSat13} \tag{3.26}$$

This ensures that the transistor remains in the saturation region. If V_{out} drops below V_{DSAT}, the transistor will enter the triode region.

$$V_{out,max} = V_{DD} - |V_{DSat15}| \tag{3.27}$$

3.0.2.2 AC Analysis

Analysing the small-signal model of the circuit, the gain of the second stage, similar to Equation 3.5, is given by

$$A_{O2} = g_{m12} \left(r_{O15} \parallel r_{O13} \right) \tag{3.28}$$

If a pole is associated with each of the nodes shown in Figure 3.7, then the poles are obtained as given in Equations 3.29 and 3.30.

$$\omega_D = \frac{1}{\left(r_{O15} \parallel r_{O13} \right) C_L} \tag{3.29}$$

$$\omega_E = \frac{1}{(r_{O12} || g_{m14}^{-1}) C_E} \tag{3.30}$$

Where C_E corresponds to the total capacitance seen at node E:

$$C_E = C_{gs15} + C_{gs14} + C_{ds14} + C_{ds12} \tag{3.31}$$

This results in the following transfer function:

$$A_2(s) = \frac{A_{O2}}{(1 + s/\omega_D)(1 + s/\omega_E)} \tag{3.32}$$

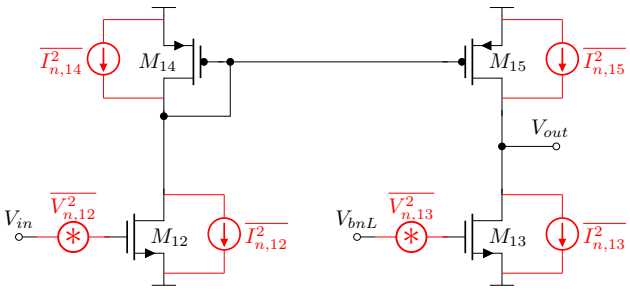


Figure 3.8: CS-Amplifier with noise contributions.

3.0.2.3 Noise Analysis

Similarly to the previous stage, noise analysis considers the contribution of all transistors, as shown in Figure 3.8.
It is possible to consider the individual contributions of each transistor by assuming the points discussed earlier. By also considering the contributions from the current mirror of transistors $M_{14,15}$, we obtain the expression shown in equation 3.33. By assuming the points discussed earlier, the individual contributions of each transistor can be considered (as well as the current mirror composed by the transistors M_{14} and M_{15}), we obtain the expression shown in equation 3.33.

$$\overline{V^2_{n,out}}\,|_{M_{14},M_{15}} = 2(4kT\gamma g_{m14,15}R^2_{out}) \tag{3.33}$$

$$\overline{V^2_{n,out}}\,|_{M_{12}} = 2(4kT\gamma g_{m12}R^2_{out}) \tag{3.34}$$

$$\overline{V^2_{n,out}}\,|_{M_{13}} = 2(4kT\gamma g_{m13}R^2_{out}) \tag{3.35}$$

The total contribution of input-referred thermal noise is obtained by dividing the total output-referred thermal noise by the square of the gain A_{O2}, as shown in equation 3.36.

$$\overline{V^2_{n,in}} = 4kT\gamma\left[\frac{1}{g_{m12}} + \frac{2g_{m14,15}}{g^2_{m12}} + \frac{g_{m13}}{g^2_{m12}}\right] \tag{3.36}$$

Considering the contribution of flicker noise for the transistors M_{12} and M_{13} shown in Figure 3.8.

$$\overline{V^2_{n,out}}\,|_{M_{12}} = \frac{\kappa_n}{(WL)_{12}C_{OX}}\frac{1}{f}g^2_{m12}R^2_{out} \tag{3.37}$$

$$\overline{V^2_{n,out}}\,|_{M_{13}} = \frac{\kappa_n}{(WL)_{13}C_{OX}}\frac{1}{f}g^2_{m13}R^2_{out} \tag{3.38}$$

The total input-referred flicker noise is then

$$\overline{V^2_{n,in}} = \frac{\kappa_n}{fC_{OX}}\left[\frac{1}{(WL)_{12}} + \frac{g^2_{m13}}{g^2_{m12}(WL)_{13}}\right] \tag{3.39}$$

Equation 3.40 shows the input-referred noise due to both flicker noise and thermal noise.

$$\overline{V^2_{n,in}} = \frac{\kappa_n}{fC_{OX}}\left[\frac{1}{(WL)_{12}} + \frac{g^2_{m13}}{g^2_{m12}(WL)_{13}}\right] + 4kT\gamma\left[\frac{1}{g_{m12}} + \frac{2g_{m14,15}}{g^2_{m12}} + \frac{g_{m13}}{g^2_{m12}}\right] \tag{3.40}$$

From Equations 3.23 and 3.40, the following design optimization considerations can be noted:

- The transconductance g_m of the transistors M_1 and M_2 in Equation 3.23 represents one of the significant contributions to thermal noise. Therefore, increasing $g_{m1,2}$ significantly reduces the contribution of thermal noise.
- The dimensions of the transistors directly influence flicker noise, which is inversely proportional to the input-referred noise. Thus, increasing the width-to-length ratio (W/L) of transistors M_1, M_2, M_4, and M_5 reduces the contribution of flicker noise.
- Equation 3.40 reveals the dependence of $\overline{v_{n,in}^2}$ on $g_{m1,2}$, g_{m13}, and $g_{m14,15}$. Therefore, g_{m13} and $g_{m14,15}$ should be minimized because they act more like current sources rather than transconductors.

Table 3.1: Summary Design Parameters

Folded Cascode - OTA	
Parameter	Expression
Min. Input Range	$V_{in,min} = V_{DD} - 2\lvert V_{DSsat3A,3B}\rvert - V_{GS1,2}$
Max. Input Range	$V_{in,max} = V_{SS} + 2\lvert V_{DSsat3A,3B}\rvert + \lvert V_{DSsat1,2}\rvert + V_{DSsat10,11}$
Min. Output Range	$V_{out,min} = V_{SS} + V_{DSsat8,9} + V_{DSsat6,7}$
Max. Output Range	$V_{out,max} = V_{DD} - \lvert V_{DSsat4,5}\rvert - \lvert V_{DSsat6,7}\rvert$
Low Frequency Gain A_O	$-g_{m1,2}\{(g_{m9}r_{O11})r_{ds9}\}\lvert\lvert\{r_{O7}[g_{m7}(r_{O5}\lvert\lvert r_{O7})]\}$
Slew Rate	$\dfrac{2I_B}{C_L}$
Input-Referred Noise	$\overline{V_{n,in}^2} = 8kT\gamma\left(\dfrac{1}{g_{m1,2}} + \dfrac{g_{m4,5}}{g_{m1,2}^2} + \dfrac{g_{m10,11}}{g_{m1,2}^2}\right) + \dfrac{2\kappa_p}{C_{OX}f}\left(\dfrac{1}{(WL)_{1,2}} + \dfrac{1}{(WL)_{4,5}}\dfrac{g_{m4,5}^2}{g_{m1,2}^2}\right)$
Common Source - Amplifier	
Parameter	Expression
Min. Input Range	$V_{in,min} = V_{GS12}$
Max. Input Range	$V_{in,max} = V_{DD} - \lvert V_{DSsat14}\rvert$
Min. Output Range	$V_{out,min} = V_{SS} + V_{DSsat13}$
Max. Output Range	$V_{out,max} = V_{DD} - \lvert V_{DSsat13,15}\rvert$
Low Frequency Gain A_O	$g_{m12}\left(r_{O15} \parallel r_{O13}\right)$
Slew Rate	$\dfrac{I_I}{C_L}$
Input-Referred Noise	$\overline{V_{n,in}^2} = \dfrac{\kappa_n}{fC_{OX}}\left[\dfrac{1}{(WL)_{12}} + \dfrac{g_{m13}^2}{g_{m12}^2(WL)_{13}}\right] + 4kT\gamma\left[\dfrac{1}{g_{m12}} + \dfrac{2g_{m14,15}}{g_{m12}^2} + \dfrac{g_{m13}}{g_{m12}^2}\right]$

3.0.3 Two-Stages Amplifier

Due to the instrumentation amplifier's internal block requirements, the proposed solution uses a two-stage amplifier. The first stage will achieve a high-gain block (constituted by the FC-OTA), while the second stage addresses the necessary swing requirements and improves the CMRR and PSRR (both positive and negative), as shown in Figure 1.9.

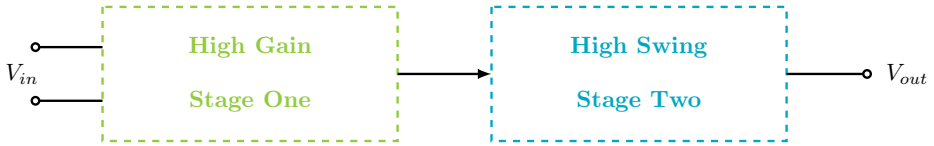


Figure 3.9: Two-Stage Operational Amplifier Requirements by Stage. [7]

Therefore, the DC gain of the entire OTA is the product of the gains of both stages, and thus its transfer function is obtained similarly to what is shown in Equations 3.41 and 3.42.

$$A_T(s) = A_1(s) \cdot A_2(s) \tag{3.41}$$

$$A_T(s) = A_{O1} \cdot A_{O2} \cdot \frac{(1 + s/2\omega_C)}{(1 + s/\omega_L)(1 + s/\omega_A)(1 + s/\omega_B)(1 + s/\omega_D)(1 + s/\omega_E)} \tag{3.42}$$

As observed in Equation 1.42, the primary advantage of using two cascaded amplifiers is the increase in Gain given by the product of AO1 and AO2. However, this configuration introduces instability into the system due to a zero in the transfer function and the five associated poles. Although some of these poles are at high frequencies, they significantly affect the system's frequency response.
Considering the structure shown in Figure 3.9, the proposed two-stage amplifier is illustrated in Figure 3.10.

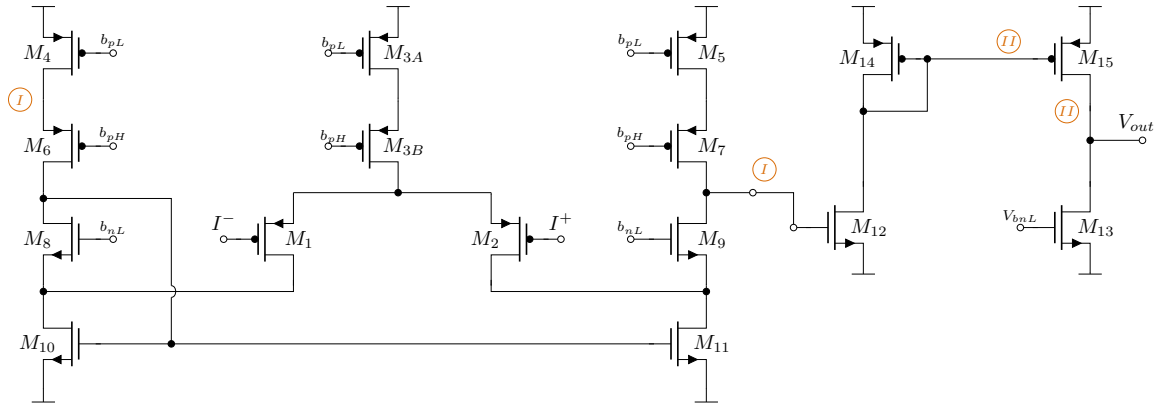


Figure 3.10: Two-Stages Amplifier Topology

3.0.3.1 Indirect Compensation

In real applications, the operational amplifiers are typically employed within a feedback system incorporating passive elements such as resistors (Figure 3.11). The portion of the output signal that is redirected to the input is known as the *feedback factor*, denoted as β. In the ideal operational amplifier configuration shown in Figure 3.11, β is determined by the ratio of the resistances R_1 and R_2 as in shown in Equation 3.43.

$$\beta = \frac{R_2}{R_1 + R_2} \tag{3.43}$$

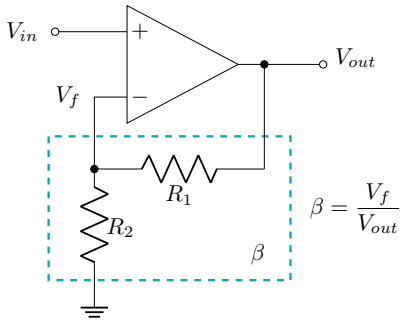


Figure 3.11: Typical Feedback Configuration

The feedback factor β defines the overall behavior of the operational amplifier circuit. By controlling β, the gain, stability, and bandwidth of the amplifier can be manipulated in order to achieve the performance characteristics for a wide range of applications. The closed loop gain is the relationship between the open loop gain (A_{OL}) and the feedback factor as shown in equation 3.44.

$$A_{CL}(f) = \frac{A_{OL}(f)}{1 + \beta A_{OL}} \tag{3.44}$$

Generally, a block diagram can represent a closed-loop system, as shown in Figure 1.12. A_{OL} denotes the amplifier's open-loop Gain and β is the resistor ratio defined by Equation 3.43.

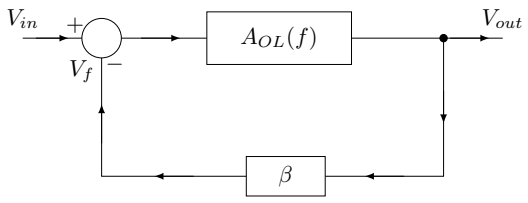


Figure 3.12: Block diagram of the topology shown in Figure 3.11

If the loop gain achieves the condition shown in Equation 3.45, the amplifier's stability

is compromised because the signal phase shift results in 180° (Equation 3.46). This causes the negative feedback to become positive, leading to instability issues.

$$|\beta \cdot A_{OL}(f)| = -1 \tag{3.45}$$

$$\angle\beta \cdot A_{OL}(f) = \pm 180^{\circ} \tag{3.46}$$

According to [8], the low impedance node, labeled as n_{LZ} in Figure 3.10, improves PSRR by isolating the compensation capacitance from V_{DD} and ground noise.

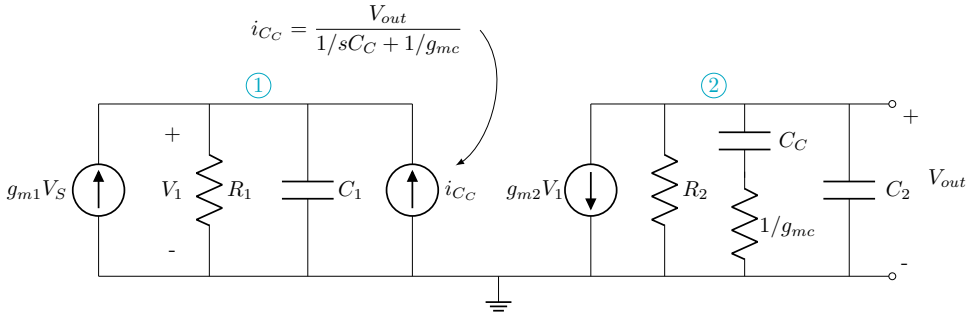


Figure 3.13: Model used to estimate bandwidth with indirect compensation. [8]

Summing the current at node results in the expression 3.47, where $1/g_{mc}$ is the resistance looking into the node v_x, where feedback current is injected.

$$-g_{m1}V_S + \frac{V_1}{R_1||\dfrac{1}{sC_1}} + \frac{V_{out}}{\dfrac{1}{sC_1} + \dfrac{1}{g_{mc}}} = 0 \tag{3.47}$$

In this case, the OA frequency response is estimated as:

$$\frac{V_{out}}{V_S}(s) = \frac{-A_V\left(1 + \dfrac{s}{\omega_z}\right)}{\left(1 + \dfrac{s}{\omega_1}\right)\left(1 + \dfrac{s}{\omega_2}\right)\left(1 + \dfrac{s}{\omega_3}\right)} \tag{3.48}$$

where s_z corresponds to a left hand plane (LHP) zero, the remaing poles are denotes as follows in Equations 3.50 to 3.52

$$\omega_z = \frac{g_{mc}}{C_C} \tag{3.49}$$

$$\omega_1 = \frac{1}{g_{m2}R_1R_2C_C} \tag{3.50}$$

$$\omega_2 = \frac{g_{m2}R_1C_C}{C_L(R_CC_C + R_1C_1)} \approx \frac{g_{m2}C_C}{C_LC_1} \tag{3.51}$$

$$\omega_3 = \frac{R_CC_C + R_1C_1}{R_1C_1R_CC_C} \approx \frac{1}{R_CC_C} \tag{3.52}$$

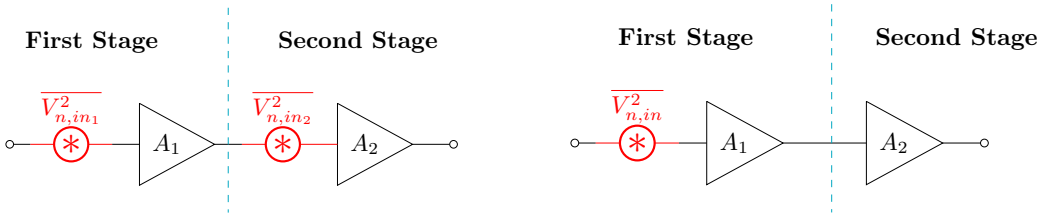
Finally, the unity gain frequency (gain-bandwidth) of the OA is approximately (under the condition $g_{m1} \approx g_{mc}$):

$$f_{un} \approx \frac{g_{m1}}{2\pi C_C} \tag{3.53}$$

All these analyses were developed by [8] and revisited in this chapter to emphasize the advantages of using indirect compensation as a compensation method.

3.0.3.2 Noise Analysis

According to [55], as a two-stage system, the input-referred noise for each stage of the cascaded amplifiers is presented as shown in Figure 3.14a. However, it is possible to refer the noise of the second stage to the first stage, as illustrated in Figure 3.14b and described by Expression 3.54.



(a) Input-Referred Noise Contribution Associated with Each Stage

(b) Total Input-Referred Noise

Figure 3.14: Noise performance of a cascade of amplifiers.

Therefore, the input-referred noise is given by

$$\overline{V^2_{n,in}} = \overline{V^2_{n,in_1}} + \frac{\overline{V^2_{n,in_2}}}{A_2^2} \tag{3.54}$$

Substituting Equations 3.40 and 3.23 into Equation 3.54

$$\begin{aligned}\overline{V^2_{n,in}} = 8kT\gamma &\left(+\frac{1}{g_{m1,2}} + \frac{g_{m4,5}}{g^2_{m1,2}} + \frac{g_{m10,11}}{g^2_{m1,2}}\right) \\ &+ \frac{2\kappa_p}{C_{OX}f}\left(\frac{1}{(WL)_{1,2}} + \frac{1}{(WL)_{4,5}}\frac{g^2_{m4,5}}{g^2_{m1,2}}\right) \\ &+ \frac{1}{A^2_{O2}}\frac{\kappa_n}{fC_{OX}}\left[\frac{1}{(WL)_{12}} + \frac{g^2_{m13}}{g^2_{m12}(WL)_{13}}\right] \\ &+ \frac{4kT\gamma}{A^2_{O2}}\left[\frac{1}{g_{m12}} + \frac{2g_{m14,15}}{g^2_{m12}} + \frac{g_{m13}}{g^2_{m12}}\right]\end{aligned} \tag{3.55}$$

The key point to notice in Equation 3.55 is that the noise of the first amplifier has the most significant effect on the noise performance of the amplifier chain. Therefore, for good noise performance, the design of the first stage is critical.

3.0.4 Instrumentation Amplifier

An instrumentation amplifier is a specialized closed-loop gain block characterized by its differential input and single-ended output referenced to a terminal. This amplifier configuration is particularly noted for its high input impedance and excellent common-mode rejection ratio (CMRR). [60] The conventional structure consists of three feedback-connected amplifiers, as illustrated in Figure 3.15.

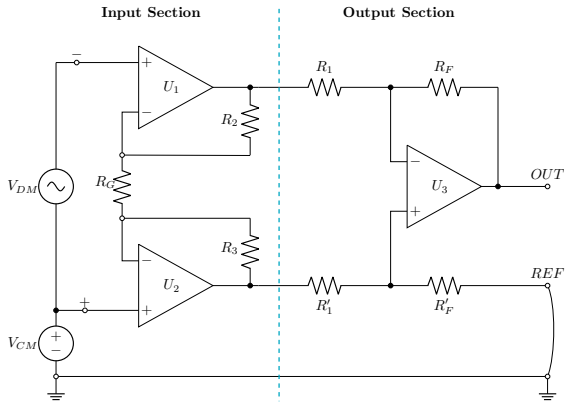


Figure 3.15: The Classic Three Op-Amp IA Circuit

The input stage of the instrumentation amplifier consist of two operational amplifiers (OAs) configured with negative feedback through resistors R_2, R_3, and R_G. This configuration ensures that the amplifier maintains symmetrical input and output characteristics. The output stage, shown in Figure 3.15, is a differential amplifier that converts the differential input into a single-ended output OUT with respect to the reference terminal REF.
Under the condition that the OAs are ideal active elements and the feedback resistor ratios of the differential output stage are equal, as shown in Equation 3.56.

$$\frac{R_F}{R_1} = \frac{R'_F}{R'_1} \tag{3.56}$$

The gain of the instrumentation amplifier is the product of the gains of the input stage and the output stage, as indicated in Figure 3.15 and described by the equation 3.57.

$$A_{IA} = A_{IS} \cdot A_{OS} = \left(1 + \frac{R_2 + R_3}{R_G}\right) \frac{R_F}{R_1} \tag{3.57}$$

where A_{IS} is the differential gain of the input section and A_{OS} is the differential gain of the output section. Equation 3.57 shows that the voltage gain can be varied by changing the value of the resistor RG without affecting the circuit's symmetry. If $R_G = \infty$, then the input section of the IA operates as a voltage follower, and the circuit's differential voltage gain is determined only by the gain of the output section.
In real applications, operational amplifiers (OAs) are not ideal; their gain is limited

within a specific frequency range (bandwidth). The open-loop gain can be approximated by a first-order transfer function, as shown in Equation 3.58.

$$A(s) = \frac{A_{IA}}{1 + s/\omega_P} \tag{3.58}$$

where A_{IA} is the low frequency open-loop voltage gain, and ω_P is the dominant pole of the OA. In this case, the total complex voltage gain of the IA is obtained as a second-order transfer function, containing two real poles. Thus the pole frequencies at $R_2 = R_3 = R$ are

$$\omega'_{P1} = \omega_{P1}(1 + \beta_1 A_{D0,1}) \tag{3.59}$$

$$\omega'_{P2} = \omega_{P3}(1 + \beta_2 A_{D0,3}) \tag{3.60}$$

The feedback coefficients of the input and output section, respectively.

$$\beta_1 = \frac{R_G/2}{R + R_G/2} \tag{3.61}$$

$$\beta_2 = \frac{R_1}{R_1 + R_F} \tag{3.62}$$

According to [60], the total Common-Mode Rejection of the IA is

$$CMRR = A_{U1} CMRR_3 \tag{3.63}$$

where $CMRR_3$ is a parameter directly associated with the common-mode rejection of the amplifier (U_3) and the tolerance of the internal resistors denoted as (δ_R).

$$CMRR = CMRR_{U3} \cdot CMRR_{\delta_R} \tag{3.64}$$

$$CMRR_{\delta_R} = \frac{1 + \dfrac{R_F}{R_1}}{4\delta_R} \tag{3.65}$$

For an IA design, according to [9], it is possible to develop a detailed noise model by applying the models shown in Figures 3.4a and 3.4b for the transistors and associating the thermal noise current with the internal resistors.
From the image shown in Figure 3.16, it can be observed that the largest contribution to the noise comes from the resistors used for the negative feedback of the input stage, as well as from the differential stage of the output stage.
Additionally, it can be noted that the internal operational amplifiers also introduce significant noise, whose contribution was calculated previously (Equation 3.55), although it is smaller in comparison to the feedback resistors. In conclusion, to reduce these sources of noise, the following considerations should be taken into account:

- Consider using resistors with lower values or design techniques that minimize the effective resistance without compromising the stability and gain of the amplifier.
- The design of the transistors in the differential stages can be optimized to reduce flicker noise by using pMOS transistors in the input stage and designing them with a larger area.

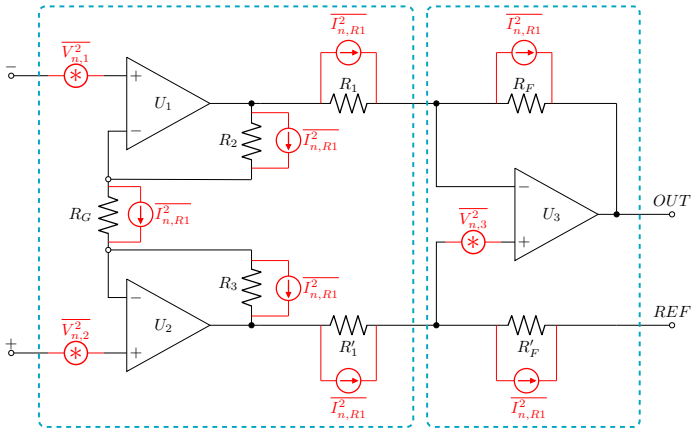


Figure 3.16: Detailed noise model of a Three-Amp IA. [9]

3.1 Design and Verification of the Two-Stages Amplifier

The starting point for the design of the two-stage amplifier is the biasing circuit, which is based on the specifications presented in Table 3.2.

Table 3.2: Design specifications of biasing circuit cell of 250 μA

Parameter	Value
$\lvert V_{D,sat}\rvert$	100 mV
I_B	250 μA
V_{bnH},$\lvert V_{bpH}\rvert$	≈790 mV
V_{bnL},$\lvert V_{bpL}\rvert$	≈550 mV

The topology shown in Figure 3.17, involves the replication of the current i_B (assumed to originate from an external source) for the generation of bias voltages for each cascode stage.
The sizing methodology carried out is as follows, proposing an L = 540nm:

- Transistors M_{0A}, M_{0B}, M_{1A}, and M_{1B}: The selection of W for transistor M_{0A} was carried out by sweeping until the defined $V_{D,sat}$ was achieved. Ideally, transistor M_{0B} would have an exact copy of the current i_B. However, the current is different due to short-channel effects (λ) and mismatch effects.

- Transistor M_2: The function of this transistor is to generate the bias voltage V_{bnH} as defined in Table 3.2. To achieve this, the width (W) of M_2 was modified.

- Transistors M_{2A} and M_{2B}: Were sized to conduct a current i_D = 250 μA at 20% higher than the previously defined $\lvert V_{D,sat}\rvert$. The widths (W) of the transistors are

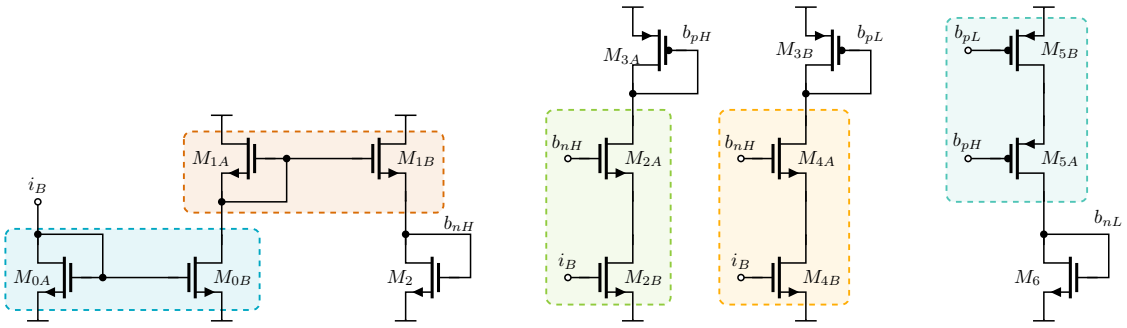


Figure 3.17: Bias Voltage Generation Circuit.

the same in this cascode stage.

- Transistors M_{3A} and M_{3B}: The value of W for these transistors was designed with the objective of obtaining the bias voltages V_{bnL} and $|V_{bpL}|$ at V_{DS}.
- Transistors M_{5A} and M_{5B}: Were sized with the objective of obtaining a pMOS mirror at 250 μA. At this stage, the sizing was done in such a way that the copy is as faithful as possible to 250μA, thus ensuring that M_6 copies the same current and generates a V_{GS} equal to that generated by the source i_B.

The procedure results in the dimensions shown in Table 3.3.

Table 3.3: Dimensions corresponding to the Biasing Stage

Transitor	W_F [m]	L [nm]	NF
M_{0A}	9.62μ	540	8
M_{0B}	10.95μ	540	8
M_{1A},M_{1B}	44.33μ	540	8
M_2	1u	540	8
M_{2A}, M_{2B}	8.2uμ	540	8
M_{3A}	3.73μ	540	8
M_{3B}	44.3μ	540	8
M_{4A}, M_{4B}	8.2μ	540	8
M_{5A}, M_{5B}	46.2μ	540	8
M_6	9.62μ	540	8

The internal amplifier of the instrumentation amplifier (IA) is crucial for the overall system performance. The proposed amplifier is a two-stage design, as shown in Figure 3.10, and its specifications are summarized in Table 3.4. These parameters have been

adjusted to ensure Gain, phase margin, and CMRR for each internal block and the entire instrumentation amplifier. Table 3.5 presents a detailed summary of the final

Table 3.4: Design specifications of 2-Stages Amplifier

Parameter	Value
Closed-Loop Gain [dB]	≥ 85
Phase Margin [degrees]	≥ 55
CMRR [dB]	≥ 120
PSRR (+ and -) [dB]	$\geq$ -60
Slew Rate (+ and -) [MV/s]	≥ 20
IRN [V_{rms}]	$\leq 2\ \mu V_{rms}$

dimensions obtained for the two-stage amplifier, additionally, this table specifies the number of fingers used throughout the design to facilitate floorplanning at the layout level in subsequent stages.

Table 3.5: Dimensions corresponding to the Two-Stage Amplifier.

Transitor	W_F [m]	L [nm]	NF
M_1,M_2	23.1μ	540	8
M_{3A},M_{3B}	23.1μ	540	16
M_4,M_5	10.95μ	540	8
M_6,M_7	1u	540	8
M_8,M_9	8.2uμ	540	8
M_{10},M_{11}	3.73μ	540	8
M_{12},M_{13}	16.4μ	540	8
M_{14},M_{15}	23.1μ	540	8

3.1.1 Simulation and Verification

Figure 3.18 shows the results of the stability analysis of the designed system, considering a closed-loop system. The design exhibits a closed-loop gain of 91.3 dB @ 0 Hz, with a phase margin of 89.64°. Although the compensation makes the system slower, it is necessary for the amplifier to handle resistive loads.

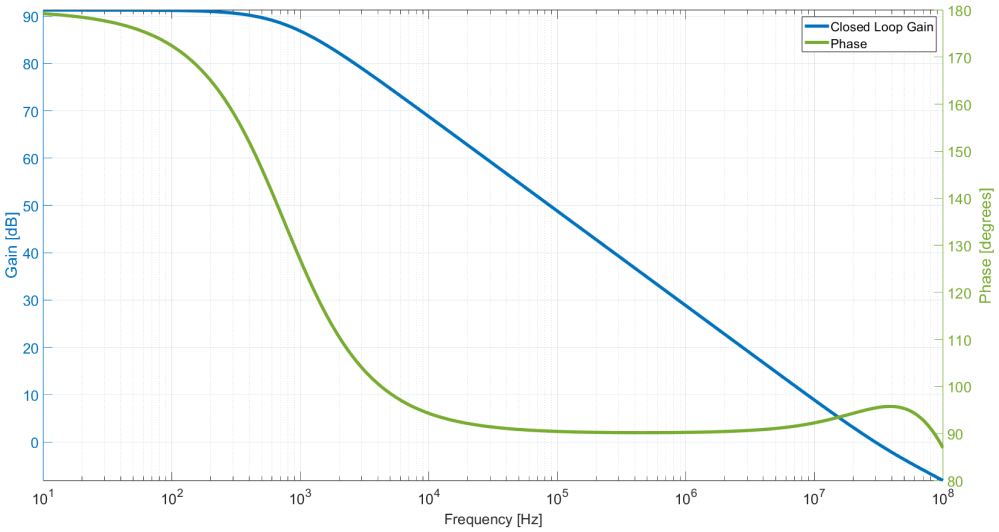


Figure 3.18: Closed Loop Frequency Response of the OTA proposed

The purpose of not using a single-stage output in the amplifier is to improve the total CMRR response of the amplifier. By adding transistors M_{13} and M_{15} in the second stage, an improvement in the internal CMRR of the amplifier was observed, resulting in a CMRR of 141.9 dB @ 0 Hz. The overall CMRR response is shown in Figure 3.19.

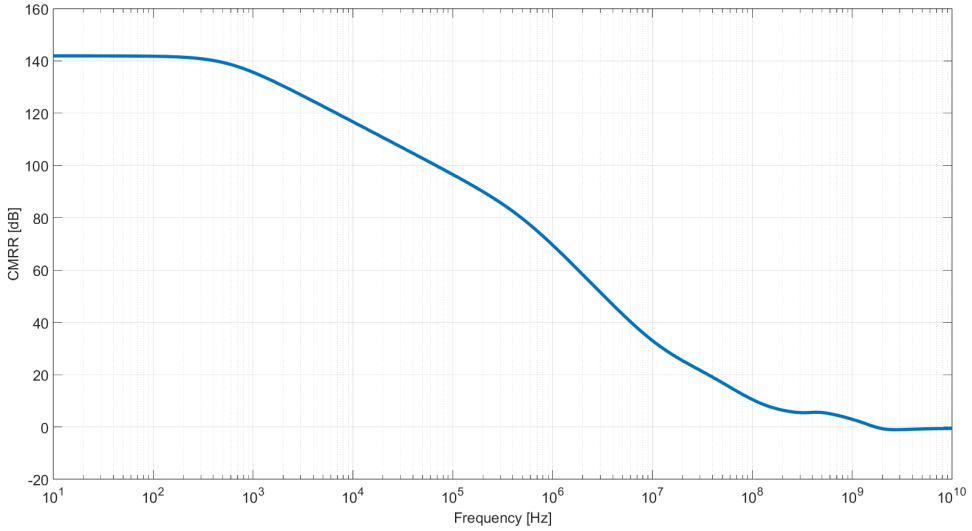


Figure 3.19: CMRR Frequency Response of the OTA proposed

Figure 3.20 shows the PSRR (Positive and Negative Supply Rejection Ratio) responses of the designed Amplifier. Simulations revealed values of -78.86 dB at 0 Hz for positive supply rejection and -81.47 dB at 0 Hz for negative supply rejection, respectively.

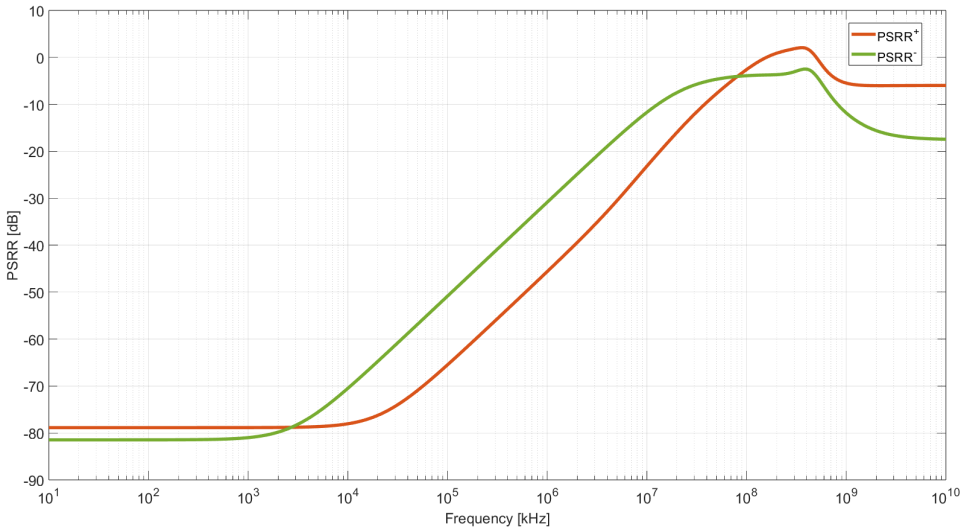


Figure 3.20: Top Design of DDS proposed

The table 3.6 summarizes each of the simulated parameters at a nominal temperature of 40°C, using the typical process model for both capacitors and transistors.

Table 3.6: Summary of nominal characterizations of the two-stage amplifier

Parameter	Value
Closed-Loop Gain [dB]	91.3
Phase Margin [degrees]	89.64
CMRR [dB]	141.9
PSRR (+) [dB]	-78.86
PSRR (-) [dB]	-81.47
Slew Rate (+ and -) [MV/s]	21.64
IRN [V_{rms}]	2.248n
THD [%]	153.3m

3.1.2 Process Variations and Monte Carlo Analysis

Simulations were conducted considering the cases above to evaluate the impact of process variations on the design's performance. These simulations were carried out in Cadence at a nominal temperature of 40°C. Table 3.7 summarizes each of the results obtained in each analysis.

Table 3.7: Results obtained from process variations for the two-stage amplifier.

Parameter	Nominal	SS	FF	FNSP	FPSN
Closed-Loop Gain [dB]	91.3	93.39	88.36	90.39	92.28
Phase Margin [degrees]	89.64	91.18	87.25	89.24	90.03
CMRR [dB]	141.9	139.5	145.5	138.9	145.7
PSRR (+) [dB]	-78.86	-84.01	-72.16	-78.05	-79.85
PSRR (-) [dB]	-81.47	-86.47	-75.07	-80.67	-82.39
Slew Rate [MV/s]	21.64	17.51	26.87	20.68	22.57
IRN [V_{rms}]	2.12n	2.169n	2.276n	2.383n	2.12n
THD [%]	153.3m	179.3m	226.2m	149.2m	143.7m

NOTE: The maximum and minimum values obtained in each simulation are indicated with the colors blue and green, respectively.

A statistical technique known as Monte Carlo analysis was used to analyze how variations in manufacturing parameters, such as transistor width and length, oxide layers, doping, and resistances, affect circuit behavior. This technique allows for evaluating the impact of random variations on circuit performance through a Gaussian response. The results obtained are statistically analyzed to determine the probability of the circuit achieve the design specifications. In this work, a Monte Carlo analysis was conducted, considering 1000 runs for each analysis performed with typical models. The results obtained are summarized in Table 3.8, specifying the mean value and its respective standard deviation.

Table 3.8: Summary of Monte Carlo simulation results for the two-stage amplifier.

Parameter	Mean [μ]	Standard Deviation [σ]
Closed-Loop Gain [dB]	91.26	848.5m
Phase Margin [degrees]	89.64	636.6m
CMRR [dB]	83.75	25.73
PSRR (+) [dB]	-72.87	9.5
PSRR (-) [dB]	-83.32	8.6
Slew Rate (+ and -) [MV/s]	21.62	0.643
IRN [V_{rms}]	2.249n	42.03p
THD [%]	199.2m	47.02m

3.2 Design and Verification of the IA

3.2.1 Simulation and Verification

Due to the gain selectivity of the instrumentation amplifier based on R_G, it was adjusted to achieve an approximate gain of 20 dB for analysing the AC performance of the differential mode gain and CMRR. The results of the nominal simulation are shown in Figure **??**.

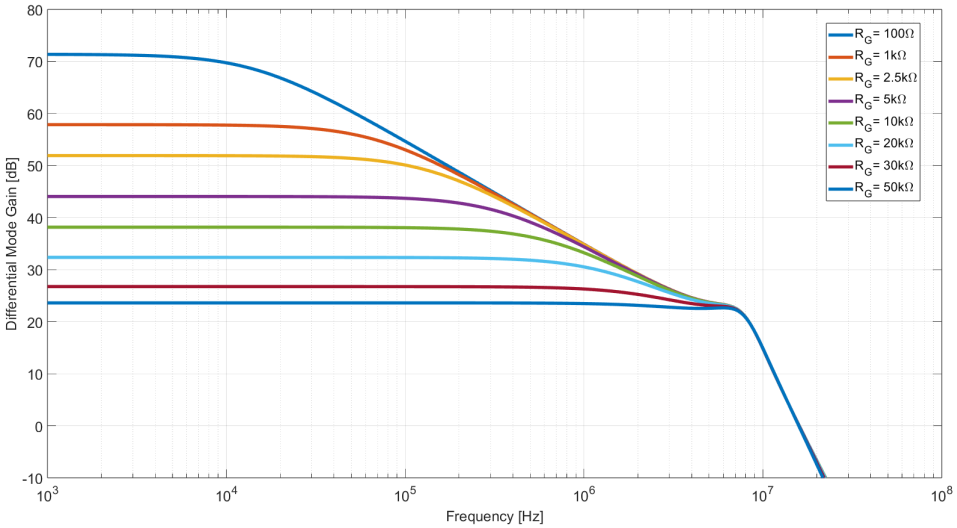


Figure 3.21: Frequency response of the IA at an approximate gain of 20 dB; differential mode gain, common mode gain, and CMRR are shown in green, blue, and orange, respectively.

Figure 3.23 shows the response of the differential mode gain as well as the CMRR for

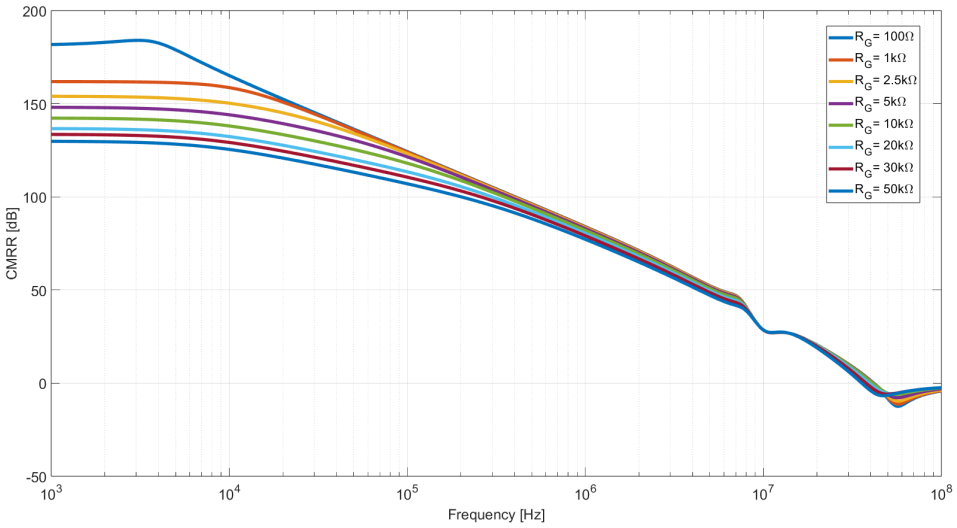


Figure 3.22: Frequency response of the IA at an approximate gain of 20 dB; differential mode gain, common mode gain, and CMRR are shown in green, blue, and orange, respectively.

different values of R_G, aiming to provide a range of gain values over which the IA can operate. Additionally, it can be observed that the CMRR is directly related to the differential mode gain, as explained in Equation 3.64.

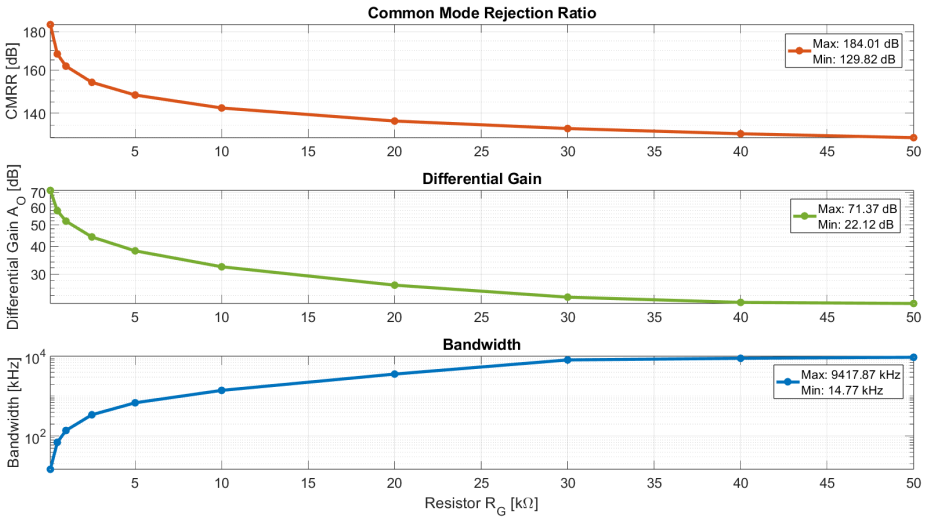


Figure 3.23: Characteristic curve of the differential mode gain (blue) and CMRR (green) as a function of R_G

3.2.2 Monte Carlo Analysis and Process Variations

To verify the robustness of the designed IA, simulations were performed considering process variations of the UMC 180nm technology. Table 3.9 shows the results of the considered corners. Additionally, the maximum and minimum values obtained in the simulation are indicated, which in this case are associated with the FF and SS corners.

Table 3.9: Results obtained from process variations for IA

Parameter	Nominal C.	SS C.	FF C.	FNSP C.	FPSN C.
Gain [dB]	23.41	25.08	21.54	23.26	23.26
CMRR [dB]	125.7	131.3	118.3	124.4	127.2

NOTE: The maximum and minimum values obtained in each simulation are indicated with the colors blue and green, respectively.

Finally, the results of the Monte Carlo analysis with 1000 runs for the differential mode gain and CMRR of the IA are presented. The mean and standard deviation are summarized in Table 3.10. The Gaussian distributions for each of the analyzed cases are provided in the Appendix, in Figures A.6a and A.6b.

Table 3.10: Summary of Monte Carlo simulation results for IA

Parameter	Mean [μ]	Standard Deviation [σ]
Differential-Mode Gain [dB]	23.409	146.736m
CMRR [dB]	105.282	9.637

3.3 Conclusions

In conclusion, the designed amplifier has achieved an optimal differential gain range, providing excellent common-mode rejection ratio (CMRR) that ensures precise operation even in environments with significant noise. The frequency response of the amplifier has been properly adjusted, delivering stable and reliable performance within the frequency range required for Bio-Impedance applications.
Simulations realized under nominal conditions and process variation scenarios have validated the robustness of the design, confirming that the amplifier maintains its expected performance despite inherent variations in manufacturing parameters. The Monte Carlo analyses performed have provided a clear insight into the variability in the amplifier's performance, demonstrating that the design is capable of maintaining its functionality within acceptable margins.
As part of future work, several enhancements can be explored to further optimize the performance and flexibility of the amplifier. One promising avenue is the integration of a resistor selector to enable digital control of the instrumentation amplifier's (IA) gain. This would provide a higher degree of flexibility and allow dynamic adjustments in real-time to better suit diverse application scenarios. Additionally, the internal topology of the amplifier could be refined to support internal delimitation of the working band, particularly to align with the β dispersion range, enhancing the system's adaptability to bio-impedance variations. Furthermore, replacing the existing internal resistive structure with a capacitive alternative could be considered. This modification would facilitate the precise delimitation of the IA's lower frequency band, potentially improving its suitability for low-frequency applications and extending its range of operation. These proposed advancements would not only strengthen the amplifier's versatility but also broaden its applicability in complex bio-medical and research environments.

Table 3.11: Comparison of the implemented design against the state of the art

	NGCT, 2016 [61] (Simulated)	**ICICM, 2019 [62] (Post Layout Simmulation)**	**ICECS, 2014 [63] (Simulated)**	**MSCAS, 2014 [64] (Simulated)**	**This Work (Post Layout Simmulation)**
Process	180 nm	180 nm	180 nm	130 nm	180 nm
Supply Voltage	NS	±0.9 V	1.8 V	NS	±0.9 V
Power	409.14 μW	38.88 μW	90 μW	93.56 μW	810μW
Gain	79.16 dB	101.61 dB	Min: 34 dB Max: 60 dB	32.2	Min: 26 dB Max: 76 dB
Bandwidth	NS	20 - 777.5 kHz	NS	100 Hz	1k - 1.5 MHz
PSRR	NS	148.21 dB (+), 154.7 dB (-)	NS	67.2 dB	-
IRN	9.65 μV/$\sqrt{Hz}$	NS	145 nV/$\sqrt{Hz}$	2.72 μV_{rms}	2.72 μV_{rms}

NS : Not Specified
IRN : Input Referred Noise

CHAPTER 4

Conclusions

The QFGT-modified Ring Oscillator shows a frequency performance aligned with expectations, depending on the feedback factor and the tuning voltage. Initially, this topology was designed with a resistive structure, which allowed, at the simulation level, the establishment of the operating point for the QFGT structure in the transistor connected as a diode. Subsequently, the topology was optimized to include capacitors, thus fulfilling the concept of QFGT at the load.

On the other hand, the second proposal leverages the advantages of using a standardized hardware description language, such as Verilog, to instantiate simple modules with specific functions within a more complex topology. This modular approach not only enhances design versatility but also facilitates implementation across different technology nodes.

Finally, the modular design of analog blocks allowed for the precise definition of parameters for each block while optimizing the system at the floorplan-level. As a result, a high-performance instrumentation amplifier was designed, characterized by a wide range of adjustable gain and high CMRR, meeting the requirements of ongoing BIS applications. The proposed ring oscillator and the designed amplifiers were validated at the nominal corner, under different process corners, and through a 1000-run Monte Carlo analysis, ensuring robustness.

In addition to the results obtained, it is important to highlight that the proposed methodologies and topologies show great potential for adaptation to new applications in the field of signal conditioning and embedded systems. The optimizations performed, such as the implementation of capacitive feedback and the modular design in hardware description language, over a flexible platform for customization in various technological environments. However, particular areas for improvement were identified, such as integrating more advanced digital control techniques to enhance parameter adjustment precision and incorporating noise mitigation strategies for susceptible applications. These extensions open new opportunities to explore the performance of the topologies in more complex scenarios, including environments with high process variability and extreme operating conditions.

Recommendations for future work

This research work has developed and analyzed several topology proposals. Below is a list of potential improvements that could be explored in future work:

- **Additional characterization of the QFGT-modified Ring Oscillator**: It is recommended to complement the analysis with jitter and phase noise studies. Additionally, a digital control system could be implemented to allow specific feedback (β) values and tuning voltages (V_{Tune}), enabling the generation of signal with a wide frequency range.

- **Extension of the Maneatis Cell modification**: The resistive configuration of the Maneatis Cell was optimized and later adapted to capacitive feedback, allowing the transistor to function as a summing point for local output signals. This structure could be extended for use in other conventional and fully differential delay cell topologies.

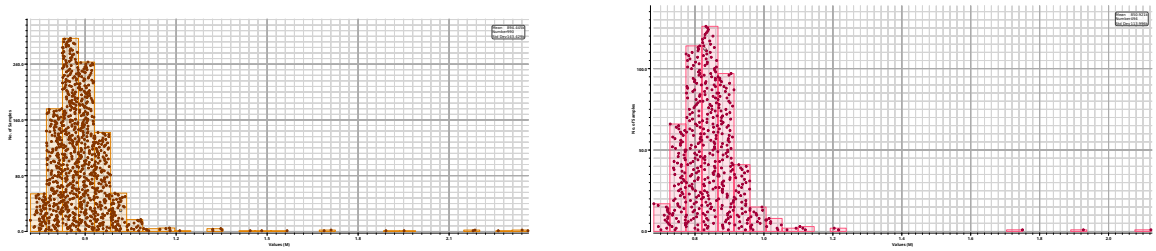
- **Optimization to DDS implementation**: Since DDS implementation requires Digital-to-Analog converters, it is suggested to incorporate Dynamic Element Matching (DEM)[65] techniques to mitigate undesirable effects inherent to the manufacturing process.

- **Optimization of the instrumentation amplifier design**: Integrating a resistor selector to control gains via digital words is proposed, adding greater flexibility and precision to the design.

APPENDIX A

Monte Carlo Simmulations

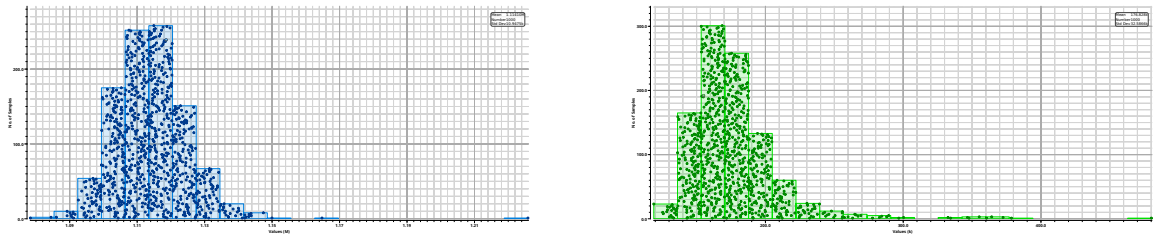
This section presents the Gaussian distributions corresponding to each of the Monte Carlo simulations for the analyses shown in Table 2.9. Figure A.1a shows the results of the transient simulation for a V_{Tune} = 650 mV, corresponding to the 5-stage Ring Oscillator based on topology A. Figure A.1b shows the Gaussian distribution corresponding to the time response of the same 5-stage Ring Oscillator based on topology B.



(a) (b)

Figure A.1: Monte Carlo Results for Transient Analysis. a) Topology A-based RO. b) Topology B-based RO.

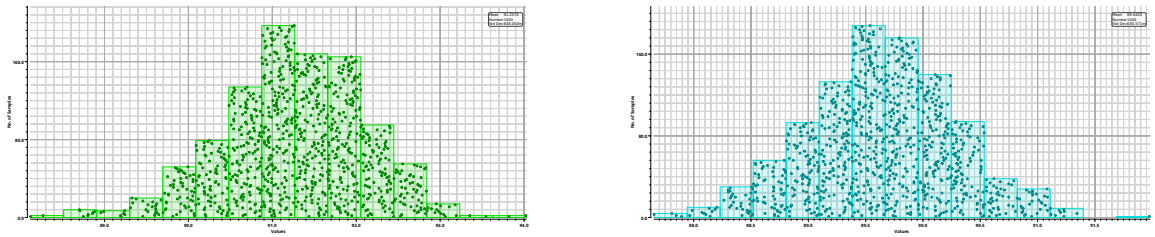
The responses shown in Figure A.2 summarize the Monte Carlo analysis responses of the 5-stage Ring Oscillator based on topology C, for two cases of feedback factor β = 0.5 in Figure A.2a and β = 0.1 in Figure A.2b.



(a) (b)

Figure A.2: Monte Carlo Results for Transient Analysis. a) RO with β=0.5 b)RO with β=0.1

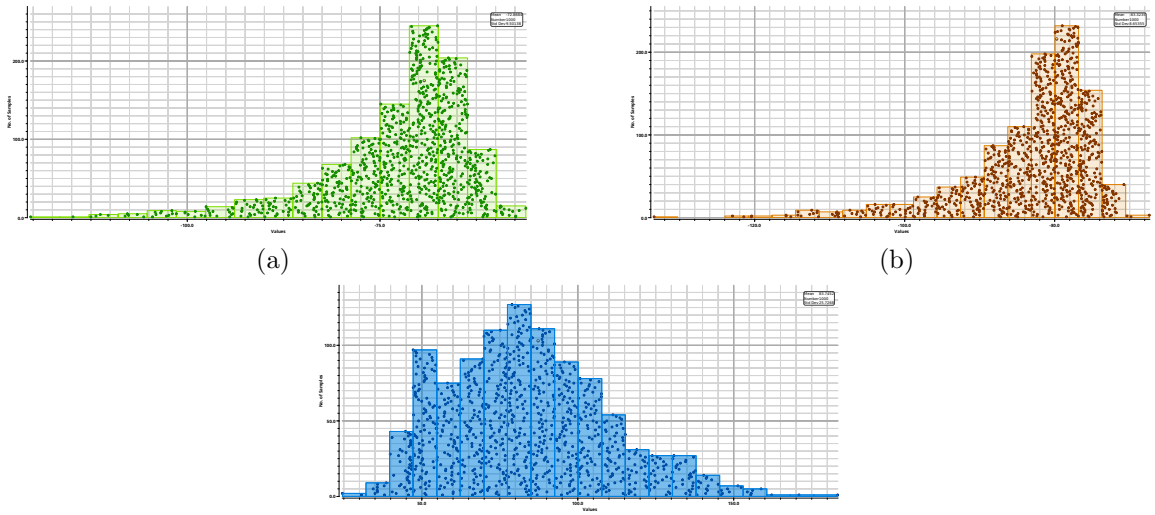
This section presents the Gaussian distributions corresponding to each of the Monte Carlo simulations for the analyses shown in Table 3.8. Figure A.3 shows the results of the closed-loop stability simulation of the two-stage amplifier. Figure A.3a shows the Gaussian distribution of the Closed-Loop Gain, and Figure A.3b corresponds to the phase margin associated with the Closed-Loop configuration. The figures shown in



(a) (b)

Figure A.3: Monte Carlo Results for Stability Analysis. a) Closed-Loop Gain. b) Phase Margin.

A.4 present the responses associated with the rejection ratio of the two-stage amplifier. Figure A.4a shows the results of the positive PSRR (measured at 0 Hz) of the amplifier, while Figure A.4b represents the negative PSRR (measured at 0 Hz). Finally, Figure A.4c shows the results of the low-frequency (0 Hz) measurement of the CMRR.

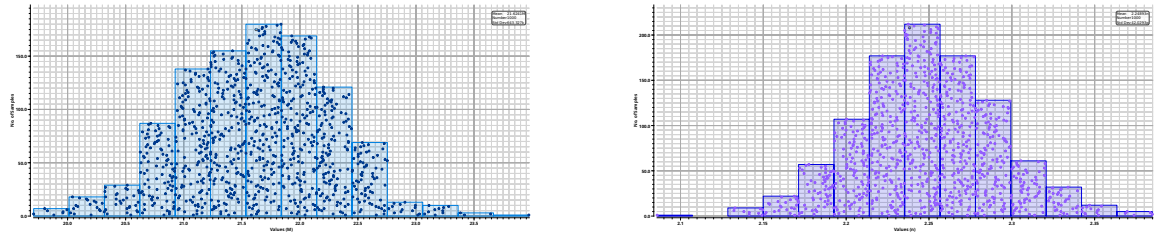


(a) (b)

(c)

Figure A.4: Monte Carlo Results for Stability Analysis. a)$PSRR^+$ b)$PSRR^-$ c) $CMRR$

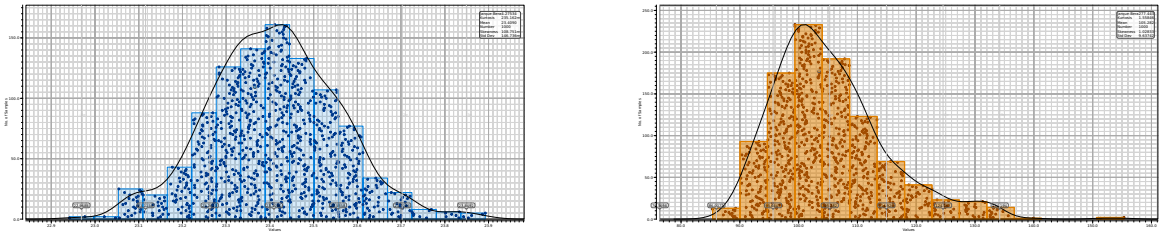
Figure A.5 presents the results of the measurements corresponding to the Slew Rate and IRN. In Figure A.5a, only the results for SR^+ are shown because the negative Slew Rate (associated with the high-to-low signal transition) is approximately the same. Finally, Figure A.5b shows the Gaussian distribution of the measurements corresponding to the IRN.



(a) (b)

Figure A.5: Monte Carlo simulation results. a) Slew Rate (+) b) IRN

Figure A.6 shows the performance results of the instrumentation amplifier. Figure A.6a presents the Gaussian distribution corresponding to the gain measurement results of the IA for a configuration of approximately 20 dB, and Figure A.6b summarizes the results corresponding to the CMRR of the same configuration.



(a) (b)

Figure A.6: Monte Carlo Results for AC Analysis. a) Gain. b) CMRR.

APPENDIX B

Layout Designs

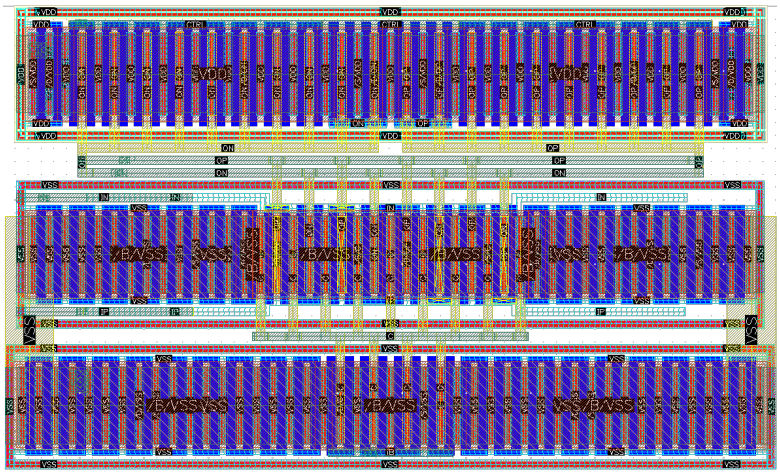


Figure B.1: Final Layout of the Basic Maneatis Cell Delay (**Topology A**)

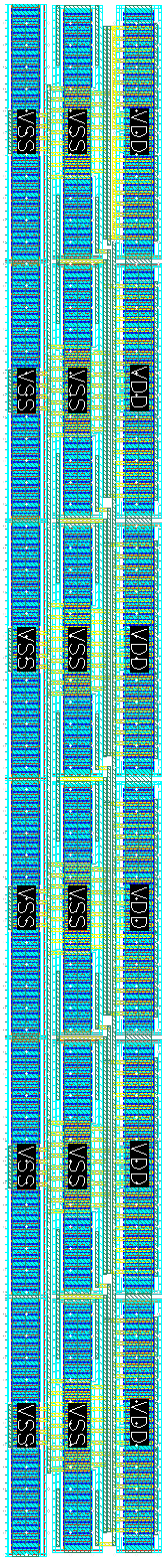


Figure B.2: 5-stages Ring Oscillator considering the Topology A

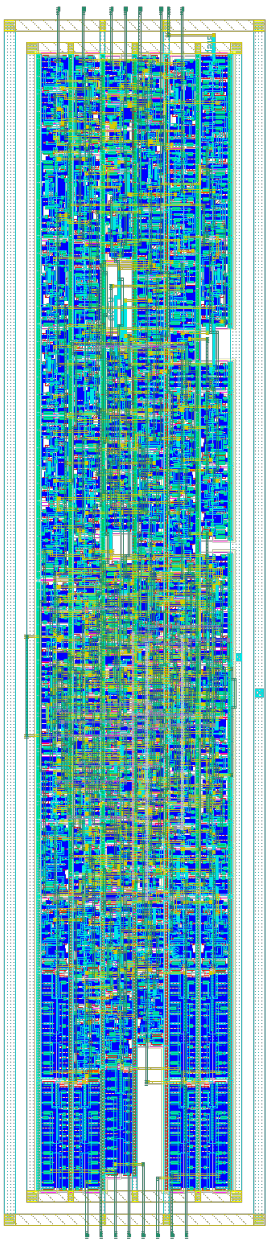


Figure B.3: Final Layout proposal for the proposed DDS

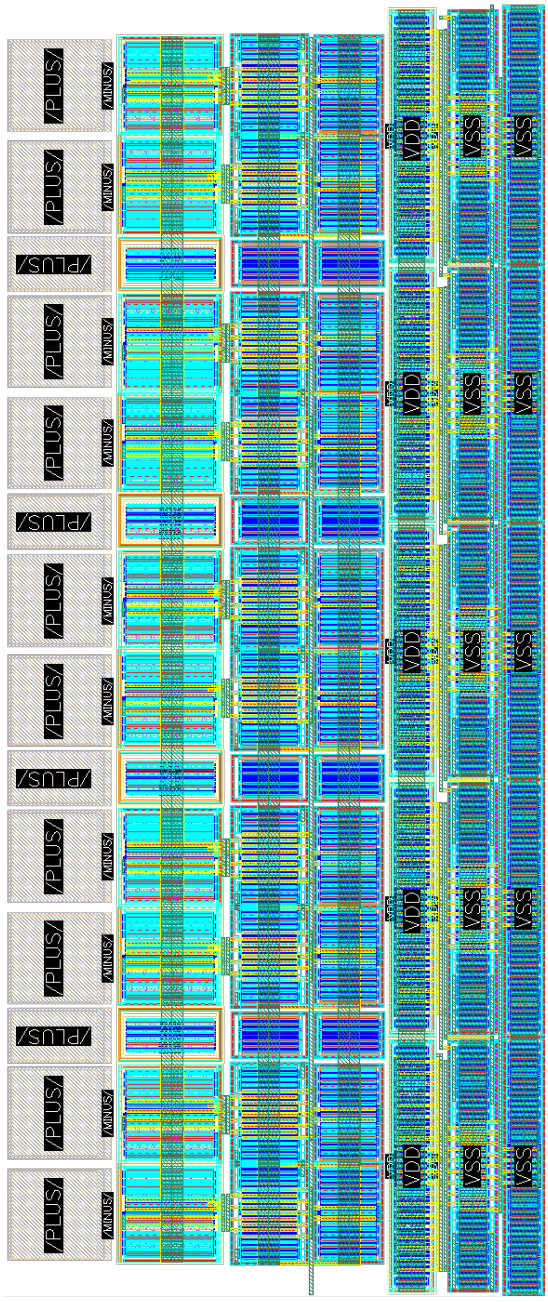


Figure B.4: 5-stages Ring Oscillator considering the Topology B

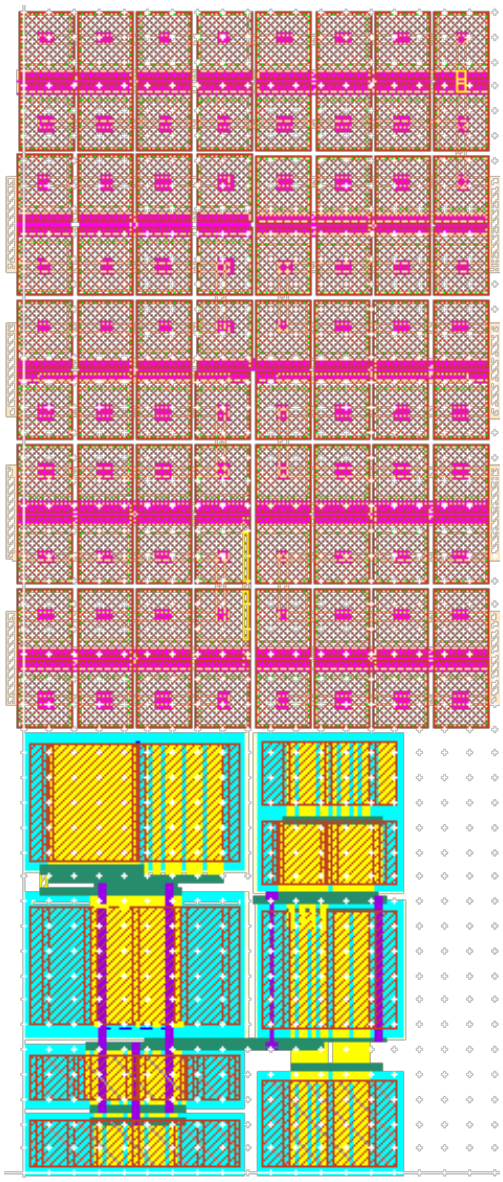


Figure B.5: Final Layout of the Basic Maneatis Cell Delay (**Topology A**)

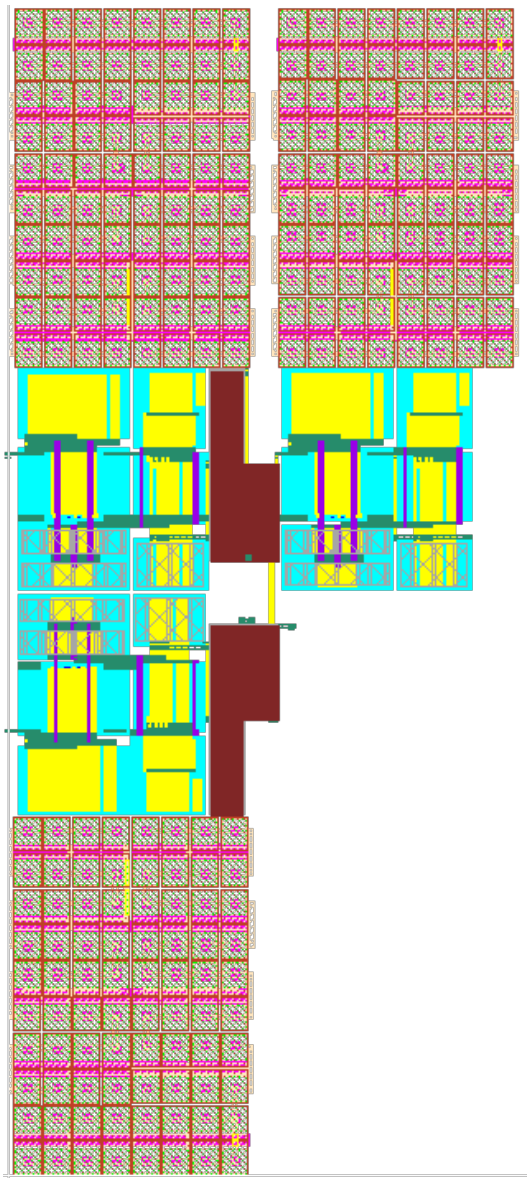


Figure B.6: Final Layout of the Basic Maneatis Cell Delay (**Topology A**)

APPENDIX C

Verilog Codes

Phase Accumulator Module

```
1  module phaseAccm (
2      input wire clk,
3      input wire rst,
4      input reg [4:0] step,
5          output reg [5:0] phaseComp,
6          output reg readEn,
7          output reg msbFlg
8  );
9          reg [7:0] phase0;
10     always @(posedge clk or posedge rst) begin
11         if (rst) begin
12             phase0 <= 8'b00000000;
13                         readEn <= 1'b0;
14         end else begin
15                         readEn <= 1'b1;
16                         phase0 <= phase0 + step;
17                         msbFlg <= phase0[7];
18                         if (phase0[6]) begin
19                                 phaseComp <= ~(phase0[5:0]);
20                         end else begin
21                                 phaseComp <= (phase0[5:0]);
22                         end
23                 end
24         end
25 endmodule
```

Frequency Divider Module

```
1     module freqDiv (
2     input wire clkMaster,
3     input wire rst,
4     input wire [1:0] select,
5     output reg clkOutput
6 );
7     reg [2:0] counter;
8     reg [2:0] max_count;
9
10    always @(posedge clkMaster or posedge rst) begin
11        if (rst) begin
12            counter <= 3'b000;
13            clkOutput <= 0;
14        end else begin
15            if (counter == max_count) begin
16                clkOutput <= ~clkOutput;
17                counter <= 3'b000;
18            end else begin
19                counter <= counter + 1;
20            end
21        end
22    end
23
24    always @(*) begin
25        case (select)
26            2'b11: max_count = 3'b000; // fclk/2
27            2'b10: max_count = 3'b001; // fclk/4
28            2'b01: max_count = 3'b010; // fclk/6
29            2'b00: max_count = 3'b011; // fclk/8
30        endcase
31    end
32 endmodule
```

Direct Digital Synthetizer Module

```
    module sinWaveGen(
    input wire clkM,
    input wire reset,
    input wire [3:0] stepFreq,
    input wire [1:0] selectI,
    output wire [7:0] dataO
);
    wire clkO;                  // Clock signal from freqDiv
    wire [5:0] phaseComp;       // Phase accumulator output
    wire readEnable;            // Read enable signal
    wire MSBflag;               // MSB flag from phase accumulator
    wire [7:0] sigOut;          // Signal output from LUT

    phaseAccm U1 (
        .clk(clkO),
        .rst(reset),
        .step(stepFreq),
        .phaseComp(phaseComp),
        .readEn(readEnable),
        .msbFlg(MSBflag)
    );

    LUT U2 (
        .clk(clkO),
        .read(readEnable),
        .address(phaseComp),
        .comFlag(MSBflag),
        .data(sigOut)
    );

    freqDiv U3 (
        .clkMaster(clkM),
        .rst(reset),
        .select(selectI),
        .clkOutput(clkO)
    );

    assign dataO = sigOut; // Assign the output of LUT to dataO

endmodule
```

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