Widely Tunable Band-Pass ΣΔ ADCs: Modulators and Decimators

por

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Abstract

In recent years, the increase in the number of wireless networks has motivated the research in Software Defined Radios (SDRs). SDRs are expected to directly convert Radio-Frequency (RF) signals to the digital domain, facilitating software-based signal processing. In the open literature it has been presented that LC-based Band-Pass Continuous-Time ΣΔ Modulators (BP CT-ΣΔM) can be used for the implementation of RF-to-digital converters. However, most of reported LC-based BP CT-ΣΔMs have used a fixed center or notch frequency, limiting the covered RF signals range.

The first part of this thesis presents bandpass continuous time ΣΔ modulators with a widely programmable notch frequency for the efficient digitization of radio-frequency signals in the next generation of SDRs. The modulator architectures under study are based on a fourth-order loop filter - implemented with two LC-based resonators - and a finite-impulsive-response feedback loop. Several topologies are studied, considering three different cases for the embedded digital-to-analog converter, namely: return-to-zero, non-returnto- zero and raised-cosine waveform. In all cases, a notch-aware synthesis methodology is presented, which takes into account the dependency of the loop-filter coefficients on the notch frequency and compensates for the dynamic range degradation due to the variation of the notch. The synthesized modulators are compared in terms of their sensitivity to main circuit error mechanisms and the estimated power consumption over a notch-frequency tuning range of $0.1f_s$ to $0.4f_s$. The use of passive circuits for the implementation is also discussed considering either a fully passive or an hybrid active/passive circuit realization of the embedded resonators. Time-domain behavioral and macromodel electrical simulations validate this approach, demonstrating the feasibility of the presented methodology and architectures for the efficient and robust digitization of radio-frequency signals with a scalable resolution and programmable signal bandwidth.

Digital-Down-Converters (DDCs) are required to complete RF-to-Digital conversion in order to down-convert digital BP signals to baseband signals and to reduce the high sampling rate to the Nyquist rate. The heart of DDCs is a pair of Low-Pass (LP) decimators (for the In-phase and Quadrature components), where the first decimation stage is usually

implemented with comb-based decimators. The second part of this thesis focuses on comb-based decimators. It is proposed a two-stage comb-based decimation structure, where the first stage is in a non-recursive form and the second stage is in a recursive form (CIC). A design methodology, which is based on power and area estimations, is presented in order to choose the best values for the first and second decimation factors, M_1 and M_2. The proposed structure simultaneously shows the power efficiency of non-recursive comb and the area efficiency of CIC, when it is designed for high values of the decimation factor that are power of two. Similarly, the presented two-stage structure can be used for decimation factors that are even numbers, featuring less power consumption and similar area requirements than the equivalent CIC. Furthermore, the two-stage structure is easily modified to cope with decimation factors that are power of three and integer multiples of three. In terms of frequency response, modified structures are presented, which improve the folding band attenuations and correct the passband droop without severally penalizing the power and area efficiency. These modifications are based on the use of simple filters working at a low sampling rate. VHDL implementation results, in both a CMOS technology and an FPGA, are shown to validate the proposed approach.

Resumen

En la actualidad, el reciente incremento en el número de redes inalámbricas ha motivado la investigación en el campo de Radios Definidos por Software (RDS). Idealmente, los RDS deben convertir, directamente, señales de Radio Frecuencia (RF) en señales digitales, de tal forma que éstas puedan ser fácilmente procesadas mediante el uso de software. En la literatura abierta se han presentado Moduladores Sigma-Delta (MΣΔ) de tiempo continuo, pasa banda y basados en resonadores LC, los cuales pueden ser usados en la construcción de convertidores de RF a digital. Sin embargo, la mayoría de los MΣΔ reportados han usado una frecuencia central fija, lo cual limita el rango de señales RF que se puede cubrir.

La primera parte de esta tesis presenta varios MΣΔ pasa banda con una frecuencia central que es altamente sintonizable, los cuales son adecuados para su uso en RDS. Los MΣΔ bajo estudio están basados en un filtro de lazo de cuarto orden implementado con dos resonadores LC. En la trayectoria de retroalimentación se consideran coeficientes con respuesta al impulso finita, además de diferentes formas de onda para el Convertidor Digital a Analógico: no retorno a cero, retorno a cero y cosenoidal. Estos moduladores son sintetizados a partir de una metodología propuesta denominada "*notch-aware*", la cual considera la dependencia de los coeficientes de lazo sobre la variación de la frecuencia central y compensa la pérdida de rango dinámico debido a esta variación. Todos los moduladores sintetizados son comparados en términos de su sensibilidad a los principales mecanismos de error y su consumo de potencia dentro del rango de sintonización de 0.1 a 0.4 veces la frecuencia de muestreo. Adicionalmente, se discute el uso de circuitos pasivos para la implementación del filtro de lazo, lo que conlleva al desarrollo de arquitecturas hibridas (activo/pasivo) y completamente pasivas. Simulaciones en macro-modelos y simulaciones eléctricas son usadas para validar la metodología propuesta, lo cual demuestra su factibilidad para el diseño de moduladores eficientes y robustos en aplicaciones de RDS.

Los Reductores de Frecuencia de Muestreo (RFM) son necesarios para completar la conversión de RF a digital, mediante la conversión de señales pasa banda en señales de banda base y la reducción de la frecuencia de muestreo a la razón establecida por Nyquist. La parte fundamental de los RFM son los filtros decimadores pasa baja (para las

componentes de cuadratura y fagse), donde la primera etapa de decimación usualmente es implementada por un filtro *comb*.

La segunda parte de esta tesis se enfoca en los decimadores comb. Se propone un decimador de dos etapas, donde la primera etapa es un decimador comb no recursivo (M_1) y la segunda etapa un decimador comb recursivo (M_2). Con base en estimaciones de potencia y área, se propone una metodología que permite elegir los mejores valores para M_1 y M_2. De esta manera, el decimador propuesto exhibe, simultáneamente, la eficiencia en potencia del decimador comb no recursivo y la eficiencia en área del decimador comb recursivo, siempre y cuando el valor total de decimación es grande y una potencia de dos. De forma similar, el decimador propuesto puede ser usado con valores de decimación que son números pares, en este caso el consumo de potencia se ve reducido y el área sufre un ligero incremento cuando es comparado con el del decimador comb recursivo. Además, el decimador propuesto se puede modificar fácilmente para tratar con valores de decimación que son potencia de tres y múltiplos enteros de tres. En términos de respuesta en frecuencia, se presentan decimadores modificados, donde simultáneamente se mejora la atenuación en la banda de rechazo y se compensan la caída en la banda de paso sin penalizar severamente la eficiencia de potencia y de área. Esas modificaciones están basadas en el uso de filtros simples que operan en una baja frecuencia de muestreo. Implementaciones en VHDL validan estos resultados.

Preface

The use of wireless networks is very usual in today's life, 2015 year. It is very common to call a friend by using cellular networks, to access the internet through WiFi networks, to listen music with wireless Bluetooth headphones, to listen conventional FM radio, among others.

The superheterodyne receiver is the most common type of radio-receiver. In this model, all incoming Radio-Frequency (RF) signals are converted to a common Intermediate-Frequency (IF), for additional amplification and selectivity, prior to demodulation. In order to cope with different wireless networks a super heterodyne receiver must have different hardware blocks to perform the demodulation of the targeted network- making it an expensive solution in multi-networks devices.

A more efficient solution is the use of the so called Software-Defined-Radios (SDRs), where most of the signal conditioning and signal processing is done in the digital domain by running software in Digital Signal Processors (DSPs) – increasing the programmability and adaptability to a large number of wireless communication networks.

Universal-Software-Radio-Peripherals (USRPs) are software-based radio receivers, mainly used in research labs and universities. USRPs are based in Direct-Conversion-Receivers (Zero IF receivers), where RF signals are directly downconverted to baseband without passing through an IF stage. Baseband signals are converted with high bandwidth Analog-to-Digital Converters (ADCs), and then they are sent to DSPs for software-based demodulation.

However, USRPs are still far from SDRs originally conceived by Joe Mitola [1]. He envisioned that in SDRs all the signal conditioning and signal processing must be perform in the digital domain, which means that RF signals must be directly converted to the digital domain by placing ADCs right after the antenna. One of the most critical building blocks, which eventually will enable such a technology, is the ADC.

Recent advances in LC-based Band-Pass (BP) Continuous-Time (CT) Sigma-Delta Modulation (ΣΔM) techniques are pushing RF-to-digital conversion forward. LC-based BP CT-ΣΔMs employ noise shaping around a center or notch frequency (f_n), where incoming RF signals are placed. In most of the reported designs the notch frequency is fixed at a quarter of the sampling frequency (f_s), i.e $f_n = f_s / 4$; therefore, a widely programmable PLL-based synthesizer is required to cover all the RF spectrum. A better solution would be the use of a tunable notch frequency: however, very few works have been presented for designing LC-based BP CT-ΣΔMs with tunable f_n. To the best of the author knowledge, the widest tuning range achieved by LC-based BP CT-ΣΔMs was reported by Gupta *et al* [2], featuring a 0.8-2GHz notch-frequency range thanks to the combination of reconfiguration in discrete f_n steps and under-sampling techniques.

Thus, one objective of this thesis is to develop a methodology for the design of LC-based BP CT-ΣΔMs with a widely tunable notch frequency in order to increase the covered RF spectrum by LC-based BP CT-ΣΔMs.

Digital-Down-Converters (DDCs) are required to complete RF-to-Digital conversion. DDCs use Numeric Controlled Oscillators (NCOs), along with digital multipliers, to perform Band-Pass to baseband down-conversion. NCOs are easily implemented by look-up tables with pre-stored coefficients for the generation of sine and cosine digital waves; thus, the design of these circuits is not considered in this thesis. The heart of the DDC is a pair of Low-Pass decimators (for the In-phase and Quadrature components), which reduce the high throughput of the modulator to the Nyquist rate required by the targeted wireless application.

Comb decimation filters are widely use as the first decimation stage, because they are very simple to implement thanks to their unitary filter coefficients, where neither multipliers nor memory storage are required for their implementation. However, comb filters themselves cannot satisfy high performance demands of LC-based BP CT-ΣΔMs, where the sampling rate must be reduced from the GHz range to tens or hundreds of MHz while preserving good characteristics in the decimated signal.

Thus, the second objective of this thesis is the design of low power comb-based decimators with improved frequency responses in order to efficiently use them in LC-based BP CT-ΣΔMs.

Major contributions of this thesis

Widely Tunable LC-based BP CT-ΣΔMs

It is presented a notch-aware synthesis methodology suitable for the design of widely tunable LC-based BP CT-ΣΔMs, which takes into account the dependency of the loop-filter coefficients on the notch frequency and compensates for the dynamic range degradation due to the tunable operation. Several 4th order topologies are presented, considering three different cases for the embedded Digital-to-Analog Converter (DAC), namely: return-to-zero, non-return-to zero and raised-cosine. The synthesized modulators are compared in terms of their sensitivity to main circuit error mechanisms and the estimated power consumption over a notch-frequency tuning range of 0.1fs to 0.4fs.

Widely Tunable Passive LC-based BP CT-ΣΔMs

The presented notch-aware synthesis methodology is extended to the use of passive circuits for the implementation of widely tunable LC-based BP CT-ΣΔMs. Several alternative loop filters, considering either a fully passive or an hybrid active/passive circuit realization of the embedded resonators are considered. Time-domain simulations validate the presented approach, showing the feasibility of using fully passive and hybrid active/passive resonators to implement LC-based BP CT-ΣΔMs.

Power and area efficient comb-based decimators

It is presented a two-stage comb-based decimator, which is efficient in terms of both power and area. This decimator is intended for high values of the decimation factor that are power of two. A slight modification of the proposed two-stage decimator structure, which can cope with high even decimation factors, is also presented. As a result, several efficient structures are identified in terms of the power consumption and silicon area. Additionally, other two-stage comb-based decimators are presented for high values that are power of three and five. Finally, VHDL (Very High Speed Hardware Description Language)

implementation results, in both a CMOS technology and an FPGA, are shown to validate the proposed approach.

Magnitude response improvement of comb-based decimators

A modified two-stage comb decimation structure, which exhibits a decreased passband droop and increased attenuation in the folding bands is presented. This is mainly achieved by introducing a simple corrector filter at the second stage, depending only on the number of the cascaded equivalent combs. Additionally, it is introduced the design of a very simple compensation filter, which only uses two adders.

Thesis Organization

In Chapter 1 it is presented the basic concept of Nyquist rate and oversampled ADCs, and then it is presented the noise shaping property of ΣΔMs in both the Low-Pass (LP) case and the BP case. Similarly, it is presented the decimation concept and the most popular decimation filter used in LP and BP decimators.

Chapter 2 further explains SDRs based in DCRs and the state of the art in both LC-based BP CT-ΣΔMs and comb-based decimators.

Chapter 3 describes the proposed notch-aware methodology for the synthesis of tunable LC-based BP CT-ΣΔMs, taking into account the dependency of the loop-filter coefficients on the notch frequency and compensating for the dynamic range degradation due to the variation of the notch. Several widely tunable LC-based BP CT-ΣΔMs, with tuning range from $0.1f_s$ to $0.4f_s$, are presented as a case of study, including active, hybrid and passive loop filter realizations.

Chapter 4 introduces a two-stage comb-based decimator with the corresponding design methodology. Several power and area efficient structures are identified and validated trough VHDL implementations. Additionally, modified and corrected structures with improved magnitude responses are also presented, keeping the power efficiency.

Finally, chapter 5 presents the conclusions and future work.

Publications and awards

(a) IEEE Journals:

- G. Molina-Salgado, A. Morgado, G. J. Dolecek, J. M. de la Rosa, "**LC-Based Bandpass Continuous-Time Sigma-Delta Modulators With Widely Tunable Notch Frequency**," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.61, no.5, pp.1442-1455, May 2014.

(b) IEEE Conferences:

- G. Molina-Salgado, G. Jovanovic-Dolecek, J. M. de la Rosa, "**Band-pass continuous-time ΣΔ modulators with widely tunable notch frequency for efficient RF-to-digital conversion**," IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS 2013), pp. 566-569, Aug 2013.

- G. M. Salgado, G. J. Dolecek, J. M. de la Rosa, "**Power and area efficient comb-based decimator for ΣΔ ADCs with high decimation factors**," Proc. of the 2013 Int. Symp. on Circ. and Syst. (ISCAS), pp.1260-1263, May 2013.

- G.M. Salgado, G.J. Dolecek and J.M. de la Rosa, "**Modified comb decimator for high power-of-two decimation factors**," 2014 IEEE 5th Latin American Symposium on Circuits and Systems (LASCAS), pp.1-4, 25-28 Feb. 2014

- G. M. Salgado, A. Morgado, G. J. Dolecek, J. M. de la Rosa, "**Design Consideration of Banpass CT Sigma-Delta Modulators for Software Defined-Radio Receivers**," Proc. of the 2014 Int. Symp. on Circ. and Syst. (ISCAS), pp.718-721, 1-5 Jun 2014.

- G. M. Salgado, G. J. Dolecek, J. M. de la Rosa, "**An Overview of Decimator Structures for Efficient Sigma-Delta Converters**," Proc. of the 2014 Int. Symp. on Circ. and Syst. (ISCAS), vol., no., pp.1592-1595, 1-5 Jun 2014.

- G. M. Salgado, G. J. Dolecek, J. M. de la Rosa, "**Comb Structures for Sigma-Delta ADCs with High Even Decimation Factors**," IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS 2014), Aug 2014.

- G.M. Salgado, G.J. Dolecek and J.M. de la Rosa, "**Novel Two-Stage Comb Decimator with Improved Frequency Characteristic**," 2015 IEEE 6th Latin American Symposium on Circuits and Systems (LASCAS), 24-27 Feb. 2014, "in press".

- G. M. Salgado, G. J. Dolecek, J. M. de la Rosa, "**On the Use of Passive Circuits to Implement LC-based Band-Pass CT ΣΔ Modulators**," IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015), "accepted".

(c) Awards:

- May 2013: Travel grant for the participation at ISCAS 2013, Beijing, China.
- May 2014: Travel grant for the participation at ISCAS 2014, Melbourne, Australia.
- May 2014: Inscription grant for the participation at ISCAS 2014, Melbourne, Australia.
- August 2014: Finalist in the top ten best student paper awards at MWSCAS 2014, Texas, USA.
- September 2014: Travel and inscription grant for the participation at VLSI-SoC 2014, October, 2014, Playa de Carmen, Mexico.

- October 2014: Second best poster in the Ph.D. Forum at VLSI-SoC 2014, Playa del Carmen, Mexico.
- November 2014: Puebla state high performance university students, Puebla, Mexico.
- February 2015: Travel grant for the participation at LASCAS 2015, Montevideo, Uruguay.
- February 2015: Acknowledgement for the presentation of a tutorial at LASCAS 2015, Montevideo, Uruguay.

References

[1] J. Mitola, "The Software Radio Architecture," *IEEE Communications Magazine*, pp. 26–38, May 1995.

[2] S. Gupta *et al.*, "A 0.8-2GHz Fully-Integrated QPLL-Timed Direct-RF Sampling Bandpass ΣΔ ADC in 0.13μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 47, pp. 1141–1153, May 2012.

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Chapter 1

Introduction

This chapter introduces Analog-to-Digital conversion concepts such as sampling and quantizing. The oversampling and noise shaping concepts are also presented along with the so called Sigma-Delta Modulator (ΣΔM). It is explained how ΣΔ Analog to Digital Converters (ADCs) are made-up from a cascade connection of a modulator and a decimator. Low-pass and Band-Pass ΣΔ ADCs are explained in detail, covering both Discrete-Time and Continuous-Time implementations.

1.1 Analog-to-Digital Converters

Analog-to-Digital Converters (ADCs) are essential building blocks in every digital system [1]. ADCs are responsible for the conversion of analog signals, continuous in both time and amplitude, into digital signals, discrete in time and amplitude. Analog-to-Digital (A/D) conversion is performed in order to process signals in digital-based devices like computers. A/D conversion is done in two separate steps: sampling and quantization, which are described in the following.

1.1.1 Sampling

The analog input signal $x_a(t)$, depicted in Fig. 1, is continuous in both time and amplitude. Sampling is the process in which the signal $x_a(t)$ is converted into the discrete time signal $x_a(nT_s)$, where n is an integer and T_s is the sampling period. In the frequency domain, this process introduces replicas of the original spectrum $X_a(f)$ around integer multiples of the sampling frequency f_s[1], as it can be seen in Fig. 1. According to the Nyquist sampling theorem, it is necessary to use a sampling frequency which is at least twice the bandwidth (BW) of $X_a(f)$ in order to avoid the aliasing [1], i.e. the distortion of $X_a(f)$ due to the replica $X'_a(f)$.

$$f_s = 2 \cdot BW \tag{1.1}$$

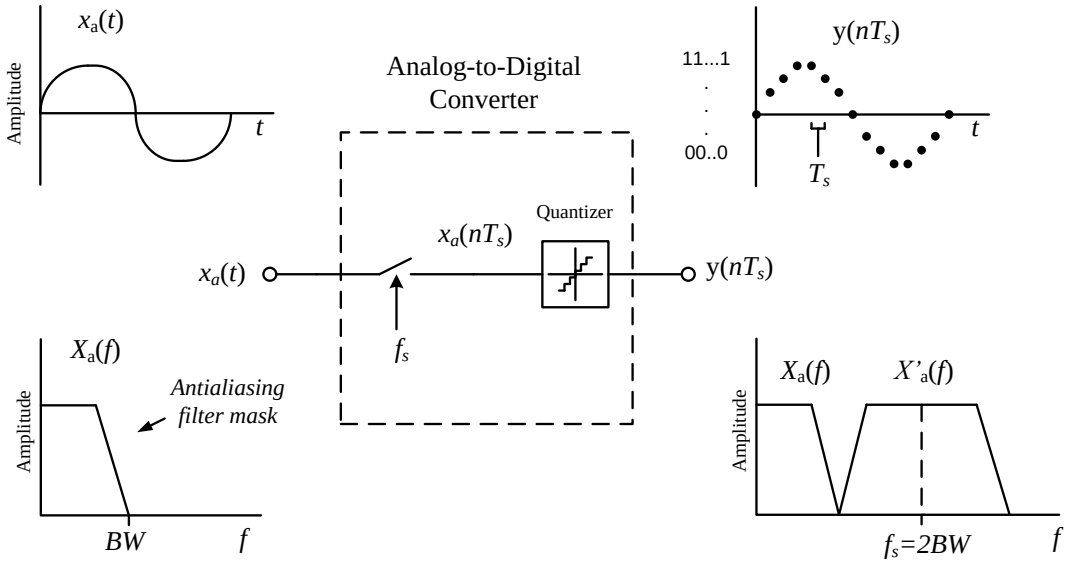


Fig. 1.1 Analog-to-Digital conversion.

In this way, the signal $X_a(f)$ must be band limited, which is done by the antialiasing filter mask, also depicted in Fig. 1. ADCs operated with the sampling frequency established by (1) are usually called Nyquist ADCs.

1.1.1.1 Oversampling

ADCs using sampling frequencies larger than the established by the Nyquist sampling theorem are called oversampled ADCs.

Oversampling is the process of sampling a signal with a sampling frequency higher than that suggested by the Nyquist sampling theorem. Thus, the Oversampling Ratio (OSR) is defined as [2]:

$$OSR = \frac{f_s}{2 \cdot BW}. \tag{1.2}$$

One of the benefits of using oversampling is that it relaxes the anti-aliasing filter specifications as it can be appreciated in Fig. 1.2.

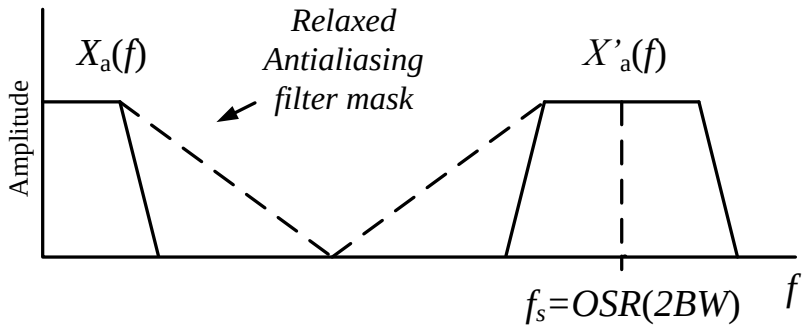


Fig. 1.2 Oversampling and relaxed antialiasing filter mask.

1.1.2 Quantization

Although the signal $x_a(nT_s)$ is discrete in time, it is still continuous in amplitude. Quantization is the process in which the signal $x_a(nT_s)$ is discretized in amplitude and converted into the signal $y(nT_s)$. In this process, the continuous amplitude values of $x_s(nT_s)$ are mapped to a limited set of amplitude values defined by the number of bits, B, in the quantizer. The number of quantization levels is equal to 2^B. The quantization process introduces a random error commonly referred to as quantization error q_e, which is the amplitude difference between $y(nT_s)$ and $x_a(nT_s)$:

$$q_e = y(nT_s) - x_a(nT_s) \tag{1.3}$$

If Bennett's criteria hold, then the quantization error has a rectangular probability density function; thus, the power spectral density (PSD) of the quantization error is constant over the entire range of the sampling frequency [1]:

$$PSD = \frac{\Delta^2}{12 \cdot f_s}, \tag{1.4}$$

where Δ is the minimum quantization step defined by 2^{-B}. Therefore, the quantization process can be modeled as an additive white noise source, as shown in Fig. 1.3, which is usually called quantization noise.

For a system designer, the most interesting feature resulting from modeling the quantization error as an additive white noise is the Signal-to-Noise ratio (SNR), i.e. the ratio between the

signal power and the quantization noise power. Provided that the input signal is a sinusouidal test tone, the maximum SNR for a Nyquist ADC is given by [3]:

$$SNR_{Nyquist\ ADC} = 1.76 + 6.02 \cdot B\ (dB). \tag{1.5}$$

The PSD of oversampled ADCs can be obtained by placing (1.2) into (1.4), i.e.

$$PSD = \frac{\Delta^2}{12 \cdot OSR \cdot 2 \cdot BW}. \tag{1.6}$$

From (1.6) it can be seen that other advantage of using oversampling is that the quantization noise is spread in a wider frequency range. Therefore, the quantization noise power is lowered in the signal band, and the SNR is increased as is illustrated in Fig. 1.4.

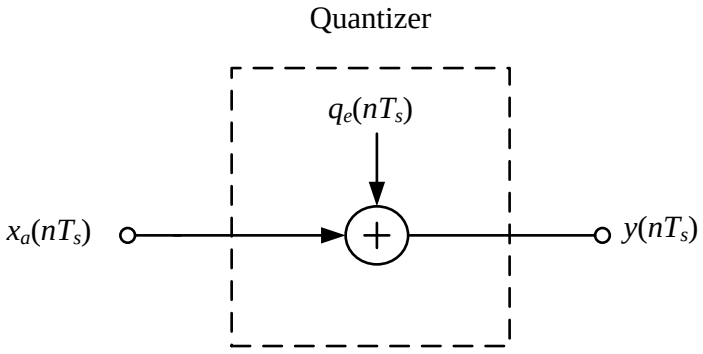
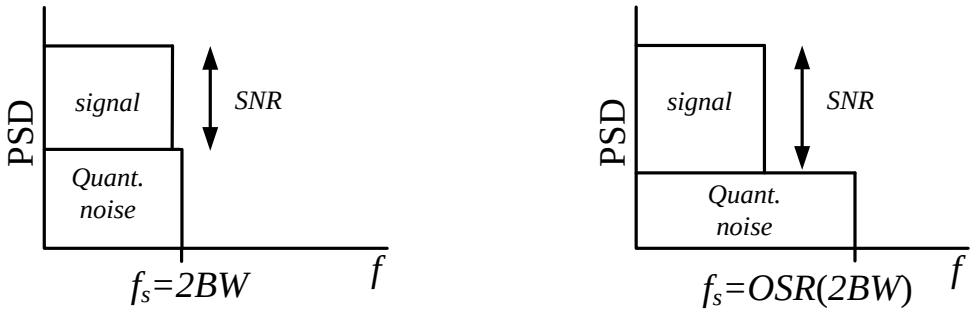


Fig. 1.3 Linear model of a quantizer.



(a) (b)

Fig. 1.4 Quantization noise power in (a) a Nyquist ADC and (b) an oversampled ADC.

The SNR of an oversampled ADC is given by [2]:

$$SNR_{aversampled\ \ ADC} = 1.76 + 6.02 \cdot B + 3 \cdot log_2(OSR). \quad (1.7)$$

According to (1.7), every time the OSR is doubled the SNR is increased in 3dB.

1.2 Low-Pass ΣΔ ADC

Sigma-Delta (ΣΔ) ADCs are made up of an analog modulator and a digital decimator as illustrated in Fig. 1.5. The ΣΔ Modulator (ΣΔM) uses oversampling and noise-shaping to improve the SNR of its embedded ADC. On the other hand, the decimator allows the reduction of the sampling frequency back to the Nyquist rate. This is illustrated in detail as follows.

1.2.1 Low-Pass Discrete-Time ΣΔM

The accuracy of an oversampled ADC can be further increased by filtering the quantization noise in such a way that most of its power lies outside the signal band [4]. In order to perform the quantization noise filtering commonly referred to as noise shaping, an oversampled ADC is embedded in a feedback loop as it is illustrated in Fig. 1.6 (a). The loop filter $H_{\mathrm{DT}}(z)$ is an analog Discrete-Time (DT) filter, which is typically implemented with the Switched-Capacitor technique [2]. Thus, the input signal must be a sampled analog

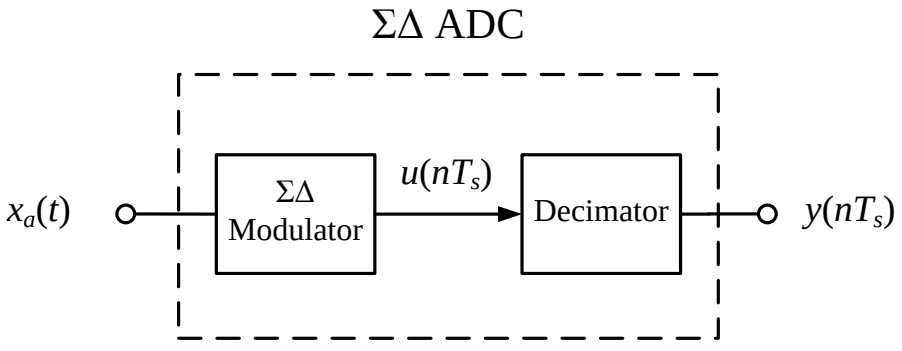


Fig. 1.5 ΣΔ ADC: Modulator and Decimator.

signal, i.e. $x_a(nT_s)$. Similarly, a Digital-to-Analog-Converter (DAC) is needed in the feedback path in order to subtract the digital output $u(nT_s)$ from the analog input $x_a(nT_s)$. Fig. 1.6(b) uses the linear model for the quantizer, where it can be seen that the output in the Z-domain is given by:

$$U(z) = X_a(z) \cdot STF + E_q(z) \cdot NTF. \tag{1.8}$$

In (1.8), STF is the Signal-Transfer-Function affecting $X_a(z)$, and it is determined as:

$$STF(z) = \frac{H_{\mathrm{DT}}(z)}{1 + H_{\mathrm{DT}}(z)}. \tag{1.9}$$

Similarly, NTF is the Noise Transfer Function affecting the quantization noise $E_q(z)$, and it is determined as:

$$NTF(z) = \frac{1}{1 + H_{\mathrm{DT}}(z)}. \tag{1.10}$$

For the case of Low-Pass (LP) oversampled signals, low-frequency in-band components of the quantization noise can be attenuated by applying a differentiating NTF given by:

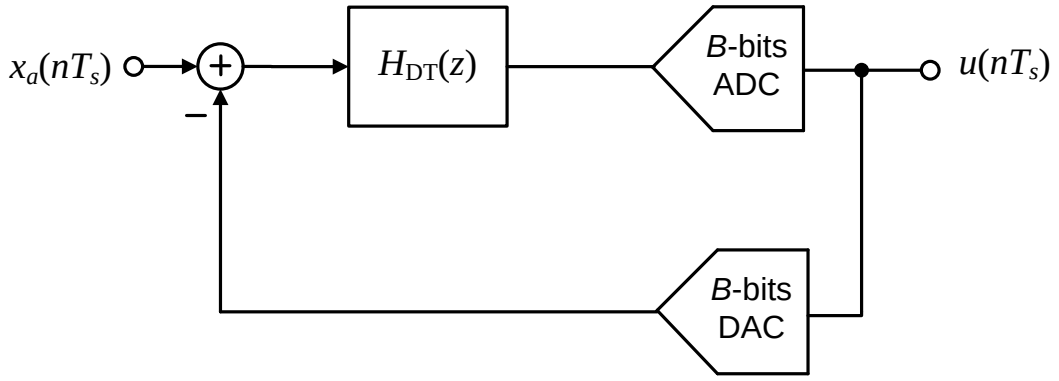
$$NTF(z) = (1 - z^{-1})^L, \tag{1.11}$$

where L is the differentiator order [5]. Thus, by placing (1.11) in (1.10) and solving for the loop-filter it is obtained:

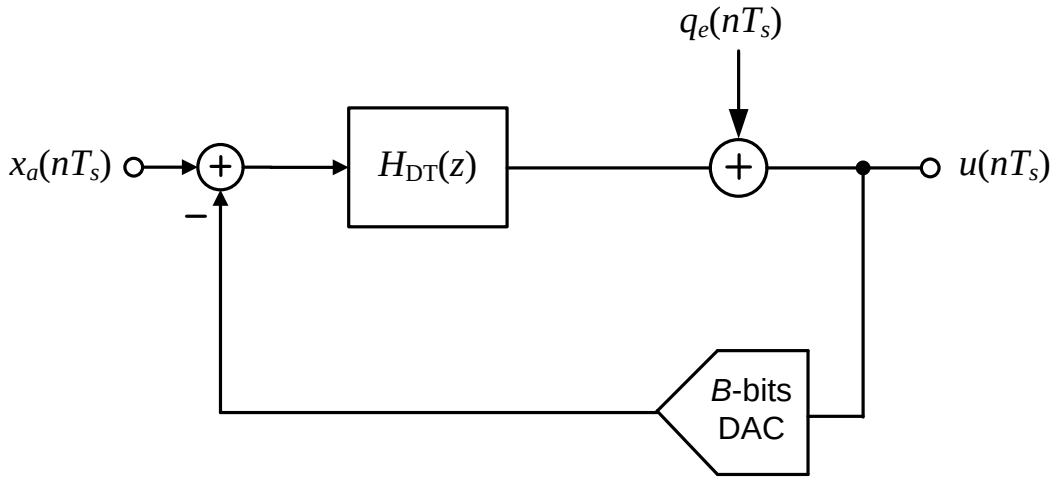
$$H_{\mathrm{DT}}(z) = \left(\frac{z^{-1}}{1 - z^{-1}}\right)^L. \tag{1.12}$$

For this reason, the structure of Fig. 1.6(a) is called the ΣΔ Modulator (ΣΔM), because it can be obtained by placing an integrator (sigma, $H_{\mathrm{DT}}(z)$) in front of a delta modulator [6].

The resulting SNR in the LP DT-ΣΔM of Fig. 1.6(a) is given by [2]:



(a)



(b)

Fig. 1.6 Discrete-Time ΣΔM (a) general block diagram and (b) block diagram with a linear model for the quantizer.

$$SNR_{\Sigma\Delta M} = 1.76 + 6.02 \cdot B + (3 + 6L) \cdot log_2(OSR). \quad (1.13)$$

From (1.13) it can be seen that the SNR of the embedded ADC in the LP DT-ΣΔM is enhanced by (3 + 6·L) dB every time the OSR is doubled, which is higher that only using oversampling. Similarly, from (1.13) it can be noticed that a low resolution ADC (usually a 1 bit quantizer) can be used inside the ΣΔM loop and still have a high SNR thanks to the combined use of oversampling and noise shaping.

The synthesis of LP DT-ΣΔMs can be accomplished following the next two steps.

- For a desired LP NTF, the loop-filter $H_{DT}(z)$ must be determined. This task can be done with the help of the "*delsig*" toolbox [7].
- The obtained $H_{DT}(z)$ must be implemented in a LP DT-ΣΔM topology, which is done through coefficients determination.

Example 1.1: The second order LP DT-ΣΔM presented in Fig. 1.7 (a) uses the CIFB (Cascade-of-Integrators Feed-Back) topology [7]. For a second order loop filter $H_{DT}(z) = (2z\text{-}1) / (z\text{-}1)^2$, it can be demonstrated that the loop-filter coefficients c_1 and c_2 are 2 and -1, respectively. This modulator produces an SNR = 84.6dB when it has f_s = 100MHz, B = 1bit, and $x_a(nT_s)$ is a sinusoidal test tone of 390.625kHz, i.e. an OSR= 128, with -6dB of amplitude with respect to the voltage of full scale (V_{FS}). Figs 1.7(a) and 1.7(b) illustrate time and frequency Matlab® simulations, respectively, for the modulator in Fig. 1.7(a).

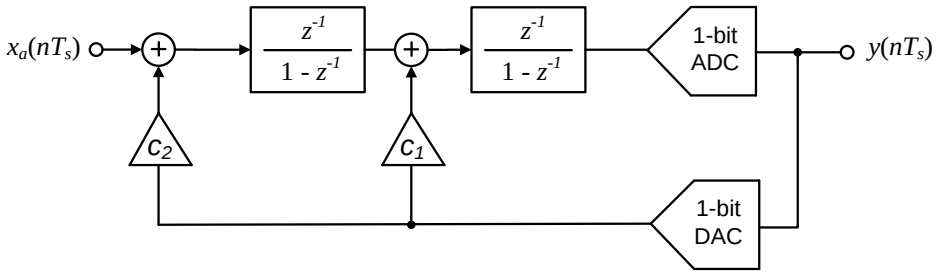
1.2.2 LP Continuous-Time ΣΔM

LP Continuous-Time (CT) ΣΔMs use CT loop-filters $H_{CT}(s)$ as depicted in Fig. 1.8. Note that in this case the analog input signal $x_a(t)$ is continuous in both time and amplitude; therefore, a sampler is explicitly shown before the ADC. LP CT-ΣΔMs have inherent anti-aliasing filter, lower thermal noise, higher sampling rate and lower power consumption than the equivalent DT-ΣΔMs, then they are interesting solutions in high speed applications.

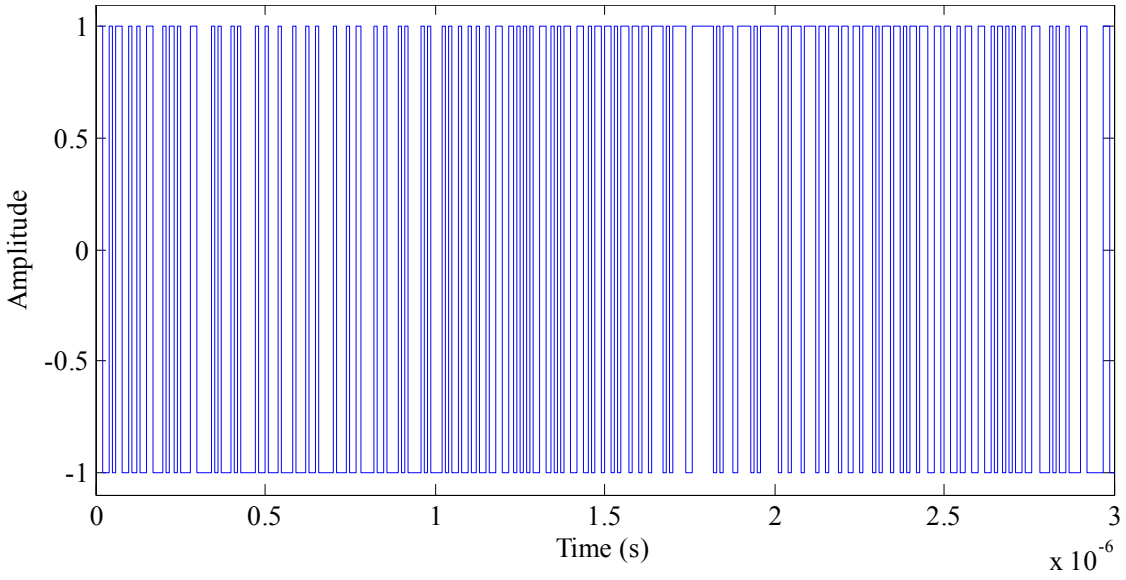
The synthesis of LP CT-ΣΔM can be done in the continuous time domain as presented in [8]. Alternatively, a LP CT-ΣΔM can be synthesized from a given LP DT-ΣΔM by means of a loop-filter transformation [9]-[10]. The transformation method is usually preferred since all the design tools for LP DT-ΣΔM (including the *delsig* toolbox) can be used in the synthesis of LP CT-ΣΔMs.

Figs. 1.9(a) and 1.9(b) present the equivalent open-loop for LP DT-ΣΔMs and LP CT-ΣΔMs, respectively. The two modulators are equivalent if, for the same input waveform, their quantizer input voltages at sampling instants are equal [9], i.e.

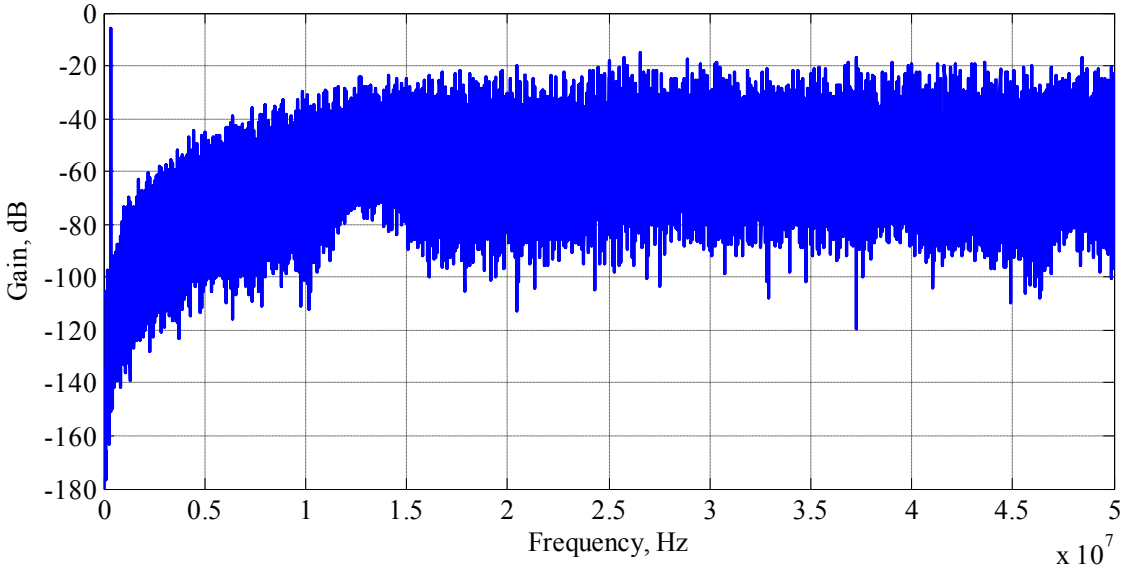
$$Z^{-1}\{H_{DT}(z)\} = L^{-1}\{H_{CT}(s)H_{DAC}(s)\}|_{t=nT_s}, \quad (1.14)$$



(a)



(b)



(c)

Fig. 1.7 Illustration of Example 1.1 (a) LP DT-ΣΔM, output in (b) time and (c) frequency.

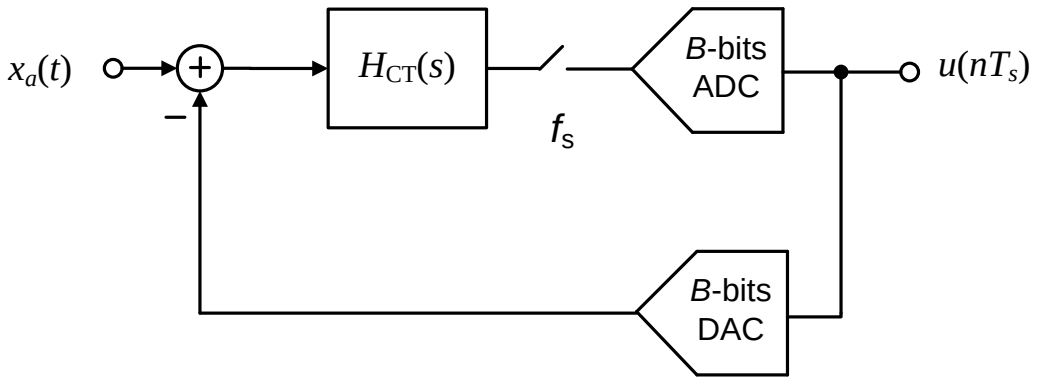


Fig. 1.8 Continuous-Time ΣΔM.

where Z^{-1} and L^{-1} are the inverse Z and Laplace transforms, respectively, and $H_{DAC}(s)$ is the feedback DAC transfer function.

As it can be seen from (1.14), the impulse response of the CT open-loop depends on the shape of the feedback DAC. Thus, different DAC waveforms would produce different impulse responses. The most common DAC waveforms such as Non-Return-to-Zero (NRZ), Return-to-Zero (RZ) and Half-delayed-Return-to-Zero (HRZ) can be modeled as:

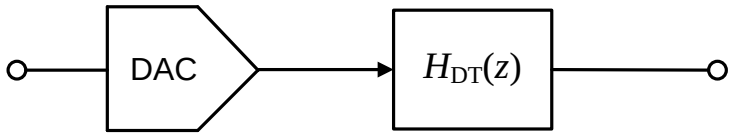
$$h_{DAC}(t) = \begin{cases} 1, & a \le t \le b, \quad 0 \le a < b \le T_s \\ 0, & Otherwise \end{cases}, \tag{1.15}$$

which is depicted in Fig. 1.8(c). The Laplace transform of (1.15) is described as:

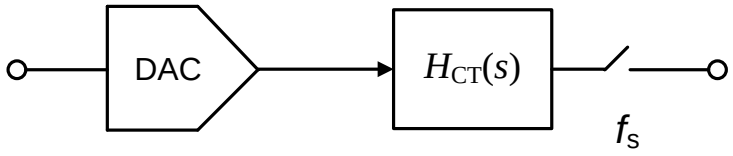
$$H_{DAC}(s) = \frac{e^{-as} - e^{-bs}}{s}. \tag{1.16}$$

The synthesis of LP CT-ΣΔMs from LP DT-ΣΔMs can be accomplished as follows:

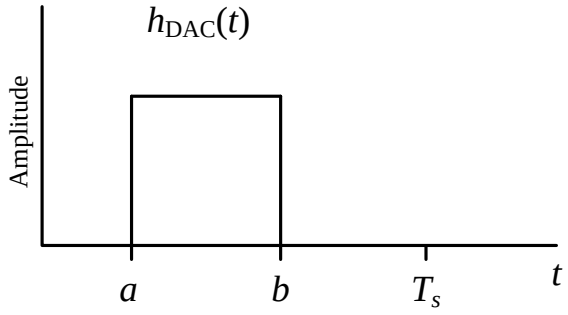
- By using (1.14), the filter $H_{DT}(z)$ of a given LP DT-ΣΔM is transformed into its CT equivalent, i.e. $H_{DT}(s)$. Alternatively, the MALAB® function "*d2c*" can be used to this end.
- The obtained $H_{DT}(s)$ must be implemented in a LP CT-ΣΔM topology, which is done through coefficients determination.



(a)



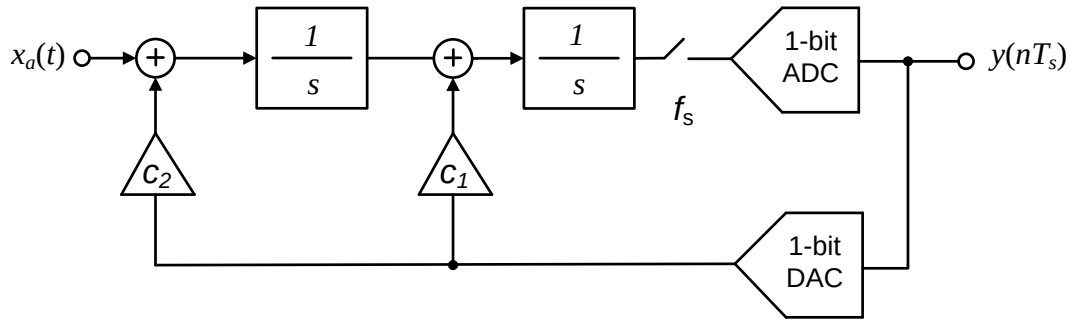
(b)



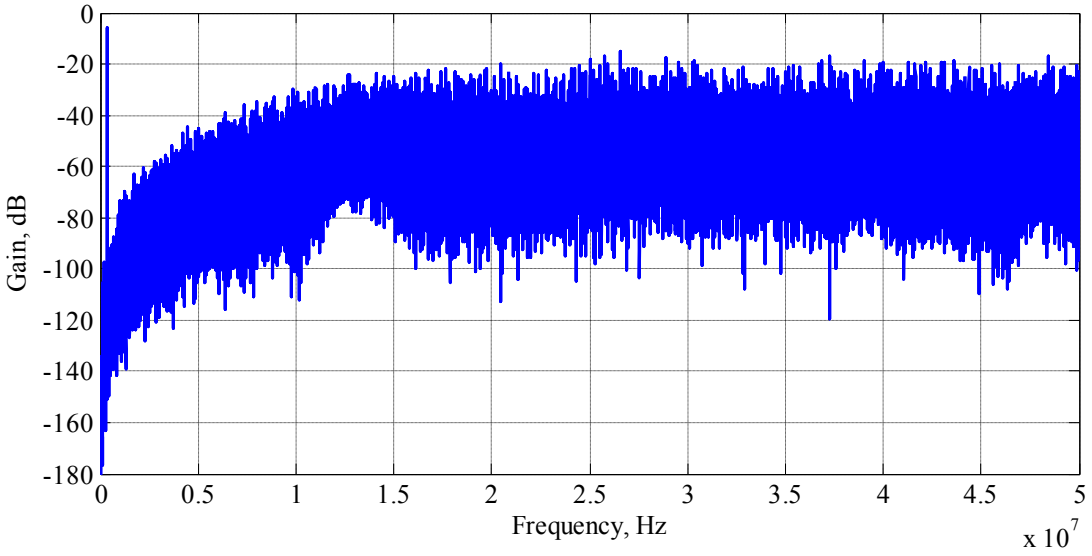
(c)

Fig. 1.9 (a) LP DT-ΣΔM open-loop equivalent, (b) LP CT-ΣΔM open-loop equivalent, and (c) general square DAC waveform.

Example. 1.2: The LP CT-ΣΔM presented in Fig. 1.10 (a) has been synthesized from the LP DT-ΣΔM of Fig. 1.7 (a) by applying the DT-to-CT loop-filter transformation. The resulting $H_{DT}(s) = (-1.5s + 1) / s^2$ loop-filter has been implemented in the CT CIFB topology with $c_1 = -1.5$ and $c_2 = 1$. For a similar OSR, input signal and sampling frequency, the noise performance of the LP CT-ΣΔM (SNR=84.4dB) is similar to that of the LP DT-ΣΔM due to the loop-filter transformation. Fig. 1.10(b) illustrates the output spectrum of the considered LP CT-ΣΔM.



(a)



(b)

Fig. 1.10 Illustration of Example 1.2 (a) Synthesized LP CT-ΣΔM and (b) its output spectrum.

1.2.2 Low-pass Decimator

Deecimators or decimation filters are composed by the cascade connection of a digital low pass filter, $G(z)$, and a down-sampler as is illustrated in Fig. 1.11. The downsampler reduces the input sampling rate by an integer factor M, which is called the decimation factor. The sampling rate reduction is done by disregarding every sample of $u(n)$ that is not an integer multiple of M [11]. Similar to what occurs in the sampling of analog signals, in the frequency domain downsampling introduces replicas of the original spectrum $U(f)$ centered around integer multiples of $2\pi/M$, which is illustrated in Fig. 1.11 (b). Therefore,

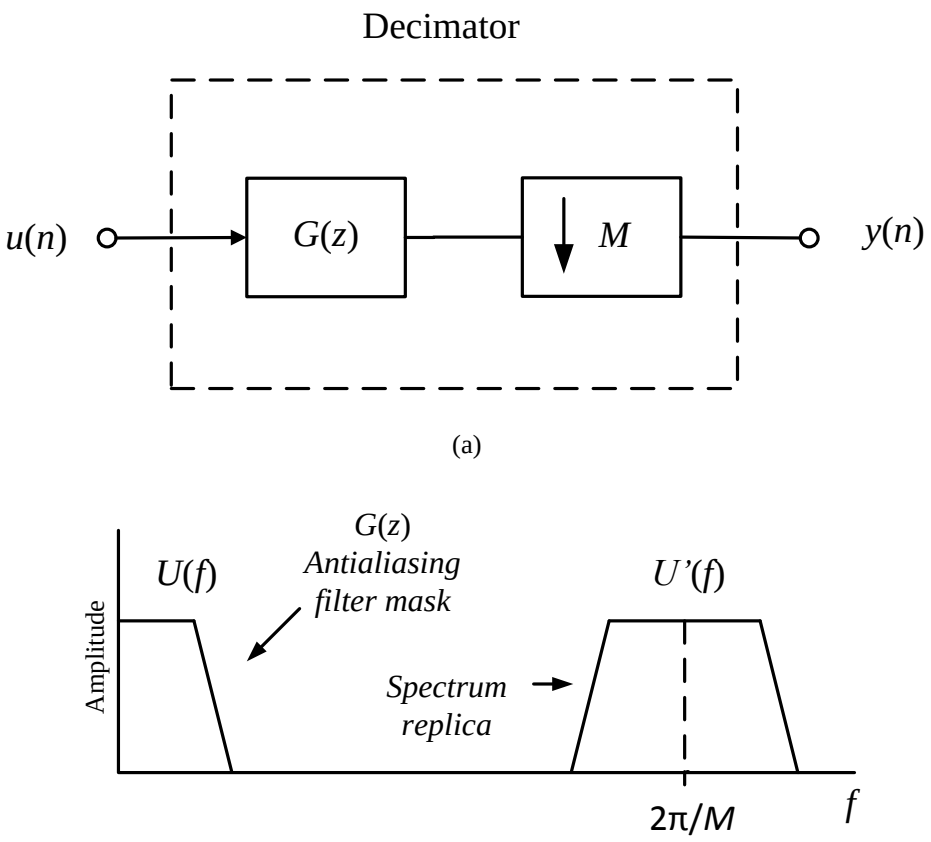


Fig. 1.11 (a) Decimator or decimation filter, and (b) downsampling in the frequency domain.

the digital filter $G(z)$ is required to bandlimit the incoming signal $u(n)$ and avoid aliasing during the downsampling process. The specifications for the LP decimation filter are given by [12]:

$$\left|G(e^{j\omega})\right| = \begin{cases} 1, & \omega \leq \omega_c \\ 0, & \pi/M \leq \omega \leq \pi \end{cases} \tag{1.17}$$

In ΣΔMs the main function of a decimator is to reduce the sampling frequency to the Nyquist rate. To this end, the decimator must have $M=OSR$.

The decimation is more efficiently performed in several stages, i.e. $M=M_1M_2...M_n$ [13]. Comb decimation filters are widely use in the first decimation stage, because they are very

simple to implement thanks to their unitary filter coefficients; therefore, neither multipliers nor memory storage are required for implementations [14].

Comb decimation filters can be implemented in either recursive form

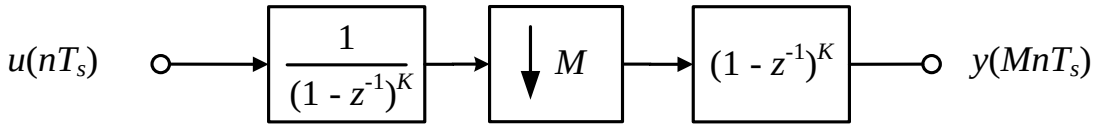
$$H(z) = \left[\frac{1 - z^{-M}}{1 - z^{-1}}\right]^K, \tag{1.18}$$

or non-recursive form

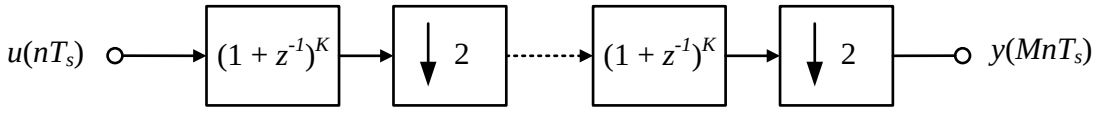
$$H(z) = \left[\frac{1}{M}\sum_{k=0}^{M-1} z^{-k}\right]^K, \tag{1.19}$$

where K is the number of cascaded filters. In [15] it was derived that comb filters must have $K = L + 1$ in order to avoid aliasing in ΣΔMs sampling rate reduction.

Fig. 1.12(a) illustrates the block diagram implementation of the recursive comb filter, which is usually called CIC (Cascade-Integrator-Comb). On the other hand, Fig. 1.12 (b) is the block diagram for the non-recursive comb in the special case when the decimation factor is a power of two, i.e. $M = 2^P$.



(a)



Stage 1 Stage P

(b)

Fig. 1.12 Block diagram representation for (a) recursive comb (CIC) and (b) non-recursive comb for $M = 2^P$.

The magnitude response of comb filters can be obtained by placing $z = e^{j\omega}$ in either (1.18) or (1.19), giving [13]:

$$\left|H\left(e^{j\omega}\right)\right| = \left[\frac{1}{M}\frac{\sin\left(\frac{\omega M}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}\right]^{K}. \tag{1.20}$$

Both implementations have the same magnitude response, which is characterized by a *sinc*-shaped form as is illustrated in Fig. 1.13 for M=8 and K=4. The comb zeros are exactly located at the angular frequencies of $2\pi/M$; therefore, it behaves well as an antialiasing filter [16].

The passband of the comb filter is defined by the edge frequency as:

$$\omega_p = \frac{2\pi}{MR}, \tag{1.21}$$

where R is the residual decimation factor implemented by the stage that follows the comb decimation stage, and the minimum value for R is equal to 2.

The regions around the zeros of the comb filter are called the folding bands and are determined by M and ω_p as follows:

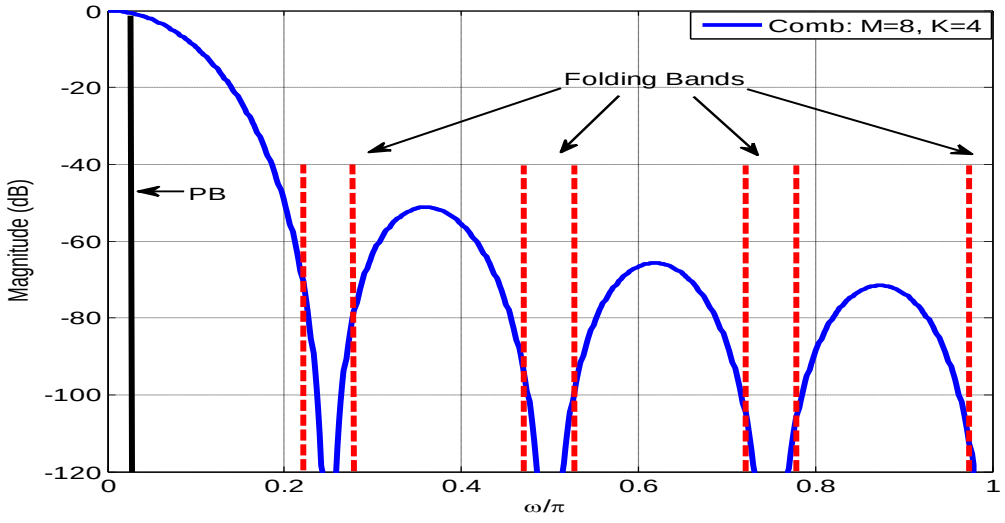


Fig. 1.13 Magnitude response of a comb filter with M=8 and K=4.

$$\left[\frac{2\pi i}{M} - \omega_p;\ \frac{2\pi i}{M} + \omega_p\right] \ for\ i \begin{cases} 1, \dots M/2 & for\ M\ even \\ 1, \dots, (M-1)/2 & for\ M\ odd \end{cases} \tag{1.22}$$

Due to the decaying magnitude response of the comb filter, the first folding band provides the lowest alias rejection at the frequency:

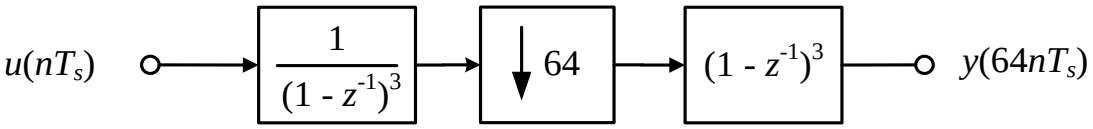
$$\omega_A = \frac{2\pi}{M} - \omega_p, \tag{1.23}$$

which is usually called the WCA (Worst Case Attenuation).

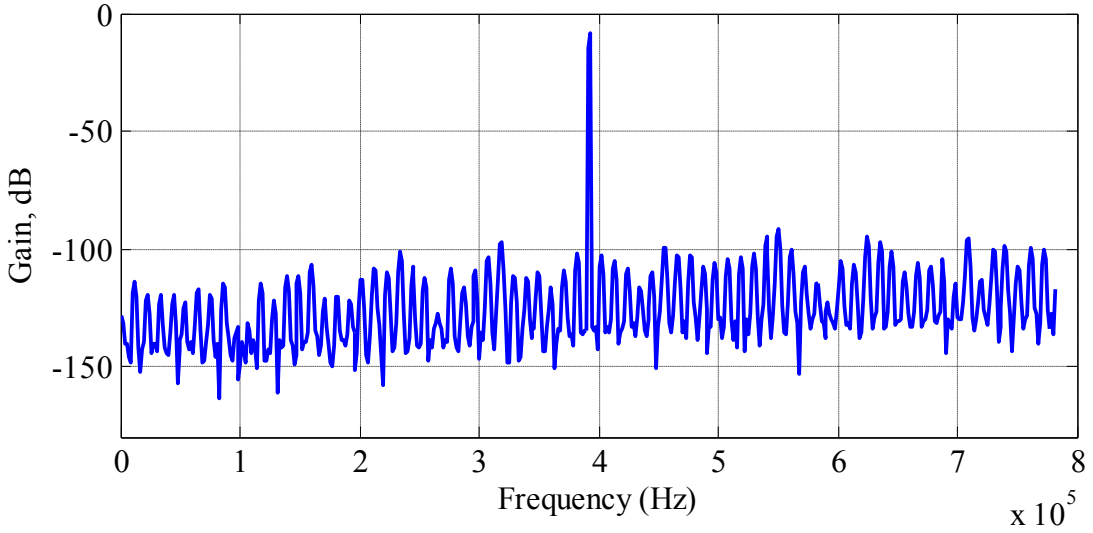
Example 1.3: Fig. 1.14 illustrates the block diagram implementation of a CIC intended for either the LP DT-ΣΔM or the LP CT-ΣΔM of Figs. 1.7(a) and 1.9(a), respectively. Note that M=64 because the minimum R is equal to 2, and thus OSR = 2M =128. Since the modulators in Example 1.1 and 1.2 have a second order loop-fiter, then the number of cascaded comb filters is K = 3. Fig. 1.14 (b) illustrates the decimator output in frequency, where it can be seen that it contains a sinusoidal tone of 390.625kHz sampled at 1.526MHz (twice the Nyquist rate), while the SNR is preserved about to 84dB. On the other hand, Fig. 1.14(c) shows the output of the decimator in time, but in this case the input sinusoidal tone to the modulator was set equal to 48.8281 kHz for clarity proposes. From Fig. 1.14 it can be appreciated that the output of the decimator is a digital representation of the analog input signal; thus, the decimator completes the A/D conversion of the whole ΣΔ ADC.

1.3 Band-Pass ΣΔ ADC

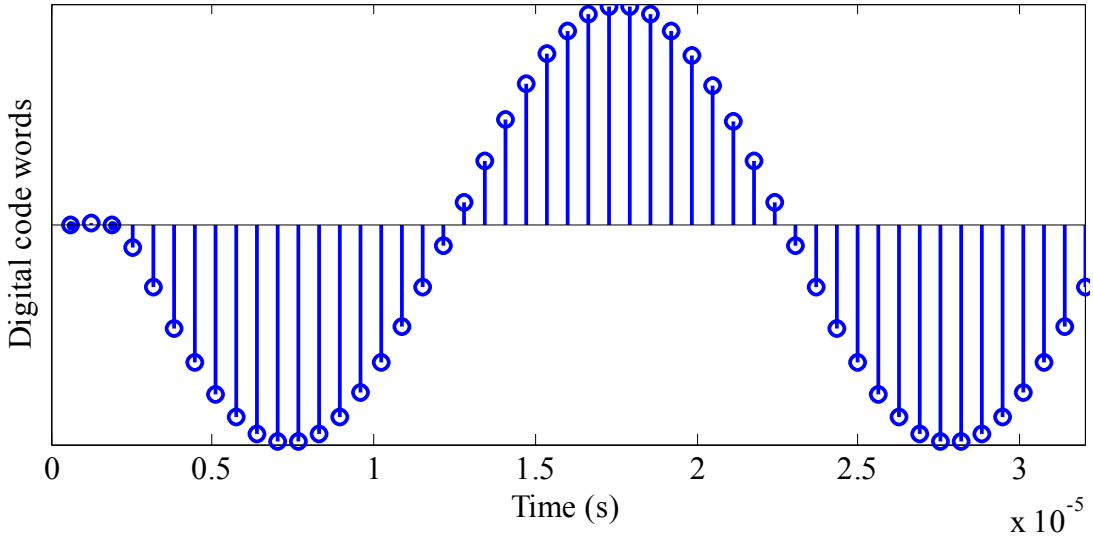
Similar to LP ΣΔ ADCs, Band-Pass (BP) ΣΔ ADCs are made-up of a modulator and a decimator. BP-ΣΔMs has their NTF zeros placed in a narrow-band around a high carrier frequency, usually called the center or notch frequency f_n. Thus, the digitization of intermediate-frequency (IF) or radio-frequency (RF) signals with a high resolution becomes possible [2]. The BP-decimator allows the reduction of the sampling frequency back to the Nyquist rate, and at the same time it performs BP to Base-Band (BB) down-conversion. This is illustrated in detail in the following section.



(a)



(b)



(c)

Fig. 1.14 (a) CIC decimator with M=64 and K = 3 for the second order LP CT-ΣΔM of Fig. 1.6(a), (b) output spectrum and (c) time output for a sinusoidal test tone of 48.8281 kHz.

1.3.1 BP DT-ΣΔM

The notch frequency in BP DT-ΣΔMs is usually set in a quarter of the sampling frequency, i.e. $f_n = f_s/4$, thus making the synthesis and decimation process easier [9].

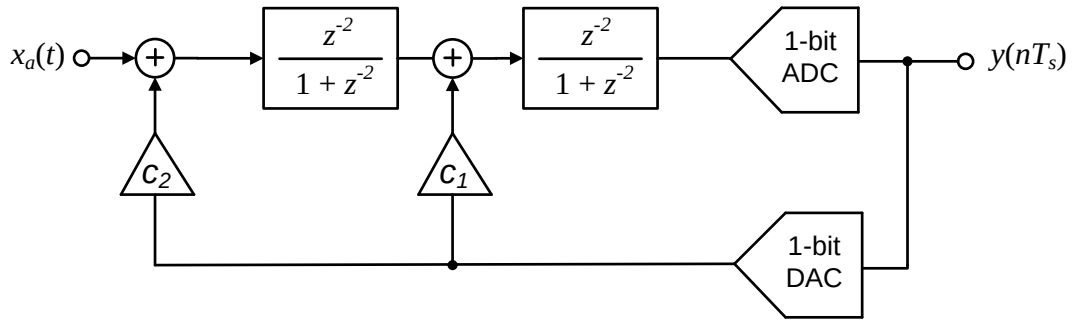
For the $f_n = f_s/4$ case, BP DT-ΣΔMs can be easily synthesized from LP DT-ΣΔMs by applying a LP-to-BP loop-filter transformation. To this end, the integrators in LP DT-ΣΔMs are replaced by resonators in order to obtain BP DT-ΣΔMs. The transfer function of DT resonators is

$$H(z) = \frac{z^{-2}}{1 - z^{-2}}. \tag{1.15}$$

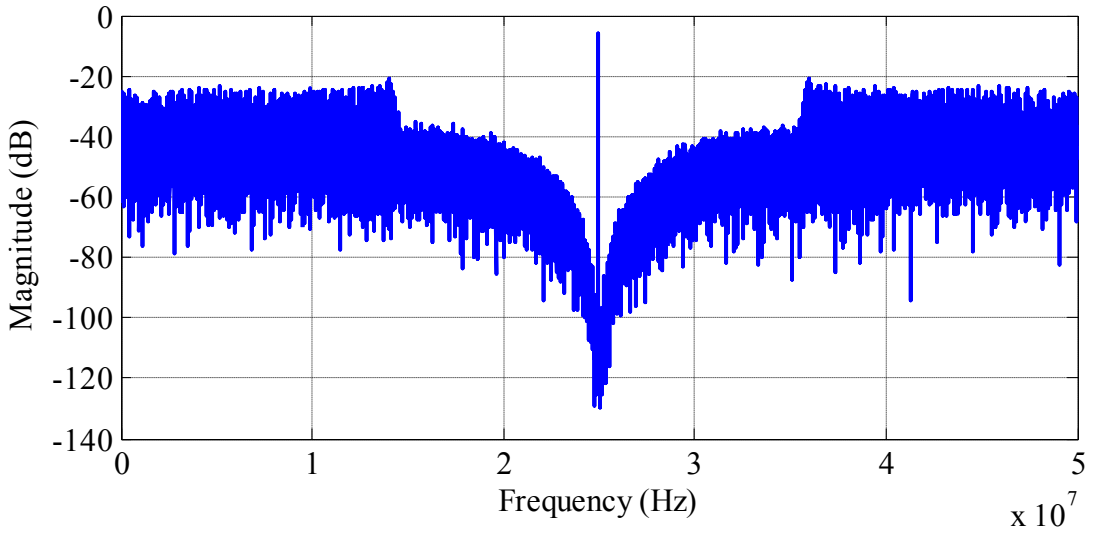
Example 1.4: The fourth order BP DT-ΣΔM shown in Fig. 1.14(a) was synthesized from the LP DT-ΣΔM presented in Example 1.1 (Fig. 1.7(a)) by replacing the integrators with resonators in the loop-filter, the loop filter coefficients c_1 and c_2 remain the same. The output spectrum of the BP DT-ΣΔM is illustrated in Fig. 1.14(b), where it can be seen that f_n is placed at a quarter of f_s. Note that the loop-filter order in the BP case is twice of that in the LP case, this is because NTF zeros are present in conjugate pairs.

It is possible to synthesize BP DT-ΣΔMs with an arbitrary f_n in the range from DC to $f_s/2$. In this case the synthesis process is as follows:

- The BP loop-filter $H_{BP}(z)$ must be determined for a given f_n. The *delsig* toolbox can be used to this end.
- The obtained $H_{BP}(z)$ must be implemented in a BP DT-ΣΔM topology through loop-filter coefficient determination.



(a)



(b)

Fig. 1.15 (a) 4th order BP DT-ΣΔM with $f_n = f_s / 4$ synthesized from a 2nd order LP DT-ΣΔM and (b) its output spectrum.

1.3.2 BP CT-ΣΔM

In section 1.3.1 it could be seen that BP DT-ΣΔMs can be easily synthesized from LP DT-ΣΔMs by replacing the integrators with resonators, at least for the $f_n=f_s/4$ case. However, the substitution of integrators by resonators in LP CT-ΣΔMs topologies does not implement BP CT-ΣΔMs [9].

BP CT-ΣΔMs can be synthesized from BP DT-ΣΔMs by means of a DT-to-CT loop-filter transformation, i.e. transforming $H_{\text{BP-DT}}(z)$ into an equivalent $H_{\text{BP-DT}}(s)$. However, the obtained $H_{\text{BP-DT}}(s)$ presents some implementation issues due to a LP term included in its numerator [9], i.e. $(As+B)/(s^2+\omega^2)$. Since it is usually easier to implement purely LC

resonators, the synthesis of a BP CT-ΣΔM is usually done with a CT-to-DT equivalency. This is further explained in Chapter 2, where the state of the art in the synthesis of LC-Based BP CT-ΣΔMs is described.

1.3.1 BP Decimation

There are two philosophies for the decimation of band pass signals. The first of them is the use of a single BP filter combined with safely under-sampling [17], in which the BP signal is translated to Base-Band by means of under-sampling. The second method is the use of a Digital Down Converter (DDC), which is usually preferred due to its utility in quadrature demodulation. A DDC includes two multipliers, a numerical controlled oscillator (NCO), and two identical LP decimators [17]. The role of the NCO is to generate cosine and sine sequences to remove the carrier frequency and obtain the *I* (In-phase) and *Q* (Quadrature) components. The LP decimators perform frequency reduction to the Nyquist rate in a similar fashion to that in the LP ΣΔM, i.e. preventing quantization noise folding. Therefore, all the design techniques for LP decimators can be applied in DDCs. Note that for BP ΣΔMs with $f_n=f_s/4$ the cosine and sine sequences generated by the NCO consist of only +1, 0 and -1 terms, which greatly simplifies the multiplication process, which is usually done with only X-OR gates [2].

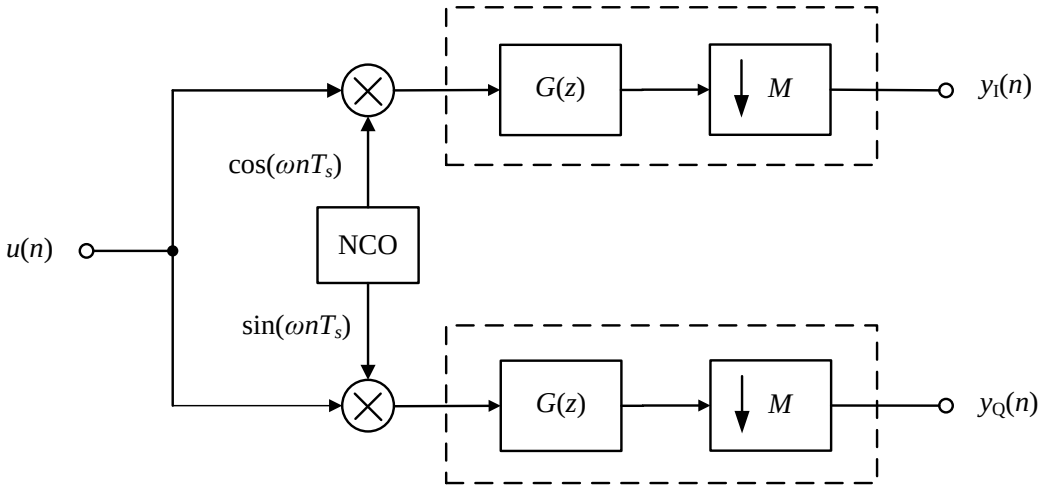


Fig. 1.16 Block diagram of a DDC.

1.4 Conclusions

This chapter has introduced the basic concept of analog to digital conversion. It has been illustrated that using oversampling the quantization noise power can be reduced within the signal band, increasing the SNR. The SNR can be further improved by embedding the oversampled quantizer in a ΣΔ loop. In this way, the quantization noise is shaped and most of its power lies outside the signal band.

High resolution ADCs can be obtained by cascading ΣΔMs with decimators. Decimators reduce the high sampling frequency of ΣΔMs to the Nyquist rate while preserving the SNR.

It has also presented that BP ΣΔMs extend the noise shaping concept to BP signals, allowing the digitization of IF or RF signals with a high resolution. In this scheme, DDCs are required to reduce the sampling rate of BP ΣΔMs. The heart of DDCs is the two identical LP decimators used to reduce the sampling rate of the I/Q components of BP signals. In this way, all the design techniques for LP decimators can be applied in DDCs.

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Chapter 2

BP CT-ΣΔM for Software Defined Radio

This chapter presents Software Defined Radio receivers based on the reconfigurable Direct Conversion Receiver (DCR). The BP ADC needed in the DCR can be efficiently implemented by BP CT-ΣΔ ADCs. It is presented how the lack of degrees of freedom in the LC-based BP CT-ΣΔMs has been overcome by using techniques such as multi-feedback-DAC, integrating-DAC, and FIR-DAC. Power and area efficient methods for comb-based decimators are also presented, along with those intended for their magnitude response improvement.

2.1 Software-Defined-Radio Receivers

SOFTWARE-DEFINED-RADIO (SDR) based mobile devices are expected to perform most of the signal processing in the digital domain, thus allowing to increase their programmability and adaptability to a large number of communication standards and operation modes. One of the most critical building blocks, which eventually will enable such a technology, is the ADC. This circuit should be ideally placed at the antenna so that Radio Frequency (RF) signals could be directly digitized, thus being processed in a flexible way by running software on a Digital Signal Processor (DSP) [1]. Unfortunately, the efficient implementation of SDR handheld terminals is still far from a consumer product deployment mostly limited by the unfeasible power-hungry specifications required for the ADC.

A more realistic implementation of SDR receivers should include an Analog-Signal-Processing (ASP) section, as depicted in Fig. 1, in order to implement the necessary signal conditioning, i.e. frequency translation, amplification and filtering before being digitized and processed by the DSP. The way in which the ASP section is implemented involves a number of design trade-offs among the different receiver building blocks. Actually, the majority of SDRs are based on a reconfigurable Direct Conversion Receiver (DCR) scheme like that shown in Fig. 1(a), where after being filtered and preamplified, RF signals are

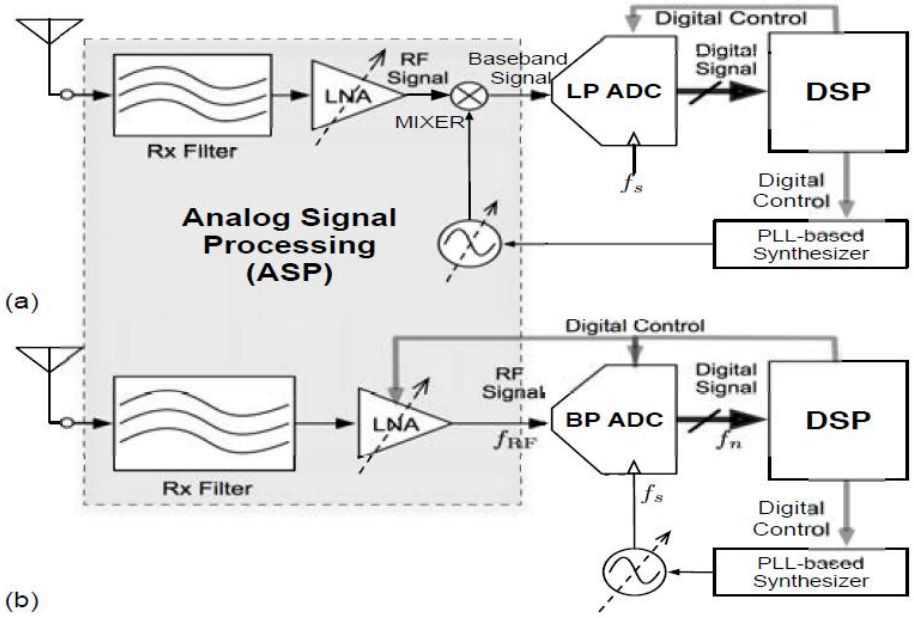


Fig. 2.1 Conceptual SDR receiver based on a: (a) LP ADC. (b) BP ADC.

down-converted to baseband, where they are digitized by a LP ADC. One of the main limitations of DCR-based SDRs is their larger sensitivity to circuit errors of the analog down-conversion process, which aggravates due to the tunable operation required to process different standards and operation modes.

The aforementioned limitations can be partially solved by using the SDR receiver scheme shown in Fig. 1(b), where the RF signals coming in from the antenna are filtered, preamplified and directly digitized by BP ADCs. The main advantage of this approach is that most part of the signal conditioning is translated from the analog to the digital domain, thus increasing their programmability and robustness against circuit and technology parasitics. The main challenge in this scheme is the design of the BP ADC, since it must be able to convert the majority of wireless communications standards. Table 2.1 summarizes the most popular wireless communication standards used today. To this end, different strategies have been reported to efficiently implement BP ADCs, most of them are frequently base on BP CT-ΣΔ ADCs. Thus, in the following it will be presented the state of the art in both BP CT-ΣΔMs and comb-based decimators.

Standard	Carrier Frequency (GHz)	BW (MHz)	Requiered SNR
GSM	0.90 / 1.8	25	90dB
UMTS	0.90 / 2.4	45	65dB
LTE	1.880 (Class 3)	75	70dB
Wimax 802.16 d	3.5 and 5.8	20	50dB
IEEE 802.11 b,n	2.4	20	50dB
Bluetooth	2.4 - 2-48	80	66dB

Table 2.1. Some wireless communication standards used today.

2.2 State of the art in BP CT-ΣΔMs

One major limitation of most of BP CT-ΣΔMs intended for RF-to-digital conversion, comes from the use of a fixed notch frequency, f_n, usually chosen at $f_n = f_s/4$. Apart from the prohibitive values of fs which result in some applications, for instance in those standards operating at f_{RF} = 5GHz, using fixed values of f_n forces the variation of f_s in order to tune the desired RF signal. Moreover, another important inconvenience of this approach is that the RF receiver would require a widely programmable PLL-based synthesizer (see Fig. 2.1 (b)) in order to place the in-coming RF signal within the passband of the modulator. This issue has motivated the interest for reconfigurable BP CT-ΣΔMs with tunable notch frequency in these applications [2], [3].

Most approaches for the implementation of tunable BP ΣΔMs have been described at a very high abstraction level [4]–[6]. In the majority of cases, the proposed modulator topologies are based on biquad loop filters implemented with either Switched-Capacitor (SC) [7], [8] or Gm-C circuit techniques [9]. Recently, the use of quadrature architectures has been considered to increase the degree of programmability [10]. However, all these approaches yield to an increase of the complexity of the modulator architecture in terms of the number of loop-filter coefficients and/or feedforward/feedback paths, thus making their application in the GHz range impractical.

Since LC filters have higher operating speed and dynamic range than their Gm-C and RC counterparts [11], they are good solutions for the loop-filter implementation in BP CT-ΣΔMs intended for SDRs. Indeed, the use of tunable LC-based loop filters becomes mandatory to digitize RF signals. However, using LC filters in BP CT-ΣΔMs makes the

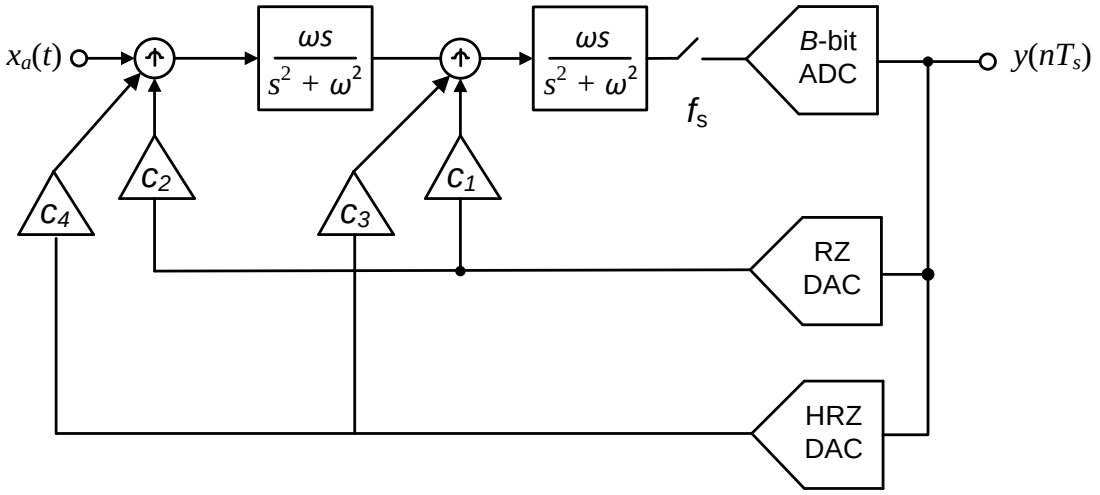
CT-to-DT equivalency impossible due to the loss of parity between the order of the loop-filter and the number of internal nodes. Fortunately, in the open literature has been presented several methods to overcome this issue.

The LC-based BP CT-ΣΔM introduced in [12], often called the multi-feedback topology, uses two types of feedback waveforms RZ-DAC and HRZ-DAC, which provides enough degrees of freedom for the CT-to-DT equivalency (Fig. 2.2(a)). A realization of this modulator has been presented in [13] featuring a sampling frequency of 4GHz for the digitization of a 1GHz RF signal.

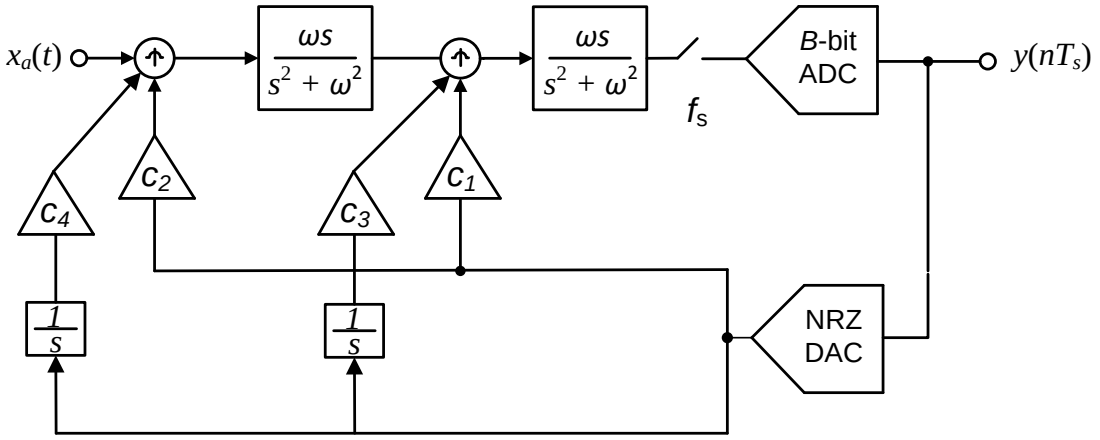
In [14] the HRZ-DAC of the multi-feedback topology has been replaced by an integrating-DAC in order to achieve better jitter performance (Fig. 2.2(b)). The realization of this LC-based BP CT-ΣΔM has achieved the conversion of an RF signal of 950MHz at a sampling frequency of 3.8GHz.

The FIR technique presented in [15]-[16] can be also used to increase the degrees of freedom in the synthesis of LC-based BP CT-ΣΔM as suggested in [17], [18]. Fig. 2.2(c) illustrates the topology of an FIR-DAC LC-based BP CT-ΣΔM, in the feedback path the coefficients are separated by half-cycle delays, $z^{-1/2}$. Due to the half-delay between the sampling instants, the modified *Z*-transform, used in [19] for the synthesis of CT ΣΔMs, is the preferred method to perform the CT-to-DT transformation [17], [18]. In [20] it has been presented a realization of an FIR-DAC LC-based BP CT-ΣΔM in which the feedback DAC is of the raised cosine form. This modulator uses under-sampling to convert an RF signal of 2.442GHz with a sampling frequency of 3.256GHz, where the alias of the RF signal is exactly placed at 0.814GHz, i.e. $f_n = f_s / 4$.

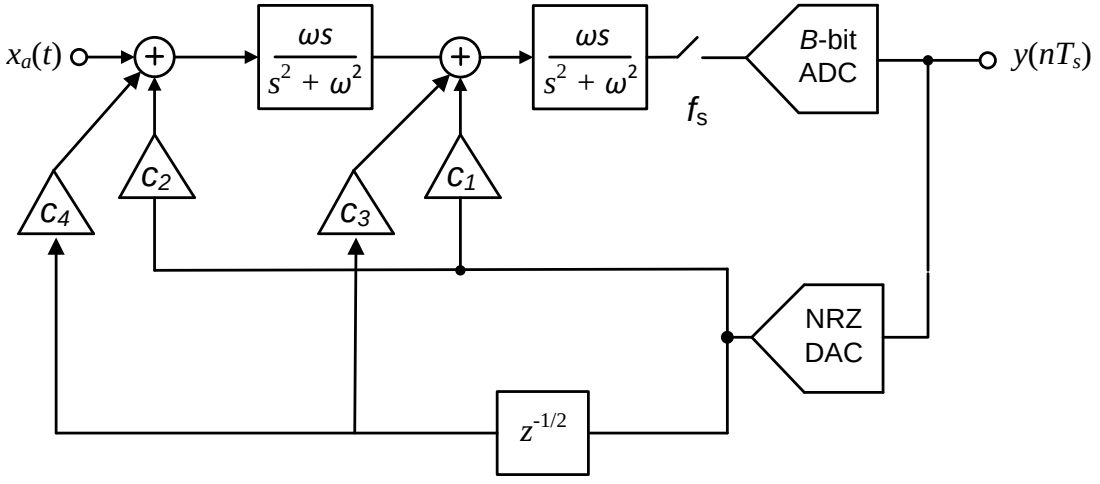
In addition to the previously mentioned modulators there are other several realizations presented in the literature [21]-[23]. However, most of them use a fixed notch frequency at $f_s/4$. To the best of the author knowledge, the widest tuning range achieved by LC-based BP CT-ΣΔMs was reported by Gupta *et al* [24], featuring a 0.8-2GHz notch-frequency range thanks to the combination of reconfiguration and under-sampling techniques. Therefore, it is still necessary to develop a design methodology for the synthesis of widely tunable LC-based BP CT-ΣΔMs.



(a)



(b)



(c)

Fig. 2.2 State of the art in LC-based BP CT-ΣΔMs: (a) multi-feedback [12], (b) integrator DAC [14] and (c) FIR-DAC [17].

2.3 State of the art in comb-based decimators

As described in Chapter 1, the most popular approach to implement decimators is based on comb filters, mainly motivated by its simplicity. However, comb filters themselves cannot satisfy high performance demands of state-of-the-art ΣΔMs: consequently, it is very important to design comb-based decimators of low complexity but with high capabilities to preserve the decimated signal, i.e. with adequate magnitude response characteristics. Similarly, it is very important to design power and area efficient comb-based decimators for ΣΔ ADCs intended for SDRs, since in this scenario the decimator must reduce the sampling rate from the GHz range to tens or hundreds of MHz, which may lead to an increased in the power consumption of the whole ΣΔ ADC. In the following, it will be presented some methods proposed in the open literature to improve the power and area efficiency of comb decimators as well as their magnitude response characteristics.

2.3.1 Power and area efficiency of comb-based decimators

Non-recursive-comb structures have been demonstrated to be more power efficient than CIC structures [25]-[26]. In [25] a two-stage non-recursive comb structure is introduced: the first stage of the structure is implemented in the polyphase form in order to reduce as early as possible the sampling frequency of the input filter; the second stage is implemented in a non-recursive form. On the base of an extensive power and area estimations, as well as experimental results in a 0.35μm CMOS technology, the author has presented a decimation filter with M_1=16 and M_2=2, which is 30% and 20% more power and area efficient, respectively, compared with the traditional non-recursive-comb structure. Similarly, in [26] a method to implement integer multiple decimation factors as a cascade of non-recursive-comb stages is presented. This method proposes the factorization of $M=N_1N_2\ldots N_n$, where N_n are prime numbers and $N_n>N_2>N_1$. The implementation of each stage is in polyphase form in order to reduce as much as possible the sampling frequency of the input stage. On the base of power and area estimations, this structure has demonstrated improved power and maximum operating speed compared with that of the equivalent CIC structure. Nevertheless, the structure of [26] has an increase in the used silicon area.

There are some published results that have considered power and silicon area optimization of comb-based decimation filters at the implementation level. These results are based on different circuit and filter implementation techniques. In [27] a 4^{th} order comb filter with M=4 is implemented only with hard-wire shifts and five adders. The implemented decimator shows improved power and area efficiency compared with the equivalent CIC structure (50% and 30%, respectively). The comb decimation filter for the ΣΔ ADC presented in [21] was designed on the base of equivalent configurations and pipeline schemes. This decimation filter allows the reduction of the sampling frequency from 8.88GHz to 200MHz.

2.3.2 Pass-Band Compensation methods

In order to obtain a correct performance of the ΣΔ ADC, the decimation filter should have a flat magnitude response in the signal bandwidth, so that the decimated signal is not degraded with respect to the oversampled signal provided by the modulator. However, the magnitude response of comb-based decimators is not flat in the passband. Indeed, the passband of comb-based decimators experiences a magnitude decaying behavior, usually referred to as passband droop. In order to address this limitation, different compensators have been proposed to reduce the passband droop of comb-based decimation structures [28]-[37]. The simple compensator with only one parameter, which depends on the number of the stages K of the comb filter, has been proposed for wideband compensation in [28]. In [29] a comb decimator with high compensation capability using maximally flat error criterion, where the filter coefficients are obtained by solving linear system of equations, was proposed. This filter needs five multipliers. However, in [30] it is shown that one can obtain even better compensation using the simple multiplierless filter and the sharpening technique. In some cases, the proposed compensators require multipliers for their implementation. However, as comb structures can be synthesized as multiplierless filters, their associated compensators should be also implemented without multipliers. In addition, the compensator should not be redesigned every time the values of M and K are modified. As an illustration, Fig. 2.3 shows the passband magnitude response of a comb filter with M = 28 and K = 5 along with compensation methods [29], [30] and [33].

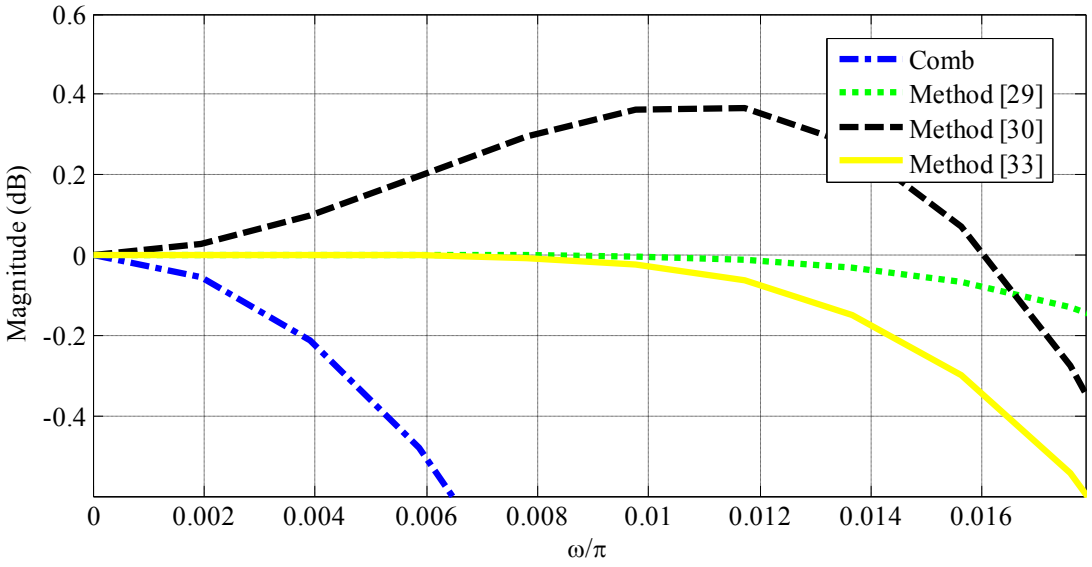


Fig. 2.3 Passband compensation in comb-based decimation filters.

2.3.3 Alias attenuation improvement methods

In addition to quantization noise, comb-based decimators for ΣΔMs have to cope with harmonic distortion introduced by the non-linear behavior of amplifiers as well as other sources of distortion not filtered by NTFs. However, the stopbands of a comb-based decimators are ordinarily very narrow, as each results from a single multiple zero [38]. Fortunately, there are several published works to improve the attenuation of comb-based decimators. The method presented in [39] introduces the zero rotation concept to comb-based decimators, and it provides increased attenuation at the expense of the introduction of two multipliers in the original CIC structure. However, in the finite precision implementation, the ideal pole-zero cancellation can be lost, thus leading to instability. The zero rotation method introduced in [39] has been generalized in [40], which provides better performance in terms of quantization noise rejection with respect to conventional comb decimation filters, at the cost of an increase in the computational complexity of the decimation filter realizations. The simplified rotated method of [41] applies the rotation only in the first folding band (where the worst case of attenuation occurs), and the subsequent bands are improved with cosine filters working at a low sampling rate. Recently, In [38] each multiple zero in the folding bands of a CIC decimator is separated into an equiripple stopband, improving the folding band deep by some 6(N-1) dB in an Nth-

order system. The increased computational complexity is modest: a few low-speed additions and multiplications by small integer coefficients that can often be chosen as powers of two. The majority of methods to improve alias attenuation in comb-based decimators usually increase the implementation filter complexity; thus, leading to an increased power consumption. Therefore, it is still necessary to develop methods that increase the alias rejection but keeping a low power consumption. Additionally, increased attenuation in comb-based decimator also leads to an increase in the passband droop. As an illustration, Fig. 2.4 shows the overall magnitude response of a comb filter with $M = 12$ and $K = 3$ along with the attenuation improvement methods [40], [41].

2.3.4 Simultaneous Pass-Band and Alias attenuation improvement methods

In [43] it has been proposed the application of the sharpening technique, developed by Kaiser and Hamming in [44], to the CIC decimator. In this way, the attenuation of the folding bands has been improved at the same time that the passband droop has been corrected. However, the magnitude response improvement of the sharpening technique is at the expenses of increased filter complexity, since the commonly used sharpening polynomial has the form of $3G(z)^2 - G(z)^3$. In this way, in [44] it is presented a two-stage

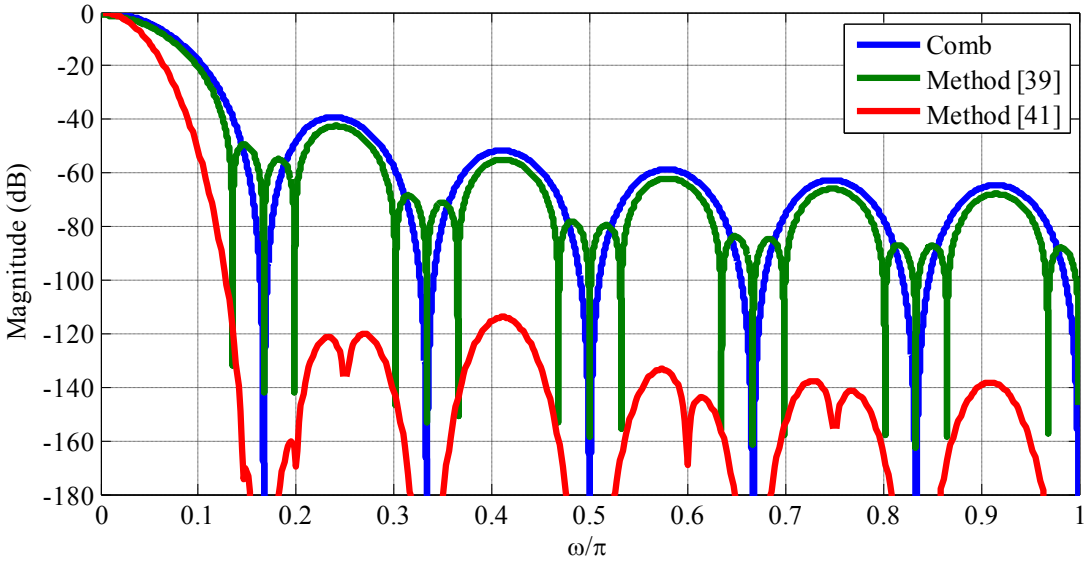


Fig. 2.4 Stop-band attenuation improvement.

comb-based decimator, where sharpening is only applied in the second stage: thus reducing the computational workload. Additionally, by the use of polyphase decomposition, the subfilters of the first stage can also be operated at the lower rate. In contrast to the sharpening–based methods, another approach to the simultaneous improvements of comb passband and folding bands was presented in [45]. Here, simple multiplierless corrector filters, each for the specified value of the comb parameter K are used. The filters are independent of the decimation factor and are designed using frequency sampling and IFIR (Interpolated Finite Impulse Response) techniques. . As an illustration, Fig. 2.5 shows the overall magnitude response of a comb filter with M = 12 and K = 3 along with the sharpening method used in [43]: additionally, a passband zoom is also illustrated.

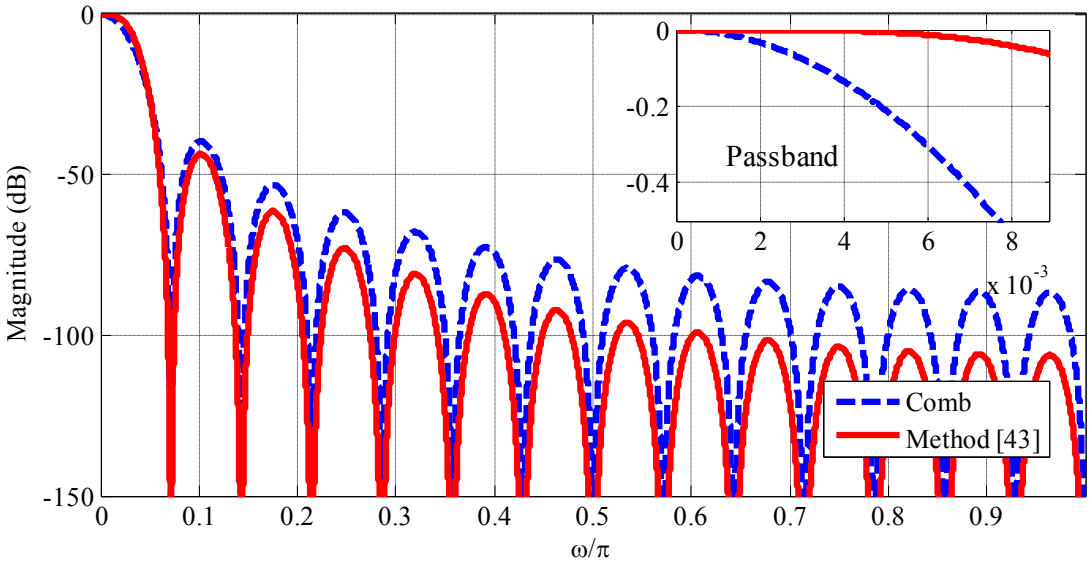


Fig. 2.5 Stop-band attenuation improvement and passband droop decrease.

2.4 Conclusions

This chapter has introduced the SDRs concept. It has been presented that the most popular way to implement SDRs is based on DCRs. DCRs with BP ADCs, directly digitizing RF signals, has superior performance compared to DRCs with LP ADCs.

The main challenge is the design of BP ADCs, since they must be able to convert the majority of wireless communications standards. Therefore, the use of BP CT-ΣΔMs with LC-based loop-filters becomes mandatory to digitize RF signals. Although LC-based BP

CT-ΣΔMs don't have enough degrees of freedom for their synthesis, there have been presented several topologies as the multi-feedback and FIR DAC topologies to overcome this issue. Nevertheless, they usually have used a fixed notch frequency, $f_n = f_s/4$, which limits the range of converted RF signals. Thus, in recent years the interest for reconfigurable BP CT-ΣΔMs with tunable notch frequency has been increased.

In other to complete the analog to digital conversion, it is necessary the use of DDCs after BP CT-ΣΔMs. DDCs use LP decimators to reduce the sampling rate. Comb-based decimators are widely used in the first decimation stage. In RF to Digital conversion, the signal coming out BP CT-ΣΔMs must be decimated from the GHz range to hundreds of kHz to teens of MHz: therefore, the use of power efficient comb-based decimators becomes mandatory.

Due to the low attenuation in the folding bands –which can introduce SNR degradation- and passband droop -which can introduce magnitude distortion in the decimated signal-, comb filters themselves cannot satisfy high performance demands of state-of-the-art ΣΔMs. Therefore, it is very important to design comb-based decimators with good magnitude responses but with low complexity.

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Chapter 3

LC-based Bandpass Continuous-Time Sigma-Delta Modulators with Widely Tunable Notch Frequency

This chapter presents bandpass continuous time ΣΔ modulators with a widely programmable notch frequency for the efficient digitization of radio-frequency signals in the next generation of software-defined-radio mobile systems. The modulator architectures under study are based on a fourth-order loop filter – implemented with two LC-based resonators – and a finite-impulsive-response feedback loop. Several topologies are studied, considering three different cases for the embedded digital-to-analog converter, namely: return-to-zero, non-returnto- zero and raised-cosine waveform. In all cases, a notch-aware synthesis methodology is presented, which takes into account the dependency of the loop-filter coefficients on the notch frequency and compensates for the dynamic range degradation due to the variation of the notch. The synthesized modulators are compared in terms of their sensitivity to main circuit error mechanisms and the estimated power consumption over a notch-frequency tuning range of 0.1fs to 0.4fs. The use of passive circuits for the implementation is also discussed considering either a fully passive or an hybrid active/passive circuit realization of the embedded resonators. Time-domain behavioral and macromodel electrical simulations validate this approach, demonstrating the feasibility of the presented methodology and architectures for the efficient and robust digitization of radio-frequency signals with a scalable resolution and programmable signal bandwidth.

3.1 Notch-Aware Synthesis of BP CT-ΣΔM

Fig. 3.1 shows the block diagram of the BP CT-ΣΔM under study. It consists of a fourth-order single-loop topology made up of two LC resonators with a transfer function

$$R(s) = \frac{\omega s}{(s^2 + \omega^2)}, \tag{3.1}$$

where normalized values of s and ω are considered with respect to f_s, so that $s = 2\cdot\pi\cdot f/f_s$ (with f standing for the frequency variable) and $\omega = 2\pi f_n/f_s$. The feedback loop is implemented by a RZ DAC and a two-tap half-delayed FIR structure, realized with four coefficients c_{1-4} in order to increase the degrees of freedom in the synthesis process when applying a CT-to-Discrete-Time (DT) equivalence [1]. An additional feedback path, with gain c_0, is included to compensate for the Excess Loop Delay (ELD) error. In addition, a full digital delay is placed between the quantizer output and the main DAC inputs, thus

The information presented in this chapter was mainly extracted from [18]-[21].

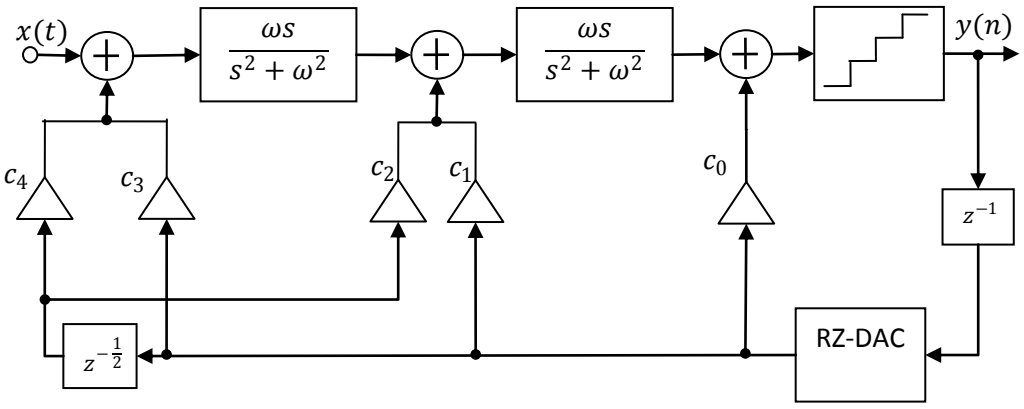


Fig. 3.1. Block diagram of a fourth-order LC-based BP CT-ΣΔM[1].

allowing a full sampling-period delay margin for the combined operation of the quantizer and DAC.

The modulator shown in Fig. 3.1 can be synthesized by applying the CT-to-DT equivalence to a fourth-order BP DT-ΣΔM with a NTF which satisfies the required specifications in terms of DR and BW. The well-known Schreier's toolbox [2] can be used to this purpose. Once the desired NTF(z) is obtained for a given notch frequency, f_n, and Out-of-Band Gain (OoBG), the DT version loop filter transfer function, can be easily derived as $H(z) = 1-1/NTF(z)$. The CT version of the loop-filter transfer function, $H(s)$, of the desired BP CT-ΣΔM is therefore derived from the well-known impulse invariant transformation presented in Chapter 1 and repeated here for convenience:

$$H(z) \equiv Z\{L^{-1}[H(s) \cdot H_{FIR-DAC}(s)]\} \tag{3.2}$$

where $Z(\cdot)$ and $L(\cdot)$ denote the Z-transform and L-transform symbols, respectively, and $H_{\text{FIR-DAC}}(s)$ is the transfer function of the FIR-based DAC. Note that, in this case, as an FIR-based RZ DAC transfer function is considered in Fig. 3.1 and this DAC waveform uses a half-delay, the modified Z-transform is a more suitable technique to compute (3.2) since there are delays that are not integer multiples of the sampling period, $T_s=1/f_s$ [1]. The

[1]It should be noted that a fourth-order LC-based loop filter has been used by the majority of state-of-the-art BP CT-ΣΔMs. For that reason, the work in this thesis focuses on modulator topologies like that shown in Fig. 3.1, although the presented synthesis methodology can be extended, without loss of generality, to other BP CT-ΣΔMs based on higher-order loop filters and/or including both feedforward and feedback paths.

residues theorem is therefore used to calculate the modified *Z*-transform of (3.2), considering the different resonator feedback paths and a constant value of f_n, which is $f_n=f_s/4$ in the majority of cases [1], [3]. However, the application of this method to a BP CT-ΣΔM with a widely tunable f_n would imply computing the modified *Z*-transform for each value of f_n, since the synthesized modulator is only stable within a very narrow band around f_n. Alternatively, the proposed methodology, referred to as *notch-aware synthesis*, computes the modified *Z*-transform of each modulator loop-filter path considering that f_n is a design (variable) parameter. This way, it can be shown that the transfer function from the modulator output to the input of the quantizer, computed for the different feedback branches with gain c_{1-4} in Fig. 3.1, can be written as:

$$H_{c_i}(s,v) = c_i \cdot e^{-s} \cdot [R(s,v)]^{\left\lceil \frac{i}{2} \right\rceil} \cdot H_{DAC}(s) \tag{3.3}$$

where $\lceil \cdot \rceil$ denotes the ceiling operator, and $R(s,v)$ and $H_{\mathrm{DAC}}(s)$ stand for the transfer function of the resonator and DAC, respectively given by:

$$R(s,v) = \frac{\left(\frac{\pi}{v}\right)s}{s^2 + \left(\frac{\pi}{v}\right)^2}, \tag{3.4}$$

$$H_{DAC}(s) = T_s \cdot \frac{e^{\frac{-t_d s}{T_s}} - e^{\frac{-(t_d+\tau)s}{T_s}}}{s}, \tag{3.5}$$

with $v=f_s/(2f_n)=\pi/\omega$ being a design parameter which accounts for the variation of f_n with respect to f_s, and t_d and τ standing respectively for the delay and duration of the rectangular pulse of the DAC waveform. Note that in the case of an RZ DAC, t_d = 0 and $\tau=T_s/2$. Therefore, applying the residues theorem, the modified *Z*-transform of (3.3) can be expressed as [3]:

$$H_{c_i}(z,v) = \sum_{\text{poles of } \frac{[R(s,v)]^{\lceil \frac{i}{2} \rceil}}{s}} \text{Res}\left[\frac{[R(s,v)]^{\lceil \frac{i}{2} \rceil}}{s} \cdot \frac{e^{m_1 s}}{z - e^{s}}\right] - \sum_{\text{poles of } \frac{[R(s,v)]^{\lceil \frac{i}{2} \rceil}}{s}} \text{Res}\left[\frac{[R(s,v)]^{\lceil \frac{i}{2} \rceil}}{s} \cdot \frac{e^{m_2 s}}{z - e^{s}}\right] \tag{3.6}$$

where Res[·] denotes the residues function, $m_1 = (1 - t_d/T_s)$ and $m_2 = 1-(t_d + \tau)/T_s$. Thus, in the case of the modulator in Fig. 3.1, $m_1 = 1$ and $m_2 = 1/2$ for feedback branches with gains c_1 and c_3, while $m_1 = 1/2$ and $m_2 = 0$, for the other branches (those with gains c_2 and c_4). In order to derive the loop-filter coefficients, c_i, the solution of (3.6) is expressed in partial-fraction form as:

$$H_{c_i}(z,v) \equiv \sum_{l=1}^{4}\left[\frac{\alpha_{il}(v)}{(\beta_{il}(v) + z)^l} + \frac{\alpha_{il}^*(v)}{(\beta_{il}^*(v) + z)^l}\right] + \frac{\alpha_{i0}}{z} \tag{3.7}$$

where $[\alpha_{il}(v), \alpha_{il}^*(v)]$ and $[\beta_{il}(v), \beta_{il}^*(v)]$ are the complex conjugated coefficients resulting from the partial-fraction form expansion of (3.6). For the sake of clarity, the results of applying (3.3)-(3.7) to each branch of Fig. 3.1 are shown in Appendix A. The resulted expressions of $H_{ci}(z, v)$ are used to compute the overall DT loop-filter transfer function, $H(z, v)$, yielding:

$$H(z,v) = \sum_{i=1}^{4} H_{c_i}(z,v) + c_0 \cdot z^{-1} \tag{3.8}$$

Therefore, in order to get the relationships between c_i and v, the DT-to-CT equivalence given in (3.2) is applied, yielding:

$$\sum_{i=1}^{4}\left\{\sum_{l=1}^{4}\left[\frac{\alpha_{il}(v)}{(\beta_{il}(v) + z)^l} + \frac{\alpha_{il}^*(v)}{(\beta_{il}^*(v) + z)^l}\right] + \alpha_{i0}(v) \cdot z^{-1}\right\} + c_0 \cdot z^{-1} = 1 - \frac{1}{NTF(z,v)} \tag{3.9}$$

Note that the terms, $\alpha_{i0}(v)\cdot z^{-1}$, result from the mentioned partial fraction-form decomposition of $H_{ci}(z, v)$. These terms can be cancelled out by the compensation feedback path with gain c_0. Thus, the above equation can be solved numerically for each value of v, i.e. for each value of f_n, using the MATLAB® script shown in Appendix A. This way, the modulator can be synthesized considering a reconfigurable set of loop-filter coefficients, $c_i(v) \equiv c_i(f_n)$, so that the desired $NTF(z)$ can be obtained within a given range of f_n, as illustrated in Fig. 3.2.

3.1.1 Effect of varying f_n on the input signal range

Fig. 3.3(a) shows the variation of c_i with the normalized notch frequency (f_n / f_s). Note that the values of these coefficients, specifically those of the main feedback path, tend to decrease as f_n increases. This reduction in the values of the loopfilter coefficients causes an attenuation of the input signal range, which becomes particularly critical for $f_n > f_s/4$. The opposite situation is given for $f_n < f_s/4$, for which the values of the loop-filter coefficients becomes relatively high compared to those obtained for $f_n = f_s/4$. As an illustration of this effect, Fig. 3.3(b) represents the Signal-to-Quantization-Noise Ratio (SQNR) versus the

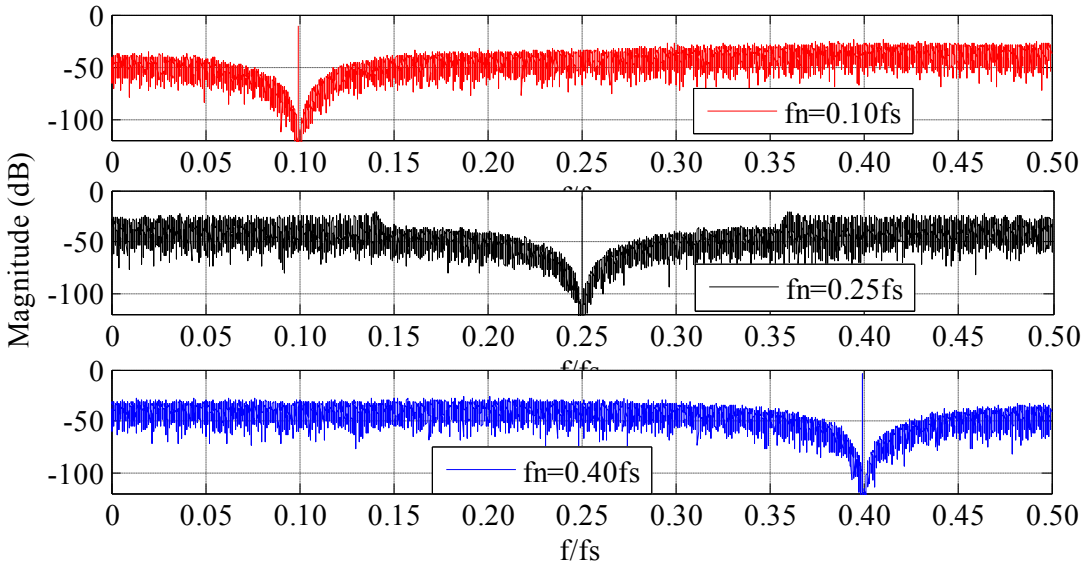
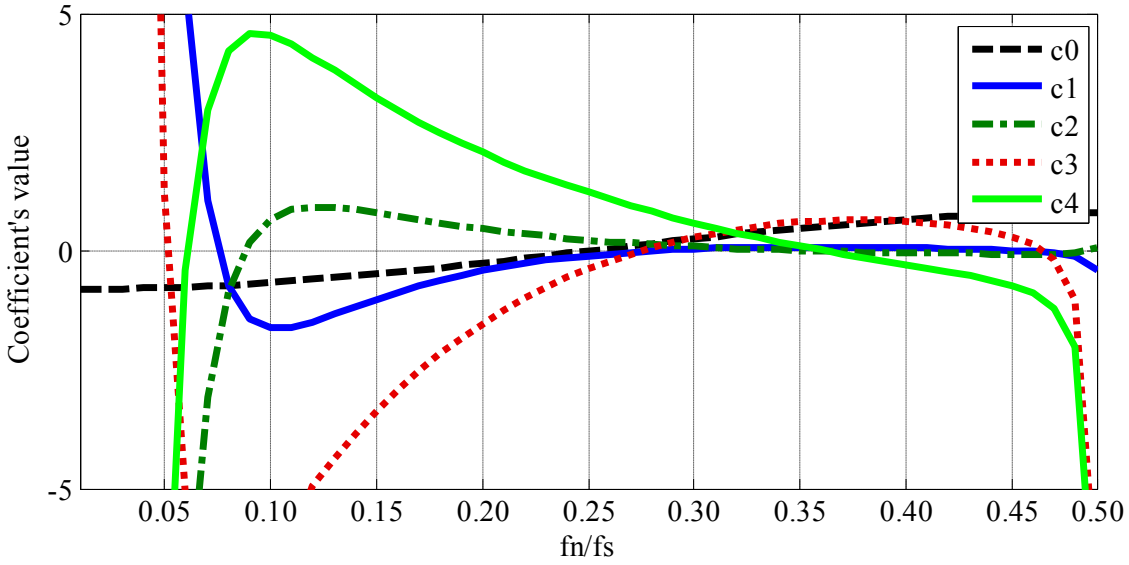
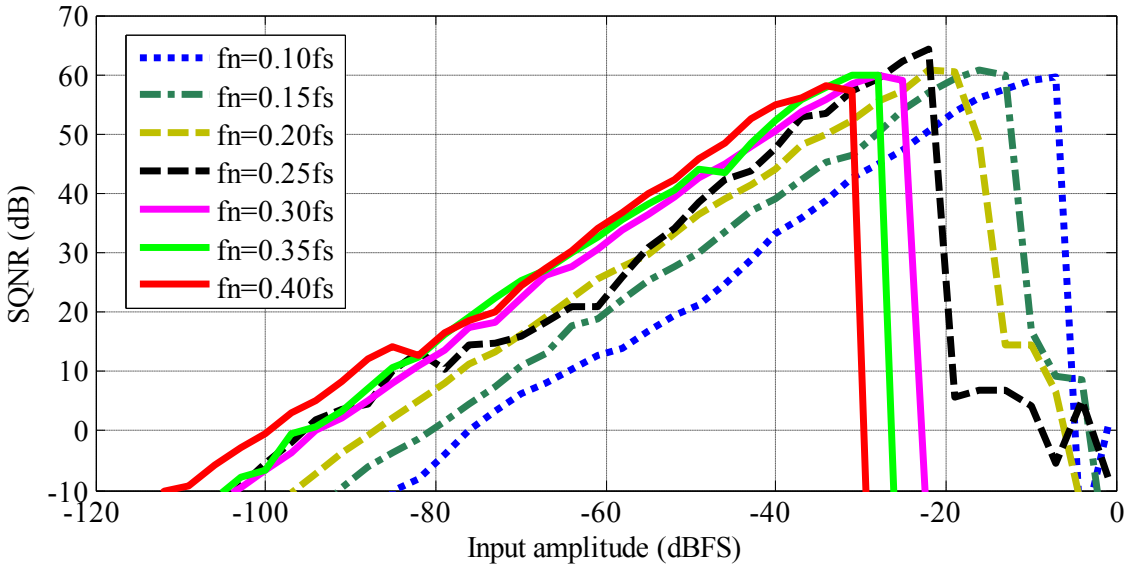


Fig. 3.2. Output spectra of modulator in Fig. 3.1 for different values of f_n. (Note that the *idle tones* observed for $f_n = f_s / 4$ are due to the correlation between the quantization error and the input signal, which is reduced in practice by nonidealities and/or using multi-bit quantization).



(a)



(b)

Fig. 3.3. Influence of f_n on the performance of Fig. 3.1: (a) Variation of loop filter coefficients. (b) SQNR vs. input signal amplitude, considering a 1-bit quantizer, f_s = 4GHz and OSR = 50.

input signal amplitude of the modulator in Fig. 3.1 considering a 1-bit quantizer, f_s = 4GHz, OSR = 50 and different values of f_n. It can be noted how the maximum input signal range is degraded as f_n increases. The attenuation of the input range is caused by the variation of the Signal Transfer Function (STF) with f_n. This variation should be taken into account in the synthesis procedure described above in order to keep the modulator performance over the

entire range of f_n. To this purpose, the expression of $STF(z)$ can be obtained by using a linear model for the quantizer in the DT equivalent diagram of Fig. 3.1, giving:

$$STF(z,v) = \frac{Z\{[R(s,v)]^2\}}{1+H(z,v)} \tag{3.10}$$

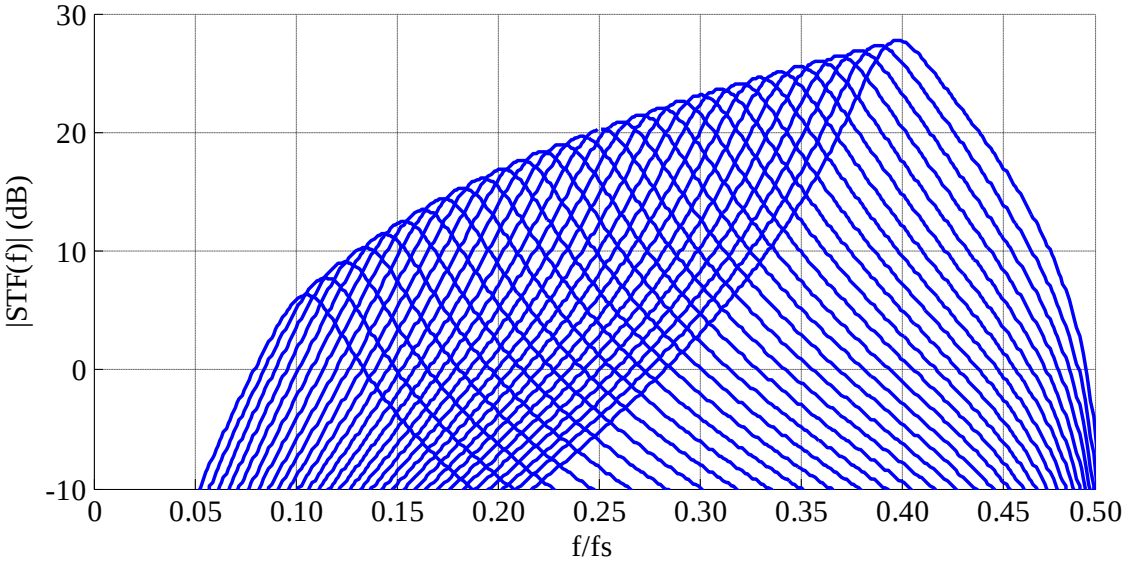
where $H(z, v)$ can be derived from (3.8) and the numerator of $STF(z, v)$ is obtained by using a conventional Z-transform since there are not any fractional delays in the feedforward path of Fig. 3.1. Therefore, applying these transforms and considering that $z = e^{j2\omega f/fs}$, with $j \equiv \sqrt{-1}$, the expression of $STF(f)$ can be derived from (3.10). Fig. 3.4(a) represents the magnitude of $STF(f)$ versus f/f_s for different values of f_n within the interval $f_n/f_s \in (0.1, 0.4)$. It can be noted that $|STF(f)|$ increases with f_n/f_s, which may explain the *premature* modulator overload obtained in Fig. 3.3(b) for higher values of f_n/f_s. This result can be derived from (3.10), by replacing $v = \pi/\omega$ in (3.4), so that the expression in (3.10) can be written as:

$$STF(z,v) = \frac{Z\left\{\left[\frac{\omega s}{(s^2+\omega^2)}\right]^2\right\}}{1+H(z,v)} = \omega^2 \cdot \frac{Z\left\{\left[\frac{s}{(s^2+\omega^2)}\right]^2\right\}}{1+H(z,v)} \tag{3.11}$$

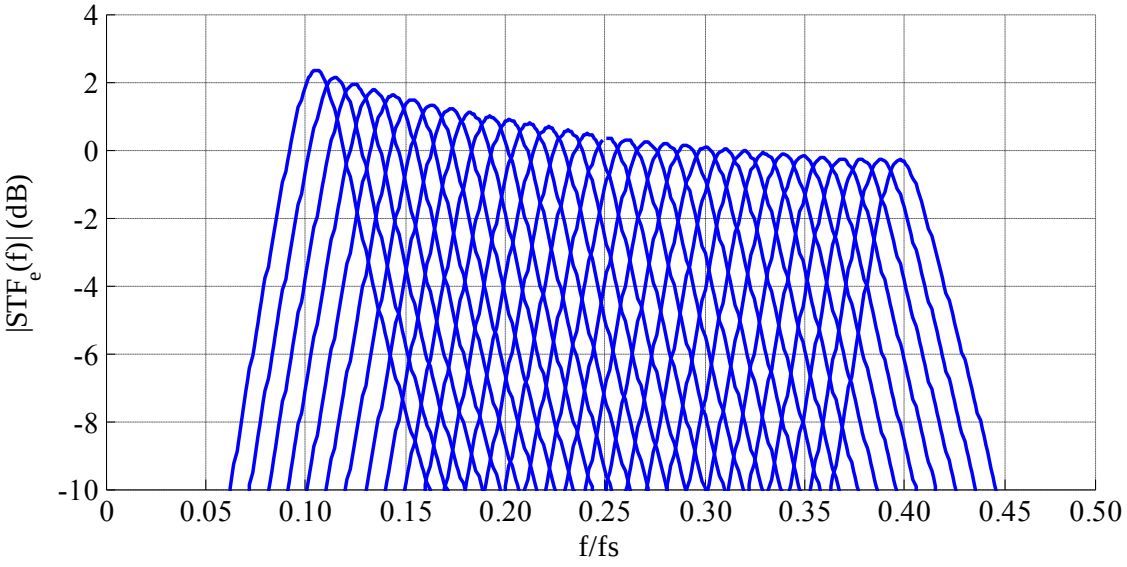
Note from (3.11) that $|STF(z, v)|$ is proportional to ω^2. Therefore, the effect of f_n can be approximately compensated if $STF(f)$ is multiplied by a factor proportional to $1/\omega^2$, so that the *equalized* expression of *STF* is given by:

$$STF_e(z,v) = k(v) \cdot STF(z,v) \tag{3.12}$$

where $k(v) \equiv 1/4 \cdot 1/\omega^2 = 1/(2\omega)^2 = (v/2\pi)^2$ stands for the equalization factor. This factor includes a proportionality coefficient of 1/4 in order to keep the magnitude of $|STFe(fn)| \approx$ 0 dB over the entire range of f_n/f_s, as illustrated in Fig. 3.4(b). Indeed, there is a difference of approximately 2dB between the maximum and the minimum values of $|STF_e(f_n)|$. That difference could be compensated by including a more accurate expression of the equalization factor, $k(v)$, which takes into account the nonlinear dependency of both the numerator and denominator of $STF(f)$ on f_n. However, such a polynomial expression of $k(v)$ would be more complicated to implement in a practical circuit based on transconductors.



(a)

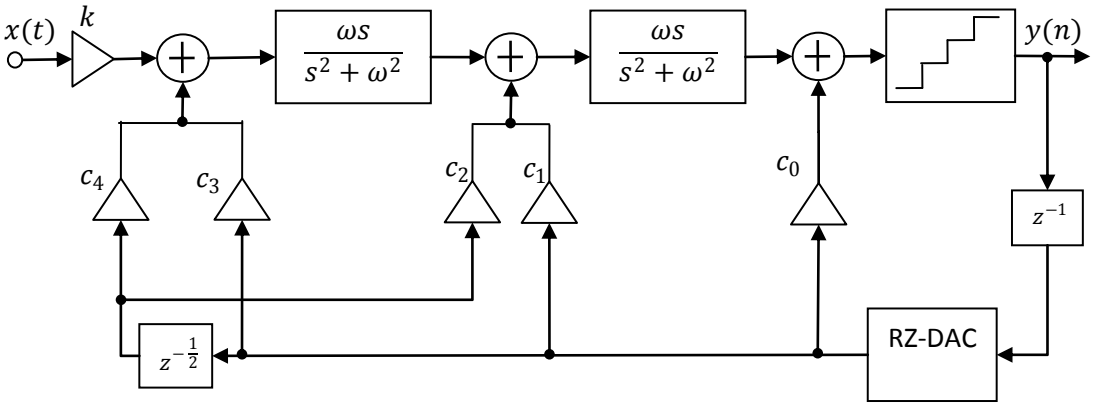


(b)

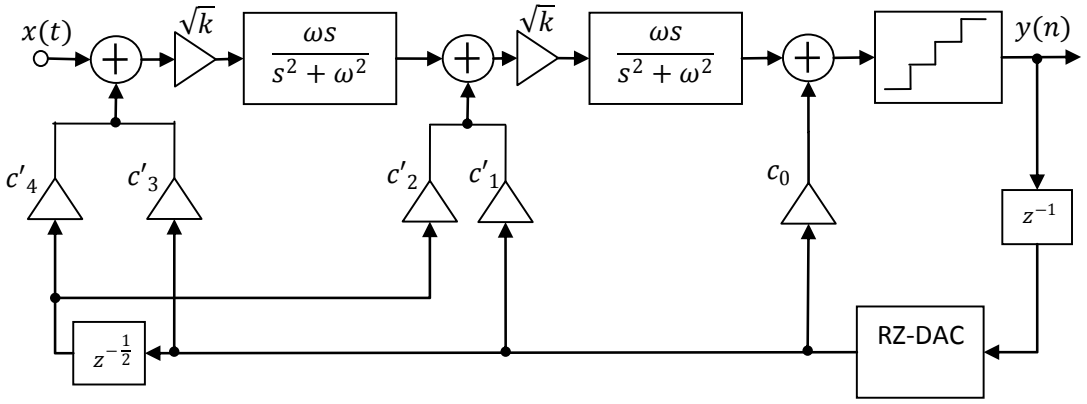
Fig. 3.4. Effect of varying f_n on $STF(f)$. (a) $|STF(f)|$ versus f / f_s. (b) $|STF_e(f)|$ versus f/f_s.

3.1.2 Alternative BP CT-ΣΔM architectures with equalized STF

Fig. 3.5 shows two alternative versions of the modulator shown in Fig. 3.1, that includes the equalization factor $k(v)$ to compensate for the $STF(f)$ variation with f_n. Fig. 3.5(a) shows the most direct way of implementing such a factor as a preamplifier in front of



(a)



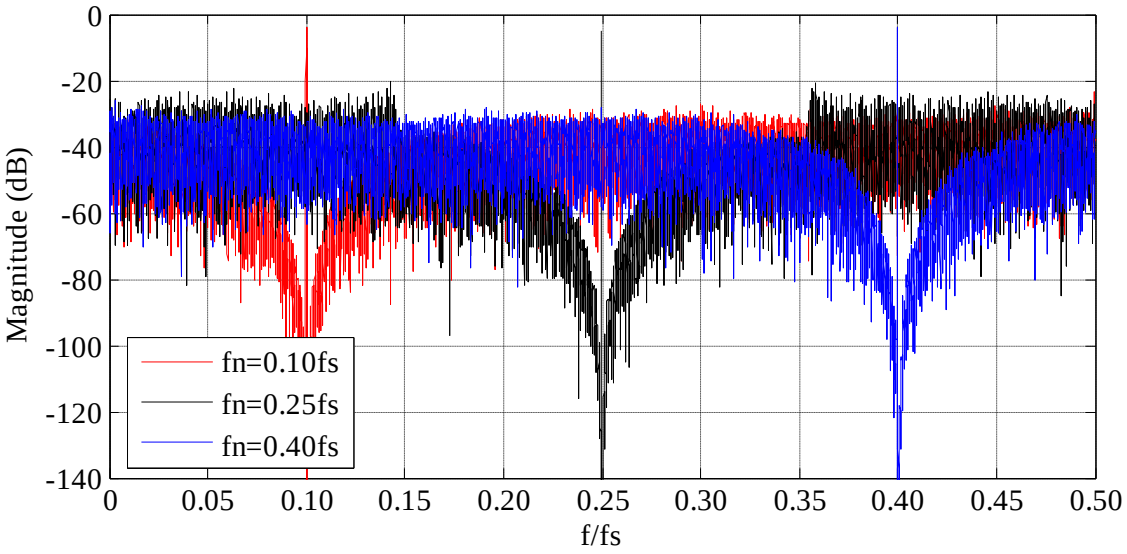
(b)

Fig. 3.5. Alternative implementations of Fig. 3.1 with equalized STF. (a) BP CT-ΣΔM with a single preamplification factor of $k(v)$ (referred to as BPΣΔ-A). (b) BP CT-ΣΔM with a preamplification distributed between both resonators in the modulator chain (named BPΣΔ-B).

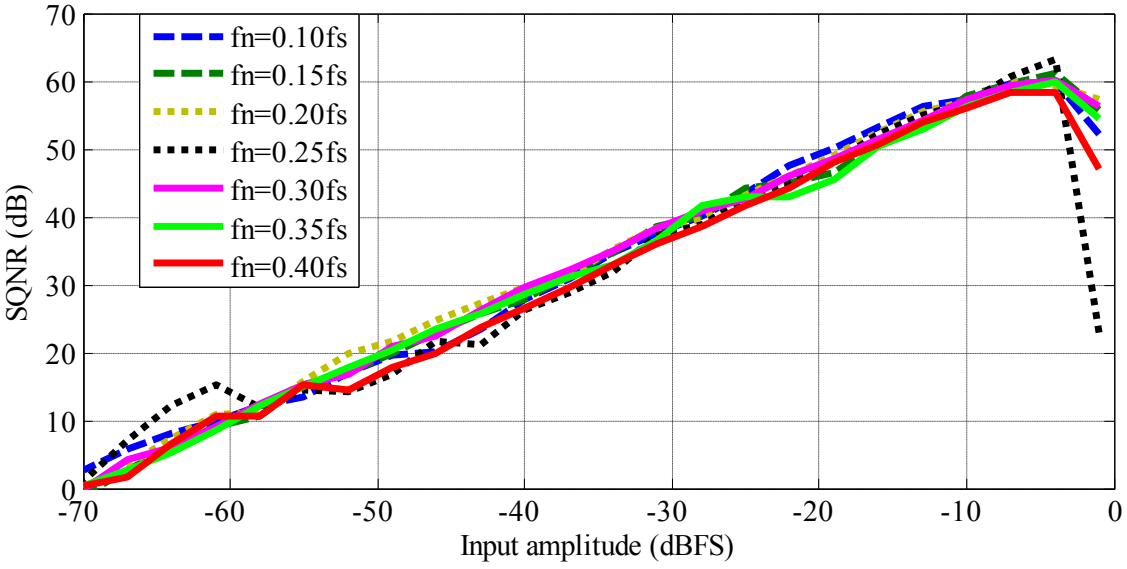
the modulator, while Fig. 3.5(b) is an alternative implementation where the effect of $k(v)$ is distributed through both resonators in the modulator chain. As a result, the loop-filter coefficients in Fig. 3.5(b), denoted as c_i', are scaled with respect to those used in Fig. 3.5(a) and Fig. 3.1, denoted as c_i. Indeed, both modulators would feature the same ideal performance provided that

$$c_i' = \frac{c_i}{(2\omega)^{\left\lceil \frac{i}{2} \right\rceil}} \quad \text{for } i = 1,2,3,4 \tag{3.13}$$

To simplify the notation, the BP CT-ΣΔMs in Fig. 3.5(a) and Fig. 3.5(b) will be referred to as BPΣΔ-A and BPΣΔ-B, respectively. As an illustration, Fig. 3.6 shows the effect of varying f_n on the output spectrum (Fig. 3.6(a)) and on the SQNR (Fig. 3.6(b)). It can be noted that, as expected, the noise shaping performance and the overloading signal amplitude is kept constant over the entire range of f_n from $0.1f_s$ to $0.4f_s$.



(a)



(b)

Fig. 3.6. Effect of varying f_n on the performance of BPΣΔ-A. (a) Output spectra. (b) SQNR vs. input signal amplitude.

3.2 Extension to other LC-Based BP CT-ΣΔMs

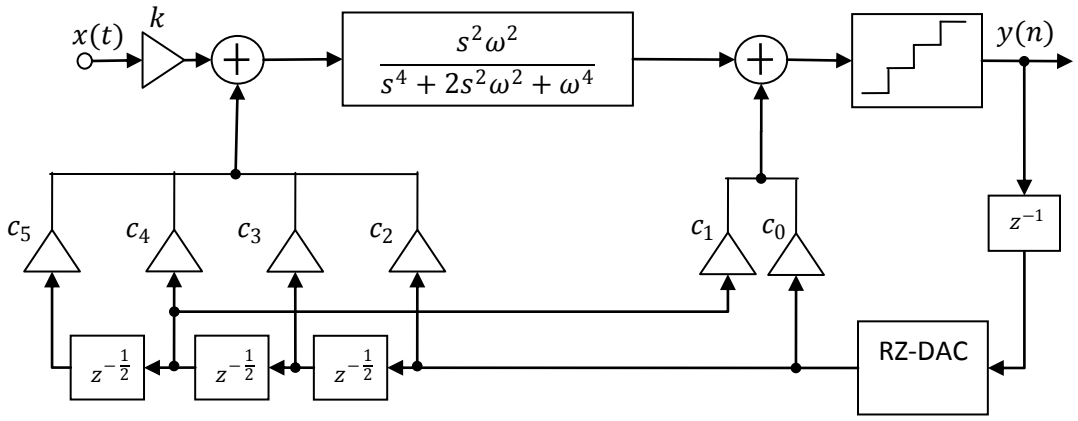
The *notch-aware* synthesis procedure described above can be extended to other families of LC-based BP CT-ΣΔMs with different loop-filter implementations and feedback DAC waveforms. As an application, an alternative topology of the modulator loop filter based on an LC-based single block, and two different cases of DAC waveforms – NRZ and RCos – are discussed in this section.

3.2.1 LC-based single-section BP CT-ΣΔMs with tunable f_n

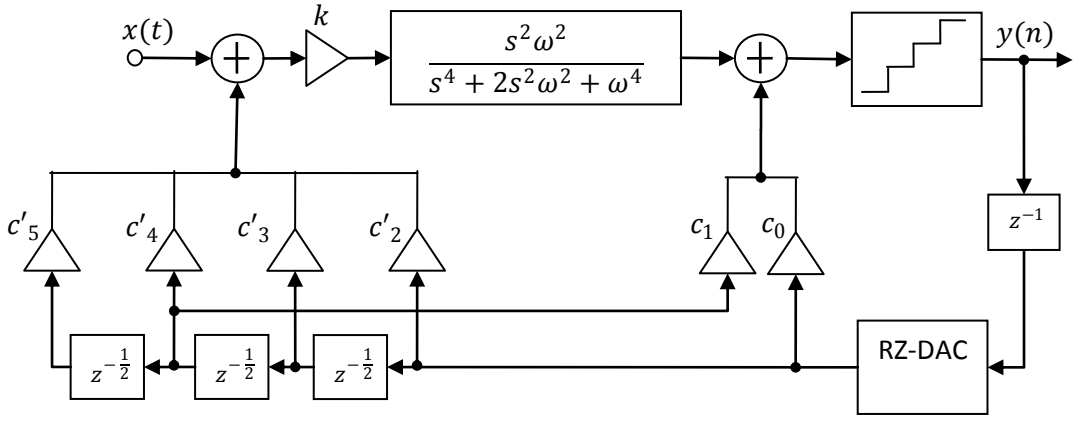
Fig. 3.7 shows the block diagram of two alternative BP CT-ΣΔMs, which will be referred to as BPΣΔ-C (Fig. 3.7 (a)) and BPΣΔ-D (Fig. 3.7 (b)). Both modulators are based on the use of a FIR-feedback DAC and an LC based *single-section* loop filter, i.e. without using either any intermediate node or feedback path, apart from that required for the ELD compensation [4], [5]. The only difference between both topologies in Fig. 3.7 is the way in which the STF equalization factor, $k(v)$, is implemented in the loop filter. Thus, BPΣΔ-C (Fig. 3.7(a)) uses a single preamplifier in front of the modulator, as done by BPΣΔ-A (Fig. 3.5(a)), while BPΣΔ-D (Fig. 3.7(b)) distributes the equalization factor between the feedforward and feedback blocks of the modulator – similarly to BPΣΔ-B (Fig. 3.5(b)). Both BP CT-ΣΔMs in Fig. 3.7 can be synthesized following the same procedure presented in Section 3.1 in order to increase the tuning range of f_n, while keeping the noise-shaping performance. To this end, the loop filter coefficients, c_{0-5}, in Fig. 3.7(a) are obtained by solving (3.9) for each value of v. The only difference is that the expression of $H_{ci}(s, v)$ in this case is given by:

$$H_{c_i}(s,v)\big|_{\mathrm{CD}} = c_i \cdot e^{-sp} \cdot \left[\frac{\left(\frac{\pi}{v}\right)s}{s^2+\left(\frac{\pi}{v}\right)^2}\right]^{\left\lfloor\frac{2i}{i+2}\right\rfloor} \cdot H_{\mathrm{DAC}}(s) \qquad (3.14)$$

where $p = 1$ for $i = 0, 2, 3$ and $p = 2$ for $i = 1, 4, 5$, and $\lfloor\cdot\rfloor$ stands for the floor operator. Thus, applying the modified Z-transform to (3.14), the modulator loop-filter coefficients can be derived as a function of the notch frequency, by solving (3.7) for the different cases



(a)



(b)

Fig. 3.7. Alternative implementations of BP CT-ΣΔMs based on a single section LC loop filter. (a) With a single preamplification factor (denoted as BPΣΔ-C). (b) With a preamplification distributed between the feedforward and the feedback blocks in the modulator chain (denoted as BPΣΔ-D).

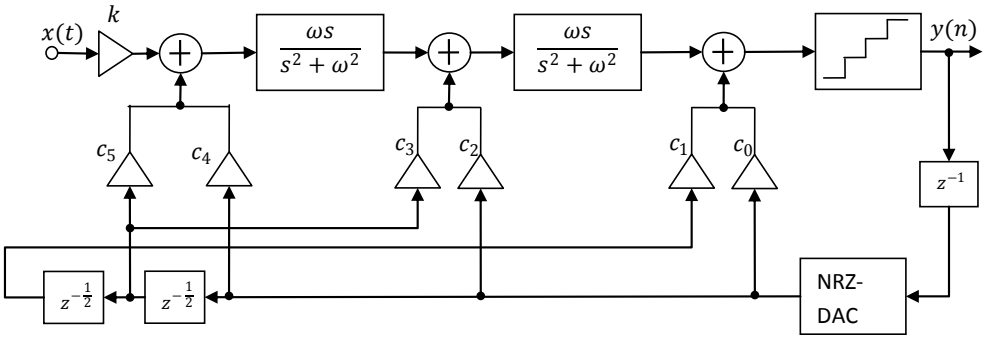
of *v*. Proceeding in a similar way as for BPΣΔ-B, the loop-filter coefficients of BPΣΔ-D, denoted as c'_i in Fig. 3.7(b), can be scaled from those used in Fig. 3.7(a), according to the relation given in (3.13), for i = 1, 2, 3, 4, 5.

3.2.2 Application to different feedback DAC waveforms

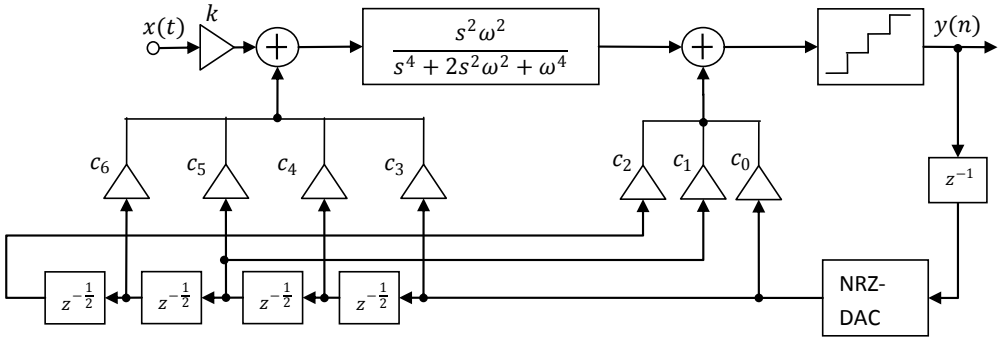
All modulator architectures discussed in previous sections include a feedback DAC with RZ waveform. However, the presented *notch-aware* synthesis method can be applied also to other DAC waveforms by adapting the corresponding transfer functions in (3.2)-

(3.9). As a case study, Fig. 3.8 shows how the block diagrams of the modulators BPΣΔ-A and BPΣΔ-C are modified if an FIR-based NRZ DAC is considered. As a consequence of using a different DAC waveform, the expressions in (3.3) and (3.14) for Fig. 3.8(a) and Fig. 3.8(b) transform respectively into the following expressions:

$$
\begin{aligned}
H_{c_i}(s,v)\big|_{\mathrm{A-NRZ}} &= c_i \cdot e^{-sp} \cdot \left[\frac{\left(\frac{\pi}{v}\right)s}{s^2+\left(\frac{\pi}{v}\right)^2}\right]^{\left\lfloor\frac{i}{2}\right\rfloor} \cdot H_{\mathrm{NRZ-DAC}}(s) \\
&(P=2\ for\ i=1\ and\ P=1\ for\ i=0,2,3,4,5) \\
H_{c_i}(s,v)\big|_{\mathrm{C-NRZ}} &= c_i \cdot e^{-sp} \cdot \left[\frac{\left(\frac{\pi}{v}\right)s}{s^2+\left(\frac{\pi}{v}\right)^2}\right]^{\left\lfloor\frac{2i}{i+2}\right\rfloor} \cdot H_{\mathrm{NRZ-DAC}}(s) \\
&(P=2\ for\ i=1\ and\ P=1\ for\ i=0,2,3,4,5)
\end{aligned}
\tag{3.15}
$$



(a)



(b)

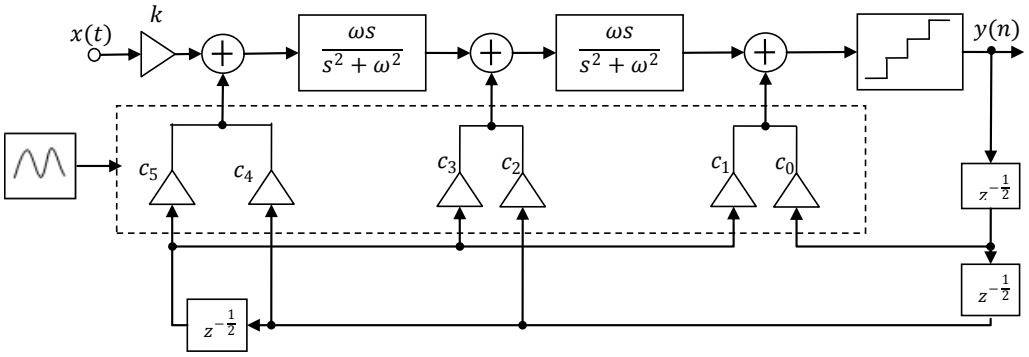
Fig. 3.8. Alternative LC-based BP CT-ΣΔMs with NRZ feedback DAC. (a) BPΣΔ-A. (b) BPΣΔ-C.

where $H_{\text{NRZ-DAC}}(s)$ is the transfer function of the NRZ DAC, given by (3.5) with $t_d = 0$ and $\tau = T_s$. In the case of NRZ DACs, $H_{ci}(z, v)$ can be computed by using the 'c2d' function provided by the Control Toolbox in MATLAB® [6]. This function can convert any delayed analog versions into digital ones, provided that the shape of the feedback is of NRZ type. Therefore, all the required transformations to derive $H_{ci}(z, v)$ and the expressions of the loop-filter coefficients, c_i, can be obtained in this case by using c2d instead of applying the modified *Z*-transform as in previous section. The rest of the procedure is the same as that followed for the RZ DAC case and can be also implemented in a MATLAB® script as is shown in Appendix A. Ideally, the performance of the synthesized BP CT-ΣΔMs with NRZ feedback DAC is the same as that obtained for those topologies with RZ DAC. However, one of the main limitations of using rectangular (either NRZ or RZ) DACs arise when undersampling is used in BP CT-ΣΔMs [4]-[7]. In this case the modulator performance is degraded by two effects. One is the attenuation of the RF mirrored replica signal in the Nyquist band and the other is the reduction of the quality factor of the resulted NTF. These problems can be partially reduced by using a RCos DAC waveform [1], [7]. This DAC waveform can be included in the BP CT-ΣΔMs under study – illustrated in Fig. 3.9. It can be shown that the expression of $H_{ci}(s, v)$ for the modulators in Fig. 3.9(a)-(b) are respectively given by:

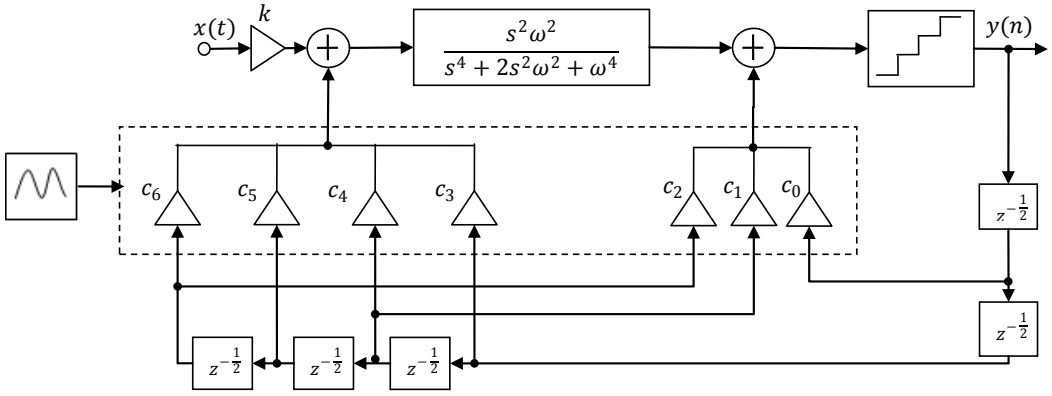
$$
\begin{aligned}
H_{c_i}(s,v)\big|_{\text{A-RCos}} &= c_i \cdot e^{-sp} \cdot \left[\frac{\left(\frac{\pi}{v}\right)s}{s^2+\left(\frac{\pi}{v}\right)^2}\right]^{\left|\frac{i}{2}\right|} \cdot H_{\text{RCos -DAC}}(s) \\
&(P = 2\ for\ i = 1\ and\ P = 1\ for\ i = 0,2,3,4,5) \\
H_{c_i}(s,v)\big|_{\text{C-RCos}} &= c_i \cdot e^{-sp} \cdot \left[\frac{\left(\frac{\pi}{v}\right)s}{s^2+\left(\frac{\pi}{v}\right)^2}\right]^{\left|\frac{2i}{i+2}\right|} \cdot H_{\text{RCos -DAC}}(s) \\
&(P = 2\ for\ i = 1\ and\ P = 1\ for\ i = 0,2,3,4,5)
\end{aligned}
\tag{3.16}
$$

where $H_{\text{RCos-DAC}}(s)$ is the transfer function of the RCos DAC, given by:

$$
H_{\text{RCos -DAC}}(s) = \frac{\omega_d^2 \cdot (1 - e^{s}) \cdot e^{\frac{-t_d s}{T_s}}}{s(s^2 + \omega_d^2)} \tag{3.17}
$$



(a)



(b)

Fig. 3.9. Alternative LC-based BP CT-ΣΔMs with RCos feedback DAC. (a) BPΣΔ-A. (b) BPΣΔ-C.

and ω_d stands for the angular frequency of the DAC sinewave. In this case, it can be shown that the modified *Z*-transform of (3.16) for the modulator BPΣΔ-A is given by:

$$H_{c_i}(s,v)\big|_{\mathrm{C-RCos}} = \frac{1}{1-z^{-1}} \sum_{\text{poles of } F_R(s,v)} \mathrm{RES}\left[F_R(s,v)\frac{e^{ms}}{z-e^{s}}\right] \tag{3.18}$$

where $m = 1$ for $i = 2,4$, $m = 1/2$ for i=0,1,3,4 and

$$F_R(s,v) = \frac{\omega_d^2}{s(s^2+\omega_d^2)} \cdot R(s,v). \tag{3.19}$$

The expression in (3.18) is also valid for BPΣΔ-C, but considering that $m = 1/2$ for $i = 0, 1, 2, 4, 5$ and $m = 1$ for $i = 3, 5$. Thus, once the expression in (3.18) is computed, the rest of the *notch-aware* synthesis procedure can be applied as described in Section 3.1.

3.3 Nonideal performance and comparative study

The analysis presented in previous sections has assumed that the BP CT-ΣΔMs under study have been implemented with ideal building blocks. However, in practice, the noise shaping performance of these modulators is degraded by the action of circuit-error mechanisms. This section analyses and compares the degradation caused by some of the most critical nonideal effects which affect the performance of LC-based BP CT-ΣΔMs, namely: limited Input/Output Swing (I/OS) of the resonators, finite quality factor, Q, and mismatch. To this end, it will be assumed that all modulators are implemented by Gm-LC resonators, while the feedback path is implemented using Current Steering (CS) DACs. As an illustration, Fig. 3.10 shows the conceptual Gm-LC schematic of the BP CT-ΣΔM showed in Fig. 3.1. All transconductances in the loop filter, gm_{0i}, are defined as a multiple of a unitary transconductance element, gm_u. In a similar way, the output currents, I_i, provided by the feedback FIR-based CS DAC are defined as a function of a unitary current source, I_u, which can be easily implemented at circuit level by using current mirrors. In this work, we will assume a full-flash ADC to implement the embedded quantizer, with a reconfigurable number of bits, $B = 1, 2, 3, 4$, and a Full-Scale (FS) reference voltage of VFS = 1V. The nonideal performance of all modulators has been analysed and compared by considering a fully-differential implementation of the schematic in Fig. 3.10, based on time domain behavioral simulations carried out in SIMSIDES [8]. In all cases, a variation of the notch frequency in the range $f_n = 0.1 - 0.4 f_s$ is considered, and three different DAC waveforms (RZ, NRZ and RCos) are used. Note that, from an ideal point of view, all these case studies present the same noise-shaping performance over the target tuning range of f_n. As an illustration, Fig. 3.11 shows the ideal SQNR which can be achieved by the BP CT-ΣΔMs under study with an RZ DAC as a function of B and OSR. It can be noted that the dependency on the OSR is the same in all modulators under study. For that reason, in the analysis that follows, a fixed value of OSR= 50 will be assumed for the sake of simplicity

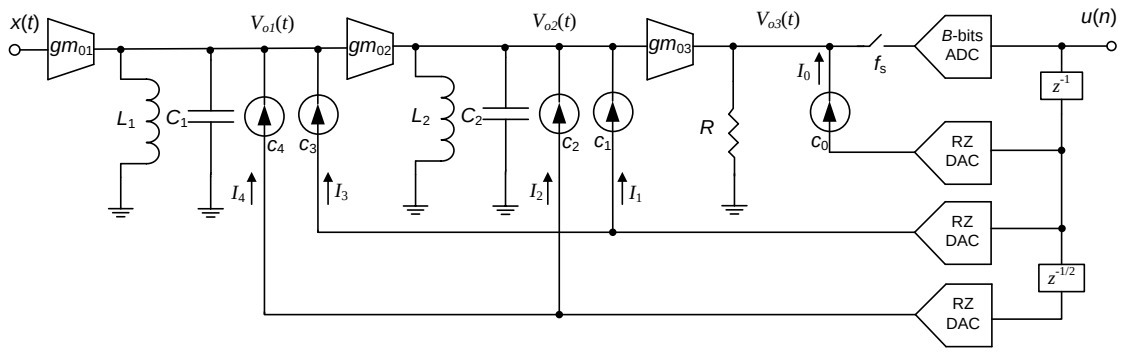


Fig. 3.10. Conceptual Gm-LC schematic of the BP CT-ΣΔM in Fig. 3.1.

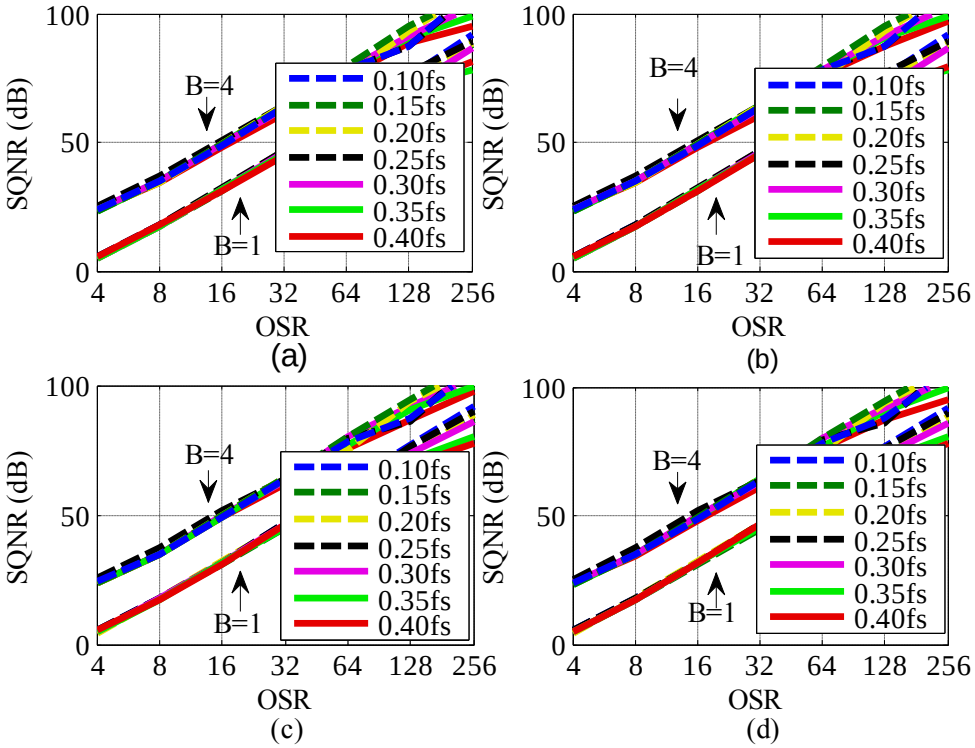


Fig. 3.11. SQNR versus OSR and B for different cases of f_n. (a) BPΣΔ-A. (b) BPΣΔ-B. (c) BPΣΔ-C. (d) BPΣΔ-D.

without loss of generality. However, the impact of varying B has a different effect on the I/OS for each BP CT-ΣΔM.

3.3.1 Limited input/output swing of loop-filter resonators

Fig. 3.12 shows the effect of I/OS on the SNR of BPΣΔ-A with RZ feedback DAC and different cases of f_n. As expected, the required values of I/OS become more relaxed as B

increases – a behavior which is similar in all BP CT-ΣΔMs under consideration. Note also that, regardless the value of B, two families of curves can be distinguished according to the relation between f_n and f_s. That is, the I/OS requirements are in general more demanding when $f_n < f_s / 4$. The performance achieved by BPΣΔ-B with RZ feedback DAC is similar to that shown in Fig. 3.12, except for $B \leq 2$. In these cases, the I/OS requirements are more demanding than for BPΣΔ-A with RZ DAC, becoming unfeasible as f_n approaches $0.1f_s$, mainly due to the increasingly variability of loop-filter coefficients as f_n is reduced (see Fig. 3.3(a)). The influence of the DAC waveform is illustrated in Fig. 3.13 and Fig. 3.14, which show the effect of I/OS on the SNR for an NRZ DAC and an RCos DAC. Overall, the best performance is achieved by BPΣΔ-A and BPΣΔ-B, regardless the DAC and the value of f_n and B. The required I/OS specifications of these architectures are shown in Table 3.1 for $B > 1$ and $f_n = 0.1$, 0.25 and $0.4f_s$. Note that the most relaxed values of I/OS are obtained by BPΣΔ-A with NRZ DAC.

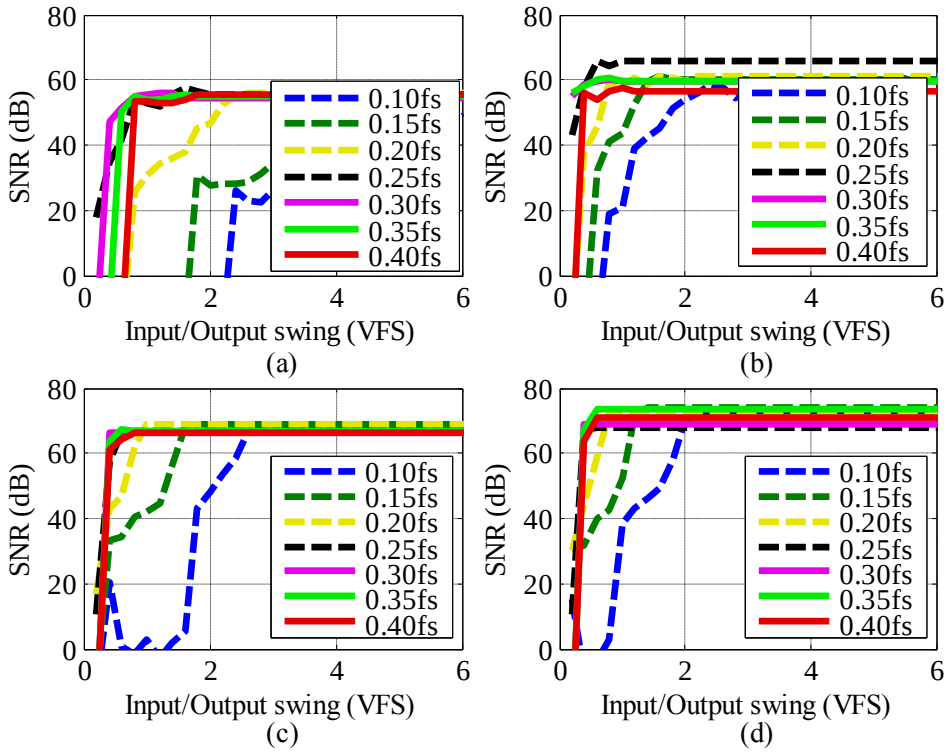


Fig. 3.12. Effect of I/OS (relative to *V*FS) on the SNR of BPΣΔ-A with RZ DAC and (a) $B = 1$, (b) $B = 2$, (c) $B = 3$ and (d) $B = 4$.

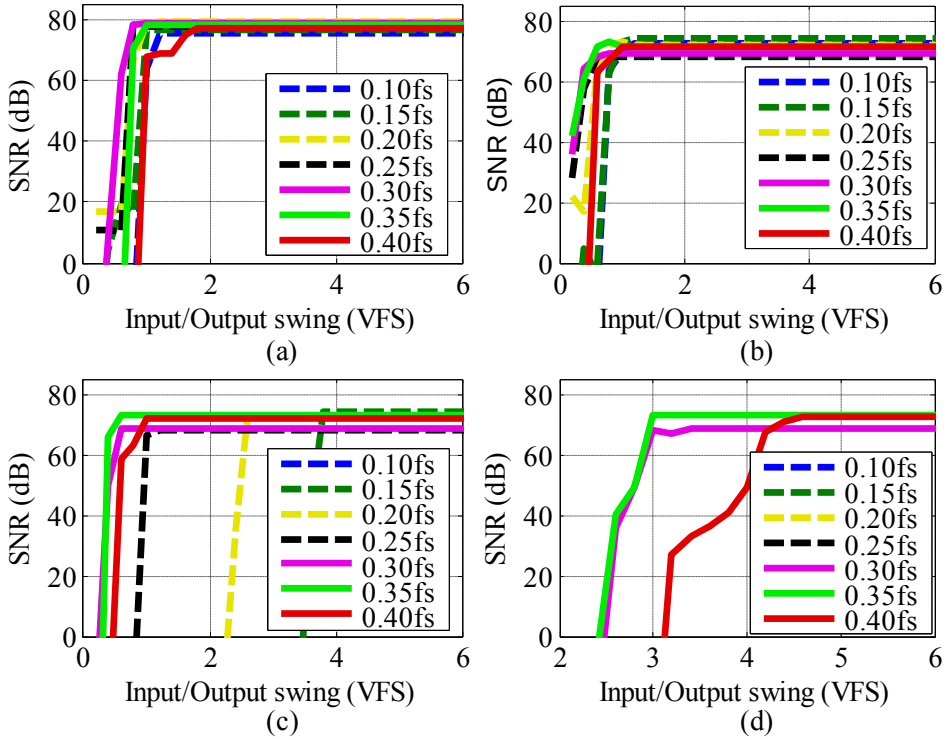


Fig. 3.13. Effect of I/OS the SNR with NRZ DAC and B = 4 for: (a) BPΣΔ-A, (b) BPΣΔ-B, (c) BPΣΔ-C and (d) BPΣΔ-D.

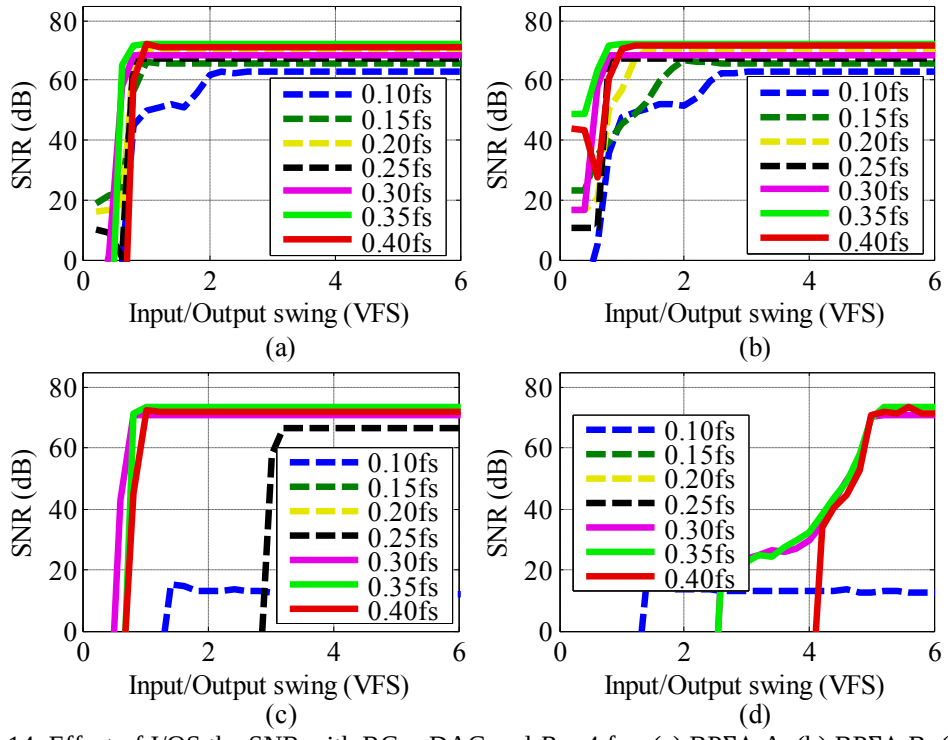


Fig. 3.14. Effect of I/OS the SNR with RCos DAC and B = 4 for: (a) BPΣΔ-A, (b) BPΣΔ-B, (c) BPΣΔ-C and (d) BPΣΔ-D. (Note that the behavior of BPΣΔ-C and BPΣΔ-D becomes unstable for $f_n / f_s = 0.1$).

Table 3.1. I/OS Requirements for BPΣΔ-A AND BPΣΔ-B, (f_n / f_s = 0.1, 0.25, 0.4).

DAC	B	BPΣΔ-A			BPΣΔ-B		
		0.1	0.25	0.4	0.1	0.25	0.4
RZ	2	6	1.5	1.5	6	1.5	1.5
	3	4	0.8	1.2	4	0.8	1.2
	4	4	0.8	1.1	4	0.8	1.1
NRZ	2	2.5	0.5	0.5	3	1	1
	3	1.5	0.5	0.5	2	0.9	0.9
	4	0.9	0.7	0.7	0.5	0.5	0.5
RCos	2	3	1	1	3	1.1	1.1
	3	2.5	1	1	3	1.1	1.1
	4	2	1	1	2.8	1	1

3.3.2 Finite quality factor

Fig. 3.15 shows the effect of the finite quality factor, Q, on the SNR, considering B = 4 and an RZ DAC. It can be noted that the Q requirements are less restrictive as the ratio f_n / f_s decreases. Overall, the behavior of all BP CT-ΣΔMs is approximately the same, obtaining an ideal performance for $Q > 20$, when $f_n = 0.1f_s$. This limit becomes more demanding as f_n / f_s increases, requiring $Q > 70$ for $f_n = 0.4f_s$. The type of feedback DAC waveform does not have a significant impact on the requirements of Q, although there is a larger degradation when an RCos DAC is used. This is illustrated in Fig. 3.16, where it can be noted that, the required values of Q to achieve the ideal performance are in general more demanding than in the case of using an RZ DAC.

The results obtained for all cases under study are summarized in Table 3.2. The most demanding modulators are BPΣΔ-B and BPΣΔ-D with RCos feedback DAC, requiring $Q >$ 90 for $f_n > 0.25f_s$, while BPΣΔ-C and BPΣΔ-D become unstable for $f_n = 0.1f_s$.

3.3.3 Mismatch

To conclude the nonideal analysis, let us consider that the loop-filter coefficients of the modulators under study have an error caused by technology process variations. These variations are due to circuit element tolerances and component mismatches. The former can be controlled in practice by using tuning and proper calibration of the circuit elements. However, mismatch error still remains and need to be computed to check the robustness and stability of a given modulator topology over the target tuning range. This computation

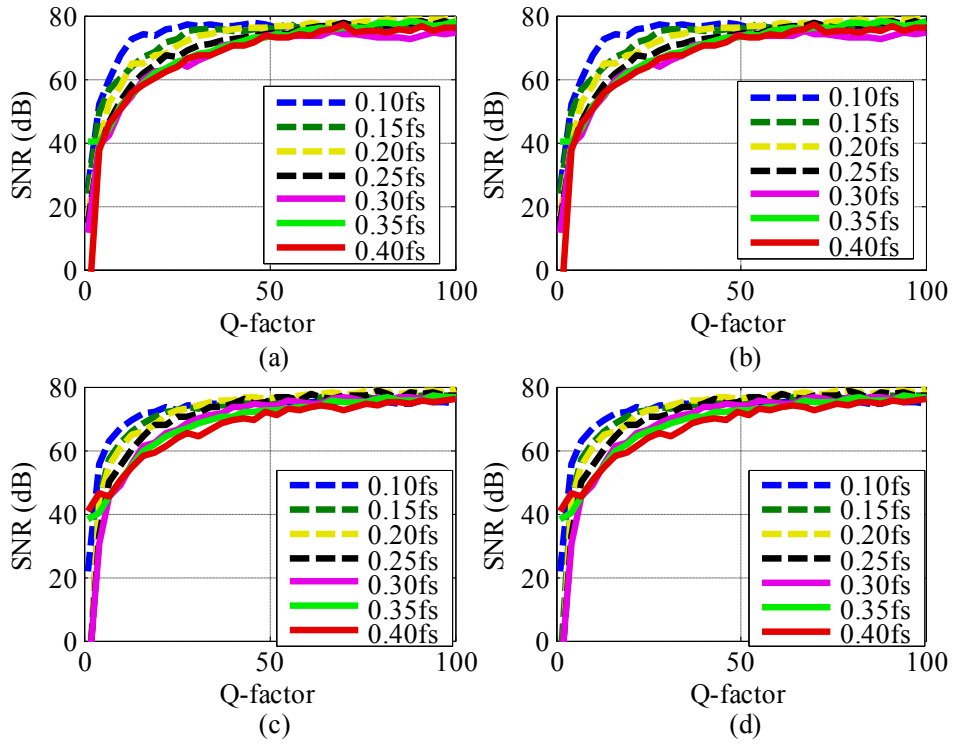


Fig. 3.15. Effect of the finite quality factor on the SNR with RZ DAC and B = 4 for: (a) BPΣΔ-A, (b) BPΣΔ-B, (c) BPΣΔ-C and (d) BPΣΔ-D.

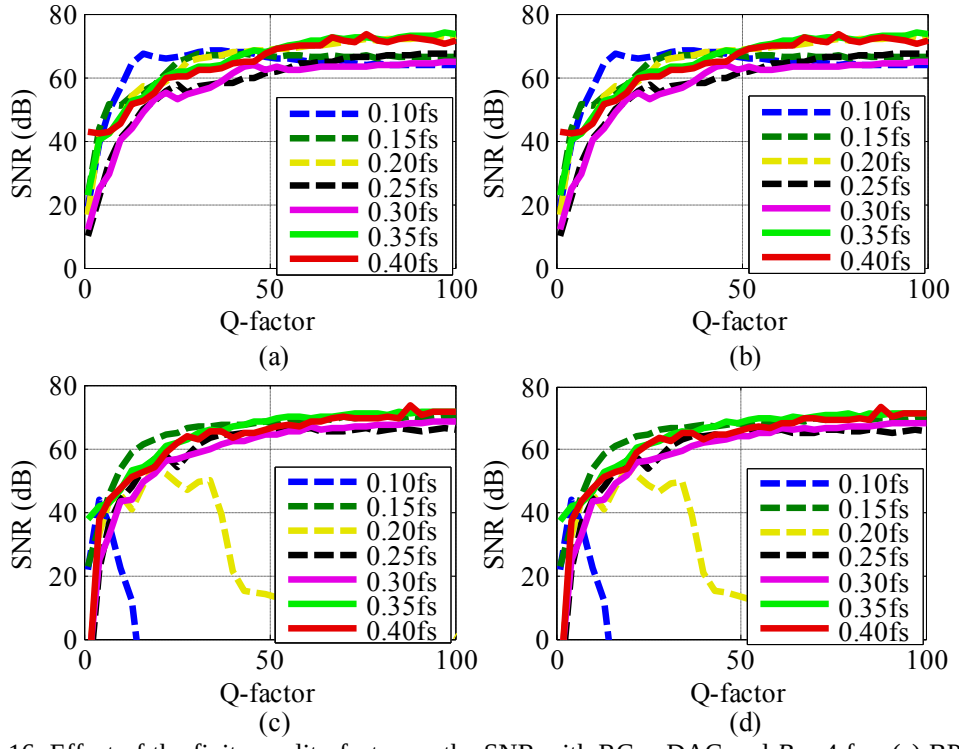


Fig. 3.16. Effect of the finite quality factor on the SNR with RCos DAC and B = 4 for: (a) BPΣΔ-A, (b) BPΣΔ-B, (c) BPΣΔ-C and (d) BPΣΔ-D.

Table 3.2. Quality factor requeriments: f_n / f_s = 0.1, 0.25, 0.4 and B = 4.

DAC	BPΣΔ-A			BPΣΔ-B		
	0.1	**0.25**	**0.4**	**0.1**	**0.25**	**0.4**
RZ	30	50	70	30	50	70
NRZ	20	60	70	20	60	70
RCos	70	70	70	40	90	90
DAC	**BPΣΔ-C**			**BPΣΔ-D**		
	0.1	**0.25**	**0.4**	**0.1**	**0.25**	**0.4**
RZ	30	50	70	30	50	70
NRZ	20	60	70	20	60	70
RCos	Unstable	70	70	Unstable	90	90

was carried out by doing 200-sample Monte Carlo simulations[2], considering that all modulator circuit elements, i.e. the transconductors and the feedback current sources, were subject to a random variation modelled by a Gaussian distribution with zero mean and different values of the standard deviation, σ. As an illustration, Fig. 3.17 shows the histogram of the SQNR for BPΣΔ-A and BPΣΔ-B, considering an NRZ DAC, B = 4 and different values of σ and f_n. Note that the performance of BPΣΔ-A is slightly worse than BPΣΔ-B, while the latter shows a similar behavior regardless the value of σ and f_n. As could be expected, BPΣΔ-A and BPΣΔ-B present a more robust behavior than both BPΣΔ-C and BPΣΔ-D, the latter being unstable in many different cases, regardless the value of σ and the type of DAC. The influence of the feedback DAC is shown in Table 3.3, where the performance of BPΣΔ-A and BPΣΔ-B is compared for B = 4 and σ = 2.5%. It can be noted that the use of a RCos DAC gives rise to a more sensitive behavior, getting worse as f_n/f_s decreases. The best results are obtained by BPΣΔ-B with NRZ DAC, keeping approximately the same SNR over the entire range of f_n.

3.3.4 Comparison in terms of power consumption

For comparison purposes, the power consumption of the modulators under study can be roughly estimated and compared, based on the values obtained for the transconductances

[2]Mismatch in the unit elements of multi-bit feedback DACs – which has a similar effect in all BP CT-ΣΔMs presented until here – was not included in the simulations in order to clearly distinguish how sensitive the different loop-filter implementations are against the technology process variations within a given notch-frequency tuning range. In practice however, linearization techniques – such as digital calibration or Dynamic Element Matching (DEM) – can be included in the feedback path of the modulators, particularly if medium-high resolutions are required.

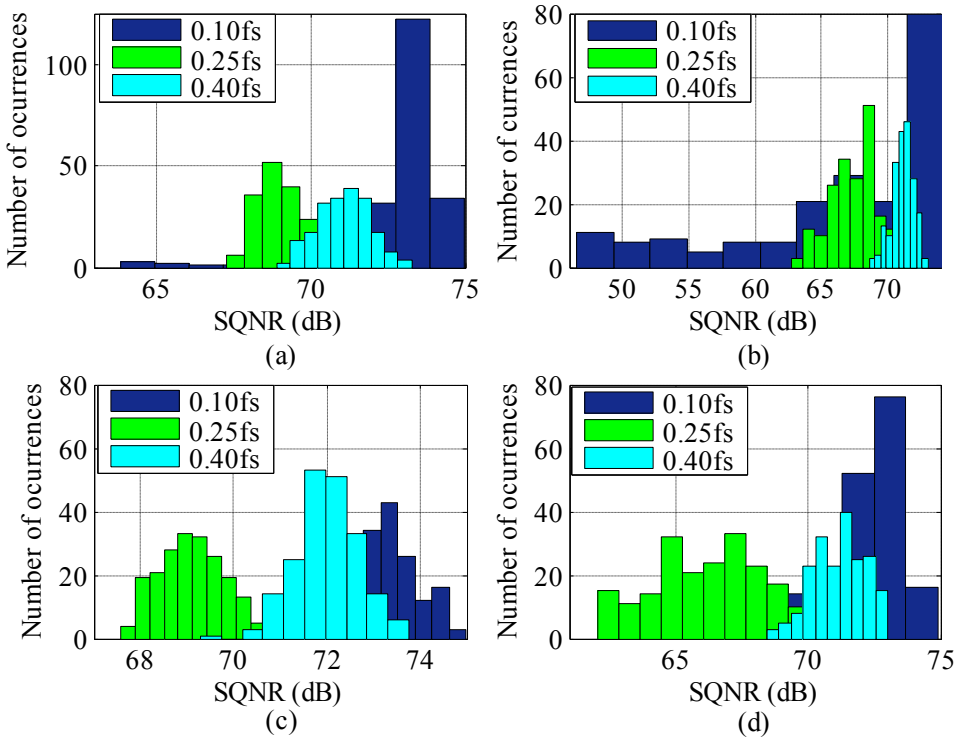


Fig. 3.17. Monte Carlo simulation with NRZ DAC and B = 4: (a) BPΣΔ-A, σ = 1%, (b) BPΣΔ-A, σ = 2.5%, (c) BPΣΔ-B, σ = 1%, (d) BPΣΔ-B, σ = 2.5%.

Table 3.3. Effect of 2.5% mismatch on the SNR(mean (dB), standard deviation (dB)), f_n / f_s = 0.1, 0.25, 0.4 and B = 4.

DAC	BPΣΔ-A			BPΣΔ-B		
	0.1	0.25	0.4	0.1	0.25	0.4
RZ	(72.1,0.8)	(69.9,1.3)	(71.3,0.8)	(72.9,1.4)	(69.7,1.4)	(70.9,0.8)
NRZ	(72.7,0.9)	(68.5,0.7)	(71.7,0.7)	(72.0,1.0)	(70.9,2.8)	(71.6,0.8)
RCos	(67.3,4.5)	(65.7,2.1)	(72.9,1.3)	(69.7,4.1)	(66.0,1.5)	(71.3,0.9)

and current sources derived from the loop-filter coefficients of each BP CT-ΣΔM topology. To this end, let us consider again the conceptual schematic of the Gm-LC BP CT-ΣΔM shown in Fig. 3.10. In order to estimate the power consumption[3], three different circuit contributions will be considered: the transconductances of the Gm-LC resonators, the current sources of the CS DAC and the adder used at the quantizer input. In order to

[3]The power consumption of the multi-bit (flash) quantizer will not be considered in the estimation of the power consumption because it would be the same in all BP CT-ΣΔMs under study, for a given sampling frequency. Note also that, as either the notch or the input frequency increases, the linearity demands for the front-end transconductor (*gm*01 in Fig. 3.10) will increase as well, thus requiring more power consumption. However, this effect would be similar in all architectures under study, and hence, it will not be taken into account in the estimation of the power consumption for the sake of simplicity.

compute the current consumed by resonators, the load capacitance of each resonator is derived as

$$C_i = \frac{1}{L_i \cdot (2\pi f_n)^2}, \tag{3.20}$$

where C_i and L_i stand respectively for the load capacitance and inductance of the i-th resonator in Fig. 3.10. This way, the value of the transconductances can be calculated as:

$$gm_{0i} = \frac{r_i}{2\pi \cdot f_n \cdot L_i}, \tag{3.21}$$

where r_i stands for the preamplification factor of the i-th resonator in each architecture under study, with i = 1, 2. For instance, $r_1 = k$ and $r_2 = 1$ in BPΣΔ-A, while $r_1 = r_2 = \sqrt{k}$ in BPΣΔ-B. Thus, the power consumption of the resonators can be computed from (3.21) for each value of f_n, assuming that the transconductance-versus-current efficiency is $gm_{0i}/I_i = 4$.

The feedback currents, I_i, provided by the CS DACs in Fig. 3.10 can be easily estimated from feedback coefficients, c_i, for each modulator architecture. In fact, the resulting I_i is calculated as $I_i = (c_i/r_i) \cdot gm_{0i} \cdot V_{FS}$, where $r_{1,2} = 1, \sqrt{k}, k$, depending on the modulator topology and $r_3 = 1$ for the adder placed at the quantizer input in all cases.

On the other hand, the third main circuit element contributing to the power consumption is the adder placed in front of the quantizer. The transconductance associated to this block, gm_{03}, is chosen to be $gm_{03} = 1/R$, so that the STF and NTF of the modulator is not affected by the value of voltage-to-current conversion resistor, R. This way, the current consumed by the adder can be estimated as $I_0 = c_0 \cdot gm_3 \cdot v_{o1}$, where v_{o1} is a full-period delayed version of the modulator output (Fig. 3.10).

Therefore, assuming a fully-differential implementation, the overall power consumption can be estimated as follows:

$$P = V_{DD} \cdot \left[2 \cdot \sum_{i=1}^{3} \left| \frac{gm_{0i}}{4} \right| + \gamma \cdot \sum_{l=1}^{P} |I_l| \right] \tag{3.22}$$

where V_{DD} is the supply voltage, and γ is a parameter which accounts for the time in which the feedback currents, I_i, are active. This depends on the DAC waveform, being γ = 1, 1⁄2 and 1/√2, for NRZ, RZ and RCos DAC, respectively. Based on these considerations, the power consumption of the modulators under study can be estimated and compared. As a case study, the following modulator parameters will be assumed: $L_1 = L_2$ = 10nH, f_s = 4GHz and a variation of f_n from $f_n = 0.05f_s$ to $f_n = 0.45f_s$. Fig. 3.18 shows the estimated power consumption versus f_n for the different modulator topologies, considering an RZ DAC (Fig. 3.18(a)), NRZ DAC (Fig. 3.18(b)) and an RCos DAC (Fig. 3.18(c)). Note that – regardless the modulator topology and the kind of DAC – the power consumption decreases with f_n, being much less efficient for $f_n < 0.25f_s$. This behavior is a direct consequence of the variation of loopfilter coefficients – and consequently gm_{0i} and I_i – with f_n, which decreases with f_n as shown in (3.21) and illustrated in Fig. 3.3(a). Comparing the modulator topologies, it can be noted from Fig. 3.18 that BPΣΔ-A and BPΣΔ-B are more efficient if $f_n \leq 0.25f_s$, while BPΣΔ-C achieves a better performance for $f_n > 0.25f_s$. However, BPΣΔ-C is worse than BPΣΔ-B in terms of I/OS and sensitivity to mismatch. Overall, taking into account the influence of nonideal effects, the DAC waveform and the estimated power consumption, BPΣΔ-B topology with NRZ DAC and multi-bit quantizer ($B \geq 2$) becomes the best solution for the target f_n tuning range.

3.3.5 Application to Software Defined Radio

As an application, this section illustrates the use of the presented *notch-aware* synthesis method to RF-to-digital conversion in SDR mobile systems. The main specifications of SDR mobile systems involves the digitization of a large number of wireless standards, whose RF signals have carrier frequencies ranging from 0.455GHz (CDMA) to 5.093GHz (WiMAX) and channel bandwidths (*Bw*) varying from 0.2MHz (GSM) to 100MHz (LTE). These requirements impose very aggressive specifications for the modulator, particularly in terms of the sampling frequencies, which can be relaxed by using *undersampling* techniques [4], [5] and [7]. This way, the selected modulator can cover the whole range of RF signals with a reconfigurable sampling frequency, *fs*, of 1, 2, 3 and 4GHz along with the widely programmable value of f_n, ranging from $0.1f_s$ to $0.4f_s$ in this case study. Taking into account these system requirements and specifications, BPΣΔ-B has been synthesized and

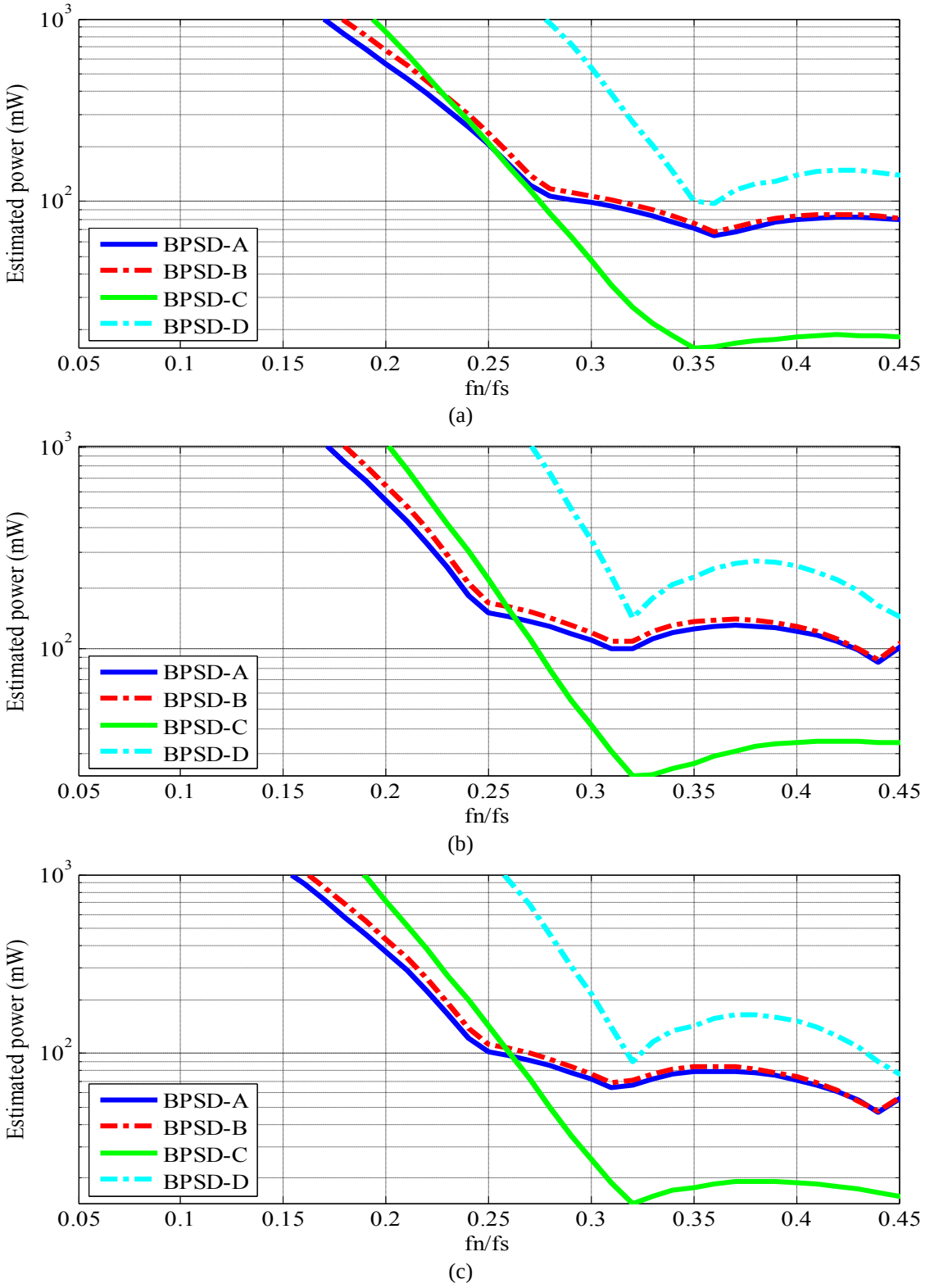


Fig. 3.18. Estimated power consumption versus f_n for: (a) RZ DAC, (b) NRZ DAC and (c) RCos DAC.

simulated considering B = 4 and an NRZ DAC. Fig. 3.19 shows the output spectra for

different standards and notch frequencies when the modulator is clocked at f_s = 3GHz. This spectra have been obtained from macromodel simulations carried out in Cadence-Spectre®, considering the electrical implementation of all modulator building blocks as well as the timing issues affecting their performance.

In addition to the circuit nonideal/nonlinear effects analyzed in previous sections, there are also other error mechanisms which – although have a similar effect on the performance of the BP CT-ΣΔMs under study – must be considered to optimize their design over the required notch-frequency tuning range. One of these limiting factors is thermal noise, which is mainly contributed by the modulator subcircuits placed at the input node, i.e. the front-end transconductance (gm_{01} in Fig. 3.10) and the feedback DAC gains (c_3 and c_4 in Fig. 3.10). Scaling and preamplifying the loop-filter coefficients affect the performance of these subcircuits in terms of noise, linearity and mismatch. As an illustration, Fig. 3.20 shows the effect of tuning the preamplification factor, $k(v)$, over the Signal-to-Thermal-Noise Ratio (STHNR) and the SQNR of BPΣΔ-B, when clocked at f_s = 3GHz. Different standards are considered, namely: CDMA, LTE 700 and GSM 900, which correspond respectively to a relative notch frequency variation of f_n / f_s = 0.15, 0.25 and 0.3157. Transient simulations were carried out in Cadence-Spectre considering macromodels that take into account the main circuit error mechanisms, in order to compute the SQNR, while

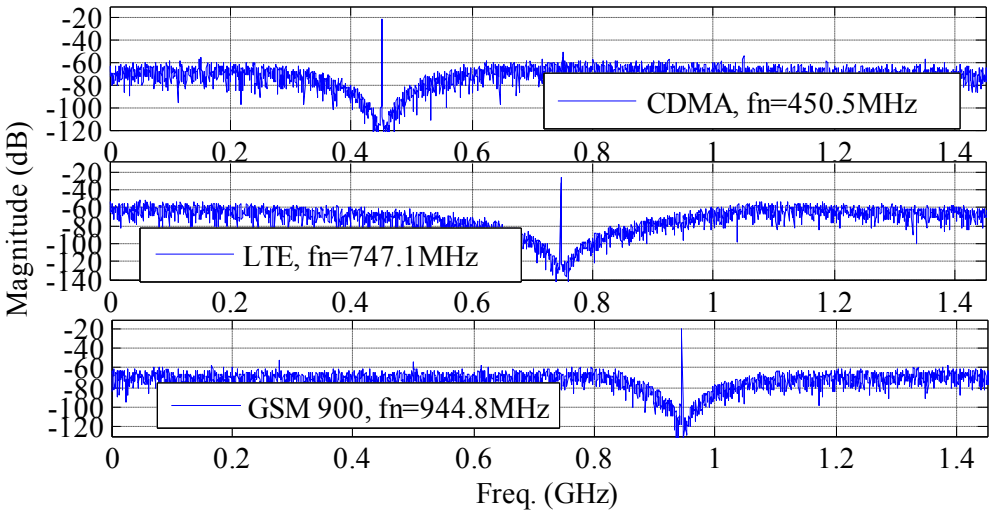


Fig. 3.19. Output spectra computed from Cadence-Spectre® macromodel simulations of BPΣΔ-B with NRZ DAC, B = 4 and f_s = 3GHz.

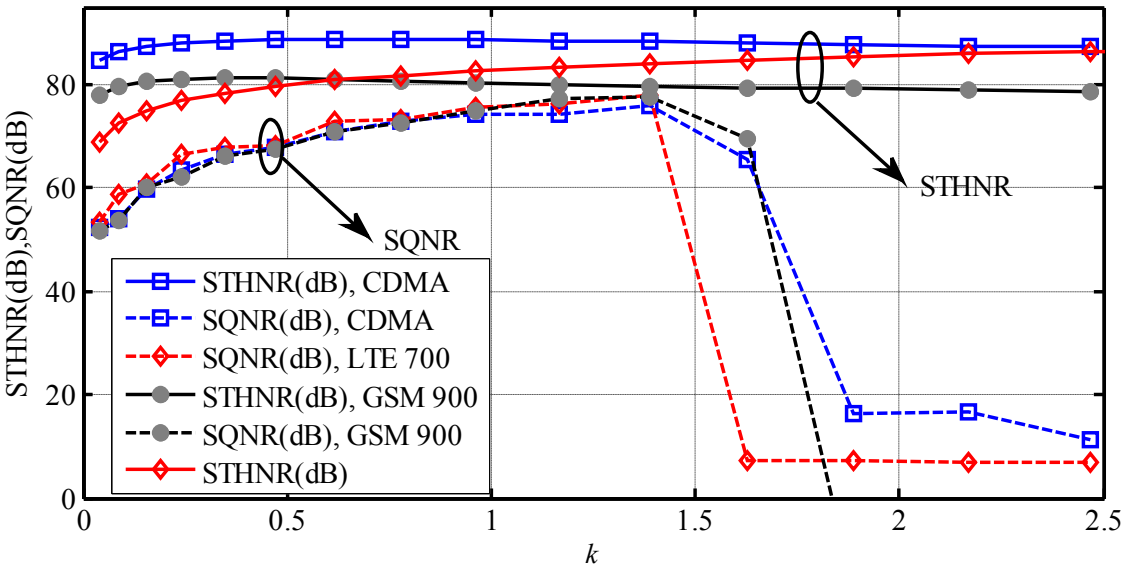


Fig. 3.20. Effect of tuning *k* on SQNR and STHNR for different standards.

noise estimations were used to obtain the STHNR. It can be noted how there is an optimum value of the scaling coefficient, *k*, which maximizes the SQNR, while the STHNR does not change significantly within the tuning range in which *k* is varied. Clock-jitter error is also a limiting factor affecting the performance of BP CT-ΣΔMs, being more and more critical as the sampling frequency increases. Although the degradation caused by the clock-jitter error will essentially depend on the feedback DAC waveform, the influence of the notch-frequency variation for a given sampling frequency – main objective of this thesis – will not have a significant impact on the SNR. This is illustrated in Fig. 3.21, where the SNR is represented versus the clock-jitter uncertainty considering a macromodel implementation of the BPΣΔ-B architecture with NRZ DAC, $B = 4$ and $f_s = 3$GHz, and the same standards and notch frequencies used in Fig. 3.20. Finally, to illustrate the flexibility of the presented approach, Fig. 3.22 shows the simulated SNR versus input signal when clocked at f_s = 2GHz for several standards, namely: CDMA-450, LTE-700, and for WLAN 802.11Y, the later operating in undersampling mode. Note that for LTE-700 standard, the sampling frequency is less than $4f_n$ but without entering in the undersampling mode. Thus, an additional advantage of the presented methodology, and the resulted modulators, is that they allow reducing the sampling frequency in BP CT-ΣΔMs.

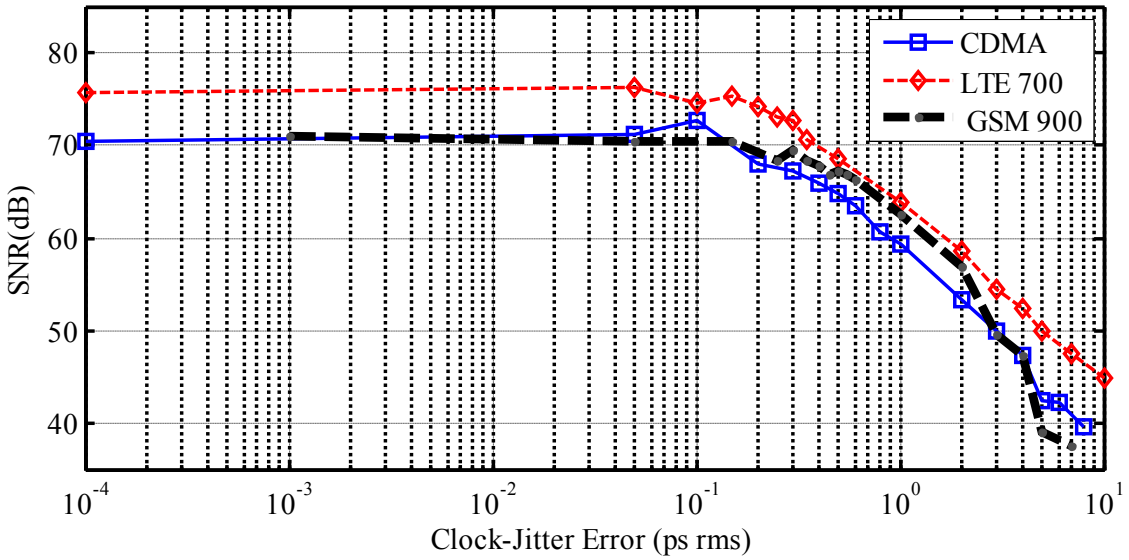


Fig. 3.21. SNR vs. clock-jitter error for different standards.

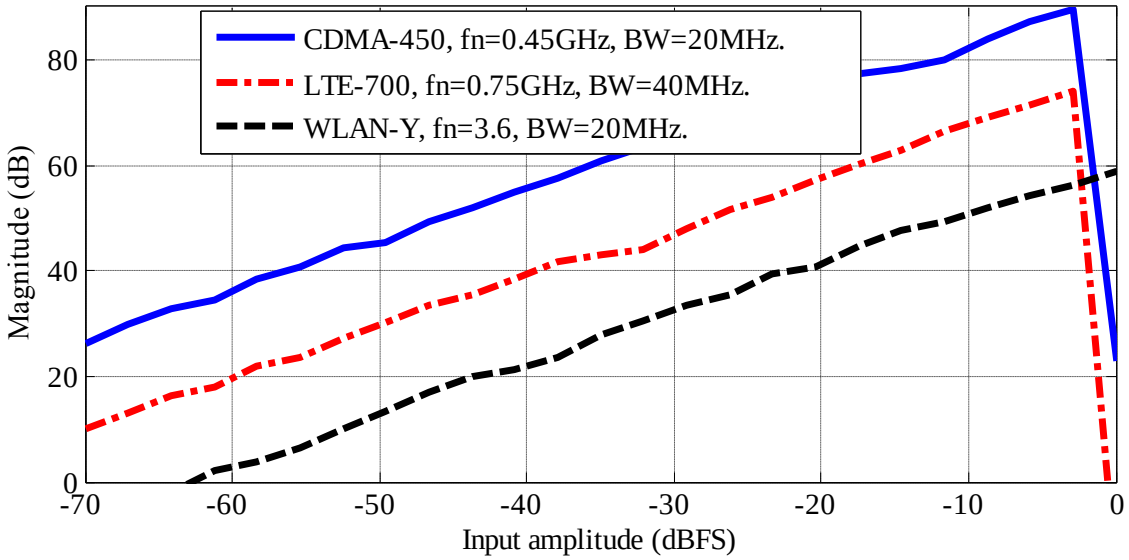


Fig. 3.22. SNR vs. input amplitude for different standards and f_s = 2GHz.

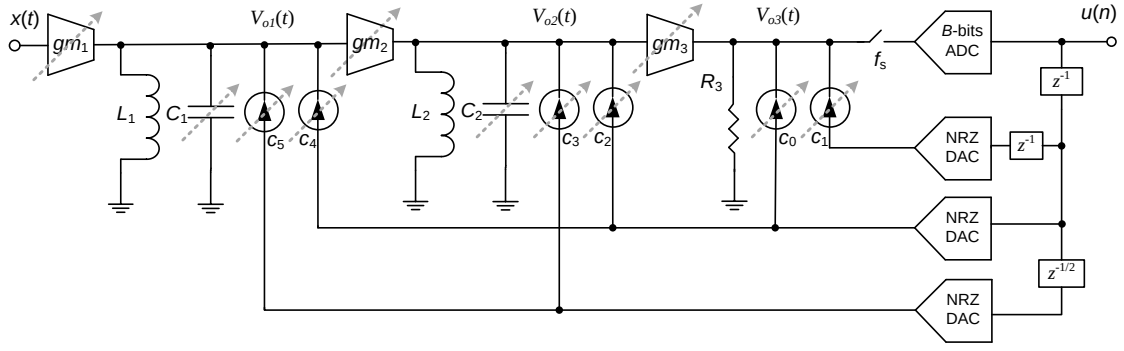
3.4 Passive modulators

In section 3.3, it could be seen that most of the power consumption is demanded by the resonator circuits used to build the modulator loop filter, which are implemented using Gm-

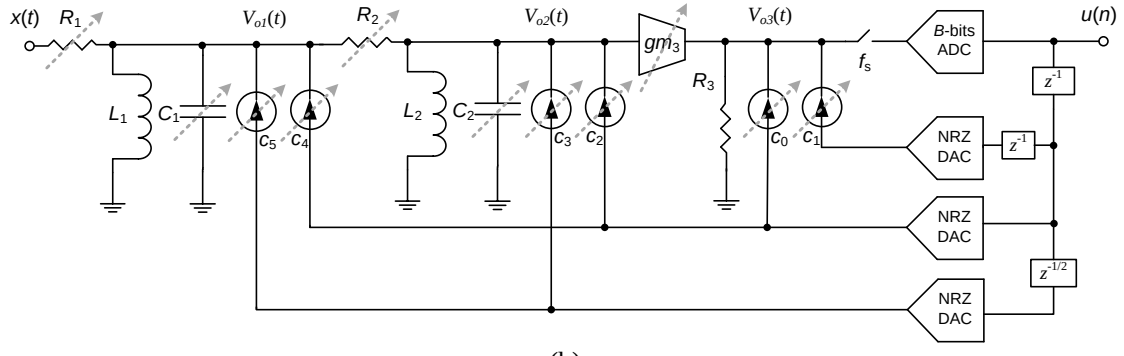
LC sections. An alternative approach to reduce the power dissipation consists of using passive loop-filters [9]–[15].

Fig. 3.23 shows two alternative conceptual circuit implementations for the BPΣΔ-B topology with NRZ DAC, considering active (Fig. 3.23(a)) and passive resonators (Fig. 3.23(b)).

Although ideally, both BP CT-ΣMs in Fig. 23 could achieve similar performance, the passive modulator (Fig. 3.23(b)) cannot be implemented in practice due to its unfeasible high loop-filter coefficients obtained in the synthesis process. This is illustrated in Fig. 3.24, where c_i are plotted versus f_n / f_s for both modulators. Note that, if $f_n / f_s < 0.25$, very high values of c_i are obtained, thus leading to unfeasible output swings and RC circuit elements [9] in the passive BP CT-ΣM.



(a)



(b)

Fig. 3.23. Conceptual circuit implementation of the BP CT-ΣΔM in Fig. 3.8(a) considering: (a) Active loop-filter. (b) Passive loop-filter. (Dashed arrows indicate that the circuit elements are programmable.)

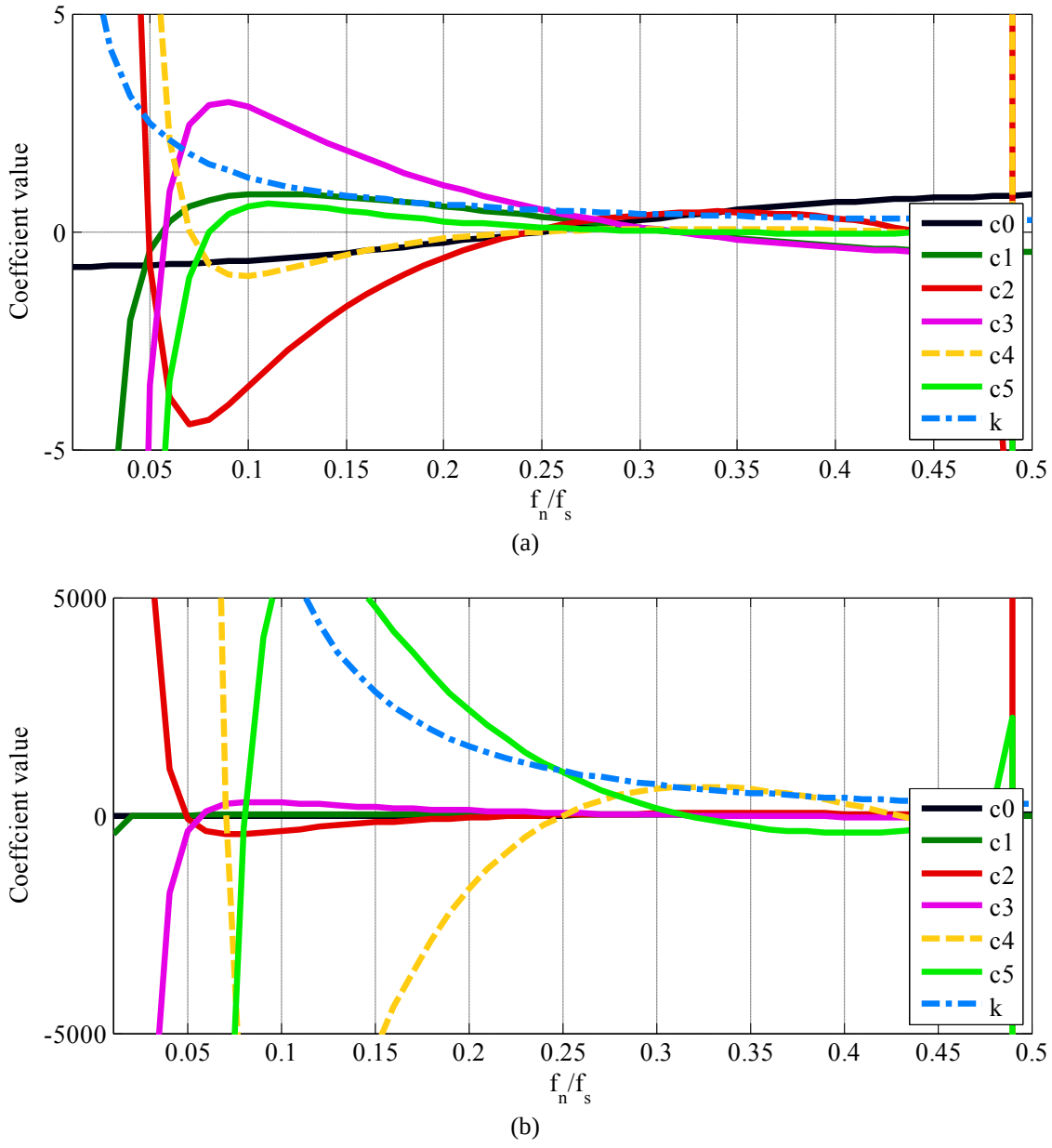
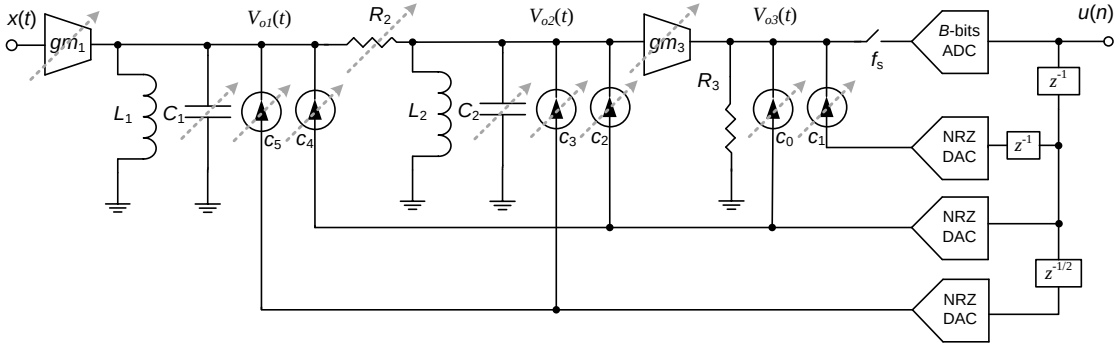


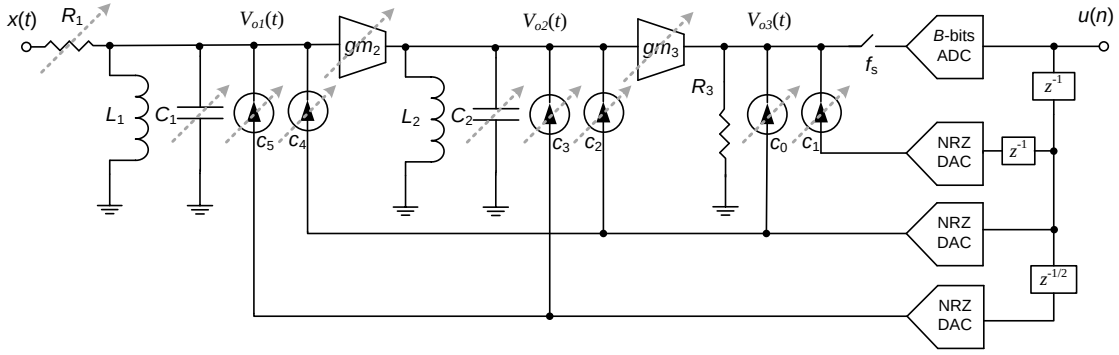
Fig. 3.24. Loop-filter coefficients, c_i, versus $f_n = f_s$ for: (a) the active modulator and (b) the passive versions of the BP CT-ΣΔM shown in Fig. 3.23.

3.4.1 Proposed Hybrid Active/Passive BP ΣΔMs

Fig. 3.25 shows the conceptual schematics of the proposed hybrid active/passive BP CT-ΣMs, considering that: the frontend resonator is active and the second resonator is passive (denoted as hybrid-1 in Fig. 3.25(a)); the front-end resonator is passive and the second resonator is active (denoted as hybrid-2 in Fig. 3.25(b)); both resonators are passive and the



(a)



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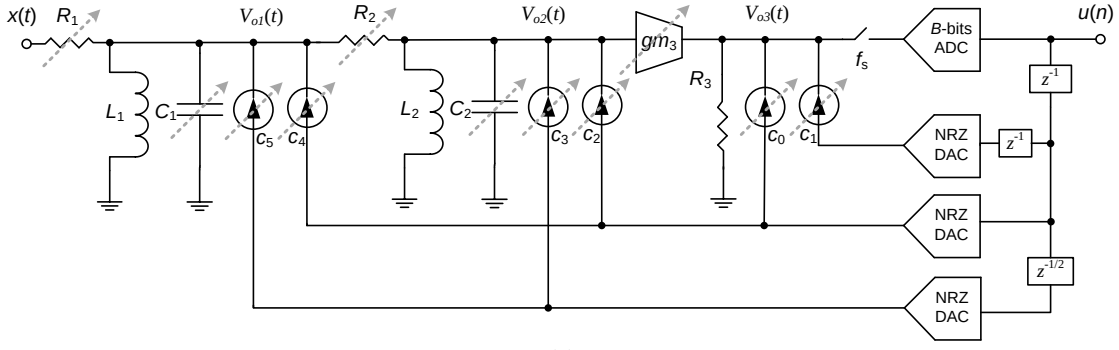
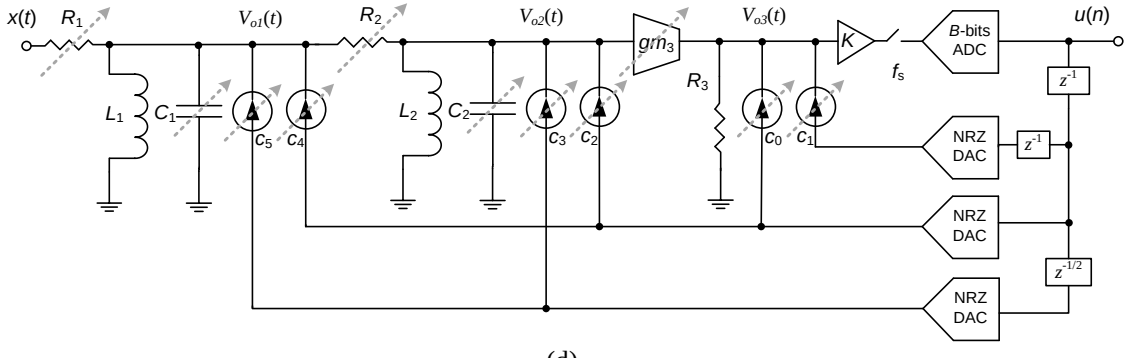


(c)



(d)

Fig. 3.25. Conceptual schematics of the proposed BP CT-ΣΔMs considering: (a) An active front-end resonator and a passive second resonator. (b) A passive front-end resonator and an active second resonator. (c) Both passive resonators with active gain at the summation. (d) A fully passive feed-forward filter.

adder is active (denoted as passive-1 in Fig. 25(c)); the whole filter is passive (denoted as passive-2 in Fig. 3.25(d)). Note that the latter can be considered as a fully-passive implementation, since it does not require any gain in the feed-forward path, although the quantizer is indeed an active circuit that provides the required gain.

The values of c_i coefficients in Fig. 3.25(b)-(d) – not shown for the sake of simplicity – are of the same order of magnitude as those obtained for the active BP CT-ΣM shown in Fig. 3.24(a). However, the BP CT-ΣM in Fig. 3.25(a) yield to unpractical output swings in the same way as the passive implementation of Fig. 3.24(b). This is due to the fact that the gain of the front-end resonator becomes larger as f_n approaches $0.1f_s$. This problem can be solved if such a gain is distributed in the remaining blocks in the modulator chain. This strategy is followed in the modulators of Fig. 3.25(b)-(d), which feature an improved output-swing performance as illustrated in Fig. 3.26, that represents the histograms of the resonators outputs for the BP CT-ΣM in Fig. 3.25(c) with a single-bit (B = 1) quantizer. These output swings can be further reduced if B > 1. All BP CT-ΣMs in Fig. 3.25 can be tuned to digitize bandpass signals placed at f_n within the range $0.1 < f_n=f_s < 0.4$. This is illustrated in Fig. 3.27, that represents the output spectra (Fig. 27(a)) and the Signal-to-Noise-Ratio (SNR) versus input amplitude (Fig. 3.27(b)) for different values of f_n,

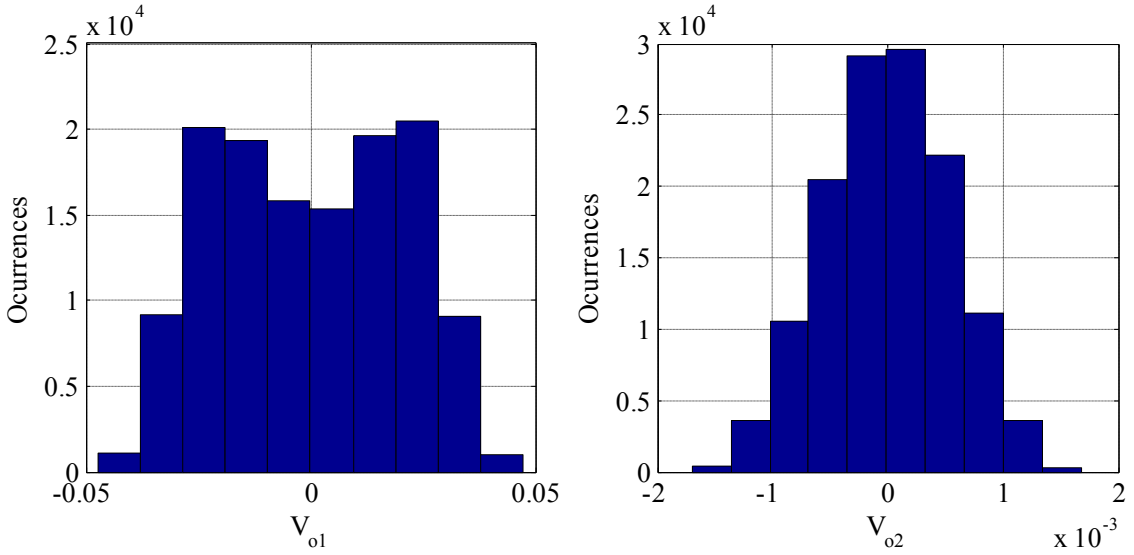


Fig. 3.26. Histograms of the resonator outputs considering B = 1 and $f_n = f_s / 4$ for the BP CT-ΣΔM shown in Fig. 3.25(c): (a) Front-end resonator output, vo1. (b) Back-end resonator output, vo2. (1-V full-scale reference voltage).

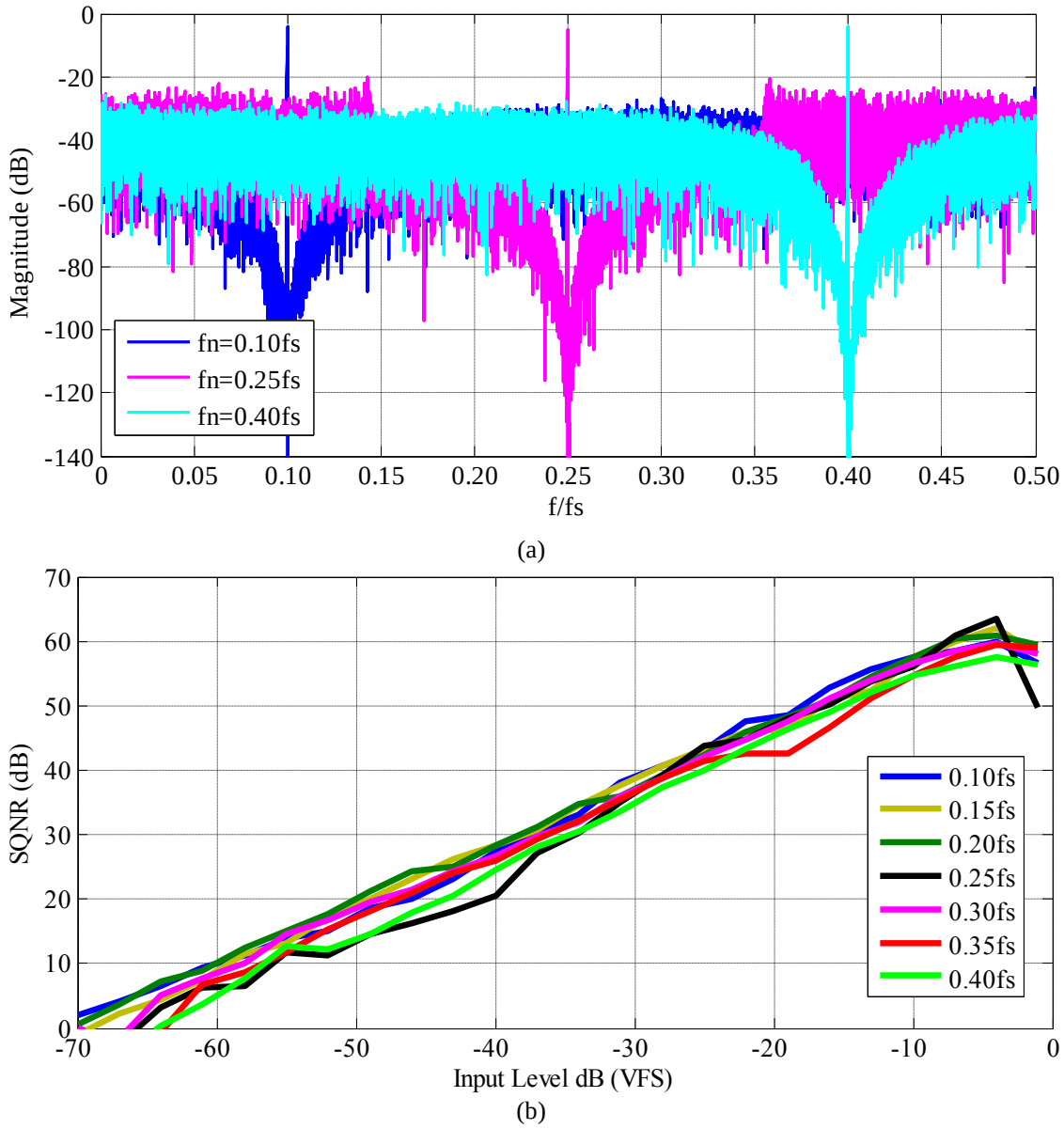


Fig. 3.27. System-level simulations of the BP CT-ΣΔM in Fig. 25(d) for different values of f_n / f_s : (a) Output spectra and (b) SNR versus input amplitude.

considering f_s = 4GHz, B = 1 and an OverSampling Ratio (OSR)= 50. These figures were extracted from simulations of the BP CT-ΣM in Fig. 3.25(d).

3.4.2 Quality factor of integrated inductors

Integrated inductors considered in the circuit implementations shown in Fig. 3.25, have a number of parasitics which cause these inductors to behave as RLC circuits in practice [7], [16], [17]. In order to take this effect into account, the equivalent circuit shown in Fig. 3.28

is used to model passive resonators. The model includes a parasitic resistance, R_{ind}, which is connected in series with the integrated inductor. Based on this model, the resonator transfer function can be written as:

$$R_Q(s) = \frac{R_{ind} + Ls}{RLCs^2 + (L + CRR_{ind})s + R + R_{ind}}, \tag{3.23}$$

which leads to an effective quality factor, Q_{eff}, given by:

$$Q_{eff} = \frac{Q \cdot Q_{ind}}{Q + Q_{ind}}, \tag{3.24}$$

where $Q_{\text{ind}} \equiv \omega L/R_{\text{ind}}$, stands for the finite quality factor of the inductor, and $Q = \omega RC$, is the quality factor of the resonator. In practice, $Q_{\text{ind}} << Q$, and hence $Q_{\text{eff}} \approx Q_{\text{ind}}$. Fig. 3.29 shows the impact of Q_{ind} on the SNR for the BP CT-ΣMs under study, considering B = 1, $f_n = f_s/4$ and an OSR as a variable parameter. Note that all modulators achieve approximately an ideal SNR for OSR ≤ 50 provided that Q_{ind} is within the range of (25, 30). However, larger values of Q_{ind} are required to achieve larger SNRs, becoming unfeasible in some cases. Thus, as a consequence of limited values of Q_{ind} in standard CMOS, the proposed modulators become more effective for low-OSR wideband applications.

To conclude the nonideal analysis, let us consider that the loop-filter coefficients of the BP CT-ΣMs under study deviate from their ideal values as a consequence of technology process variations. The computation of these variations was carried out by doing 200-sample Monte Carlo simulations, considering that all modulator circuit elements were

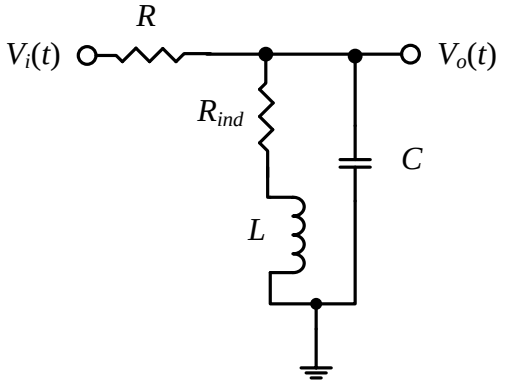


Fig. 3.28. Equivalent circuit used to model a passive resonator with a parasitic series resistance, R_{ind}.

subject to a random variation modeled by a Gaussian distribution with zero mean and different values of the standard deviation, σ.

Fig. 3.30 shows the histograms of the SNR for all the proposed BP CT-ΣMs for σ = 2%, B = 1, OSR=50 and different values of f_n / f_s. Note that the presented modulators are in general quite robust against circuit element tolerances, getting worst-case variations of 4-5dB around nominal values, and becoming more sensitive as f_n / f_s is reduced – as also happens to active implementations (see section 3.3).

3.5 Conclusions

This chapter has presented a *notch-aware* synthesis methodology for the design of LC-based BP CT-ΣΔMs with a widely programmable notch frequency. The proposed method allows us to extend the tuning range of the notch frequency from 0.1*fs* to 0.4*fs*, and it has been applied to the system-level design of several fourth-order BP CT-ΣΔMs with different types of FIR-based DACs, including RZ, NRZ and RCos waveforms.

All the synthesized widely tunable LC-based BP CT-ΣΔMs have been analyzed in terms of their robustness to the main circuit error mechanisms, including input/output swings in the resonators, finite quality factor of inductors, thermal noise, clock jitter and mismatch in the feedback elements.

The power consumption of the presented widely tunable LC-based BP CT-ΣΔMs has been estimated on the base of their main circuit contributions: transconductors implementing the loop-filter resonators and current sources implementing the feedback DAC.

On the base of its robustness against main circuit error mechanism and the estimated power consumption, it has been determined that the widely tunable LC-based BP CT-referred to as BPΣΔ-B topology with NRZ DAC and multi-bit quantizer ($B \geq 2$) is the best solution for the target f_n tuning range.

In order to reduce the power consumption in the BPΣΔ-B topology with NRZ DAC, it has been discussed the use of passive circuits for the implementation of the modulator loop-filter. As a result, several modulator topologies, which combine both active and passive resonators, have been proposed.

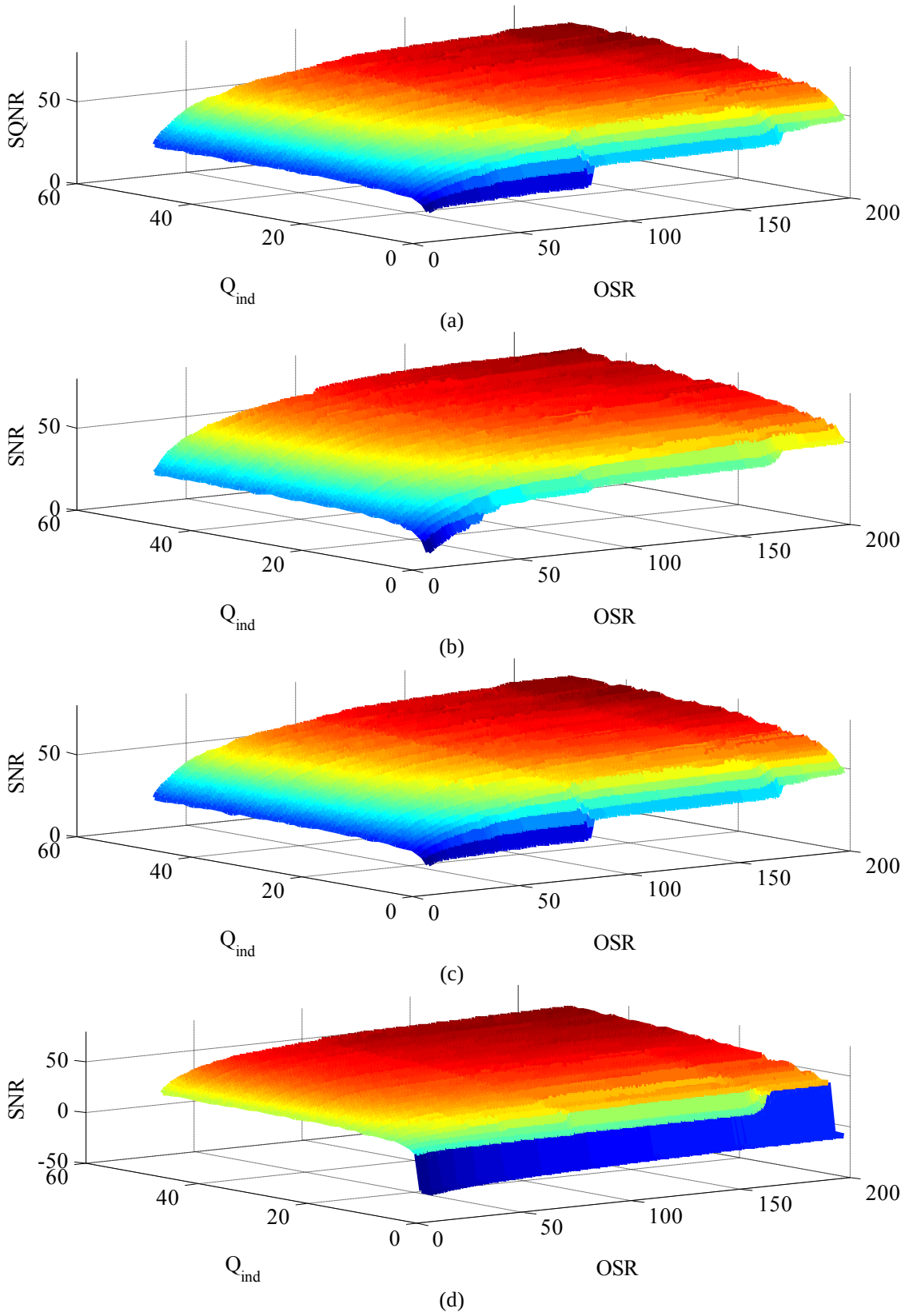


Fig. 3.29. Impact of Q_{ind} on the SNR for the BP CT-ΣΔMs of Fig. 25: (a) Hybrid-1, (b) Hybrid-2, (b) Passive-1, (c) Passive-2.

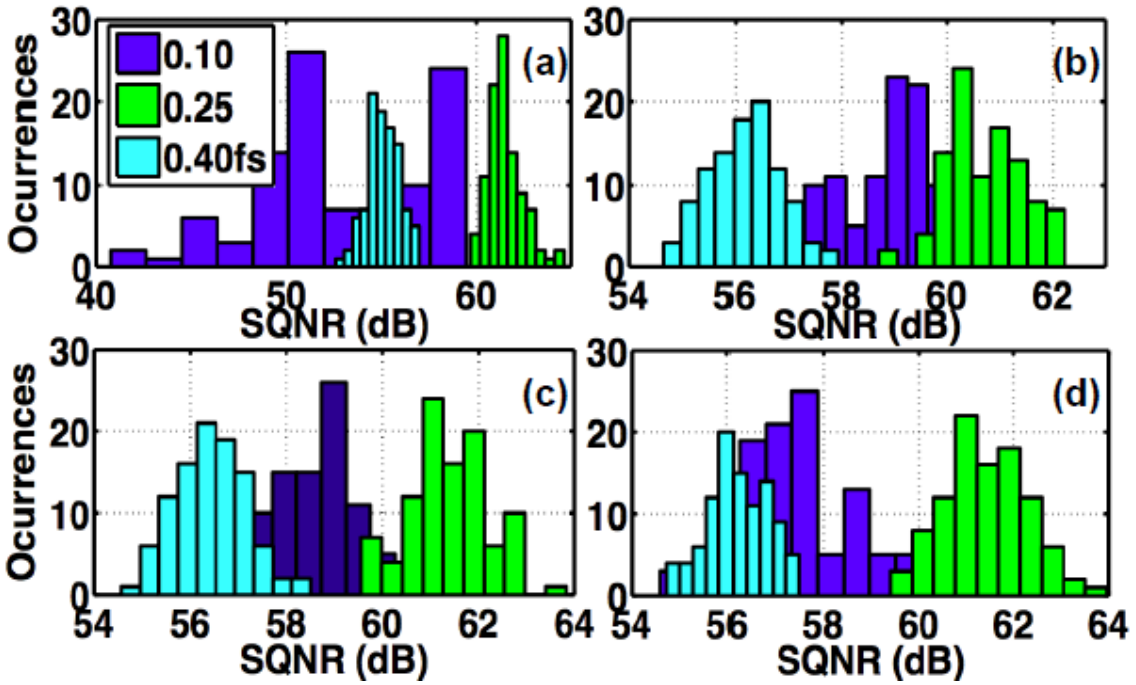


Fig. 3.30. Monte Carlo simulation of the BP CT-ΣΔMs under study with σ = 2%, OSR=50: (a) Hybrid-1, (b) Hybrid-2, (c) Passive-1, (d) Passive-2.

The hybrid and passive modulator topologies were also analyzed in terms of most critical error mechanisms, demonstrating that hybrid active/passive circuit techniques can be a feasible alternative for the implementation of RF-to-digital converters.

Time-domain simulations considering system-level behavioral models in MATLAB and circuit macromodels in Cadence-Spectre have validated the presented approach, demonstrating the effectiveness of the proposed methodology for the efficient implementation of next-generation RF-to-digital BP-ΣΔMs.

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Chapter 4

Power and Area Efficient Comb-based Decimators

This chapter introduces a two-stage comb-based decimation structure, where the first stage is in a non-recursive form and the second stage is in a recursive form (CIC). A design methodology, which is based on power and area estimations, is presented in order to choose the best values for the first and second decimation factors, M_1 and M_2. The proposed structure simultaneously shows the power efficiency of non-recursive comb and the area efficiency of CIC, when it is designed for high values of the decimation factor that are power of two. Similarly, the presented two-stage structure can be used for decimation factors that are even numbers, featuring less power consumption and similar area requirements than the equivalent CIC. Furthermore, the two-stage structure is easily modified to cope with decimation factors that are power of three and integer multiples of three. In terms of frequency response, modified structures are presented, which improve the folding band attenuations and correct the passband droop without severally penalizing the power and area efficiency. These modifications are based on the use of simple filters working at a low sampling rate. VHDL implementation results, in both a CMOS technology and an FPGA, are shown to validate the proposed approach.

4.1 Power and area estimation of comb decimators

The dynamic power consumption of a decimation filter can be estimated by the number of required full adders (*FA*) and registers (*FF*) as follows [1]:

$$P = \gamma(FA + FF)B_{out}, \tag{4.1}$$

where γ is the relative frequency of the filter compared with the input frequency, and B_{out} is the word length increase to avoid overflow. The word length increase in comb-based decimators can be calculated as [2]:

$$B_{out} = B_{in} + K \times log_2(M), \tag{4.2}$$

where *K* is the number of cascaded filters.

The used area *A* can be modeled in a similar fashion, since it also depends on the number of adders and registers, giving:

$$A = (FA + FF)B_{out}. \tag{4.3}$$

The information presented in this chapter was mainly extracted from [8]-[11].

Using (4.1) and (4.3), the power and area estimations for the CIC decimator illustrated in Chapter 1, Fig. 1.12(a) are:

$$P_{CIC} = (FA_I + FF_I)B_{out} + \frac{(FA_C + FF_C)B_{out}}{M}, \tag{4.4}$$

$$A_{CIC} = [(FA_I + FF_I) + (FA_C + FF_C)]B_{out}, \tag{4.5}$$

where the subscripts *I* and *C* are for integrator and comb sections, respectively.

Similarly, the power and area estimations for the non-recursive comb decimator with a decimation factor that is a power of two (Cahpter 1, Fig. 1.12(b)), i.e. $M = 2^P$, are given by:

$$P_{Comb} = \sum_{i=0}^{P-1} \frac{(FA + FF)[B_{in} + log_2(2)K \times (i+1)]}{2^i}, \tag{4.6}$$

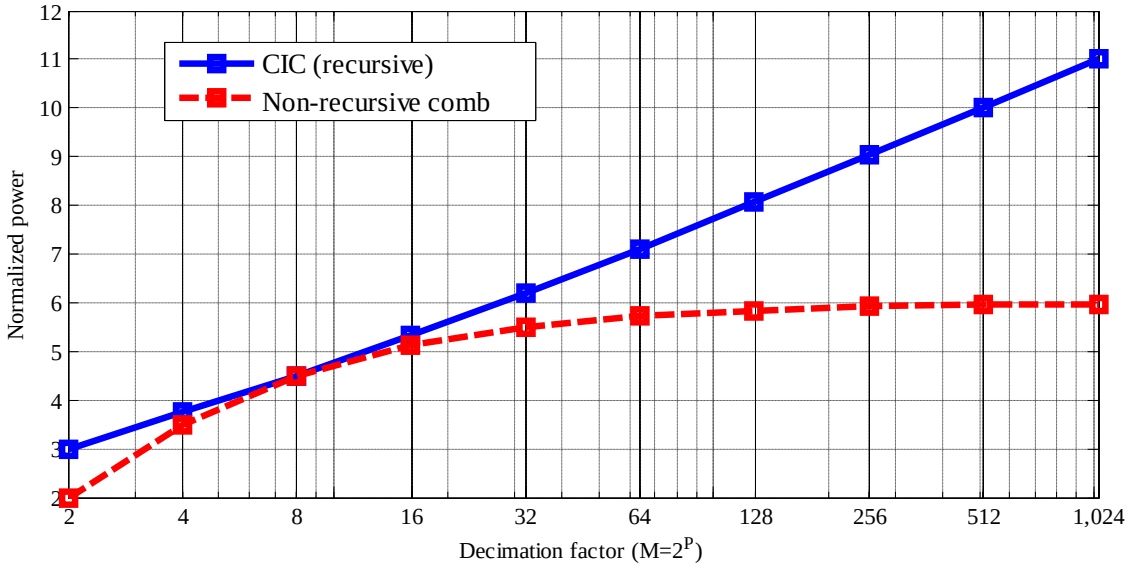
$$A_{Comb} = \sum_{i=0}^{P-1} (FA + FF)[B_{in} + log_2(2)K \times (i+1)]. \tag{4.7}$$

As an illustration, Figs. 4.2(a) and 4.2(b) present the estimated power consumption and the required area for CIC and non-recursive comb filters, respectively, assuming one bit at the input. The values are normalized by $(FA + FF)K^2$.

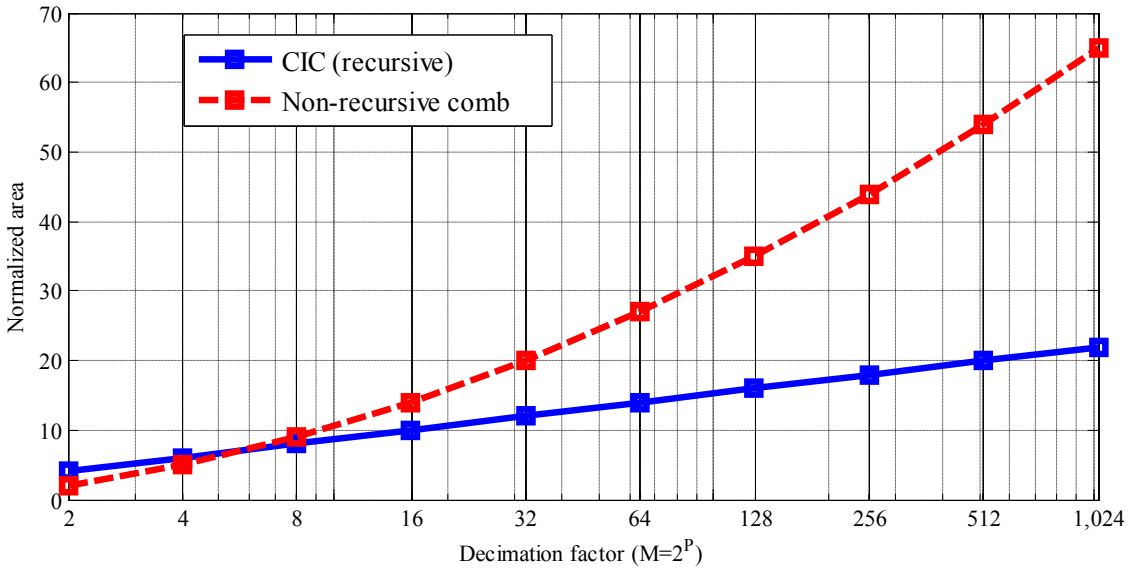
From Fig. 4.1(a) it can be seen that, as *M* increases, the power consumption for CIC grows logarithmically while for non-recursive comb the growth is asymptotic due to the frequency reduction through each stage. As a result, the power consumption for a CIC filter is higher than that for a non-recursive comb filter, especially for high decimation factors. On the other hand, from Fig. 4.1(b) it can be seen that the required area of CIC filter increases logarithmically while in non-recursive comb the growth is approximately quadratic. As a result, the used area for CIC filter is generally less than that for the corresponding non-recursive comb, especially for high decimation factors.

4.2 Proposed two-stage structure

A more efficient decimation structure is presented in this thesis, which balances both, power and area. The decimator consists of two stages. The first stage is implemented as a



(a)



(b)

Fig. 4.1 Estimated (a) Power and (a) area for CIC and non-recursive comb, $M = 2^P$.

non-recursive comb structure and the second stage with the CIC structure. Fig. 4.2 shows the block diagram of the proposed structure. The transfer function, referenced to high sampling rate, is given by:

$$H_P(z) = \left[\left(\prod_{i=0}^{log_2(M_1)-1} \frac{1}{2}\left(1+z^{2^i}\right)\right)\left(\frac{1}{M_2}\frac{1-z^{-M_2}}{1-z^{-1}}\right)\right]^K, \qquad (4.8)$$

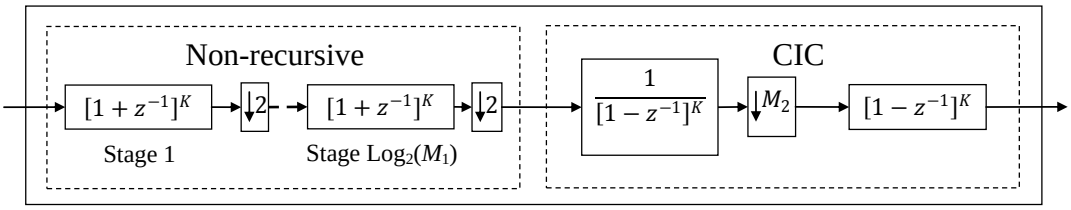


Fig. 4.2 Proposed structure.

where M_1 and M_2 are the decimation factors of the first and second stages, respectively, and K is the number of cascaded non-recursive comb and CIC filters.

Due to the world length growth implied by the first non-recursive comb stage, the input for the second, CIC stage, has a word length given by

$$B_{in,CIC} = B_{in} + \sum_{i=0}^{log_2(M_1)-1} [log_2(2)K * (i+1)]. \tag{4.9}$$

Thus, placing (4.9) into (4.2), and substituting (4.2) in (4.4), from (4.6) and (4.4), we get the power estimation for H_p(z) given by:

$$\begin{aligned} P_P = & \sum_{i=0}^{log_2(M_1)-1} \frac{(FA+FF)[B_{in} + log_2(2)K \times (i+1)]}{2^i} \\ & + \frac{(FA_I + FF_I)\left(B_{in,CIC} + K \times log_2(M_2)\right)}{M_1} \\ & + \frac{(FA_C + FF_C)(B_{in,CIC} + K \times log_2(M_2))}{M_1 M_2} \end{aligned} . \tag{4.10}$$

A similar approach is used to obtain the area estimation A_p of $H_p(z)$, as follows:

$$\begin{aligned} A_p = & \sum_{i=0}^{log_2(M_1)-1} (FA+FF)[B_{in} + log_2(2)K \times (i+1)] \\ & + [(FA_I + FF_I) + (FA_C + FF_C)]\left(B_{in,CIC} + log_2(M_2)K\right) \end{aligned} . \tag{4.11}$$

4.3 Proposed structure for high power of two decimation factors

Note that, in (4.10) and (4.11), the values of M_1 and M_2 are not specified. Considering that $M = M_1M_2 = 2^p$, it is possible to find P-1 different combinations for M_1M_2, where $M_1 = 2^k$

and $M_2 = 2^{P-k}$, with $k = 1, 2\ldots, (P\text{-}1)$. In order to find the optimum value for M_1, we propose choosing the value of M_1 which allows us having an estimated power consumption as close as possible to the power consumption of a non-recursive comb structure, but at the same time, an estimated area as close as possible to the area required for a CIC structure.

To illustrate this process, let us consider $M = 512 = 2^P$, so that M_1 can take the values of 2, 4, 16, 32, 64, 128 and 256. In this case, the normalized power consumption of the proposed structure for those values of M_1 is plotted in Fig. 4.3(a). The referent normalized values of power consumption for non-recursive comb and CIC structures, both with M=512 (see Fig. 4.1(a)), are also presented. From Fig. 4.3(a), it can be seen that for $M_1 \geq 4$ the proposed structure (4.8) has the same power consumption as that of non-recursive comb structure. In fact, the power consumption in the proposed structure is slightly lower than that in non-recursive comb when $8 \leq M_1 \leq 32$.

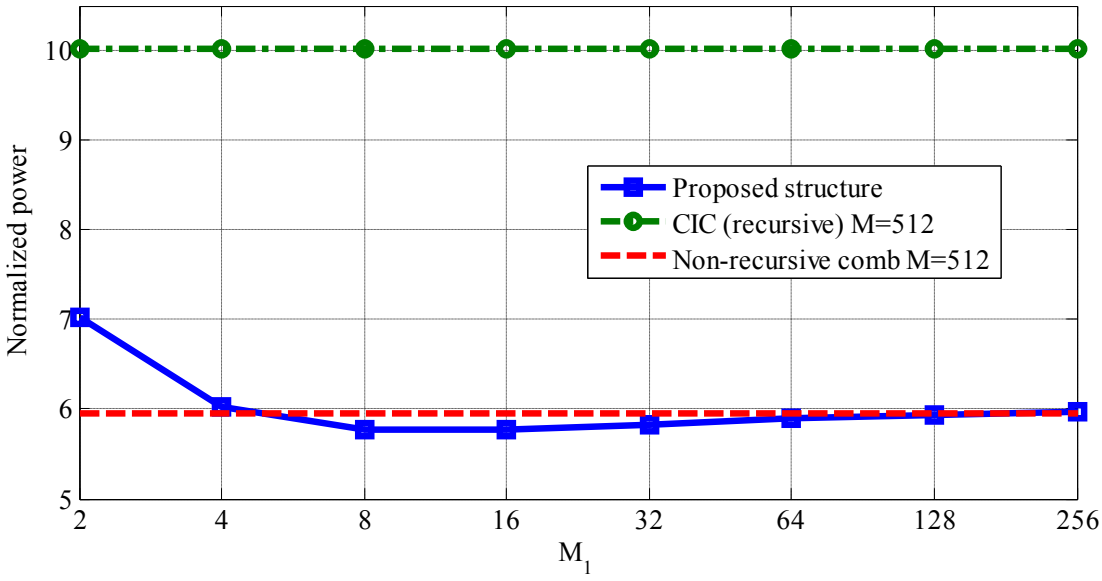
Similarly, the used area of the proposed structure for the eight different values of M_1 is shown in Fig. 4.3(b). The referent normalized values of area for non-recursive comb and CIC structures, both for M=512 (see Fig. 4.1(b)), are also shown. From Fig. 4.3(b) it can be seen that the used area increases in the same fashion as in non-recursive comb filter, (see Fig. 4.1(b)). Thus, to obtain a low area in the proposed structure, similar to that in the CIC structure, low values of M_1 must be used.

Observing Figs. 4.3 (a)-(b), it can be concluded that the optimal value for M_1 is 4; thus, M_2 = 128. In this way, the proposed structure exhibits the low power characteristic as a non-recursive comb structure and a low area as the CIC structure.

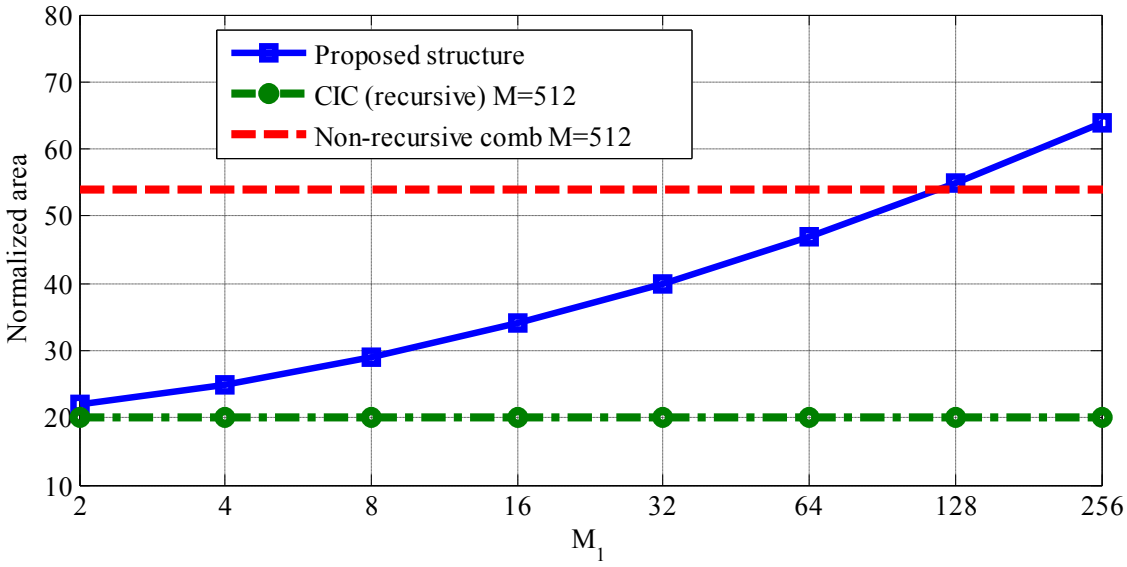
Following a similar procedure, the optimal value of M_1 can be found for higher decimation factors M. For example, the optimal values of M_1 are 8 and 16 for M = 1024, 2048 and M = 4096, 8192, respectively.

4.3.1 Alias rejection improvement

Although the proposed structure of Fig. 4.2 is efficient in terms of power an area, its magnitude response exhibits low attenuation in the folding bands and passband droop like the simple comb decimators. In order to improve the alias rejection of the proposed



(a)



(b)

Fig. 4.3 Estimated (a) Power and (b) area for the proposed structure along with CIC and non-recursive comb for *M*=512.

structure in Fig. 4.2, when it is configured for decimation factors that are power of two, we have adopted the idea from [3], where the expanded cosine filter

$$H_{cos}(z) = 0.5\left(1 + z^{-M/2}\right), \tag{4.12}$$

is introduced in a non-recursive structure to improve the aliasing rejection in the first folding band. Fig. 4.4 shows the modified proposed structure, which has K_1 cascaded cosine filters working at a lower sampling rate.

It is useful to remember from that the worst case aliasing of the comb filter is at the frequency [3]:

$$\omega_A = \frac{2\pi}{M} - \frac{\pi}{RM}, \tag{4.13}$$

where R is the decimation factor which follows the comb decimation stage. Without loss of generality, here, it will be considered $R = 2$.

By placing $z = e^{-j\omega}$ in (4.12) and evaluating at the frequency of (4.13), it can be demonstrated that the worst case attenuation (WCA) improvement for each added cosine filter is given as:

$$A = 20 * \log_{10}(\cos(3\pi/8)) = -8.34dB. \tag{4.14}$$

Thus, denoting the desired WCA as A_M in the modified proposed structure, the number of cascaded cosine filters can be obtained as:

$$K_1 = \left\lceil \frac{A_M - A_P}{8.34} \right\rceil, \tag{4.15}$$

where $\lceil . \rceil$ is the ceiling function and A_P is the WCA in the proposed structure of Fig. 4.2.

As an example, let us consider the efficient proposed structure with M_1=4, M_2=128 and K=3, which has the WCA = -30dB. However, a WCA of at least -45dB is required. To this end, the modified proposed structure should be use with

$$K_1 = \left\lceil \frac{45 - 30}{8.34} \right\rceil = \lceil 1.79 \rceil = 2.$$

Fig. 4.5 shows the overall magnitude responses for the proposed structure with K = 3 and the improved proposed structure with K = 3 and K_1 = 2 along with a zoom in the first folding. It can be seen that the modified proposed structure improves the alias rejection in the first folding band and all other folding bands that are not multiple of two.

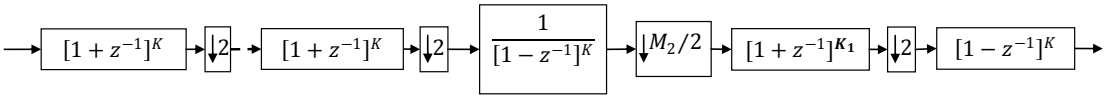


Fig. 4.4 Modified proposed structure.

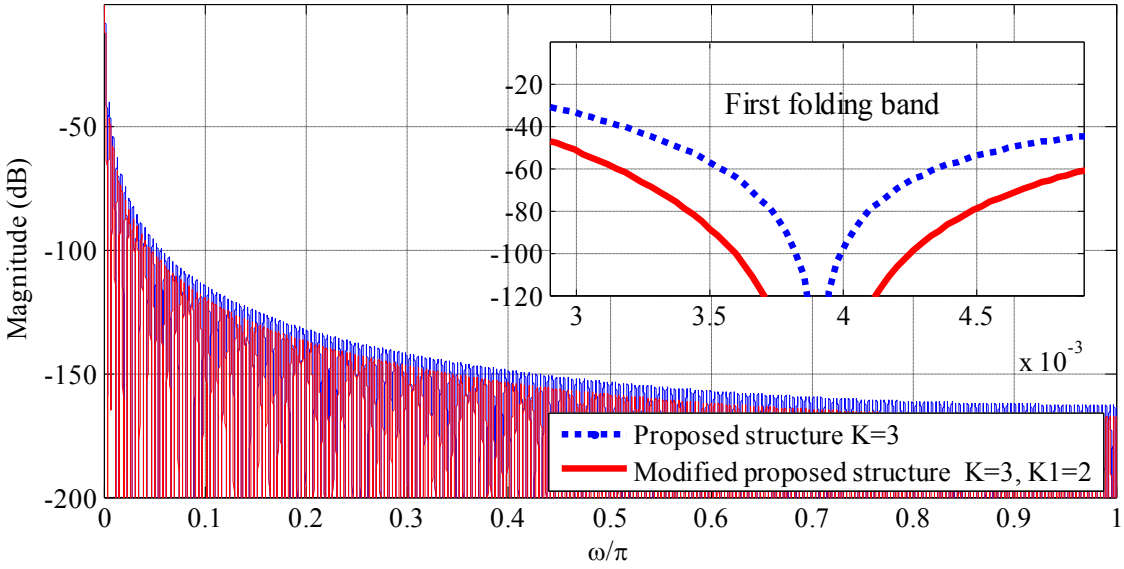


Fig. 4.5 Magnitude response for proposed and modified proposed structure, *M*=512.

Since the improved proposed structure only improves the odd folding bands, the number of K_1 filters cannot be increased without bound. The condition $K_1 < K$ must be satisfied in order to warranty a magnitude decaying behavior in the subsequent folding bands.

4.3.2 VHDL Implementation

In order to validate the power and area characteristics of the proposed structure and modified proposed structure, these decimators have been implemented in VHDL at the Register Transfer Level. The VHDL models, including the frequency divider, have been synthesized into standard cells of a 0.18µm CMOS-technology. The obtained transistor level models of each decimator, without parasitic effects, were used in Synopsys Hspice in order to simulate power consumption with a power supply of 1.8V. The input signal used to verify the performance of the decimators was the output bitstream of an ideal, first-order one-bit SD modulator, in which the input is a sine wave of 9.76 kHz and the modulated

output has a sampling frequency of 10MHz, and an OSR = 512. On the other hand, the obtained layouts were used to measure the used area of each decimator.

Table 4.1 presents a summary of power consumption and used area for the non-recursive comb, CIC and proposed structure for M=512 and K=3. It can be seen that the CIC structure requires more power than the others, but it uses less area. The non-recursive comb has less power consumption than the CIC, but uses more area. The proposed structure has similar power consumption than the non-recursive comb and almost the same used area of the CIC filter, validating its combined power and area efficiency.

Table 4.2 presents a summary of power consumption and used area for the proposed structure and the improved proposed structure considered in Example 4.1. It can be appreciated that the improved version of the proposed structure has an increase in power consumption of 1% compared with the proposed structure. Additionally, the improved version of the proposed structure has a relative increase of 20% in the used area. Therefore, the improved proposed structure increases the attenuation in the folding bands at the expenses of non-significant power increase and a slight area increase.

4.4 Proposed structure for high even decimation factors

In most of the cases the OSR of ΣΔMs is not a power of two. Therefore, in this section it is presented a slight modification of the proposed structure of Fig. 4.2 in order to extend the range of decimation factors without penalizing its main features.

It is know that the power of two number set belongs to the even number set. Thus, in the

Table 4.1 Summary of area and power consumption of comb, CIC and proposed structure for M=512.

Decimator for M=512, K=3.	Total Power (µW)	Total Area (µm^2)
Non-R Comb	226	424,569
CIC	408	326,041
Proposed M_1=4, M_2=128	235	339,309

Table 4.2 Summary of area and power consumption of proposed structure and modified proposed structure.

Proposed structure with M_1=4, M_2=128	WCA (dB)	Total Power (µW)	Extra Power (%)	Total Area (µm^2)	Extra Area (%)
Original K=3	-30	235	0	339,309	0
Improved K=3, K_1 =2	-46	238	1	423,832	20

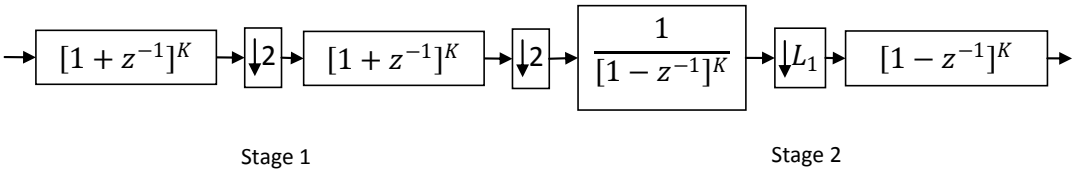
analysis that follows, it will be considered that M is an even number, i.e. M=2L, where L is an integer, which can be factorized in the form of $M=M_1M_2$ to be applied in the proposed structure of Fig. 4.2. The choice of the best values of M_1 and M_2 is discussed below considering that L is either an even or an odd number.

4.4.1 *L* is an even number

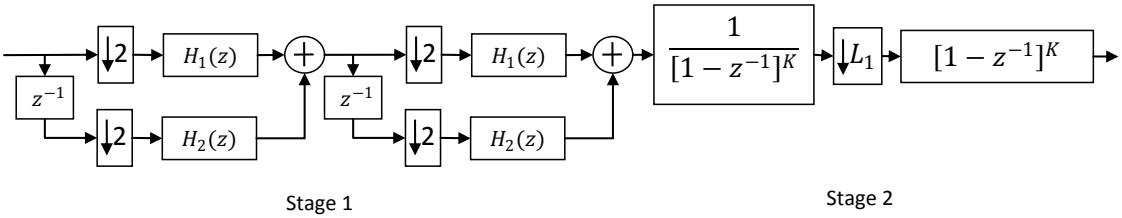
If L is an even number, it can be factorized in the form of $L=2L_1$, and therefore the overall decimation factor can be expressed as $M=4L_1$, indicating that M_1=4 and $M_2=L_1$. Therefore, the decimator structure presented in Fig. 4.2 can be modified as those shown in Figs. 4.6.

Fig. 4.6(a) presents a direct form realization for the non-recursive-comb stage, denoted as *Direct*-1 structure. Similarly, Fig. 4.6(b) shows the polyphase decomposition for the non-recursive part, referred to as *Polyphase*-1 structure.

By modifying the power and area expressions in (4.10) and (4.11), and also adding the polyphase decomposition of the non-recursive-comb stage, Fig. 4.7 presents the power and area estimations for *Direct*-1 and *Polyphase*-1, along with that of the equivalent CIC, taking as an example K=3. From Fig. 4.7(a) it can be seen that *Direct*-1 and *Polyphase*-1 structures are more power efficient than the equivalent CIC. For example at M = 100, *Direct*-1 and *Polyphase*-1 are 45% and 50%, respectively, more power efficient than CIC. The lower slopes in the power estimation curves of *Direct*-1 and *Polyphase*-1 structures, compared with that of the CIC structure, suggest that *Direct*-1 and *Polyphase*-1 become more power efficient as M increases. On the other hand, Fig. 4.7(b) indicates that *Direct*-1



(a)



(b)

Fig. 4.6 Decimator structure (a) *Direct*-1 and (b) *Polyphase*-1, for $M=4L_1$.

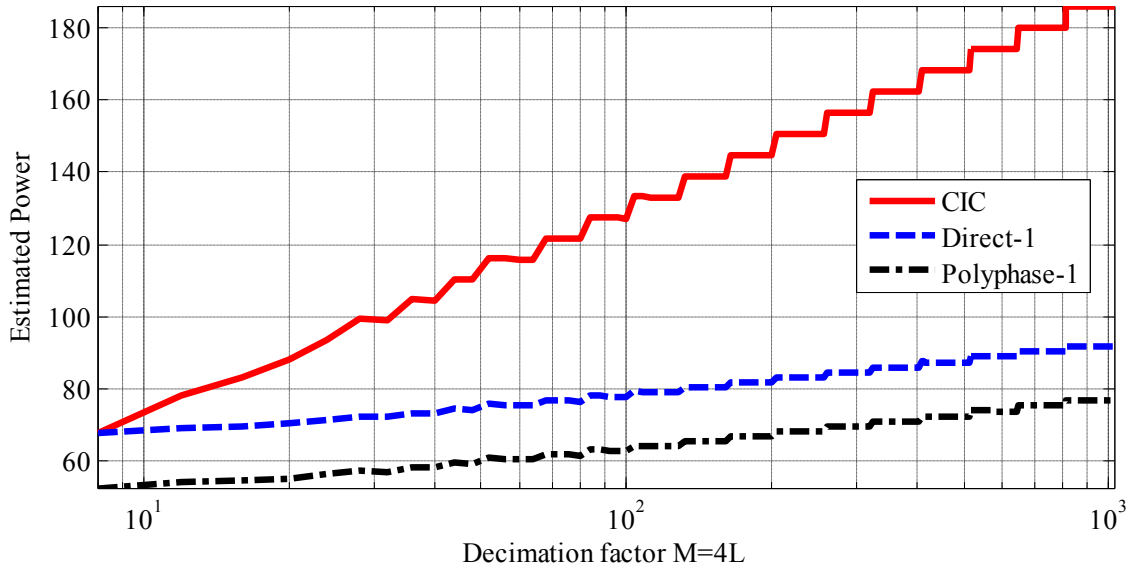
and *Polyphase*-1 requires about 20% and 25%, respectively, more area than the equivalent CIC for the same value of *M*. Based on MATLAB® simulations it can be determined that the relative power and area of *Direct*-1 and *Polyphase*-1, with respect to that of CIC, practically do not depend on the value of *K*. Therefore, *Direct*-1 and *Polyphase*-1 are power efficient structures with a moderate used area, for any value of *K*.

4.4.2 *L* is an odd number

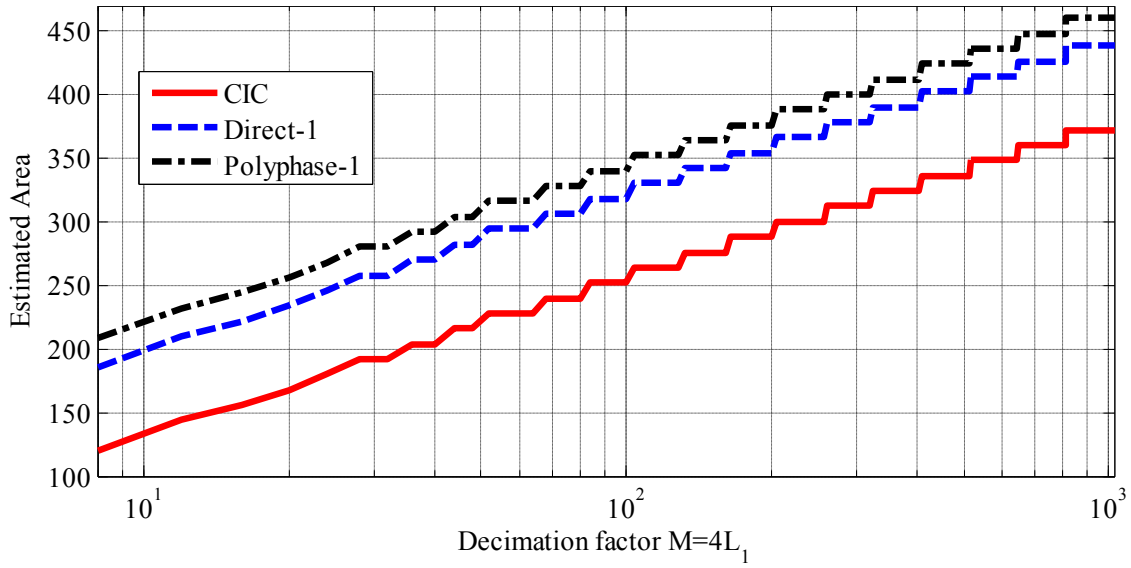
In this case, two different situations will be considered for *L*, either as an integer number or a number factorized in the form of $L = N_1N_2$, where N_1 is a prime number and N_2 and integer.

4.4.2.1 *L* is an integer number

In this case $M_1 = 2$ and $M_2 = L$ thus resulting in the structures *Direct*-2 and *Polyphase*-2 shown in Fig. 4.8. In addition, Fig. 4.9 presents the power and area estimations for *Direct*-2 and *Polyphase*-2 structures along with than of the equivalent CIC structure, considering *K*=3. From Fig 4.9(a), it can be observed that both *Direct*-2 and *Polyphase*-2, are always more power efficient than the equivalent CIC structure. Appreciable power savings are



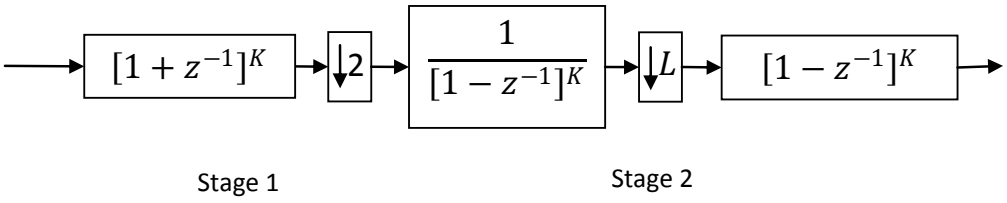
(a)



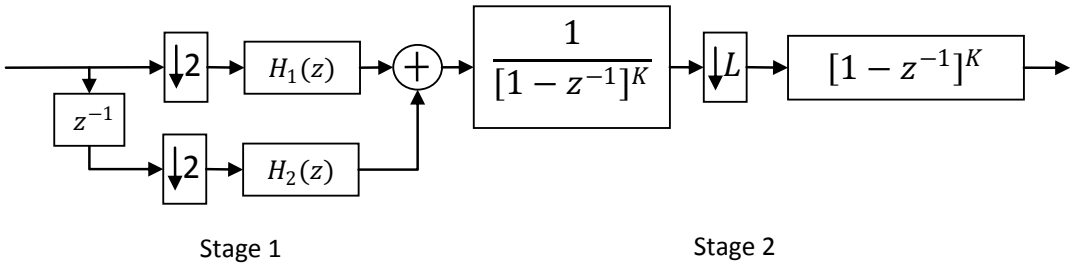
(b)

Fig. 4.7 (a) Power and (b) Area estimations for *Direct*-1, *Polyphase*-1 and CIC, for $M=4L_1$.

achieved for $M \geq 100$, where the minimum power saving is around 30% and 33% for *Direct*-2 and *Polyphase*-2, respectively. On the other hand, similarly as in Fig. 4.7(b), Fig. 4.9(b) shows that the area of *Direct*-2 and *Polyphase*-2 is 10% and 12%, respectively, larger than in the equivalent CIC structure, for the same value of *M*. Therefore, it can be concluded that *Direct*-2 and *Polyphase*-2 are more power efficient than CIC, preserving the area efficiency.



(a)



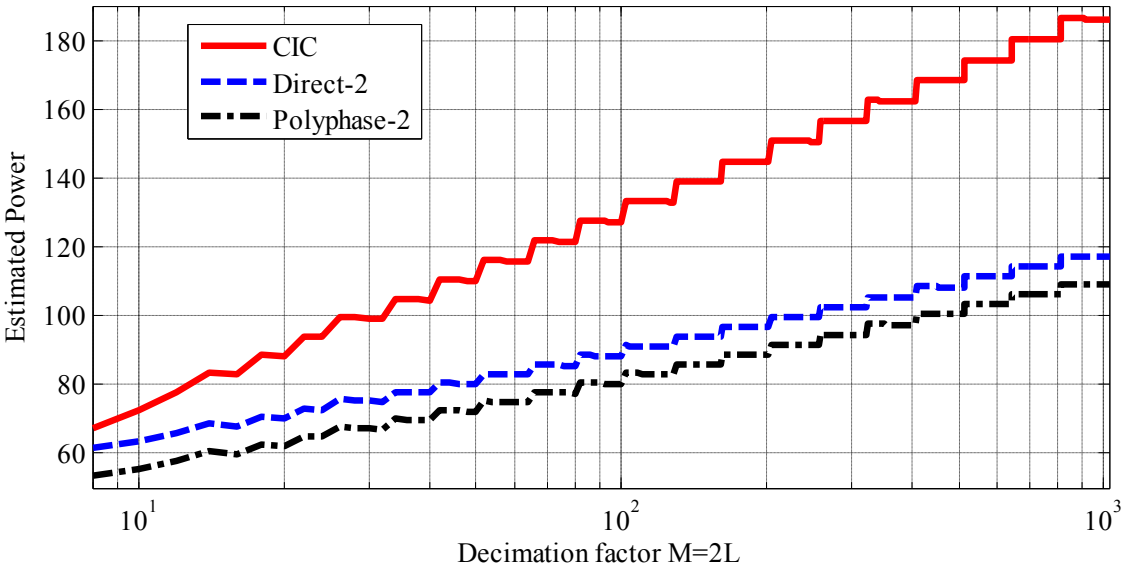
(b)

Fig. 4.8 Decimator structure (a) *Direct*-2 and (b) *Polyphase*-2, for M=2L.

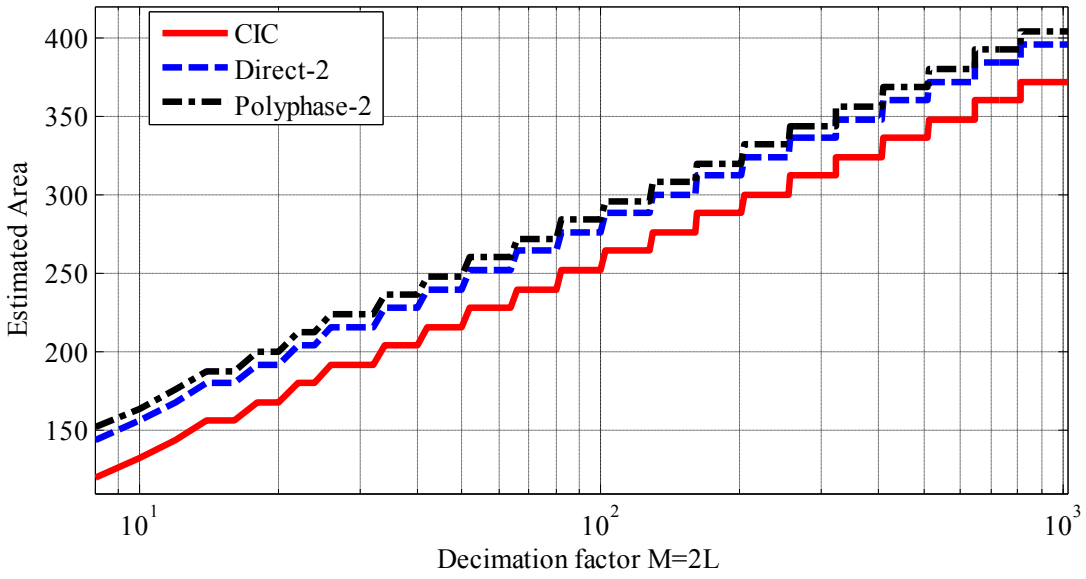
4.4.2.2 L can be factorized in the form of $L=N_1N_2$

In this case, it will be considered that L can be factorized in the form of $L = N_1N_2$, where N_1 and N_2 are integers and N_1 is a prime number (3, 5, 7, 11…). Let us consider the case when $N_1 = 3$, and thus $M_1 = 6$ and $M_2 = N_2$. In this case the first stage is realized with two non-recursive-comb stages decimating by 2 and 3, resulting in the structures *Direct*-3 and *Polyphase*-3 of Fig.4.10.

Fig. 4.11 shows the power and area estimations for the *Direct*-3 and *Polyphase*-3 along with that of the equivalent CIC structure, considering $K = 3$. In this case, *Polyphase*-3 is roughly 50% more power efficient that the equivalent CIC at $M = 100$, and the efficiency improves as M increases. In terms of active area, *Direct*-3 and *Polyphase*-3 require 40% and 45%, respectively, of extra area, compared with that of the equivalent CIC, for the same value of M. As a result, these structures are mainly power efficient. Similarly, the *Direct* and *Polyphase* realizations obtained for $N_1 \geq 5$ result in power efficient structures but with a relatively high increase in the required area when compared with an equivalent



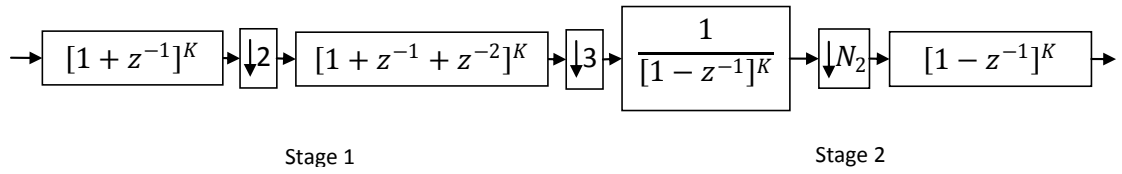
(a)



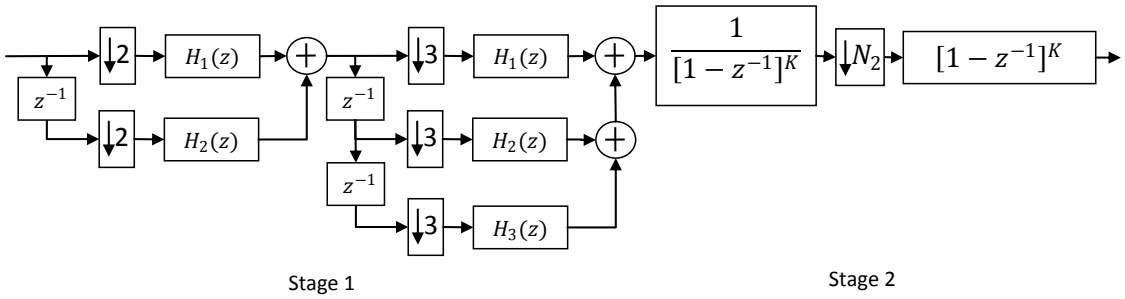
(b)

Fig. 4.9 (a) Power and (b) Area estimations for *Direct*-2, *Polyphase*-2 and CIC, for M=2L.

CIC structure. Thus, from a practical point of view values of $N_1 \geq 5$ are not recommended. Next section introduces a slight modification on the presented structures in order to improve the alias rejection in the first folding band.



(a)



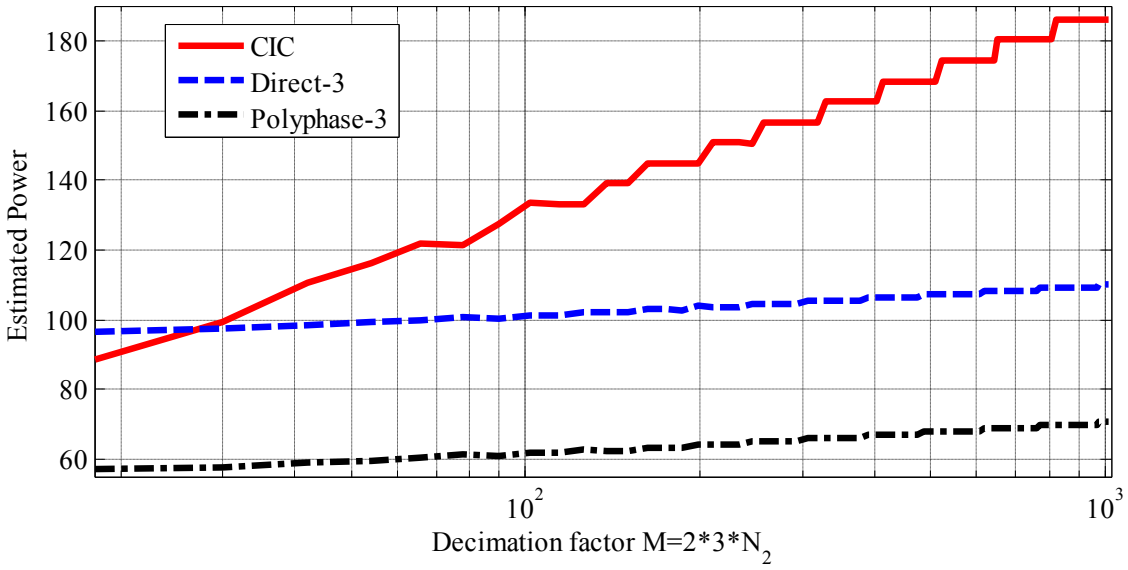
(b)

Fig. 4.10 Decimator structure (a) *Direct*-3 and (b) *Polyphase*-3, for M=2·3N_2.

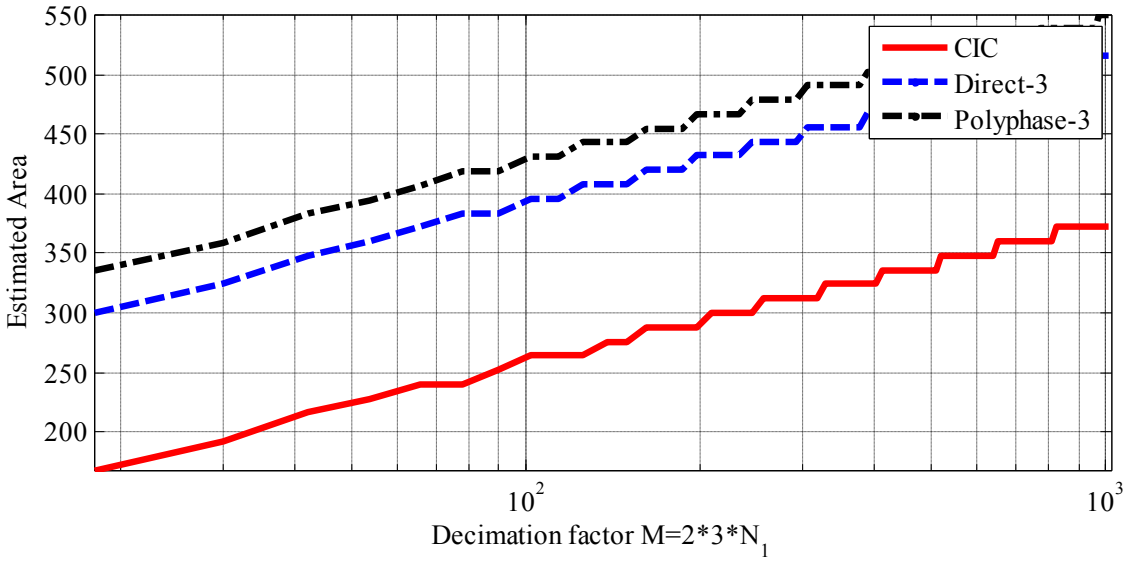
4.4.3 Alias rejection improvement

In order to improve the alias rejection in the proposed structures for high even decimation factors, the method proposed in [4], where the WCA is improved by means of increasing the number of cascaded filters in last stage, has been considered. Therefore, Fig. 4.12 presents a slight modification of *Direct*-1 and *Polyphase*-1, referred to as *Modified-direct*-1 and *Modified-Polyphase*-1, respectively. The added K_1 filters in the last stage of *Modified-direct*-1 and *Modified-Polyphase*-1 structures will result in an improved alias attenuation in all folding bands except the even bands. Similarly, Fig. 4.13 presents a modified realization of *Direct*-3 and *Polyphase*-3, referred to as *Modified-direct*-3 and *Modified-Polyphase*-3, respectively.

From Figs. 4.12 and 4.13 it can be seen that excluding the last non-recursive-comb section, the modified structures are like *Direct*-2 and *Polyphase*-2. Therefore, in terms of power the modified structures behave in a similar fashion than *Direct*-2 and *Polyphase*-2. On the other hand, the area is being increased, since the last stage has a cascade of $K + K_1$ non-recursive-comb stages, which should work with the full arithmetic precision.



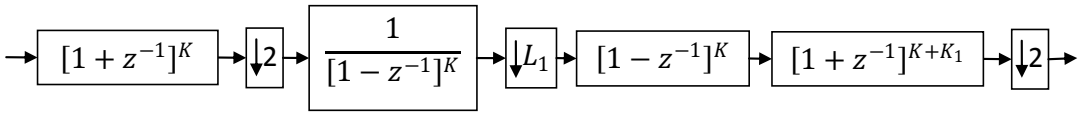
(a)



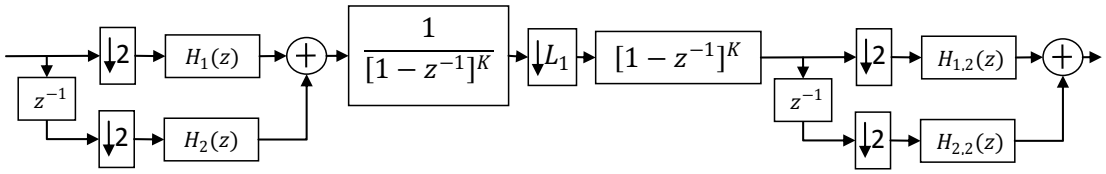
(b)

Fig. 4.11 (a) Power and (b) Area estimations for *Direct*-3, *Polyphase*-3 and CIC, for $M=2\cdot 3N_2$.

Note also from Figs. 4.12 and 4.13 that the added K_1 filters in the last stage will improve the alias rejection with a non-significant power increase, since they work almost at the final sampling rate. From section 4.3.1, it is known that each added cascaded filter $K_1=1$, in the modified proposed structure of Fig. 4.4, provides an increased attenuation of –8.53dB. A similar formula to (4.15) can be used to determine K_1, since each added K_1 in the structures of Fig. 4.13 provides an increased attenuation of -9.11dB.

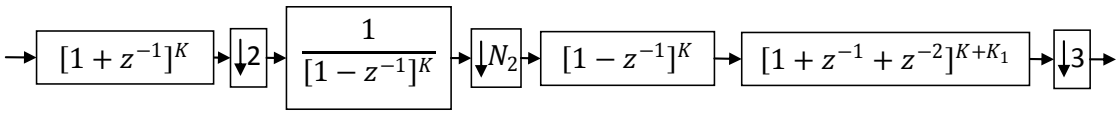


(a)

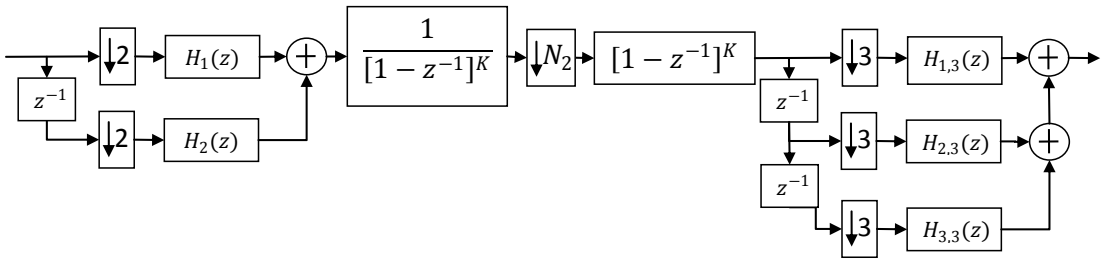


(b)

Fig. 4.12 Modified decimator (a) *Modified-Direct*-1 and (b) *Modified-Polyphase*-1, for M=2·L_1·2, where $H_{i,2}(z)$, i=1,2 are the polyphase components at last stage.



(a)

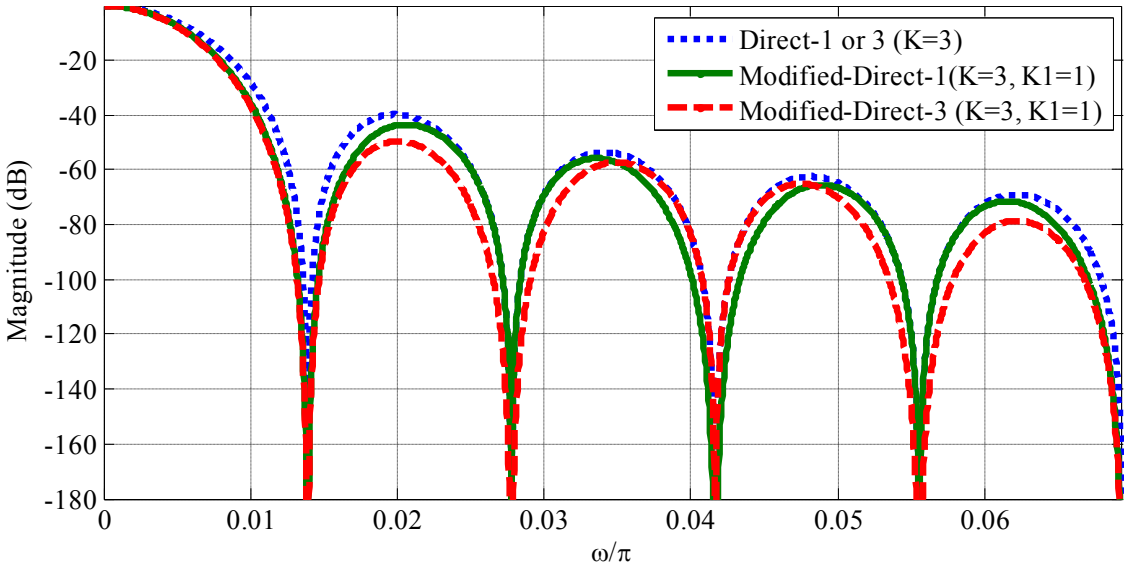


(b)

Fig. 4.13 Modified decimator (a) *MDF*-3 and (b) *MPD*-3, for M=2·N_2·3, where $H_{i,3}(z)$, i=1,2,3 are the polyphase components at last stage.

As an example, let us consider M = 144 and K = 3 for either *Direct*-1 or *Direct*-3. Those structures will have a WCA of about –30dB, considering that the residual decimation factor is two. The *Modified-direct*-1 and *Modified-Direct*-3 structures with an additional cascade of K_1 = 1 filters in last stage will provide a WCA of 38.53 and 39.11, as it can be seen in

Figs. 4.14. Note that the attenuations in the first and the all-folding bands, which are not multiples of either two or three, are improved.



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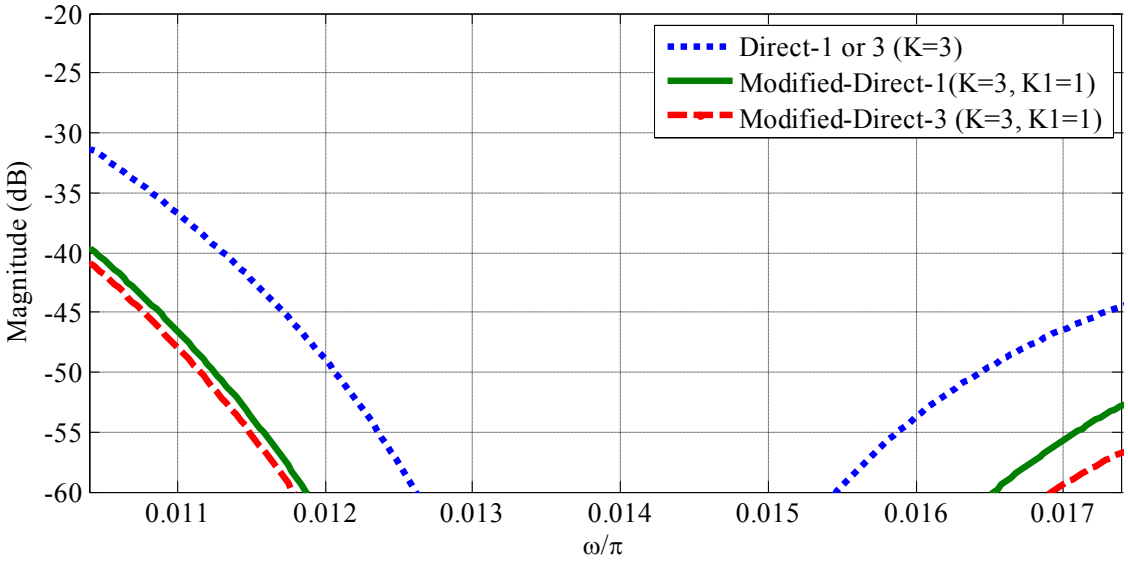


(b)

Fig. 4.14 Magnitude responses for *Direct*-1, *Modified-Direct*-1 and *Modified-Direct*-3 considering M=144 (a) the fisrt ten folding bands and (b) a zoom in the first folding band.

4.4.4 VHDL Implementation

Some of the presented two stage structures and the equivalent CIC have been implemented in VHDL taking as a reference a Spartan 3E FPGA device from Xilinx. The area is measured in terms of the number of used slices whereas the power is estimated with the XPower Analyzer tool from Xilinx. For the power estimation, the input to the decimators is the output bit stream of a second order low-pass one bit Sigma-Delta modulator. The modulator is implemented in a fully differential way so that the output signal is either -1 or 1, which are represented with two bits in a two´s complement format, i.e. 11 and 01. The sampling frequency of the modulator has been fixed to 100MHz whereas the input is a sinusoidal test tone of 170kHz, thus the OSR is about 144. Such an OSR has been chosen since it can be accommodated in all the implemented structures.

Table 4.3 shows a summary of dynamic power consumption and used area of the implemented structures *Direct*-1, *Direct*-2, *Ddirect*-3, *Modified-direct*-1, and *Modified-Direct*-3 along with the equivalent CIC. From Table 4.3, it can be seen that there is a good correspondence between the implementation results and the estimations presented in Section 4.3.1 and 4.3.2. Actually, implemented power results suggest more power efficiency, of the two-stage structures, than in the estimations made in the previous sections. This last is due to the fact that the activity factor in the integrator section of CIC, as suggested by the power analyzer tool, is sensitively larger than in the non-recursive-comb. On the other hand, implemented area results provide larger relative area increase of the presented two stage structures compared with that of CIC. This is because the clock divider, which provides the different sampling rates, was not considered in the area estimations of previous sections.

From Table 4.3, it can be seen that the *Direct*-1 and *Direct*-2 structures provide the best power and area efficiency trade-off, making possible considerable power savings at the expense of a small area increase. The structure *Direct*-3 is power efficient but it has a considerable area penalty. On the other hand, the *Modified-Direct*-1 and *Modified-Direct*-2 structures keep the power efficiency while the WCA is improved, but at the cost of large area increase. Thus those structures are mainly power efficient.

Table 4.3 Summary of power and area results of the implemented structures for M = 144.

Decimator (M=144)	WCA (dB)	Total Power (mW)	Power Savings (%)	Total Area (Slices)	Extra Area (%)
CIC (K=3)	30	3.79	0	125	0
Direct-1 (K=3)	30	2.00	47.22	180	44
Direct -2 (K=3)	30	2.48	34.56	148	18.40
Direct -3 (K=3)	30	2.41	36.41	220	76
Modified-direct-1 (K=3, K_1=1)	38.58	2.52	33.50	241	92.80
Modified-direct -3 (K=3, K_1=1)	39.11	2.58	31.92	383	206.40

4.5 Proposed structure with decimation factors that are power of three

Similar to the power of two case, a popular non-recursive comb structure is that in which the decimation factor can be expressed as a power of three, i.e. $M = 3^P$. The transfer function for this non-recursive comb decimator is defined as:

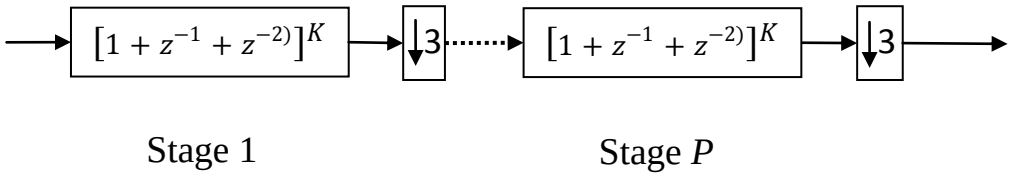
$$H_3(z) = \frac{1}{3^{PK}}\left[\prod_{i=0}^{P-1}(1 + z^{-1} + z^{-2})\right]^K. \tag{4.16}$$

Figs. 4.15(a) and 4.15(b) illustrate the implementation of the comb in (4.16) in both direct form and polyphase form, respectively. By using (4.1)-(4.3), the power and area estimations for the direct form implementation (Fig. 4.15(a)) are:

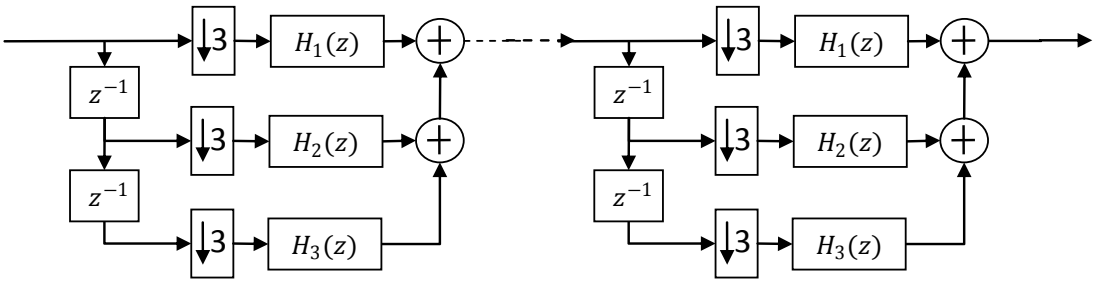
$$P_{Comb} = \sum_{i=0}^{P-1} \frac{(FA + FF)[B_{in} + log_2(3)K \times (i+1)]}{3^i}, \tag{4.17}$$

$$A_{Comb} = \sum_{i=0}^{P-1} (FA + FF)[B_{in} + log_2(3)K \times (i+1)]. \tag{4.18}$$

Similar expressions can be used for the polyphase implementation; the only difference is that the number of required full adders and flip-flops depend on the number of cascaded stages K, the coefficient representation and the use or not of sub-expression sharing techniques [5]. As an illustration, Table 4.4 shows the number of *FA* and *FF* with cascades,



(a)



(b)

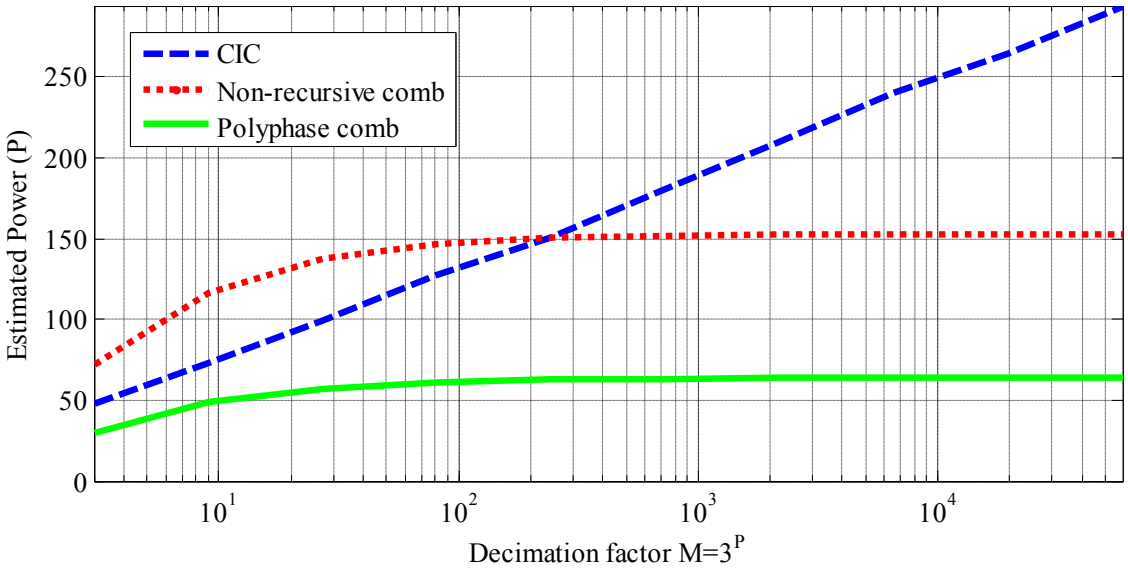
Fig. 4.15 Non-recursive comb for $M = 3^P$: (a) direct form implementation and (b) polyphase form implementation.

K, ranging from 2 to 5, considering binary representation of coefficients and no sub-expression sharing.

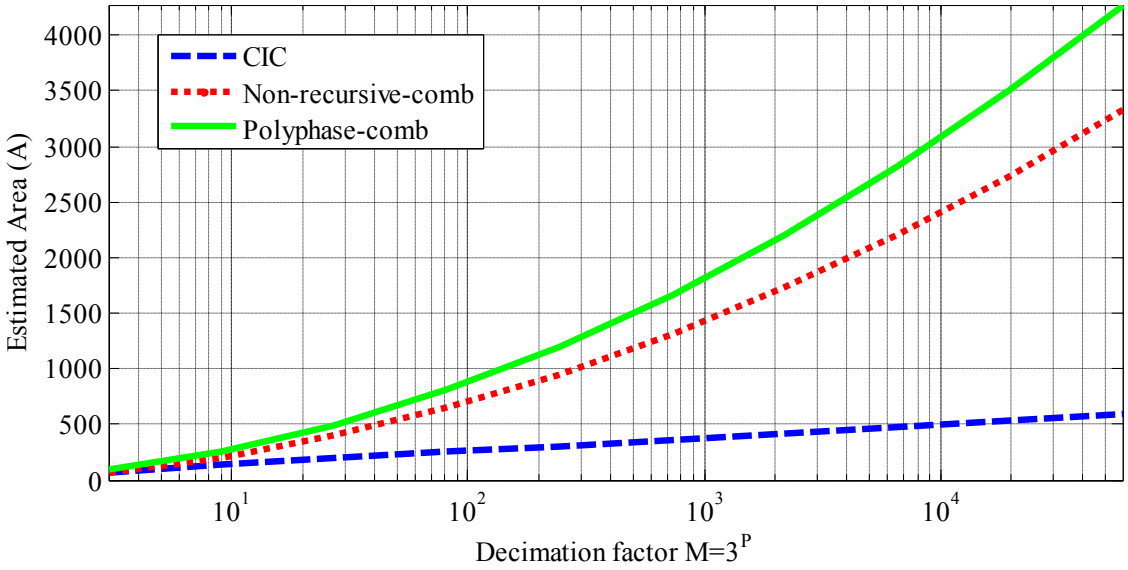
By considering $K = 3$ and $M = 3^P$, Fig. 4.16(a) and Fig. 4.16(b) present the estimated power consumption and the required area, respectively, for non-recursive comb, polyphase comb and CIC structures for $M=3^P$. From Fig. 4.16(a) it can be seen that for high values of the decimation factor, the estimated power of non-recursive comb and polyphase comb is lower than that of the CIC structure, similar to that shown for the case of $M = 2^P$. However, there are some values of the decimation factor at which non-recursive comb is less power

Table 4.4 Adders and flip-flops required in polyphase comb for *M*=3.

K	*FA* structure	*FA* coefficients	*FA* total	*FF* total
2	4	1	5	2
3	6	5	11	4
4	8	4	12	6
5	10	21	31	8



(a)

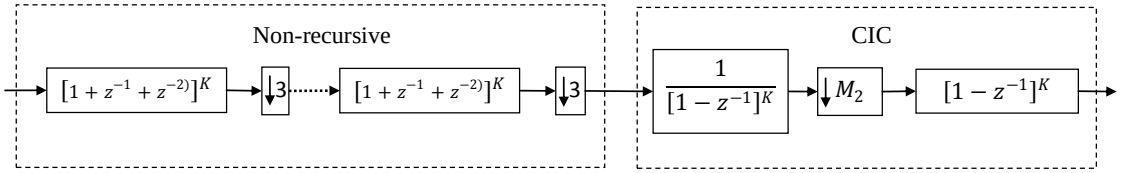


(b)

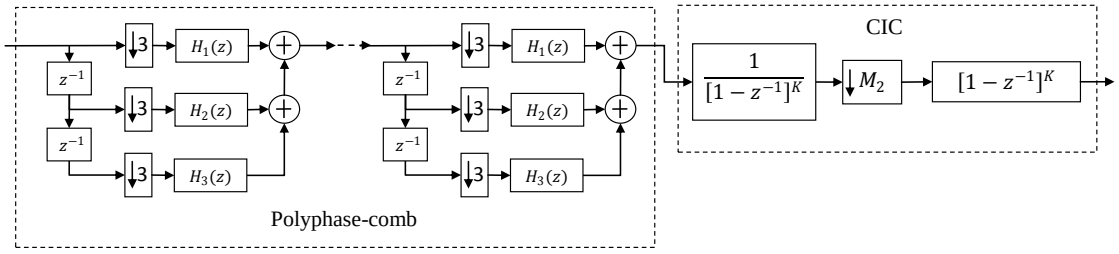
Fig. 4.16 Estimated (a) power and (b) area, for CIC, non-recursive comb and polyphase comb, for $M=3^P$.

efficient than CIC structure. Nevertheless, polyphase-comb structure always exhibits less power requirements than CIC for all the values of *M*, mainly due to the frequency reduction at the first stage. On the other hand, for high values of *M* the area requirements for polyphase comb and non-recursive comb are higher than that for the CIC structure.

The proposed structure in Fig. 4.2 is based on the fact that the first stage, implemented by the non-recursive comb 2, constitutes an economical way to reduce the input sampling rate for the second stage. The second stage in turn, implemented by the CIC, takes part in the area efficiency of the overall structure. This concept can be extended to the use of non-recursive comb structure, in the first stage, with the decimation factor that is a power of three (4.16). As a result, Fig. 4.17 illustrates the proposed structure for $M = 3^P$. The structure of Fig. 4.17(a) has the first stage implemented in direct form, referred to as *NR-CIC*-1, while the structure of Fig. 4.17(b) has the first stage implemented in polyphase form, referred to as *NR-CIC*-2.



(a)



(b)

Fig. 4.17 Proposed structure for M=3^P: (a) *NR-CIC*-1 and (b) *NR-CIC*-2.

From (4.8) and (4.16), the transfer functions of *NR-CIC*-1 and *NR-CIC*-2, referenced to the high sampling rate, can be written as:

$$H(z) = \left[\left(\prod_{i=0}^{log_3(M_1)-1} (1+z^{-1}+z^{-2})\right)\left(\frac{1-z^{-M_2}}{1-z^{-1}}\right)\right]^K . \qquad (4.19)$$

By using (4.4), (4.5), (4.17) and (4.18) it can be shown that the power and area estimations for *NR-CIC*-1 are given by:

$$P_{NR-CIC-1} = \sum_{i=1}^{log_3(M_1)} \frac{(FA+FF)\cdot\lceil B_{in}+K\cdot log_2(3^i)\rceil}{3^{i-1}} + \frac{(FA_I+FF_I)B_{out}}{M_1} + \frac{(FA_C+FF_C)B_{out}}{M_1M_2}, \quad (4.20)$$

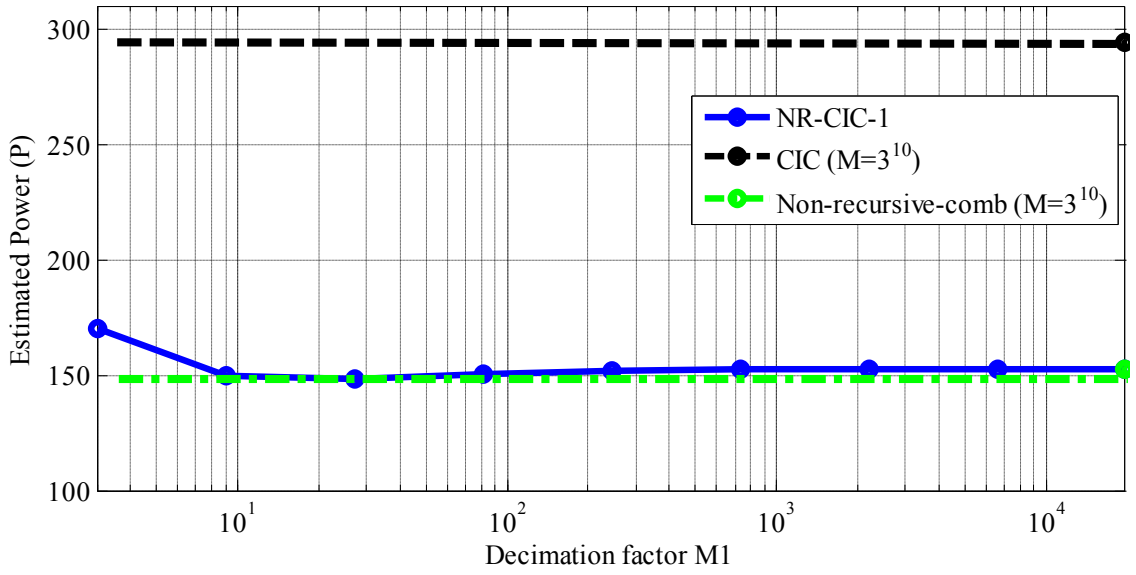
$$A_{NR-CIC-1} = \sum_{i=1}^{log_3(M_1)} (FA+FF)\cdot\lceil B_{in}+K\times log_2(3^i)\rceil + (FA_I+FF_I)B_{out} + (FA_C+FF_C)B_{out}, \quad (4.21)$$

which are very similar to that in (4.10) and (4.11). Thus, the methodology for the choice of M_1 and M_2 presented in section 4.2 can be applied to the structures of Figs. 4.17.

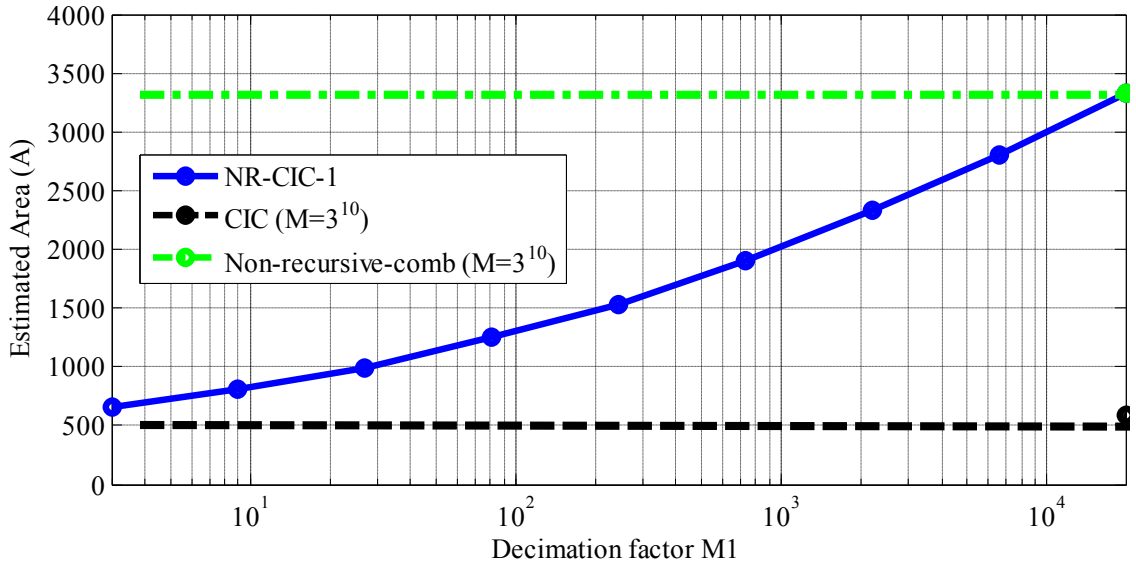
4.5.1 Choice of M_1

Let us consider first the *NR-CIC*-1 structure with a decimation factor $M=3^{10}=59049$. In this case, M_1 can take the values 3, 9, 27... 3^9. The reason for choosing those values of M_1 lies on the fact that for decimation factors lower than $3^8=6561$, the required power of non-recursive-comb is larger than in the equivalent CIC structure, (see Fig. 4.16(a)). If the power estimation of non-recursive-comb is larger than that of the CIC, then the *NR-CIC*-1 will not be power efficient.

Fig. 4.18(a)-(b) show the estimated power and area of the *NR-CIC*-1 structure, considering different possible values of M_1, along with the reference values for non-recursive-comb and CIC structures with $M=3^{10}$. Observing Fig. 4.18 it can be concluded that the best choice for M_1 is 3, and hence $M_2=3^9=19683$. In this way, the *NR-CIC*-1 exhibits the same low power characteristic as a non-recursive comb structure and at the same time low area as the CIC structure. However, although, in this example, the *NR-CIC*-1 is both power- and area-efficient, a decimation factor larger than 3^{10} is unfeasible for practical applications in ΣΔ-ADCs, where such OSRs would result in excessively power consumption in the ΣΔM. Therefore, *NR-CIC*-1 is not adequate for the targeted application in ΣΔM.



(a)



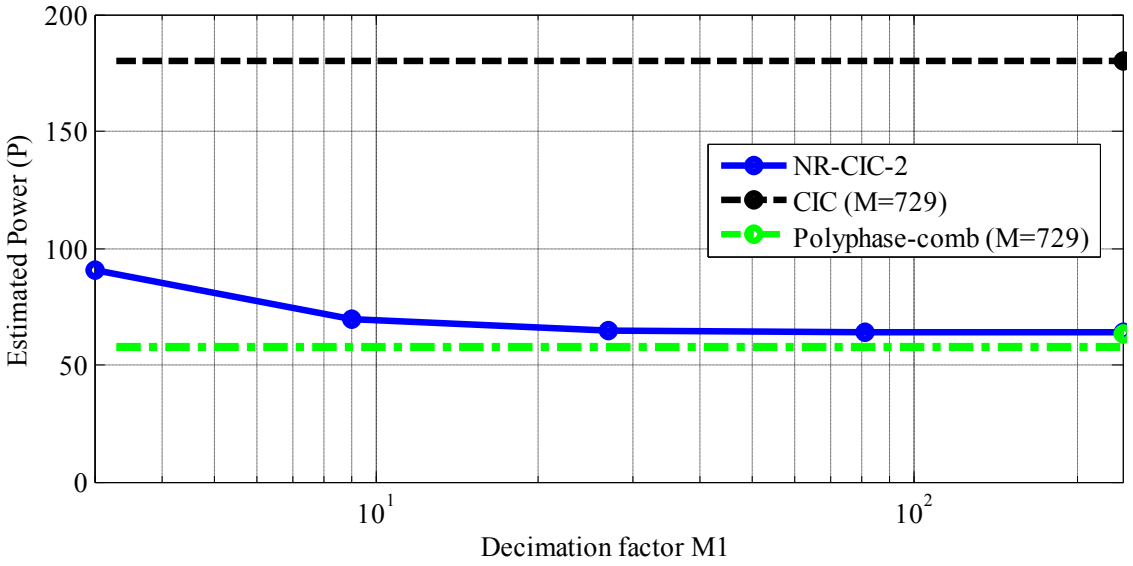
(b)

Fig. 4.18 Estimated (a) power and (b) area, for *NR-CIC*-1, $M=3^{10}$.

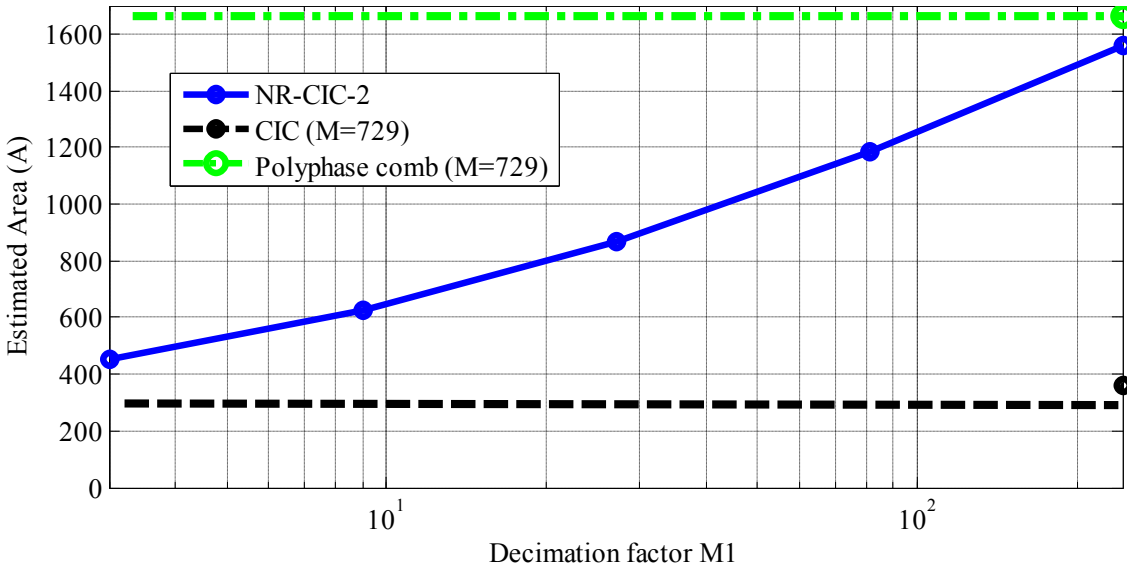
On the other hand, since polyphase comb requires less power than CIC for all values of M (see Fig. 416(a)) the *NR-CIC*-2 topology can be both power- and area-efficient for lower values of the decimation factor, or equivalently lower values of P.

Let us consider $K=3$, $M=3^6=729$, which is a feasible value for ΣΔ-ADCs in low-frequency applications. Fig. 4.19(a) and 4.19(b) show the estimated power and area, respectively, for the *NR-CIC*-2 topology, as a function of M_1. The reference values for non-recursive comb

and CIC structures with $M=3^6$ are also presented. From Figs. 4.19 it can be seen that the best value for M_1 is 9: thus, M_2=81. In this case, the *NR-CIC*-2 topology shows similar power efficiency as that of polyphase comb structure, and area efficiency similar to the CIC structure. Therefore, the proposed *NR-CIC*-2 structure results in a more efficient solution in terms of power and active area. However, an overall decimation factor of $M=3^6=729$ is still



(a)



(b)

Fig. 4.19 Estimated (a) power and (b) area, for *NR-CIC*-2, $M=3^6$.

unpractical for most of the ΣΔM. Therefore, a slight modification of the *NR-CIC*-2 is presented in the following.

4.5.2 Structure for decimation factors that are multiples of three

Since the second stage (CIC) of the *NR-CIC*-2 structure is able to decimate by any integer value, *NR-CIC*-2 can be easily modified to cope with decimation factors that are integer multiples of 3. In this way, the first stage is composed by the polyphase comb decimating by three and the second stage is a CIC decimating by an integer value *L*. This structure is illustrated in Fig. 4.20, which is referred to as polyphase-4. Fig. 4.21 presents the power and area estimations for the polyphase-4 structure along with that for the equivalent CIC structure. It can be noticed that the polyphase-4 structure is always more power efficient than the corresponding CIC, especially for high values of the decimation factor. This power efficiency comes at the cost of an area increase of about 36%, which is independent of *M*.

4.6 Corrected-1 structure

The proposed structure of section 4.2 has demonstrated to be both power and area efficient for decimation factors that are power of two and even numbers. Although there have been proposed modified structures to improve the alias rejection, the passband still shows a passband droop like simple comb decimators. Therefore, in this section a corrector filter

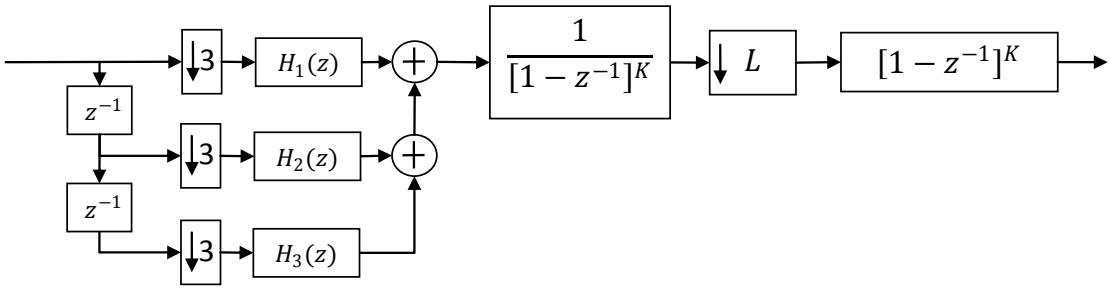
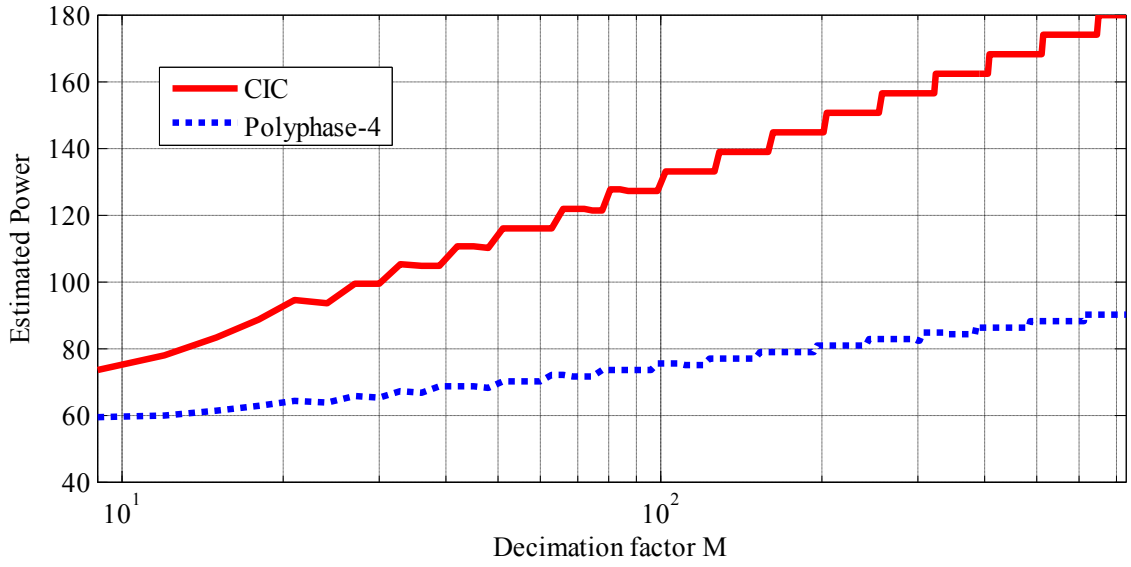
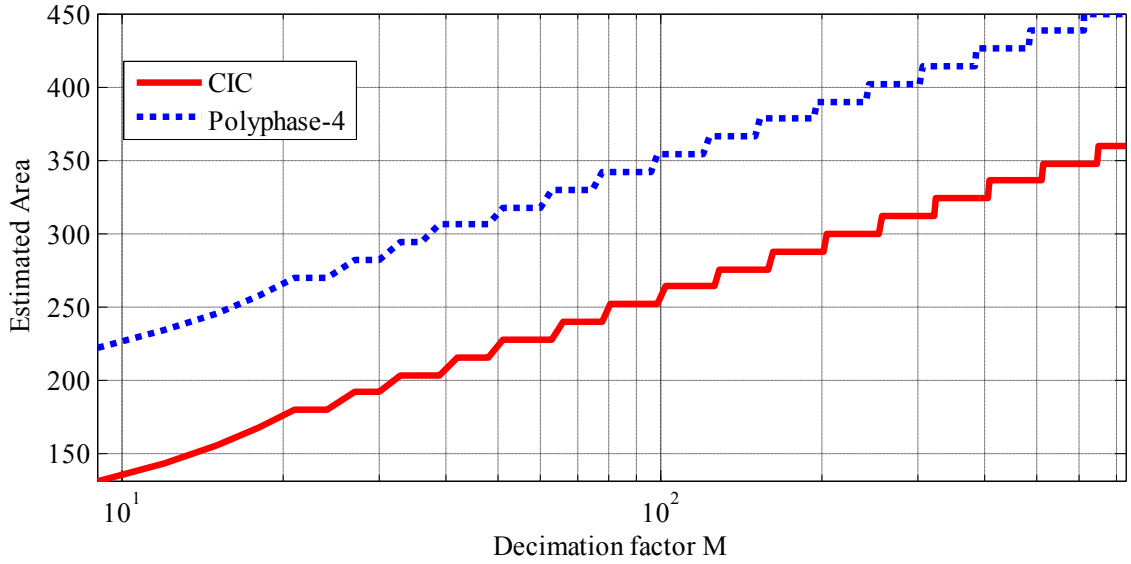


Fig. 4.20 Polyphase-4 structure, for decimation factors that are multiples of three.



(a)



(b)

Fig. 4.21 Estimated (a) power and (b) area, for *polyphase*-4 structure along with the corresponding CIC.

will be introduced in the two-stage structure to improve its magnitude response in both the passband and the stop bands.

The corrector filter should not significantly penalize the efficiency of the two-stage structure: consequently, the corrector filter has to be *multiplierless* and to work at a low sampling rate.

To this end, the corrector filters proposed in [6] have some important characteristics which make them suitable for this application:

- The choice of the corrector does not depend on the decimation factor but depends only on the parameter *K*.
- The filters decrease the comb passband droop and increase the alias rejections in the most critical first folding band.
- Additionally, the alias rejections are increased in all sub sequential folding bands which are not multiple of two, i.e in all odd folding bands.
- The coefficients of the filter can be presented as sums of power of two, thus resulting in a multiplierless design.
- The filters work at a rate which is *M*/2 times less than the high input rate.

By using the corrector filter of [6] in the proposed structure of Fig. 4.2 it is obtained the *corrected*-1 structure, which is illustrated in Fig. 4.22 The transfer function of the corrected-1 proposed structure is as follows:

$$H(z) = H_P(z)C_K\left(z^{M/2}\right), \tag{4.22}$$

where $H_P(z)$ is given in (4.2). In (4.22), $C_K(z)$ is the corrector filter, which depend on the number of cascaded filter K in $H_P(z)$, this is illustrated in Table 4.5.

Next examples illustrate how the magnitude response of the two-stage structure can be improved by using the corresponding corrector filter from Table 4.5.

As an example, let us consider the proposed structure of Section 4.2 with $M_1 = 4$ and $M_2 = 128$ and $K = 3$, and the *corrected*-1 structure of Fig. 4.22 with the same parameters and C_3. Fig. 4.23(a) illustrates the overall magnitude response of these two structures along with a zoom in the first five folding bands, and Fig. 4.23(b) shows the corresponding passband and first folding band zooms.

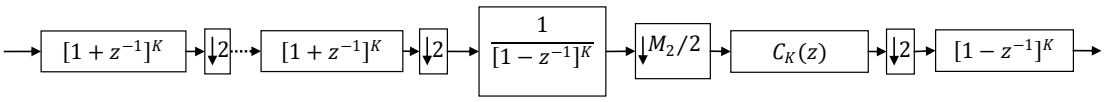


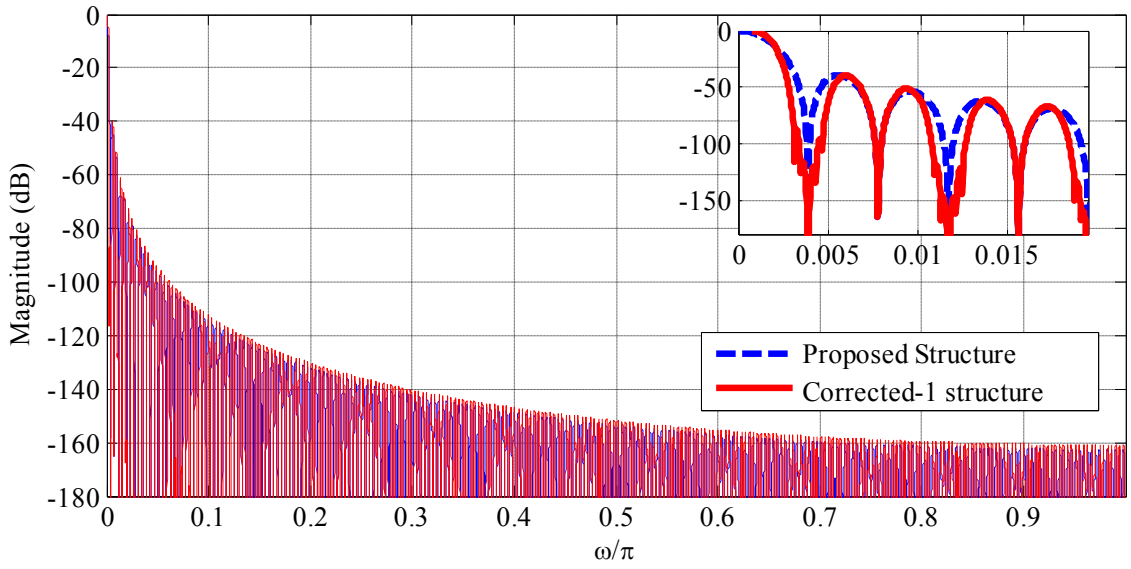
Fig. 4.22 *Corrected*-1 structure.

Table 4.5 Corrector filters from [6]

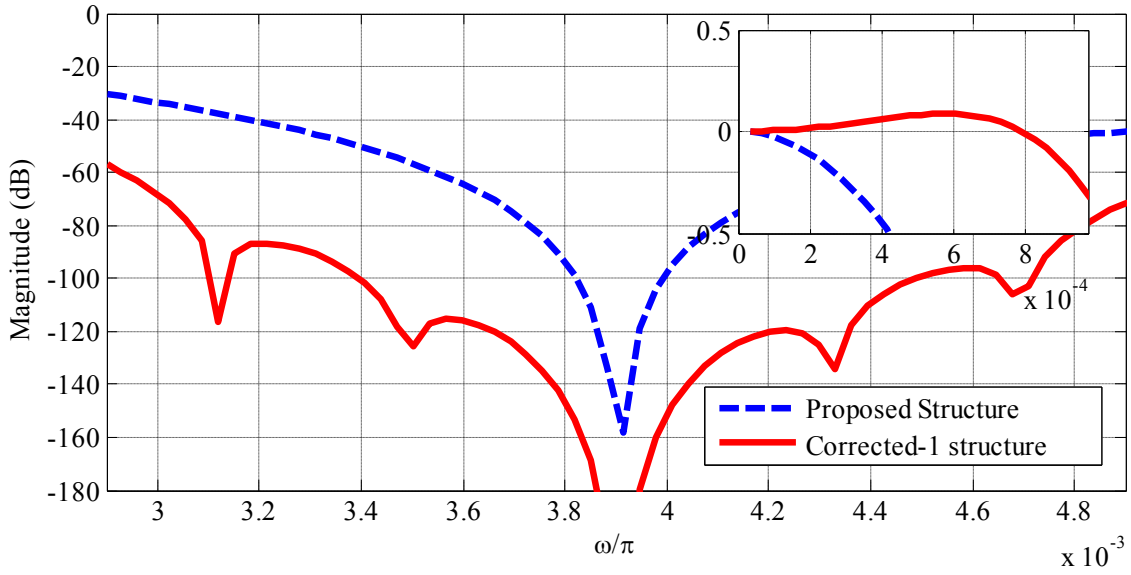
K	$C_K(z)$
1	$-3+2z^{-1}+17z^{-2}+17z^{-3}+2z^{-4}-3z^{-5}$
2	$1-z^{-1}-5z^{-2}+3z^{-3}+18z^{-4}+18z^{-5}+3z^{-6}-5z^{-7}-z^{-8}+z^{-9}$
3	$1-z^{-1}-6z^{-2}+2z^{-3}+21z^{-4}+21z^{-5}+2z^{-6}-6z^{-7}-z^{-8}+z^{-9}$
4	$1+z^{-1}-2z^{-2}-8z^{-3}+z^{-4}+24z^{-5}+24z^{-6}+z^{-7}-8z^{-8}-2z^{-9}+z^{-10}+z^{-11}$
5	$1+2z^{-1}-2z^{-2}-11z^{-3}+27z^{-5}+27z^{-6}-11z^{-8}-2z^{-9}+2z^{-10}+z^{-11}$

4.6.1 VHDL implementation

Here it is considered the implementation of the *corrected*-1 structure with $M_1 = 4$, $M_2 = 128$ and C_3, and it is compared in terms of power and area efficiency with the two-stage structure and improved two-stage structure presented in Section 4.3. To this end, the corrector filter C_3 is implemented with only shifts and adds as is illustrated in Fig. 4.24. The bit word-length increase for the corrector C_3 is 6 bits. The *corrected*-1 structure, with the corrector C_3, was described at the register transfer level in VHDL, considering the same design parameters used for the two-stage and improved two-stage structure of section 4.3. Therefore, the power simulation was carried out at the transistor level, without considering parasitic effects, with a power supply of 1.8V, which is summarized in Table 4.6. Although C_3 introduces 11 adders with the full word length, the power consumption increase is negligible compared with that of the structures of section 4.2. On the other hand, the layout of the proposed structure was used to measure the required active area, which is also presented in Table 4.6. It can be seen that the *corrected*-1 has a relatively high area increase mainly due to the introduced adders at the full word-length. Thus the magnitude response



(a)



(b)

Fig. 4.23 Magnitude response of *corrected*-1 structure and proposed structure (Section 4.2): (a) overall and (b) fists folding band and passband.

improvements in *corrected*-1 structure come at the expense of an area increase. Nevertheless, it can be demonstrated that if the proposed structures of section 4.2 were designed for a minimum attenuation of -61dB and a compensation in the passband, their area would be larger compared with that of the *corrected*-1 structure.

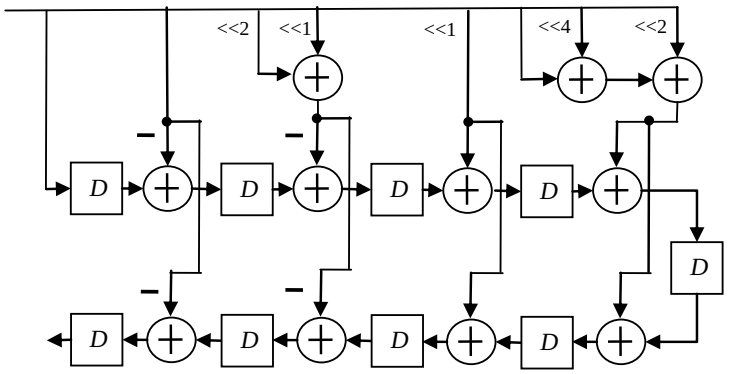


Table 4.24 Multiplierless implementation of C_3.

Table 4.6 Power and area results of structures *corrected*-1, proposed and modified structure.

Decimators with M_1=4, M_2=128	WCA (dB)	Pass band comp.	Total Power (µW)	Total Area (µm^2)
Proposed structure (section 4.2) K=3	-30	No	235	339,309
Improved structure (section 4.2) K_1=3, K_2 =2	-46	No	238	423,832
Corrected-1 structure K=3 and C_3	-61dB	Yes	242	640,000

4.7 Corrected-2 structure

In the last section it could be seen that the corrector filters C_K are multiplierless filters defined for the parameter K=1,…5. From Table 4.5 it can be noticed that the correctors require 7 adders for C_1, (K=1); 12 adders for C_2, $C_3(z)$, and C_4, (K=2, 3, 4, respectively); and 16 adders for C_5, (K=5). It is clear to see that as K increases, a more complex corrector is required. In order to overcome this issue here it is proposed:

- In the last stage, use the simplest corrector C_1 along with the single comb filter $(1 + z^{-1})$.
- Apply the sharpening technique to the cascade of C_1 and $(1 + z^{-1})$.

The *corrected*-2 structure is illustrated in Fig. 4.25, where only the corrector $C_1(z)$ is used: additionally, there is a sharpening section composed of the corrector filter $C_1(z)$ and the single comb filter $(1 + z^{-1})$. In the sharpening section, it is used the simple sharpening polynomial in the form of $2H\text{-}H^2$. Note that in this structure the overall decimation factor must be expressed as $M=M_1M_2\cdot 2$.

As an example, consider the parameters $M = 144 = 2\cdot 36\cdot 2$ and $K=3$. The magnitude responses of the *corrected*-2 structure along with that of the proposed structure, with the aforementioned parameters, are presented in Fig. 4.26. The overall response along with a zoom in the first five folding bands is presented in Fig. 4.26(a), while Fig. 4.26(b) presents the corresponding zoom in the first folding band and passband. Note that the attenuations in all odd folding bands are increased, and the passband droop is decreased as well.

An interesting feature of the *corrected*-2 structure is that the cascade of C_1 and the sharpening of C_1 with $(1 + z^{-1})$ can remain unchanged independently of the value of K. Fig. 4.27 illustrates the passband of the *corrected*-2 structure considering $M = 144$ and different values for K. It can be seen that the passband deviation remains within an absolute value of about 0.5dB regardless the value of K. In this sense, the last stage of the *corrected*-2 structure is designed and implemented only one time in the decimator design process.

4.7.1 VHDL Implementation

In order to verify the performance of the *corrected*-2 structure, it has been implemented at the register transfer level in VHDL, taking as a reference a Spartan 3E FPGA device from

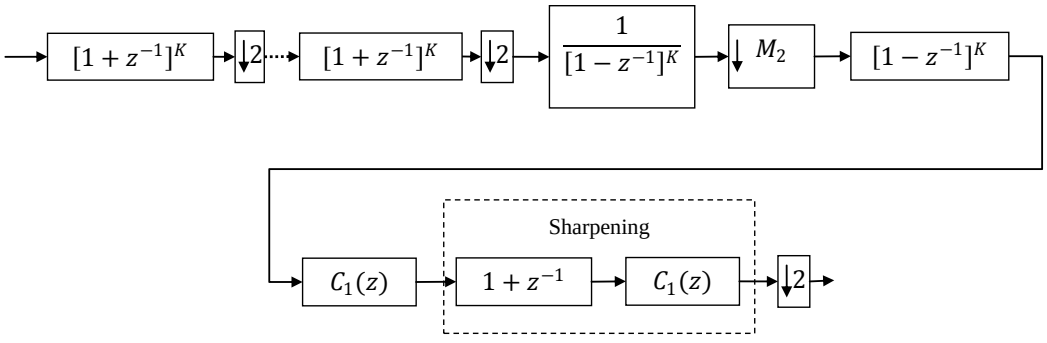
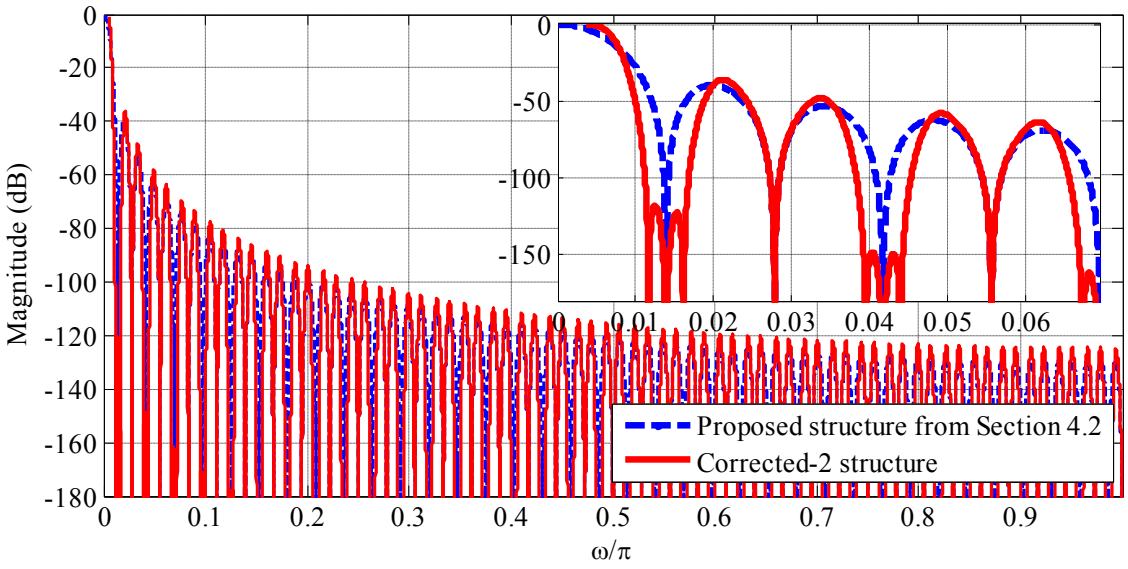
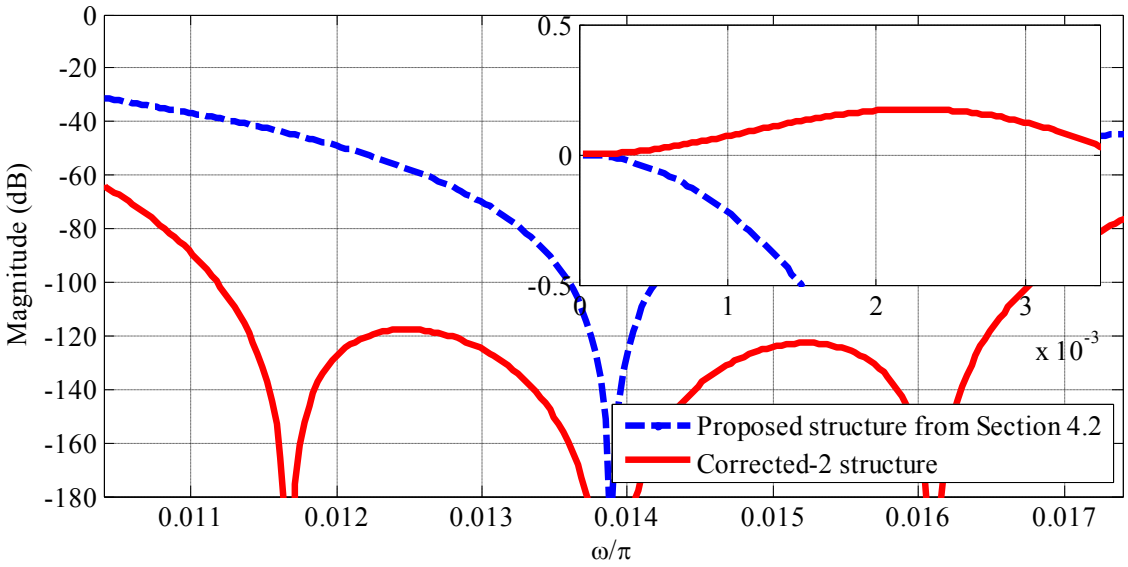


Fig. 4.25 *Corrected*-2 structure.



(a)



(b)

Fig. 4.26. Magnitude response of corrected-2 and proposed structure from section 4.2 (M = 144 and K=3): (a) Overall, (b) first folding band and passband.

Xilinx. In this case it has been considered a second-order continuous-time low-pass Sigma-Delta Modulator (ΣΔM) with 1-bit in the embedded quantizer. The sampling frequency of the modulator is fixed at 100MHz, thus an input sine tone of 390,625 Hz is oversampled 128 times, i.e. M = 128. Additionally, the amplitude of the sine tone is half of the full scale of the modulator, which is -6dB, Fig. 4.28(a) illustrates the output spectra of the modulator output. In order to decimate this signal it is considered the use of the *corrected*-2 structure

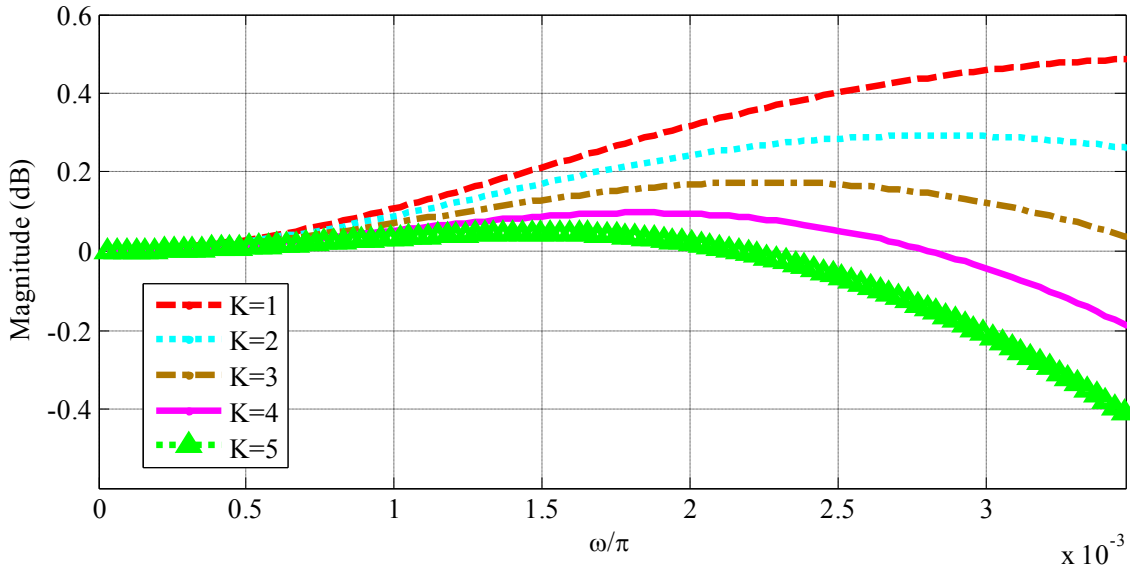


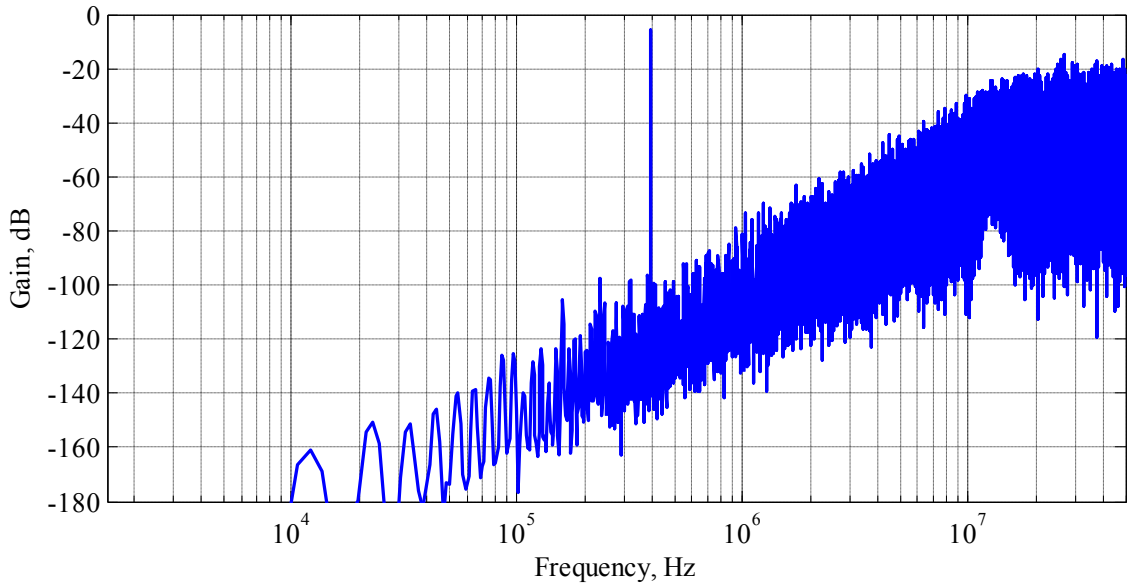
Fig. 4.27. Magnitude response in the passband of corrected-2 structure, considering different values of *K*.

with K = 3 and R = 2, Fig. 4.28(b) illustrates the output spectra for *corrected*-2 structure and the proposed structure from section 4.2. Additionally, Fig 4.28(b) also presents a zoom in the peak of the sine tone, where it can be seen that the *corrected*-2 structure compensates for the passband droop, of about -2.75dB. From Fig. 4.28(b) it can be also appreciated that the quantization noise is slightly lower in the *corrected*-2 structure due to the odd folding bands attenuations improvements.

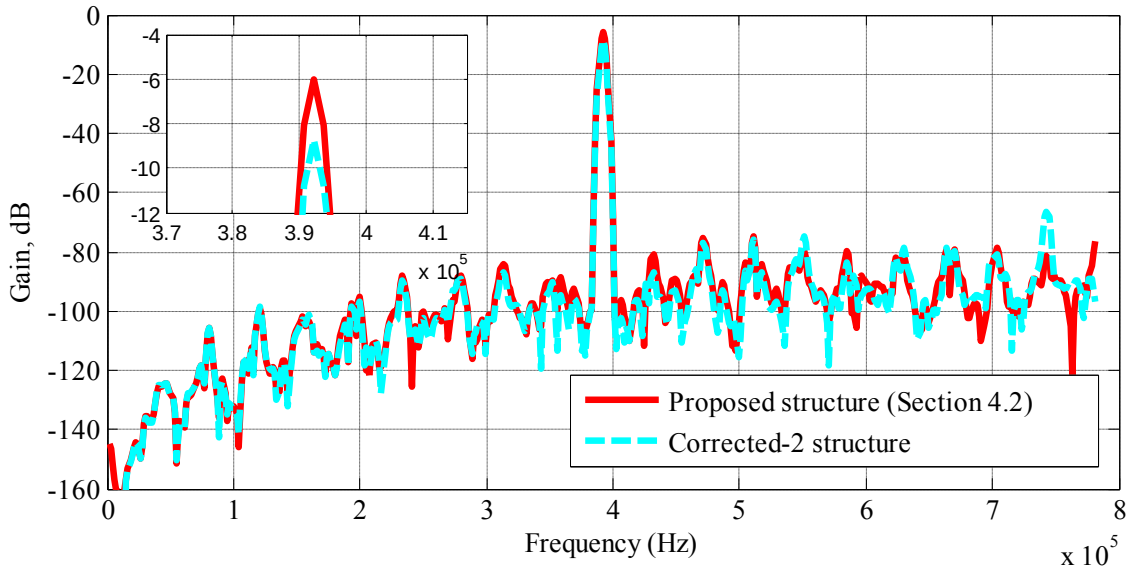
The simulated power consumption of *corrected*-2 structure and proposed structure from Section 4.2 are 12 and 9mW, respectively. On the base of the implementation results, it can be noticed that *corrected*-2 structure achieves improvement in both passband droop and quantization noise attenuation compared with the proposed structure from Section 4.2. The aforementioned improvements are at the cost of 33.3% increase in the power consumption.

4.8 Conclusions

In this chapter, power and area estimations for non-recursive comb structure and CIC structure have been presented. On the base of these estimations, a new two-stage comb-based structure has been proposed, where the first stage is a non-recursive comb structure (decimating by M_1) and the second stage is a CIC structure (decimating by M_2). By



(a)



(b)

Fig. 4.28 Output spectra of (a) ΣΔM and (b) *corrected*-2 structure and proposed structure from Section 4.2.

considering that $M = M_1M_2 = 2^P$, a design methodology for the best value for M_1 and M_2 has been also presented. As a result, the obtained two-stage structure efficiently combines the low power characteristic of non-recursive comb structure and the low silicon area characteristic of the CIC structure, provided that the decimation factor is a high power of two value.

The proposed two-stage structure has been slightly modified to cope with decimation factors that are even numbers. As a result, several structures have been identified, showing reduced power consumption when compared with the CIC structure, especially for $M \geq 100$. This power efficiency comes at the expense of a slight area increase, being about 10% in the best of the cases.

It has been determined that for practical application in ΣΔM, the *polyphase*-4 structure is the best option for decimation factors that are multiples of three and powers of three.

Simple modified structures with increased number of cascaded filters in the last stage have been introduced to improve the magnitude response in the folding bands without severally penalizing the power and area efficiency of the original structures.

Based on the use of corrector filters, corrected structures have been derived in order to simultaneously increase the attenuation in the folding bands and compensate for the passband droop.

VHDL implementations in both FPGA and 0.18μm CMOS technology been presented in order to validate the power and area efficiency of the proposed structures compared with the traditionally used non-recursive comb structure and CIC structure. In this way, the proposed two-stage structures constitute an efficient way to decimate signals in SDRs, where OSRs can have a high value and good magnitude response characteristics are desirable.

Finally, although all the presented structures, examples and implementations have focused on LP applications, it can also be applied to BP ΣΔM because the LP decimators are the most important part in DDCs.

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Chapter 5

Conclusions and Future Work

5.1 Conclusions

One objective of this thesis was the design of widely tunable LC-based BP CT-ΣΔMs. This objective has been met by proposing the *notch-aware* synthesis methodology, which considers the loop filter variations at the very beginning of the synthesis process and compensates for STF variations. This methodology has effectively increased the tuning rage of LC-based BP CT-ΣΔMs from $0.1f_s$ to $0.4f_s$ independently of the considered feedback DAC type: namely RZ, NRZ and RCos.

Among all the twelve widely tunable LC-based BP CT-ΣΔMs under study, the BPΣΔ-B topology with NRZ DAC and multi-bit quantizer ($B \geq 2$) is the best solution for the target f_n tuning range, since it is the most robust topology to circuit error mechanism, and it has lower estimated power than other topologies. Additionally, hybrid and passive loop filter realizations of the BPΣΔ-B topology with NRZ DAC have been investigated, which are feasible alternatives to reduce the power consumption.

Time-domain simulations considering system-level behavioral models in MATLAB have validated the presented approach. Additionally, circuit macromodels in Cadence-Spectre considering the BPΣΔ-B topology with NRZ DAC have demonstrated, with an example, that the presented modulator is able to convert three different cellular networks by using the notch reconfiguration.

Therefore, it has been demonstrated that it is possible to extend the covered RF signal range of LC-based BP CT-ΣΔMs by using the proposed *notch-aware* synthesis methodology. Apart from the necessary tunable feedback coefficients, the circuit complexity of the widely tunable LC-based BP CT-ΣΔMs is similar to those with a fixed f_n, since no additional feedback coefficients have been introduced to achieve the tunable operation. Similarly, the required compensation factor k, compensating STF variations, does not represent a significant complexity increase in the overall widely tunable LC-based BP CT-

ΣΔMs. Thus, the proposed design methodology and some studied modulators represent a good solution for the implementation of next-generation RF-to-digital converters for true SDRs.

The second objective of this thesis was the design of low power comb-based decimators with improved frequency responses in order to efficiently use them in LC-based BP CT-ΣΔMs. This objective has been met by proposing a two-stage comb-based decimator structure along with the corresponding design methodology to configure it as a power and area efficient decimator.

Several two stage structures that meet different design criteria, specially focused on power and area efficiency, have been identified. The structure for decimation factors that are a power of two combines the low power characteristic of non-recursive comb structure and the low silicon area characteristic of the CIC structure. *Direct*-1 to *Direct*-3 and their corresponding polyphase representations, being intended for even decimation factors, use less power than the corresponding CIC, but at the expense of a small area increase.

Based on the use of corrector filters, corrected structures have been derived in order to simultaneously increase the attenuation in the folding bands and compensate for the passband droop at a non-significant power consumption increase.

VHDL implementations in both FPGA and 0.18μm CMOS technology have been presented in order to validate the power and area efficiency of the proposed decimators compared with the traditionally used non-recursive comb structure and CIC structure. In this way, the proposed two-stage structures constitute an efficient way to decimate signals in SDRs, where high decimation factors and good magnitude response characteristics are needed.

5.2 Limitations

Probably the major limitation in the synthesized tunable LC-based BP CT-ΣΔMs is in the tuning range below $0.25f_s$, where modulators consume more power and are more sensitive to element variations. Additionally, allocating RF signals below $f_n = f_s / 4$ implies sampling

frequencies higher that fourth times the incoming signal, leading to a less efficient RF-to-Digital conversion.

The major limitation in all the two-stage decimation structures is the necessity of high decimation factors in order to take advantage of the power and area efficiency. High decimation factors are frequent in old cellular networks such as GSM, where the signal bandwidth is relatively small compared with the sampling frequency. However, newer cellular networks such as LTE are demanding higher bandwidth - which means lower decimation factors. As a consequence the power and area efficient structures could be out of function as the bandwidths demands continue increasing, provided that the sampling frequency remains unchanged.

5.3 Future work

Implement user programmable resonator gains over the *notch-aware* synthesis of widely tunable LC-based BP CT-ΣΔMs, meaning that the resonator gain can be different to ω. This additional degree of freedom could be used to translate the tunable operation to the resonators gain, giving less loop-filter coefficient variations: thus, improving robustness and power efficiency especially for the case $f_n \leq 0.25 f_s$.

Apply the multiplier-free concept to polyphase proposed structures in order to further reduce both power and area requirements when 1-bit ΣΔM streams are considered. This in turn could extend the covered decimation factors to lower values ($M < 50$): thus, avoiding the major limitation of proposed structures.

Appendix A

This appendix shows how to apply the *notch-aware* synthesis method to three LC-based BP CT-ΣΔM with FIR-based RZ DAC (Fig. 3.1), FIR-based NRZ DAC (Fig. 3.9) and FIR-based RCos DAC (Fig. 3.9). Additionally, MATLAB® scripts, which automatically compute the feedback coefficients, are provided.

A.1 LC-based BP CT-ΣΔM with FIR-based RZ DAC

The first step consists of deriving the modified *Z*-transforms, *Hci* (*z, v*), for each branch of Fig. 3.1. To this end, the well-known symbolic computational software Mathematica® [1] was used, resulting in the following expression:

$$H_{C_i}(z,v) = \frac{c_i z^{-1} \cdot \sum_{p=1}^{4} n_{ip}(v) z^{-p}}{1 + e^{\frac{-2j\pi}{v}} z^{-2} + 2\cos(\pi/v) \cdot (z^{-1} + z^{-3}) + z^{-4}} \qquad (A.1)$$

$$\begin{aligned}
n_{11}(v) = n_{24}(v) = n_{14}(v) \cdot \left(-e^{\frac{j\pi}{v}} + e^{\frac{j3\pi}{2v}} - e^{\frac{j2\pi}{v}}\right) \\
n_{12}(v) = n_{23}(v) = n_{14}(v) \cdot \left(1 - e^{\frac{j\pi}{2v}} + e^{\frac{j\pi}{v}} + e^{\frac{j3\pi}{2v}} + e^{\frac{j2\pi}{v}} - e^{\frac{j5\pi}{2v}} + e^{\frac{j3\pi}{v}}\right) \\
n_{13}(v) = n_{22}(v) = n_{14}(v) \cdot \left(-e^{\frac{j\pi}{2v}} - e^{\frac{j\pi}{v}} + e^{\frac{j3\pi}{2v}} - e^{\frac{j2\pi}{v}} - e^{\frac{j5\pi}{2v}}\right) \\
n_{14}(v) = n_{21}(v) = -e^{\frac{-3j\pi}{2v}} \cdot \sin\left(\frac{\pi}{2v}\right) \\
n_{31}(v) = n_{44}(v) = n_{34}(v) \cdot \left(-2e^{\frac{j\pi}{2v}} + e^{\frac{j\pi}{v}} - 2e^{\frac{j3\pi}{2v}}\right) \\
n_{32}(v) = n_{43}(v) = n_{34}(v) \cdot \left(1 + 3e^{\frac{j\pi}{v}} + e^{\frac{j2\pi}{2v}}\right) \\
n_{33}(v) = n_{42}(v) = -n_{34}(v) \cdot \left(-1 + 2e^{\frac{j\pi}{2v}} - 3e^{\frac{j\pi}{v}} + 2e^{\frac{j3\pi}{2v}} - e^{\frac{j2\pi}{v}}\right) \\
n_{34}(v) = -n_{41}(v) = -\frac{\pi}{4v} \cdot e^{\frac{-j\pi}{v}} \cdot \sin\left(\frac{\pi}{2v}\right)
\end{aligned} \qquad (A.2)$$

Therefore, using (A.1) and (A.2), and after expanding it in a partial-fraction form like that shown in (3.7), the equation in (3.9) can be solved numerically to get a direct relationship

between the modulator loop-filter coefficients, *ci*, and the relative notch frequency parameter, *v*. This procedure is implemented in the MATLAB® script shown below.

```
%Calculation of the loop coefficients for the LC-based BP CT-SDM
%presented in Fig. 3.1 of this thesis.

clear all

fs=4e9;                                 %Modulator's Sampling frequency.
fi=1e9;                                 %Input frequency.
Ts=1/fs;                                %Sampling time.
notch= fi/fs;                           %Relative notch frequency.

M=128;                                  %Oversampling Ratio for the
delsigToolbox (This field is taken into account only when we speficy the
optimization of the zeros in the NTF)
H = synthesizeNTF(4,M,0,1.5,notch);     %NTF del modulador
y=tf(1-1/H);                            %Loop Filter
[num,den] = tfdata(y,'v');              %Loop Filter in Vector Form
v=1/(2*notch);                          %variable that acounts for the DR
compensation
w=pi/v;                                 %Normalized frequency of the LC-
filter

% Computation of H_c1(z,v) to Hc4(z,v) (Derived in Mathematica)

a=real (0.5*i*exp(-2*i*pi/v)*(-1 + exp(pi*i/v))*( -exp(pi*i/v) +
exp(3*pi*i/(2*v)) -exp(2*pi*i/v)));
b=real (0.5*i*exp(-2*pi*i/v)*(-1 + exp(i*pi/v))*(1 - exp(i*pi/(2*v)) +
exp(i*pi/v) + exp(3*i*pi/(2*v)) + exp(2*i*pi/v) - exp(5*i*pi/(2*v)) +
exp(3*i*pi/v)));
c=real (0.5*i*exp(-2*pi*i/v)*(-1 + exp(i*pi/v))*( -exp(i*pi/(2*v)) -
exp(i*pi/v) + exp(3*i*pi/(2*v)) - exp(2*i*pi/v) - exp(5*i*pi/(2*v))));
d=real (0.5*i*exp(-i*pi/(2*v))*(-1 + exp(pi*i/v)));

e=real (i*exp(-3*i*pi/(2*v))*(-1 + exp(pi*i/v))*(-2*exp(i*pi/(2*v)) +
exp(i*pi/v) - 2*exp(3*i*pi/(2*v)))*pi/(8*v));
f=real ((i*exp(-3*i*pi/(2*v)))*(-1 + exp(pi*i/v))*(1 + 3*exp(pi*i/v) +
exp(2*pi*i/v))*pi/(8*v));
g=real ((i*exp(-3*i*pi/(2*v)))*(-1 + exp(pi*i/v))*( -1 +
2*exp(i*pi/(2*v)) - 3*exp(pi*i/v) + 2*exp(3*i*pi/(2*v)) -
exp(2*pi*i/v))*pi/(8*v));
h=- real ((i*exp(-i*pi/(2*v)))*(-1 + exp(pi*i/v))*pi/(8*v));

%Numerators of Hc1 to Hc4 in vector form
Hc1_z=[a b c d];
Hc2_z=[-d -c -b -a];
Hc3_z=[e f g h];
Hc4_z=[h g f e];

%Partial fraccions expansion of Hc1 to Hc5
```

```
[r1,p1,k1] = residue(Hc1_z,[den 0]);
[a1,b1] = residue(r1(1:4),p1(1:4), k1);

[r2,p2,k2] = residue(Hc2_z,[den 0]);
[a2,b2] = residue(r2(1:4),p2(1:4), k2);

[r3,p3,k3] = residue(Hc3_z,[den 0]);
[a3,b3] = residue(r3(1:4),p3(1:4), k3);

[r4,p4,k4] = residue(Hc4_z,[den 0]);
[a4,b4] = residue(r4(1:4),p4(1:4), k4);

%Coefficients determination
%Matrix of coefficients definition
matrix_coeff=real([a1(1) a2(1) a3(1) a4(1);a1(2) a2(2) a3(2) a4(2); a1(3)
a2(3) a3(3) a4(3); a1(4) a2(4) a3(4) a4(4)]);
dt=[num(2);num(3);num(4);num(5)];        %Discrete time numerator.
ci=matrix_coeff\dt;                      %Coefficient's determination.


%Coefficients for the modulator in Fig. 3.1.
c1=ci(1);
c2=ci(2);
c3=ci(3);
c4=ci(4);

c0=-(r1(5)*c1+r2(5)*c2+r3(5)*c3+r4(5)*c4); % ELD compensation coeficient

k=0.25/w^2;  %Equialization factor.in Fig. 6(a)

%Note how the main coefficientes c1-c4 are computed firts, and the
%compesation coefficient c0 depens upon the additional terms
%introduced due to exces loop delay of one full sampling clock period.
```

A.2 LC-based BP CT-ΣΔM with FIR-based RCos DAC

The MATLAB® routine used to synthesize the loop-filter coefficients of BP CT-ΣΔMs with FIR-based RCos DACs, like that shown in Fig. 3.9, is similar to that used for RZ DACs. The main difference lies in the expression derived for the modified *Z*-transform of *Hci* (*s*, *v*), which strongly depends on the feedback DAC waveform, being more complex in the RCos case with more compensation coefficients, $c_{0\text{-}1}$, used to cancel the effect of ELD. The script for the synthesis of this modulator is presented in the following.

```
%Calculation of the coefficients of a LC-based 4th-order BP CT-SDM %
%with variable notch frequency, RCos-DAC ( by Gerardo Molina Salgado)%

clear all
```

```
fs=4e9;                                 %Modulator's Sampling frequency.
fi=1e9;                                 %Input frequency.
Ts=1/fs;                                %Sampling period.
notch= fi/fs;                           %Relative notch frequency.
M=128;                                  %Oversampling Ratio.
H = synthesizeNTF(4,M,0,1.5,notch);     %NTF of the DT BP-SDM with delsig
                                        %Toolbox [22]
y=tf(1-1/H);                            %DT Loop Filter
[num,den] = tfdata(y,'v');              %DT Loop Filter in Vector Form
v=1/(2*notch);                          %For calculation of Hci(z)
w=pi/v;                                 %Normalized freq. of the LC-filter


% Computation of H_c2(z,v) to Hc5(z,v) (Derived in Mathematica)

a=real(exp(-2*i*pi/v)*(-1 + exp(i*pi/v))*v*(2*v*exp(i*pi/v)-
2*v*exp(2*i*pi/v)-i*pi*exp(i*pi/v)*(-1+4*v^2)-i*pi*exp(2*i*pi/v)*(-
1+4*v^2))/(1-4*v^2)^2);
b=real(exp(-2*i*pi/v)*(-1 + exp(i*pi/v))*v*(-2*v + 4*exp(i*pi/v)*v-
4*exp(2*i*pi/v)*v + 2*exp(3*i*pi/v)*v + i*pi*exp(i*pi/v)*(-1+4*v^2) +
i*pi*exp(2*i*pi/v)*(-1+4*v^2))/(-1+4*v^2)^2);
c=real(0.5*exp(-2*i*pi/v)*v*(-4*exp(4.71239*i/v)*v - 8*exp(2*i*pi/v)*v -
4*exp(7.8539*i/v)*v + i*pi*exp(4.71239*i/v)*(-1 + 4*v^2) -
i*pi*exp(7.8539*i/v)*(-1+4*v^2))/(1-4*v^2)^2);
d=real(0.5*exp(-2*i*pi/v)*v*( 16*exp(pi*i/v)*v + 12*exp(4.71239*i/v)*v +
12*exp(7.8539*i/v)*v + 16*exp(3*pi*i/v)*v + exp(10.9956*i/v)*(i*pi + 4*v
- 12.5664*i*v^2) + exp(1.5708*i/v)*(-i*pi + 4*v + 12.5664*i*v^2) +
i*pi*exp(4.71239*i/v)*(-1 + 4*v^2) - i*pi*exp(7.8539*i/v)*(-1+4*v^2))/(1-
4*v^2)^2);
e=real(0.5*exp(-2*i*pi/v)*v*(-8*v - 16*exp(3*pi*i/(2*v))*v -
32*exp(2*i*pi/v)*v - 16*exp(5*pi*i/(2*v))*v - 8*exp(4*pi*i/v) -
2*exp(7*pi*i/(2*v))*(i*pi + 4*v -4*pi*i*v^2)- 2*exp(pi*i/(2*v))*(-i*pi +
4*v + 4*pi*i*v^2) - 4*pi*i*exp(3*pi*i/(2*v))*(-1 + 4*v^2) +
4*pi*i*exp(5*pi*i/(2*v))*(-1 + 4*v^2))/(1-4*v^2)^2);

f=real((2*i*exp(-i*pi/v)*v^2 - 2*i*exp(i*pi/v)*v^2)/(-1+4*v^2));
g=real((-2*i*exp(-i*pi/v)*v^2 + 2*i*exp(i*pi/v)*v^2 +
2*i*exp(2*i*pi/v)*v^2 - 2*i*exp(-2*i*pi/v)*v^2)/(-1+4*v^2));
m=real((-2*i*exp(-i*pi/(2*v))*v^2 + 2*i*exp(i*pi/(2*v))*v^2)/(-1+4*v^2));
n=real((2*i*exp(-i*3*pi/(2*v))*v^2 - 2*i*exp(-i*pi/(2*v))*v^2 +
2*i*exp(i*pi/(2*v))*v^2 - 2*i*exp(i*3*pi/(2*v))*v^2)/(-1+4*v^2));


%Numerators of Hc1 to Hc4 in vector form
Hc4_z=[a b b a];
Hc5_z=[c d e d c];

Hc2_z=[f g -g -f];
Hc3_z=[-m -n 0 n m];


%Partial fraction expansion of Hc2(z) to Hc5(z).
```

```
[r2,p2,k2] = residue(Hc2_z,[den 0 ]);        %Partial fraction expansion
of H2
[a2,b2] = residue(r2(1:4),p2(1:4), k2);

[r3,p3,k3] = residue(Hc3_z,[den 0 0 ]);      %Partial fraction expansion
of H3
[a3,b3] = residue(r3(1:4),p3(1:4), k3);

[r4,p4,k4] = residue(Hc4_z,[den 0]);         %Partial fraction expansion
of H4
[a4,b4] = residue(r4(1:4),p4(1:4), k4);

[r5,p5,k5] = residue(Hc5_z,[den 0 0 ]);      %Partial fraction expansion
of H5
[a5,b5] = residue(r5(1:4),p5(1:4), k5);

%Coefficients determination
%Matrix of coefficients definition
matrix_coeff=real([a2(1) a3(1) a4(1) a5(1); a2(2) a3(2) a4(2) a5(2);
a2(3) a3(3) a4(3) a5(3) ; a2(4) a3(4) a4(4) a5(4)]);% ELD and notch
Compensation
dt=[num(2);num(3);num(4);num(5)];         %Discrete time numerator
ci=matrix_coeff\dt;                       %Coefficients Determination

%Coefficients for the modulator in Fig. 10(a).
c2=ci(1);
c3=ci(2);
c4=ci(3);
c5=ci(4);

c0=-(r2(5)*c2 + r3(5)*c3 + r4(5)*c4 + r5(5)*c5)/2; %Compensation coeff.
c1=-(r3(6)*c3 + r5(6)*c5)/2;

k=0.25/w^2  %Equialization factor.

%Note how the main coefficientes c2-c5 are computed firts, and the
%compesation coefficients c0 and c1 depens upon the additional terms
%introduced de to exces loop delay of one full sampling clock period.
```

A.3 LC-based BP CT-ΣΔM with FIR-based NRZ DAC

Finally, the synthesis of LC-based BP CT-ΣΔMs with a feedback FIR-based NRZ DAC, like that shown in Fig. 3.8(a), can be done by using the c2d function of MATLAB® in order to compute the *Z*-transform of each feedback path. Therefore, there is no need to obtain an analytic expression for *Hci* (*z, v*) like that shown in (A.1)-(A.2). The rest of the

synthesis procedure is the same as that used for RZ DACs and RCos DACs. The corresponding MATLAB® script is as follows:

```
%Calculation of the loop coefficients for the LC-based BP CT-SDM
%presented in Fig. 3.1 of this thesis.


fs=4e9;                                 %Modulator's Sampling frequency.
fi=1e9;                                 %Input/carrier frequency.
Ts=1/fs;                                %Sampling period.
notch= fi/fs;                           %Relative notch frequency.
M=128;                                  %Oversampling Ratio.
H = synthesizeNTF(4,M,0,1.5,notch);     %NTF of the DT BP-SDM with delsig
                                        %Toolbox [22].
y=tf(1-1/H);                            %DT Loop Filter.
[num,den] = tfdata(y,'v');              %DT Loop Filter in Vector Form.
v=1/(2*notch);                          %For calculation of Hci(z).
w=pi/v;                                 %Normalized freq. of the LC-
filter.


%Definition of Hc2(s,v) to Hc5(s,v)

Hc2_s = tf([w 0], [1 0 w^2]);                                   %Non-delayed
Hc3_s = tf([w 0], [1 0 w^2], 'inputdelay', 0.5);                %Delayed
Hc4_s = tf([w^2 0 0], [1 0 2*w^2 0 w^4]);                       %Non-delayed
Hc5_s = tf([w^2 0 0], [1 0 2*w^2 0 w^4], 'inputdelay', 0.5); %Delayed

%Hc2(z,v) to Hc5(z,v) by using 'c2d' function of the Control toolbox (R)

Hc2_z = c2d(Hc2_s, 1);                  %Discretisation of Hc2_s
Hc3_z = c2d(Hc3_s, 1);                  %Discretisation of Hc3_s
Hc4_z = c2d(Hc4_s, 1);                  %Discretisation of Hc4_s
Hc5_z = c2d(Hc5_s, 1);                  %Discretisation of Hc5_s


[numc2,denc2] = tfdata(Hc2_z,'v');      %Vector form of Hc2_z
[numc3,denc3] = tfdata(Hc3_z,'v');      %Vector form of Hc3_z
[numc4,denc4] = tfdata(Hc4_z,'v');      %Vector form of Hc4_z
[numc5,denc5] = tfdata(Hc5_z,'v');      %Vector form of Hc5_z

H4=[numc4(2) numc4(3) numc4(4) numc4(5)];           %Numerator of Hc4_z,
H5=[numc5(1) numc5(2) numc5(3) numc5(4) numc5(5)];  %Hc5_z,
H2=conv(numc2,denc2);                               %Hc2_z, and
H3=conv(numc3,denc3);                               %Hc3_z in vector form

%Partial fraction expansion of Hc2(z) to Hc5(z).


[r2,p2,k2] = residue(H2,[den 0 ]);        %Partial fraction expansion of
H2
[a2,b2] = residue(r2(1:4),p2(1:4), k2);
```

```
[r3,p3,k3] = residue(H3,[den 0 0 ]);      %Partial fraction expansion of
H3
[a3,b3] = residue(r3(1:4),p3(1:4), k3);

[r4,p4,k4] = residue(H4,[den 0]);         %Partial fraction expansion of
H4
[a4,b4] = residue(r4(1:4),p4(1:4), k4);

[r5,p5,k5] = residue(H5,[den 0 0 ]);      %Partial fraction expansion of
H5
[a5,b5] = residue(r5(1:4),p5(1:4), k5);

%Coefficients determination
%Matrix of coefficients definition
matrix_coeff=real([a2(1) a3(1) a4(1) a5(1); a2(2) a3(2) a4(2) a5(2);
a2(3) a3(3) a4(3) a5(3) ; a2(4) a3(4) a4(4) a5(4)]);% ELD and notch
Compensation
dt=[num(2);num(3);num(4);num(5)];             %Discrete time numerator
ci=matrix_coeff\dt;                           %Coefficients Determination

%Coefficients for the modulator in Fig. 9(a).
c2=ci(1);
c3=ci(2);
c4=ci(3);
c5=ci(4);

c0=-(r2(5)*c2 + r3(5)*c3 + r4(5)*c4 + r5(5)*c5);
c1=-(r3(6)*c3 + r5(6)*c5);

%Note how the main coefficientes c2-c5 are computed firts, and the
%compesation coefficients c0 and c1 depens upon the additional terms
%introduced due to exces loop delay of one full sampling clock period.

k=0.25/w^2;  %Equialization factor.
```