An Aware Methodology to Evaluate Circuit Testability for Small Delay Defects

By

José Luis García Gervacio

A Dissertation submitted in partial fulfillment of the requirements for the degree of
Doctor on Science with Major on Electronics
at the
National Institute for Astrophysics, Optics and Electronics

Thesis Advisor:
Dr. Víctor Hugo Champac Vilela
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Summary

In this work, an aware methodology to evaluate circuit testability for small delay defects due to resistive open and bridge defects in the presence of process variations has been proposed. The circuit testability has been evaluated analyzing the timing information of the circuit. Statistical timing analysis is used to propagate the signal delay through the logic levels until the primary outputs are reached. Then, the outputs of the defect-free circuit and those of the defective one are compared to determine the fault coverage of the circuit. This is used as the circuit testability metric. The methodology is applied to some ISCAS-85 benchmark circuits.

In the first chapter, state of the art issues involving circuit testability due to small delay defects are presented. Interconnect defects on nanometer technologies such as: resistive opens and resistive bridges are described. The main causes for the occurrence of interconnect defects during the manufacturing process are given. Process parameter variations during the manufacture process are analyzed. Their impact of correlation on circuit delay is outlined. State of the art on test strategies for timing defects is also presented, such as: delay test techniques, test parameter conditions and small delay defect test. Statistical timing analysis issues are discussed such as with the main subjects: problem formulation, challenges in statistical static timing analysis and solution approaches.

In the second Chapter, the implementation of our Statistical Timing Analysis Framework (STAF) is presented. The most important issues in nanometer technologies were considered in the framework. The modeling of the process variation was considered using a rectangular grid model. Using this model, inter-die and intra-die variations are taken into account simultaneously. The statistical timing analysis is done using levelized covariance propagation. ISCAS benchmark circuits were used to test the capabilities of the framework. Finally, circuit delay (mean and variance) is given for each circuit.

In the third Chapter, a methodology to evaluate circuit testability for small delay defects due to resistive opens in the presence of process variations is presented. An Statistical Timing Analysis Framework is used to propagate delay defects related to resistive open defects. Assessment and proposed resolution to the problem are given. An statistical methodology to estimate the probability of detection of resistive open defects is proposed. Using the probability of detection the statistical fault coverage (SFC) of the circuit is obtained. The SFC gives an indication of the circuit testability for open defects. The methodology is applied to some ISCAS-85 benchmark circuits.

In the fourth Chapter, a methodology to evaluate circuit testability for small delay defects due to resistive bridges in the presence of process variations is presented. A Statistical Timing Analysis Framework is used to propagate delay defects related to bridge defects. A statistical methodology to estimate the probability of detection of bridge defects is proposed. Using the probability of detection the SFC of the circuit is obtained.

In the fifth Chapter, a methodology to reduce the number of simulated faults to estimate the fault coverage of the circuit is presented. The fault coverage gives a measurement of the circuit testability. Resistive open defects and resistive bridge defects are considered. Stratified random sampling is used to reduce time computation because their efficiency. Using the proposed methodology, the stratified SFC of resistive open and bridge defects producing small delays is evaluated for some ISCAS benchmark circuits.

Finally, the conclusions of the thesis are given in the sixth Chapter.

Resumen

En este trabajo se ha propuesto una metodología para evaluar la capacidad de prueba de un circuito para defectos de retardo pequeño como aberturas resistivas y puentes con la presencia de variaciones de proceso. La capacidad de prueba del circuito se ha evaluado analizando la información de tiempo del circuito. Un análisis estadístico de tiempo es utilizado para propagar el retardo de la señal a través de los niveles lógicos hasta llegar a las salidas primarias. Posteriormente, los resultados del circuito libre de defecto y los del circuito con defecto se comparan para determinar la cobertura falla del circuito. Este se utiliza como una métrica de la capacidad de prueba del circuito. La metodología es aplicada en algunos circuitos ISCAS.

En el capítulo primero se presenta el estado del arte sobre los tópicos relacionados con la capacidad de prueba del circuito para defectos de retardo pequeo. Se describen los defectos de interconexión en tecnologías nanómetricas, tales como: aberturas resistivas y puentes. También, se dan las principales causas de aparición de los defectos de interconexión durante el proceso de fabricación y se analizan las variaciones de proceso de los parámetros y sus fuentes de origen. Además, se describe el impacto de la correlación sobre el retardo del circuito. Se analiza el estado del arte sobre las estrategias de prueba para detectar defectos y se aborda el análisis estadístico con sus principales retos.

En el capítulo segundo se presenta la herramienta implementada para el análisis estadístico de tiempo (STAF). Las retos más importantes en tecnologías nanómetricas fueron considerados en la herramienta. La variación de proceso se tomo en cuenta con un modelo rectangular cuadriculado. Usando este modelo, variaciones del tipo inter-die e intra-die son considerados simultáneamente. El análisis estadístico de tiempo se realiza mediante la propagación nivelizada de la covarianza. Circuitos ISCAS se utilizaron para probar las capacidades de la herramienta.

En el capítulo tercero y cuarto se presenta una metodología para evaluar la capacidad de prueba de un circuito para defectos de aberturas y puentes resistivos con la presencia de variaciones de proceso, respectivamente. La herramienta para análisis estadístico es utilizado para propagar los retardos debido a defectos de abertura y puentes resistivos. Se propone una metodología estadística para estimar la probabilidad de detección de defectos de aberturas y puentes resistivos. La cobertura de falla estadística (SFC) del circuito es obtenida usando la probabilidad de detección. La SFC da una indicación de la capacidad de prueba del circuito para defectos de retardo pequeños. La metodología es aplicada en algunos circuitos ISCAS.

En el capítulo quinto se presenta una metodología para reducir el número de defectos simulados para estimar la cobertura de falla del circuito. Se consideran defectos de aberturas y puentes resistivos. Un muestreo aleatorio estratificado es utilizado para reducir el tiempo de computo debido a su eficiencia. Usando la metodología propuesta, la SFC estratificada se evalúa para algunos circuitos ISCAS.

Por último, las conclusiones de la tesis se presentan en el capítulo sexto.

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To my fried Claudia Juarez
for her unconditional support with the CAD tools.

To **GOD** for give me health and forces to follow ahead..

Dedications

To my sweet and loved wife

Gina

.

To my dear parents:

Nélida y Domingo

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To my family who always has believed in me.

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Contents

Preface

In a demanding world where the people are looking for comfort in the electronic products, as well as, industrial, military and space customers push for more advanced products, electronic research on semiconductors has become a priority in the development of the countries. This implies, manufacture electronic products with higher performance and reliability. These electronic products have their base on integrated circuits. Therefore, there is a continuos demand for better performance requirements for integrated circuits. Some of these requirements are: faster processing of the information, lower power consumption, smaller area; all at a lower cost. This has lead to more complex designs, affecting the reliability and the yield. To accomplish with these requirements, a fast shrink in the critical dimensions of the devices and of the interconnects have been part of this difficult task. Critical dimensions are more significantly affected by manufacturing process variations. As design sizes and performance increase, more and more circuit nodes will be susceptible to a delay defects. Delay defects refer to any type of physical defect that adds enough signal-propagation delay in a circuit to produce an invalid response when the circuit operates at the targeted frequency. Furthermore, experimental data over the last two decades has shown that the failure distribution due to delay defects is skewed towards smaller delays. This data consistently indicates that the majority of circuits that fail due to delay-related defects fail due to delay defects smaller than the typical clock cycle times for the respective technology node. Targeting small delay defects (SDDs) during test improves defect coverage and lowers the test escape rate, avoiding reliability problems in short time of the product.

In this work an aware methodology to evaluate circuit testability for small delay defects in the presence of process variations is proposed. Small delay defects due to resistive opens and resistive bridges are considered. An Statistical Timing Analysis Framework is used to propagate the delay defects related to resistive open and bridge defects. An statistical methodology to estimate the probability of detection of these defects is proposed. The statistical fault coverage

(SFC) of the circuit can be calculated using the probabilities of detection of the defects. Using the proposed methodology, the SFC of interconnect defects producing small delays is evaluated for some ISCAS-85 benchmark circuits. The SFC is a metric of the circuit testability for small delay defects due to resistive open and bridge defects.

Acronyms

CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuit
VLSI	Very Large Scale Integration
STA	Static Timing Analysis
DSTA	Deterministic Static Timing Analysis
SSTA	Statistical Static Timing Analysis
PDF	Probability Distribution Function
CDF	Cumulative Distribution Function
RV	Random Variable
CMP	Chemical Mechanical Polish
CD	Critical Dimension
LER	Line-Edge Roughness
RDF	Random Dopant Fluctuation
SDD	Small Delay Defect
PCB	Printed Circuit Board
ATG	Automatic Test Generation
BIST	Built-In Self Test
STAF	Statistical Timing Analysis Framework
SFC	Statistical Fault Coverage
WRB	Weak Resistive Bridge
SRS	Simple Random Sampling
STRS	Stratified Random Sampling
CL	Confidence Level
ME	Margin of Error

Chapter 1

Introduction

In this Chapter, state of the art issues related with the circuit testability due to small delay defects are presented. Shrink in the dimensions of the devices has allowed better circuit performance. However, at the same time new issues affecting the reliability and yield have become a challenge. Critical dimensions have been affected by the manufacturing process. Therefore, subtle defects impacting the final operation of the circuits have become more important. Interconnect defects are an important source of defects encountered in circuits, these producing small delay faults may escape test. This Chapter is organized as follows: In Section 1.1, common defects on nanometer technologies are introduced. In Section 1.2, sources of timing variation, which affect the final operation of the product are presented. In Section 1.3, test strategies for timing defects are outlined. In Section 1.4, statistical timing analysis challenges and solution approaches are discussed. In Section 1.5, the justification of the present work is presented. Finally, in the Section 1.6, the organization of the present work is presented.

1.1 Defects on Nanometer Technologies

Digital circuits move to the next technology node driven by performance, power and cost (area, yield) improvement [1]. It was taken for granted that all these aspects improve moving to the next node. It meant that the same design would become cheaper, faster and more power efficient. However, this is not that obvious any more for the coming nodes [1]. Move to the next technology node also implies smaller critical dimensions, which means that the same logic function can be implemented in a smaller area. However, circuits implemented in smaller critical dimensions become more sensitive to defects (random and systematic defects), which may produce a yield loss and reliability problems [2][3][4][5].

In the past, two common interconnect defects in integrated circuits (ICs) have been opens and bridges [6]. This is expected to remain in nanometer circuits where the increasing number of metal layers leads particularly to a risk of open vias and metal bridges [7]. Nowadays, in nanometer technologies is common see shorts (bridges) and opens due to particles and spots, opens in vias and interconnection lines, silicidation problems, etc. In addition, new technologies introduce new defect types.

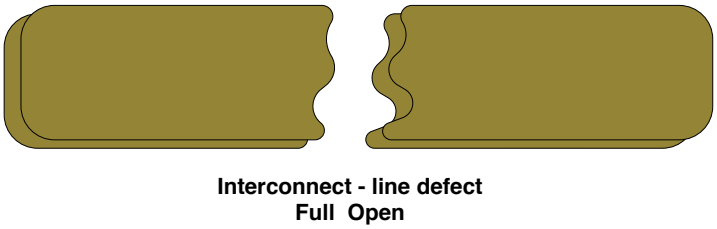
Next, open and bridge defects are described with more detail.

1.1.1 Resistive Open Defects

A full open in an interconnection occurs when the conductive material is completely broken. On the other hand, a resistive open appears when the conductive material is not completely broken. As a consequence an extra resistance (R_o) within the connection appears. The possible resistance values of the open can be in the range $0 < R_o < \infty$. Resistive open defects have considerably increased in recent technologies, due to the presence of many interconnection layers and an ever growing number of connections between each layer [8]. Intel reports that open/resistive vias are the most common root cause of test escapes in nanometer technologies [9]. Previous research classified opens into strong opens (R>10MΩ) and weak opens (R<10MΩ) [10]. The impact of open defects on circuit performance is a function of the location and size of the defect, as well as the electrical parameters of the circuits. Resistive weak open in a via and in an interconnect line are shown in Figure 1.1.

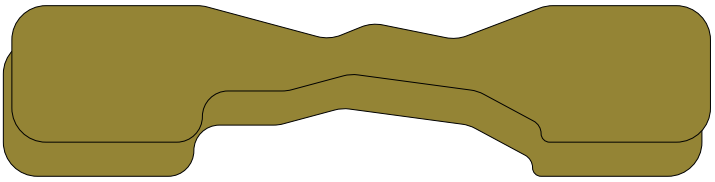
The main causes for the occurrence of interconnect open defects during the manufacturing process can be due to several factors, such as:

- the chemical mechanical polishing (CMP) (which is used to planarize metal lines) originating metal erosion and dishing,
- metal filling,
- spots during the lithography, which are undesired particles called spot defects.
- optical proximity effects which are a consequence of patterning features smaller that the wavelength of light,
- lens imperfections in the optical system,



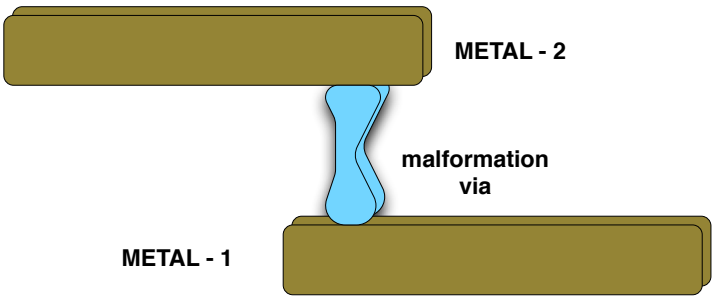
Interconnect - line defect
Full Open

(a)



Interconnect - line defect
Partial Open or Resistive Open

(b)



(c)

Figure 1.1: a) Full open in an interconnect line and Resistive Open in an b) interconnect line and c) via, due to manufacturing defects.

- metal density,
- silicide agglomeration,
- chemical slurry, and some others.

A typical via has a resistance of around 1Ω at 250nm but it has been observed that via opens often produce a high resistance connection, from a few ohms up to several kilo-ohms [11]. This problem appears to be more significant as the geometry shrinks. One cause is the etch and slurry residues in the now common damascene CMP approach to building multiple metal

layers. Although stress testing sometimes clears the problem it does not always do so [12]. As IC voltages fall the voltage stressing also it is reduced which make stress testing more difficult to be used. Resistive open combined with the circuit capacitance cause a signal delays. Such delays would not often be long enough to be caught by static tests. At-speed or delay-fault tests are required for good coverage of resistive opens [6][11][13].

1.1.2 Resistive Bridge Defects

Resistive bridges are common manufacturing defects [6]. Bridges (or shorts) occur when two or more distinct nodes of the circuit get connected due to a defect. Figure 1.2 shows a bridge (short) defect between two parallels interconnects lines.

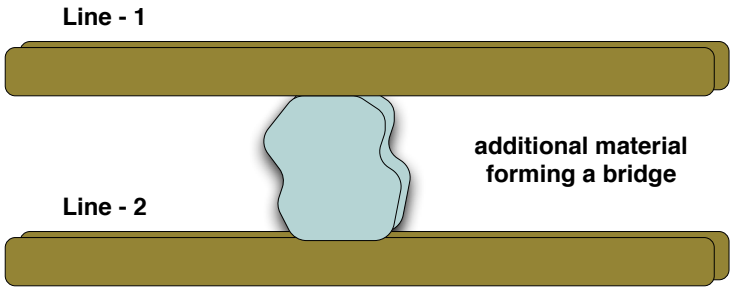


Figure 1.2: Defect forming an unintentional bridge between two parallel interconnect lines

As the opens case, the main causes for the occurrence of bridges during the manufacturing process can be due to different factors, such as:

- the chemical mechanical polishing (CMP)
- metal filling,
- spots during the lithography,
- optical proximity effects,
- lens imperfections in the optical system,
- metal density,
- conductive particle contamination,

- crack in the insulator,
- gate oxide defect causing pinhole, and some others.

Bridge's defects have an immeasurable effect on signal timing, unless the bridge impedance is in a sensitive range [6] [14]. For a particular bridge, the bridge resistance for which logic error occurs can be referred as the critical bridge resistance ($Rcrit$). Previous woks consider the critical bridge resistance ranges in 500Ω to 1000Ω [12][15][16]. The value of the critical resistance may depend mainly on their bridge position and on the drivers of the lines involved in the bridge. Bridges with resistances lower than the critical resistance may be detected with Boolean test based on the Stuck-at fault model. Resistances upper than the critical resistance are almost undetectable with a Boolean test [17][18] and more sophisticated tests are required. For this instance, the position of the bridge has a very small impact on the delay [15].

1.2 Process Variations

Process parameter variations during the manufacturing process have become an important issue in the performance on nanometer digital circuits. Process variations impact the maximum frequency at which the circuit can operate. Therefore, designers must know the sources of variation in order to fulfill the initial specifications. In this section, we describe the key sources of variation in timing prediction, that make timing analysis a challenging task for nanoscale digital circuits. We first describe different types of uncertainties that arise as a design moves from specification to implementation and final operation in the field. We then focus on process variations in more detail and explain the distinction between inter-die and intra-die variations and the source of so-called spatial correlations. Finally, the impact of different types of process variations on the timing of a circuit is given.

1.2.1 Model, Process, and Environmental Uncertainties

The uncertainty in the timing estimate of a design can be classified into three main categories [19]:

1. Modeling and analysis errors – modeling inaccuracy in device, in extraction and reduction of interconnect parasitics. Also in timing-analysis algorithms;

2. Manufacturing variations – uncertainty in the parameters of fabricated devices and interconnections from die to die and within a particular die;

3. Operating context variations – uncertainty in the operating environment of a particular device during its lifetime, such as temperature, supply voltage, mode of operation, and lifetime wear-out.

To illustrate each of these uncertainties, consider the stages of the design process, from initial specification to final operation, as shown in Figure 1.3.

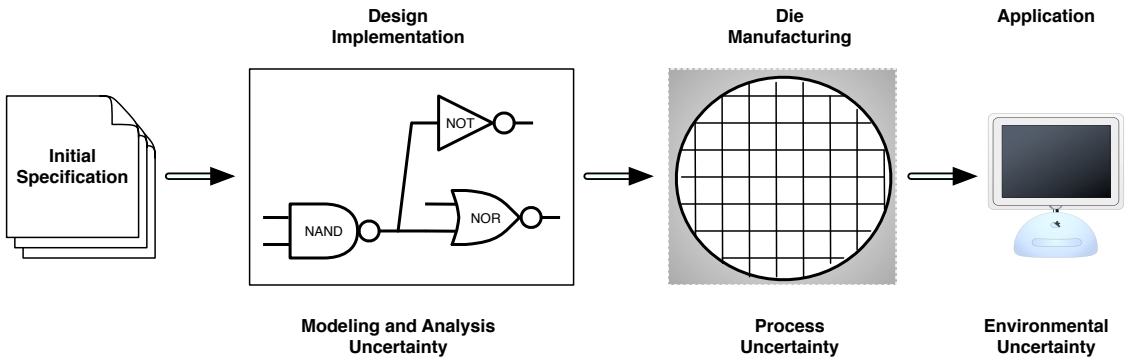


Figure 1.3: Stages of the design process and their resulting timing uncertainties

Since each of the three discussed variabilities represents orthogonal sample spaces, it is difficult to perform a combined analysis in a meaningful manner. Environmental uncertainty and uncertainty due to modeling and analysis errors are typically modeled using worst-case margins. However, uncertainty in the process is generally treated statistically. Hence, most Statistical Static Timing Analysis (SSTA) research works focus only on modeling process variations.

1.2.2 Sources of Process Variation

1. Physical Parameters, Electrical Parameters, and Delay Variation:

   The semiconductor manufacturing process has become more complex, at the same time process control precision is struggling to maintain relative accuracy with continued process scaling. As a result, a number of steps throughout the manufacturing process are prone to fluctuations [19]. These include effects due to chemical mechanical polishing

(CMP), which is used to planarize insulating oxides and metal lines, optical proximity effects, which are a consequence of patterning features smaller than the wavelength of light [20][21][22], and lens imperfections in the optical system. These, as well as other numerous effects, cause variation of device and interconnection physical parameters such as gate length (also called critical dimension-CD), gate-oxide thickness, channel doping concentration, interconnection thickness and height, etc., as shown in Figure 1.4. Among these, CD variation and channel doping fluctuations have typically been considered as dominant factors. Many SSTA methods model a much wider range of physical parameters. Variations in these physical parameters, in turn, result in variations in electrical device characteristics (See Figure 1.4), such as the threshold voltage, the drive strength of transistors, and the resistance and capacitance of interconnections. Finally, the variations in electrical characteristics of circuit components result in delay variations of the circuit.

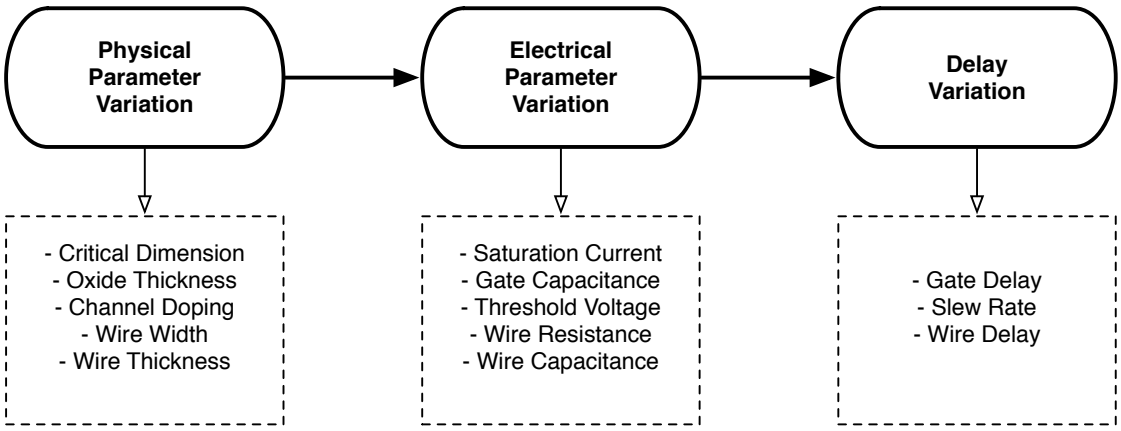


Figure 1.4: Cause-effect of parameters variation: Physical parameter variations resulting in electrical parameter variations, which, in turn, result in circuit delay variations.

It would be ideal to model each process step in the manufacturing process to determine the variations and correlations in the physical parameters. However, such an analysis is complex and impractical due to the number of equipment-related parameters in each fabrication step and the total number of steps. Hence, most SSTA approaches have taken the physical parameters (such as CD, doping concentration, and oxide thickness) to be the basic random variables (RVs). These variables are either assumed to be independent or to have well-understood correlations.

2. Classification of Physical-Parameter Variation:

   Physical-parameter variations can be classified based on whether they are deterministic (systematic) or statistical (non-systematic) and based on the spatial scale over which they operate [19], as shown in Figure 1.5 and Figure 1.6.

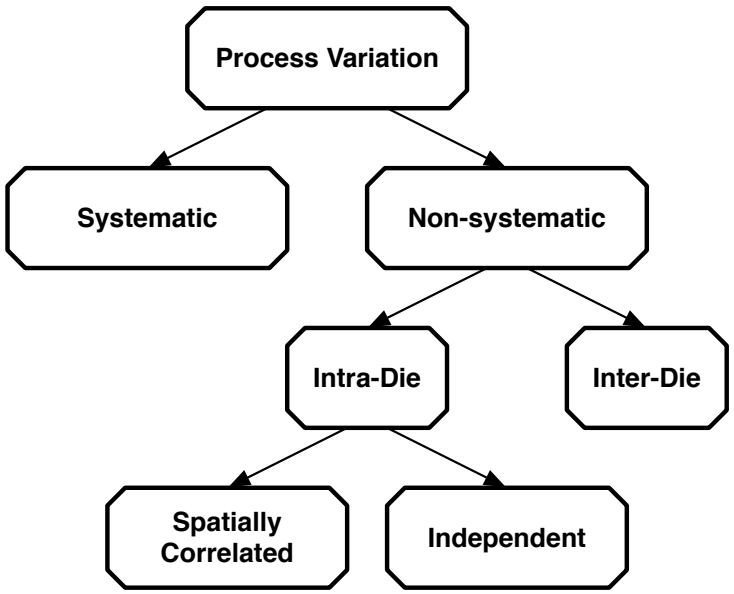


Figure 1.5: Taxonomy of process variations

- Systematic or deterministic variations are components of physical-parameter variation that follow a well-understood behavior and can be predicted upfront by analyzing the designed layout. Systematic variations arise in large part from optical proximity effects, CMP, and its associated metal fill.

  These layout-dependent variations can be modeled pre-manufacturing by performing a detailed analysis of the layout. Therefore, the impact of such variations can be accounted for using deterministic analysis at later stages of the design process [23][24] and particularly at timing sign-off. However, since designer engineers do not have layout information early in the design process, it is common to treat these variations statistically. In addition, the models required for analysis of these systematic variations are often not available to a designer, which makes it advantageous to treat them statistically, particularly when it is unlikely that all effects will assume their worst-case values.

- Non-systematic or random variations represent the truly uncertain component of physical parameter variations. They result from processes that are orthogonal to the design implementation. For these parameters, only the statistical characteristics are known at design time, and hence, they must be modeled using RVs throughout the design process. Line-edge roughness (LER) and random dopant fluctuations (RDF) are examples of non-systematic random sources of variation.

3. Spatial Reach of Variations:

   Non-systematic variations can be further analyzed by observing that different sources of variations act on different spatial scales. Some parameters shift when the equipment is loaded with a new wafer or between processing one lot of wafers to the next; this can be due to small unavoidable changes in the alignment of the wafers in the equipment, changes in the calibration of the equipment between wafer lot processing, etc [19].

   On the other hand, some shift can occur between the exposure of different reticles on a wafer, resulting in reticle-to-reticle variations. A reticle is the area of a wafer that is simultaneously exposed to the mask pattern by a scanner. The reticle is approximately 20 mm * 30 mm and will typically contain multiple copies of the same chip layout or multiple different chip layouts. At each exposure, the scanner is aligned to the previously completed process steps, giving rise to a variation in the physical parameters from one reticle to the next. Finally, some shift can occur during the reticle exposure itself. For instance, a shift in a parameter, such as laser intensity, may occur while a particular reticle is scanned leading to within-reticle variations. Another example is non-uniform etch concentration across the reticle, leading to the variation in the CD.

   These different spatial scales of variation give rise to a classification of non-systematic variations into two categories (See Figure 1.6).

   - **Inter-Die** variations (also referred to as global or die-to-die variations) affect all the devices on the same die in the same way. For instance, they cause the CD of all devices on the same chip to be larger or smaller than nominal. We can see that inter-die variations are the result of shifts in the process that occur from lot to lot, wafer to wafer, reticle to reticle, and across a reticle if the reticle contains more than one copy of a chip layout.

- **Intra-Die** variations (also referred to as local or within-die variations) affect each device on the same die differently. In other words, some devices on a die have a smaller CD, whereas other devices on the same die have a larger CD than nominal. Intra-die variations are only caused by across-reticle variations within the confines of a single chip layout.

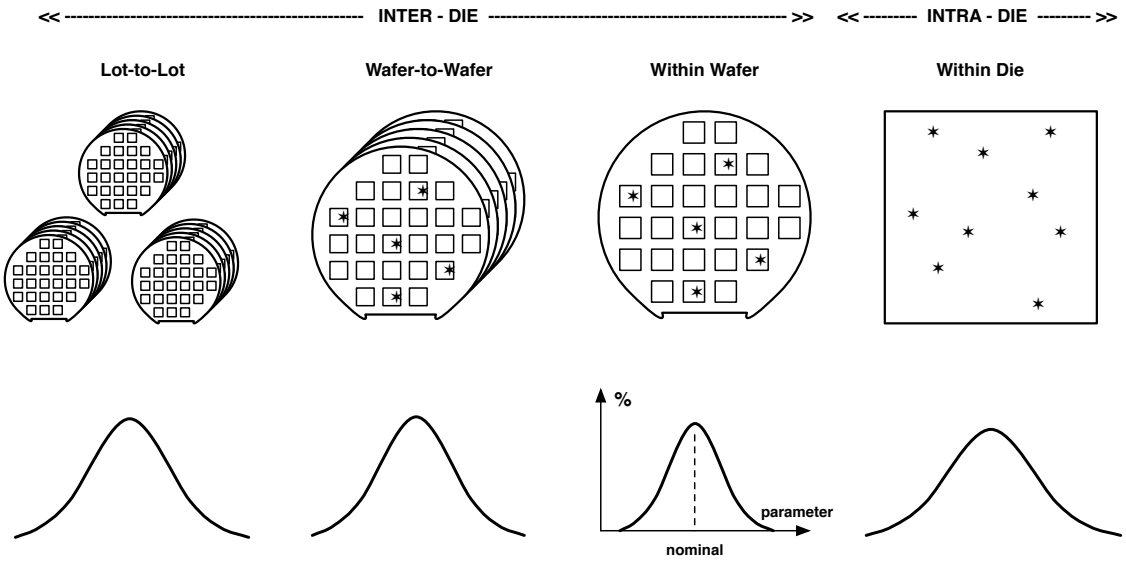


Figure 1.6: Spatial and temporal variation scales

Finally, intra-die variations can be categorized into spatially correlated and independent variations as examine as follows.

- Spatially correlated variations. Many of the underlying processes that give rise to intra-die variation change gradually from one location to the next. Hence, these processes tend to affect closely spaced devices in a similar manner, making them more likely to have similar characteristics than those placed far apart. The component of variation that exhibits such spatial dependence is known as spatially correlated variation.
- Independent variations. The residual variability of a device that is statistically independent from all other devices and does not exhibit spatially dependent correlations is referred to as independent variation. These variations include effects such as RDF and LER. It has been observed that with continued process scaling, the contribution of independent intra-die variation is increasing. Models such as

those of Pelgrom et al. [25], which express the amount of independent variation as a function of nominal device parameters, are gaining increased importance.

1.2.3 Impact of Correlation on Circuit Delay

As examined in the previous section, non-systematic process variations must be modeled using RVs. Furthermore, the RVs associated with different gates in a design will be partially correlated due to the joint contributions from intra-die, spatially correlated, and independent process-variation components [19]. This partial correlation creates significant difficulties for SSTA. The analysis can be substantially simplified if the RVs are assumed to be either fully correlated with a correlation coefficient of ”1” or are assumed completely independent (correlation coefficient of ”0”). If the RVs are assumed to be fully correlated, the variation has the same characteristics as intra-die variation, and DSTA can be used to bound the circuit delay using a set of corner files. On the other hand, while the assumption of independence requires an statistical analysis approach it significantly simplifies the required operations.

Given a combinational-circuit block, the overall circuit delay maybe either overestimated or underestimated by both the fully correlated and independence assumptions. The fully correlated assumption will overestimate the delay of individual paths, whereas it will underestimate the maximum of those path delays. Hence, the final outcome depends on the topology of the circuit. If the logic depth of the circuit is large while, at the same time, only a few paths are critical, the overestimation along the critical paths will dominate, resulting in a pessimistic analysis result. On the other hand, for circuits with shallow logic depth and highly balanced paths, the underestimation occurring in the maximum computation will dominate, and the analysis will be optimistic under the fully correlated assumption. The inverse is true for the independence assumption.

1.3 Test Strategies for Timing Defects

1.3.1 State of the Art

The capability to identify systematic defects also means a shift in the position of testing. If one looks at the chain – fab-test-product-customer, manufacturing test had as purpose to minimize the cost down-stream. Testing was only about determining if a chip is good or bad, and we were

willing to spend this money on testing because is knew that replacing bad ICs in PCBs or products is far more costly. Test gets additional requirements; however, testing has also to provide feed-back to the process engineers to correct systematic defects. It is not sufficient to tell which ICs are bad and good, but it should also tell if the defect is systematic or random in nature. This is of course impossible on basis of a single event and requires an statistical analysis. The simplest and very common method is to compare the observed yield with the expected yield. This method only allows to detect large yield anomalies. In current technologies is very likely that yield becomes affected by multiple systematic defects. Each of these defects can have a small impact on their own but combined they can have a profound impact on yield. Therefore, the detection of small yield anomalies requires more sophisticated methods [1].

A single test which is cheap and detects all defects is ideal for removing bad ICs. However, this test is not very helpful for providing feed-back to the yield/process engineers, since they have only one metric to compare the yield to. Therefore, multiple tests, which could even be partially redundant can be more cost economical for the total product chain than this single test [1].

In traditional logic tests, open and bridge defects are considered to have zero and high resistance values respectively, and are modeled as stuck-at faults, such as [16]. However, resistive opens and bridges have a wide range of resistance values, which plays an important role in both logic and delay behaviors.

Azimane and Majhi [26] proposed a new test methodology for resistive open defect in Memory Address Decoders. They categorize the opens in strong and weak according the fault coverage obtained. The weak opens are those with a resistive value lower that $\approx$1MΩ which may escape the test. James Li et al. [27] made a study of the behavior of resistive open defects and the effects on test results of three test conditions (power supply, speed and temperature) were evaluated. They conclude that at-speed test are effective for resistive open defects. Changing other test conditions, such as test temperature and supply voltage, could be effective for resistive open defects but some knowledge about the material and location of opens have to be known in advance.

1.3.2 Delay Test

Delay fault testing can be used to catch those defects that create delays which cause a poor or mal-function of the IC. Delay test can be computed using one of several known delay fault models, most important of these models are given and described below:

Transition Fault Model [28][29][30][31] assumes that the delay fault affects only one gate in the circuit. There are two transition fault models associated with each gate: a ”slow-to-rise” fault and a ”slow-to-fall” fault. It is assumed that in the defect-free circuit each gate has some nominal delay. Delay faults result in an increase or decrease of this delay. Under the transition fault model, the extra delay caused by the defect is assumed to be large enough to prevent the transition from reaching any primary output at the time of observation. In other words, the delay fault can be observed independent whether the transition propagates through a long or a short path to any primary output as Figure 1.7 shows. Therefore, this model is also called *gross delay fault model* [32]. Figure 1.7 shows a circuit illustrating a transition delay fault. The short path is A through C to E. The long path is A through D and I to J. Small delay defects may not be detected along the short path.

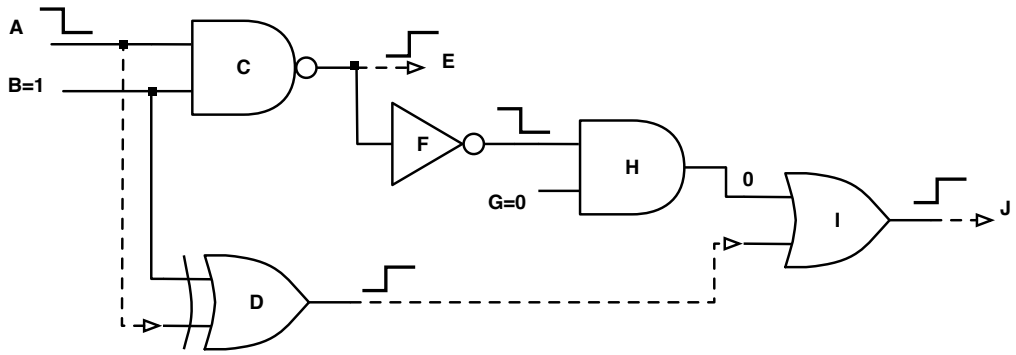


Figure 1.7: Example circuit for transition delay fault. A-C-E: Short path and A-D-I-J: Long path.

To detect a transition fault in a combinational circuit it is necessary to apply two input vectors, $V = (v_1, v_2)$. The first vector, v_1, initializes the circuit, while the second vector, v_2, activates the fault and propagates its effect to some primary output. A transition fault is considered detected if a transition occurs at the fault site and a sensitized path extends from the fault site to some primary output.

The main advantage of the transition fault model is that the number of faults in the circuit is linear in terms of the number of gates. On the other hand, the expectation that the delay fault is large enough for the effect to propagate through any path passing through the fault site might not be realistic because short paths may have a large slack. The assumption that the delay fault only affects one gate in the circuit might not be realistic, either. A delay defect can affect more than one gate and even though none of the individual delay faults are large enough to affect the performance of the circuit, several faults can together result in a performance degradation. For practical simplicity, the transition fault model is frequently used as a qualitative delay model and circuit delays are not considered in deriving test.

Gate Delay Fault Model [28][33][34] assumes that the delay fault is lumped at one gate in the circuit, and captures the defect as a ”slow-to-rise” or a ”slow-to-fall” fault at an input or an output of one gate. However, unlike the transition model, the gate delay fault model does not assume that the increased delay will affect the performance independent of the propagation path through the fault site. It is assumed that long paths through the fault site might cause performance degradation. The gate delay fault model is a quantitative model since it takes into account the circuit delays. The delays of the gates are represented as either the worst-case values or intervals.

Taking the timing into consideration when deriving test for gate delay faults allows application of some test that would otherwise not be considered. To determine the ability of a test to detect a gate delay defect it is necessary to specify the delay size of the fault.

The limitations of the gate delay fault model are similar to those for the transition fault model. Because of the single gate delay fault assumption a test may fail to detect delay faults that are result of the sum of several small delay defects (SDDs). The main advantage of this model is that the number of faults is linear with the number of gates in the circuit.

Path Delay Fault Model [28][35][36] assumes that a (combinational) circuit is considered faulty if the delay of any of its paths exceeds a specified limit. This model, captures the more general scenario where delay variations and defects at multiple gates and wires collectively cause a circuits delay to exceed the limit given in its specifications. A delay defect on a path can be observed by propagating a transition through the path. Therefore, a path delay fault specification consists of a physical path and a transition that will be applied at

the beginning of the path. The delay or length of the path represents the sum of the delays of the gates and interconnections on the path. Then, a path delay fault assumes that a logic transition is delayed along an entire path. Figure 1.8 shows a circuit illustrating a path delay fault. Consider the path from A through D, H and I to J. A gate delay fault can be thought of as a path delay fault through a single gate.

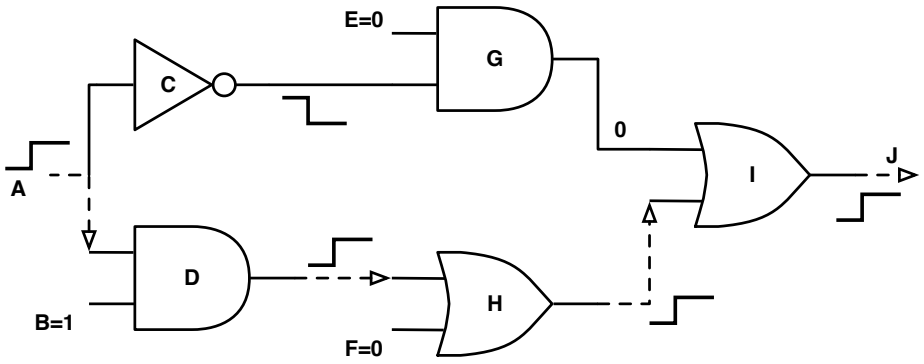


Figure 1.8: Example circuit for path delay fault.

Test for the path delay fault model can detect small distributed delay defects caused by statistical process variations. A major limitation of this fault model is that the number of paths in the circuit can be very large (possibly exponential in the number of gates). For this reason, testing all path delay faults in the circuit is not practical. Two strategies are commonly used for selecting the set of path delay faults for testing. One is to select a minimal set of paths such that for each signal s in the circuit the longest path containing s is selecting for testing. The other is to select all paths with expected delays greater than a specified threshold (called critical paths). This strategy might work for circuits whose paths have very different delays so that there is a small percentage of long paths. However, often in performance optimized designs almost all paths have long delays and in these circuits not even all longest paths can be tested. Therefore, even after path delay fault testing, the temporal correctness of the circuit under test often can not be guaranteed. The problem can be alleviated by developing techniques for re-synthesizing the circuits such that the path count is reduced.

Fault models represent an approximation of the effects that defects produce in the behavior of the circuit [28]. An ideal model should provide a high confidence level that faulty circuits will be isolated. The path delay fault model is usually considered to be closest to the ideal model

for delay defects. Developing a more accurate fault model and selection of critical paths in new designs that are highly sensitive to process variations, circuit defects and signal coupling effects are important research problems nowadays and for the future.

At-Speed Testing

Delay testing is fundamentally different from at-speed testing. In at-speed testing is assumed that manufacturing defects, like bridges and opens, cause the circuit to malfunction at operating speed. Delay testing, on the other hand, is a form of parametric testing. Variations in the width of the interconnections between gates, via contact resistance, etc. causes a change in the rise and fall times of gate outputs. The cumulative effect of this variation causes the circuit to malfunction. Delay testing attempts to isolate circuits with such problems [37]. Part of the testing community has not been making a distinction between the two forms of testing, whose objectives are very different, and using one for other.

Delay fault testing has weaknesses including the following [11]:

- Parameter variation in fabrication requires extra guard-banding to protect against rejection of statistically slow ICs.
- Use of unit delay model for logic gates in automatic test generation (ATG).
- Inability of delay fault test patterns to detect small delay defects that delay the signal, but less than the IC clock period.
- Inability of delay fault ATG to generate good test coverage that is free of hazards or timing errors in setting control logic for the sensitized path.
- Generation of delay fault patterns for non-scan portions of the IC.
- Less predictable path delays and many paths with delays close to the clock period are the main trends affecting the delay testability of nanometer designs.

Delay fault testing has uncertainties for detecting defects that slow a signal [11]. However, concerns about the difficulty of applying I_{DDQ} test have led to a growing interest in delay fault

testing [12]. It has been shown that delay fault testing is valuable in improving parallel path metal issues detection [11].

Test engineers usually use scan to apply delay tests. However, timing-wise, a scan environment is very different from the normal circuit operation. In addition, scan allows the application of non-functional tests that can create high switching, overtesting, and yield loss. Similar problems occur when a test engineer conducts delay testing using BIST [38].

1.3.3 Test Conditions

The capabilities of test conditions on the detectability of interconnect defects, which can lead to delay defects, is briefly described.

Speed

Since the main target of delay-fault testing is to catch defects that create delay and thereby cause a poor or mal-function of the IC. It is clear that at least the specification speed should be met.

The class of non-speed-binned chips, however, is designed in such a way that this speed is met for the worst process and working conditions. Hence, performing the delay-fault test at the specification speed and at the nominal supply voltage, severely underestimates the capabilities of the silicon [39]. This has the risk of missing gross delay-faults which can be detected. Although these IC's could still work in an application it is clear that they do pose a reliability risk. Moreover, there is the risk that the defect is activated along a longer path in the application and therefore causes a malfunction [40].

One way to cope with this is to use adaptive delay-fault testing [40]. Instead of having a fixed limit for all chips, one first determines the capabilities of the silicon, e.g. by measuring a ring-oscillator, and based on this set the test limit. This method may ensures that all defects (opens and shorts) that cause a total delay which is longer than the longest path are detectable. More subtle delays require more advanced test methods, such as fine delay-fault testing [40].

Supply Voltage

The supply voltage is parameter that one can control to enhance the test. For the detection of shorts it is well known that reducing the supply voltage during testing improves the detectability of defects which are missed at the nominal supply voltage [39][41][42]. This is not necessarily true for opens [39]. Some opens have a larger impact at elevated supply voltages while others have a larger impact at reduced supply voltage.

Temperature

Finally, other test condition able to control is the temperature. Cold testing improves the detectability for opens because it makes defect-free circuits faster (0.1-0.2%/K) while defective paths in general become slower [39]. Usually this increase in delay of the affected path is only due to an increase of the resistance of the open itself (0.4%/K for opens in metal). Sometimes a stronger temperature dependency is observed. This can be explained by a change in the contact resistance caused by thermal contractions.

1.3.4 Small Delay Defect Testing

Delay defect refers to any type of physical defect, or an interaction of defects, that adds enough signal-propagation delay in a device to produce an invalid response when the device operates at the targeted frequency [43]. Experimental data over the last two decades has shown that the failure distribution due to delay defects is skewed towards smaller delays (See Figure 1.9) [43][44][45] [46]. This data consistently indicates that the majority of devices that fail due to delay-related defects fail due to delay defects smaller than the typical clock cycle times for the respective technology node [43][44][45] [46][40]. As design sizes and performance increase, more and more circuit nodes will be susceptible to a small delay defect (SDD). Targeting these SDDs during test improves defect coverage and lowers the test escape rate, measured as DPPM (defective parts per million).

Several defect classes including interconnect defects can slow a signal [6]. Resistive opens are a common interconnect defects that lets the circuit function, but poorly with degraded performance in the form of signal delay. For resistive opens is known that the extra delay increases linearly with the value of the open resistance. Resistive bridges are also common manufacturing defects [6]. Bridge defects have an immeasurable effect on signal timing unless the bridge

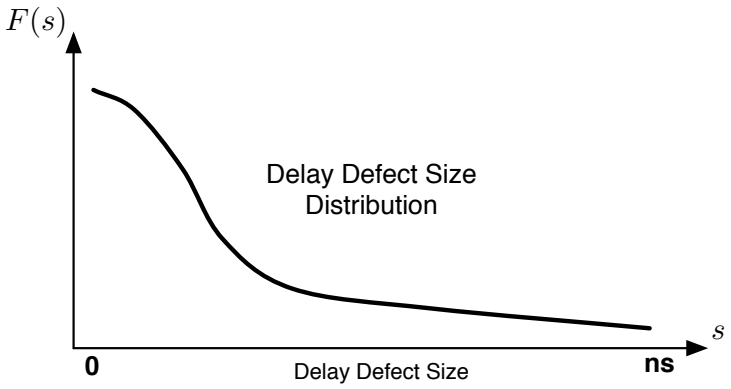


Figure 1.9: Failure distribution due to delay defects is skewed towards smaller delays

impedance is in a sensitive range [6] [14]. Small delay defects are common in current nanometer process; they are originated by resistive opens and resistive bridges, each one for a given range of defect resistance [10][27][47]. Moreover, resistive opens and bridges cause small delay defects difficult to detect and that may escape the test. Kruseman et al. [16] say delay-fault testing is not a very attractive method for the detection of resistive shorts. And that only for a narrow resistance range from one to three times the critical resistance (Rcrit) is expected to observe delays and even in this narrow range the additional delays are typically less than 100 ps in static CMOS designs.

The primary challenge in detecting SDDs is that the delay increment caused by these defects is less than the path slack, but traditional delay test methods only detect defects that are greater than the slack interval. One of the methods to detect SDDs is to estimate the actual path delay during test instead of just checking if it meets a certain timing constraint. This can be achieved by doing multiple captures with fast clocks in the slack interval [48]. If the path delay exceeds the nominal value, then it can be taken as an indication of the presence of a defect. However, due to process variations, path delays are non-deterministic and hence it is difficult to determine if the delay increment observed on a path is due to random process parameters or due to the presence of small defects.

Traditionally, burn-in has been used to screen out dies with reliability hazards. Burn-in is a very expensive process, and it has been argued that burn-in might damage the dies due to excessive stress conditions [49]. Studies also suggest that burn-in might not be very effective in

screening reliability defects in future technologies due to supply voltage scaling [46]. Hence, there is an increasing interest in finding alternative reliability screening procedures to reduce or eliminate burn-in. Small delay defect detection tests can be used as a pre-burn-in reliability screen such that dies are divided into three bins [2]: 1) Defective, 2) Good but unreliable, and 3) Good and reliable. Dies for which SDDs are detected go in the second bin and should be sent in for burn-in. The chips in the third bin which have low probability of failure can be skipped from burn-in or sent for shorter burn-in cycles.

SDDs are difficult to detect by typical test methodologies. SDDs are not properly covered by stuck-at and transition test sets [50]. Nigh et al. [46] have found that SDDs due to resistive opens are an important group of defects that escape the tests. Furthermore, SDDs can cause reliability issues in circuits [2][4][5][11][51]. Due to all these facts there is strong interest for developing test oriented techniques targeting small delay defects [43][52][53][54].

Commercial EDA companies have proposed timing-aware pattern generation tools for testing SDDs [43][52][53][54]. This achieved by integrating timing information in the ATPG. For each transition fault, the fault effect is attempted to be excited and observed along the longest path. The resulting test pattern count and tool run time can be significantly increased [55]. Alternative methods have been proposed to counteract these drawbacks [56] [55] [57]. Lin et al. [56] have proposed to use timing aware pattern generation for only timing critical transition faults. Yilmaz et al. [55] have proposed a technique for test pattern selection and grading based on output deviations. Kumar et al. [57] have proposed a methodology to identify a subset of transition faults that should be targeted by the timing-aware ATPG.

Kruseman et al. [40] uses a different approach to deal with SDDs. They have proposed grouping conventional delay-fault patterns into sets of almost equal-length paths. Tayade et al. [2] have proposed a test approach to increase the set of detectable resistive open defects in the presence of process variations. They find that the probability of detecting a delay defect on a net is higher using a path with lower delay variance. Czutro et al. [58] present a small-delay fault simulation approach which calculates realistic coverage of such faults based on the occurrence probability of the low-resistance interconnect open defects.

1.4 Statistical Timing Analysis

Static Timing Analysis (STA) has been one of the most pervasive and successful analysis engines in the design of digital circuits for the last 20 years. However, in recent years, the increased loss of predictability in semiconductor devices has raised concern over the ability of STA to effectively model statistical variations [19]. This has resulted in extensive research in the so-called Statistical STA (SSTA), which marks a significant departure from the traditional STA framework.

1.4.1 Problem Formulation

In traditional DSTA, the most basic goal of the analysis is to find the maximum delay between the source node and the sink node of a timing graph, which is the delay of the longest path in the circuit. When modeling process-induced delay variations, the sample space is the set of all manufactured dies. In this case, the device parameters will have different values across this sample space, hence the critical path and its delay will change from one die to the next. Therefore, the delay of the circuit is also a RV, and the first task of SSTA is to compute the characteristics of this RV. This is performed by computing its probability distribution function (PDF) or cumulative distribution function (CDF) (See Figure 1.10). Alternatively, only specific statistical characteristics of the distribution, such as its mean and standard deviation, can be computed. Note that the CDF and the PDF can be derived from one another through differentiation and integration. Given the CDF of circuit delay of a design and the required performance constraint the anticipated yield can be determined from the CDF. Conversely, given the CDF of the circuit delay and the required yield, the maximum frequency at which the set of yielding chips can be operated at can be found.

Similar to traditional DSTA, we can formulate the SSTA problem as that of finding the latest arrival time distribution at the sink node in the timing graph [59][60]. The latest arrival time distribution at the sink node can be found by propagating the arrival time from the source node through the timing edges while computing the latest arrival time at every node in topological order. Subsequently, the latest arrival time distribution at the sink node is the circuit delay distribution.

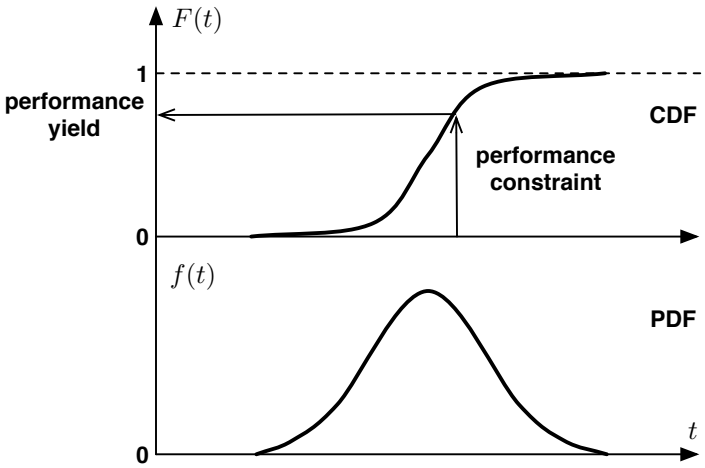


Figure 1.10: Probability distribution function (PDF) and cumulative distribution function (CDF)

In addition to the problem of finding the delay of the circuit, which has been posed as the basic SSTA problem, it is also key to improve this delay when the timing requirements are not met. Hence, DSTA methods typically report the slack at each node in the circuit, in addition to the circuit delay and critical paths. The slack of a node is the difference between the latest time a signal can arrive at that node, such that the timing constraints of the circuit are satisfied (referred to as the required time), and the actual latest arrival time of the signal at that node [61]. Similar to the circuit delay, the slack of a node is an RV in the SSTA formulation.

1.4.2 Challenges in SSTA

The statistical formulation of timing analysis introduces several new modeling and algorithmic issues that make SSTA a complex and enduring research topic [62]. In this section, we introduce some of these issues, as well as the relevant SSTA terminology.

1. Topological Correlation:

   Paths that start with one or more common edges after which the paths separate and join again at a later node are called reconvergent paths and the node at which these paths reconverge is called the reconvergent node. For instance, in Figure 1.11, the two paths P_1 and P_2 share the same first edge (corresponding to gate G0) and reconverge at the output of gate G3. In such case, the input arrival times at the reconvergent node become dependent on each other because of the shared edge delay. This dependence leads to

so-called topological correlation between the arrival times and complicates the maximum operation at the reconvergent node. To perform accurate analysis, the SSTA algorithm must capture and propagate this correlation so that it is correctly accounted for during the computation of the maximum function.

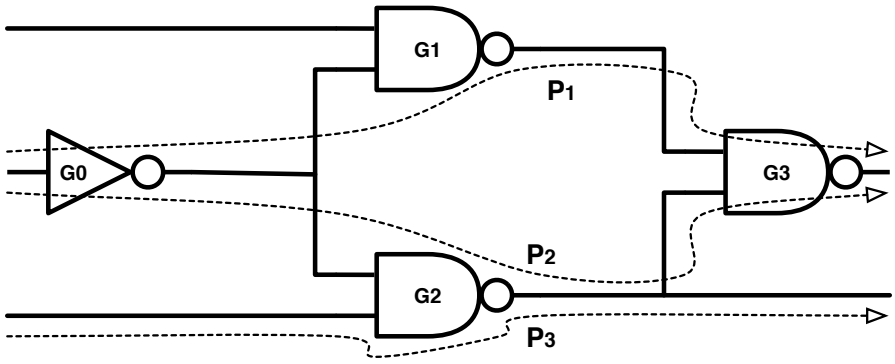


Figure 1.11: Example circuit shows the topological correlation due to reconvergent paths.

2. Spatial Correlation:

   As discussed previously, intra-die variation of the physical device parameters often exhibits spatial correlation, giving rise to correlation between the gate delays. Hence, if the gates that comprise two paths have spatially correlated device parameters they will have correlated path delays. In this way, correlation can be introduced between paths that do not share any common timing edges. For instance, in Figure 1.11, the paths P_1 and P_3 do not share any common delay edges, but if gates G1 and G2 are within close proximity on the die, their spatially correlated delays can give rise to correlation between the two path delays. Hence, spatial correlation of the arrival times must be captured and propagated during SSTA so that it is correctly accounted for during the maximum operation. Spatial correlation also impacts the sum operation. For example, if in Figure 1.11, gates G1 and G3 have spatially correlated delays then the arrival time at output of gate G1 will be correlated with the delay of gate G3 .

   While topological correlation only affects the maximum operation, spatial correlation affects both the sum operation and the maximum operation. This raises two fundamental challenges for SSTA: 1) how to model gate delays and arrival times such that the spatial correlation of the underlying device parameters can be expressed; and 2) given a model

of the spatial correlation, how to propagate and preserve the correlation information while performing the sum and maximum operations in SSTA. A common approach to this problem has been to represent delay in terms of the device-parameter-space basis, which is common to all gate delays.

3. Non-normal Process Parameters and Non-linear Delay Models:

   Normal or Gaussian distributions are found to be the most commonly observed distributions for RVs, and a number of elegant analytical results exist for them in the statistics literature. Hence, most of the initial work in SSTA assumed normal distributions for physical device parameters, electrical device parameters, gate delays, and arrival times.

   However, some physical device parameters may have significantly non-normal distributions. Even if the physical device parameters are indeed normally distributed (e.g., doping concentration has a normal distribution), the dependence of the electrical device parameters and gate delay on these physical parameters may not be linear, giving rise to non-normal gate delays. Some works in modeling spatial correlations [63][64][65] used a first order delay model which assumed a linear dependence of the gate delay on physical device parameters. If the variations are small, this linear approximation is justified, as the error introduced by ignoring higher order terms is negligible. However, with reduction of geometries, process variation is becoming more pronounced, and the linear approximation may not be accurate for some parameters.

4. Skewness Due to Maximum Operation:

   Even if gate delays are assumed to be normal, SSTA has to cope with the fact that the maximum operation is an inherently non-linear function. The maximum of two normal arrival times will result in a non-normal arrival time that is typically positively skewed. In addition, the non-normal arrival time distribution produced at one node is the input to the maximum computation at down-stream nodes. Hence, a maximum operation that can operate on non-normal arrival times is required.

   Most of the existing approaches ignore the skewness introduced by the maximum operation and approximate the arrival times with normal distributions. The error of this normal approximation is larger if the input arrival times have similar means and dissimilar variances [66], as Figure 1.12 shows. In other words, the error is most pronounced when two converging paths have nominally balanced path delays, but one path has a tighter delay

distribution than the other. This can occur in a circuit when two paths with equal nominal delay have a different number of gates or when the correlation among their gates differs. Another example is when one path is dominated by interconnect delay while the other is dominated by gate delay.

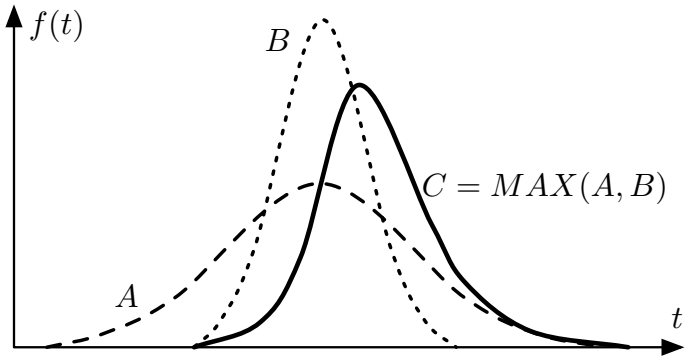


Figure 1.12: Skewness due to non-linear maximum operation.

1.4.3 SSTA Solution Approaches

1. Numerical Integration Methods:

   The simplest SSTA approach follows directly from the problem formulation definition. A numerical integration over the process parameter space is performed to compute the yield of the circuit for a particular delay. Typically, the delay of a set of critical paths is expressed as a linear function of the physical device parameters and a feasible region in this parameter space is defined by the desired circuit delay. This region is then numerically integrated, exploring all possible permutations of physical device parameter values that lie in the feasible region.

   Efficient numerical integration methods were proposed in [67]. The advantage of this method is that it is completely general and process variation with any type of distribution and correlation can be modeled. However, it can be quite expensive in runtime, in particular for balanced circuits with a large number of critical paths.

2. Monte Carlo Methods:

   The second general approach performs an statistical sampling of the sample space using Monte Carlo simulation, based on the Metropolis sampling algorithm [68]. Instead of

explicitly enumerating the entire sample space, the key idea is to identify the regions of signicant probability and to sufficiently sample these regions. Using the PDF of the physical device parameters, a number of samples are drawn. For each sample, the circuit delay is computed using the traditional DSTA methods. Thereafter, by evaluating a fraction of samples that meet the timing constraint, an estimate of timing yield is found. If a sufficient number of samples are drawn, the estimation error is small. By sweeping the timing constraint and finding the yield for each value, the entire circuit delay distribution can be found.

As with numerical integration, the Monte Carlo approach has the advantage of being completely general. Furthermore, it is based on existing mature DSTA methods and performs significantly faster than the numerical integration-based methods. However, since DSTA is in the inner loop of the Monte Carlo simulation, the runtime can still be significant, particularly if a fully featured industrial DSTA tool is used. Using the Monte Carlo simulation, it is also difficult to perform incremental analysis after a designer makes a small change to the circuit. It has been shown that the performance of Monte Carlo techniques can be improved using methods such as importance sampling [69][70][71][72]. However, more research is required to examine if fast sampling techniques can be effective for SSTA.

3. Probabilistic Analysis Methods:

   Both previous approaches are based on sample space enumeration. In contrast, probabilistic methods explicitly model gate delay and arrival times with RVs. These methods typically propagate arrival times through the timing graph by performing statistical sum and maximum operations. They can be classified into two broad classes: 1) path-based approaches; and 2) block-based approaches. The key difference between the two approaches is where in the algorithm the maximum function is invoked.

   - Path-based approaches: In path-based SSTA algorithms, a set of paths, which is likely to become critical, is identified, and an statistical analysis is performed over these paths to approximate the circuit delay distribution. First, the delay distribution of each path is found by summing the delay of all its edges. Assuming normal gate delays, the path delay distribution is normal and can be analytically computed [73][74][75]. The overall circuit delay distribution is then found by performing an

statistical maximum operation over all the path delays.

The basic advantage of this approach is that the analysis is clearly split into two parts; the computation of path delays followed by the statistical maximum operation over these path delays. Hence, much of the initial research in SSTA was focused on path-based approaches [73][74][76][77][78][79][80]. Clearly, the difficulty with the approach is how to rigorously find a subset of candidate paths such that no path that has significant probability of being critical in the parameter space is excluded. In addition, for balanced circuits, the number of paths that must be considered can be very high. Therefore, most of the later research has focused on the block-based approaches.

- Block-based approaches: The block-based methods follow the DSTA algorithm more closely and traverse the circuit graph in a topological manner. The arrival time at each node is computed using two basic operations: 1) For all fan-in edges of a particular node, the edge delay is added to the arrival time at the source node of the edge using the sum operation; and 2) given these resulting arrival times, the final arrival time at the node is computed using the maximum operation. Hence, the block-based SSTA methods propagate exactly two arrival times (a rise and a fall arrival time) at each circuit node, resulting in a runtime that is linear with circuit size. The computation of the sum function is typically not difficult; however, finding the statistical maximum of two correlated arrival times is not trivial. Due to its runtime advantage, many current research and commercial efforts have taken the block-based approach. Furthermore, unlike other approaches, the block-based approach lends itself to incremental analysis which is advantageous for diagnostic/optimization applications. In block-based SSTA methods, the result of the maximum operation performed at one node is the input to the maximum operation which is performed at downstream nodes. It is therefore essential that the sum and maximum operations preserve the correlation information of the arrival times so that this information is available at later operations. Furthermore, the skewness introduced by the maximum operation must be considered.

1.5 Justification of the Present Work

Since the shrink in the dimensions of the devices in order to get circuits with higher performance and more benefits, new issues affecting the reliability and yield have appeared. Thus, critical dimensions have been affected by the manufacturing process variations. In the same direction, interconnect defects are an important source of faults encountered in circuits. These defects are opens and bridges. This kind of defects can produce small delay faults that may escape test which turn into a reliability concern.

In this thesis, an aware methodology to evaluate circuit testability for small delay defects in the presence of process variations is proposed. Small delay defects due to resistive opens and bridges are considered. An Statistical Timing Analysis Framework is used to propagate delay defects related to resistive open and bridge defects. An statistical methodology to estimate the probability of detection of resistive open and bridge defects is proposed. Using the probability of detection the Statistical Fault Coverage (SFC) of the circuit is obtained. Using the proposed methodology, the statistical fault coverage of interconnect defects producing small delays is evaluated for some ISCAS benchmark circuits. Finally, circuit testability for the detection of small delay defects is determined.

1.6 Organization of the Thesis

The remain of this work is organized as follows: Chapter 2 presents the statistical timing analysis framework. Chapter 3 describes the proposed method to evaluate circuit testability due to resistive opens. Chapter 4 describes the proposed method to evaluate circuit testability due to resistive bridges. Chapter 5 proposes a sampling methodology to compute the statistical fault coverage for small delay defects due to resistive opens and bridges. Finally, Chapter 6 gives the conclusions of the present work.

Chapter 2

Statistical Timing Analysis Framework

In this chapter, an Statistical Timing Analysis Framework is implemented. The most important issues in nanometer technologies were considered. ISCAS benchmark circuits were used to test the capabilities of the framework. Finally, circuit delay (mean and variance) are given for each circuit. This Chapter is organized as follows: In Section 2.1, the introduction to SSTA is given. In Section 2.2 the Statistical Timing Analysis Framework implemented is described. In Section 2.3 simulation results are presented. Finally, the conclusions of this chapter are given in Section 2.4.

2.1 Introduction

Static timing analysis (STA) has been a widely adopted tool for all facets of VLSI chip designs. Traditional STA tools are deterministic and compute the circuit delay for a specific process condition. Hence, all parameters that impact the delay of a circuit, such as device gate length and oxide thickness, as well as operating voltage and temperature, are assumed to be fixed and are uniformly applied to all the devices in the design [19]. This is also called deterministic STA (DSTA). However, with process scaling progressing well into the nanometer regime, process variations and others technological parameters variations that affect the circuit delay have become more significant. Therefore, the need for an effective modeling of process variations in timing analysis has led to extensive research in Statistical STA (SSTA). Some recent works with an accurate SSTA tool considering the process variations are the developed by Kang et al. [81] and Agarwal et al. [64][74]. An accurate timing analysis tool should consider the following three issues simultaneously [81]: (1) spatial correlation of the process parameters, (2) random placement of dopants, and (3) the signal correlation due to reconvergent paths.

Recently process variability has become a problematic issue in digital design. Variations are classified in two types: inter-die and intra-die. Inter-die variations affect the deviation of performance distribution in a lot of chips and intra-die variations affect the media of performance distribution [82]. This has significant consequences for digital systems, because variations which were ignored in the past, have become significant in nanometer technologies. A synchronous clocked digital system contains a number of logic paths whose propagation delays determine the system performance.

2.2 Statistical Timing Analysis Framework

The core of the Statistical Timing Analysis Framework (STAF) used in this work was mainly based in the technique statistical timing analysis using levelized covariance propagation of Kang et al. [81][83]. In this technique, a block-based statistical timing analysis is used. Also, include simultaneously the most important issues in nanometer technologies, such as: (1) spatial correlation of the process parameters such as length, width and oxide thickness of the transistor, (2) random placement of dopants, and (3) the signal correlation due to reconvergent paths.

Three important aspects in the STAF are: the modeling of the process variation, modeling of gate delay and the statistical timing analysis; which are detailed explained below.

2.2.1 Modeling the Process Variations

The random process parameters considered in this work are channel length (L), transistor width (W), oxide thickness (Tox) and threshold voltage (Vth); which are represented by a random variable (RV) with normal distribution and assumed mutually independent. The process parameters can be divided in two groups based on their statistical behavior.

The parameters such as length, width and oxide thickness exhibit spatial correlations among different transistors close to each other. This correlation is captured using the rectangular grid model proposed by Agarwal et al. [74], as shown in Figure 2.1. In this model, the die area is divided by a multi-level quad-tree partitioning. All the transistors in a particular grid are assumed to experience the same parameter variations. The spatial correlation among transistors in different grids is governed by their parent grids.

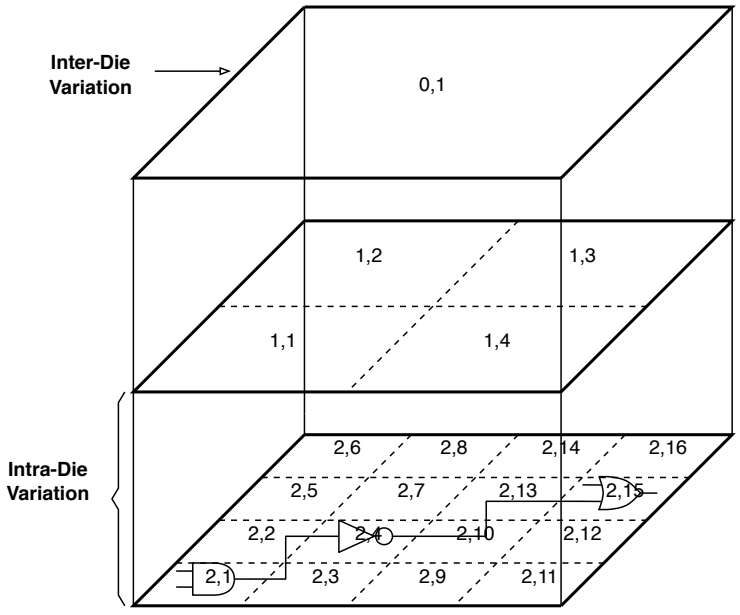


Figure 2.1: Rectangular grid model [74]

For every grid at all levels a single random variable is used to represent each process parameter. The parameter variation of a transistor in any grid at the bottom most level is represented by the sum of the variation in that particular grid and the variations in all its parent grids. For example, the variation of channel length of transistors in grid [2,1] is represented by

$$L(2,1) = L_0 + \Delta L_{2,1} + \Delta L_{1,1} + \Delta L_{0,1} \tag{2.1}$$

where $L(2,1)$ is the RV representing the variation in the channel length in grid [2,1]. L_0 is the nominal value of the channel length. $\Delta L_{2,1}, \Delta L_{1,1} and \Delta L_{0,1}$ represent the deviation in channel length in grids (2,1), (1,1) and (0,1) respectively.

At circuit level, gates that lie within close proximity of each other will have many common intra-die device parameter components resulting in a strong correlation. Gates that lie fart apart on a die share few common components and therefore have weaker correlation. For example, the RVs representing the channel length in grid [2,1], [2,2] and [2,16] are expressed as,

$$L(2,1) = L_0 + \Delta L_{2,1} + \Delta L_{1,1} + \Delta L_{0,1}$$
$$L(2,2) = L_0 + \Delta L_{2,2} + \Delta L_{1,1} + \Delta L_{0,1}$$
$$L(2,16) = L_0 + \Delta L_{2,16} + \Delta L_{1,4} + \Delta L_{0,1}$$

In this example, $L(2,1)$ and $L(2,2)$ share two parent grids while $L(2,1)$ and $L(2,16)$ share only one parent grid. Hence, the correlation between $L(2,1)$ and $L(2,2)$ are stronger than the correlation between $L(2,1)$ and $L(2,16)$. Since the top level is the parent grid of all the grids, it represents the inter-die variation. While the intra-die variation is represented by all other lower levels. Hence, using this model inter- and intra-die variations are considered simultaneously. In this work, we used a model with three levels of hierarchy.

The threshold voltage is different for each transistor in a die due to the effect of random placement of dopants [84][85]. Hence, separate random variables are used to represent each transistor. This discrete dopant effect on threshold voltage variation is incorporated by employing the following equation [85] into the STAF while computing the variation of threshold voltage of each transistor.

$$\sigma_{Vth} = \frac{q}{C_{ox}} \sqrt{\frac{N_a W_{dm}}{3LW}} \tag{2.2}$$

σ_{Vth} represents the standard deviation of threshold voltage variation due to random placement of dopants, q is electron charge, C_{ox} is the oxide capacitance, N_a is the substrate doping concentration, and W_{dm} represents the maximum depletion layer width. L and W are the channel length and width of the transistor, respectively.

2.2.2 Modeling the Gate Delay

The equation used to model the gate delay is given by a simple expression, as shown in (2.3). D_o represents the nominal value of the gate delay without variation, which includes the effect of the load and diffusion capacitance. The Sakurai's gate delay model [86] is used to obtain the nominal delay of each gate in the circuit. X_i's are the sources of variation, which are modeled as normal random variables. X_i can be any process parameter such as channel length, width, oxide

thickness and the threshold voltage, that affects the delay of a specic gate. s_i is the sensitivity of the gate delay to the variation in process parameter X_i. All s_i's are extracted through HSPICE simulation by varying the process parameters from their nominal value.

$$D = D_o + \sum_{i}^{n} s_i X_i \tag{2.3}$$

The variance of the gate delay can be obtained as,

$$\sigma_D^2 = \sum_{i}^{n} s_i^2 \sigma_{X_i}^2 \tag{2.4}$$

where σ_{X_i} is the standard deviation of the RV X_i.

2.2.3 Statistical Timing Analysis

This section is the core of the STAF since its generates and compute the statistical timing information at the output edges of a particular logic level using the signal information at its inputs edges. The calculated timing information is then propagated to next logic level until the last one. The statistical timing information contains:

1. The mean μ and the variance σ^2 of signal arrival time at each output edge.
2. The covariance among the output signal arrival times.
3. The covariance between the output arrival time and the process parameters.

Since the kind of information calculated and propagated, this technique is named as *Levelized Covariance Propagation*. The above information is required to calculate the arrival times at the output of any gate considering the effects of process variation with spatial correlation, random placement of dopants and signal correlation due to reconvergent paths.

The methodology to calculate the statistical timing information at the output of a logic level, is briefly explained below. To show how the signal information is calculated at the output edges, a two-input gate is considered, as shown in Figure 2.2.

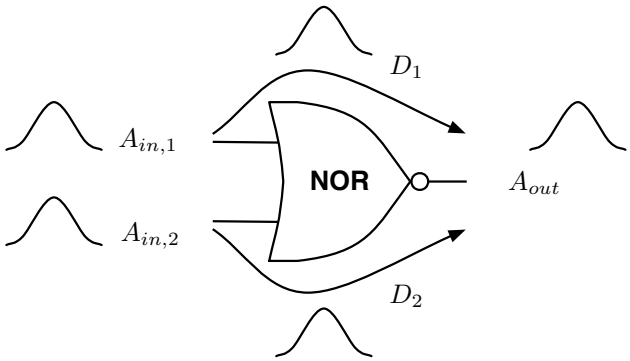


Figure 2.2: Two-input NOR gate

The mean μ_{Aout} and the variance σ^2_{Aout} of signal arrival time at the output A_{out} of a gate is calculated using the input arrival time and the corresponding gate delay, and can be obtained employing the MAX function (the MAX function refers to the statistical maximum operation). The expression formulated is given by

$$A_{out} = MAX(A_{in,1} + D_1, A_{in,2} + D_2) \tag{2.5}$$

$A_{in,1}$ and $A_{in,2}$ are the signal arrival times at the input 1 and 2, respectively. D_1 and D_2 are the corresponding pin-to-pin delays of the gate.

This equation can be solved with the technique *The greatest of a finite set of random variables* developed by Clark [66]. For the case of two inputs gates, the mean ($\mu_{A_{out}}$) and the variance ($\sigma^2_{A_{out}}$) at the output are obtained by the following expressions:

$$\mu_{A_{out}} = \mu_{S_1}\Phi(\alpha) + \mu_{S_2}\Phi(-\alpha) + \beta\phi(\alpha) \tag{2.6}$$

$$\sigma^2_{A_{out}} = (\mu^2_{S_1} + \sigma^2_{S_1})\Phi(\alpha) + (\mu^2_{S_2} + \sigma^2_{S_2})\Phi(-\alpha) + (\mu_{S_1} + \mu_{S_2})\beta\phi(\alpha) - \mu^2_{A_{out}} \tag{2.7}$$

where,

$$S_i = A_{in,i} + D_i \qquad i = 1, 2 \tag{2.8}$$

$$\mu_{S_i} = \mu_{A_{in,i}} + \mu_{D_i}$$

$$\sigma^2_{S_i} = \sigma^2_{A_{in,i}} + \sigma^2_{D_i} + 2 * cov(A_{in,i}, D_i)$$

$\mu_{A_{in,i}}$, $\sigma_{A_{in,i}}$, μ_{D_i} and σ_{D_i} are the mean and the standard deviation of input arrival time and the gate delay, respectively. $\Phi(\alpha)$ and $\phi(\alpha)$ represent the cumulative distribution function (CDF) and the probability distribution function (PDF) of standard normal distribution, respectively. The coefficients α y β can be calculated as follows:

$$\alpha = (\mu_{S_1} - \mu_{S_2})/\beta \tag{2.9}$$

$$\beta^2 = \sigma_{S_1}^2 + \sigma_{S_2}^2 - 2\sigma_{S_1}\sigma_{S_2}\rho \tag{2.10}$$

The correlation coefficient ρ gives a linear relation measurement between two qualitative variables. Unlike the covariance, the correlation coefficient is independent of the scale of the variables (S_1, S_2). The correlation value can took values defined in the range [-1, +1] , and is given by

$$\rho = cov(S_1, S_2)/\sigma_{S_1}\sigma_{S_2} \tag{2.11}$$

Since ρ gives the relation degree between two variables, solving this expression according to Kang's methodology [81], is possible to consider simultaneously the next technological issues: spatial correlation of the process parameters such as length, width and oxide thickness of the transistor (L, W, Tox), random placement of dopants, and the signal correlation due to reconvergent paths. Then, the covariance $cov(S_1, S_2)$ from (2.11) is given by

$$cov(S_1, S_2) = cov(A_{in,1}, D_2) + cov(A_{in,2}, D_1) + cov(A_{in,1}, A_{in,2}) + cov(D_1, D_2) \tag{2.12}$$

The first and second term take into account the spatial correlation effect, the third term considers the signal correlation, and last term incorporates the random placement of dopants.

The covariance among the output signal arrival times $cov(A_{out,i}, A_{out,j})$ and the covariance between the output arrival time and the process parameters $cov(A_{out}, X)$ are included at time the equation (2.12) is solved. These information are calculated using the timing information obtained in the previous logic level.

In this approach, the spatial correlation effect is taken into account at the time that the covariance between the output arrival time and the process parameters $cov(A_{out}, X)$ is included,

and the signal correlation due to reconvergent paths is considered at the time that the covariance among the output signal arrival times $cov(A_{out}, A_{out})$ is incorporated.

Figure 2.3 shows the flow diagram of the levelized covariance propagation algorithm. The algorithm starts with levelizing the logic gates. Then, the algorithm is initialized applying the timing information at the primary inputs. To compute the signal information at the output edges, the method described previously is used. Finally, the MAX function is applied at the primary outputs to calculate the circuit delay.

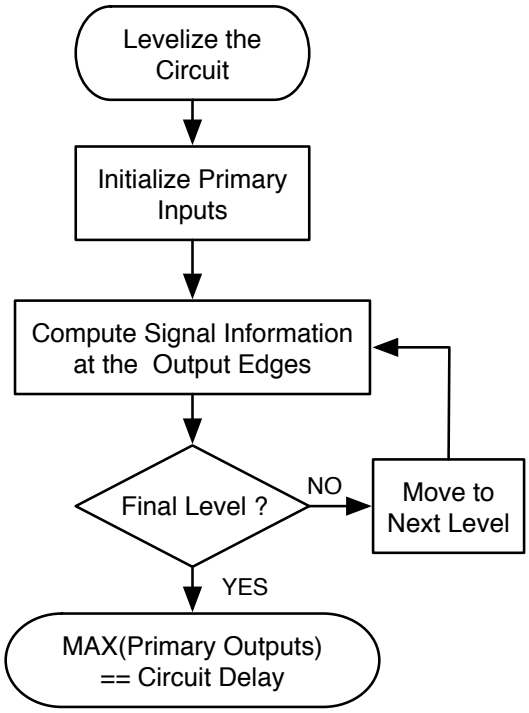


Figure 2.3: Levelized covariance propagation algorithm

2.3 ISCAS Simulation Results

The SSTA was applied to some ISCAS 85 benchmark circuits considering process parameter variations on channel length, transistor width, oxide thickness and threshold voltage. In addition, the most important issues in nanometer technologies were take into account. The circuits were implemented with TSMC $0.18\mu m$ technology. Mentor Graphics Tools were used to implement the benchmark circuits. The ASIC Design Kit (ADK v3.1) was utilized to create each circuit.

The simulation results for these benchmark circuits are shown in the Table 2.1. This show the mean (μ) and standard deviation (σ) of the circuit delay, and the number logic levels (LL) or logic depth for each circuit.

Table 2.1: Simulation results of ISCAS 85 benchmark circuits. These are combinational circuits.

CIRCUIT	LL	MEAN (μ)[ns]	SD (σ)[ps]
C432	22	2.89	27
C499	12	1.72	29
C1908	20	2.31	26
C2670	30	2.29	77
C3540	35	3.17	49
C6288	91	8.62	63

In the synthesizing, the circuits were not optimized neither area nor timing. Hence, the results data, basically shows a dependence on the architectural topology of the circuits. This means that the circuits are unbalanced and the longest paths determine the circuit delay.

2.4 Conclusions

An Statistical Timing Analysis Framework (STAF) was implemented using levelized covariance propagation. In this technique, a block-based statistical timing analysis is used. Process parameters variation considered in this work are the channel length and width, the oxide thickness and the threshold voltage. Also, the most important issues in nanometer technologies, such as: spatial correlation of the process parameters such as length, width and oxide thickness of the

transistor, random placement of dopants, and the signal correlation due to reconvergent paths are simultaneously included. The spatial correlation due to the process parameters is considered using a rectangular grid model. Using this model inter- and intra-die variations are simultaneously considered. The mean and variance at the output of the gates are computed using the timing information at their inputs and applying the MAX function. Spatial correlation, random placement of dopants and signal correlation are taking into account at time the MAX function is solved.

Then, using the STAF, combinational ISCAS 85 benchmark circuits were simulated and the mean and the standard deviation of the circuit delay were obtained.

Chapter 3

Resistive Open Defects

In this chapter, an aware methodology to evaluate circuit testability for small delay defects due to resistive opens in the presence of process variations is presented. An Statistical Timing Analysis Framework is used to propagate delay defects related to resistive open defects. An statistical methodology to estimate the probability of detection of resistive open defects is proposed. Using the probability of detection the Statistical Fault Coverage (SFC) of the circuit is obtained. An exhaustive analysis of the SFC is done in this chapter, i.e. the SFC is obtained for all the possible open locations. The SFC gives an indication of the circuit testability for small delay defects due to resistive opens. The methodology is applied to some ISCAS benchmark circuits. This Chapter is organized as follows: In Section 3.1, state of the art for open defects on nanometer technologies is introduced. In Section 3.2, formulation of the problem and the proposed methodology are given. In Section 3.3, the procedure to estimate the probability of detection and the SFC of the circuit for open defects is developed. In Section 3.4, an example of the methodology is given. In Section 3.5, the simulation results for ISCAS circuits are presented. Finally, the conclusions of this chapter are given in Section 3.6.

3.1 Introduction

Physical defects appear in some of the fabricated chips due to the complexity and imperfections of the manufacturing process. Typical defects encountered in today technologies are the so-called interconnect defects that can lead to shorts and/or opens at different conductive levels [3]. Interconnect based defects have become an important issue in nanometer technologies. Vias are a likely place for an open to occur [11]. Vias have become an important yield detractor in modern technologies which have a high number of vias due to the many used metal levels [9][11].

The use of copper and damascene process has lead to think the way that metal defects are considered [87]. The open density in copper shows higher values than those found in aluminum [88]. Micromasking during the lithography can occur [88]. Dishing and erosion can also lead to opens [87]. If the open defect does not completely eliminates the electrical connection between two nodes, the open defect is a weak open defect. Weak resistive opens producing small delays are an issue in modern nanometer technologies.

Previous research classified opens into strong opens (R>10MΩ) and weak opens (R<10MΩ) [10]. Weak opens let the circuit function, but poorly with degraded performance in the form of signal delay. Moreover, weak opens cause small delay defects difficult to detect by typical test methodologies. Small delay defects are common in current process; they are in part originated by resistive opens, for a given range of defect resistance [10][27][47]. Weak opens in vias and interconnection lines are an issue in modern nanometer technologies. Small delay defects are not properly covered by stuck-at and transition test sets [50]. Nigh et al. [46] have found that small delay defects due to resistive opens are an important group of defects that escape the tests. Furthermore, small delay defects can cause reliability issues in circuits [2]. For this reason, the interest to study this kind of defect in this work. The detection of resistive opens may depend on various factors, such as: value of the resistive open, location in the circuit, logic depth of the circuit, delay and variance of the defect-free circuit [2][3]. Tayade et al. [2] have proposed a test approach to increase the set of resistive open defects in the presence of process variations. They find that the probability of detecting a delay defect on a net is higher using a path with lower delay variance. Czutro et al. [58] have developed a simulator which determines the fault coverage of small delay defects caused by resistive open defects. They obtain a realistic fault coverage (probabilistic) for these opens. Also, they obtain the probability that a detectable small delay defect is actually detected by the test set.

3.2 Assessment and Proposed Resolution to the Problem

3.2.1 Formulation of the Problem

Resistive opens are interconnect defects that have a high occurrence in advanced CMOS technologies [6][9][10]. The focus of this work is to deal with those resistive opens that produce small delay faults. As the technology continue scaling, testing of small delay defects are becoming more important. A range of the resistance values for the open that represent the small delays

is considered.

Figure 3.1 shows a two inverter chain with a resistance R_o and a capacitance C. This represents an open fault model. R_o models the resistive open and C is the load capacitance due to fanout gates.

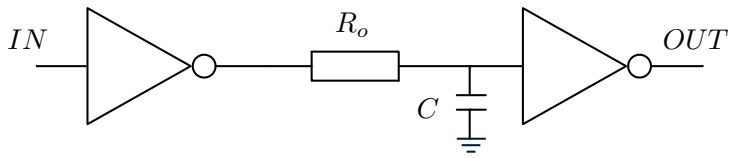


Figure 3.1: Inverter chain with a resistive open defect

Figure 3.2 shows the electrical behavior at the output of the two inverter chain (See Figure 3.1) with a resistive open taking different values. The signals are the outputs for the defect-free and for different values of the resistive open are shown. For the considered open resistance range, it can been observed that the resistive open defect produces small delays of approximately 29ps up to 200ps. Some of them may be not detected depending on the clock slack.

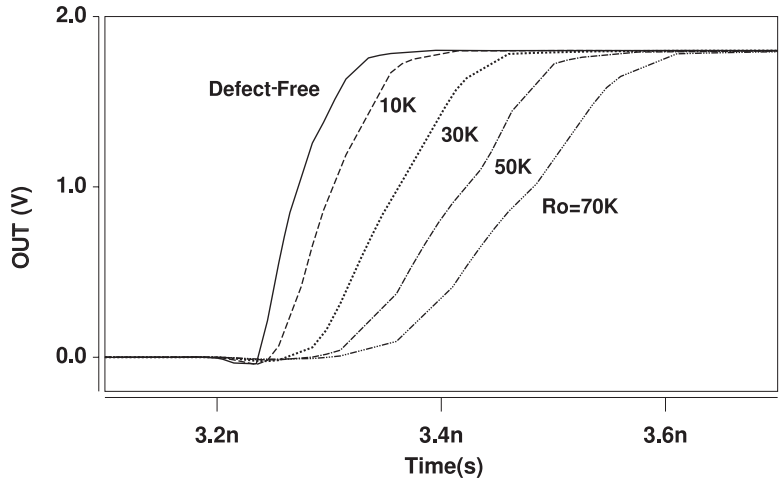


Figure 3.2: Output response simulation of the two inverter chain with a resistive open for different values. Resistances values: 10KΩ, 30KΩ, 50KΩ and 70KΩ

In a first order approach, the extra delay due to the resistive open defect can be estimated by

$$t_{R_o} = R_o * C \tag{3.1}$$

Figure 3.3 shows that the delay increment due to a resistive open has a linear dependence on the resistance value of the open.

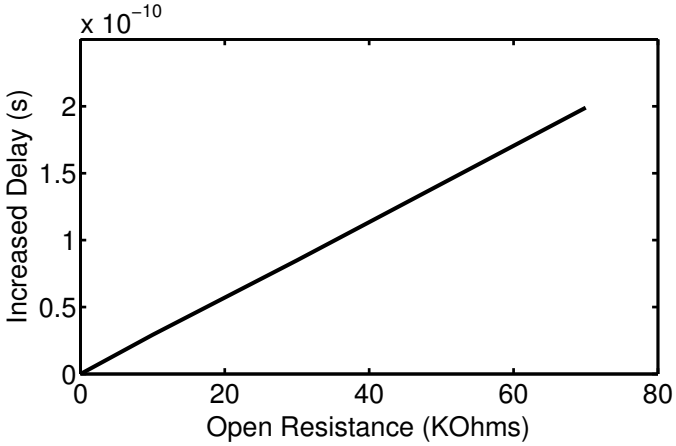


Figure 3.3: Linear dependence of the delay increment due to the resistance open value

Static timing and process parameter variations (L, W, Tox and Vth) analysis for the inverter chain (See Figure 3.1) are shown in Figure 3.4. A resistive open of R_o=100KΩ has been considered. The signals are the outputs (OUT) for the defect-free circuits (panel 1) and for the defective circuit (panels 2 & 3). The increased delay due to the resistive open defect is ≈220ps (see panel 2). Even more, the possible delay values due to the open in the presence of process parameter variations are in the range between ≈190ps and ≈250ps (see panel 3). It can be observed the importance to consider process parameter variations. This variability can impact the final operation of the product. Open defects producing small-delays are critical in performance of a circuit and they can escape test.

3.2.2 Proposed Methodology

An aware vector-less methodology to estimate the circuit testability for small delay defects due to resistive open defects is proposed. The circuit testability is evaluated analyzing the timing information of the circuit. Statistical timing analysis is used to compute the gates output(s) of a particular logic level analyzing the information at the gates input(s). Under this schema, the calculated timing information is then propagated to the next logic level until to reach the primary outputs. Then the outputs of the defect-free circuit and defective one are compared to determine the fault coverage of the circuit. This is used as the circuit testability metric.

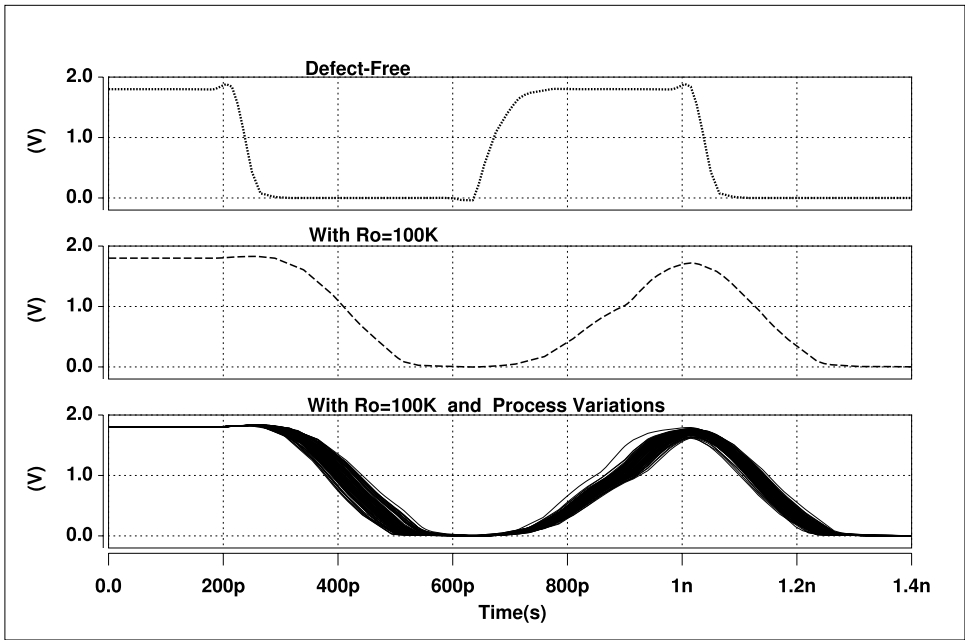


Figure 3.4: Static timing and process variation analysis with a resistive open $R_o = 100K\Omega$

In this work, we have developed an Statistical Fault Coverage (SFC) methodology. Our implemented Statistical Timing Analysis Framework (STAF) propagates the increased delay through all possible paths using the MAX function [81]. Because of this the longest path that includes the small delay defect under analysis is sensitized. Other trajectories are also sensitized.

An example of signal propagation using statistical timing analysis is illustrated in Figure 3.5. Signal delay on each node is represented by a random normal distribution, which include the effect of process parameter variations and nanometer technologies issues (spatial correlation, random placement of dopants and signal correlation). Timing information at the primary inputs (μ_{IN}, σ_{IN}) is propagated through the circuit until the primary outputs are reached. Input timing information arriving at each gate is processed using the MAX function to obtain the output timing information. Finally, timing information arriving at the primary outputs is used to calculate the circuit delay $(\mu_{cir}, \sigma_{cir})$. Signal correlation due to reconvergent paths is illustrated with the paths $P1$ and $P2$, starting at input $IN3$ and ending at output $OUT1$. In the presence of a resistive open defect R_o, the random normal distribution also includes the increased delay due to the open defect. Then, the small-delay induced by the interconnect defect is propagated through all possible paths until the primary outputs are reached. This propagation is done statistically.

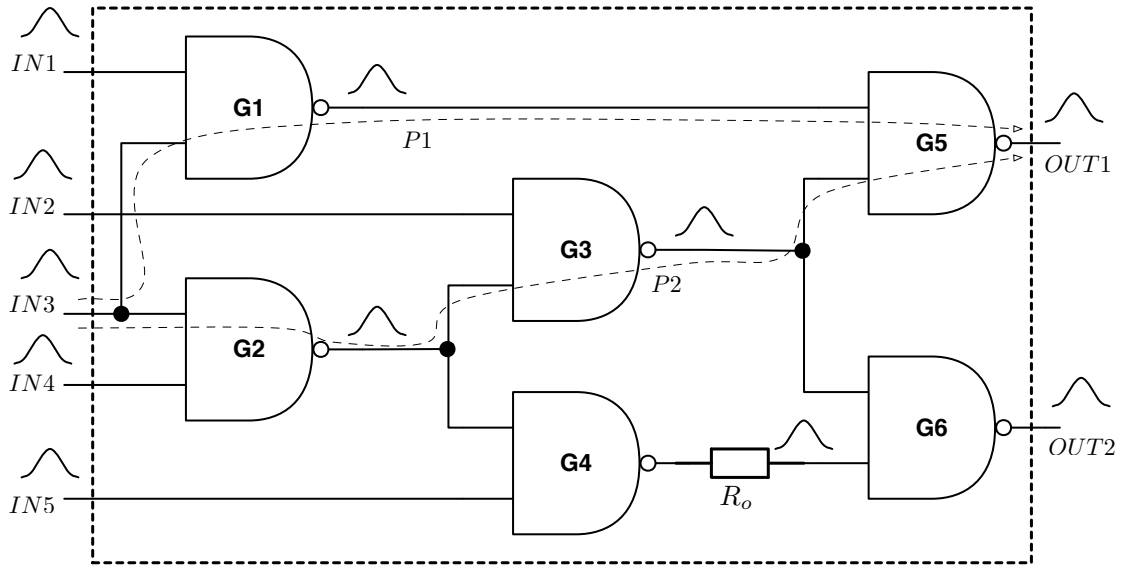


Figure 3.5: ISCAS circuit C17 illustrating the problem formulation

The statistical analysis methodology propagates the maximum delay of each output edge. Because of this the probabilistic delays (PDF function) at the outputs are obtained for each open location. In this work the maximum clock frequency is given by the circuit delay (PDF) of the defect-free circuit. Using the Statistical Timing Analysis Framework (STAF), the circuit delay is obtained applying the MAX function at the primary outputs. This procedure takes into account each mean and variance of each primary output. This ensures that the calculated circuit delay covers the delays of all the primary outputs.

In this work, the statistical fault coverage is obtained for all the possible open locations including also those open locations located in non-critical paths. This is because these opens could be a reliability issue [2].

3.3 Estimation of the Probability of Detection of a Resistive Open Defect

The *Probability of Detection* (P_{det}) is a metric of the circuit testability for small delay defects. In this chapter, the probability of detection of delay defects due to resistive open defects is computed based on three steps: First, timing information for the defect-free circuit delay is

obtained. Second, propagation of all the delay defects from the open location through all the possible paths until the primary outputs are reached and the defective circuit delay is obtained. Third, using the timing delay information of the defect-free and defective circuit, a proposed statistical methodology is applied to obtain the probability of detection of resistive opens. An Statistical methodology to evaluate the probability of detection of open defects for a single resistance value has been proposed. This has been extended to evaluate the probability of detection of an open for a range of resistances values. Finally, the statistical fault coverage of the circuit can be obtained.

3.3.1 Propagation of the Small Delay due to the Resistive Open

In order to propagate the small delay due to the resistive open through the different paths, this is added to the delay of the previous gate as Figure 3.6 shows. In other words, adding the gate delay D with the resistive open delay t_{R_o}, a defective gate delay D' value is obtained (See equation 3.2).

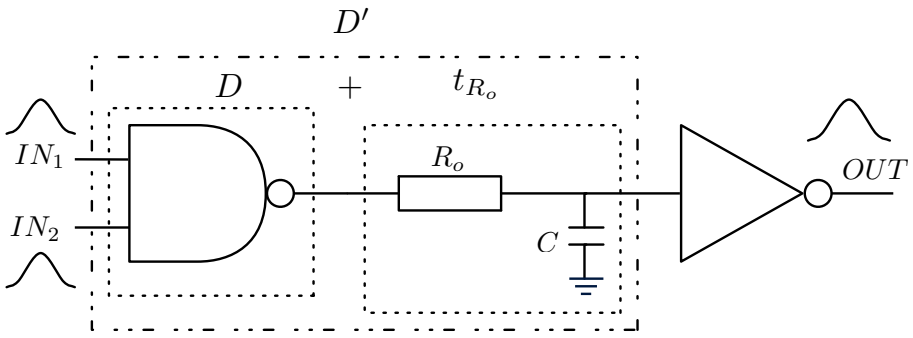


Figure 3.6: Association of the resistive open delay to the previous gate delay

$$D' = D + t_{R_o} \tag{3.2}$$

In the STAF the extra delay is included adding the resistive open delay t_{R_o} to the mean of the gate delay $D = (\mu_D, \sigma_D^2)$. The delay t_{R_o} includes the capacitance of the driven gates. After the sum of the open delay increment with the precedent gate delay, the MAX function is applied to obtain the mean and variance of the output gate delay. Then it is propagated to the next logic level until the primary outputs are reached. The STAF propagates the delay increment through

all possible paths using the MAX function. Because of this the longest path that includes the small delay defect under analysis is sensitized, other trajectories are also sensitized.

3.3.2 Probability of Detection of an Open for a Single Resistance Value

In this subsection, the probability of detection of an open for a single resistance value is obtained. The PDFs representing circuit delays for the defect-free circuit and for the circuit with an open defect (defective circuit) are obtained. Using these timing information and applying the proposed statistical methodology, the probability of detection of the open can be calculated. Basically, the timing information is composed by the mean and variance of normal distributions. Reminding that the normal distribution is given by the process parameter variations of the considered devices.

Figure 3.7 shows the simulation results, illustrated with the Probability Density Function (PDF), given by the STAF for the benchmark circuit ISCAS C432. An open location with a given resistance value of R_o=200KΩ has been considered. Signal circuit delay distributions for the defect-free circuit and other having a resistive open in an internal node are shown. Solid curve corresponds to the defect-free circuit delay and the dashed curve corresponds to the circuit delay with an open. Making comparison of both curves the probability of detection of the open gives 1. This is because all the delay occurrences for the defective circuit are larger than for the defect-free case. The defective circuit delay will be used to build the dashed line chart and compute the probability of detection.

Figure 3.8 shows the simulation results given by the STAF for another open location in the benchmark circuit ISCAS C432. The same value of resistance (R_o=200KΩ) for the open is considered. In this case, it can be observed that both curves intersect. Some of the delay occurrences of circuits having a resistive open defect may fall in a certain region below the defect-free curve. These delay occurrences are marked with a shaded area ($AREA$) in Figure 3.7. Because of this, delay occurrences in the shaded area are considered non-faulty. Therefore, for intersected delay curves the probability of detection of an open for a given resistance value can be estimated by

$$P_{det} = 1 - AREA \tag{3.3}$$

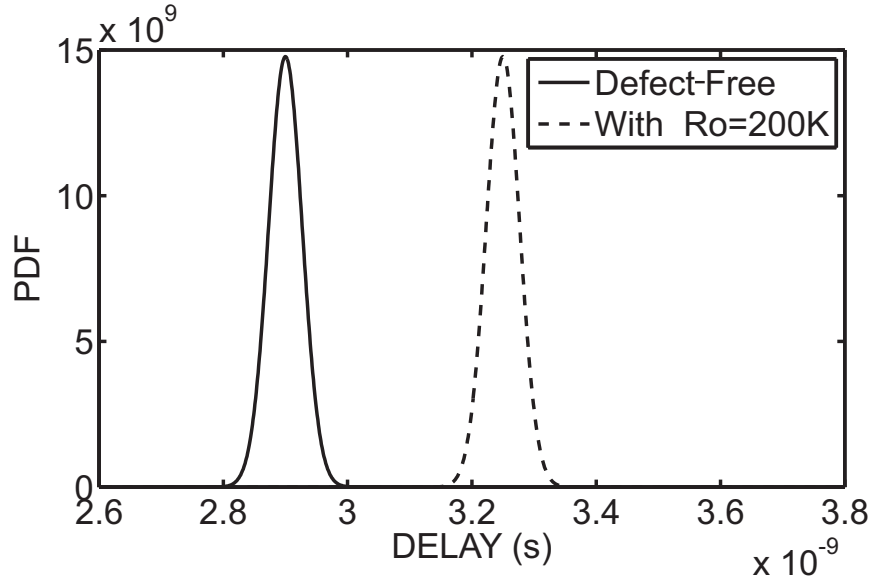


Figure 3.7: STAF simulation results for the circuit C432, at the internal node 192.

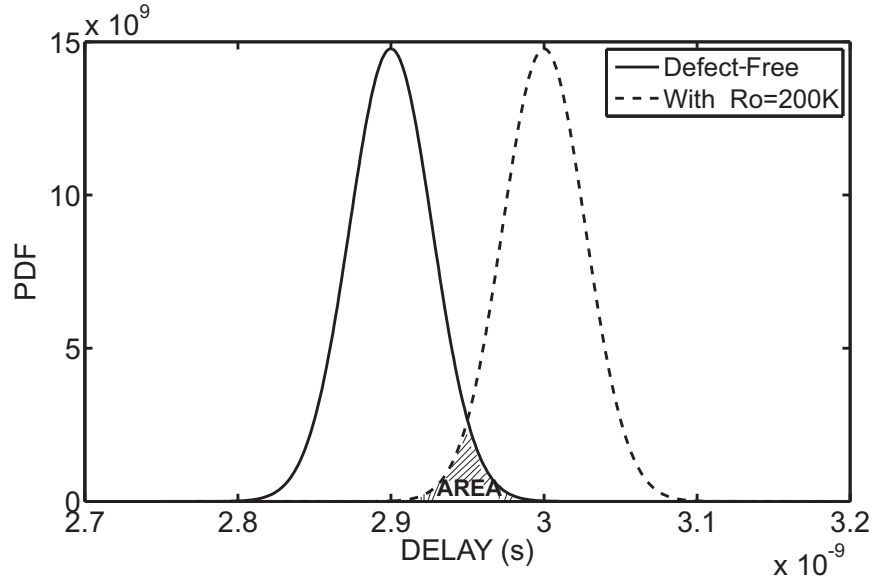


Figure 3.8: STAF simulation results for the circuit C432, at the internal node 105.

The shaded area (See Figure 3.8), $AREA$, represents the probability of error. The intersected area can be calculated from the complementary error function (*erfc*) given in the equation (3.4) [89].

$$AREA = \frac{2}{\sqrt{\pi}} \frac{\exp^{-x^2}}{x + \sqrt{x^2 + \frac{4}{\pi}}} \tag{3.4}$$

$$x = \frac{\mu_{fc} - \mu_{df}}{2\sigma\sqrt{2}} \tag{3.5}$$

where μ_{df} is the mean delay of the defect-free circuit, μ_{fc} is the mean delay of the defective circuit and σ is the standard deviation of the defect-free circuit. Using (3.3), (3.4) and (3.5), the probability of detection of an open for a given location and resistance value can be computed. The probability of detection of a resistive open of 200KΩ for the particular case shown in Figure 3.8 gives $P_{det} = 0.93$.

Another example is shown in Figure 3.9. For the same benchmark circuit ISCAS C432 and a different open location with a resistance value of R_o=170KΩ. Signal circuit delay distributions for the defect-free and defective circuits are shown. Solid curve corresponds to the defect-free circuit delay and the dashed curve corresponds to the circuit delay with the open. The probability of detection of a resistive open of 170KΩ for the particular case shown in Figure 3.9 gives $P_{det} = 0.73$.

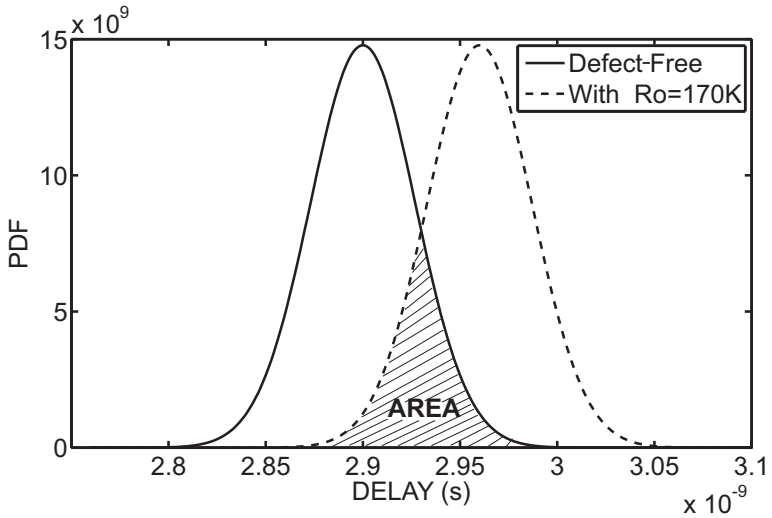


Figure 3.9: STAF simulation results for the circuit C432, at the internal node 15.

3.3.3 Probability of Detection of an Open for a Given Range of Resistance Values

The probability of detection of an open for a given range of resistance values (P_{det}^{R}) is obtained extending the concept of probability of detection for a single resistance value. To accomplish this the following aspects are considered:

1) The probability of detection for a single value of resistance of the open represents a conditional probability. This will be further explained later.

2) The delay increment has a linear dependence on the resistance value of the open (See Figure 3.3) [47][2]. According to this, it is assumed that the mean delay of the defective circuit (μ_{fc}) is directly related to the value of the resistive open R_o, as Figure 3.10 shows.

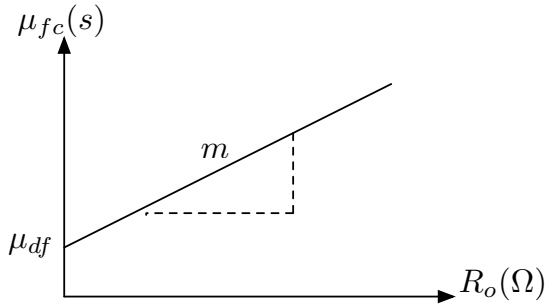


Figure 3.10: A linear approach to estimate the dependence of the μ_{fc} on the R_o value. The slope m is different for each open location.

A linear approach of first order (See Figure 3.10) can be used to estimate the dependence of the mean delay of the defective circuit (μ_{fc}) on the value of the resistive open (R_o) as shown by

$$\mu_{fc} = mR_o + \mu_{df} \tag{3.6}$$

where m is the slope that define the rate of change for the mean delay of the defective circuit with respect to the value of the open.

Thus, substituting (3.6) in (3.5) and this in (3.4), the defined probability of detection in (3.3) can be rewritten in function of the open resistance value, as shown by

$$P_{det} = 1 - AREA(R_o) \tag{3.7}$$

3) We assume that the standard deviation for the new distribution of the defective circuit is the same as the defect-free circuit [2], this means that the resistive open only affects the mean.

The probability of detection for a range of resistance values of the open can be estimated using the concept of Joint Probability ($f_{X,Y}(x,y)$) of two random variables X and Y [90]. The variable X represents the detection of the open for the considered resistance range and the variable Y represents the presence of the open (R_o) for the considered resistance range. The marginal probability density is used to calculate the probability of detection of the open for the range of resistance values. Then, given X and Y whose joint distribution $f_{X,Y}(x,y)$ is known, the marginal distribution of X ($f_X(x)$) is the probability distribution of X averaging over information about Y. $f_X(x)$ is the PDF representing the probability of detection of an open for a given range of resistance values (P^R_{det}). This is calculated by integrating the joint probability distribution over Y as shown in equation (3.8) [90].

$$P^R_{det} = f_X(x) = \int_y f_{X,Y}(x,y)dy \tag{3.8}$$

From the Bayes' theorem, is known that the conditional probability is the probability of some event, given the occurrence of some other event. For probability densities (continuous distributions) this is given by

$$\begin{aligned} f_{X|Y}(x|y) &= \frac{f_{X,Y}(x,y)}{f_Y(y)} \\ f_{X,Y}(x,y) &= f_{X|Y}(x|y)f_Y(y) \end{aligned} \tag{3.9}$$

Since, we assume the probability of detection for a single value of resistance of the open represents a conditional probability, using (3.9), equation (3.8) can be rewritten as follows:

$$P^R_{det} = f_X(x) = \int_y f_{X,Y}(x,y)dy = \int_y f_{X|Y}(x|y)f_Y(y)dy \tag{3.10}$$

In the definition of Joint Probability, the variable Y represents R_o, thus, the probability of detection is rewritten as follows

$$P_{det}(y) = f_{X|Y}(x|y) = 1 - AREA(y) \tag{3.11}$$

where $AREA(y)$ represents the probability of error as function of the resistance value y as given by equation (3.7).

In this work, the probability density function ($f_Y(y)$) of the resistance (R_o) has been assumed to be uniform in the range $[a-b]$. The PDF of the resistance is plotted in Figure 3.11. The limits a and b represent the minimum and maximum values of the resistive open which corresponds to the minimum and maximum small delays considered. Thus, the occurrence probability of any value of resistance in the selected range is given by

$$f_Y(y) = \frac{1}{b-a} \tag{3.12}$$

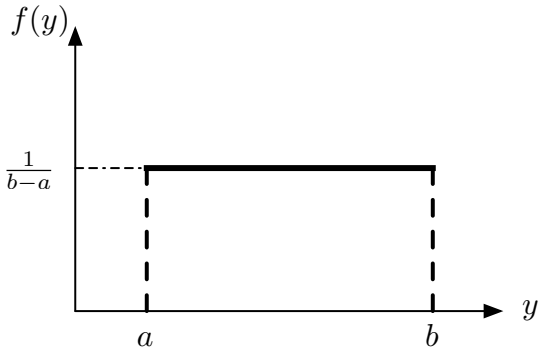


Figure 3.11: Probability density function for the resistance R_o ($y = R_o$)

Replacing equation $f_Y(y)$ and $P_{det}(y)$ in equation (3.10), the probability of detection of the open for the considered range of resistance values is given by the following expression

$$P^R_{det} = f_X(x) = \frac{1}{b-a}\int_a^b (1 - AREA(y))dy \tag{3.13}$$

3.3.4 Statistical Fault Coverage

Statistical Fault Coverage (SFC) will be used to evaluate the circuit testability for resistive opens of a circuit. This is evaluated for a range of resistive opens producing small delays. The SFC is calculated as the ratio of the sum of the probabilities of detection for all the open locations to the total number of opens considered. Then, the SFC of a circuit with n opens can be estimated by

$$Statistical \;\; Fault \;\; Coverage = \frac{\sum_n f_X(x)}{n} * 100\% \tag{3.14}$$

The detected faults in this work are not deterministic instead statistical, then, the detected faults are given in a measure of probability of detection in the range [0 - 1]. Values close to "0" means low probability of detection and close to "1" indicates a high probability of detection. Moreover, this methodology gives a more realistic approach in the measurement of the actual detectability of resistive opens producing small delays.

Let us consider that resistive opens are the internal faults which produce small delays, hence, we can define the circuit testability as the probability that small delay defects will result in an externally visible increment in the circuit delay. Thus, SFC will be a metric to evaluate the circuit testability for small delay due to resistive open defects.

3.4 Example of the Methodology

Step by step, a procedure has been developed to show the proposed methodology. The ISCAS circuit C432 has been used in order to exemplify the methodology

1. The PDFs at the outputs for the defect-free circuit are obtained. The MAX function at the outputs is applied.

2. Then, an internal node in the circuit is chosen, ex. node 192.

3. A resistance range for the open defect is defined [R_{oa} - R_{ob}]. Ex. R_o = [10Ω - 200KΩ]

4. Defective circuit delays (PDF) for R_{ob} at the chosen open location are obtained.

5. The slope m that define the rate of change for the mean delay of the defective circuit for any resistance open on that particular node is calculated using both defect-free and defective circuit delay.

6. Using the slope m, defective circuit delay for any resistance open value on that node is considered. Then, the intersection area $AREA$ can also be obtained.

7. The probability distribution function ($f_Y(y)$) of the resistance open values occurrence is defined. For this work a uniform distribution has been assumed.

8. For a uniform distribution of the resistance open values ($f_Y(y) = \frac{1}{b-a}$) , the probability of detection of an open for a range of resistance values is computed:

$$P_{det}^{R} = f_X(x) = \frac{1}{b-a}\int_a^b (1 - AREA(y))dy$$

This is done, sing the PDFs information of Figure 3.7, 3.8 and 3.9 which corresponds on the internal nodes 192, 105 and 15 respectively, and applying this procedure, we can compute the probability of detection for resistive opens ranging from 10Ω to 200KΩ; resulting in $f_X(x) = 0.87$, $f_X(x) = 0.58$ and $f_X(x) = 0.83$ respectively.

9. Finally, once the probability of detection of the considered range of resistive opens for all open location (n) have been obtained, the statistical fault coverage (SFC) can be calculated as follows.

$$SFC = \frac{\sum_n f_X(x)}{n} * 100\%$$

3.5 Simulation Results

The proposed methodology has been applied to some ISCAS-85 benchmark digital circuits implemented with TSMC 0.18μm technology. Mentor Graphics Tools were used to implement the benchmark circuits. The ASIC Design Kit (ADK v3.1) was utilized to create each circuit. From these, netlist at different hierarchy levels are extracted. These are feed into the STAF to be processed. More information can be found on Appendixes A and B.

Table 3.1 shows the Statistical Fault Coverage results for the considered ISCAS benchmark circuits. The resistance values of the open ranges from 10Ω to 200KΩ, and a uniform distribution has been assumed. The data given are: the number of logic levels (LL), the mean (μ) and the standard deviation (σ) of the delay of the defect-free circuits, the total number of opens considered, and the Statistical Fault Coverage (SFC) of the circuit. The number of logic levels means the logic depth of the circuit.

Table 3.1: SFC results for some ISCAS benchmark circuits. Resistance range: [10Ω - 200KΩ]

CIRCUIT	LL	MEAN (μ)[ns]	SD (σ)[ps]	OPENS	SFC (%)
C432	22	2.89	27	162	76.5
C499	12	1.72	29	158	96.7
C1908	20	2.31	26	200	85.2
C2670	30	2.29	77	356	49.0
C3540	35	3.17	49	898	46.7
C6288	91	8.62	63	1618	61.5

SFCs higher that 50% are obtained for the circuits C432, C499, C1908 and C6288. One of the reason of these values may be because the delay due to the open is propagated through all the possible paths starting from open location. This propagation is limited by the MAX function. A SFC lower than 50% is obtained for circuit C2670 and C3540. This could be explained by the fact there is a small set of primary outputs having higher logic levels than the rest of primary outputs. It can also been observed that the number of logic levels affects the probability of detection of the opens. Circuits with fewer logic levels have higher probability of detection than circuits with many logic levels.

Therefore, it can be stated that circuits C432, C499, C1908 and C6288 present better circuit testability for small delay defects due to resistive opens, and that circuits as C2670 and C3540 have a lower circuit testability. Thus, the circuit testability to the detection of small delays due to resistive open defects depend on its architecture [91].

3.6 Conclusions

In this chapter, an aware methodology to evaluate circuit testability for small delay defects due to resistive opens in the presence of process variations has been presented. A STAF is used to propagate small delays due to resistive opens considering process variations. Important nanometer technologies issues are considered. Process parameter variations are considered, which have become a critical issue affecting the performance and test of nanometer digital circuits. Statistical metric have been developed to evaluate the probability of detection of resistive opens for a given range of values.

Using the probability of detection of the opens the statistical fault coverage (SFC) of the circuit is obtained. The SFC gives an indication of the circuit testability for small delay defects due to resistive opens. Using the proposed methodology, the SFC of resistive opens producing small delays is evaluated for some ISCAS benchmark circuits, which is a metric of the circuit testability.

It can been observed that the number of logic levels affects the probability of detection of the opens. Circuits with fewer logic levels have higher probability of detection than circuits with many logic levels. Hence, the architecture of the circuit influence the fault coverage of a circuit. Thus, the circuit testability for small delays due to resistive open defects depend on its architecture.

Chapter 4

Resistive Bridge Defects

In this chapter, an aware methodology to evaluate circuit testability for small delay defects due to resistive bridges in the presence of process variations is presented. An Statistical Timing Analysis Framework is used to propagate delays. An statistical methodology to estimate the probability of detection of resistive bridge defects is proposed. Using the probability of detection the Statistical Fault Coverage (SFC) of the circuit is obtained. An exhaustive analysis is done, i.e. the SFC is obtained for all the possible bridge locations. The SFC gives an indication of the circuit testability for small delay defects due to resistive bridges. The methodology is applied to some ISCAS benchmark circuits. This Chapter is organized as follows: In Section 4.1, state of the art of bridge defects on nanometer technologies is introduced. In Section 4.2, formulation of the problem and the proposed methodology are given. In Section 4.3 the procedure to estimate the probability of detection and the SFC of the circuit for bridge defects is developed. In Section 4.4, an example of the methodology is given. In Section 4.5, the simulation results for ISCAS circuits are presented. Finally, the conclusions of this chapter are given in Section 4.6.

4.1 Introduction

Resistive bridge is another interconnect defect that has a high occurrence in nanometer circuits [6]. Bridges (or shorts) occur when two or more distinct nodes of the circuit get connected due to a defect. Bridge defects have an immeasurable effect on signal timing, unless the bridge impedance is in a sensitive range [6] [14]. Severity of a bridge is inversely proportional to its resistance. For high values of resistive bridges, a bridge has nearly no impact on delay. As the bridge resistance decreases, the slow-down/speed-up effect becomes more severe. At some resistance value, the bridge behavior becomes severe enough to cause logic error.

For a particular bridge, the maximum bridge resistance for which logic error occurs can be referred to as the bridge's critical resistance (R_{crit}) [15]. Previous woks consider the critical bridge resistance ranges between 500Ω to 1000Ω [12][15][16]. The value of the critical resistance may depend mainly on their bridge position and on the drivers of the lines involved in the bridge. If the drivers of the lines are weaker, then the critical resistance is higher, and vice-versa [15]. The bridge position can significantly impact not only the delay caused due to the bridge but also the critical resistance value. However, the dependence of the delay on the bridge position is significant only for bridge resistance values close to the critical resistance [15]. For resistances upper than the critical resistance, the position of the bridge has a very small impact on the delay [15].

Bridges with resistances lower than the critical resistance can typically be modeled as a logic fault and may be detected with a Boolean test based on the Stuck-at fault model [16]. Resistances upper than the critical resistance may only alter delay values, and are almost undetectable with a Boolean test [17][18] and more sophisticated tests are required. A resistive bridge whose resistance is not low enough to cause a logic error for low speed tests could be called a weak resistive bridge (WRB) [92]. A WRB between a pair of lines, namely an aggressor line and a victim line, may slow-down a transition at the victim line under certain conditions. If the delayed transition at the victim line is propagated to circuit outputs, it may cause timing errors [15] [93]. Therefore, testing for WRB-induced slow-down is essential.

The bridge slow-down delay is a function of the bridge degrading the voltage levels combining with the victims own capacitance [12]. The longest delays will occur with bridges when the victim is rising (falling) and the aggressor is low (high). If the aggressor is appreciably faster than the victim, or if its transitions are slightly earlier, it would not matter what its previous level was but otherwise the longest delay occurs when aggressor is at a constant level. It may arise that two bridged nodes have equal strength drivers but that their pull-up and pull down strengths are unequal. If both nodes have a weak pull-up, each may assume the role of victim when the other is low [12]. Bridge speed-up can also occur when the victim starts from a degraded level, e.g. the victim is rising and the aggressor is high [12].

For any given pair of nodes, low resistance bridges up to some critical resistance value can lead to static errors. For some range above the critical resistance, the bridge may yet be detected

by the delay that it causes or by IDDQ tests [6][13][94]. Several authors have looked at increasing the range of bridge resistance that may be detected by logic or by delay-fault tests by testing at low supply voltage, and high temperature [94][95].

4.2 Assessment and Proposed Resolution to the Problem

4.2.1 Formulation of the Problem

Resistive bridges are another interconnect defect that has a high occurrence in advanced CMOS technologies [6]. For a particular bridge, the bridge resistance for which logic error occurs can be referred as the critical bridge resistance. The value of the critical resistance may depend mainly on their bridge position and on the drivers of the lines involved in the bridge. Since we are interesting in bridges that produce small delay faults difficult to detect, then, this work focus on resistive bridges higher than their critical resistance. For resistances upper than the critical resistance, the position of the bridge has a very small impact on the delay [15], thus, it is not considered in this work. The effect of resistive bridge defects producing small delays is analyzed and a model to capture the effect is presented. The used model is based on the proposal by Zhuo Li et al. [47].

Nets affected by bridge defects can be identified from the coupling capacitance information [96]. We are excluding those that incorporate the power supply nets (VDD and GND) and any input/output port.

Figure 4.1 shows a circuit with two inverters chain interconnected with a resistive bridge. R_b typify the resistance of the bridge defect, and C_1, C_2 the capacitances due to the respective loading gates. This represents a resistive bridge fault model. In this schematic, parasitic resistances and capacitances have not been included.

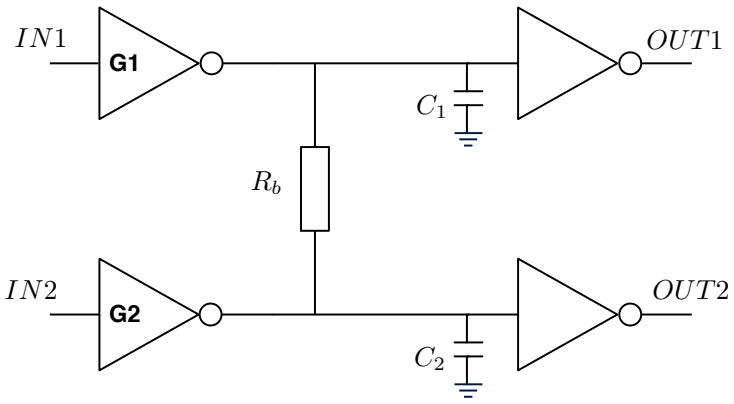


Figure 4.1: Example circuit illustrating the resistive bridge fault model

Figure 4.2 shows the electrical behavior of the circuit modeling the resistive bridge defect (See Figure 4.1). Resistive bridge values considered for this example are: 10KΩ, 5KΩ, 3KΩ, 1KΩ and 500Ω. The signals are the outputs for the defect-free and for the defective circuit. The charts in Figure 4.2 correspond for the $OUT1$ in the circuit with the input pattern $IN1$=falling, $IN2$=1. It can been observed that the resistive bridge defect produces small delays of approximately 4ps up to 86ps. Thus, depending on the location of this bridge defect in the circuit a delay fault may appear.

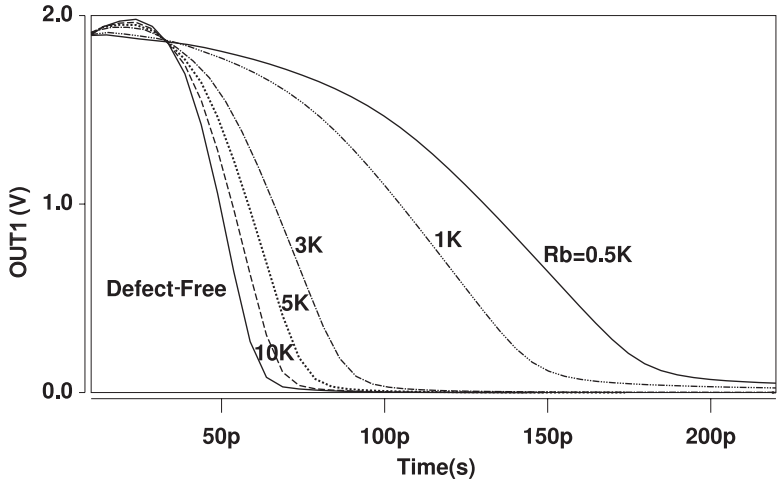


Figure 4.2: Electrical response for $OUT1$ with an increase of the delay ($IN1$=fall, $IN2$=1). Resistances values: 10KΩ, 5KΩ, 3KΩ, 1KΩ and 500Ω

For the bridge case, the increased delay has an exponential behavior on the resistance value of the bridge R_b (negative exponential behavior) as Figure 4.3 shows [15]. This means that the rate of change for the mean delay of the defective circuit in resistive bridges ranges from a to b, where a and b represent the minimum and maximum value considered resistance values, respectively. Then, larger delay increments exits for those bridges close to a and smaller delay increments exist for those bridges close to b.

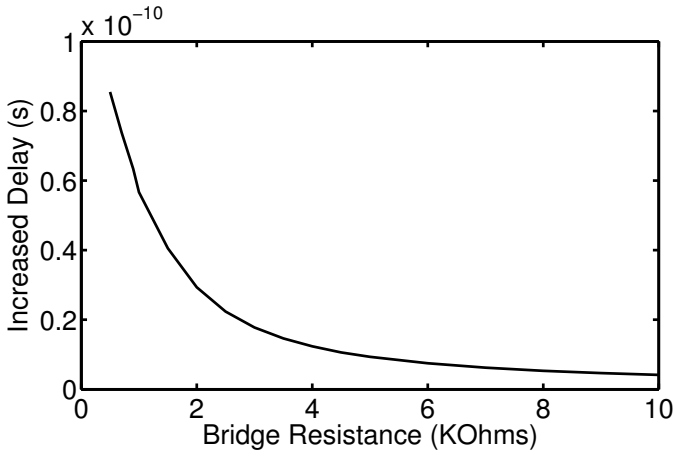


Figure 4.3: Delay behavior on the resistance value of the bridge defect. Relationship between R_b and increased delay at the output

Static timing and process parameter variations (L, W, Tox and Vth) analysis for the defect-free inverter chain (See Figure 4.1) and defective one for a given bridge resistance values are shown. connected with the bridge are shown in Figure 4.4. A resistive bridge of R_b=1KΩ has been considered and the inputs $IN1$=pattern and $IN2$=1. The signals are the outputs ($OUT1$) for the defect-free circuit (panel 1) and for the defective circuit (panels 2 $\&$ 3). The increased delay due to the resistive bridge defect is $\approx$59ps (see panel 2). Even more, the possible delay values due to the bridge in the presence of process parameter variations are in the range between $\approx$83ps and $\approx$160ps for the falling transition (see panel 3). It can be observed the importance to consider process parameter variations. This variability can impact the final operation of the product. Bridge defects producing small-delays are critical in performance of a circuit and they may escape test. Furthermore, small-delay defects can cause reliability issues [2].

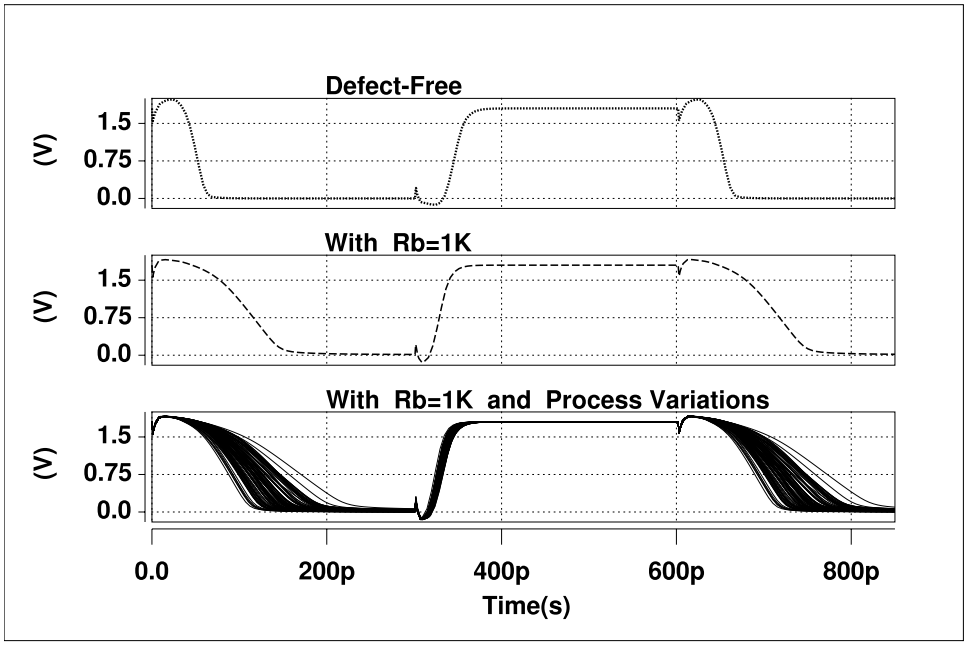


Figure 4.4: Static timing and process variation analysis with a resistive bridge $R_b = 1K\Omega$

4.2.2 Bridge Delay Fault Modeling

Traditional bridge fault models include functional fault models or delay fault models. A bridge fault model incorporating both functional and delay is presented by Zhuo Li et al. [47][97]. The increased delay induced by the bridge defect at each affected node is calculated using the mathematical model proposed by Zhuo Li et al. [47][97]. The mathematical model is obtained making a static and dynamic analysis of a RC network that lumps interconnect parasitics capacitance with load capacitance and logic gates replaced by switches and linear resistors. In this work, we do not consider the RC interconnect component. Then, parasitic resistances and capacitances due to interconnections are not considered in the model.

Figure 4.5 shows a simplified circuit of Figure 4.1. The logic gates G1, G2 (See Figure 4.1) are replaced by switches and linear resistors. R_{up} and R_{down} are the resistances of the PMOS and NMOS transistors, respectively, both operating in the linear region.

The expression to model the resistive bridge delay at each output is given by

$$d_{b,i} = (-c * log_2\left(\frac{0.5 - h}{g - h}\right) - 1) * d_{o,i} \tag{4.1}$$

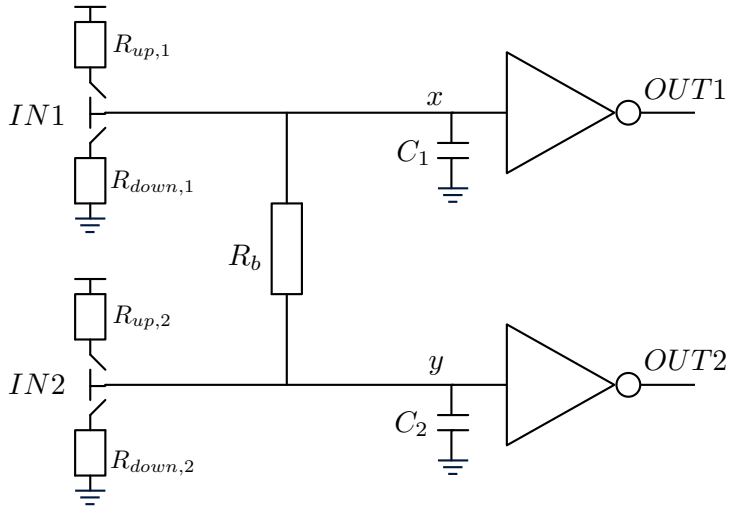


Figure 4.5: Example circuit illustrating the simplified bridge fault model

The parameters c, h and g are calculated according to the input pattern ($IN1, IN2$), and the way to calculate them are given in Table 4.1. $d_{o,i}$ is the nominal delay of the outputs $OUT1$ or $OUT2$ (i = 1 for $OUT1$ and i= 2 for $OUT2$). For simplicity, the delay of $OUT1$ ($OUT2$) means the delay at node x (y). Then, $d_{b,i}$ is the increased or decreased delay due to the resistive bridge defect for the affected line. So, c, h and g parameters are in function of the resistances and capacitances included in the simplified bridge fault model (See Figure 4.5).

Table 4.1 shows the output behavior for $OUT1$ according to the input pattern. It is assumed that the two input signals change simultaneously. The coefficients a_1, a_2, b_1 and b_2 can be calculated using equation (4.2) [97].

$$
\begin{aligned}
a_1 &= 1 + \frac{R_{down,2}^2}{(R_{down,2} + R_b)^2} \frac{C_2}{C_1} \\
a_2 &= 1 + \frac{R_{up,2}^2}{(R_{up,2} + R_b)^2} \frac{C_2}{C_1} \\
b_1 &= \frac{(R_{down,2} + R_b)}{(R_{down,2} + R_{up,1} + R_b)} \\
b_2 &= \frac{(R_{up,2} + R_b)}{(R_{down,1} + R_{up,2} + R_b)}
\end{aligned}
\tag{4.2}
$$

Input Pattern ($IN1$, $IN2$)	$OUT1$ behavior
Both static (0,0),(0,1),(1,0),(1,1)	NO ID nor DD
same direction (r,r),(f,f)	NO ID nor DD
$IN1$ static (0,r),(0,f),(1,r),(1,f)	NO ID nor DD
(r, 0)	ID, $g = 0$, $h = b_1$, $c = a_1 * b_1$
(f, 0)	DD, $g = b_1$, $h = 0$, $c = a_1 * b_1$
(r, f)	ID or DD, $g = 1 - b_2$, $h = b_1$, $c = a_1 * b_1$
(f, r)	ID or DD, $g = b_1$, $h = 1 - b_2$, $c = a_2 * b_2$
(r, 1)	DD, $g = 1 - b_2$, $h = 1$, $c = a_2 * b_2$
(f, 1)	ID, $g = 1$, $h = 1 - b_2$, $c = a_2 * b_2$

Table 4.1: Behavior at the output $OUT1$ according to input pattern. Increased Delay (ID) or Decreased Delay (DD). Rise $0 \rightarrow 1$ (r) and Fall $1 \rightarrow 0$ (f) transitions. [97]

Similar results for $OUT2$ can be derived from Table 4.1 by substituting $OUT2$ for $OUT1$, input pattern ($IN2$, $IN1$) for ($IN1$, $IN2$). Equations (4.1) and (4.2) need to be recomputed by exchanging all the subscripts 1 with 2.

4.2.3 Proposed Methodology

In this chapter, an aware vector-less methodology to estimate the circuit testability for small delay defects due to resistive bridge defects is proposed. The circuit testability is evaluated analyzing the timing information of the circuit. Measures can be taken for those circuits presenting poor circuit testability. More information about the methodology can be found in the Chapter 3.

An example of signal propagation using statistical timing analysis is shown in Figure 4.6. Signal delay on each node is represented by a random normal distribution, which include the effect of process parameter variations and issues in nanometer technologies (spatial correlation, random placement of dopants and signal correlation). Timing information at the primary inputs (μ_{IN}, σ_{IN}) is propagated through the circuit until the primary outputs. Input timing information arriving at each gate are processed using the MAX function to get an output timing information. Finally, timing information arriving at primary outputs is used to calculate the circuit delay (μ_{cir}, σ_{cir}). Signal correlation due to reconvergent paths is illustrated with the paths $P1$ and $P2$, starting at output of gate G2 and ending at output $OUT2$. In the presence of a resistive bridge defect R_b, the random normal distribution also includes the increased delay due to the

bridge defect. Then, the small-delay induced by the interconnect defect is propagated through all possible paths until the primary outputs are reached. This propagation is done statistically.

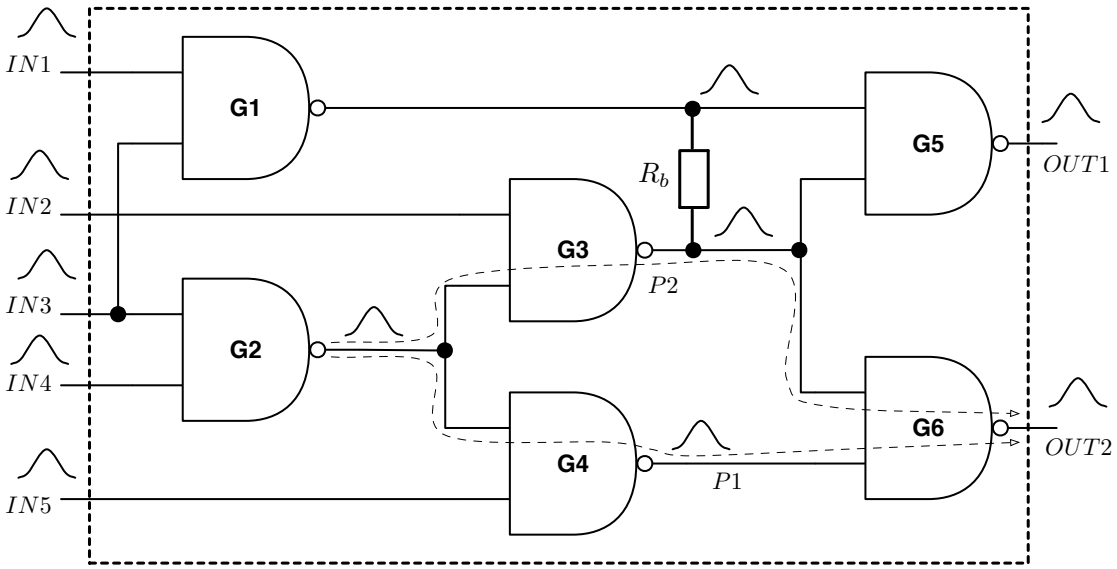


Figure 4.6: ISCAS circuit C17 illustrating the problem formulation

In this work, the statistical fault coverage is obtained for all the possible bridge locations including also those bridge locations located in non-critical paths. This is because these bridges could be a reliability issue [4][5].

4.3 Estimation of the Probability of Detection of a Resistive Bridge Defect

The *Probability of Detection* (P_{det}) is a metric of the circuit testability for small delay defects. To calculate the probability of detection of delay defects due to resistive bridge defects, the same methodology for open defects is used, but with slight variants. The mean of the defective circuit (μ_{fc}) is calculated using a different approach when the probability of detection of a bridge for a single resistance value is extended to consider a range of resistance values.

4.3.1 Propagation of the Small Delay due to the Resistive Bridge

The propagation of the delays due to the resistive bridge through the paths in the circuit is done in the same way that the propagation delays for resistive open defects. The bridge delay is integrated with the previous gate delay at the affected node, as Figure 4.7 shows. In other words, adding the gate delay D with the resistive bridge delay d_b, a defective gate delay D' value is obtained for the affected node (See equation 4.3).

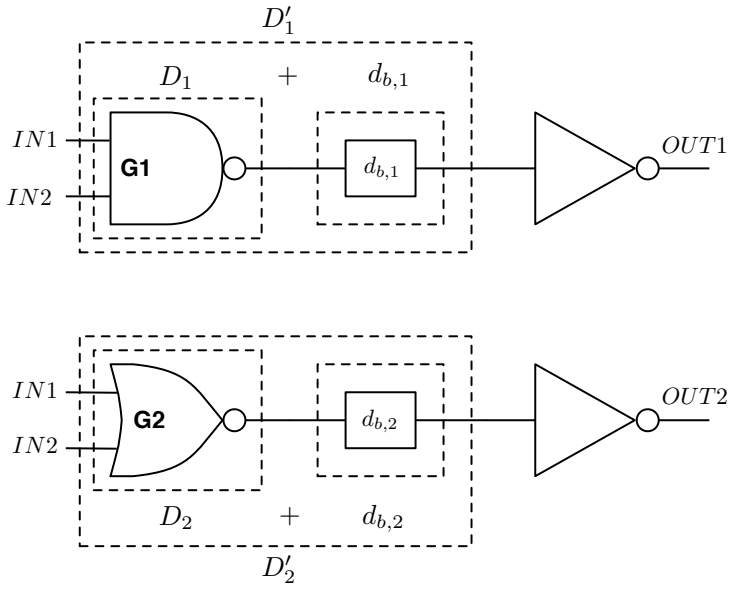


Figure 4.7: Summing the resistive bridge delay to the previous gate delay

$$D'_i = D_i + d_{b,i} \qquad i = 1or2 \tag{4.3}$$

In the STAF the extra delay is included adding the resistive bridge delay d_b to the mean of the affected gate delay $D = (\mu_D, \sigma_D^2)$. After summing the resistive bridge delay with the precedent gate delay, the MAX function is applied to obtain the mean and variance at the output gates. Then it is propagated to the next logic level until the primary outputs are reached.

For the bridge case, two delays for each bridge location are calculated, but only the one with the greater delay increment is considered for fault coverage estimation. This means that the SFC is estimated for the most favorable delay of the affected node. Taking into account the model

used to calculate the delay increment, the greater delay increment corresponds to the node with lower load capacitance [97].

4.3.2 Probability of Detection of a Bridge for a Single Resistance Value

In this subsection, the probability of detection of a bridge for a single resistance value is obtained. The PDFs representing circuit delays for the defect-free circuit an other with a bridge defect (defective circuit) are obtained. Using this timing information and applying a proposed statistical methodology, the probability of detection can be calculated. Basically, the timing information refers to the mean and variance of normal distributions.

Figure 4.8 shows the simulation results given by the STAF for one bridge location of the benchmark circuit ISCAS C432. A resistance value of R_b=1KΩ for the resistive bridge has been considered. Circuit delays for the defect-free and defective circuits are shown. Solid curve corresponds to the defect-free circuit delay and the dashed curve corresponds to the circuit delay with the bridge. Some of the delay occurrences of circuits having a resistive bridge defect may fall in a certain region below the defect-free curve. These delay occurrences are marked with a shaded area ($AREA$) in Figure 4.8. Because of this, delay occurrences in the shaded area are considered non-faulty.

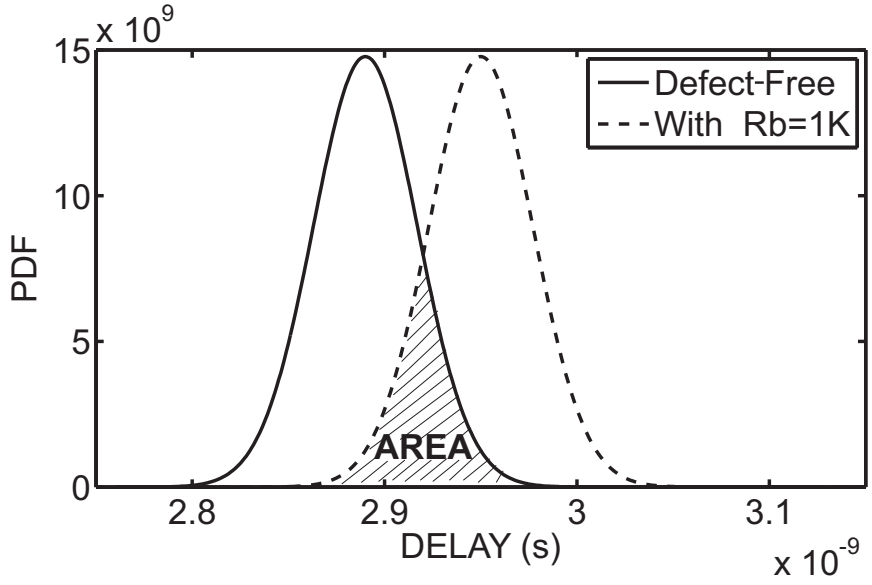


Figure 4.8: Results from the STAF for the circuit C432 with R_b=1KΩ, at the internal nodes (27, 14). The probability of detection is $P_{det} = 0.73$.

As given in Chapter 3 for the case of opens, the probability of detection of a bridge defect for a given resistance value can be estimated by the following expression:

$$P_{det} = 1 - AREA \tag{4.4}$$

The shaded area (See Figure 4.8), $AREA$, represents the probability of error. The intersected area can be calculated from the complementary error function (*erfc*) [89], given by

$$AREA = \frac{2}{\sqrt{\pi}} \frac{\exp^{-x^2}}{x + \sqrt{x^2 + \frac{4}{\pi}}} \tag{4.5}$$

$$x = \frac{\mu_{fc} - \mu_{df}}{2\sigma\sqrt{2}} \tag{4.6}$$

where μ_{df} is the mean delay of the defect-free circuit, μ_{fc} is the mean delay of the defective circuit and σ is the standard deviation of the defect-free circuit.

The probability of detection for a given location and resistance value of the bridge, can be computed using (4.4), (4.5) and (4.6). The probability of detection of a resistive bridge of 1KΩ for the particular case shown in Figure 4.8 gives $P_{det} = 0.73$.

For the case, where not intersection exist between the delay curves, the probability of detection of the bridge is $P_{det} = 1$. This is because all the delay occurrences for the defective circuit are larger than for the defect-free case.

4.3.3 Probability of Detection of a Bridge for a Given Range of Resistance Values

The probability of detection of a bridge for a given range of resistance values (P^R_{det}) is obtained extending the concept of probability of detection for a single resistance value. To accomplish this the following aspects are considered:

1) The probability of detection for a single value of resistance of the bridge represents a conditional probability. This will be further explained later.

2) The delay increment has a negative exponential dependence on the resistance value of the bridge (See Figure 4.3) [97]. According to this it is assumed that the mean delay of the defective circuit (μ_{fc}) is assumed to be inversely related to the value of the resistive bridge (R_b) as Figure 4.9 shows

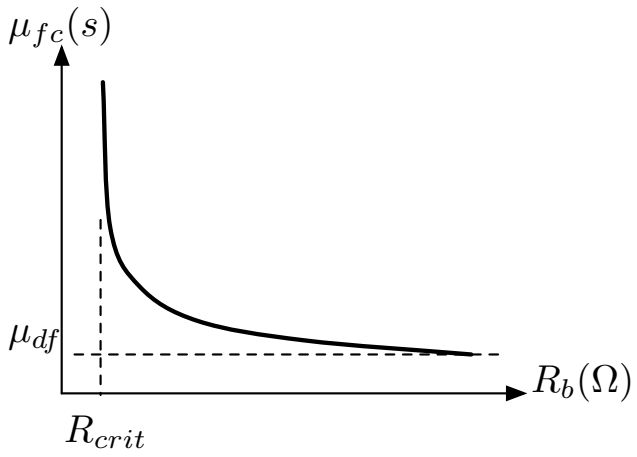


Figure 4.9: An hyperbola approach to estimate the dependence of the μ_{fc} on the R_b value. The constant k is different for each bridge location.

An hyperbola approach of first order (See Figure 4.9) can be used to estimate the dependence of the mean delay of the defective circuit (μ_{fc}) on the value of the resistive bridge (R_b) as shown by

$$\mu_{fc} = \frac{k}{R_b} + \mu_{df} \tag{4.7}$$

where k is the constant that define the rate of change for the mean delay of the defective circuit. The value of k used to evaluate a range of resistive values is obtained averaging two k's values previously calculated for two values of resistance. $R_b = 1K\Omega$ and $R_b = 3K\Omega$ were used. Then, the value of k can be approached by $k = k(1K\Omega) + k(3K\Omega)/2$.

Thus, substituting (4.7) in (4.6) and this in (4.5), the defined probability of detection in (4.4) can be rewritten in function of the bridge resistance value, as shown by

$$P_{det} = 1 - AREA(R_b) \tag{4.8}$$

3) For bridge defects, it has also been assumed that the standard deviation for the new distribution of the defective circuit is the same than that the defect-free circuit, which means that the resistive bridge defect only affects the circuit mean delay.

Using the concept of Joint Probability ($f_{X,Y}(x,y)$) [90], the probability of detection for a range of resistance values of the bridge can be estimated. The variable X represents the detection of the bridge for the considered resistance range and the variable Y represents the presence of the bridge (R_b) for the considered resistance range. Given X and Y whose joint distribution $f_{X,Y}(x,y)$ is known, the marginal distribution of X ($f_X(x)$) is the probability distribution of X averaging over information about Y. Thus, $f_X(x)$ is the PDF representing the probability of detection of a bridge for a given range of resistance values (P^R_{det}). This is calculated by integrating the joint probability distribution over Y as shown in equation (4.9).

$$P^R_{det} = f_X(x) = \int_y f_{X,Y}(x,y)dy = \int_y f_{X|Y}(x|y)f_Y(y)dy \tag{4.9}$$

In the definition of Joint Probability, the variable Y also represents the resistance R_b , thus, the probability of detection can be rewritten as $P_{det}(y) = f_{X|Y}(x|y) = 1 - AREA(y)$. $AREA(y)$ represents the probability of error as function of the resistance value R_b as given by (4.8).

The probability density function of the resistance of the bridge ($f_Y(y)$) has been assumed to be uniform in the range [a to b]. This is given by $f_Y(y) = \frac{1}{b-a}$. The limits a and b represent the minimum and maximum values of the resistive bridge which correspond to the maximum and minimum small delays considered.

Replacing the density function of the resistive bridge $f_Y(y)$ and $P_{det}(y)$, the probability of detection of the bridge defect for the considered range of resistance values is given by

$$P^R_{det} = f_X(x) = \frac{1}{b-a}\int_a^b (1 - AREA(y)dy \tag{4.10}$$

4.3.4 Statistical Fault Coverage

Statistical Fault Coverage (SFC) will be used to evaluate the circuit testability for resistive bridges of a circuit. This is evaluated for a range of resistive bridges producing small delays. The SFC is calculated as the ratio of the sum of the probabilities of detection for all the bridge locations to the total number of bridges considered. Hence, the SFC of a circuit with n bridges can be estimated by

$$Statistical \;\; Fault \;\; Coverage = \frac{\sum_n f_X(x)}{n} * 100\% \tag{4.11}$$

Let us consider that resistive bridges are the internal defects which produce small delays, hence, we can define the circuit testability as the probability that small delay defects will result in an externally visible increment in the circuit delay. Thus, SFC will be a metric to evaluate the circuit testability for small delay due to resistive bridge defects.

4.4 Example of the Methodology

Step by step, a procedure has been developed to show the proposed methodology. The ISCAS circuit C432 has been used in order to exemplify the methodology

1. The PDFs at the outputs for the defect-free circuit are obtained. The MAX function at the outputs is applied.

2. Then, a pair of internal nodes from the coupling capacitance information of the circuit are chosen, ex. node 27 and 14.

3. A resistance range for the bridge defect is defined [R_{ba} - R_{bb}]. Ex. R_b = [500Ω - 5KΩ]

4. Defective circuit delays (PDF) for two values of R_b's in the defined range, at the chosen bridge location are obtained.

5. Two defect delays each one for each affected node (line) is calculated for each value of the resistive bridge, but only that one with the greater increment delay is propagated. We assume that the correct input patterns to gets the greater increment delay is applied.

6. The constant k that define the rate of change for the mean delay of the defective circuit for any resistance bridge on the pair of chosen nodes is calculated using both defective circuit delays.

7. Using the constant k, defective circuit delay for any resistance bridge value on the pair of nodes is considered. Then, the intersection area $AREA$ can also be obtained.

8. The probability distribution function ($f_Y(y)$) of the resistance bridge values occurrence is defined. For this work a uniform distribution has been assumed.

9. For a uniform distribution of the resistance bridge values ($f_Y(y) = \frac{1}{b-a}$) , the probability of detection of a bridge for a range of resistance values is computed:

$$P_{det}^{R} = f_X(x) = \frac{1}{b-a}\int_a^b (1 - AREA(y))dy$$

   This is done using the PDFs information of Figure 4.8 which correspond at the internal nodes 27 and 14, and applying this procedure, we can compute the probability of detection for resistive bridges ranging from 500Ω to 5KΩ; resulting in $f_X(x) = 0.27$.

10. Finally, once the probability of detection of the considered range of resistive bridges for all bridge location (n) have been obtained, the statistical fault coverage can be calculated as follows.

$$SFC = \frac{\sum_n f_X(x)}{n} * 100\%$$

4.5 Simulation Results

The proposed methodology has been applied to some ISCAS-85 benchmark digital circuits implemented with TSMC 0.18μm technology. Table 4.2 shows the Statistical Fault Coverage results for the considered ISCAS benchmark circuits. Resistance bridge values considered ranges from 500Ω to 5KΩ. The data given are: the number of logic levels (LL), the mean (μ) and the standard deviation (σ) of the delay of the defect-free circuits, the total number of bridges considered, and the Statistical Fault Coverage (SFC) of the circuit. The number of logic levels means the logic depth of the circuit.

SFCs are obtained for the circuits C432, C499 and C1908. One of the reasons of these values may be because delay increases due to bridges are smaller than that delay increases due to opens. This propagation is limited by the MAX function. Circuit with SFC lowest is

Table 4.2: SFC results for some ISCAS benchmark circuits. Resistance range: 500Ω to 5KΩ.

CIRCUIT	LL	MEAN (μ)[ns]	SD (σ)[ps]	BRIDGES	SFC (%)
C432	22	2.89	27	467	29.3
C499	12	1.72	29	602	35.1
C1908	20	2.31	26	800	11.7

obtained for circuit C1908. This could be explained by the fact that there is an unbalance upper than the others. Therefore, it can be stated that the circuits C432 and C499 present better circuit testability for small delay defects due to resistive bridges, and that the circuit C1908 has a lower circuit testability. Thus, the circuit testability to the detection of small delays due to resistive bridge defects depend on its architecture.

4.6 Conclusions

In this chapter, an aware methodology to evaluate circuit testability for small delay defects due to resistive bridges in the presence of process variations has been presented. A STAF is used to propagate small delays due to resistive bridges considering process variations and some important issues in nanometer technologies. An Statistical methodology has been developed to evaluate the probability of detection of resistive bridges for a given range of values.

Using the probability of detection the statistical fault coverage (SFC) of the circuit is obtained. The SFC gives an indication of the circuit testability for small delay defects due to resistive bridges. Using the proposed methodology, the SFC of resistive bridges producing small delays is evaluated for some ISCAS benchmark circuits, which is a metric of the circuit testability.

It can be observed that the SFCs of circuits with bridge defects are lower than for circuits with open defects. This is because the delay increments due to bridges are smaller than the delay increments due to opens. And only when the resistive bridge takes values close to the critical resistance value the circuit is more significantly influenced. Also, the architectural of the circuit influences the fault coverage of a circuit. Thus, the circuit testability to the detection of small delays due to resistive bridge defects also depends on its architecture.

Chapter 5

Fault Coverage using Stratified Random Sampling

In this chapter, a methodology to reduce the number of simulated faults to estimate the fault coverage of a circuit is presented. Resistive open defects and resistive bridge defects are considered. Random sampling techniques is commonly used to reduce computation time cost in different fields. In this work, stratified random sampling is used to reduce computation time cost because their efficiency. This Chapter is organized as follows: In Section 5.1, state of the art to reduce computation time cost using random sampling techniques is intoduced. In Section 5.2, the basics of random sampling techniques are given. In Section 5.3, a methodology to reduce the number of simulated faults to estimate the fault coverage of a circuit is presented. In Section 5.4, simulation results for some ISCAS circuits are given. Finally, the conclusions of the chapter are given in Section 5.5.

5.1 Introduction

Fault simulation is commonly used in the development and evaluation of test vectors (manufacturing test) of integrated circuits. With the continuos reduction in the critical dimension on devices and interconnections, chip density and the number of possible defects in IC's increase. As a result, time computation of simulated faults to obtain the fault coverage has become an important concern in IC design. In the past, sampling techniques have been widely used to reduce computation time because their efficiency [98][99]. With sampling techniques, we can establish a sampling procedure that will significantly reduce the number of simulated faults to compute the fault coverage of the circuit while satisfying a given error and confidence level. The result is

an *estimated fault coverage*.

Stratified random sampling for power estimation has been used in [98]. The stratification is based on a low-cost predictor, such as zero delay power estimates. This significantly reduces the number of simulated vectors while a given error and confidence level are satisfied. Also, they propose a two-stage stratified sampling to handle very long initial sequences. A methodology for defect-oriented fault sampling and its implementation in an extraction tool for estimation of defect coverage was presented in [99]. A stratified sampling methodology was applied to non-equally probably faults exhibiting a wide range of probabilities of occurrence. It was concluded that stratified sampling adequately solves the problem of sampling non-equally probable faults. The defect coverage is estimated with similar confidence intervals as that obtained with fault samples of the same dimension collected from equally probable faults. Statistical technique for estimating fault coverage in combinational circuits by fault-free simulation of a random sample from the test vector set is presented in [100]. The fault coverage is computed from controllabilities and observabilities both defined as probabilities and the method is applicable to any fault model like stuck-at-faults or delay faults.

5.2 Random Sampling

One of the primary reasons that statistics has become of great importance in science and engineering is the knowledge we have concerning sampling and the conclusions that can be drawn from samples. It is perhaps a curious and counter intuitive fact that knowledge about a population or group can be found with great accuracy by examining a sample [101].

In statistics, a sample is a subset of a population or group. Typically, the population is very large, making a census or a complete enumeration of all the values in the population impractical or impossible. The sample represents a subset of manageable size. Samples are collected and statistics are calculated from the samples so that one can make inferences or extrapolations from the sample to the population. This process of collecting information from a sample is referred as sampling.

A probability sampling method is any method of sampling that utilizes some form of random selection. In order to have a random selection method, you must set up some process or

procedure that assures that the different units in your population have equal probabilities of being chosen. The best way to avoid a biased or unrepresentative sample is to select a random sample, also known as a probability sample. A random sample is defined as a sample where the probability that any individual member from the population being selected as part of the sample is exactly the same as any other individual member of the population. Several types of random samples are simple random samples, systematic samples, stratified random samples, and cluster random samples.

5.2.1 Simple Random Sampling Background

In statistics, a Simple Random Sample (SRS) [101] is a subset of individuals (a sample n) chosen from a larger set (a population N). Each individual (u_i) is chosen randomly and entirely by chance, such that each individual has the same probability of being chosen at any stage during the sampling process, and each subset of n individuals has the same probability of being chosen for the sample as any other subset of n individuals. This process and technique is known as simple random sampling, and should not be confused with Random Sampling [101].

Figure 5.1 shows a SRS schematic illustrating the fault coverage estimation. The fault coverage for defects localized in a system is estimated. First, the population of defects (N) is defined, second, applying SRS a small sample (n) is obtained from the population, third, fault simulation on the sample chosen is performed in order to get a measurement of the detectability of the defects, fourth, statistical calculations using the information of detectability are done. These statistical calculations give an estimated of the fault coverage of the system.

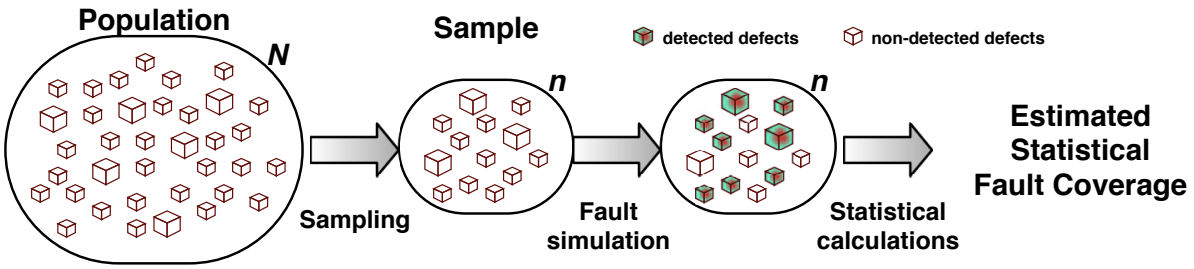


Figure 5.1: Simple random sampling illustrating the fault coverage estimation.

Using the characteristic values (x_i) obtained after the processing the units falling in the sample, statistical calculations to get the mean ($\overline{x}$) and the variance (s^2) of the sample representing

the population can be estimated by

$$\overline{x} = \frac{1}{n}\sum_{i=1}^{n} x_i \tag{5.1}$$

$$s^2 = \frac{1}{n-1}\sum_{i=1}^{n}(x_i - \overline{x})^2 \tag{5.2}$$

In small populations and often in large ones, such sampling is typically done *without replacement*, i.e., one deliberately avoids choosing any member of the population more than once. Although simple random sampling can be conducted *with replacement* instead, this is less common and would normally be described more fully as simple random sampling *with replacement*. Sampling done *without replacement* is no longer independent, but still satisfies exchangeability, hence many results still hold. Further, for a small sample from a large population, sampling *without replacement* is approximately the same as sampling *with replacement*, since the likelihoods of choosing the same sample twice is low. An unbiased random selection of individuals is important so that in the long term, the sample represents the population. However, this does not guarantee that a particular sample is a perfect representation of the population. Simple random sampling merely allows one to draw externally valid conclusions about the entire population based on the sample.

Simple random sampling is the simplest of the probability sampling techniques. It requires a complete sampling frame which may not be available or feasible to construct for large populations. Even if a complete frame is available, more efficient approaches may be possible if another useful information is available about the units in the population. Advantages are that it is free of classification error, and it requires minimum advance knowledge of the population other than the frame. Its simplicity also makes it relatively easy to interpret data collected via SRS. For these reasons, simple random sampling best suits situations where not much information is available about the population and data collection can be efficiently conducted on randomly distributed items, or where the cost of sampling is small enough to make efficiency less important than simplicity. If these conditions are not true, stratified sampling or cluster sampling may be a better choice.

5.2.2 Stratified Random Sampling Background

Stratified Random Sampling (STRS) [101], sometimes also called proportional or quota random sampling, involves dividing the population (N) into homogeneous subgroups (K), called strata, and then taking a simple random sampling for each subgroup. There are several major reasons why you might prefer stratified sampling over simple random sampling. First, it assures that you will be able to represent not only the overall population, but also key subgroups of the population, especially small minority groups.

When sub-populations vary considerably, it is advantageous to sample each subpopulation (stratum) independently. Stratification is the process of grouping members of the population into relatively homogeneous subgroups before sampling. The stratify is done based in the characteristic value (x_i) of the unit (u_i). However, as this characteristic value is unknown at this time, a predictor should be used. The strata should be mutually exclusive: each element in the population must be assigned to only one stratum. The strata should also be collectively exhaustive: no population element can be excluded. Then simple random or systematic sampling is applied within each stratum. This often improves the representativeness of the sample by reducing sampling error. It can produce a weight mean ($\overline{X}_{ST}$) that has less variability (S_{ST}) than the arithmetic mean of a simple random sample of the population.

Figure 5.2 shows a STRS scheme illustrating the fault coverage estimation for a population of defects of a circuit. The fault coverage for the defects localized in a system is estimated. First, the population of defects (N) is defined. Second, the stratification of the population is done ($K = 4$). Third, applying SRS a small sample (n_k) is obtained from each stratum. Fourth, fault simulation on the chosen stratified samples is performed in order to obtain the probability of detection of the defects. Fifth, statistical calculations related with the STRS procedure are done. These statistical calculations give an estimated of the fault coverage of the system.

The main advantages of stratified random sampling over other sampling methods can be the next: 1) focuses on important subpopulations and ignores irrelevant ones, 2) allows use of different sampling techniques for different sub-populations, 3) the results from each stratum may be of intrinsic interest and can be analyzed separately, 4) improves the accuracy/efficiency of estimation. Some disadvantages are: 1) Requires selection of relevant stratification variables

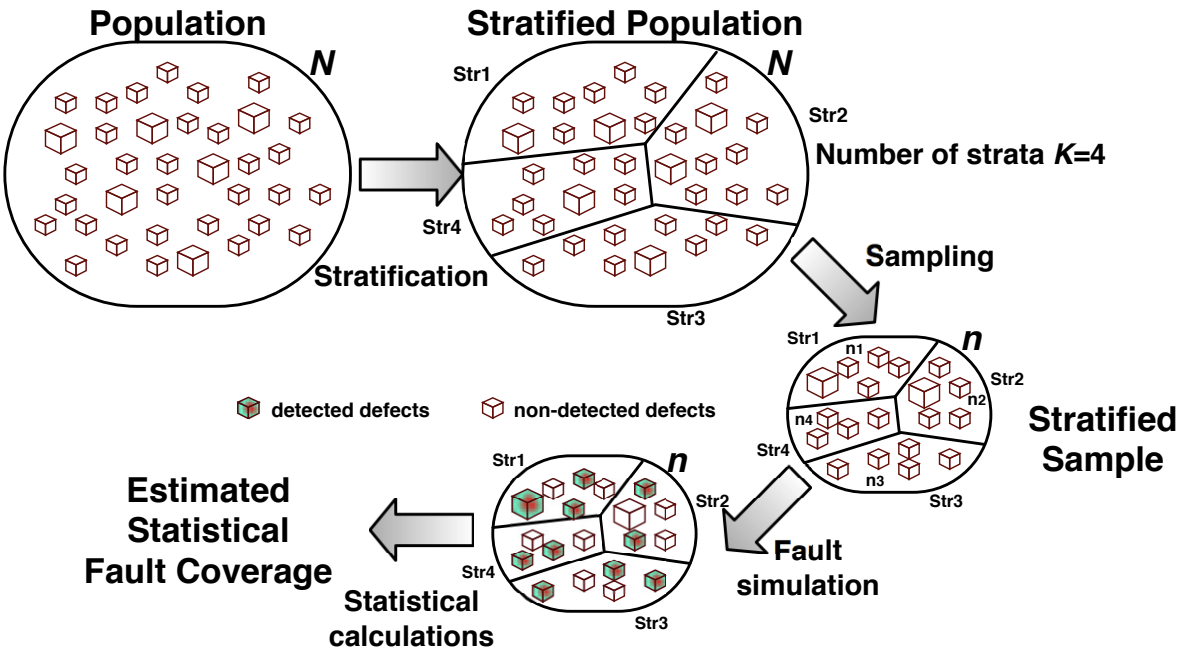


Figure 5.2: Stratified random sampling illustrating the fault coverage estimation [99]. $n = n_1 + n_2 + n_3 + n_4$

which can be difficult, 2) it is not useful when there are no homogeneous subgroups, and 3) it can be complex/expensive to implement.

5.2.3 Stratified Random Sampling Theory

First, some useful notation and its definitions used in this work are listed below [101]:

N The number of units in the population

u_i The ith unit in the population

K The number of strata in the population.

N_k The number of units in the kth stratum. Where, $k = 1, ..., K$, thus, $N_1+N_2+\cdots+N_K = N$

W_k Stratum weight or fraction of the population in the kth stratum. Where, $k = 1, ..., K$, thus, $W_1 + W_2 + \cdots + W_K = 1$

$$W_k = \frac{N_k}{N} \tag{5.3}$$

n_k The number of units in a sample falling in the kth stratum.

x_{ik} Characteristic x of the i unit in the kth stratum in a sample

Stratified random sampling is used according to the following steps [101][102]: 1) Partitioning the population, 2) Estimates of the samples and of the population, and 3) the Margin of Error given a confidence interval.

Partitioning

The partitioning or stratification is the process of dividing the population (N) into relatively homogeneous subgroups. This is done, using the characteristic value (x_i) of the unit. However, as this value is unknown at the moment of the partitioning, a predictor of this value is needed. Following, SRS is applied to get a small sample (n_k) from each stratum.

Estimates of the Samples and of the Population

Statistical calculations using the information of detectability of the sample are performed. Stratified estimate of the population mean ($\overline{X}_{ST}$) and the variance (S^2_{ST}) of the stratified sample mean are calculated. The sample variability of each stratum is used. The sample mean ($\overline{x}_k$) of each stratum and its variance (s^2_k) are calculated using the characteristic value of the units falling in the sample.

Within each stratum, a SRS of size n_k is taken. The sample mean in each stratum k should be obtained. This is obtained summing all the characteristics values x_{ik} of the sample falling in stratum k divided by the size of the sample. The sample mean using SRS for kth stratum is denoted by

$$\overline{x}_k = \frac{1}{n_k} \sum_{i=1}^{n_k} x_{ik} \tag{5.4}$$

In order to estimate the standard error of the stratified estimated $\overline{X}_{ST}$, the variances of the individual strata must be separately estimated. Thus, the variance for the kth stratum is given by

$$s^2_k = \frac{1}{n_k - 1} \sum_{i=1}^{n_k} (x_{ik} - \overline{x}_k)^2 \tag{5.5}$$

The stratified estimate of the population mean, also known as weight mean, is given by

$$\overline{X}_{ST} = \sum_{i=1}^{K} W_k \overline{x}_k \tag{5.6}$$

Assuming that the samples from different strata are independent of one another and that within each stratum a SRS is taken, the variance of the stratified sample mean $\overline{X}_{ST}$ (stratified variance of the population) can be estimated as follows

$$S^2_{ST} = \sum_{i=1}^{K} W_k^2 (\frac{1}{n_k})(1 - \frac{n_k - 1}{N_k - 1}) s_k^2 \tag{5.7}$$

The stratified standard deviation of the population is $S_{ST} = \sqrt{S^2_{ST}}$.

Margin of Error

In order to give confidence to the stratified estimated of the population mean, $\overline{X}_{ST}$, a confidence interval should be given. The range of the confidence interval is defined by the stratified estimate $\pm$ Margin of Error. That is, given a confidence level, we are confident that the true population mean is in the range defined by $\overline{X}_{ST} \pm$ Margin of Error.

Thus, when a confidence interval is required, the next procedure can be done [102]:

First, find the critical value (z). The critical value is a factor used to compute the margin of error. Based on the central limit theorem, we can assume that the sampling distribution of the mean is normally distributed. Therefore, we express the critical value as a z score (See Figure 5.3). To find the critical value for a given confidence level (CL), we take the following steps:

- Compute alpha (α):

$$\alpha = 1 - \frac{CL}{100} \tag{5.8}$$

- Find the critical probability (p^*):

$$p^* = 1 - \frac{\alpha}{2} \tag{5.9}$$

- The critical value is the z score having a cumulative probability equal to p^*. From the Normal Distribution Table [102], we find that the critical value is z.

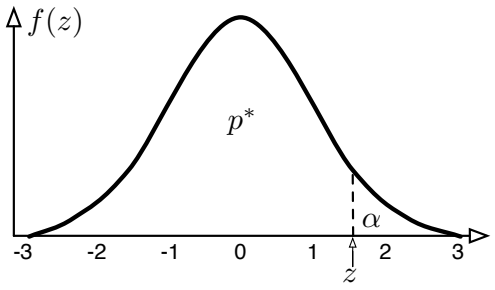


Figure 5.3: Cumulative normal distribution. Values of p^* corresponding to z.

Second, compute margin of error (ME), which is the product of the critical value with the stratified standard deviation also knows as standard error.

$$ME = z * S_{ST} \tag{5.10}$$

The range of the confidence interval is defined by the stratified estimate $\pm$ margin of error ($\overline{X}_{ST} \pm ME$), and the uncertainty is denoted by the confidence level. That is, we are $CL\%$ confident that the true population mean is in the range defined by $\overline{X}_{ST} \pm ME$.

5.3 Fault Coverage Estimate using Stratified Sampling

In this section, random sampling techniques have been used to compute statistical fault coverage of circuits with defects. Resistive open and resistive bridge defects are considered. Stratified random sampling is used to get a representative sample of the population in order to reduce computation time cost.

5.3.1 Methodology to Stratify the Population of Defects Locations

In this work, we address the fault coverage problem from a survey sampling perspective. A number of resistive defects is assumed to estimate the fault coverage of a given combinational circuit with certain statistical constrains, such as error and confidence level. We transform the fault coverage problem in a survey sampling problem by dividing the defects into small units to constitute the population for the survey.

As the probability of detection of the defects determines the fault coverage of the circuit, the probability of detection is the characteristic under study. The average probability of detection (fault coverage) is estimated by simulating the circuit for a number of samples drawn from the population. The objective is to establish a sampling procedure that will significantly reduce the number of simulated faults while satisfying a given error and confidence level.

Stratified sampling is used in this work. The purpose of stratification is to partition the population into disjoint sub-populations so that the characteristic within each sub-population is more homogeneous than the original population. The probability of detection of the defect is the characteristic value x_i of the defect, however, as this is unknown, a predictor to make the allocation of the units in each stratum is required. In this work, we use the delay increment of the defect as a predictor of the probability of detection of the defect. The model to estimate the delay increment is different for the two type of defects considered in this work. However, both type of defects have in common that the delay increment is related to its fanout loading capacitance (C). Therefore, our used predictor will be the fanout loading capacitance (C) of the affected node by the defect. This partitioning is based in a low-cost predictor that is easily obtained for each member of the population. This information is available on-line in our data-base in the framework used.

Next, more detailed information about the predictor assumption for each kind of defect are given:

For resistive opens

As described in Chapter 3, the delay increment due to resistive open defects is modeled with a simple expression given by $t_{R_o} = R_o * C$. The R_o is the resistive open and C is the load capacitance. Figure 5.4 illustrates a resistive open defect with the parameters used in the model.

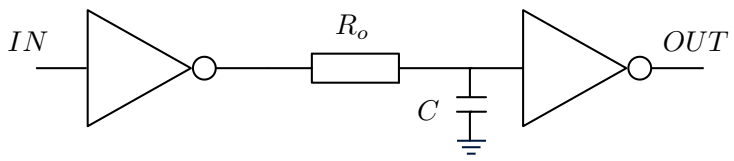


Figure 5.4: Circuit illustrating the resistive open fault model

Since the value of R_o is the same for all open locations, the fanout loading capacitance C which is directly proportional to the delay increment can be used as the predictor. That is, for higher (lower) capacitance values the resulting delay increment is higher (lower). This gives a relative measurement of the probability of detection of the defect. Using this information, the open locations are stratified according to their capacitance value.

Figure 5.5 shows the stratification of the open locations according to their capacitance values for the circuit C432. A population of 162 open defects is divided in six strata (A, B, C, D, E and F). Let stratum A consists of the 27 open defects with lowest capacitance values, stratum B of the 27 next opens with higher capacitance values, and so forth until stratum F with the 27 opens with the highest capacitance values. The capacitance values ranges from $C \approx [3fF - 58.1fF]$.

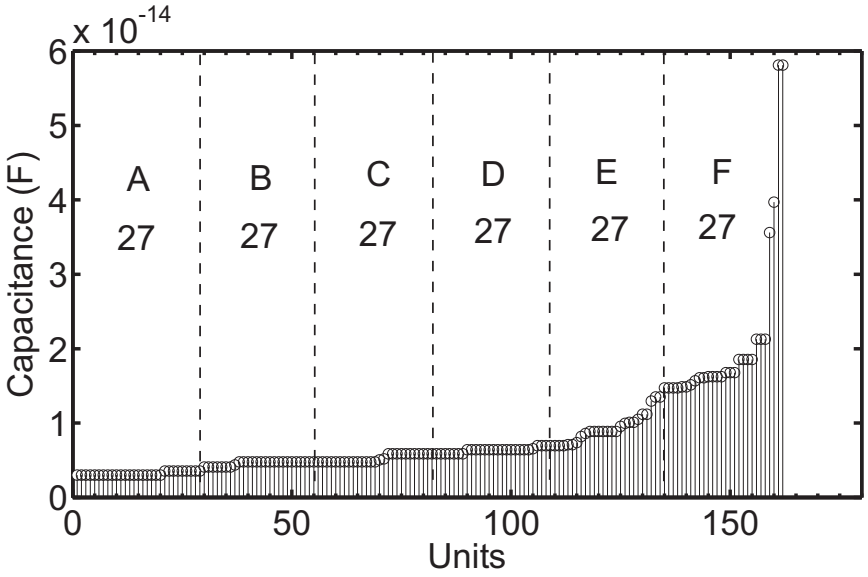


Figure 5.5: Stratification of the open defects according to its loading capacitance value used as the predictor of the probability of detection. For the ISCAS circuit C432. Opens=162.

Figure 5.6 shows a histogram plot of the open defects according to its loading capacitance value used as the predictor of the probability of detection. The histogram shows the distribution of the capacitance values, observing that the majority of open defects presents small capacitance values. This gives an indication of the sample mean ($\overline{x}_k$) expected for each stratum. Also shown that the failure distribution due to delay defects is skewed towards smaller delays [43][44], and may indicates that the majority of circuits that fail due to delay-related defects fail due to delay defects smaller than the typical clock cycle times for the respective technology node.

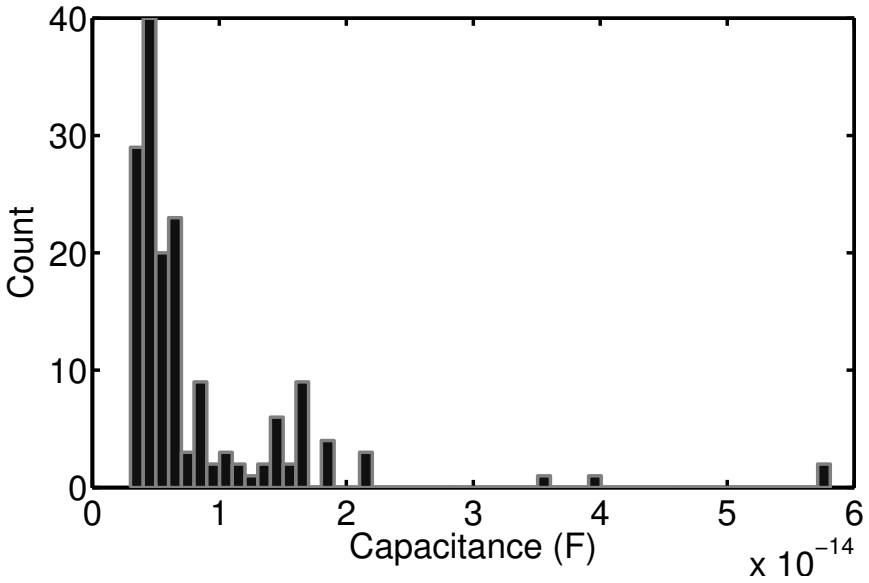


Figure 5.6: Distribution histogram of the open defects according to its loading capacitance value. For the ISCAS circuit C432.

For resistive bridges

For resistive bridge defects, the procedure is similar to that used for open defects with a slight difference. Resistive bridge defects involve two interconnect lines, i.e., involves two loading capacitances in two different nodes. Figure 5.7 illustrates a resistive bridge fault. R_b is the resistance of the bridge and C_1 and C_2 are the load capacitances.

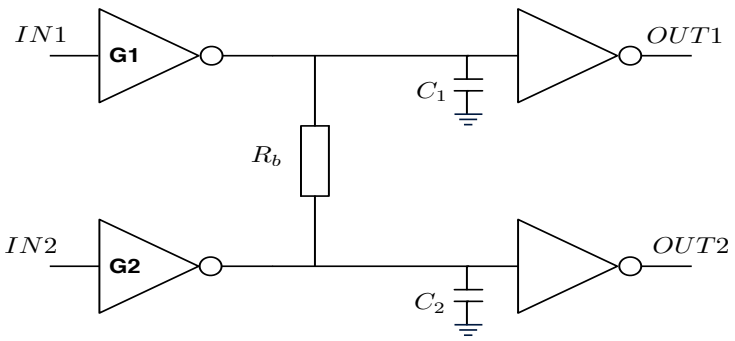


Figure 5.7: Circuit illustrating the resistive bridge fault model

As described in Chapter 4, for the bridge case, two defective delays each one for each affected node (line) is calculated, but only that one with the greater delay increment is propagated.

We assume that the input patterns to get the greater delay increment in the bridge location is applied. According to the model used to calculate the delay increment, the greater delay increment is obtained for the node with lower load capacitance [97]. The delay increment due to the resistive bridge $d_{b,i}$ defect is modeled by

$$d_{b,i} = (-c * log_2\left(\frac{0.5 - h}{g - h}\right) - 1) * d_{o,i} \tag{5.11}$$

The parameters c, h and g are calculated according to the input pattern $(IN1, IN2)$, and the way to calculate them are given in Table 4.1. The parameter c is function of the loading capacitances (C_1 and C_2). When the delay increment in the upper line is analyzed (See Figure 5.7), the next is true

$$d_{b,1} = f(\frac{C_2}{C_1}) \tag{5.12}$$

Taking into account the previous expression, the delay increment in a line is inversely proportional to its fanout loading capacitance. Higher capacitance values give lower delay increment and lower capacitance values give higher delay increment. Hence, lower capacitance values for each defect are used as the predictor, which indicates a relative measurement of the probability of detection. For each bridge location, we have to evaluate which one is smaller than the other, for example, if $C_1 < C_2$, then we choose C_1 as the predictor, in the same way for all the defects. Using this information, we will stratify the bridge defects according to the chosen capacitance values.

Figure 5.8 shows the stratification of the bridge locations according to their capacitance values for circuit C432. A population of 467 bridge defects is divided in six strata (A, B, C, D, E and F). Let stratum A consist of the 78 bridge defects with lowest capacitance values, stratum B of the 78 bridges with the next higher capacitance values, stratum C of the 78 next, stratum D of the 78 next, stratum E of the 77 next, and the last stratum F with the 78 highest capacitance values. It can be observed that the capacitance values ranges from $C \approx [3fF - 58.1fF]$.

Figure 5.9 shows a histogram plot of the bridge defects according to its loading capacitance value used as the predictor of the probability of detection. The histogram shows the distribution of the capacitance values, observing that the majority of bridge defects present small capacitance

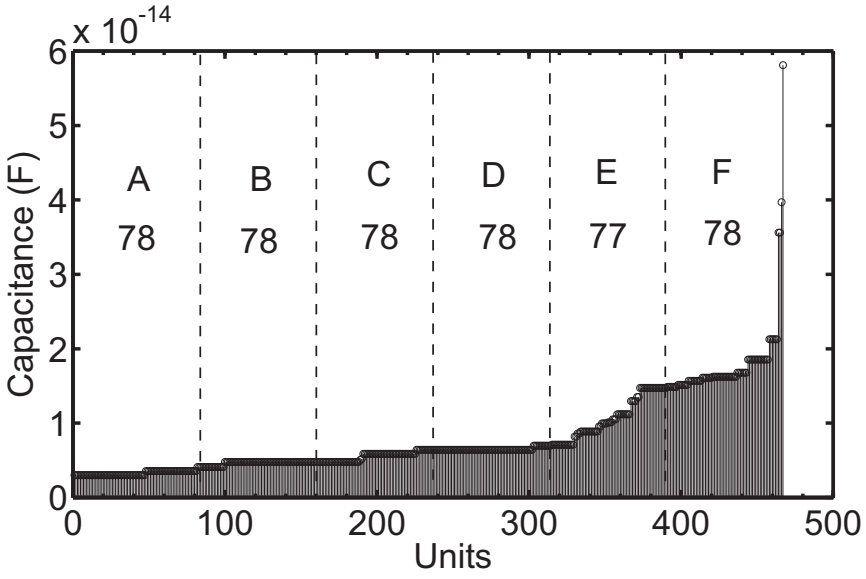


Figure 5.8: Stratification of the bridge defects according to its loading capacitance value used as the predictor of the probability of detection. For the ISCAS circuit C432. Bridges=467.

values. This gives an indication of the sample mean ($\overline{x}_k$) expected for each stratum.

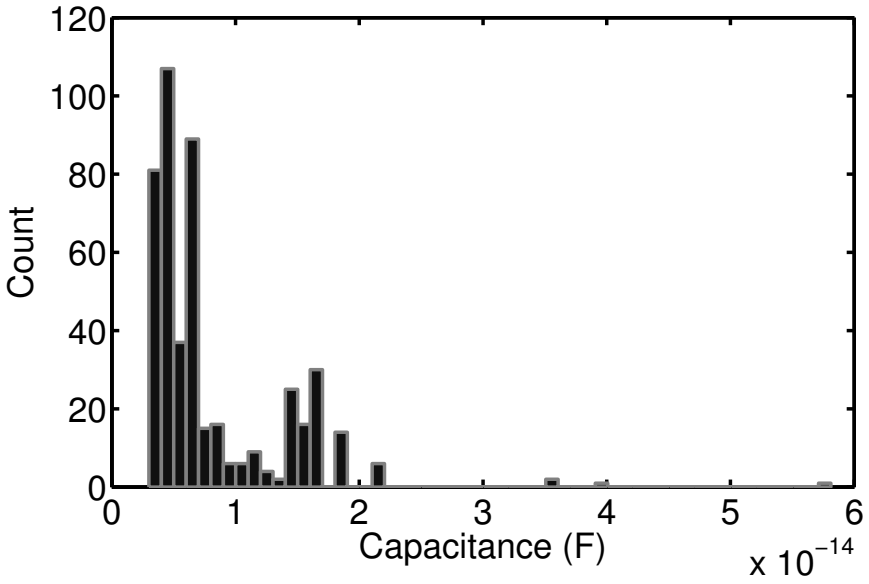


Figure 5.9: Distribution histogram of the bridge defects according to its loading capacitance value. For the ISCAS circuit C432.

5.3.2 Examples of Application to ISCAS Benchmark Circuit C432

To illustrate the sampling methodology, a population of resistive defects in the ISCAS Circuit C432 is considered. First, a population of resistive open defects is studied, and second, a population of resistive bridge defects is studied. The stratification process is based in the previously defined predictors.

Example A: Resistive Open Defects

A population of 162 resistive open defects in the circuit C432 is assumed. Using the predictor to stratify the open defects, the population is divided in six subgroups called strata. Let stratum A consist of the 27 open defects with lowest probability of detection, stratum B of the 27 next upper, and so forth until stratum F with the 27 highest. Within each stratum, a simple random sample of size n_k is taken. A sample of size 3 (10% of each stratum) was drawn from each of the six strata of defects. Table 5.1 shows the results of the stratification of open defects ordered by its delay increment:

Table 5.1: Stratified Random Sampling for the ISCAS Circuit C432. The units in the Population are Resistive Open defects.

Stratum	N_k	W_k	n_k (10%)	$\overline{x}_k$	s_k^2
A	27	0.166	3	0.2779	148.81e-3
B	27	0.166	3	0.9075	1.13e-3
C	27	0.166	3	0.5260	143.76e-3
D	27	0.166	3	0.9636	8.65e-6
E	27	0.166	3	0.9815	12.01e-6
F	27	0.166	3	0.9892	26.86e-6
$K = 6$	$N = 162$	$\sum W_k = 1$	$\sum n_k = 18$		

The sample mean $\overline{x}_k$ and variance s_k^2 in stratum k are shown in the Table 5.1. The sample mean $\overline{x}_k$ is obtained summing all the characteristics values x_{ik} of the sample falling in stratum k divided by the size of the sample (See equation 5.4) and the variance s_k^2 for the kth stratum can be calculated with equation (5.5). The characteristic values x_{ik} are the probability of detection of the open defects for the stratified sample, obtained after propagates the chosen delay defects with STAF and apply the statistical methodology proposed in Chapter 3. With this information, stratified mean $\overline{X}_{ST}$ and variance S_{ST}^2 of the sample which represent the fault coverage of the

circuit can be estimated using (5.6) and (5.7). These and the stratified standard deviation S_{ST} are given next:

Stratified Mean and Variance		
$\overline{X}_{ST} = 0.7743$	$S^2_{ST} = 0.0025$	$S_{ST} = 0.0501$

Whether a confidence interval is specified, the confidence interval procedure given above in a previous section should be done. Thus, the margin of error ME is required, which denoted the uncertainty. Assuming a 95% of confidence level, we have $ME = 1.96 * 0.0501 = 0.0982$. Therefore, the 95% confidence interval is $0.67611 \leqslant \overline{X}_{ST} \leqslant 0.87253$, and the margin of error is equal to 0.0982. That is, we are 95% confident that the true population mean is in the range defined by 0.7743 ± 0.0982.

Example B: Resistive Bridge Defects

A population of 467 resistive bridge defects in the circuit C432 is assumed. Using the predictor to stratify the bridge defects, the population is divided in six subgroups called strata. Let stratum A consist of the 78 bridge defects with highest probability of detection, stratum B of the 78 next lower, stratum C of the 78 next lower, stratum D of the 78 next lower, stratum E of the 77 next lower, and the last stratum F with the 78 lowest. Within each stratum, a simple random sample of size n_k is taken. A sample of size 8 (10% of each stratum) was drawn from each of the six strata of defects. Table 5.2 shows the results of the stratification of bridge defects ordered by its loading capacitance:

The sample mean $\overline{x}_k$ and variance s^2_k in stratum k are shown in the Table 5.2. The sample mean $\overline{x}_k$ is obtained summing all the characteristic values x_{ik} of the sample falling in stratum k divided by the size of the sample (See equation 5.4) and the variance s^2_k for the kth stratum can be calculated with equation (5.5). The characteristic values x_{ik} are the probability of detection of the bridge defects for the stratified sample, obtained after propagates the chosen delay defects with STAF and apply the statistical methodology proposed in Chapter 4. With this information, stratified mean $\overline{X}_{ST}$ and variance S^2_{ST} of the sample which represent the fault coverage of the circuit can be estimated using (5.6) and (5.7). These and the stratified standard deviation S_{ST} are given next:

Table 5.2: Stratified Random Sampling for the ISCAS Circuit C432. The units in the Population are Resistive Bridge defects.

Stratum	N_k	W_k	n_k (10%)	$\overline{x}_k$	s_k^2
A	78	0.167	8	0.183	56.81e-3
B	78	0.167	8	0.236	123.57e-3
C	78	0.167	8	0.215	105.61e-3
D	78	0.167	8	0.401	89.23e-3
E	77	0.164	8	0.276	45.29e-3
F	78	0.167	8	0.388	105.12e-3
$K = 6$	$N = 467$	$\sum W_k = 1$	$\sum n_k = 48$		

Stratified Mean and Variance		
$\overline{X}_{ST} = 0.2836$	$S_{ST}^2 = 1.66e-3$	$S_{ST} = 0.0407$

Whether a confidence interval is specified, the confidence interval procedure given above in a previous section should be done. Thus, the margin of error ME is required, which denoted the uncertainty. Assuming a 95% of confidence level, we have $ME = 1.96 * 0.0407 = 0.0799$. Therefore, the 95% confidence interval is $0.20369 \leqslant \overline{X}_{ST} \leqslant 0.36353$, and the margin of error is equal to 0.0799. That is, we are 95% confident that the true population mean is in the range defined by 0.2836 ± 0.0799.

5.4 Simulation Results for some ISCAS Benchmark Circuits

The proposed methodology has been applied to some ISCAS-85 benchmark digital circuits implemented with TSMC $0.18\mu m$ technology. Mentor Graphics Tools were used to implement the benchmark circuits. The ASIC Design Kit (ADK v3.1) was utilized to create each circuit. From these, netlist at different hierarchy levels are extracted. These are feed into the STAF to be processed. More information can be found on Appendixes A and B.

Table 5.3 and 5.4 show the Stratified Statistical Fault Coverage for the considered ISCAS benchmark circuits. The resistance open values considered ranges from 10Ω to 200KΩ and the resistance bridge value considered ranges from 500Ω to 5KΩ. For both, a uniform distribution has been assumed. The data given are: total number of defects in the population N (OPENS,

BRIDGES), conventional SFC of the circuit, defects sampling (OPENS, BRIDGES), stratified estimate of the population (Stratified SFC $\overline{X}_{ST}$), stratified standard deviation of the population (S_{ST}) and the margin of error (ME).

Table 5.3: Stratified SFC results for some ISCAS benchmark circuits for open defects with a confidence level CL=95%. Resistance range: [10Ω - 200KΩ]

CIRCUIT	OPENS (N)	SFC (%)	OPENS (≈10%)	$\overline{X}_{ST}$(%)	S_{ST}(%)	ME(%)
C432	162	76.5	18	77.4	5.0	9.8
C499	158	96.7	18	96.7	0.47	0.92
C1908	200	85.2	18	88.3	3.3	6.4
C2670	356	49.0	36	43.4	4.0	7.8
C3540	898	46.7	90	42.3	3.1	6.1
C6288	1618	61.5	162	55.3	2.6	5.1

Table 5.4: Stratified SFC results for some ISCAS benchmark circuits for bridge defects with a confidence level CL=95%. Resistance range: 500Ω to 5KΩ.

CIRCUIT	BRIDGES (N)	SFC (%)	BRIDGES (≈10%)	$\overline{X}_{ST}$(%)	S_{ST}(%)	ME(%)
C432	467	29.3	48	28.3	4.1	8.0
C499	602	35.1	60	29.9	3.8	7.4
C1908	800	11.7	78	10.9	2.0	3.9

Fault coverages of the circuits using the proposed methodology, based on STRS, agree with the obtained using the conventional methodology. The interval confidence given, lets confident in the results. The sampling methodology proposed, produce good results in estimate the fault coverage faster than the conventional methodology. As the stratified sample representing the population is approximately 10% of the population, approximately 90% of the computation time is saved with respect to simulate the total population. Fault coverage estimated comes with an estimated standard deviation, and whether a confidence level is given the fault coverage estimated has a margin of error. 95% of confidence level is used in this work. Based on the central limit theorem, sampling distribution of the mean has assumed to be normally distributed, that's when a confidence interval is required.

Measures may be taken for those circuits presenting poor fault coverage in order to improve their test quality. Among them to use multiple clock frequencies [103], and to use techniques to

improve the process tolerance of the circuits [104][105]. Circuit timing optimization may also affect the detection of SDDs [103]. Using special test conditions (e.g. speed, supply voltage and temperature) [27][39] may be explored.

5.5 Conclusions

In this chapter, a sampling methodology to estimate the fault coverage of small delay defects, in order to reduce computation time cost, is proposed. Stratified random sampling is used in order to get the sample that represents the population, because its efficiency for surveys. Probability of detection of the defect is its characteristic value x_i , however, as this is unknown, a predictor to make the allocation of the units in each strata is used. Fanout loading capacitance of the affected node by the defect is used as the predictor since the direct relation with the delay increment of the defect and this with the probability of detection. Also, a confidence interval is used to give confidence to the obtained results.

With this sampling procedure the number of simulated faults to compute the fault coverage of the circuit is significantly reduced while satisfying a given error and confidence level. The result is an estimated fault coverage.

In the stratified, the partitioning is based on a low-cost predictor that is easily obtained for each member of the population. This information is available on-line in our data-base in the framework used. The capacitance parameter has been used as the predictor of the probability of detection of the defects giving good results for both kind of defects.

The STAF is used to analyze the detectability of resistive open and bridge defects, considering process variations and the most important issues in nanometer technologies. Using the proposed methodology, the stratified SFC of resistive open and bridge defects producing small delays is evaluated for some ISCAS benchmark circuits. The SFC gives a metric of the circuit testability. The results presented in this work show the feasibility of the proposed methodology.

Chapter 6

Conclusions

In this thesis, an aware methodology to evaluate circuit testability for small delay defects due to resistive open and bridge defects in the presence of process variations has been proposed. The circuit testability has been evaluated analyzing the timing information of the circuit. Statistical timing analysis is used to propagate the signal delay through the logic levels until the primary outputs are reached. Then, the outputs of the defect-free circuit and those of the defective one are compared to determine the fault coverage of the circuit. This is used as the circuit testability metric. The methodology is applied to some ISCAS benchmark circuits.

A background on state of the art of the major challenges in circuit design and testability of modern integrated circuits were collected and analyzed to give support at the present work. Small delay defects (SDDs) modeling, delay testing, timing analysis, process parameter variations and statistics are some of these topics.

An Statistical Timing Analysis Framework (STAF) was developed and implemented based on the technique called Statistical Timing Analysis using Levelized Covariance Propagation. In this framework, the main issues in nanometer technologies were considered, such as: 1) spatial correlation of the process parameters, 2) random placement of dopants, and 3) the signal correlation due to reconvergent paths. One objective of this framework is to propagate SDDs in order to get the circuit fault coverage. Process parameter variations on devices are included in the framework. Most important parameters affected by the variability in the manufacturing process, and which are considered in this work are: channel length (L), transistor width (W), oxide thickness (Tox) and threshold voltage (Vth). A rectangular grid model is used to evaluate the spatial correlation of the process parameters between devices allocated in different spatial

positions within die and inter-die.

A methodology to estimate the Statistical Fault Coverage (SFC) of resistive open and resistive bridge defects has been proposed. This is used as a metric of the circuit testability for small delay defects due to open and bridge defects. The methodology is applied to some ISCAS-85 benchmark circuits. The effect of the delay defect is included by adding the delay increment due to the defect to the precedent gate delay, afterwards, the MAX function is applied to obtain the timing information at the output gate. Then it is propagated to the next logic level until the primary outputs are reached. Statistical methodology to evaluate the probability of detection of open defects for a single resistance value has been obtained. This has been extended to evaluate the probability of detection of an open for a range of resistances values. To accomplish this the following aspects were considered: 1) the probability of detection for a single value represents a conditional probability, 2) the delay increment has a direct dependence on the value of the resistive defect, and 3) the standard deviation for the new distribution of the defective circuit is the same as the defect-free circuit. The difference between the open and the bridge evaluations resides in the dependence of the resistive value on the delay increment. A linear dependence for the opens and a negative exponential dependence for the bridges have been assumed.

Simulation results show a diverse SFC for the circuits. Some circuits have higher SFC than others. It can be observed that the number of logic levels affects the probability of detection of SDDs. Circuits with fewer logic levels have higher probability of detection than circuits with many logic levels. Hence, the circuit testability for the detection of small delays due to resistive defects also depends of the circuit architecture. In this methodology, the statistical fault coverage is obtained for all the possible defects locations including also those defects locations located in non-critical paths. This is because these defects could be a reliability concern.

In order to reduce computation time to estimate the fault coverage, a sampling methodology to estimate the fault coverage of SDDs has been proposed. The objective is to reduce the number of simulated faults to compute the fault coverage of the circuit while satisfying a given error and confidence level. The result is an estimated fault coverage. Stratified random sampling is used in order to get the samples that represent the population. Probability of detection of the fault is the characteristic value of the unit. However, as this characteristic value is unknown at the moment the strata is formed, a predictor to make the allocation of the units in each strata is used.

The fanout loading capacitance of the affected node by the defect has been used as low-cost predictor due to its direct relation with the delay increment of the defect, and hence, with the probability of detection. Our partitioning is based on a low-cost predictor that is easily obtained for each member of the population. This information is available on-line in our data-base in the framework used.

The used sampling methodology estimates the fault coverage faster than the conventional methodology. When the stratified sample represents 10% of the population, 90% of the computation time is saved approximately. With this sampling procedure, the number of simulated faults to compute the fault coverage of the circuit is significantly reduced while satisfying a given error and confidence level. The result is an estimated fault coverage.

The results obtained in each circuit after simulations show the feasibility of the proposed methodologies.

Measures may be taken for those circuits presenting poor fault coverage in order to improve their test quality. Among them to use multiple clock frequencies, and to use techniques to improve the process tolerance of the circuits. Circuit timing optimization may also affect the detection of SDDs. Using special test conditions (e.g. speed, supply voltage and temperature) may be explored. Measures to improve test quality will be analyzed in a future work.

This framework along with the toolboxes were implemented using the programming language C/C++. The Xcode compiler for Macintosh machines was used. This project was built using the standard libraries.

Appendix A

ISCAS Benchmark Circuits Implemented

The widely accepted ISCAS-85 [106][107][96] benchmark suite has been in use ever since being introduced in netlist form at the International Symposium on Circuits and Systems in 1985. The circuits are industrial designs whose functions and high-level designs have not been published, both for confidentiality reasons and to allow them to be viewed as random logic circuits with no significant high-level structure.

ISCAS 85 benchmark circuits are a group of well-defined, gate level netlist and functions based on common building blocks (such as multiplexers, ALUs, and decoders). They are widely used in Digital Integrated Circuit research works in the area of design verification, test generation, clock distribution, power consumption and timing analysis [108].

The ISCAS circuits are combinational networks provided to authors at the International Symposium on Circuits and Systems in 1985. They subsequently have been used by many researchers as a basis for comparing results with others works.

Each circuit implemented in this work is characterized in the table below:

Circuit Name	Circuit Function	Gates	Transistors	Inputs	Outputs
C432	Priority Decoder	166	886	36	7
C499	32 Bit SEC circuit	190	1424	41	32
C1908	Error Detector/Corrector	225	1460	33	25
C2670	ALU and Control	393	2146	155	50
C3540	ALU and Control	909	4276	50	22
C6288	16 Bit Multiplier	1649	8942	32	32

Table A.1: ISCAS 85 Benchmark circuits characteristics: Combinational circuits.

A.1 Layout of the Circuits

Mentor Graphics Tools was used to implement the benchmark circuits. The ASIC Design Kit (ADK v3.1) was utilized to create each circuit.

The ASIC Design Kit (ADK) is a generic design kit providing all the requisite data, libraries, and documentation to create ASIC designs using the Mentor Graphics suite of layout, synthesis, simulation, and DFT tools. The target technologies are AMI 0.5μm and 1.2μm and **TSMC** 0.35μm, 0.25μm and **0.18μm** [109].

The kit provides:

- Support for schematic, HDL or mixed schematic/HDL based designs
- Synthesis support for Leonardo Spectrum
- Pre-layout timing simulations with ModelSim (VHDL or Verilog)
- Scan insertion support for DFTAdvisor
- Automatic test pattern generation support for FastScan or FlexTest
- Static timing analysis models for SST Velocity
- Automatic place and route of designs using IC Station
- Post-layout timing simulations with ModelSim (VHDL/Verilog), MachTA, or Eldo
- Support for DA-IC

The ISCAS benchmark circuits used in this work were implemented using the technology TSMC 0.18μm. The layouts portrait are shown below:

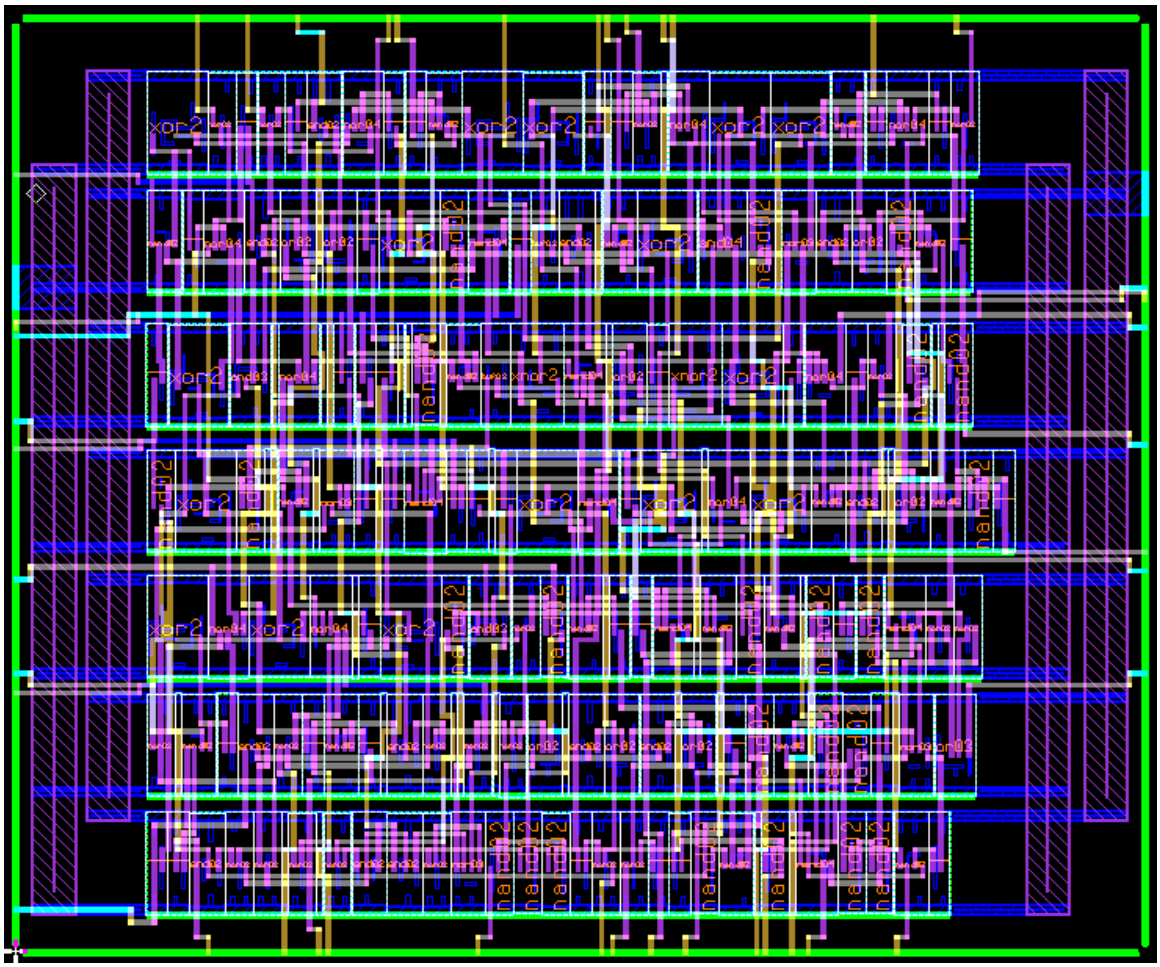


Figure A.1: C432 – 27-channel interrupt controller

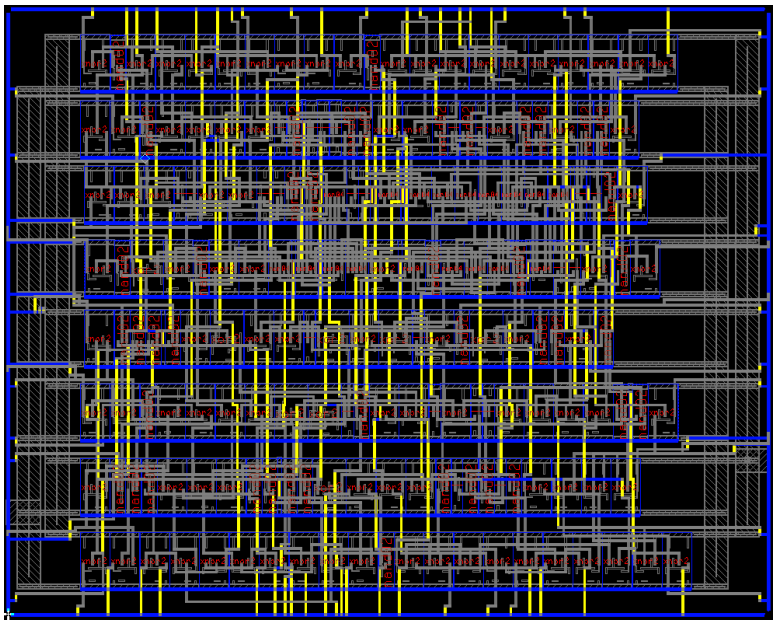


Figure A.2: C499 – 32-bit SEC circuit

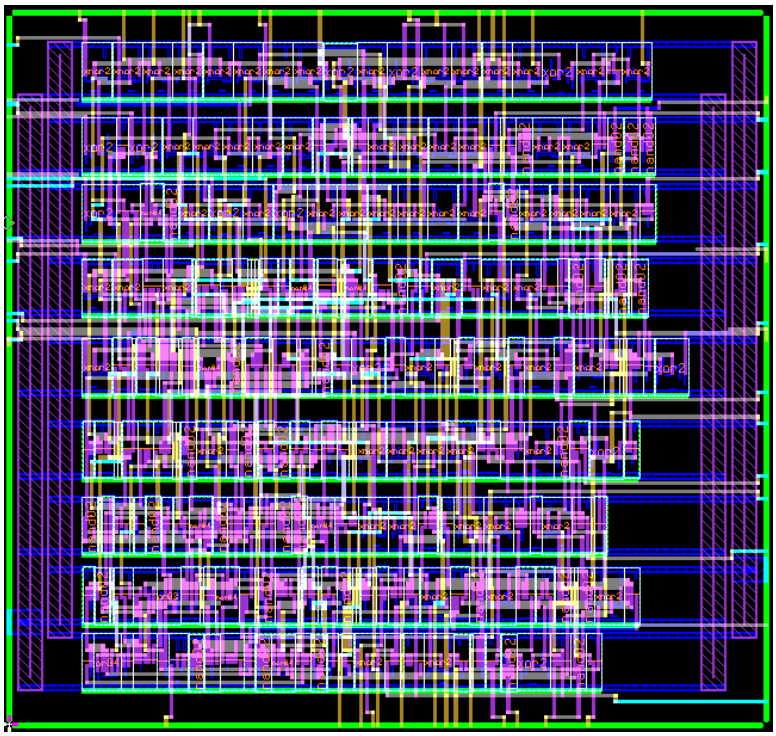


Figure A.3: C1908 – 16-bit SEC/DED circuit

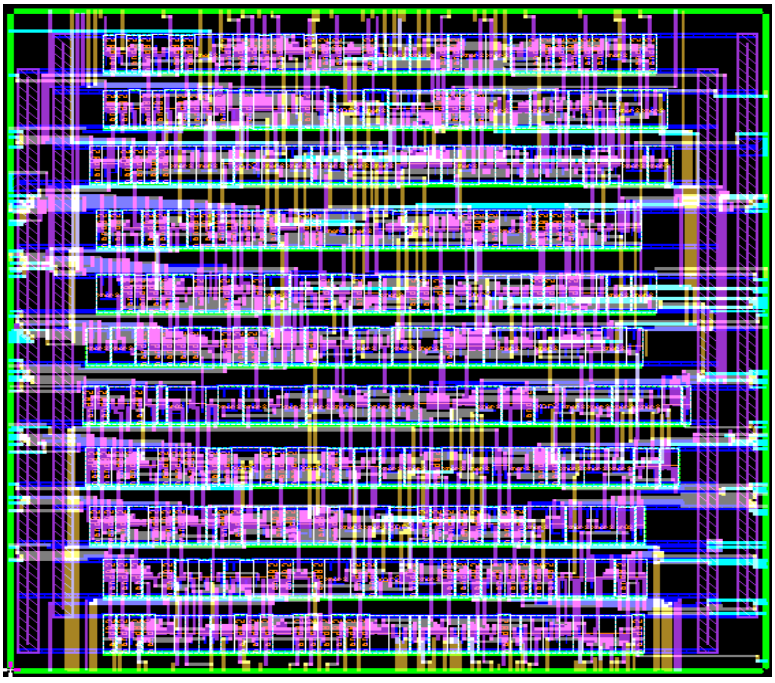


Figure A.4: C2670 – 12-bit ALU and controller

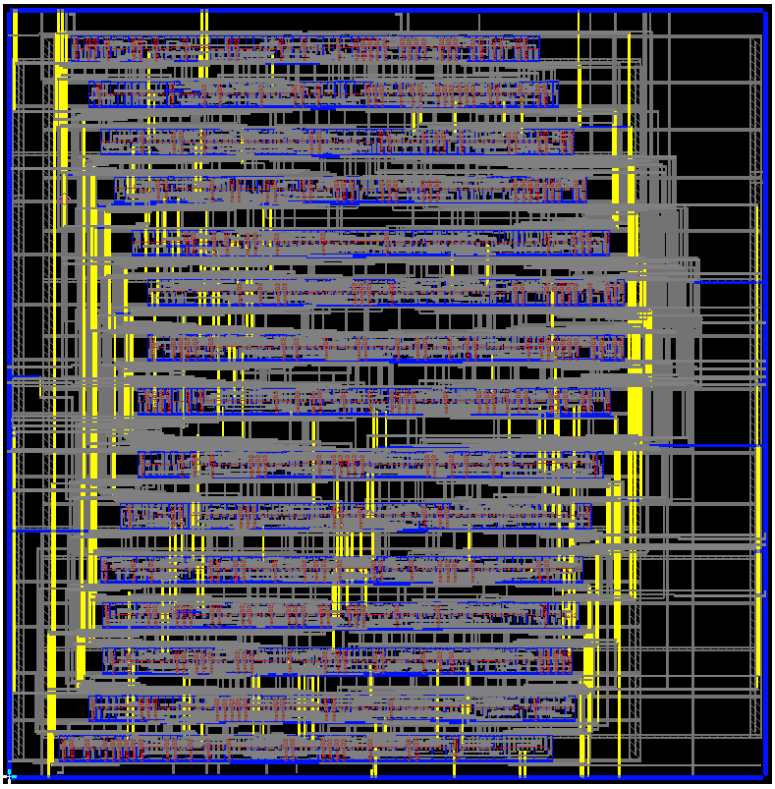


Figure A.5: C3540 – 8-bit ALU and controller

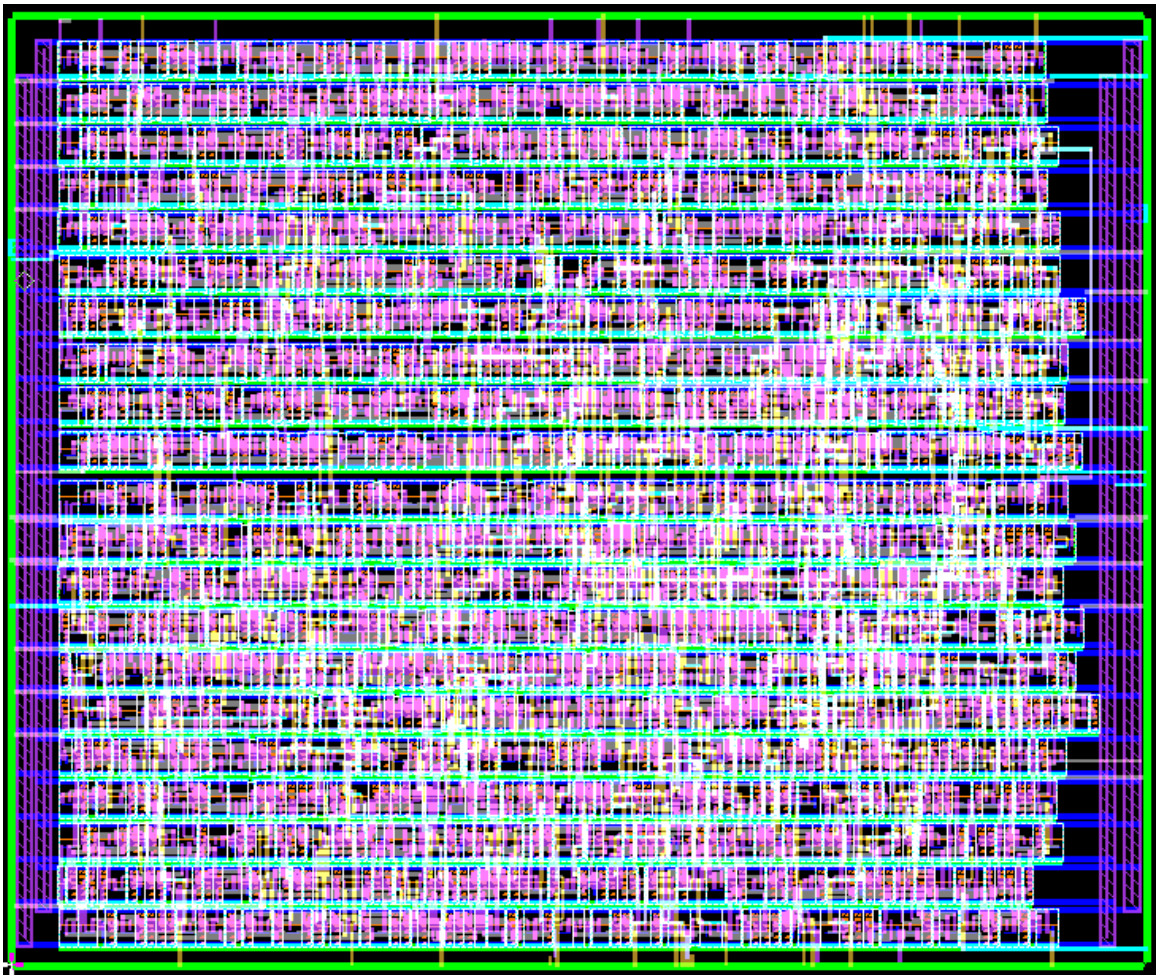


Figure A.6: C6288 – 16 * 16 multiplier

Appendix B

Description of the Small Delay Defects Detection Framework

The Small Delay Defects (SDDs) Detection Framework is a implemented tool with the goal to perform a statistical timing analysis to designed circuits with static logic. The timing analysis is directed to analyze the detectability of small-delays produced by resistive defects that will escape the test. Process parameter variations on devices are considered in the framework. At the end of the framework, the fault coverage is computed and given for each circuit. Finally, the circuit testability to the detection of small delays defects can be evaluated.

This tool was developed using the programming language C/C++. The Xcode compiler for Macintosh machines was used. This project was builded using the standard libraries.

Figure B.1 shows a summarized schematic flow of the framework, emphasizing the most important stages of the algorithm. Starting with the circuit information – netlist, passing by the STAF and the defect fault modeling until the SFC estimation. Concluding with the final fault coverage. Each one, described in the following lines:

NETLIST – The netlist information required in the framework are extracted from the layout circuit using the software design tool Calibre-MentorGraphics. All the netlist information can be obtained in the LVS and PEX steps. The obligatory netlist are listed below, and each one must be in the given form next.

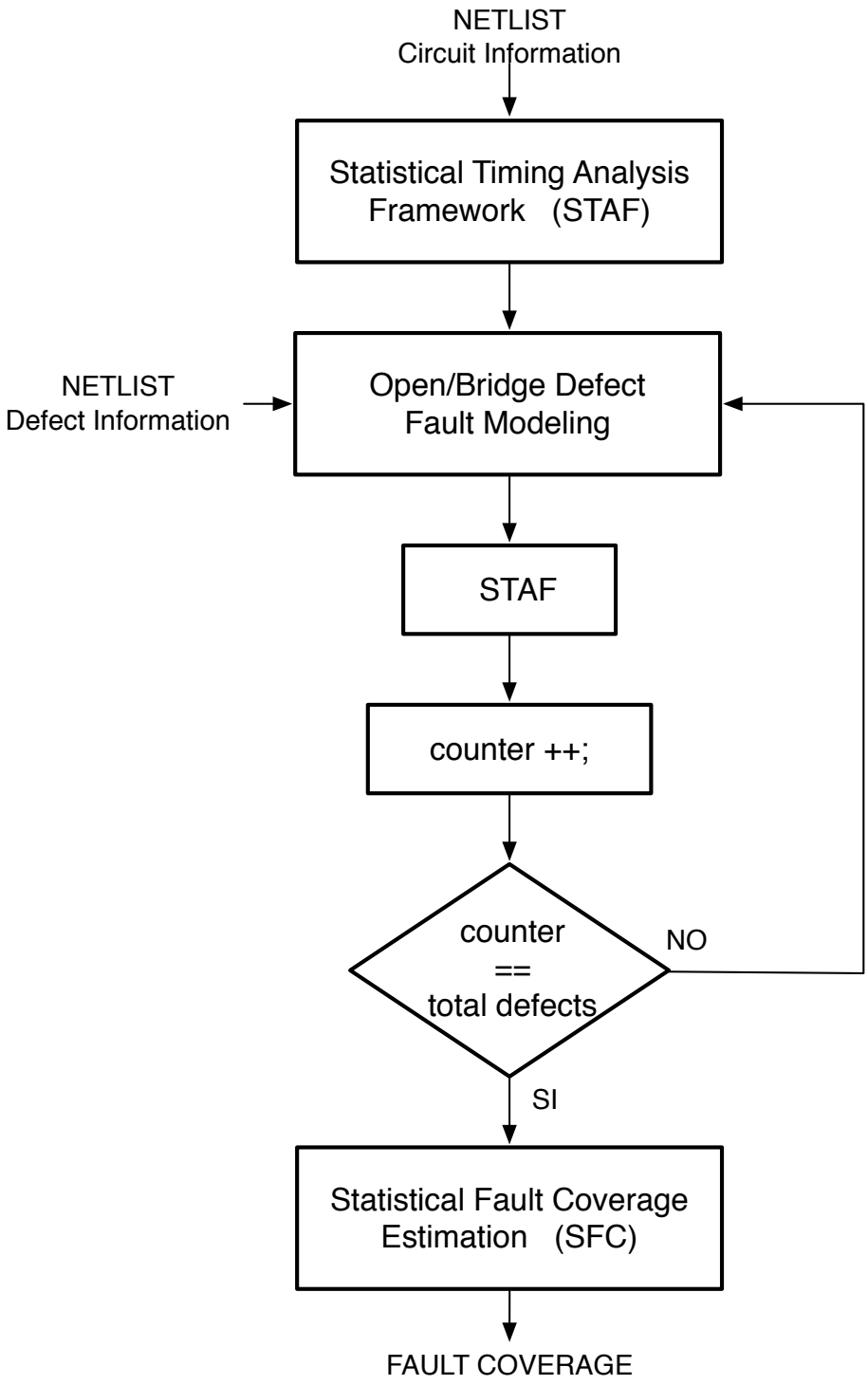


Figure B.1: Schematic illustrating the flow of the SDD detection framework

- gate level netlist

```
x965 N8 84 GND VDD INV01 $X=178 $Y=45
x1035 153 50 159 VDD GND XOR2 $X=859 $Y=469.5
x1037 N21 38 83 GND VDD NAND02 $X=153 $Y=469.5
x1136 146 197 136 140 N79 GND VDD NOR04 $X=762.5 $Y=912
x1167 62 71 21 GND VDD XNOR2 $X=764 $Y=617
x1168 138 124 151 149 62 GND VDD AND04 $X=797.5 $Y=773.5
x1169 182 N431 204 164 VDD GND OR03 $X=1075 $Y=183.5
....
```

- transistor level netlist

```
mX963/M0 82 N4 GND GND n L=1.8e-07 W=4.5e-07 AD=2.2275e-13 AS=2.9565e-13
mX963/M1 82 N4 VDD VDD p L=1.8e-07 W=9.9e-07 AD=4.9005e-13 AS=5.6295e-13
mX1037/M0 X1037/6 N21 GND GND n L=1.8e-07 W=9.9e-07 AD=3.564e-13 AS=5.6295e-13
mX1037/M1 83 38 X1037/6 GND n L=1.8e-07 W=9.9e-07 AD=4.9005e-13 AS=3.564e-13
mX1037/M2 83 N21 VDD VDD p L=1.8e-07 W=1.35e-06 AD=7.29e-13 AS=6.9255e-13
mX1037/M3 VDD 38 83 VDD p L=1.8e-07 W=1.35e-06 AD=6.9255e-13 AS=7.29e-13
...
```

- netlist with the position of the inputs/output pins of each type of gate

```
.SUBCKT inv01 A Y GND VDD
.SUBCKT nor02 A1 Y A0 VDD GND
.SUBCKT xor2 A0 A1 Y VDD GND
.SUBCKT nand02 A1 A0 Y GND VDD
.SUBCKT nand03 A0 Y A1 A2 VDD GND
.SUBCKT and02 A0 A1 Y GND VDD
.SUBCKT nor04 Y A3 A2 A1 A0 GND VDD
...
```

- inputs/outputs ports of the circuit

```
input N1 N4 N8 N11 N14 N17 N21 N24 N27 N30 N34 . . .
output N223 N329 N370 N421 . . .
```

STAF – In the STAF the process parameters variations (such as length, width, oxide thickness and threshold voltage) are considered. Also, include simultaneously the most important issues in nanometer technologies, such as: (1) spatial correlation of the process parameters such as length, width and oxide thickness of the transistor, (2) random placement of dopants, and (3) the signal correlation due to reconvergent paths. This block receives the netlist information. Levelized covariance propagation along with the maximum operation, propagate the timing delay information considering each issue.

FAULT MODELING – An Open / Bridge defect fault modeling is implemented. Generated information by the STAF is required at this step. In addition, defect information is necessary. In this step the increase small-delay due to defects are added at the previous gate

delay. Later, the STAF function is called again to propagate these small-delays. The defect information consist of another netlist containing the list of defects to consider, which, also must have the given form.

- coupling capacitance netlist for bridge defects

```
cc_117 93 12 0.10962f
cc_118 102 12 0.05481f
cc_130 15 14 1.04451f
cc_131 16 14 0.1224f
cc_133 18 14 0.05481f
cc_134 19 14 0.294f
....
```

CONDITIONAL IS TRUE? – When the propagation of the small-delay is reached, the procedure is repeated for the next defect. Then, the conditional is true if all defects were considered.

SFC – A methodology to calculate the probability of detection for each defect in a given range of values is developed and implemented. Using this, the SFC is computed for the circuit.

FAULT COVERAGE – Knowing the fault coverage for each circuit, the circuit testability to the detection of small delay defects can be evaluated.

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Bibliography

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