Wide tuning range CMOS quadrature oscillators for high frequency phase shifter circuits

By

Clara Iliana Martínez Gómez

A Dissertation submitted in partial fulfillment of the requirements for the degree of:

MASTER OF SCIENCE IN ELECTRONICS

at the

Instituto Nacional de Astrofísica, Óptica y Electrónica

June 10, 2016

Santa María Tonantzintla, Puebla

Under the supervision of:

Dr. Alejandro Díaz Sánchez

Dr. Luis Abraham Sánchez Gaspariano

"There is nothing so powerful as
an idea whose time has come."

Victor Hugo.

To José Manuel,
who is the hope for a better future

Aknowledgements

My Master studies were funded by the CONACyT of México through the scholarship number 549773 at the INAOE. To both institution I extend my acknowledgements for providing me the facilities to realize my Master.

I would also like to thank Dr Alejandro Díaz Sánchez and Dr. Luis Abraham Sánchez Gaspariano not only for being my advisors and provide all the support for carrying out my project, but for keeping alive the sense of discovery and enjoyment in circuit design.

I also thank the members of my dissertation committee. With their remarks, valuable suggestions, and enlightening discussions, the final manuscript improved vastly.

Clara Iliana

RESUMEN

TÍTULO:

Osciladores CMOS de cuadratura con amplio rango de entonado para circuitos de desplazamiento de fase en frecuencias altas.

AUTOR:[1] Clara Iliana Martínez Gómez

PALABRAS CLAVE:

Oscilador de cuadratura; circuito de corrimiento de fase; RF; comunicaciones inalámbricas.

DESCRIPCIÓN:

El uso de señales en cuadratura, es decir señales desfasadas una respecto a la otra por 90 grados, es una práctica común en áreas tales como los sistemas de comunicación inalámbrica y el procesamiento digital. Entre las bondades de la cuadratura se encuentran su elegante representación matemática de baja complejidad así como el hecho de que al realizar convoluciones con estas señales la componente de imagen o banda lateral inferior desaparece realizando simples operaciones aritméticas entre ellas.

Algunas técnicas sofisticadas de recepción inalámbrica, como los arreglos multi-fase de formación de haz (beamforming phased arrays), requieren seales de alta frecuencia (RF) con múltiples fases para cancelar interferencias. Una posibilidad para la generación de corrimientos de fase de señales senoidales de RF es la suma o resta de señales en cuadratura con diferentes amplitudes. La precisión del corrimiento de fase realizado de este modo es sensible a la exactitud de la cuadratura, por lo que el error de ésta debe ser bajo ($< 3\%$).

En la investigación desarrollada se analizaron diversas técnicas para la generación de señales en cuadratura de alta precisión y amplio rango de entonado en frecuencias altas (GHz). El estudio reveló que aquellas que reúnen las mejores características son las basadas en acoplamiento de osciladores de primer orden, específicamente los os-

[1]Departamento de Electrónica. Diseño de circuitos integrados.

ciladores de dos integradores. A partir de estos hallazgos, se diseñó un oscilador CMOS de cuadratura de dos integradores controlado por voltaje (Q-VCTIO por sus siglas en inglés) en tecnología UMC mixed-mode/RF de 180nm cuyos resultados de simulación incluyen: frecuencia central de 2.445GHz; ancho de banda de 570MHz; ruido de fase de -115dB y error de fase de 0.008grados.

A su vez, con el oscilador propuesto se verificó, a nivel simulación, que es posible generar 140 diferentes corrimientos de fase, entre 4 y 345 grados con incrementos de 0.6grados, aproximadamente, controlados digitalmente por un palabra de 8 bits. Dichos corrimientos se pueden realizar en un rango de frecuencias comprendido entre los 2.12GHz y los 2.49GHz. Por lo tanto, el trabajo realizado introduce una novedosa arquitectura CMOS para realizar corrimientos de fase con una ancho de banda de 370MHz a una frecuencia central de 2.305GHz.

SUMMARY

TITLE:

Wide tuning range CMOS quadrature oscillators for high frequency phase shifter circuits.

AUTHOR:[2] Clara Iliana Martínez Gómez

KEY WORDS:

Quadrature oscillator; phase shifter circuit; RF; wireless communications.

DESCRIPTION:

The use of quadrature signals, i.e. signals out of phase by 90 degrees with respect each other, is a common practice in areas such as wireless communications and digital signal processing. Quadrature signals are easy to deal with and they do possess the convenient feature of filterless image cancellation by simple arithmetic manipulation.
Some sophisticated radio-receiver technologies, such as the phased array antennas, demand multi-phase high-frequency signals for interference cancellation. One possibility for generating phase shifts at RF frequencies is by fadding up quadrature signals. The accuracy of the phase shift realized in this way is sensitive to quadrature mismatch, thus a quadrature error $< 3\%$ must be guaranteed.
Diverse approaches for producing high-precision quadrature waveforms are discussed in this Thesis. From those, the ones with wide tuning range behavior at high frequencies are based on the use of coupled first order oscillators. The synthesis and design in UMC mixed-mode/RF 180nm CMOS technology of a wide tuning range quadrature voltage-controlled two-integrator oscillator (Q-VCTIO) is presented. Some important simulation results include: a center frequency of 2.445GHz; a bandwidth of 570MHz; a phase noise of -115dB; and a phase error of 0.008 degrees.
Finally, with the proposed Q-VCTIO, the design of an 8-bit digitally controlled phase

[2]INAOE. Electronics Department. Integrated circuits design.

shifter circuit with 140 phase steps ranging from 4 to 345 degrees is realized. The proposed phase shifter has a frequency of operation from 2.12GHz to 2.49GHz. Therefore, a wide tuning range high frequency phase shifter circuit based on a Q-VCTIO is introduced.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Quadrature Signals

Nowadays, many wireless communications use quadrature signal (I/Q) processing. Technologies such as Wi-Fi, UWB and WCDMA employ the Zero-IF transceiver (TRX) architecture [1]. Zero-IF CMOS TRXs exploit the I/Q processing advantage of avoiding the image problem with a high-integrable low-cost solution [2]. The main drawback of these TRXs is their high sensitivity to low-frequency interference and 1/f noise [3].

One of the key building blocks of Zero-IF CMOS TRXs is the oscillator that produces the quadrature waveforms which make possible the I/Q processing. However, before inquiring about the oscillator some background about quadrature signals is needed to establish a starting point. The purpose of this section is to provide the big picture about the complex signals representation. References [4]- [11] describe the topic in more detail.

Figure 1.1 shows a continuous complex signal (red) in time domain with its in-phase (black), I, and quadrature (blue), Q, components. Mathematically, the quadrature is expressed by the identity of Euler:

$$Ae^{j2\pi f_0 t} = Acos(2\pi f_0 t) + jAsen(2\pi f_0 t) \tag{1.1}$$

where A and f_0, are the amplitude and frequency of the signal, respectively; j is the

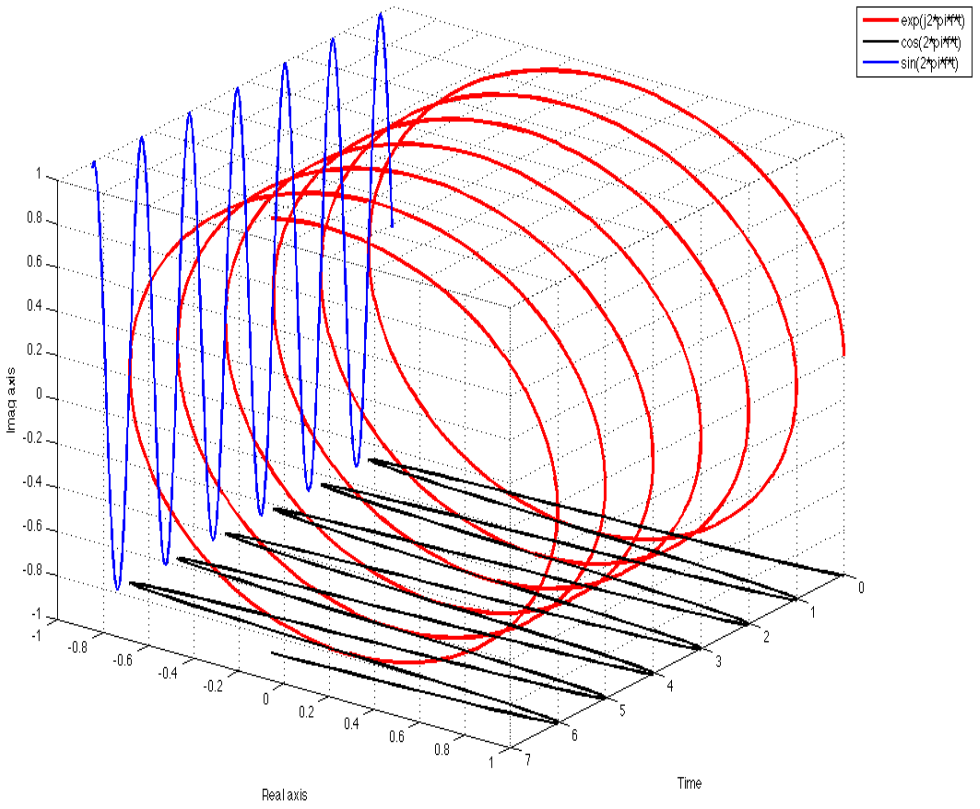


Figure 1.1: $Ae^{j2\pi f_0 t}$ continuous complex signal in time domain.

imaginary number $\sqrt{-1}$.

From a 3-D perspective with *time*, I and Q as the axes, continuous quadrature signals follow a corkscrew path. The amplitude of the twist depends on the amplitude of both the in-phase and quadrature components meanwhile the turn speed is determined by the frequency f_0. In case the quadrature component is positive, then the spin direction is counter clockwise; on the other hand, if the Q component is negative, then the spin direction is clockwise.

Another way to look at the complex signal is from the outlook of phasors. Since the I and Q components are sinusoidal functions, these have a magnitude and a phase that produce a new phasor (the phasor of the complex signal) when added up. Figure 1.2 depicts this representation. It can be seen that for a given instant of time the built

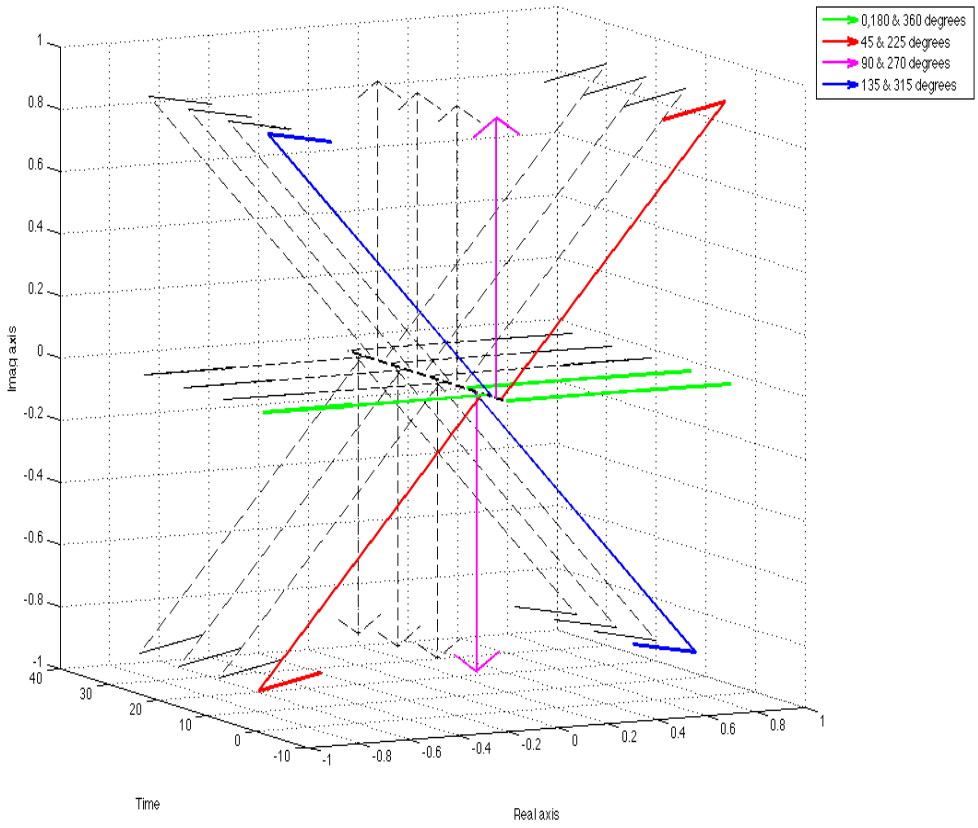


Figure 1.2: $Ae^{j2\pi f_0 t}$ as a phasor.

complex phasor is highlighted. The advantage of the phasor representation in the time domain is the ease of the mathematical handling [4].

Finally, the frequency domain representation of a complex signal is illustrated in Figure 1.3. The bandwidth of the in-phase and the quadrature components are combined to generate the bandwidth of the complex signal. As in the real signals case, complex signals have positive and negative frequency components. However, for quadrature signals the negative frequency parts are in counter phase whereas positive frequency components are aligned.

To appreciate the advantage of frequency properties of complex signals Figure 1.4 depicts the process of quadrature sampling by means of I/Q demodulation. As can be seen, frequency translation to base band is performed by mixing quadrature signals

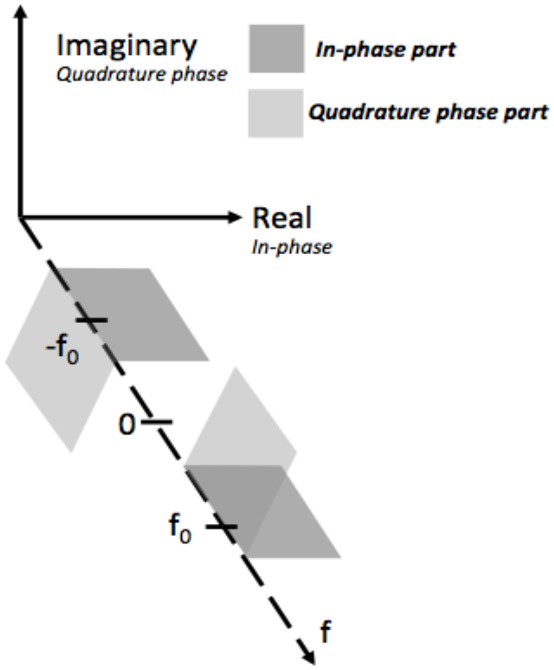


Figure 1.3: Representation of quadrature signal in frequency domain.

with the bandpass signal, X_{bp}. The bandwidth of X_{bp} is centered at frequency f_c and then down-converted by the in-phase, $cos(2\pi f_c t)$, component as well as the quadrature, $sin(2\pi f_c t)$, component into two different signal paths. By subtracting the I/Q signals at the end of the chains, the attained spectrum corresponds to a single signal with the bandwidth of X_{bp} but centered at DC.

In sum, due to the ease of complex signal representation quadrature signals processing is very useful to accomplish operations such as frequency translation and combination/separation of signals. This features are specially advantageous in wireless communications where upconversion and downconversion of information is performed.

1.2 Complex Signal Processing in Electronics and Telecommunications

As mentioned earlier, I/Q processing is used in many wireless communications. In addition, some other signal processing applications take advantage of the I/Q pro-

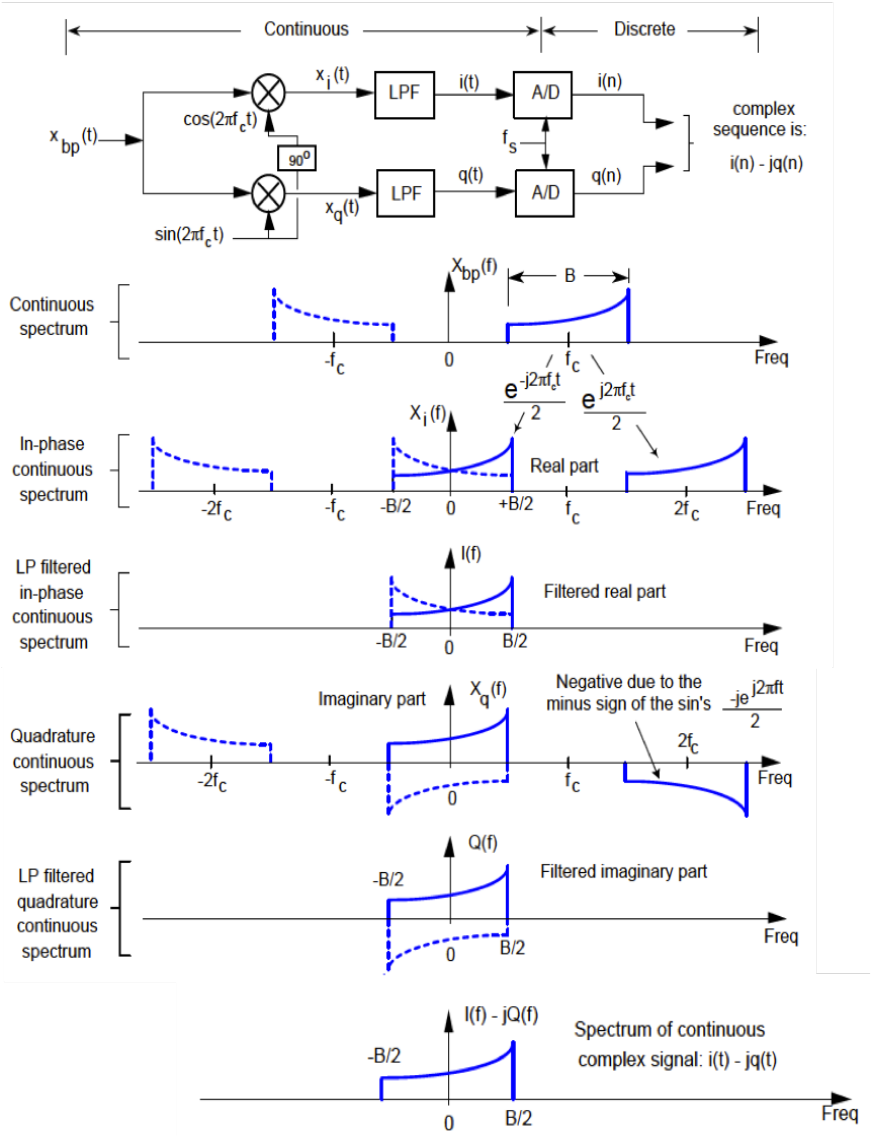


Figure 1.4: Quadrature-sampling block diagram and spectra.

cessing. Figure 1.5 illustrates some of these systems, which include [1], [4], [12]- [17]: digital communications systems, radar systems, time difference of arrival processing in radio direction finding schemes, coherent pulse measurement systems, antenna beamforming applications, single sideband modulators, image-reject mixers, low-intermediate frequency transceivers, complex filters, synchronous filtering, polyphase filter, phase-locked loops and arbitrary waveform generators, among others.

The application of interest in this Thesis is within the scope of wideband, wide tuning range CMOS quadrature oscillators. By generating I/Q signals capable of being

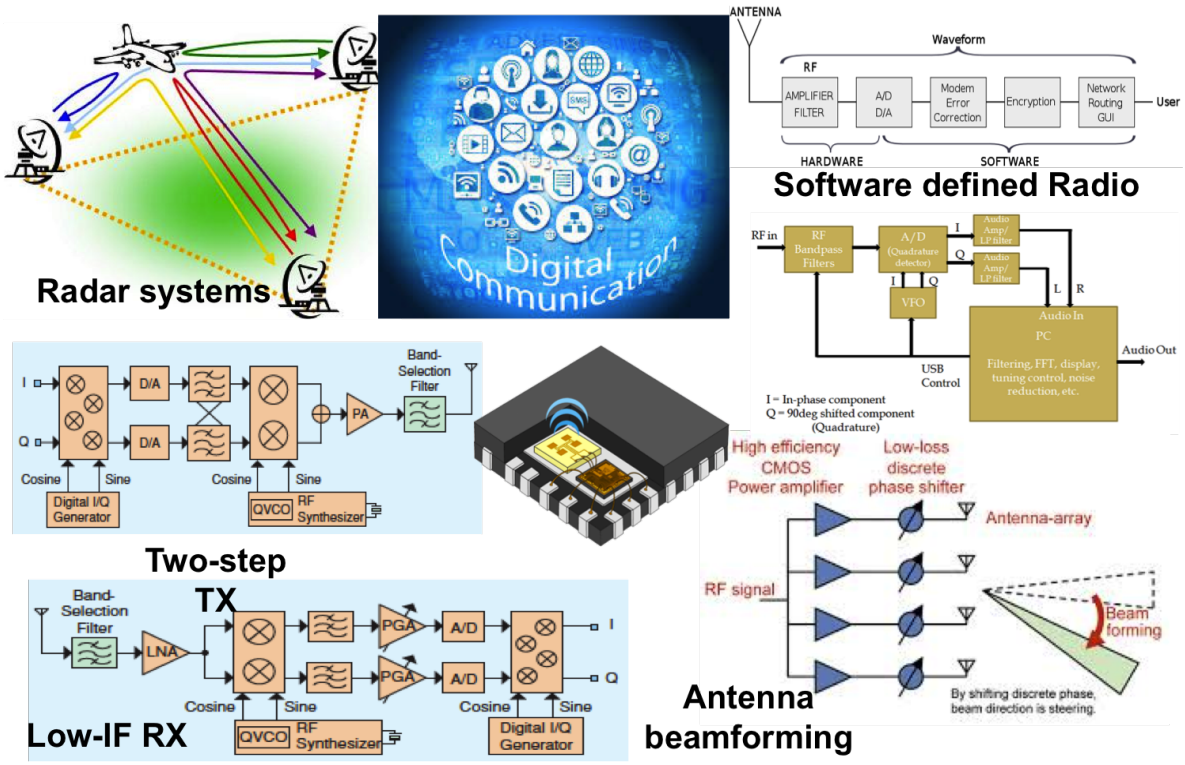


Figure 1.5: Complex signal processing in electronics and telecommunications.

tuned in a large frequency range, the possibility to extend the use of signal processing commonly confined to the low frequency domain to the RF realm is open.

1.3 Motivation and Thesis Outline

Phase shifter circuits have several applications in different systems such as phased array antennas [18], PSK modulators/demodulators [19], and distortion cancellation produced by nonlinear circuits with a combination of multi-paths and polyphase signals [20], to name a few. There are two fundamental demands for phase shifters: to preserve a constant phase versus frequency and to exhibit a linear phase versus frequency. Since low cost and high integration are preferable, an intense research has focused in many different approaches for high-frequency phase shifter circuits in CMOS technology [21].

To overcome the lack of implementations that make available a broad range of phase control combined with low complexity, a wide range phase shifter based on the concept

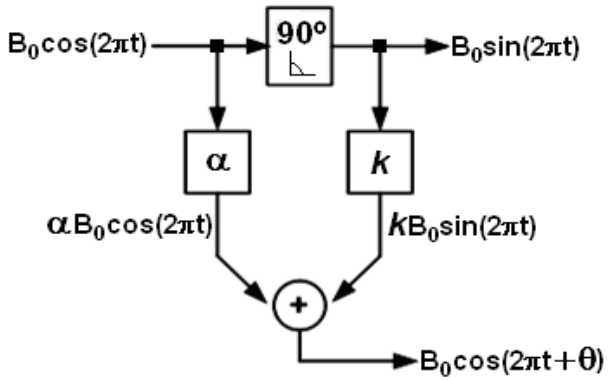


Figure 1.6: Block diagram of the phase shifter solution proposed in [22].

of vector projection has been proposed in [22]. One of the key building blocks of this solution is the orthogonalizer, whose function is to shift 90 degrees the input signal to, subsequently, modify the in-phase and quadrature components which are added at the end to produce the phase shift; like depicted in Figure 1.6.

Instead of using an all-pass filter as the orthogonalizer block, like in [22], it may be more convenient to employ a quadrature signal generator since a larger bandwidth is exhibited by quadrature oscillators. Thus, the Thesis is focused on the synthesis and design of sideband, wide tuning range CMOS quadrature oscillators. The manuscript is organized as follows: chapter two delves into the diverse techniques for complex signal generation; later, in chapter three, the two alternatives explored, a new two-integrator oscillator topology and the known two-integrator oscillator improved with programmable current mirrors, with their corresponding simulation results are reported; finally, conclusion is drawn in chapter 4 along with directions along which to take future research.

Chapter 2

Complex Signal Generation

2.1 Quadrature Oscillators Basics

Oscillators are key building blocks in diverse electronic systems such as clock and data recovery [24], wired and wireless transceivers [25], timing reference in digital signal processing [26], and high speed data converters [27], among others. The basic function of an oscillator is to generate a periodic signal with certain properties. An ideal oscillator generates a signal that only has wanted properties. The signal waveform can have any form and any number of harmonics. Figure 2.1 depicts four types of commonly used oscillators.

The output voltage of an ideal harmonic oscillator with angular frequency ω_{osc} in radians per second and peak amplitude V_{peak} in Volts, can be written as [23]

$$V_{out}(t) = V_{peak}cos(\omega_{osc}t + \phi_0) \tag{2.1}$$

where ϕ_0 is the initial phase of $V_{out}(t)$ at $t = 0$. In the frequency domain, this is equivalent to a discrete spectral line with amplitude V_{peak} at angular frequency ω_{osc}. This means that all carrier power is located in an infinitely small bandwidth around ω_{osc}. This is the kind of oscillator illustrated in Figure 2.1 (a).

On the other hand, the output signal of tunable harmonic oscillator can be represented by [23]

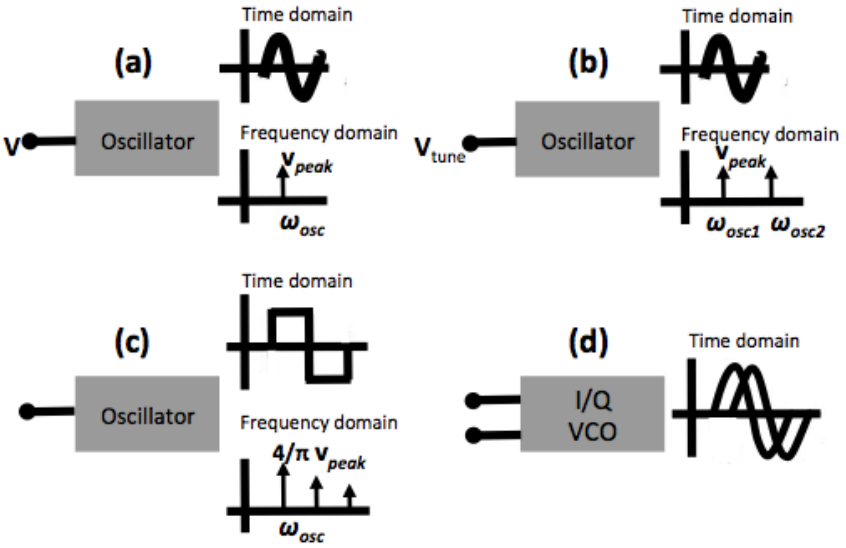


Figure 2.1: (a) harmonic oscillator, (b) harmonic VCO, (c) square wave oscillator, (d) I/Q oscillator.

$$V_{out}(t) = V_{peak}cos(2\pi(K_{VCO}V_{tune} + f_{center})t + \phi_0) \tag{2.2}$$

Frequency ω_{osc1} and ω_{osc2} in Figure 2.1 (b) represent the minimum and maximum frequency of the oscillator. Tuning voltage V_{tune} controls the frequency, and tuning constant K_{VCO} in Hz/V determines the tuning slope. f_{center} is the oscillation frequency with a zero tuning voltage. As the tuning input is a voltage, the oscillator in Figure 2.1(b) is a Voltage Controlled Oscillator (VCO). In the case of a Current Controlled Oscillator(CCO), the tuning constant K_{VCO} will have the units Hz/A.

Another possibility is an oscillator which produces a square wave instead a sinusoid at its output port, like in the case depicted in Figure 2.1 (c). The most common way to produce square waves in CMOS technology is by means of ring oscillators [3]. Digital systems, data converters and some transceiver arquitectures employ this kind of oscillator.

Instead of generating one output signal, an oscillator can generate several output signals with different phases. A special case of a multi-phase oscillator is an oscillator, which generates a sine and a cosine, see Figure 2.1 (d). Many modern transceiver

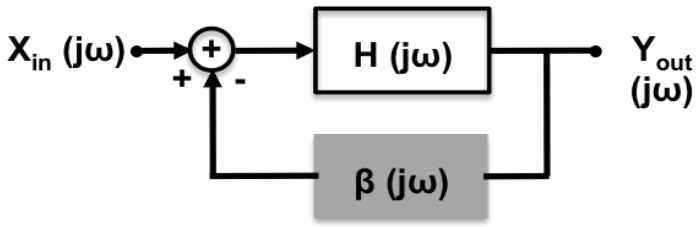


Figure 2.2: Block diagram of a linear feedback model for analyzing oscillation conditions.

architectures require these so-called I/Q signals in their signal-processing component.

It is crucial to predict whether the oscillator under design is properly dimensioned, so that the oscillator will start and produce a periodic signal. All oscillators in Figure 2.1 are feedback systems and in most instances feedback modeling is used to assess the oscillation conditions.

Figure 2.2 shows a general block diagram of a linear feedback system with transfer functions *H(jw)* and *β(jw)*. The conditions needed for oscillation are most easily analyzed using linear models. For many practical oscillators, linear analysis of the oscillation conditions provides sufficiently qualitative and quantitative insight for oscillator design. The transfer function $Y_{out}/\ X_{in}$ of the linear system in Figure 2.2 is the general equation for a feedback system

$$\frac{Y_{out}(jw)}{X_{in}(jw)} = \frac{H(jw)}{1 + H(jw)\beta(jw)} \tag{2.3}$$

The necessary conditions for steady-state oscillation are known as the Barkhausen conditions. The first condition is called the gain condition and specifies that the open-loop gain must be unity. The gain condition for steady state oscillation states [23]

$$|H(jw)\beta(jw)| = 1 \tag{2.4}$$

The second condition for oscillation is referred to as the phase condition, which is expressed as [23]

$$\angle H(jw)\beta(jw) = (2m + 1)180^{\circ} \tag{2.5}$$

This phase condition states that the total open-loop phase shift must be $(2m + 1)$ times 180 degrees, where m is an integer value including zero.

Additionally, once an oscillator has started there must be a mechanism that reduces the loop gain α_{OL}=$|H(jw)\beta(jw)|$ effectively to unity, since this is a necessary condition for steady state oscillation. There are two mechanisms, automatic gain control and self-limiting, which reduce α_{OL} to one after start-up and stabilize the amplitude.

One option for amplitude stabilization, called self-limiting, is to use the nonlinear characteristic of an active element in the oscillator. Since this method does not need additional circuitry, it is often used in high-frequency oscillators. In the literature the simplest self-limiting oscillator is often referred to as the *Van der Pol* oscillator.

A second method for amplitude stabilization is to use an Automatic Gain Control (AGC), where the oscillation amplitude is measured and used in a negative feedback control loop that stabilizes the oscillator amplitude to a set value after start-up. Main reasons to use AGC are: fast and reliable start-up; combining optimum biasing for noise with reliable start-up; obtaining a well-defined output level; power dissipation reduction.

For many practical oscillators, including the quadrature oscillators, linear analysis of the oscillation conditions provides sufficiently qualitative and quantitative insight for oscillator design. However, an oscillator may well operate in the weakly or strongly nonlinear region making linear modeling inadequate for capturing the full behavior of these oscillators. The least a designer should do is see how well application of the linear oscillation conditions compares with transient simulations, which reveals the influence of nonlinearities in the oscillator.

2.2 Requirements for Quadrature Oscillators

The design space of an oscillator can be visualized by an N-dimensional hyper-cube, in which each oscillator property is assigned to a separate axis [23]. Figure 2.3 depicts the design space for quadrature oscillators. It can be appreciated that it consists of an

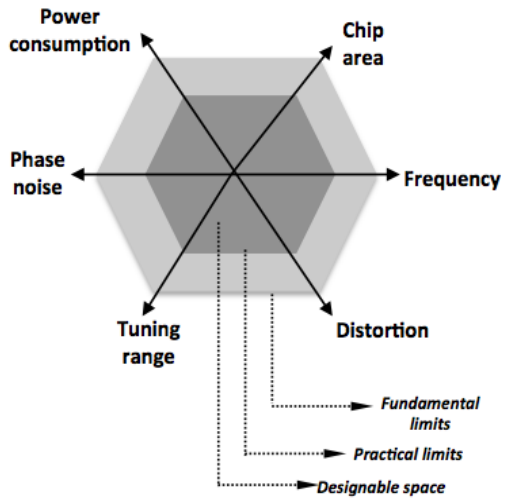


Figure 2.3: Design space for Quadrature Oscillators.

hexagon whose edges include: *tuning range, frequency, phase noise, power consumption, chip area* and *waveform aspect (distortion).*

Frequency and tuning range are important specifications that can have a significant impact on the level of difficulty when designing an oscillator. In general, the higher the center frequency of an application, the more difficult it is to design an oscillator for this application. For some applications only the center frequency is specified, but most oscillators need to cover a band of interest around a center frequency. As for any specification, the tuning range specification must be met under worst case conditions. Therefore frequency deviations due to temperatura changes, process spread and power supply variations should be added to the tuning range.

In practice, every oscillator generates some power at other frequencies than the fundamental frequency desired. Due to nonlinearities in the oscillator, harmonics of the fundamental frequency will be generated. These harmonics are specified in dB relative to the carrier (dBc). In many cases, nonlinear operation of an oscillator improves the phase noise, but also generates harmonics.

An oscillator normally is part of a larger system with a restricted power budget. Low power design is important, especially for portable applications. Minimum power dissipation also is important for applications that are connected to the mains, since the

whole system has to fit into a cheap package with a certain termal resistance. In such a case, low power means the possibility of a higher degree of integration. The power budget of an oscillator is usually specified in milli-watts, or by the available current given by a supply voltage. The attainable phase noise $\mathcal{L}(fm)$ levels in an oscillator are directly related to the power dissipation.

The technology plays an important role in the performance and cost of an oscillator. For example, the inductor quality is much better on high-ohmic substrates compared to low-ohmic substrates. It is therefore much easier to realize high-performance LC oscillators on high-ohmic substrates. However, one of the most salient problems with LC oscillator is the area consumption of the inductors. If chip area minimization is important, the use of a large number of large planar coils should be avoided. Ring oscillators usually are much more compact than LC oscillators, but also are much noisier (as a rough rule of thumb, approx. Q2 times) at comparable power dissipation levels.

Figure 2.4 illustrates the definition of phase noise, $\mathcal{L}(fm)$. As shown, P_{signal} is the result of an integration of the power spectral density of the output waveform, $S_{v_{out}}$, around f_{osc}. Provided that the integration interval is large enough to capture about 99%, P_{signal}, is a good approximation of total signal power. Clearly a high P_{signal}, and thus a large V_{peak} is desired for a small $\mathcal{L}(fm)$. Commonly, $10log(\mathcal{L}(fm))$ is specified and its units are dBc/Hz, indicating that the phase noise is measured relative to the carrier and in an 1 Hz bandwidth.

Design solutions always are inside the fundamental boundaries and practical boundaries. The area inside the practical limits can be regarded as designable space [23]. Fundamental limits refer to limits imposed by nature as we know it, for example the speed of light, c, or the charge of an electron, q. All the limits set by nature impose fundamental limits on the oscillator performance. Practical limits are imposed by the design resources, like technology. The IC technology used for oscillator implementation has non-ideal devices and properties, such as finite transition frequencies, interconnect capacitance, etcetera. These non-ideal elements limit practical oscillator performance.

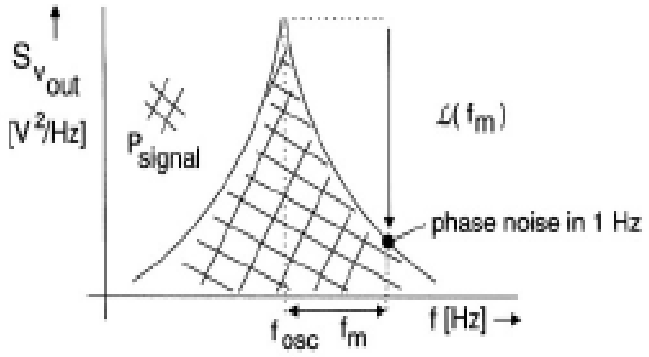


Figure 2.4: Phase noise definition.

At the beginning of an oscillator design, the functional specifications and design resources must be completely clear. Deriving a well understood and complete set of oscillator specifications from the application in which the oscillator will be used, can be a challenging task in itself. In any case, time spent on this task in the beginning of the design process is worth the effort, since it is difficult to "hit a moving target" (specification). Therefore, it is recommended to write the design specification of a certain oscillator property as [23]: *design specification equals nominal specifications plus technology margin plus safety margin.*

2.3 Quadrature Signal Generation

Quadrature signals can be generated in many ways. Some of the most employed approaches are depicted in Figures 2.5 and 2.6 with their most salient properties [23], [28]. Both advantages and disadvantages are highlighted.

As stated in section 1.3, the quadrature oscillator pursuit in this Thesis is intended for being employed in the phase shifter circuit based on vector projection. Since such phase shifter is desired to be suitable for RF applications [22], then the quadrature oscillator must exhibit high frequency operation, large tuning range, and very accurate quadrature.

From the many approaches detailed in Figures 2.5 and 2.6, those who present the adequate features for the application of interest are the even-stage ring oscillator and

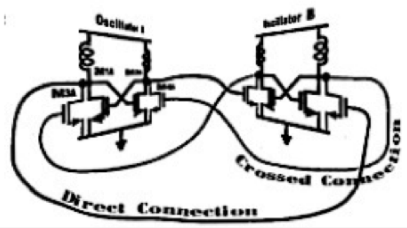
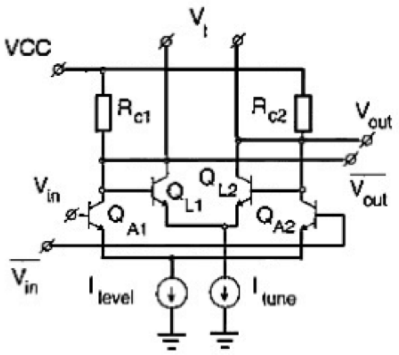
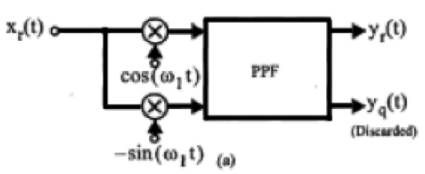
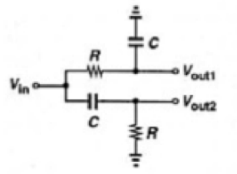
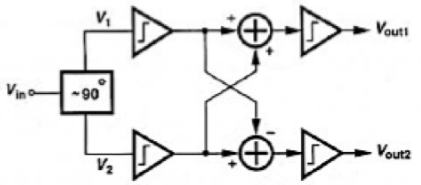
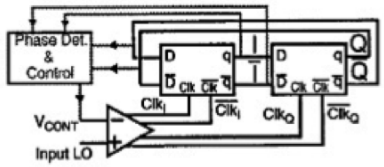
Approach	Properties	Topology
Even-stage LC oscillator	Good $\mathcal{L}(f_m)$ and linearity; large chip area and narrow bandwidth.	
Even-stage ring oscillator	Large tuning range and compact chip area; poor $\mathcal{L}(f_m)$ and power hungry.	
Oscillator at f_{osc} and Poly-phase filter	Good $\mathcal{L}(f_m)$; high noise floor **and** insertion loss; bandwidth limited.	
Oscillator at f_{osc} and RC-CR Network	Simple circuit; narrow bandwidth.	
Havens' Technique	Mismatch tolerant; large chip area; power hungry.	
Oscillator at 2 or 4 X f_{osc} with divider	Good $\mathcal{L}(f_m)$ when combined with LC oscillator; power hungry and relative low frequency operation.	

Figure 2.5: Different approaches for quadrature signal generation (I).

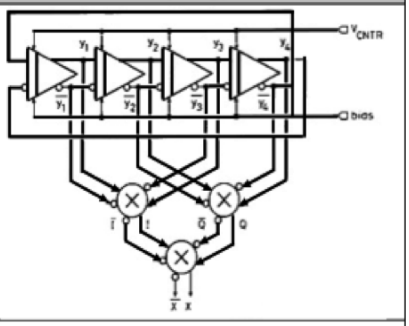
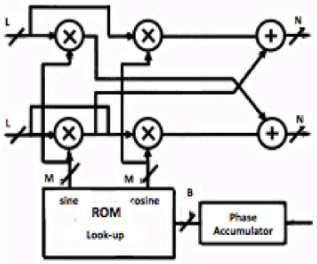
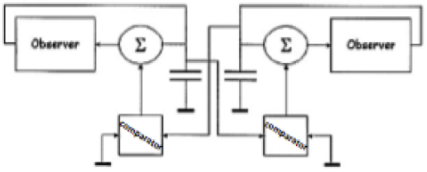
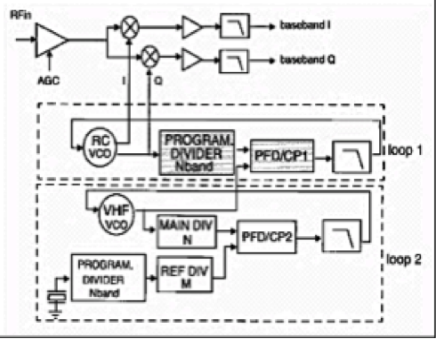
Approach	Properties	Topology
Four stage oscillator at ½ f_{osc} with mixers or addition of phases	Wide bandwidth; large chip area; poor $\mathcal{L}(f_m)$.	
Digital implementation (look up table and reference clock)	Accurate; wide bandwidth; A/D needed if signals are in the analog domain; low frequency operation.	
Injection locked oscillator - Quadrature coupling of first order oscillators	Very accurate quadrature; design flexibility - features are equal to those of the first order oscillator employed.	
Double PLL loop (ring oscillator at f_{osc} looked to LC oscillator)	Good $\mathcal{L}(f_m)$ and bandwidth; high complexity and power dissipation.	

Figure 2.6: Different approaches for quadrature signal generation (II).

the quadrature coupling of first order oscillators. However, the former solution has two significant drawbacks: poor $\mathcal{L}(f_m)$ and output waveform. Typically, ring oscillator produce square waves. Unfortunately, the phase shift technique based on vector projection is effective only in sinusoidal signals. Thus, additional circuitry like resonators or bandpass filters must be employed with ring oscillators to have sine waves, which adds up complexity, noise and chip area.

On the other hand, the plus of the quadrature coupling of first order oscillators is its design flexibility since the features of the quadrature oscillator depend on the behavior of the occupied first order oscillator [32]. Quadrature coupling of first order oscillators is based on injection locking. It is possible to derive a stable pulse from a first-order oscillator by observing the integrator output signal by means of a comparator and compare it to a reference level (Figure 2.6). In that case the two oscillators run in quadrature [33]. From each of the two oscillators a pulse is derived that is injected in the other one to force a transition. The result is a much more stable first-order oscillator system that additionally produces quadrature signals with a high quality phase relation. Some choices to implement this injection locked system include: relaxation oscillators, LC-oscillators and two-integrator oscillators [34].

2.4 Quadrature Coupling of First Order Oscillators

This section summarizes the most salient features of quadrature coupling of: relaxation oscillators, LC-oscillators and two-integrator oscillators.

2.4.1 Quadrature Relaxation Oscillator

Figure 2.7 shows the circuit implementation with bipolar devices of a quadrature relaxation oscillator (named cross-coupled relaxation oscillator). The cross-coupled relaxation oscillator is implemented with two relaxation oscillators, which are cross-coupled using, as coupling blocks (soft-limiters), differential pairs that sense the capacitor voltage and have the differential output connected to the other oscillator [29]. The soft-limiter output is a differential current, which is added at the collector nodes. The effect of this current is to change the input switching levels of the Schmitt-trigger. Thus, this is equivalent to adding a voltage signal at the Schmitt-trigger input.

Each of the coupled oscillators in Figure 2.7 can be studied as a relaxation oscillator with two extra current sources, which are responsible for the coupling action. For instance, the two current sources i_{SL1} and i_{SL2} are provided by the soft-limiter circuit

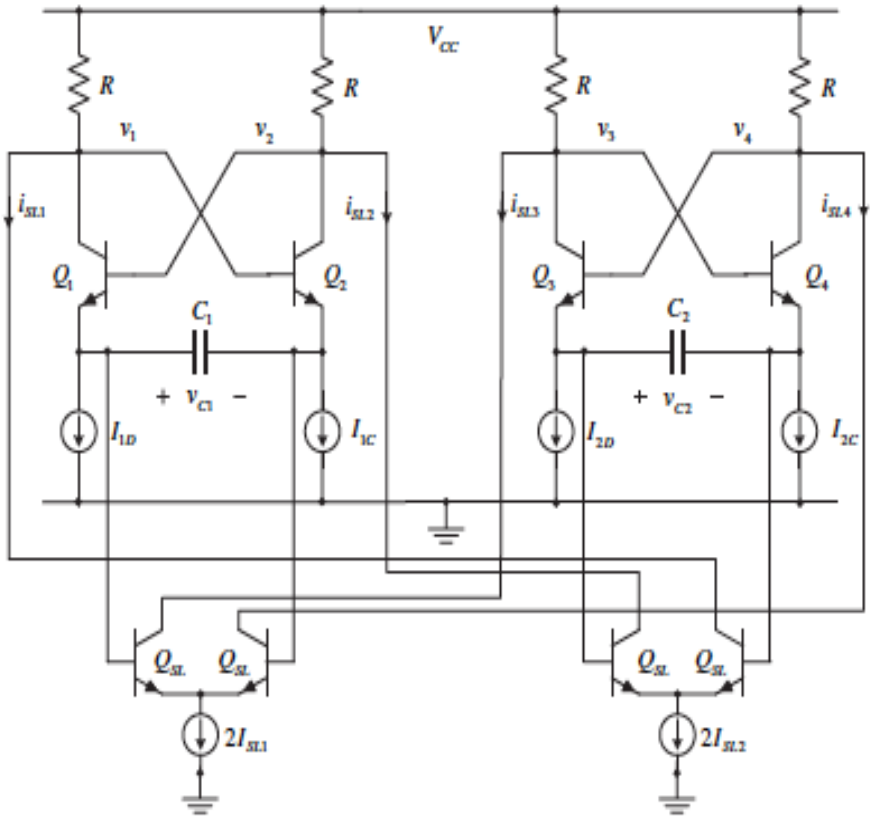


Figure 2.7: Cross-coupled relaxation oscillator.

driven by the second oscillator, i.e., one oscillator is synchronously switched (triggered) by the other oscillator.

We assume that there are no mismatches between the two oscillators and that the switching occurs instantly when there is a transition of the capacitor voltages by zero. The transistors are assumed to act as switches, which is a good approximation for bipolar transistors; this is also valid for MOS implementations (with high W/L transistors). The waveforms are shown in Figure 2.8.

It can be proved that the oscillation frequency is expressed as [29]

$$f_0 = \frac{1}{T} = \frac{1}{2RI^2} \frac{C}{C_1 C_2} \frac{I_{1C} I_{1D}}{(I_{1C} + I_{1D})} \frac{I_{2C} I_{2D}}{I_{2C} + I_{2D}} \tag{2.6}$$

where $I_{1D} = I_{1C} = I_{2D} = I_{2C} = I$.

Likewise, it can be verified that the $\mathcal{L}(f_m)$ is given by [29]

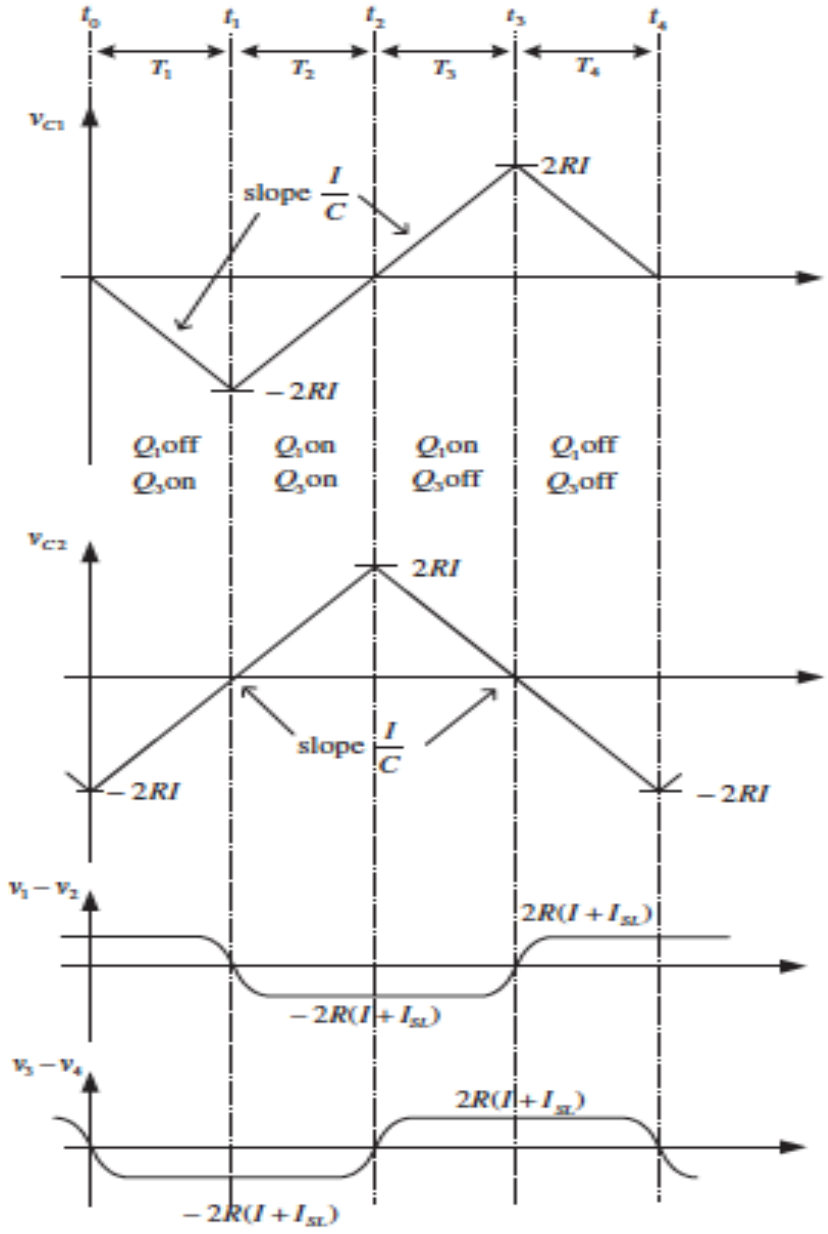


Figure 2.8: Waveforms in a symmetric quadrature oscillator (without mismatches).

$$\mathcal{L}(f_m) = 2\alpha \frac{4S(v_n)}{2V^2} \left(\frac{f_0}{f_m} \right)^2 \tag{2.7}$$

where $S(v_n)$ is the spectral density of the equivalent noise voltage, V is the Schmitt-trigger difference of threshold voltages, f_m is the frequency of a sinusoidal signal which represents the phase noise [29], and

$$\alpha = \frac{B_c}{2f_0} \tag{2.8}$$

B_c is the bandwidth for which there is significant noise conversion. This depends on the circuit implementation.

Some other aspects of the cross-coupled relaxation oscillator are discussed in subsection 2.4.4.

2.4.2 Quadrature LC Oscillator

The simplest and most used implementation of the LC oscillator uses transistors to generate the negative conductance [30]. The implementation in Figure 2.9 couples two equal LC oscillators, expecting to inherit the good phase noise performance of the individual oscillators. The coupling block is implemented, as in the relaxation oscillator, with a differential pair that senses the voltage at one oscillator output and injects a current in the second oscillator, in order to trigger it.

It has been demonstrated [30] that the oscillation frequency, f_0, of the circuit in Figure 1.5 is given by

$$f_0 = 2\pi f_{LC} - \frac{g_{mc}}{2C} \tag{2.9}$$

where f_{LC} is the resonance frequency of the LC tank and g_{mc} is the transconductance of the differential pair (M_{SL} devices).

The quality factor of the circuit, Q, which is other important parameter of LC oscillators [23], can be expressed as [30]

$$Q = \pi f_{LC} \left| \frac{LR_P(CL\omega^2 + 1)}{C^2L^2R_P^2\omega^4 - 2CLR_P^2\omega^2 + L^2\omega^2 + R_P} \right| \tag{2.10}$$

where R_P is the equivalent resistance of the cross-coupled pair (M devices) and ω the frequency.

Output waveform of quadrature LC oscillator are sinusoids, like those illustrated in

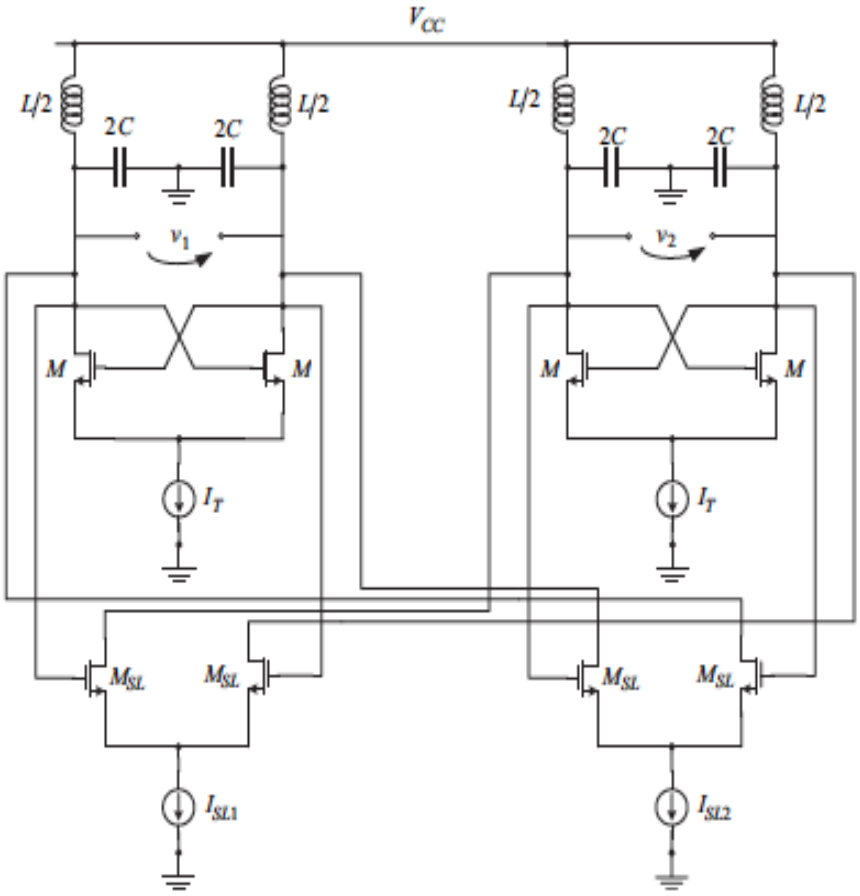


Figure 2.9: Quadrature LC oscillator.

Figure 2.10. Spectral purity of these signals depend on Q.

Finally, the $\mathcal{L}(f_m)$ for this oscillator is provided by [30]

$$\mathcal{L}(f_m) = 10log\left[\frac{2KT}{P_{carrier}}\left(\frac{\pi f_{LC}}{Q2\pi f_m}\right)\right] \tag{2.11}$$

where K is the constant of Boltzmann, T the temperature, $P_{carrier}$ the power of the output waveform, and f_m is the frequency of a sinusoidal signal which represents the phase noise [30].

Again, other aspects of the quadrature LC oscillator are discussed in subsection 2.4.4.

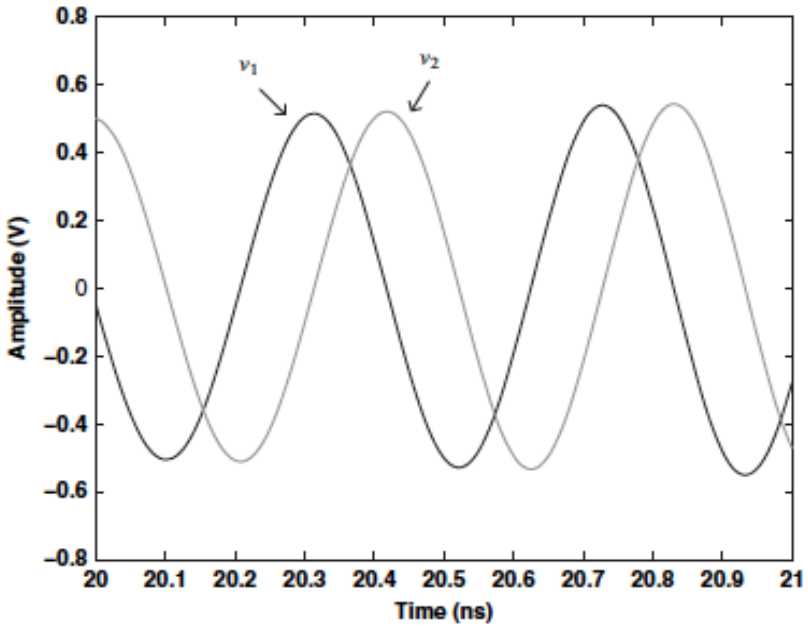


Figure 2.10: Waveforms in a quadrature LC oscillator.

2.4.3 Two-Integrator Oscillator

In the previous subsections the most salient features of the quadrature relaxation oscillator, which is strongly non-linear, and the quadrature LC oscillator, which is quasi-linear, were summarized. Both relaxation and LC oscillators have a limited tuning range, which is below one decade (typically lower than 20%) [28]. A third type of oscillator that exhibits either a non-linear behavior or a quasi-linear nature with a higher oscillation frequency and wide tuning range is the two-integrator oscillator (TIO).

The block diagram of a TIO is shown in Figure 2.11. As can be seen, it is composed of two integrators and two limiters that implement the sign function, connected in a feedback loop. Each integrator output determines the input polarity of the other integrator [32]. The oscillation frequency is proportional to the constant of integration and depends on the oscillator amplitude.

Depending on the non-linear nature of the limiters it is possible to have a non-linear behavior or a quasi-linear conduct. If the limiters are hard-limiters, then triangular waveforms are available at the output meanwhile sinusoids are feasible in case the limiters are soft-limiters. Moreover, if the integration constant is different in each inte-

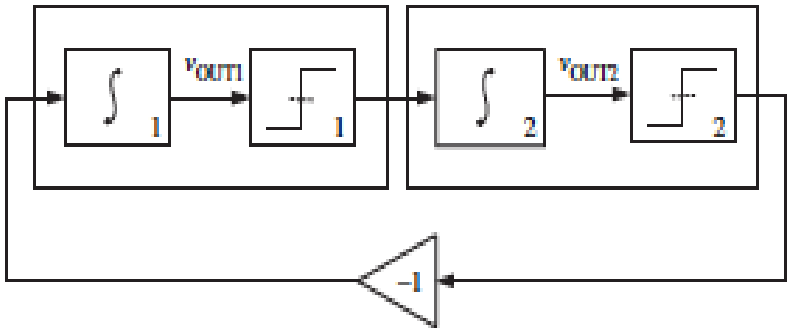


Figure 2.11: Block diagram of a two-integrator oscillator.

grator, the amplitudes of the output waveforms will differ but the quadrature condition will remain. Figures 2.12 and 2.13 depicts these two types of possible output waveforms.

For the hard-limiter case, the oscillation frequency considering different integration constants, K_{i1} and K_{i2}, is given by [31]

$$f_0 = \frac{1}{4\left(\frac{V_{INT1}}{K_{i1}} + \frac{V_{INT2}}{K_{i2}}\right)} \tag{2.12}$$

where V_{INT1} and V_{INT2} are the initial values.

The integrator output amplitudes are dependent on the initial conditions of the two-integrators and on their integration constants, i.e. [31]

$$V_{OUT1} = 2\left(V_{INT1} + \frac{K_{i1}}{K_{i2}} V_{INT2}\right) \tag{2.13}$$

$$V_{OUT2} = 2\left(V_{INT2} + \frac{K_{i2}}{K_{i1}} V_{INT1}\right) \tag{2.14}$$

On the other hand, for the soft-limiter case, the oscillation frequency is expressed as [31]

$$f_0 = \frac{\sqrt{K_{i1} K_{i2}}}{2\pi} \tag{2.15}$$

where K_1 and K_2 are the gains of the first and second integrators in cascade with their

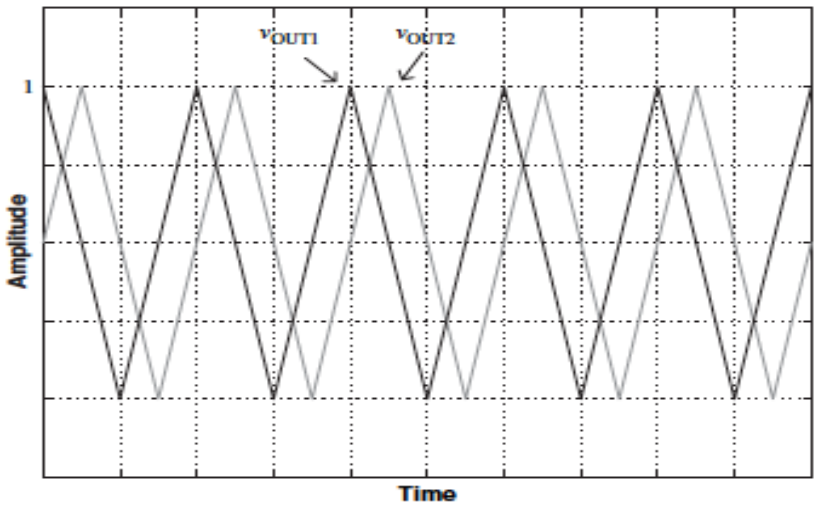


Figure 2.12: Triangular output waveforms of a two-integrator oscillator.

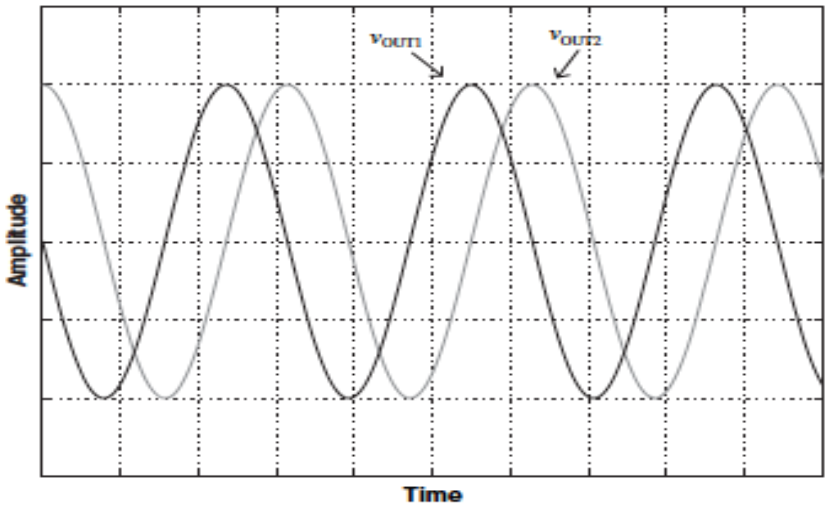


Figure 2.13: Sinusoid output waveforms of a two-integrator oscillator.

corresponding limiters.

For this case, the output waveform amplitudes are defined by the soft-limiter saturation levels. It is important to point out that in the presence of mismatches, amplitudes of both hard-limiter and soft-limiter cases change as the oscillation frequency is tuned [31].

Considering that hard-limiters are critical blocks because it is difficult to design them for high frequencies, at such frequencies quasi-linear behavior is easier to attain.

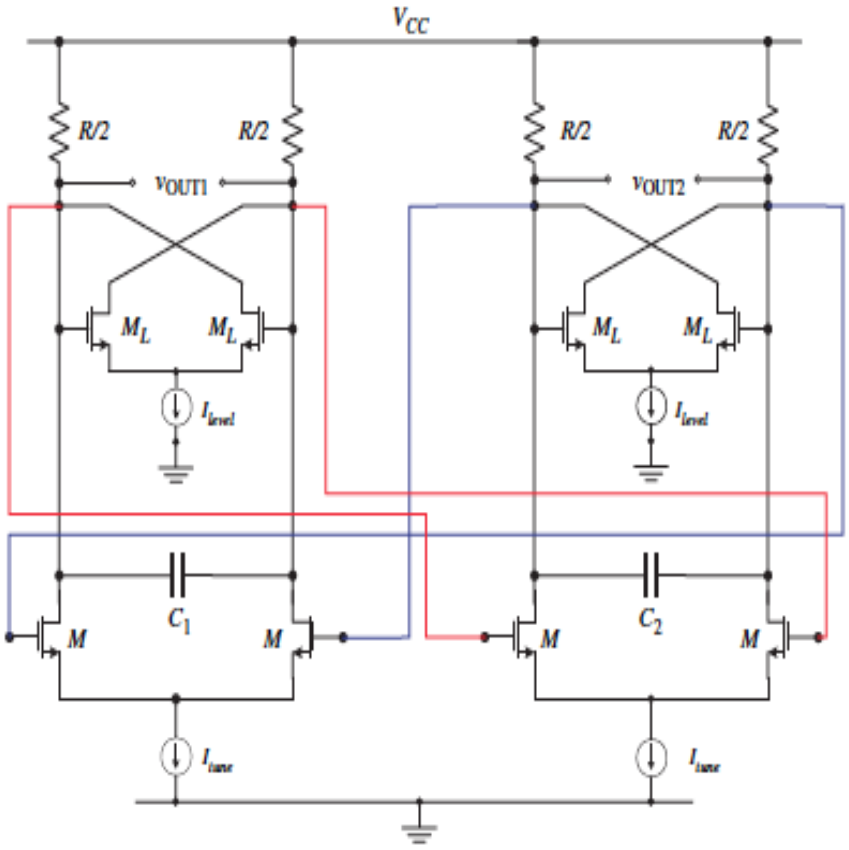


Figure 2.14: Two-integrator oscillator implementation.

A TIO circuit is presented in Figure 2.14 [28]. Each integrator is realized by a differential pair (transistors M) and a capacitor ($C_{1,2}$). The oscillator frequency is controlled by I_{tune}. There is an additional differential pair (transistors M_L), with the output cross-coupled to the inputs, which performs two related functions: compensation of the losses due to R to make the oscillation possible (a negative resistance is created in parallel with C); and amplitude stabilization, due to the non-linearity (the current source I_{level} controls the amplitude).

It should be noted that the correspondence between the circuit of Figure 2.14 and the block diagram in Figure 2.11 is conceptual and not topological. It is easy to demonstrate that the oscillation frequency of circuit in Figure 2.14 is given by [31]

$$f_0 = \frac{g_m}{2\pi C} \tag{2.16}$$

where g_m is the transconductance of the differential pair (M_L devices).

From equation (2.16) we can conclude that the oscillator frequency varies by changing either the capacitance or the transconductance. In a practical circuit we can use varactors to change the capacitance or, most commonly, we can change the tuning current and therefore the transconductance. With the second approach, if the transconductances are implemented by bipolar transistors the frequency changes linearly with the tail current. If the transconductances are implemented with MOS transistors the frequency will be proportional to the square root of the tail current. Since we can change the transconductance in a wide range, these oscillations have wide tuning range.

The circuit of Figure 2.14 can work in two different modes: (1) If we over-compensate the losses by increasing I_{level}, the performance is nonlinear and resembles that of the block diagram in Figure 2.11. With a strong non-linear performance (the transistors operate as switches) the waveforms are approximately triangular. In this case the oscillator amplitude is:

$$V_{OUT} = I_{level} R \tag{2.17}$$

and thus, the oscillation frequency is given by [31]

$$f_0 = \frac{I_{tune}}{2CV_{OUT}} \tag{2.18}$$

In this case the oscillator has a behavior similar to that of a relaxation oscillator. (2) If we compensate the losses only to the amount necessary for the oscillations to start, the transistors in the circuit of Figure 2.14 work in the linear region, and the outputs are close to sinusoidal with the amplitude that satisfies the condition [31]:

$$\frac{1}{g_{mL}} = R \tag{2.19}$$

Since linear operation has been assumed, the currents in the transistors of the differential pair do not reach the value of the source current I_{level}. However, it has been found that in practice the output amplitude can be approximated as [31]

$$V_{OUT} = I_{level}R \tag{2.20}$$

Finally, the two-integrator oscillator phase-noise is [31]

$$\mathcal{L}(f_m) = 10log\left[\frac{4KT}{RI_{rms}^2}\left(\frac{f_0}{f_m}\right)^2\right] \tag{2.21}$$

where K is the constant of Boltzmann, T the temperature, f_m is the frequency of a sinusoidal signal which represents the phase noise [31], and I_{rms} is the rms current at the output of transconductance g_m.

In section 2.4.4 a discussion about the three reviewed coupled oscillators is provided.

2.4.4 Comparisons

Table 2.1 provides a comparison among the three quadrature coupling of first order oscillators discussed in the previous subsections. It can be seen that the three approaches exhibit the mixing function. However, only quadrature relaxation and two integrator oscillators possess very accurate quadrature. From these, $\mathcal{L}(f_m)$ is good in the relaxation oscillator and variant in the TIO. The most distinctive benefits of the TIO architecture are the availability of both sinusoid and triangular waveforms, and its wide tuning range.

In addition to the disadvantages pointed out in Table 2.1, the quadrature relaxation oscillator presents the inconvenient that only square waves are available. Unfortunately, the application of interest (the phase shift technique based on vector projection) is effective only in sinusoidal signals. Thus, additional circuitry like resonators or bandpass filters must be employed with relaxation oscillators to have sine waves, which adds up complexity, noise and chip area.

On the other hand, the quadrature LC oscillator approach is not a good candidate for the application of interest since it has a narrow bandwidth. A wide tuning range is required by the application of interest aiming to a large bandwidth phase shifter. Thus, narrow bandwidth oscillators are not handy.

Table 2.1: Comparison among the quadrature coupling of first order oscillators.

Architecture	Advantages	Drawbacks
Quadrature relaxation oscillator	• Reduction in $\mathcal{L}(f_m)$ • Mixing function	• Quadrature errors • Power consumption
Quadrature LC oscillator	• Good $\mathcal{L}(f_m)$ • Good spectral purity • Mixing function	• Narrow bandwidth • Chip area • $\mathcal{L}(f_m)$ degradation
Two integrator oscillator	• Sinusoid and triangular waveforms • Wide tuning range • Very accurate quadrature • Mixing function	• Mismatches affect amplitude • $\mathcal{L}(f_m)$ depends on the circuit employed

2.5 Possibilities for Contribution

According to the study of quadrature oscillators in the previous section, the TIO is the approach which shows the more convenient characteristics for the application of interest. There is only one TIO reported in the literature [31]. This oscillator circuit possesses a large tuning range ($\approx$ a decade) at Gigahertz frequencies and a good $\mathcal{L}(f_m)$ ($\approx -100dB/Hz$). However, its tuneability is a nonlinear function of the tail current of the differential pairs which conform the circuit. Moreover, the output swing is rather narrow (a few mili volts). Thus, areas of opportunity for contribution regarding the known implementation of the TIO are: *linear tuneability control and a larger output swing.*

Another alternative to push the state-art in high frequency two-integrator oscillators is to synthesize a brand new circuit topology. Such new TIO may feature a voltage controlled quadrature oscillator instead a current controlled solution, a *cross-coupled* free circuit, and, perhaps, a waveform generator orientation, i.e. to produce waveforms other than sinusoids, like triangular, sawtooth and square waves.

It seems that by choosing the synthesis of a new TIO circuit, there is more room for contribution in the topic. Chapter 3, presents the proposed solutions.

Chapter 3

CMOS Two-Integrator Oscillator

3.1 The proposed Two-Integrator Oscillator

Based on the block diagram of a TIO depicted in Figure 2.11, which is compound of two integrators in cascade within a feedback loop, the schematic of Figure 3.1 has been devised. As can be appreciated, it consists of two transconductance based integrators in a fully differential fashion. The center frequency, f_0, is established by the values of capacitors C_{L1+}, C_{L1-}, C_{L2+} and C_{L2-} along with the transconductances gm_1 and gm_2. For simplicity, we will assume $C_{L1+} = C_{L1-}$ and $C_{L2+} = C_{L2-}$. By modifying the values of gm_1 and gm_2 f_0 can be tuned. Thus, the key for high frequency operation is to employ a broad bandwidth transconductor. A simple transconductor topology with a minimum number of internal nodes and consequently with a high frequency operation was proposed by Bram Nauta in [35]. Even though its major drawback of drawing transient currents from the power supply, which increases the potential of signal coupling between stages [36] as well as exhibiting a considerable power consumption at very high frequencies, with more than 300 citations, papers and patents included, the circuit has proved to be a very useful building block. The Nauta transconductor is the elementary unit used herein for the proposed TIO.

At glance, the Q-VCO in Figure 3.1 resembles a two-stages ring oscillator (TSRO). However, most of the reported TSROs make use of building blocks other than the

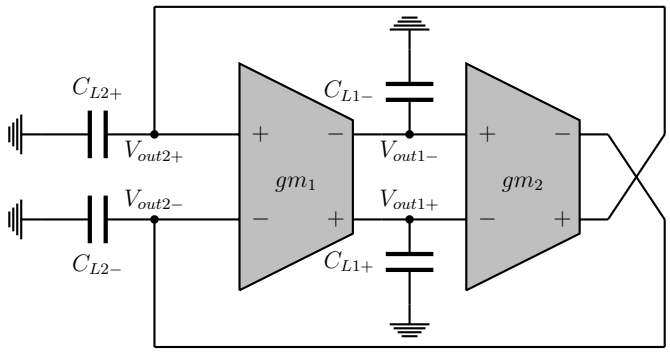


Figure 3.1: Schematic of the proposed Q-VCO.

Nauta transconductor, for instance, differential stages with cross coupled pairs [37] or composite loads [38], Maneatis delay cells [39]- [40], varactor based LC tanks [41]- [42], or simple inverter gates [43]- [44]. In addition, the pursuit of TSORs focuses mainly on a good performance in terms of tuning range and phase noise [45]. On the other hand, the purpose of this Thesis is to design a wide tuning range CMOS TIO with accurate quadrature waveforms at high frequencies.

3.2 The Nauta Transconductor

Figure 3.2 shows the Nauta transconductor built up with CMOS devices. As can be appreciated, it consists of a fully-differential amplifier based on six inverter gates, i.e. six PMOS ($M_{P1,\ldots,P6}$) and six NMOS ($M_{N1,\ldots,N6}$) transistors. Since inverter gates are the key building block of the circuit, the design of the transconductor is performed as follows: a symmetrical threshold gate is desired, thus, depending on the threshold voltages of the CMOS devices, V_{THP} and V_{THN}, PMOS transistor must be three or more times larger than the NMOS transistor; in addition, since there is an equivalent RC circuit formed by the ohmic value of the devices and the capacitive load at the output of the gate, transistors must be sized such as the time constant is low enough to be capable of processing the fastest possible signal at the input port. The design equations are reduced to the following expressions:

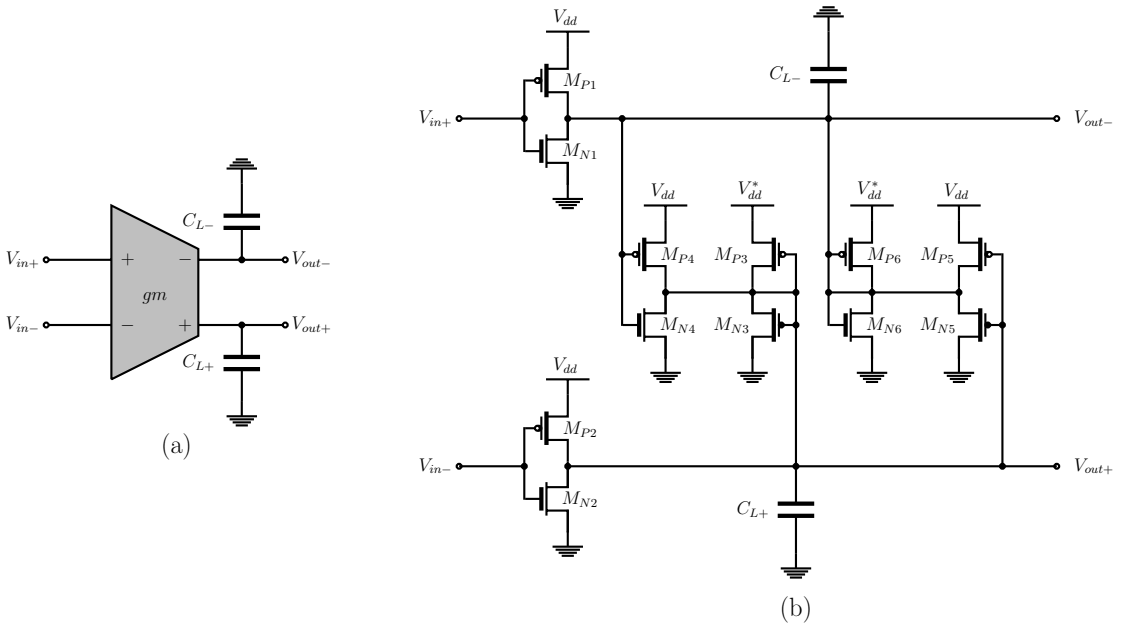


Figure 3.2: Fully differential Nauta transconductor: (a) symbol; (b) CMOS schematic.

$$\left(\frac{W}{L}\right)_{N1,\ldots,N2} = \frac{C_L V_{dd}}{\mu_n C_{OX}(V_{dd} - V_{THN})^2 t_{pHL}} \tag{3.1}$$

$$\left(\frac{W}{L}\right)_{P1,\ldots,P6} = \frac{C_L V_{dd}}{\mu_p C_{OX}(-V_{dd} - |V_{THP}|)^2 t_{pLH}} \tag{3.2}$$

where V_{dd} is the bias voltage; C_L is the effective output capacitance of the inverter gate; C_{OX} is the oxide capacitance of the MOS technology; μ_n is the mobility of the electrons and μ_p the mobility of the holes; $\left(\frac{W}{L}\right)_{P1,\ldots,P6}$ and $\left(\frac{W}{L}\right)_{N1,\ldots,N6}$ are the aspect ratio of PMOS and NMOS devices, respectively, whereas V_{THP} and V_{THN} are their corresponding threshold voltages; t_{pLH} and t_{pHL} are the propagation delays of the inverter gate [46], these must be chosen such as their value are a small fraction of the period of the fastest signal which is intended to be processed.

Table 3.1 highlights the most salient features of the Nauta transconductor [47]. Important parameters such as low frequency gain, quality factor (for filtering purposes), noise factor, distortion, signal swing available, dissipation and frequency limitations are listed. Design trade-offs among all of them are discussed deeply in [47].

Table 3.1: Transconductor properties.

Parameter	**Expression**
Transconductance	$g_m = (V_{dd} - V_{THN} + V_{THP})\sqrt{K_N K_P}$
Small-signal DC-gain	$A_0 = \frac{g_{md}}{\delta g_m}$
Quallity factor	$\frac{1}{Q_{int}(\omega_T)} = \frac{\delta g_m}{g_{md}}$
Noise factor	$F = C_{inv}\frac{g_{mi}}{g_{md}} > 4C_{inv}$
Distortion	$\frac{C_3}{C_1} \approx -\frac{\theta_n + \theta_p}{8(V_{dd} - V_{THN} + V_{THP})}$
Maximal signal	$V_{max} \sim \sqrt{\frac{8(V_{dd} - V_{THN} + V_{THP})}{\theta_n + \theta_p}}$
Dissipation per g_m	$\frac{3}{4}(V_{dd} - V_{THN} + V_{THP})V_{dd}$
Maximal resonance frequency	$\omega_{max} \approx \frac{\mu_n}{8L_n^2}(V_{dd} - V_{THN} + V_{THP})$

Table 3.2: Design detail of the Nauta transconductor.

Transistor	**Aspect ratio (W/L)**
$M_{N1}, M_{N2}, M_{N3}, M_{N4}, M_{N5}, M_{N6}$	$45\mu m/0.18\mu m$
$M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_{P5}, M_{P6}$	$135\mu m/0.18\mu m$

Table 3.3: Performance characteristics of the designed Nauta transconductor.

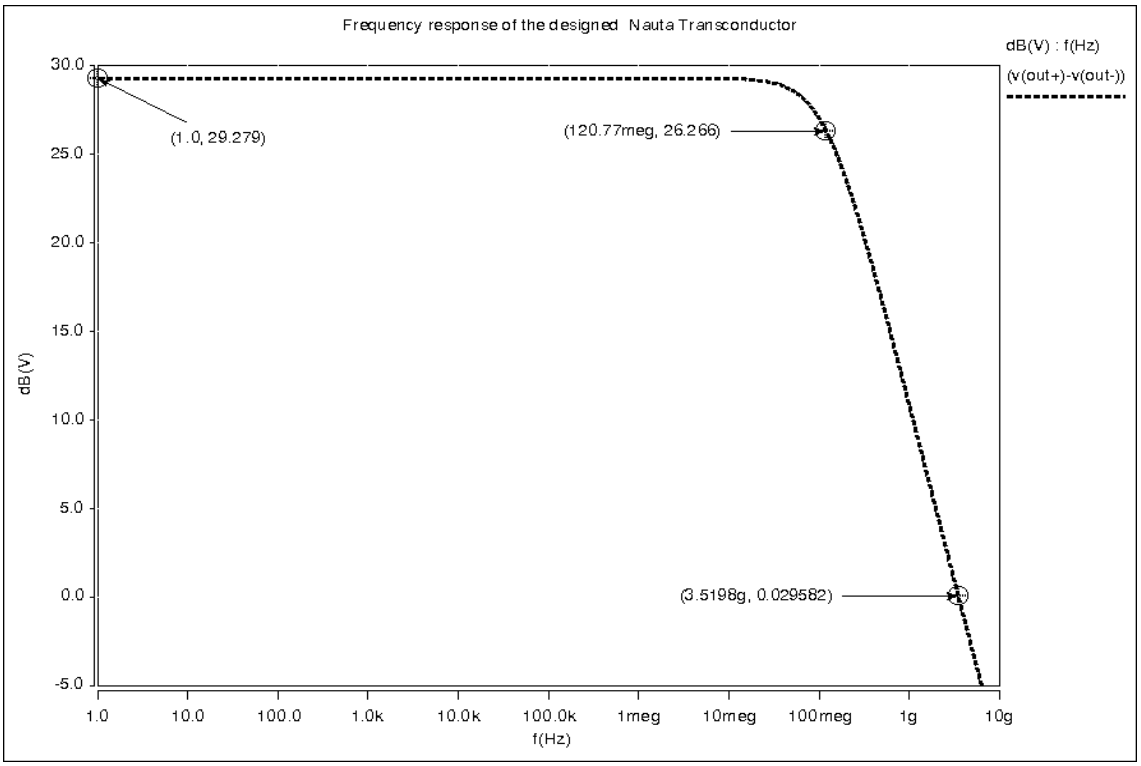
Parameter	**Value**
Supply voltage	1.8V
Power consumption	$\approx 56mW$
DC gain	$\approx 29dB$
BW @ $C_L = 0.3pF$	$124.4MHz$
GBW @ $C_L = 0.3pF$	$3.5GHz$
CMRR	$35.2dB$
Output swing	1.27Vpp ($\approx 70\%V_{dd}$)
Slew-rate +, Slew-rate -	365.44KV/sec, 287.27KV/sec
Settling time	$1\mu sec$
PSRR @ DC, 100MHz	35dB
Input common mode voltage	900mV

By means of equations (3.1) and (3.2) and considering a frequency of operation around the 3.5GHz, the sizes of the devices of the transconductor in Table 3.2 were determined. Parameters of the CMOS/mixed-mode/RF 0.18μm technology from UMC foundry were employed. An output capacitance, C_L, of 300fF was considered. This value was estimated taking into account parasitic self load of the transconductor.

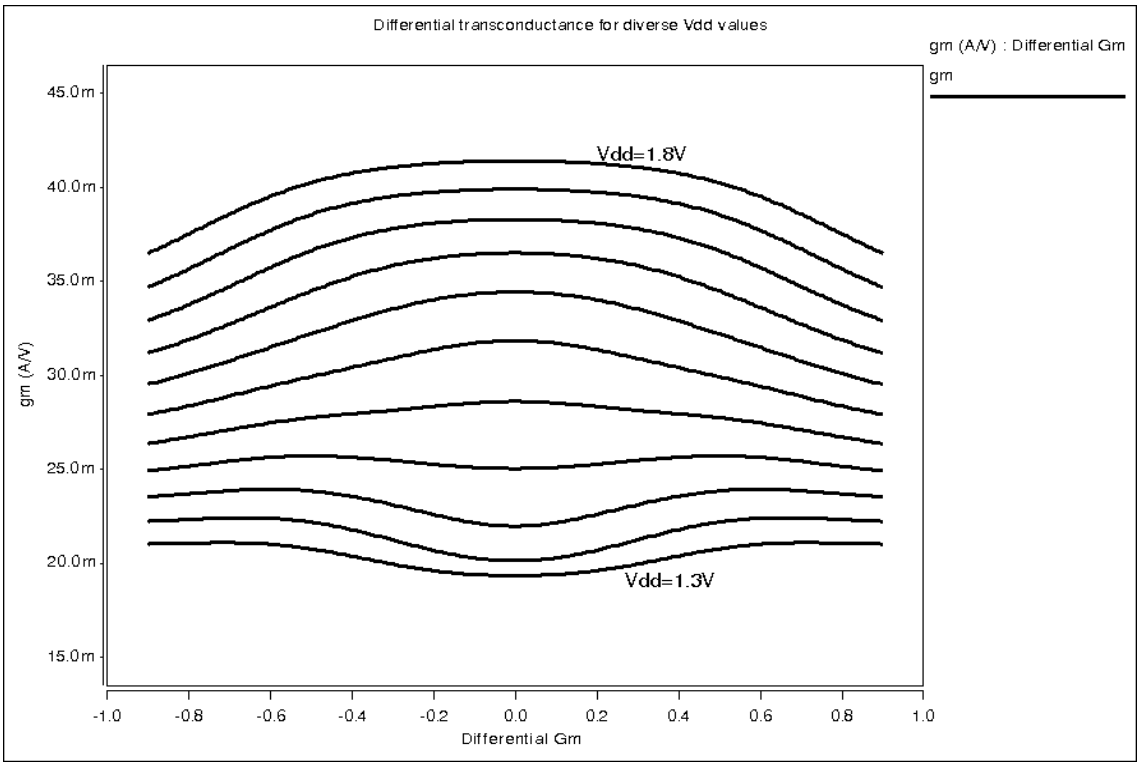
Finally, Table 3.3 shows some of the most important characteristics of the designed Nauta transconductor. Those are simulated results obtained in *Mentor Graphics® IC studio 2008.2b*. As can be seen, there is a good trade-off between GBW and DC-gain. Unfortunately, power consumption is large due to the nature of the circuit to draw transient currents from the power supply in combination with the fact that the aspect ratio, (W/L), of the involved transistors is large to exhibit high frequency operation. Figure 3.3 (a) shows the magnitude response of the transconductor versus frequency whereas Figure 3.3 (b) depicts the transconductance of the circuits for diverse V_{dd} values. It can be appreciated that for one third variation of the highest V_{dd} value (1.8V) an approximate of 20mA/V transconductance tuning is achieved. With both, the high frequency benefits and the transconductance tuning capability exhibited by the circuit, a wide tuning range TIO at high frequency is expected.

3.3 CMOS Quadrature Voltage Controlled Two Integrator Oscillator

Figure 3.4 depicts the schematic of the Quadrature Voltage Controlled Two-Integrator Oscillator (Q-VCTIO) with CMOS devices. Since the Nauta transconductor designed in the previous section is the key building block of the oscillator, it is quite straight forward assembling the Q-VCTIO by cascading two of these transconductors within a feedback loop as indicated in Figure 3.1. There are two output ports in the circuit given by the output differential voltages $(V_{out1+} - V_{out1-})$ and $(V_{out2+} - V_{out2-})$, who are in quadrature with respect each other. The capacitance values C_{L1+}, C_{L1-}, C_{L2+} and C_{L2-} are parasitic self-loads of the transconductor. The tuning of the oscillation



(a)



(b)

Figure 3.3: (a) Frequency response (magnitude) of the designed Nauta transconductor and (b) Transconductance versus differential input voltage for diverse Vdd values.

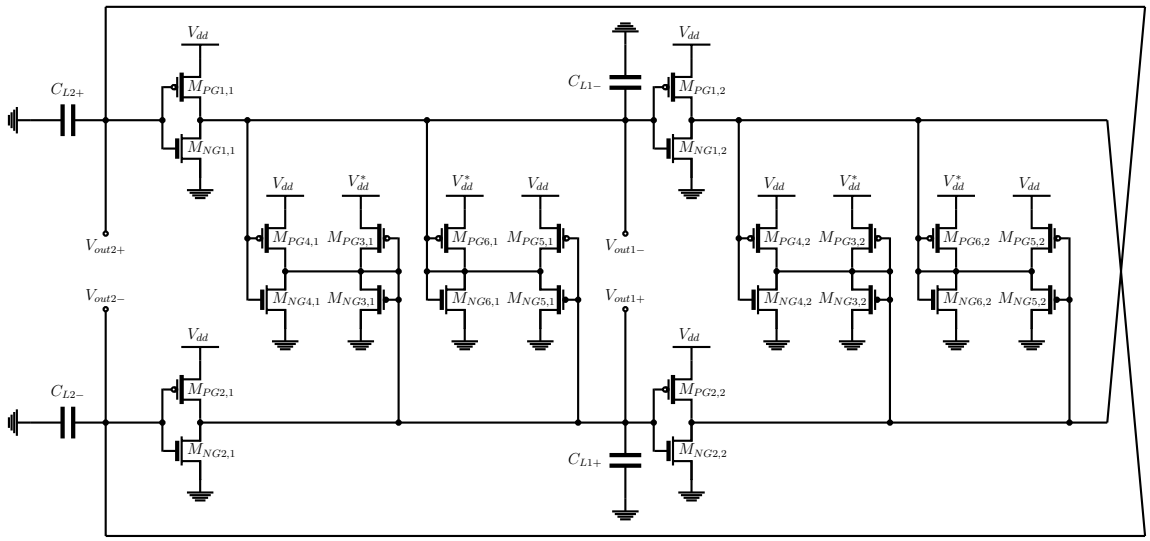


Figure 3.4: Proposed CMOS Q-VCTIO.

frequency, f_0, is performed by means of V^*_{dd}.

The design of the Q-VCTIO was made with the CMOS/mixed-mode/RF 0.18μm technology from UMC foundry. Figure 3.5 shows the layout realized in *Mentor Graphics® IC studio 2008.2b*. Characterization of the oscillator was also performed in the same program, Table 3.4 summarizes the most noticeable aspects of the proposed Q-VCTIO and a comparison with some other quadrature oscillators in CMOS 0.18μm technology reported in diverse journals. Some of the performance parameters are not possible to compare since these are not reported in the examined papers, such is the case of the output voltage swing and the total harmonic distortion (THD). For the proposed circuit, the average voltage swing obtained between the output ports was 67% of $2V_{dd}$, which is the largest possible swing in case of rail-to-rail operation. 67% corresponds to $\approx 2.4Vpp$, which is a good number considering that the bias is 1.8V, which by the way, is among the largest values of voltage supply employed for biasing the circuit. On the other hand, the purity of the sinusoids at the output is given by the THD. A 3% THD value may be on the limit of harmonic voltage allowed but that depends on the system where the oscillator is going to be employed. However, considering the fact that inductors are not present in the circuit and, consequently, the quality factor of the oscillator is not high, 3% THD is acceptable.

Table 3.4: Comparison among the proposed TIO and diverse reported Q-VCOs in $0.18\mu m$ CMOS technology.

Parameter	**This Work 2015**	Zhang [48] 2014	Li [49] 2013	Cheng [50] 2013	Xie [51] 2012	Lin [52] 2012	Atarodi [53] 2011	Lee [54] 2010	Jang [55] 2010	Zhang [56] 2009	Mazzanti [57] 2006
CMOS Technology	**0.18μm**	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm
Area [mm^2]	**0.0024**	NR	0.32	NR	NR	0.45	0.25	0.938	0.7968	0.252	0.6
Supply Voltage[V]	**1.8**	1.2	1.3	1.5	1.5	1.8	1.8	1.0	1.45	1.8	NR
Power Consumption [mW]	**104.35**	3.6	3.5	0.75	3	10.8	7	4.9	8.7	7.2	18
$F_{center}[GHz]$	**2.445**	2.7	2.2	0.488	2.455	16.28	2.5	2.345	5.08	2.0145	1.86
$BW[MHz]$	**570**	470	352	97.6	450	288	200	350	280	397	316.2
$K_{VCO}[MHz/V]$	**712.5**	NR	NR	NR	321.4	262	NR	350	280	220	NR
$FTR[\%]$	**23.3**	17.4	16	20	14	1.77	8	15	5.5	19.7	17
P. Noise [dBc/Hz] @ 1MHZ	**-115**	-126.8	-114.1	-118	-126	-125	-136*	-126.11	-124.58	-112.25	-119*
Voltage Swing [V]	**2.4**	NR	NR	NR	NR	NR	2.0	NR	1.0	NR	0.5
THD [%]	**3**	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR
$FOM_{PN}[dB]$	**160.6**	190	NR	173	189	184	186	186	189.42	170.4	185
$FOM_{PN+FTR}[dB]$	**167.9**	NR	NR	179	NR	199	NR	NR	NR	NR	NR
Phase error [Degrees]	**0.008**	0.5	NR	0.3	0.1	0.01	NR	< 6	0.65	< 5	0.6

NR=No reported, *@3MHz

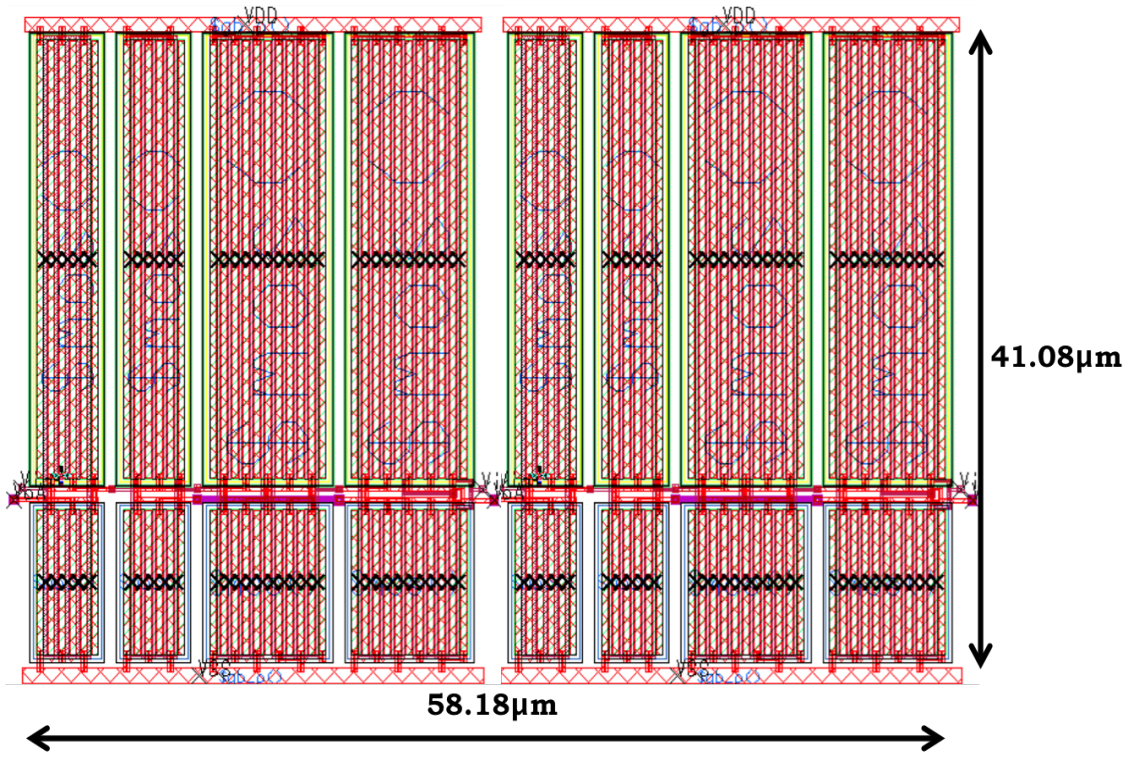


Figure 3.5: Layout in the CMOS/mixed-mode/RF 0.18μm technology from UMC foundry of the designed Q-VCTIO.

There are some drawbacks of the proposed Q-VCTIO when compared to the other proposals: it is power hungry as expected since power consumption of the Nauta transconductor is high; the phase noise is not as low as in the other oscillators, which was anticipated in chapter 2; and both Figures of Merit, FOM_{PN} and FOM_{PN+FTR}, are not the lowest neither. The suffixes PN and $PN + FTR$ refer to Phase Noise and Frequency Tuning Range, correspondingly. FOM_{PN} and FOM_{PN+FTR} are respectively given by [58]

$$FOM_{PN} = -\mathcal{L}\{f_m\} + 20log\left(\frac{F_{center}}{f_m}\right) - 10log\left(\frac{P_{DC}}{1mW}\right) \tag{3.3}$$

$$FOM_{PN+FTR} = FOM_{PN} + 20log\left(\frac{FTR}{10}\right) \tag{3.4}$$

where $\mathcal{L}(f_m)$ is the phase noise at the offset frequency (f_m), F_{center} is the center os-

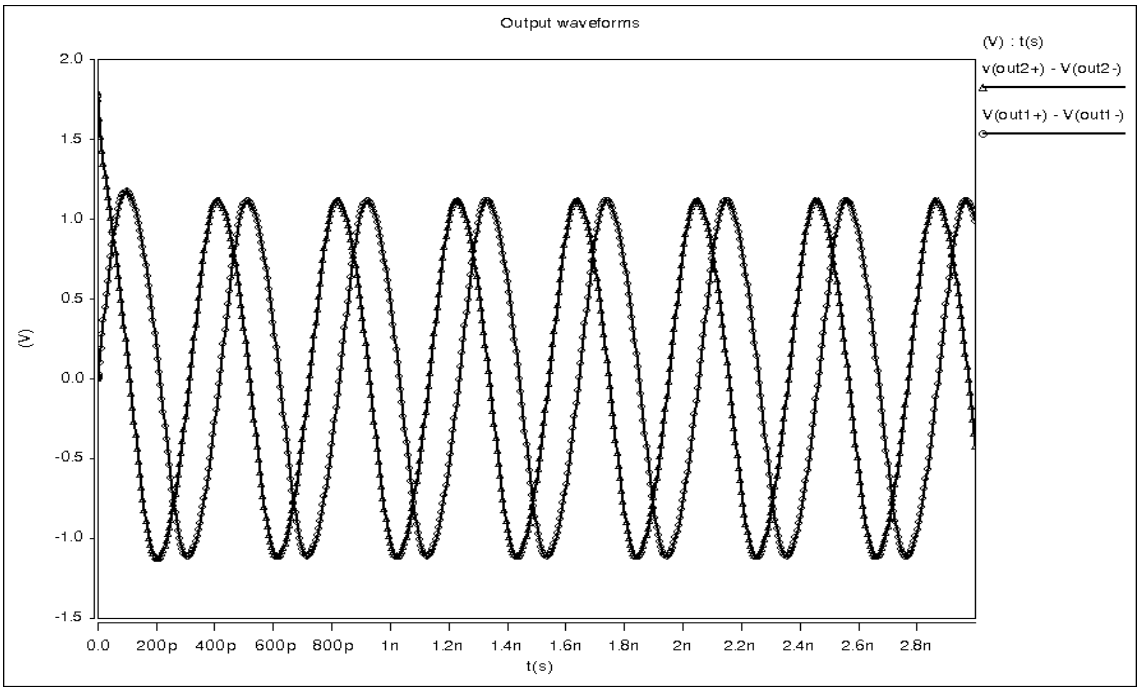


Figure 3.6: Output waveforms of the Q-VCTIO at 2.445GHz.

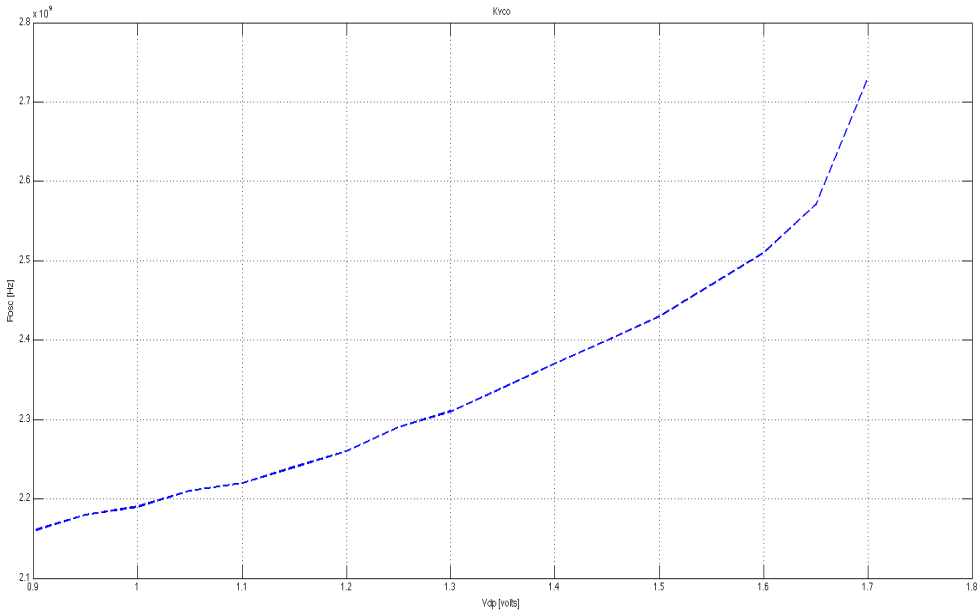


Figure 3.7: Kvco of the Q-VCTIO.

cillation frequency and P_{DC} is the power consumption of the circuit. Since $\mathcal{L}(f_m)$ is rather a low value and P_{DC} is high, the FOMs are damaged. Nevertheless, compact-

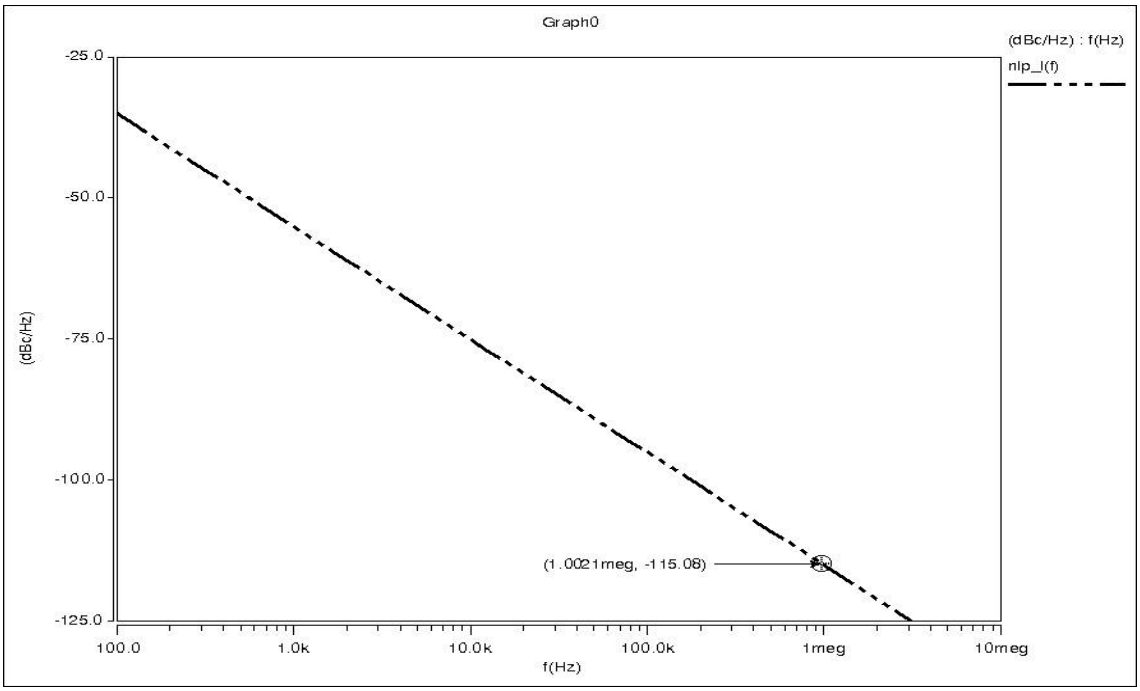


Figure 3.8: Phase noise of the Q-VCTIO @ 1MHz f_m.

ness (Area), bandwidth (BW), tuning constant (K_{VCO}), FTR and Phase error are the brightest characteristics of the proposed Q-VCTIO. This elements outline the oscillator for small-form-factor/high-quadrature-precision/wide-tuning-range applications, such as phase shifter circuits. In terms of F_{center} the oscillator is ranked in the middle compared to the other approaches.

Figure 3.6, depicts the output waveforms of the proposed Q-VCTIO at 2.445GHz. As can be seen, there is not delay time for having an steady output swing. On the other hand, Figure 3.7 details the K_{VCO} of the oscillator. It can be appreciated that K_{VCO} is a nonlinear function of the tuning voltage V_{dd}^{*}. Finally, the $\mathcal{L}(f_m)$ of the circuit is sketched in Figure 3.8 for an f_m=1MHz.

Chapter 4

A Q-VCTIO Based Wideband Phase Shifter Circuit

4.1 Phase Shifter Circuits

Phase shifter circuits have several applications in different systems such as phased array antennas [60], [61], radar applications [62], image rejection in low-IF receivers [63], PSK modulators/demodulators [19], phase correction in multiple clocking circuits in high-speed I/O applications [64], and distortion cancellation produced by non-linear circuits with a combination of multi-paths and polyphase signals [65], to name a few. The main function of a phase shifter is to produce at its output port a replica of the signal fed at its input port, but with a modified phase. Depending on the nature of the insertion phase, i.e., whether switchable continuously or in discrete steps, phase shifters are further classified into analog and digital, respectively [66], [67], [68]. There are two fundamental demands for phase shifters: to preserve a constant phase versus frequency and to exhibit a linear phase versus frequency.

In the RF area, the constant phase designs are typically implemented by means of switched networks, whereas the linear phase designs are predominantly synthesized using switched delay lines [63]. Another approach to the design of phase shifters in the analog domain is the use of polyphase (complex) filters, which produce nonsymmetric

gain responses with regard to the positive and negative frequencies [69], [70]. There are various procedures to implement complex filters, some of those include the Hilbert transform, which adds up a shift on the position of the poles and zeros of the transfer function of a real filter, and the employment of passive RC ladders with multiple inputs for realizing the complex coefficients of the transfer function in the linear network. The last, presents an important rotational symmetry property concerning to the rotation conversion of the input ports, and consequently, is referred as linear rotational symmetry (LRS) network. That symmetry property can be extended to active polyphase circuits [65]. Nevertheless, the phase shifts attained by such circuits are fixed multiples of a given phase value, and thus, even if the interconnection of the cascaded networks is changed, the range of possible shifts is bounded. This is inconvenient in applications where a wide phase shift range is required, e.g. the multipath polyphase linearization technique, where a large phase control range is necessary in order to provide a large linear control range [20].

Unfortunately, despite of the many available approaches for phase shifters, there is a lack of architectures which exhibit a wideband with a broad range of phase control. In the present chapter, a solution that satisfies those features based on the use of the proposed Q-VCTIO is introduced.

4.2 Wide Range Phase Shifter Circuit Based on Vector Projection

Figure 4.1 depicts the projection in a plane, $\Re^2$, of vector **A** along vector β, with $\beta \neq \bigcirc$. The result of such projection is the vector $\alpha\beta$, where α is an scalar defined as the component of **A** along β [59]. It is possible to generate a vector perpendicularly orientated with respect to β, by subtracting **A** and $\alpha\beta$. As a result, A can be redefined as the sum of the linearly dependent vector $\alpha\beta$ plus the orthogonal vector **A-**$\alpha\beta$. If the magnitudes of the linearly dependent and the orthogonal vectors are chosen properly, then the resultant vector has the same magnitude of vector β but with a different

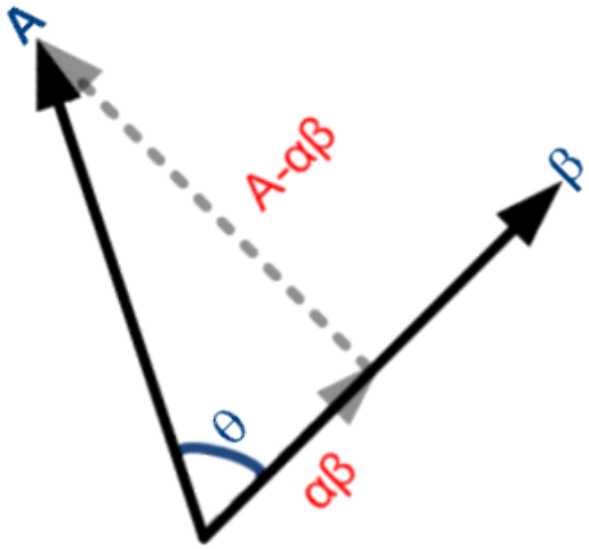


Figure 4.1: The projection of vector **A** along vector β.

orientation, i.e. β is virtually rotated. The angle, θ, of the rotated vector can be computed in terms of the magnitudes of the orthogonal and the linearly dependent vectors as

$$\theta = \arctan\left(\frac{\|A - \alpha\beta\|}{\|\alpha\beta\|}\right) \tag{4.1}$$

Note that owing to the fact that A_0 and αB_0 are amplitudes of signals with either polarity, positive (with an initial phase of 0 degrees) or negative (with an initial phase of 180 degrees), the argument of the arctangent function is not restricted to positive numbers. Thus, the range of the resultant phase mathematically lies within $-90 < \theta < 90$. However, because of the polarity property of the cosine signal and its orthogonal sine, the phase shift achieved covers almost entirely a period, i.e. 360 degrees. Thus, if both signals have a positive polarity, the phase shift lies within $0 \leq \theta < 90$; nevertheless, if αB_0 has a negative polarity and A_0 a positive one, then the phase shift lies within $90 < \theta < 180$; on the other hand, if both signals have a negative polarity, the phase shift lies within $180 < \theta < 270$; but if A_0 has a negative polarity whereas the polarity of αB_0 is positive, then the phase shift lies within $270 < \theta < 360$. In this way, the phase shift can be expressed as

$$\theta = \begin{cases} \arctan\left(\dfrac{A_0}{\alpha B_0}\right) & \text{if } \varphi_A = 0^o, \varphi_B = 0^o \\ 180 - \arctan\left(\dfrac{A_0}{\alpha B_0}\right) & \text{if } \varphi_A = 0^o, \varphi_B = 180^o \\ 180 + \arctan\left(\dfrac{A_0}{\alpha B_0}\right) & \text{if } \varphi_A = 180^o, \varphi_B = 180^o \\ 360 - \arctan\left(\dfrac{A_0}{\alpha B_0}\right) & \text{if } \varphi_A = 180^o, \varphi_B = 0^o \end{cases}$$

where φ_A and φ_B are the initial phases of the sine and cosine waveforms, respectively.

Therefore, the insertion phase for a single-tone signal can be done by adding to the waveform previously modified in amplitude and polarity, its orthogonal counterpart, also modified in amplitude and polarity. A low-frequency prototype based on the vector projection technique has been reported in [22]. The presented results demonstrate the feasibility of the technique for generating phase shifts. However, the problems with the circuit employed in [22] are: the orthogonalizer block, built up with a first order all-pass network, exhibits a very narrow bandwidth; the fact that the circuit was realized with low frequency elements such as op amps. Thus, the design of a wide tuning range phase shifter based on the vector projection approach at high frequencies needs to be addressed.

4.3 Digitally Controlled Programmable Phase Shifter Circuit

Figure 4.2 illustrates the proposal for insertion phase. Unlike the circuit in [22], the new topology differs from the original in the way in which quadrature is accomplished. The proposed circuit makes use of the quadrature Voltage-Controlled Two-Integrator Oscillator (Q-VCTIO) to produce quadrature signals in a wideband range at high frequencies. Since the input is a DC control signal that tunes the frequency of operation of the quadrature oscillations which are further programmatically attenuated by an 8-bit word to be subsequently added-up, the system may be considered a wideband high-frequency signal generator with programmable phase.

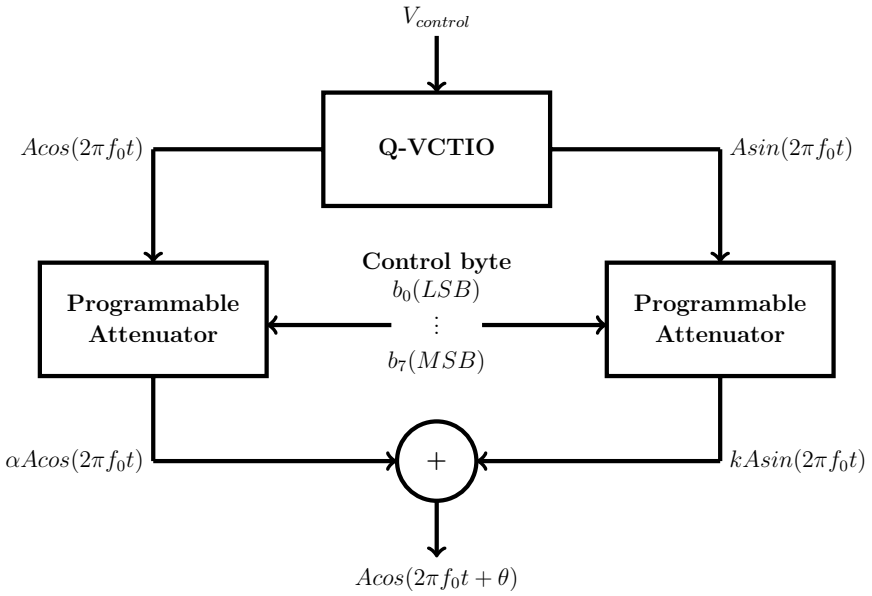


Figure 4.2: Block diagram of the proposed Q-VCTIO based Phase Shifter Circuit.

Figure 4.3 depicts the schematic of the proposed CMOS Q-VCTIO based Phase Shifter Circuit. Relating Figures 4.2 and 4.3, it can be seen that the programmable attenuation is done by means of $R-2R$ networks which in turn are driven by analog multiplexers built-up with transmission and inverter gates. The attenuation factors, α and k, are given by

$$\alpha, k = \sum_{i=0}^{N-1} S_i 2^{i-N} \tag{4.2}$$

where S_i is the *i-th* switch in the $R-2R$ ladder whose logic value is "0" or "1" in function of the interconnection of the switch to either ground or the corresponding $2R$ resistor, respectively. N is the number of bits (NOB) employed for controlling the attenuation. An $N = 8$ is proposed, from those half a byte is for attenuating the Q signal and the other half the I signal. By doing this, an effective attenuation factor between 0.0625 and 0.9375 with non-monotonic steps is achieved. The output signals from the $R-2R$ ladders are in current mode.

The addition of the attenuated signals from the $R-2R$ ladders is done by means of the flipped voltage followers compound by devices $M_{N1}, M_{N2}, \ldots M_{N6}$. The flipped volt-

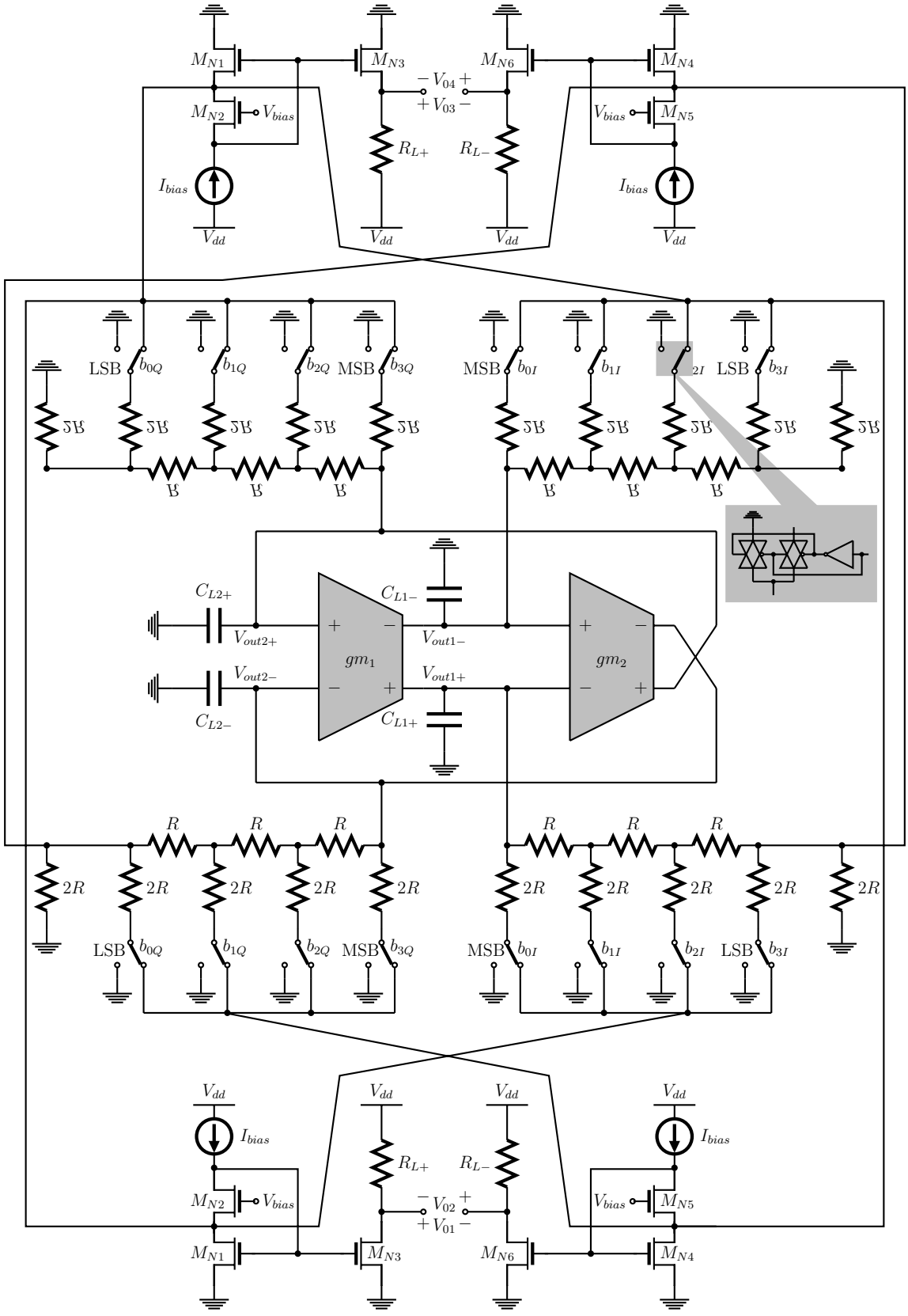


Figure 4.3: Schematic of the proposed Q-VCTIO based Phase Shifter Circuit.

Table 4.1: Design detail of the proposed Phase shifter circuit.

Q-VCTIO	
Transistor	**Aspect ratio (W/L)**
$M_{N1}, M_{N2}, M_{N3}, M_{N4}, M_{N5}, M_{N6}$	$45\mu m/0.18\mu m$
$M_{P1}, M_{P2}, M_{P3}, M_{P4}, M_{P5}, M_{P6}$	$135\mu m/0.18\mu m$
$R-2R$ **ladder**	
R	$100K\Omega$
$2R$	$200K\Omega$
Transmission gates	
Transistor	**Aspect ratio (W/L)**
M_{NT}, M_{NI}, M_{PT}	$4.86\mu m/0.18\mu m$
M_{PI}	$14.58\mu m/0.18\mu m$
Flipped voltage follower	
$M_{N1}, M_{N3}, M_{N4}, M_{N6}$	$169.74\mu m/0.18\mu m$
M_{N2}, M_{N5}	$174.6\mu m/0.18\mu m$

age follower blocks are employed since a low-impedance node is available between the source terminal of transistor $M_{N2}(M_{N5})$ and the drain terminal of transistor $M_{N1}(M_{N4})$, which favors the sink of external currents with very few modification of the output impedance of the sources from which the currents are delivered [84]. Finally, once the currents have been added-up these are mirrored and converted once more to voltage-mode signals to produce the differential outputs V_{01}, V_{02}, V_{03} and V_{04}. These correspond to the phase shifted signals in the first (1-90^o), second (91-180^o), third (181-270^o) and fourth (271-360^o) quadrants of the I/Q plane, respectively.

Table 4.1. shows the design details of the phase shifter circuit of Figure 4.3. The aspect of ratio of the transistors of the Q-VCTIO were already disclosed in the previous chapter. These sizes were obtained with the design procedure in [47]. The value of the resistors of the $R-2R$ network were chosen trying to keep a balance among noise, the load seen by the transconductors of the Q-VCTIO and area. On one hand, the load seen by the transconductors must be the highest possible since, theoretically, the Nauta transconductor has an infinite differential output impedance. On the other hand,

noise and area increase conforming the value of R rises. Again, the transmission gates were sized trying to maintain a good trade-off between compactness and a low resistive value. This is easy since the $2R$ value is relatively large and in a series connection with the resistive value of the switch it prevails. Moreover, the transmission gates does not operate dynamically and, consequently, there is not a processing rate that imposes large sizes for the switches. Finally, even though the flipped voltage follower is typically a low-frequency building block, it has been also employed for realizing RF circuitry [85]. Herein, the design was focused on preserving the low impedance node (a few Ω) between the source terminal of transistor $M_{N2}(M_{N5})$ and the drain terminal of transistor $M_{N1}(M_{N4})$.

4.4 Simulation results

The simulation of the Q-VCTIO based phase shifter was done with *Mentor Graphics® IC studio 2008.2b*. Table 4.2 summarizes the most remarkable aspects of the proposed phase shifter circuit and a comparison with some other analogous in CMOS technology. Power consumption is difficult to compare since there is only a few papers who reported it. However, compared to those references, the suggested architecture is one of the most power hungry. In terms of frequency range, the designed circuit has a bandwidth of 370MHz ranging from 2.12GHz to 2.49GHz. In contrast with the other approaches, the frequency of operation is one the smallest, but the bandwidth is in a medium term. The best features of the proposed solution are its large phase range and its small phase error. The latter is an important characteristics if high precision is required.

It is important to mention that the 328^o phase range is covered with 140 phase steps controlled digitally by the 8-bit word, i.e. the proposed solution has $\sim 0.6^o$ phase shift step. For each quadrant in the I/Q plane, there is 82^o of effective phase shift. Thus, in the first quadrant the phase shift goes from 4^o to 86^o, in the second from 94^o to 176^o, in the third from 184^o to 276^o, and in the fourth from 274^o to 354^o. There are some reported works [81–83] where the phase shifts are accomplished as follows:

Table 4.2: Comparison among the proposed Q-VCTIO based phase shifter circuit and diverse reported phase shifters in CMOS technology.

Parameter	**This Work 2015**	Tal [71] 2011	Sheng [72] 2012	Domenico [73] 2015	Jinbo [74] 2015	Garakoui [75] 2015	Sang [76] 2015	Mehdi [77] 2015	Meng [78] 2015	Lee [79] 2015	Dongho [80] 2015
CMOS Tech. [nm]	**180**	45	180	28	65	140	65	180	65	65	130
Power Supply [V]	**1.8**	1.2	1.8	NR	1.2	1.5	NR	1.2	NR	0.4	NR
P. Consumption [mW]	**230**	13	NR	NR	NR	250	NR	0	NR	NR	NR
Freq. Range [GHz]	**2.12-2.49**	24	60	60	9-10.75	1-2.5	60	24	57-64	75-85	13
Phase range [Degrees]	**328**	62	270	155	115	180	90	185	315	90	90
Phase error [Degrees]	**1.4°**	NR	NR	6°	NR	1.8°	<6.5°	NR	7.8°	7.2°	NR

NR=No reported

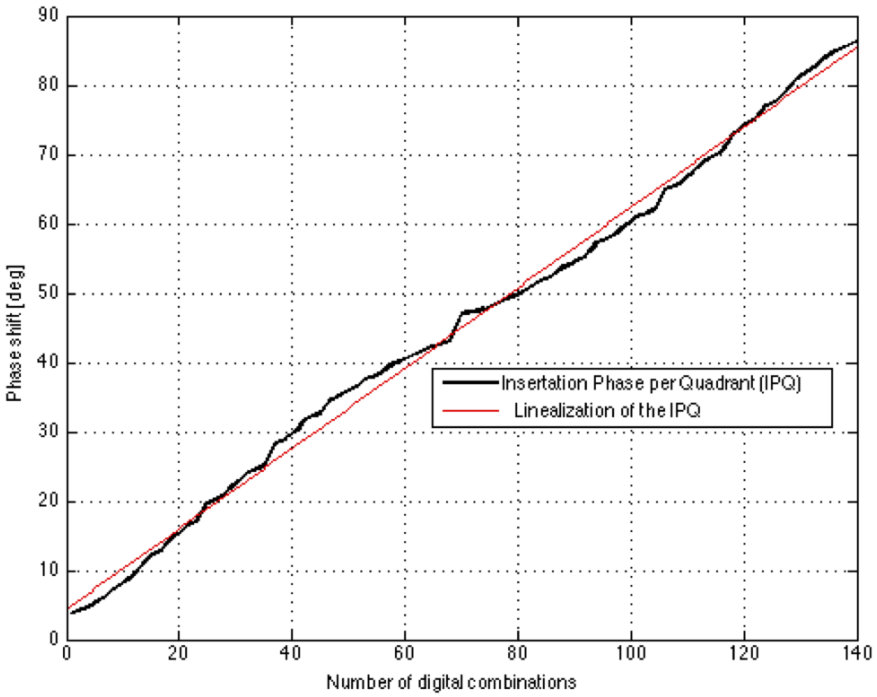


Figure 4.4: Insertion phase per quadrant of the proposed phase shifter as a function of the number of digital combinations.

within a certain bandwidth a fixed phase shift is realized by vector-sum and then by a digital control the phase shift is step-down or step-up. In this way, a reduced set of phase shifts with coarse phase step is achieved. On the other hand, with the proposed solution, a better resolution is reached due to the two-degree-of-freedom incorporated to the circuit, i.e. a DC voltage for tuning the frequency and a digital control to produce the phase shift. An 8-bit control is recommended for fine phase shift steps. Increasing the number the of bits beyond does not reduce significantly the phase shift step. For coarse shift steps, a reduced number of bits, till 4, is better.

Figure 4.4 shows, in black, the insertion phase per quadrant of the proposed phase shifter as a function of the number of digital combinations. In red, a linearized version is depicted. As can be appreciated, they are quite similar. Thus, we can conclude that the phase step of the proposed phase shifter is quasi-linear.

Figure 4.5 shows some of the different phase shifts attained by the suggested archi-

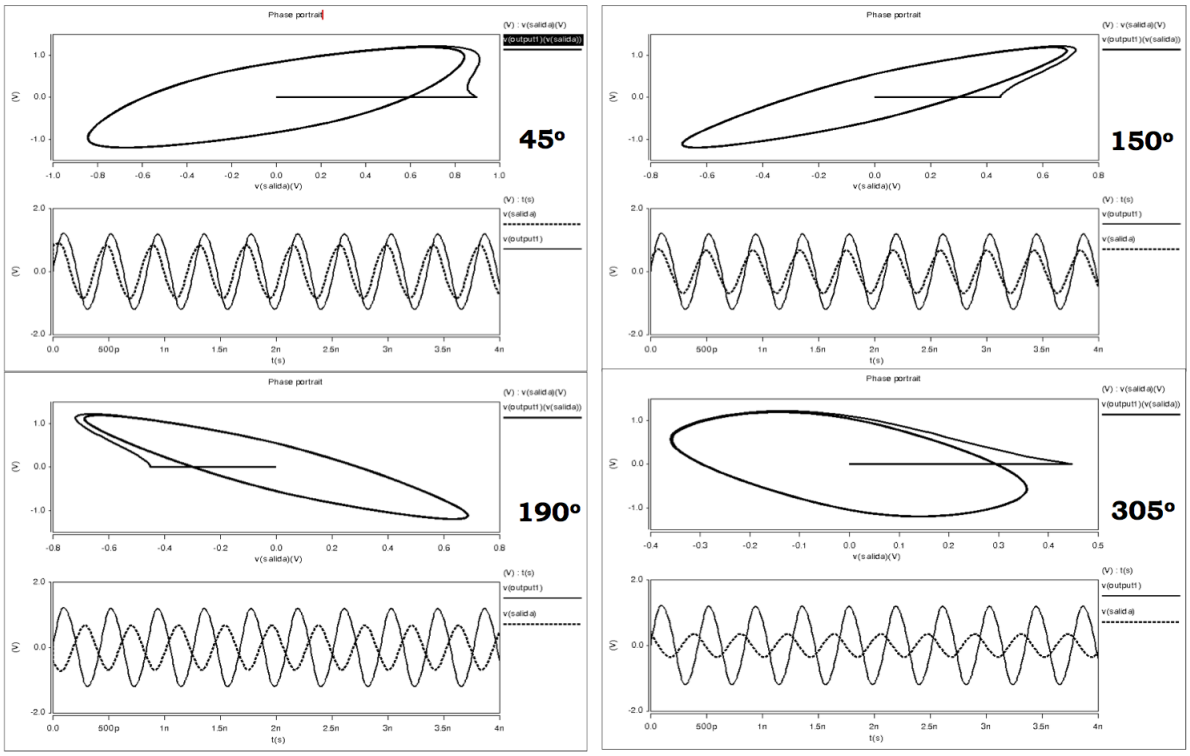


Figure 4.5: Different phase shifts in the four quadrants of the I/Q plane.

tecture at 2.305GHz. It can be seen that the resultant output swing varies depending on the phase shift. However, the smallest swing is around 300mV.

Finally, some important tasks are left to do before coming to a realization and characterization of a prototype of the proposed CMOS phase shifter circuit. For instance, post-layout simulation of the complete phase shifter circuit to assess in a more complete way its functionality and process corners characterization to evaluate how PVT variations affects the proposed circuit and, if necessary, compensate them. These and other activities are part of the future work, which will be described in the next chapter.

Chapter 5

Conclusion

5.1 Summary and Conclusions

Many electronics and telecommunication systems have benefited from the quadrature processing. On-chip high frequency profitable phase shifters can be realized with quadrature signals if these are combined for producing insertion phase with CMOS circuits. Some CMOS phase shifters have been reported in the literature. However, only a few present a good trade-off among frequency of operation, bandwidth and phase range. In this Thesis, the synthesis and design of a CMOS phase shifter solution with 370MHz bandwidth ranging from 2.12GHz to 2.49GHz is proposed. Phase shifts within an extent of $\sim 82^o$ per quadrant in 140 phase steps controlled by an 8-bit word are exhibited by the suggested solution. However, the circuit has a high power consumption which makes it impractical for battery-biased applications. Yet, for those systems where power consumption is not an issue, the recommended circuit still is an option.

5.2 Original contributions

The original contributions derived from the Thesis include:

- An alternative for achieving wide range phase shifter circuits has been proposed

with the combination of the vector projection approach and the use of quadrature voltage controlled oscillators.

- A compact ($0.0024mm^2$), cross-coupled pair free, Q-VCTIO based on the Nauta transconductor with very low phase error (0.008^o), large output swing (2.4Vpp), large frequency tuning range ($FTR = 23.3\%$) and large gain ($K_{VCO} = 712.15MHz/V$) has been introduced.

- The synthesis and design in CMOS technology of a digitally programmable wide tuning range (370MHz) phase shifter circuit aiming at high-frequency operation (2.12GHz-to-2.39GHz) has been presented.

5.3 Future work

Future work involves two categories:

Near future work

- Post-layout simulation of the complete phase shifter circuit to assess in a more complete way its functionality.

- Process corners characterization to evaluate how PVT variations affects the proposed circuit and, if necessary, compensate them.

- Fabrication and characterization of a prototype.

Medium-term future work

- Debugging of the proposed Q-VCTIO by focusing in alleviating the power consumption.

- To extend the functionality of the proposed Q-VCTIO to present its inherent both linear and quasi-linear behavior.

- To explore the possibility of broadening the tuning range of the proposed Q-VCTIO.

- To verify the chance of insertion phase in waveforms other than sinusoidal signals.

5.4 Recommendations

Some recommendations for a proper use of the proposed phase shifter circuit are listed below:

- If power consumption matters, then it is not recommended to use the proposed solution since it is power hungry.
- An 8-bit control is recommended for fine phase shift steps. Increasing the number the of bits beyond does not reduce significantly the phase shift step. On the other hand, for coarse shift steps, it is recommended to reduce the number of bits till 4.
- The proposed phase shifter only works for sinusoidal signals. If a different waveform needs to be shifted in the time-domain, then it is recommended to use true time delay cells instead.

Bibliography

[1] Mak, P.-I.; U, S.-P.; Martins, R.P., "Transceiver architecture selection: Review, state-of-the-art survey and case study", *IEEE Circuits and Systems Magazine*, vol.7, no.2, pp.6,25, Second Quarter 2007.

[2] Luis B. Oliveira, Jorge R. Fernandez, Igor M. Filanovsky and Chris J.M. Verhoeven, "Analysis and Design of Quadrature Oscillators", 1st ed., Springer, 2008, ch. 1, pp. 1-5.

[3] B. Razavi, "RF Microelectronics", 2nd ed., Prentice Hall, 2008, ch. 4, pp. 155-214.

[4] R. Lyons, "Understanding Digital Signal Processing", 2nd ed. P. Hall, 2004, ch. 8, pp. 335-360.

[5] Martin Kenneth, "Complex Signal Processing is Not Complex", *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 51, NO. 9, pp. 1823-25, Jun. 2007.

[6] Coleman, J.O., "Signals and Systems II Part I: Signals and their representations," Potentials, IEEE , vol.29, no.1, pp.41,45, Jan.-Feb. 2010.

[7] Coleman, J.O., "Signals and Systems II: Part II: Interpolation, decimation, complex signals, and Nyquist signaling," Potentials, IEEE , vol.29, no.2, pp.40,45, March-April 2010.

[8] Coleman, J.O., "Signals and systems II-Part III: Analytic signals and QAM data transmission," Potentials, IEEE , vol.29, no.3, pp.40,44, May-June 2010.

[9] Coleman, J.O., "Signals and systems II-Part IV: DSP approaches to IQ modulation and demodulations," Potentials, IEEE , vol.29, no.4, pp.33,36, July-Aug. 2010.

[10] Coleman, J.O., "Signals and Systems II Part V: Frequency conversion," Potentials, IEEE , vol.29, no.5, pp.41,44, Sept.-Oct. 2010.

[11] Coleman, J.O., "Signals and Systems II Part VI: Vestigial-sideband modulation and nonintegral rate changes," Potentials, IEEE , vol.29, no.6, pp.33,38, Nov.-Dec. 2010.

[12] Keping Wang; Zhigong Wang; Xuemei Lei; Xiang Cao; Peng Han; Geliang Yang; Kaixue Ma; Kiat Seng Yeo "A Low-Loss Image-Reject Mixer Using Source Follower Isolation Method for DRM/DAB Tuner Applications", Circuits and Systems II: Express Briefs, IEEE Transactions on, On page(s): 729 - 733 Volume: 58, Issue: 11, Nov. 2011

[13] Laoudias, C.; Psychalinos, C. "1.5-V Complex Filters Using Current Mirrors", Circuits and Systems II: Express Briefs, IEEE Transactions on, On page(s): 575 - 579 Volume: 58, Issue: 9, Sept. 2011

[14] Frey, D. "Synchronous filtering", Circuits and Systems I: Regular Papers, IEEE Transactions on, On page(s): 1772 - 1782 Volume: 53, Issue: 8, Aug. 2006

[15] Ni, R.; Mayaram, K.; Fiez, T.S. "A 2.4 GHz Hybrid Polyphase Filter Based BFSK Receiver With High Frequency Offset Tolerance for Wireless Sensor Networks", Solid-State Circuits, IEEE Journal of, On page(s): 1250 - 1263 Volume: 48, Issue: 5, May 2013

[16] Golestan, S.; Monfared, M.; Freijedo, F.D. "Design-Oriented Study of Advanced Synchronous Reference Frame Phase-Locked Loops", Power Electronics, IEEE Transactions on, On page(s): 765 - 778 Volume: 28, Issue: 2, Feb. 2013

[17] Hunter, M.T.; Mikhael, W.B.; Tocco, T.J. "Arbitrary Waveform Generators for synthetic instrumentation", AUTOTESTCON, 2008 IEEE, On page(s): 138 - 143

[18] Soer, M.C.M.; Klumperink, E.A.M.; Nauta, B.; van Vliet, F.E., "A 1.0-to-4.0GHz 65nm CMOS four-element beamforming receiver using a switched-capacitor vector modulator with approximate sine weighting via charge redistribution," IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC) 2011, pp.64,66, 20-24 Feb. 2011

[19] F. Xiong, "Digital Modulation Techniques", 2nd ed., Artech House, 2006, ch 4, pp. 135-205.

[20] Subhan, S.; Klumperink, E.A.M.; Nauta, B., "Towards suppression of all harmonics in a polyphase multipath transmitter," IEEE International Symposium on Circuits and Systems (ISCAS), 2011, pp.2185,2188, 15-18 May 2011.

[21] Garakoui, S.K.; Klumperink, E.A.M.; Nauta, B.; Van Vliet, F.F.E., "A 1-to-2.5GHz phased-array IC based on gm-RC all-pass time-delay cells," Digest of Technical Papers of the IEEE International Solid-State Circuits Conference (ISSCC), 2012, pp.80,82, 19-23 Feb. 2012

[22] Luis A. Sánchez Gaspariano et. al., "An 8-Bit Digitally Controlled Programmable Phase Shifter Circuit for Sinusoidal Signals with 252? Phase Control Range", Springer journal of Circuits, Systems and Signal Processing, vol. 32, issue 2, pp. 415-431, April 2013.

[23] Johan van der Tang, Dieter Kasperkovitz, Arthur van Roermund, "High-Frequency Oscillator Design for Integrated Transceivers", 1st ed., Springer, 2005, ch 3, pp. 37-64.

[24] Braud-Sudreau, Q. et. al., "SiGe Clock and Data Recovery System Based on Injection-Locked Oscillator for 100 Gbit/s Serial Data Link," IEEE Journal of Solid-State Circuits, vol.49, no.9, pp.1895-1904, Sept. 2014.

[25] Staszewski, R.B., "Digitally intensive wireless transceivers," IEEE Design & Test of Computers, vol.29, no.6, pp.7,18, Dec. 2012.

[26] Pamarti, S., "Digital techniques for integrated frequency synthesizers: A tutorial," IEEE Communications Magazine, vol.47, no.4, pp.126,133, April 2009.

[27] Azeredo-Leme, C., "Clock Jitter Effects on Sampling: A Tutorial," IEEE Circuits and Systems Magazine, vol.11, no.3, pp. 26-37, third quarter 2011.

[28] Luis B. Oliveira et. al., "Analysis and Design of Quadrature Oscillators", 1st ed., Springer, 2008, ch. 2, pp. 31-34.

[29] Luis B. Oliveira et. al., "A 5 GHz quadrature relaxation oscillator with mixing for improved testability or compact front-end implementation", John Wiley & Sons, International Journal of Circuit Theory and Applications, 38, April 2010, pp. 359-366.

[30] Luis B. Oliveira et. al., "Experimental comparison of phase-noise in cross-coupled RC - and LC - oscillators", John Wiley & Sons, International Journal of Circuit Theory and Applications, 38, April 2009, pp. 681-688.

[31] Luis B. Oliveira et. al., "An inductorless CMOS quadrature oscillator continuously tuneable from 3.1 to 10.6 GHz", John Wiley & Sons, International Journal of Circuit Theory and Applications, 40, April 2012, pp. 209-219.

[32] Christian J. M. Verhoeven, "First order oscillators", PhD Thesis, Delft University, 1985, ch. 2, pp. 3-19.

[33] Christian J. M. Verhoeven, "Coupled regenerative oscillator circuit", U.S. Patent, 1993.

[34] Jan R. Westra, Chris J. M. Verhoeven, and Arthur H.M. van Roermund, "Analysis and Design of Quadrature Oscillators", 1st ed., Springer, 1999, ch. 8, pp. 215-267.

[35] Nauta, B., "A CMOS transconductance-C filter technique for very high frequencies," IEEE Journal of Solid-State Circuits, vol.27, no.2, pp.142-153, Feb 1992.

[36] Mondal, I.; Krishnapura, N., "Gain enhanced high frequency OTA with on-chip tuned negative conductance load," IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp.2085-2088, 24-27 May 2015.

[37] Fahs, B.; Ali-Ahmad, W.Y.; Gamand, P., "A Two-Stage Ring Oscillator in 0.13-um CMOS for UWB Impulse Radio," IEEE Transactions on Microwave Theory and Techniques, vol.57, no.5, pp.1074-1082, May 2009.

[38] Anand, S.B.; Razavi, B., "A CMOS clock recovery circuit for 2.5-Gb/s NRZ data," IEEE Journal of Solid-State Circuits, vol.36, no.3, pp.432-439, Mar 2001.

[39] Yan, W.S.T.; Luong, H.C., "A 900-MHz CMOS low-phase-noise voltage-controlled ring oscillator," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol.48, no.2, pp.216-221, Feb 2001.

[40] Carnes, J.; Vytyaz, I.; Hanumolu, P.K.; Mayaram, K.; Un-Ku Moon, "Design and Analysis of Noise Tolerant Ring Oscillators Using Maneatis Delay Cells," 14th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2007, pp.494-497, 11-14 Dec. 2007.

[41] ElSayed, A.M.; Elmary, M.I., "Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure," IEEE Journal of Solid-State Circuits, vol.36, no.4, pp.701-705, Apr 2001.

[42] van der Tang, J.; van de Ven, P.; Kasperkovitz, D.; van Roermund, A., "Analysis and design of an optimally coupled 5-GHz quadrature LC oscillator," IEEE Journal of Solid-State Circuits, vol.37, no.5, pp.657-661, May 2002.

[43] Nizhnik, O.; Pokharel, R.K.; Kanaya, H.; Yoshida, K., "Low Noise Wide Tuning Range Quadrature Ring Oscillator for Multi-Standard Transceiver," IEEE Microwave and Wireless Components Letters, vol.19, no.7, pp.470-472, July 2009.

[44] Xuan Zhang; Apsel, A.B., "A Low-Power, Process-and- Temperature- Compensated Ring Oscillator With Addition-Based Current Source," IEEE Transactions on Circuits and Systems I: Regular Papers, vol.58, no.5, pp.868-878, May 2011.

[45] Abdul-Latif, M.M.; Sanchez-Sinencio, E., "Low Phase Noise Wide Tuning Range N-Push Cyclic-Coupled Ring Oscillators," IEEE Journal of Solid-State Circuits, vol.47, no.6, pp.1278-1294, June 2012.

[46] J.M. Rabaey et al., "Digital Integrated Circuits: A Design Perspective", Prentice Hall, 2003.

[47] B. Nauta, "Analog CMOS filters for very high frequencies", Kluwer Academic Press ,1993.

[48] Y. Zhang and C. Chye-Boon, "An In-Phase-Coupled Class-C Quadrature VCO With Tunable Phase Error", IEEE Letters on Microwave and Wireless Components, Vol. 24, No. 11, 2014, pp.796-798.

[49] Wei Li and Kwok-Keung M. Cheng, "A Novel, Low-Voltage, Current Reused, Quadrature VCO and Divide-by-4 Frequency Divider Circuit", IEEE Letters on Microwave and Wireless Components, Vol. 23, No. 2, 2013, pp.87-89.

[50] Kuang-Wei Cheng, "A Current-Switching and gm-Enhanced Colpitts Quadrature VCO", IEEE Letters on Microwave and Wireless Components, Vol. 23, No. 3, 2013, pp.143-145.

[51] Juan Xie et al., "A low power low phase noise dual-band multiphase VCO", Elsevier Microelectronics Journal, No. 43, 2012, pp. 1016-1022.

[52] Chi-Hsien Lin and Hong-Yeh Chang, "A Low-Phase-Noise CMOS Quadrature Voltage-Controlled Oscillator Using a Self-Injection-Coupled Technique", IEEE Transaction on Circuits and Systems - II: Express Briefs, vol. 59, no. 10, 2012, pp. 623-627.

[53] Mojtaba Atarodi, "A low power, low phase noise, square wave LC quadrature VCO and its comprehensive analysis for ISM band", Elsevier International Journal of Electronics and Communications AE, No. 65, 2011, pp. 458-467.

[54] Shuenn-Yuh Lee et al., "A CMOS Quadrature VCO With Subharmonic and Injection-Locked Techniques", IEEE Transaction on Circuits and Systems - II: Express Briefs, vol. 57, no. 11, 2010, pp. 843-847.

[55] Sheng-Lyang Jang et al., "A 0.18um CMOS Quadrature VCO Using the Quadruple Push-Push Technique", IEEE Letters on Microwave and Wireless Components, Vol. 20, No. 6, 2010, pp.343-345.

[56] Ke Zhang et al., "A wideband differentially switch-tuned CMOS monolithic quadrature VCO with a low Kvco and high linearity", Elsevier Microelectronics Journal, No. 40, 2009, pp. 881-886.

[57] Andrea Mazzanti, Francesco Svelto, "CMOS injection locked oscillators for quadrature generation at radio-frequency", Elsevier Microelectronics Journal, No. 37, 2006, pp. 1241-1250.

[58] Ying Chen and Koen Mouthaan, "Wideband Varactorless LC VCO Using a Tunable Negative-Inductance Cell", IEEE Transaction on Circuits and Systems - I: Regular papers, Vol. 57 No. 10, 2010, pp. 2609-2617.

[59] Lang, S.; Introduction to Linear Algebra, 2nd Edition, Springer, 1986.

[60] Tiku Yu; Rebeiz, G. M.; "A 24 GHz 6-Bit CMOS Phased-Array Receiver", IEEE Microwave and Wireless Components Letters, vol. 18, Issue 6, pp. 422 424, June 2008.

[61] Padilla, P.; Muñoz-Acevedo, A.; Sierra-Castaer, M.; "Low loss 360 Ku band electronically reconfigurable phase shifter", AEU - International Journal of Electronics and Communications, vol. 64, Issue 11, November 2010, pp. 1100-1104.

[62] Robertson, B; Fat Duen Ho; Hudson, T.; "Optimization of MEMS Ku-band phase shifter", Digest of papers of the IEEE 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, pp. 265, September 2004.

[63] De Los Santos, H.J.; Fischer, G.; Tilmans, H.A.C.; van Beek, J.T.M.; "RF MEMS for ubiquitous wireless connectivity. Part II". Application, IEEE Microwave Magazine, vol. 5, Issue 4, pp. 50-65, January 2005.

[64] Hongjiang Song, ?A general method to VLSI Polyphase filter analysis and design for integrated RF applications", IEEE International SOCC conference, pp. 31-34, September 2006.

[65] Mensink, E.; Klumperink, E.A.M.; Nauta, B.; ?Distortion Cancellation by Polyphase Mul-tipath Circuits", IEEE Transaction on circuits and systems-I:Regular papers, vol. 52, Issue 9, pp. 1785-1794, September 2005.

[66] Koul, S. and B. Bhat; "Microwave and Millimeter Wave Phase Shifters", vol. II, Norwood, MA: Artech House, 1991.

[67] Minaei, Shahram; Yuce, Erkan; "High Input Impedance NMOS-based Phase Shifter with Minimum Number of Passive Elements"; Circuits, Systems, and Signal Processing; Doi: 10.1007/s00034-011-9290-0

[68] Yuce, Erkan; "A Novel CMOS-Based Voltage-Mode First-Order Phase Shifter Employing a Grounded Capacitor"; Circuits, Systems, and Signal Processing, pp. 235-245, vol. 29, Issue: 2, 2010. Doi: 10.1007/s00034-009-9143-2

[69] Galal, S. H.; Ragaie, M. S. Tawfik; "RC Sequence Asymmetric polyphase Networks for RF Integrated Transceivers", IEEE Transaction on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 1, pp. 18-27, January 2000.

[70] Sinem Oztayfun, Selcuk Kilinc, Adem Celebi, Usur Cam; "A new electronically tunable phase shifter employing current-controlled current conveyors";AEU - Inter-

national Journal of Electronics and Communications, vol. 62, Issue 3, 3 March 2008, pp. 228-231.

[71] Tal Vitaly Zlotnikov, Ofir Degani, Igor Brouk, Yael Nemirovsky, "A 45nm CMOS miniature phase shifter with constant amplitude response", Microelectronics Journal, vol.42, pp.1143-1150, 2011.

[72] Yu-Sheng Su; Min-Chi Tsai; Jen-Chieh Wu; Ting-Yueh Chin; Chia-Chan Chang, "A V-/W-band 0.18-?m CMOS phase shifter MMIC with 180-300 phase tuning range," in Microwave Conference Proceedings (APMC), 2012 Asia-Pacific , vol., no., pp.91-93, 4-7 Dec. 2012.

[73] Pepe, D.; Zito, D., "A novel phase shifter for 60 GHz phased arrays," in Signals and Systems Conference (ISSC), 2015 26th Irish , vol., no., pp.1-4, 24-25 June 2015.

[74] Jinbo Li; Ran Shu; Gu, Q.J., "10 GHz CMOS hybrid reflective-type phase shifter with enhanced phase shifting range," in Electronics Letters , vol.51, no.23, pp.1935-1937, 11 5 2015.

[75] Garakoui, S.K.; Klumperink, E.A.M.; Nauta, B.; van Vliet, F.E., "Compact Cascadable g m -C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency," in Solid-State Circuits, IEEE Journal of , vol.50, no.3, pp.693-703, March 2015

[76] In Sang Song; Giwan Yoon; Chul Soon Park, "A Highly Integrated 1-Bit Phase Shifter Based on High-Pass/Low-Pass Structure," in Microwave and Wireless Components Letters, IEEE , vol.25, no.8, pp.523-525, Aug. 2015.

[77] Mehdi Askari, Hooman Kaabi, Yousef S. Kavian, "A 24 GHz reflective-type phase shifter with constant loss in 0.18um CMOS technology", International Journal of Electronics and Communications(AE), pp.1134-1142, 2015.

[78] Meng, F.; Ma, K.; Yeo, K.S.; Xu, S., "A 57-to-64-GHz 0.094-mm 5-bit Passive Phase Shifter in 65-nm CMOS," in Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.PP, no.99, pp.1-1, 2015.

[79] Hyo-Sung Lee; Byung-Wook Min, "W-Band CMOS 4-Bit Phase Shifter for High Power and Phase Compression Points," in Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.62, no.1, pp.1-5, Jan. 2015.

[80] Dongho Lee, "CMOS phase shifter with low phase-variation VGA for V-band application and Ku-band scaled design," in Electronics Letters , vol.51, no.12, pp.910-912, 6 11 2015.

[81] You Zheng; Saavedra, C.E., "Full 360^o Vector-Sum Phase-Shifter for Microwave System Applications," in Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.57, no.4, pp.752-758, April 2010.

[82] Asoodeh, A.; Atarodi, M., "A Full 360^o Vector-Sum Phase Shifter With Very Low RMS Phase Error Over a Wide Bandwidth," in Microwave Theory and Techniques, IEEE Transactions on , vol.60, no.6, pp.1626-1634, June 2012.

[83] Sanghoon Sim; Jeon, L.; Jeong-Geun Kim, "A Compact X-Band Bi-Directional Phased-Array T/R Chipset in 0.13um CMOS Technology," in Microwave Theory and Techniques, IEEE Transactions on , vol.61, no.1, pp.562-569, Jan. 2013.

[84] Carvajal, R.G.; Ramirez-Angulo, J.; Lopez-Martin, A.J.; Torralba, A.; Galan, J.A.G.; Carlosena, A.; Chavero, F.M., "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," in Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.52, no.7, pp.1276-1291, July 2005.

[85] Francisco R. Trejo-Macotela, Luis A Sánchez-Gaspariano, Carlos Muñiz-Montero, Alejandro Díaz-Sánchez, Roberto S. Arteaga-Murphy, Abel García-Barrientos, José M. Rocha-Pérez; "Flipped voltage follower based low noise amplifier with 640 MHz BW at 2.26 GHz, 1.3 dB NF, 1.2V Vdd, and up to 10 dBm IIP3", Indian Journal of Pure & Applied Physics, vol. 53, pp. 546-553, August 2015.