A Test Framework for interconnection Open Defects

by

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To

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Summary

The scaling down of dimensions of the devices and integrated circuits generates lines of interconnection in a circuit, presenting a proximity every greater time among them. This proximity causes that some lines are reconciled. These couplings at interconnections creates parasitic capacitances that can get to cause interference levels which they affect the logical value of the information. Because of this, it is important to improve the conventional methodology of test.

This thesis has the following organization:

In Chapter 1, the different basic concepts of test of integrated circuits are presented. Also the definition of faults and errors are showed. The concept of test and logic testing are presented too. Finally difficult to testing is reviewed.

In Chapter 2, the basic concepts and the importance of test of integrated circuits are presented. The properties that must have the stuck-at fault model are also presented. Also, the basic defect model proposed in this work is exposed. Some simulations results from this basic defect model are depicted and extended to consider some effects like coupling effects, sensitization gates and trapped gate charge. Finally the proposed test framework for interconnection opens is shown.

In Chapter 3, the basic design of a CAD tool called OPVEG (Opens Vectors Generator) oriented to generate favorable test vectors for opens is presented using data obtained from layout and circuit logic description, favorable test vectors considering capacitive couplings between adjacent nodes are obtained. These vectors can be used to improve the detectability of interconnection opens.

In Chapter 4, a Fault Simulator for Interconnection Opens (FASOP) is presented which is able to evaluate the defect coverage of interconnection opens. Also gives useful information to evaluate the detectability of these defects. Based on this information better test vectors may be generated to improve the defect coverage or DFT measures can be undertaken. FASOP uses circuit logic description and layout information as inputs.

FASOP considers the effect of the coupling lines and the sensitized and un-sensitized gates influencing the floating line of the interconnection open. FASOP also evaluates the defect coverage considering the gate trapped charge.
In Chapter 5, The conclusions of this work are given.

Sumario

La reducción de dimensiones de los dispositivos y circuitos integrados genera cada vez más líneas de interconexión en un circuito, presentando además, una cercania cada vez mayor entre ellas. Esta cercanía provoca que algunas líneas se acoplen. Estos acoplamientos en líneas de conexin crean capacitancias parásitas que pueden llegar a causar niveles de interferencia que afecten el valor lógico de la información. Debido a esto es importante mejorar los métodos convencionales de prueba.

La organización de esta tesis es la siguente:

En el capítulo 1, los conceptos básicos de prueba en circuitos integrados son analizados. Además, las definiciones de algunas de las fallas más importantes que se pueden llegar a presentar en los circuitos integrados así como los conceptos de prueba y prueba lógica son presentadas.

En el capítulo 2, los conceptos básicos y la importancia de la prueba de circuitos integrados se presentan. Las características que deben tener el modelo de fallas stuck-at también es presentado. Aí como, el modelo básico del defecto propuesto en este trabajo es expuesto. Los resultados de algunas simulaciones de este modelo básico del defecto es representado y extendido para considerar algunos efectos tales como acoplamientos capacitivos, compuertas sensibilizadas y no sensibilizadas y los efectos de las cargas atrapadas. Finalmente el marco propuesto de prueba para aberturas en interconexiones es presentado.

En el capítulo 3, el diseño básico de la herramienta CAD llamada OPVEG (Generador de vectores de prueba tipo open) orientado para generar los vectores de prueba favorables, se presenta usando los datos obtenidos del layout y la descripción lógica del circuito, de donde se pueden obtener los vectores favorables de prueba que consideran acoplamientos capacitivos entre los nodos adyacentes. Estos vectores se pueden utilizar para mejorar la detectabilidad de aberturas en interconexiónes.

En el capítulo 4, un simulador de la fallas para aberturas en interconexiones (FASOP),

el cual es capaz de evaluar la cobertura del defecto de la interconexión es presentado. También proporciona información útil para evaluar la detectabilidad de estos defectos. Basado en esta información, mejores vectores de pueba pueden ser generados para mejorar la cobertura de estos defectos o emprender medidas de DFT. FASOP utiliza la descripción lógica del circuito y la información del layout como archivos de entrada. Además de considerar los efectos de los acoplamientos entre líneas y de las compuertas sensibilizadas y no sensibilizadas que afectan el voltaje en el nodo flotante. FASOP tambin evalúa la cobertura del defecto considerando las cargas atrapadas en las compuertas afectadas.

Finalmente en el capítulo 5 se presentan las conclusiones de este trabajo.

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Acronyms

ATPG	Automatic Test Pattern Generation
BSIM	Berkeley Short-Channel IGFET Model
CAD	Computer Aid Design
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CUT	Circuit Under Test
DFT	Design For Testability
FASOP	Fault Simulator for Opens
GCC	GNU C Compiler
IC	Integrated Circuit
ISCAS	International Symposium on Circuits and Systems
OPVEG	Opens Vector Generator
TSMC	Taiwan Semiconductor Manufacturing Company
VLSI	Very Large-Scale Integration

Chapter 1

Introduction

1.1 Introduction

Since the 80's, the silicon transistor has been the driving force in the electronic industry. The technological advances had made possible to have smaller transistors because lithography and the fabrication process have been improved. Due to this the density integration and the complexity of the circuits have been increased. At the same time the test complexity in modern integrated circuits has also increased. Several types of defects can appear due to alterations in the fabrication process. Defects may affect the functionability in integrated circuits (IC's) or to degrade their performance. According with its impact, defects can be classified as parametric and catastrophic [68]. Parametric defects impact the performance of integrated circuits. There is a widely spread of causes of parametric defects among them we can mention: temperature gradient variations in the etching process, local aberrations in the lens, variation in the doping process. Catastrophic defects affect the functionability of the integrated circuits as permanent, intermittent or transient faults. Permanent faults can be the consequence of short circuits, open defects, gate-oxide short and other defects. Intermittent faults are those excited by non-zero probability. Transient faults are due to random events such as alpha particles, crosstalk or ground bounce.

1.2 Defects, Errors, and Faults

According to [3] the concepts defects, errors, and faults can be defined as follows:

DEFECT. A defect in an electronic system is the non-desired difference between the *designed hardware* and the *fabricated hardware*. Some typical defects in VLSI circuits are:

1. Defects of the process: Absence/addition of non-expected materials, parasitic transistors, oxide breakage.

2. Defects of material: Defects of the body (imperfections of the crystal), impurities of the surface, etc.

3. Defects of use: Dielectric rupture, electromigration. etc.

4. Defects of encapsulation: Degradation of contacts, holes or openings in the sealed.

ERROR. An erroneous output signal produced by a system with defects is called error.

FAULT. Representation of a defect at an abstract level of operation.

This thesis is focused in interconnection open defects. Opens in interconnection paths disconnect the driven gate(s) from the driving gate. Due to the break the Pmos and Nmos transistors connected gates of the driven gate(s) float. Interconnections opens can be full opens or resistive opens (See figure 1.1). A full open is when there is complete absence of material in a section of the layer. The distance between the two disconnected points is large enough than there is non-influence from the input signal on the floating line. A resistive open is when the conductive material is not completely broken (See figure 1.1). As a consequence the resistance in this conducting path increases.

Contacts/vias are a likely place for an open to occur [10, 30, 81, 87]. Contact/vias have become an important yield detractor in modern technologies which have a high number of contact/vias due to the many used metal levels [10, 81]. Figure 1.2 illustrates defects on vias. A malformed contact or a via can give as result a defective connection. In subtractive-aluminum based technologies these problems became severe for 0.25μm generation and lower [77]. In cupper based technologies more defective connections are expected.

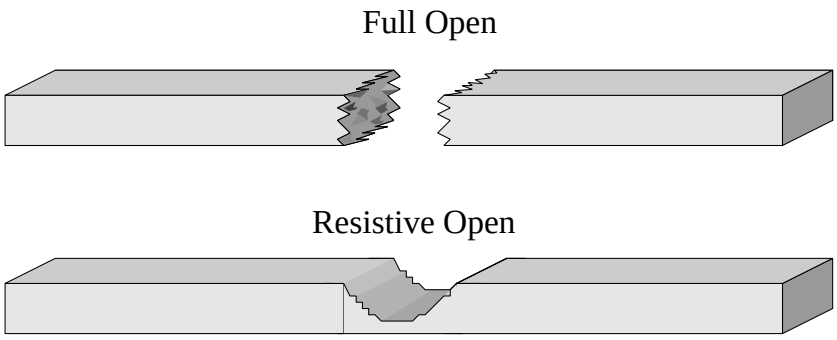


Figure 1.1: Concept of full and resistive open in interconnection line [70]

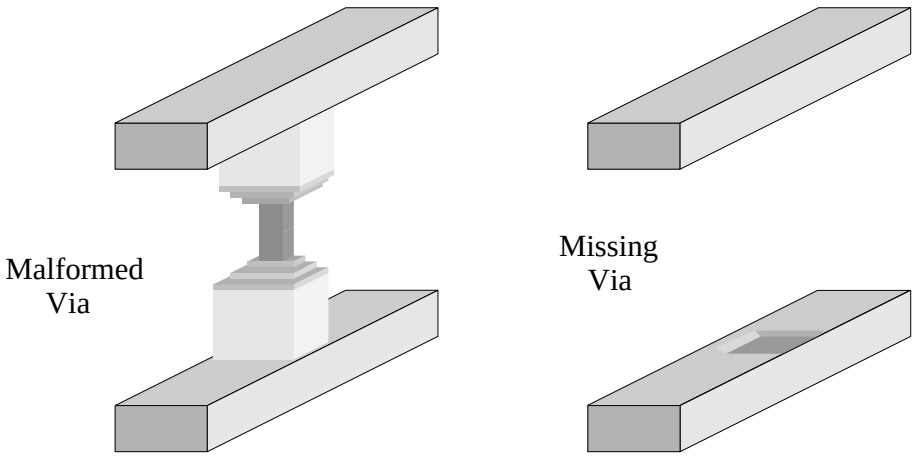


Figure 1.2: The concept of full open and resistive open in vias

Damascene-copper process uses a dual-damascene process [80, 89]. In this case vias and metal lines are both patterned and etched prior to the additive metalization. In the flow of this process there is the potential for residual resist or polymer blockage in the damascene through metal or via [77]. Because this micromasking during the subsequent lithography step or blockage of the post-RIE metalization can occur. In figure 1.3, a particle dust producing a resistive open in a copper based interconnection process is illustrated. The open defect density in copper shows a higher value that those opens in aluminum [77]. Higher metal levels are more prone to opens that those in lower metal levels.

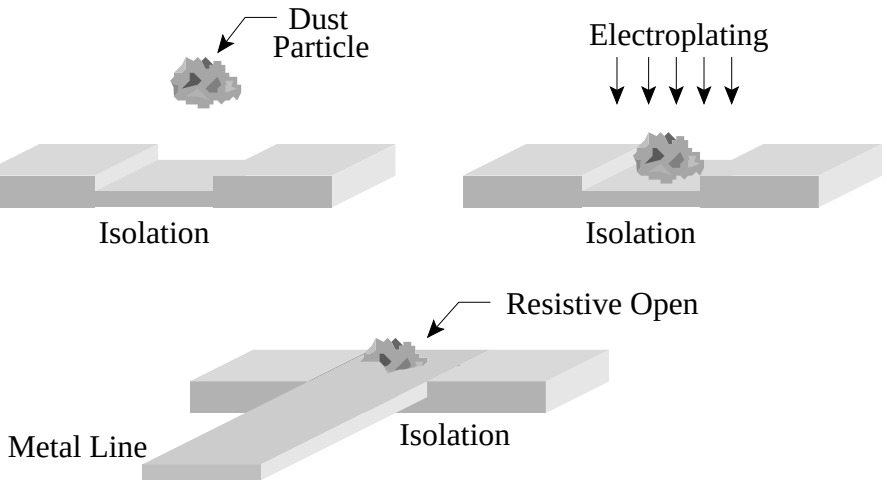


Figure 1.3: Resistive opens in cupper process

Poly and metal wires leaves hills in the oxide in planarization technologies [36, 93]. The bumps in the oxide can be smoothed by different chemical or mechanical methods. Due to this step coverage problems can occur which can produce breaks in subsequent metalization layers.

1.3 Test of Integrated circuits

The goal of the test of integrated circuits is to identify those fabricated circuits which do not satisfy the initial specifications. The test of an IC has the following steps [70]:

1.- Apply the input vectors to the controllable inputs of the circuits. The input vectors sensibilize the defect and propagate the possible error to an observable output.

2.- A measurement is made at an observable output.

3.- The measured value is compared against a reference value to determine if the circuit is accepted as fault-free or rejected.

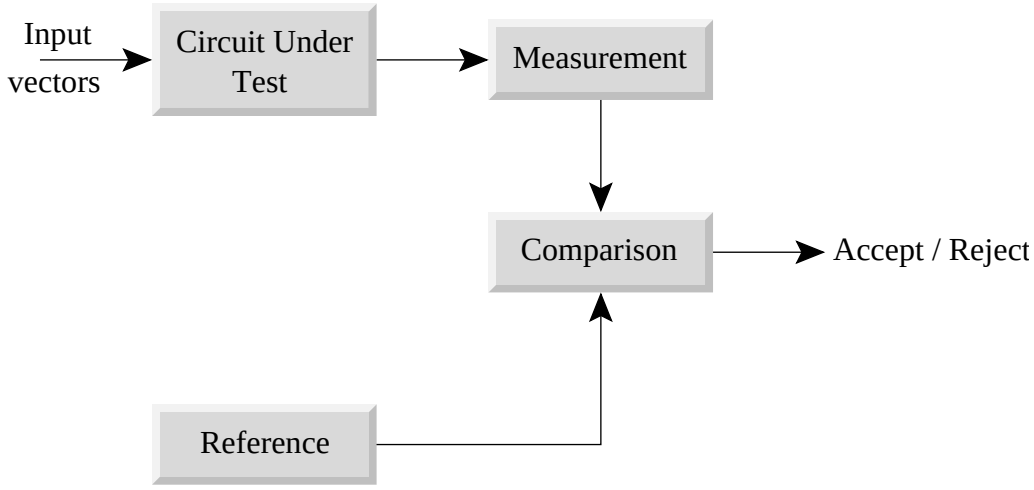


Figure 1.4: General test diagram

1.4 Fault Models

For testing the integrated circuits the physical defects are represented adequately in a superior level of abstraction. This is called Fault Modeling. Fault modeling can be made at different levels of abstraction such as electrical, logical or functional. Models [58, 70, 91] are defined which describe the effect of the physical defects in the behavior of the circuit. Test pattern generation takes place based on a given fault model. A good fault model should have the following properties [33, 68]:

- It should match the type of circuit in which it is to be used.
- The complexity of the faults should not imply excessive computation effort.
- The fault model should reflect the behavior of the physical faults with sufficient accuracy.

1.4.1 Stuck-at Fault Model

The most widely used fault model is the stuck-at model [39, 63] [27]. The *Single Stuck-at Fault* (SSF) model abstracts the implementation and technology details of a circuit's representation by placing fault occurrence directly into the gate-level representation of the circuit.

The *SSF* fault model assumes that a defective node behaves like a node permanently connected to one of the supply voltages, either V_{DD} or GND. In this model, *SA0* (*Stuck-at-0*) and *SA1* (*Stuck-at-1*) are used to describe a node that exhibits a fault [2]. At the gate level, the number of faults that can occur for a combinational gate with n-inputs and 1-output is *2n +2* [72]. Each of the n input nodes can suffer a SA0 or SA1 faults. The same is true for the output nodes. In the stuck-at fault model, the set of vectors is applied to the primary inputs of the circuit to sensitize the fault. The error is propagated to a primary output (PO). In a circuit several stuck-at faults can occur simultaneously. A circuit with n lines would have $3^n - 1$ possible states stuck-at which is a high number and computationally expensive. Therefore, it is common to model only a single fault *stuck-at* at the same time (non-multiple faults). In this way a circuit with n lines will have $2n$ faults *stuck-at*. This number is further reduced by the process of compaction of faults due that exist equivalent faults.

Some of the characteristics of this model can be summarized as:

- Many different physical defects may be modeled by the same logic
- The complexity is greatly reduced
- The stuck-at model is technology independent
- Single stuck-at test covers a large percentage of multiple stuck-at
- Single stuck-at test covers a large percentage of unmodeled physical defects

In spite of the great advantages of the stuck-at fault model, it has been found that this model is not adequate to represent some defects in CMOS technologies [26, 70, 82, 84, 90]. Because of this other fault models have been proposed.

1.4.2 Bridging defects

Bridging defects have also been shown to be a major source of failure in VLSI [31, 45]. These types of defects are defined in [40] as unintentional connection between two or

more circuit nodes. Ferguson et. al. [29] defined these types of defects as undesired electrical connections between two or more lines resulting from extra conducting material or missing insulating material. In order to create the fault condition for a bridging defect, the test vectors must set the shorted nodes to opposite logic polarities. The test vector also propagate the weaker, incorrect logic value, to a PO [29, 51]. The requirement for creating the fault condition is not considered by the traditional SSF model. So a test set with 100 percent stuck-at fault coverage does not guarantee that two bridged circuits will be detected [76].

Figure 1.5 shows two inverters with an ohmic defect bridge that produce a short between the output of the inverter (I_1) and V_{DD}. When a low voltage (0 V) is applied to the input of the inverter (I_1) this produce a high voltage in node V_2. This condition makes that pmos transistor is on, whereas the Nmos is off. When the input signal change to high voltage a path between V_{DD} and G_{ND} through the Nmos appears. This can be seen in figure 1.5. A plot of V_2 versus the input voltage is shown in figure 1.6. It can be seen while the input remain at low voltage the output of the inverter (I_1) is high. When the input switch from 0 logic to 1 intermediate voltages appears at the output voltage V_2. As Nmos transistor try to pull node V_2 to ground the short resistance pulls this node to V_{DD}. The final voltage is given by the value of the short resistance.

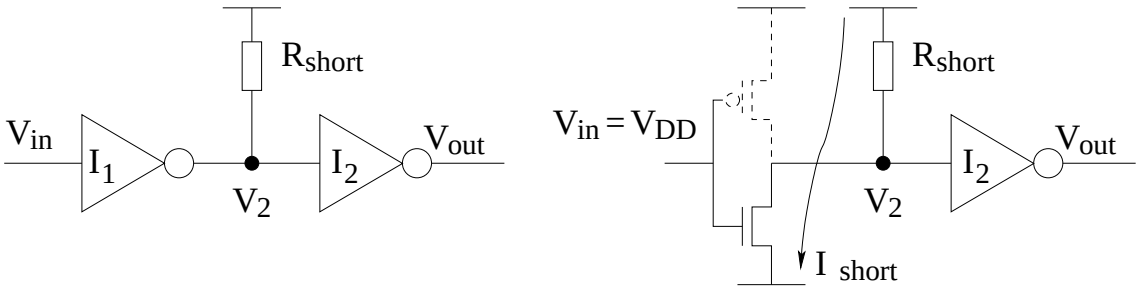


Figure 1.5: Power rail to signal node bridge defect [40]

The transfer characteristic of the gate driven by the weak node will determine the impact of the defect, since they will interpret the logic value that corresponds to each intermediate voltage [40].

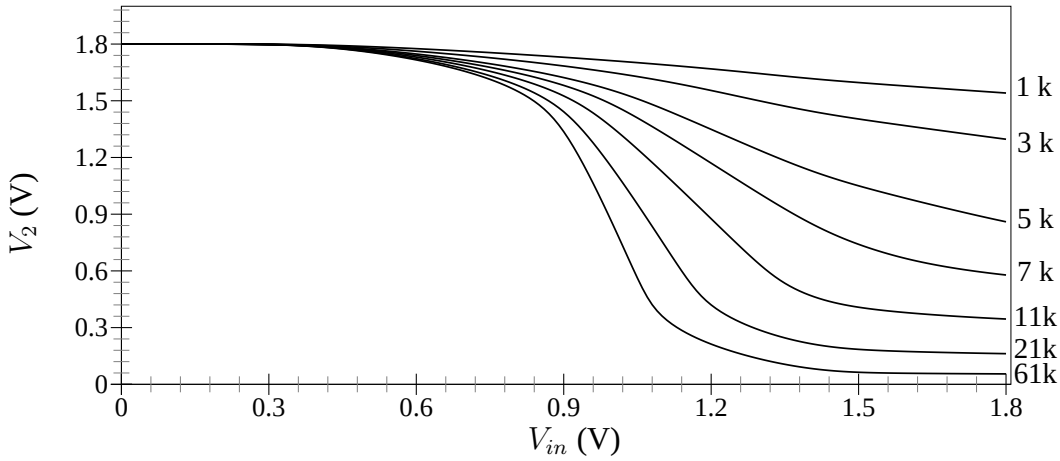


Figure 1.6: Voltages for different resistance values [40]

1.4.3 Open defects

Opens or breaks in CMOS circuits are faults difficult to diagnose using any of the current device testing techniques. A wide range of faulty behaviors have been observed. Opens can be caused by missing conducting material or by extra insulating material so that a single electrical node is separated into multiple nodes [29]. An open circuit can occur in any of the interconnect materials affecting either the gate, drain or source connections. The fault behavior caused by the presence of an open is dependent on its location, its resistance, the values of parasitic coupled capacitances and leakage currents associated with the floating node.

In [40] are defined six general classes of opens. This classes are the follows:

- Transistor on
- Transistor pair on
- Transistor pair on/off
- Delay
- Memory (Transistor off)
- Sequential

The first five open categories appear in combinational logic circuits, and in certain instances in sequential circuit open defect behavior.

In general, for wide opens occurring in gates, fault behavior differs depending on the location of break. When opens occur that cause pairs of transistor gates to float, it is likely that one transistor conducts and the other does not leading to stuck-at behavior [92] [21]. In the case where only one transistor of the gate is floating, the defective transistor may be stuck-on. In this case the gate may function properly but switching at slower speeds [92]. A floating transistor gate may also be suspectable to coupling influences of adjacent metal conductors [67] [92] [21]. However, whether or not the logic function is disturbed depends on the transistor width and length ratios, the topology of the circuit and the manufacturing process variations [29]. When the width of the break is narrow enough electron tunneling may occur. Leakage current may also play an important role on defect behavior [92].

1.5 Types of tests

1.5.1 Logic Testing

Logic testing [33] is used to monitor the logic levels (Boolean values) of circuits under test (CUT). The output node of a CUT shows a defined logic value for a given combination of the inputs. Logic testing compares the response of the output node of the CUT with the expected fault-free response of the CUT. If both results are not the same the CUT is faulty. In logic testing, it is assumed that a sufficient time is waited after the vector application at the input for the output to settle to stable levels.

Functional Testing

In the early years of integrated circuit technology, an exhaustive or full functional testing strategy was employed for small scale integration (SSI) circuits IC's since circuit complexity was limited to single gates [17]. Internal nodes were easily accessible directly through the package IO pins and test process generation was easy. However, the method is only applicable to small circuits since the test set size is exponentially related to the number of inputs. For combinational circuit with *n* inputs, an exhaustive test set consists of 2^n input test vectors [88]. For a sequential logic circuit with *m* one-bit registers (memory elements) and an input-to-output relationship in which the outputs depend on both the inputs and the registers values, an exhaustive test set would consist of 2^{n+m} test vectors.

Structural Testing

As levels of integration evolved from SSI and MSI to LSI, full functional testing

was no longer possible due to the cost of applying the test set to the device [17]. A test set whose size is linear to the number of nodes in the circuit would have a clear advantage over the full functional testing strategy if it could meet the objectives of the device test. The cost additional due to find an appropriate test set could be amortized over the time saved in applying the reduced test set to every IC. Consequently, for LSI circuits the test process generation objective is to determine the minimum number of test vectors necessary to perform a structural verification of the IC.

Roth presents a simple method to derive a test set that meets this objective [73]. In this method, a truth table is constructed for the correct circuit and for each of the p faulty circuits. An iterative process compares the correct truth table with each of the faulty truth tables. When a discrepancy is found between the output values of the correct and faulty truth tables, the input vector is saved. Each faulty truth table is processed in this way until an input vector is found or the entries are exhausted. The resulting set of test vectors represents the device test set for these faults.

The obvious problem with this technique is its exponential time and space relationship with the number of inputs. Each truth table contains 2^n lines. If the circuit contains *p* nodes, then *p+1* truth tables would be required to carry outthe analysis. Clearly, this type of approach can not be used for large circuits. Investigations of alternative methods were considered in the 1960's [73] [65].

1.6 Delay Testing

Delay faults are parametric faults defined as out-of specification path delays which result in unstabilized or incorrect circuit behaviors [29] [20]. Correct circuit operation requires the signal propagation delay along every path from PI to PO to be less than the operational system clock interval. Defects that cause the propagation delay along one or more paths to be longer than operational system clock interval may result in either the latching of incorrect logic values by internal registers or the untimely arrival of circuit functional values at the POs. Delay fault testing is a parametric device testing method that uses an IC's output response time to input transitions as a defect detection mechanism.

Delay testing is not based to assure the logic levels of the CUT. Instead of that, the timing conditions of the observed nodes are assured to be under design specifications. The delay model can be mainly divided into gate delay model and path delay model

[5]. The gate delay model [22] is based in testing timing specifications of the selected device. However, cumulative delay variations from previous gates escape to this model. Path delay model resolves this problem [75]. A path is selected to be the target for measure the delay, then 0→1 and 1→0 transitions are propagated through the path. If the measured delays are inside of the observation window then the path is fault-free, otherwise the path is faulty. The observation window can be defined close to the functional timing of the path in statical distributions of delay [9].

A number of manufacturing defects including local defects and random process variations can cause CMOS logic to switch at speeds slower than normal but leave the functional behavior unchanged [24] [48]. For example, GOS defects can increase the propagation delay of defective nodes and cause failure of the IC in clocked environment. Parasitic transistor leakages, defective pn junctions and incorrect or shifted threshold voltages can also result in increased propagation delays. Additionally, delay faults can result from certain types of open circuit defects [9] [24] [48].

The transmission gate open circuit can not detected using logic testing but may be detected as a delay fault [51] [76] [72]. Moreover, delay faults can occur as intermittent (transient) faults which are responsible for most failures of digital equipment in the field [20] [62]. Delay testing showed to be an adequate testing tool in order to detect fault mechanisms as resistive opens and resistive bridges for sub-micron technologies [53].

Timing verification of integrated circuits is considered to be more difficult than logic verification [20] [62]. Even though the traditional DC test and the delay fault test share implementation characteristics, delay fault testing additionally requires both the accurate timing of a two-vector sequence and a sensitized path that extends from a PI to a PO [24]. The specification of a delay test can be defined as follows. At time t_1, the first vector of the two-pattern test, the initializing vector V_1, is applied to the PIs and circuit is allowed to stabilize. At time t_2, the second test pattern, V_2 is applied. Finally, at time t_3, a logic value measurement is made at the POs. The effectiveness of the delay fault test is dependent on the both the delay defect size and the propagation delay of the tested path [25] [62].

1.7 I_{DDQ} Testing

IDDQ testing is a test technique based on measuring the quiescent supply current of the device under test. A distinction needs to be made between its application to tech-

nologies with neglectable leakage current and application to technologies with non-neglectable leakage current. The traditional decision criterion which is valid for technologies with low leakage currents is based on the fact that a CMOS circuit does not draw any significant current in a stable situation. In a quiescent state, only the leakage current flows, which is in most cases can be neglected. The fact that under certain conditions a significant current flows when the device under test is in a quiescent state, indicates the presence of a manufacturing defect in the circuit. The defect causing a current increase, may influence the functionality of the circuit (functional failure) or may affect the lifetime and reliability of the circuit negatively.

Suppose a CMOS NAND gate (see Figure 1.7) with stuck-on in the source-drain terminals of transistor NB. The applied input vector A=1, B=0 should charge-up node OUT, however because the bridge, the Nmos network is active and a current path from V_{DD} to ground is created. NAND gate is detected as faulty because a high quiescent current consumption (I_{DDQ}) appears.

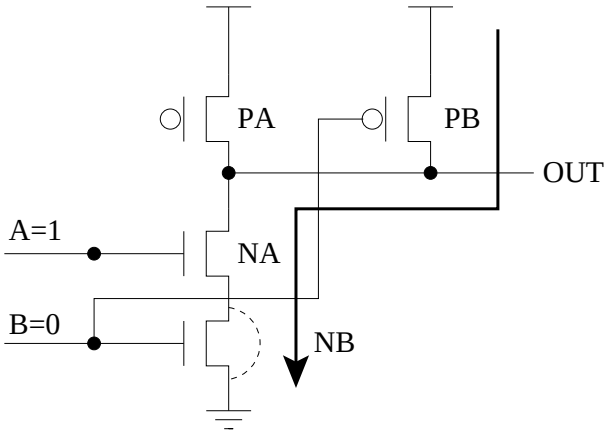


Figure 1.7: A faulty CMOS NAND gate [70].

For newer technologies, where the leakage current is non-neglectable, the base leakage cannot be neglected but needs to be considered as an offset level. The fact that under certain conditions there is an increase in the current flowing when the device under test is in a quiescent state, indicates the presence of a manufacturing defect in the circuit. By using a relative decision criterion (based on the comparison of the measured current to the base leakage current) defects can be screened reliability and effective, even in the presences of large background currents.

IDDQ testing is a very sensitive technique, able to detect such problems in an early stage before they really harm the circuit. It is also a possible alternative to replace

other, more expensive or more time-consuming test approaches, needed to guarantee the quality and reliability of the tested chip. In combination with emission spectroscopy and spectral analysis IDDQ is also a very powerful technique for defect location and defect diagnosis, obviating the need for fibbing.

The IDDQ test technique can be applied at wafer level, at packed device level, during incoming inspection, during life tests or even during on-line testing. Making use of an IDDQ test approach supported by the use of proper measurement instrumentation offers the following advantages :

- Increased product quality
- Replacement (or reduction) of Burn-in tests
- Elimination of early lifetime failures
- Increased product reliability
- Reduction of the overall test cost.
- Increase of engineering and failure analysis productivity.

I_{DDQ} current test demonstrated to be adequate to detect defects as bridging [78] and certain open defects [16]. However, as the technology scales the detection of some defects is missing. Not only simple current measurements have been used but also more elaborate strategies as current signatures [7] [35]. The information of defective circuits is contained in the level and the magnitude of the static current. High leakage current due to defects could be detected by the current signature. The detectability of I_{DDQ} has been increased by the concept of variable current thresholds [60]. Also layout-based test generation have been proposed [57]. Using layout, a fault list is created taking into account realistic defect representations.

Differential I_{DDQ} has also been proposed [11]. Differential I_{DDQ} is limited by leakage currents The proposal of Kruseman [11] is not efficient for off-state currents above 100mA. Cooling techniques [49] can be used to counter at the effect of subthreshold currents. Sachdev [74] has proposed other solutions to this I_{DDQ} limitation.

1.8 ATPG

A fault model is a hypothesis of how the circuit may go wrong in the manufacturing process. A fault is said to be detected by a test pattern if, when applying the pattern

set different logic response (values) appears between the assigned circuit and the faulty circuit in at least one of the primary outputs. ATPG for a given target fault consists of two phases: Fault activation and Fault propagation. Fault activation establishes a signal value at the fault site opposite to that produced by the fault. Fault propagation propagates the fault effect from the fault site to a primary output.

ATPG can fail to find a test for a particular fault in at least two cases. First, the fault may be intrinsically undetectable, so no vectors exist that can detect that particular fault. This situation appears for redundant circuits designed so that no single fault causes the output to change. Second, it is possible that a vector(s) exist, but the algorithm cannot find it.

The automatic generation of test vectors (Automatic Test Pattern Generation, ATPG) is the process to generate vectors of test for a circuit. This process is normally done at logical level. Algorithms ATPG could be considered like multipurpose, since they can generate test vectors, find logical redundant or unnecessary, and can provide another type of information of the circuit.

1.9 Difficulty of testing of opens

Because the scaling of the technology some trends will affect the actual testing methodologies [4,59]. Some faults may escape to conventional test methods. Non-conventional test methods [47, 61] should be used to obtain higher quality.

A significant research effort has been devoted to test of opens [16, 28, 38, 44, 47, 50, 55]. It has been found that breaks is an important contributor to test escapes [61, 86]. The problem has became worst with scaling of the technologies. The trends have increased sensitivity to subtle defects [61]. Subtle defects increases the delay for a small amount but they didn't cause a functional failure. However, for circuits running at higher speeds a system failure can occur. It has been found that full opens have a complex behavior [16, 38, 50, 55]. The detectability of this defects depends on technology and topology parameters. Furthermore, they behavior also depends on the gate oxide trapped charge [41, 44]. Needham et al. [86] have found that test of opens would require special temperature, voltage and timing conditions. Silicide open defects need to be tested at low temperature [13]. Delay fault testing has been suggested to be used to test resistive vias/contacts [10]. From simulation data it has been found that resistive opens have a significant range of resistances increasing the delay [83]. A high resis-

tance value is required for a stuck-at to occur. This makes a stuck-at based test less effective for opens. In addition, opens are more difficult to sensitize [15, 83]. Others authors [53] have pointed-out that crosstalk [18, 96] and power rail coupling [53] influences the detectability of resistive opens.

As the technology for the design and manufacture of integrated circuits scales, there is a progressive reduction of all the distances between lines, wide of lines, etc. (Scaling down). This has lead that in scaled technologies there is an important interaction in the lines near to each other. This is know as crosstalk. The interconnections may be responsible of until a 90% of the delay in an integrated circuit [46]. The parasitic coupling, induced by the proximity of two lines, includes capacitive and inductive effects. There is also mutual inductance between lines, which may becomes significant at very high frequencies and long lines.

The first step for the analysis of crosstalk consists on the study of the different effects that can cause the Crosstalk on a basic scheme of two lines with a problem of coupling. One line is denominated *Aggressor* or causative of the effect and another is denominated line *Victim*, which undergoes the consequences and effects of the previous one. In other words, if one of the lines remains in a permanent logical state 0 or 1 is denominated *Victim*. If the near line has a change of logical state of $0 \Rightarrow 1$ or $1 \Rightarrow 0$ it denominate aggressor line.

The basic scheme of the two coupled lines is showed in Figure 1.8. Each line connects the output of an inverter with the input of another inverter, there is a parasitic capacitance between the lines. This parasitic capacitance C_{AV} represents the *Crosstalk* effect among them.

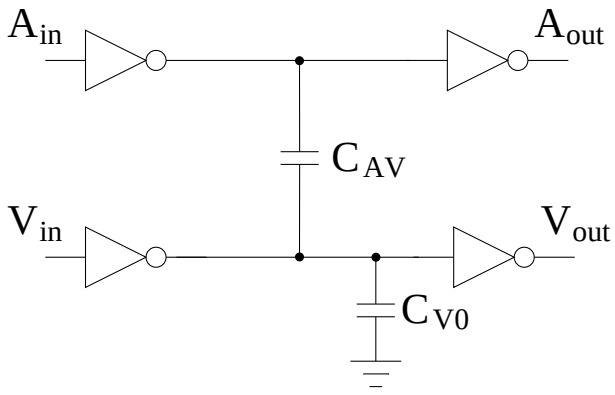


Figure 1.8: Scheme of two coupled lines

One of these two lines will behave like aggressor (Let's say *Line A*) and will be

the one that will produce a wrong operation at the victim line (*Line V*). The capacitive coupling can take to a possible wrong operation of the circuit (permanent errors in the logic) and to increase of power dissipation of the microcircuit. Other detailed studies on the Crosstalk behavior can be found in [69, 70]. In advanced technologies, with pulses of short length, the capacitive coupling distorts the signals that travel in the lines of metal with dispersion of frequencies to attenuation [64]. The Crosstalk has been analyzed by several methods [6, 8, 85] like the one of distributed parameters [23], domain of the frequency and lines of communication [32, 34, 37, 95].

The crosstalk effect may influence significantly the behavior of the circuit in the presence of a defect. This thesis is focused to consider the influence on the test detectability of the lines near to a line presenting an interconnection open defect.

1.10 Organization of the Thesis

This thesis is organized as follows: In Chapter II, the proposed basic electrical model for interconnection opens is presented. Coupling effects are studied. Simulation results for one single coupled line and several coupled lines over the floating node are depicted. The effects of sensitization and unsensitization gates are studied for different cases. In Chapter III, a methodology to generate enhanced vectors for interconnection opens considering the signals at the coupled lines is proposed. This methodology has been implemented in a CAD tool named OPVEG (Opens Vectors Generator). Experiments and results obtained by applying OPVEG are exposed in comparative tables for four Benchmark circuits ISCAS'85. In Chapter IV, a Fault Simulator for Interconnection Opens (FASOP) is presented which is able to evaluates the defect coverage of interconnection opens (FASOP). The general environment where FASOP works is described and the structure of FASOP is explained. A methodology to estimate the range of detection of interconnection opens is presented in 4.4. The results of applying FASOP to some ISCAS'85 benchmark circuits [12] are presented. FASOP is also used for making detectability analysis. This may allow to improve the test quality. Finally, in Chapter V, the conclusions of the thesis are given.

Chapter 2

Interconnect Opens

2.1 Introduction

In this chapter the basic concepts and the importance of test of integrated circuits are presented. Opens in interconnection paths disconnect the driven gate(s) from the driving gate. Due to the break the PMOS and NMOS transistor connected gates of the driven gate(s) float. From experiments made on ISCAS'85 benchmark circuits, it has been found that interconnection opens have the highest probability of occurrence among the different types of opens [10, 30, 81, 94]. Vias are a likely place for an open to occur and there are a high number of vias in actual process due to the many metal levels [59] [4]. Breaks defects have been found to be an important contributor of test scape. The effects on floating node, due to capacitive couplings are studied [61] [47]. An important effort has been dedicated to the tests focused to the defects caused by interconnection opens of a circuit. It has been found that interconnection opens contributes to the non-detection of faults. The problem has been increased with the scaling of the technology. The detection of these defects depends on the technology and topology of the circuits. In addition, the technology scaling has increased the sensitivity of circuits that is had when slight defects appear. These defects increase the delay of the circuits to a certain extent but they do not really cause a functional fault. Nevertheless in circuits that work at high speeds faults can appear. Among these the faults caused by opens have a complex behavior [50] [38]. Some authors [53] have found that the Crosstalk [18] [96] and the coupling with supply lines influence [53] the detectability of these defects. Simulation results are showed in this section too. The influence on defective line by one coupled line and more than one coupled line have been simulated.

Different cases have been considered to study these effects. Different coupling signals are applied for different capacitive values.

In this chapter the properties that must have the stuck-at fault model are presented. Also, the basic defect model proposed in this work is exposed. Some simulations results from this basic defect model are depicted and extended to consider some effects like coupling effects, sensitization gates and trapped gate charge. Finally the proposed test framework for interconnection opens is shown in section 2.6.

2.2 Defect Modeling

In order to make the tests of integrated circuits the defects are represented a suitable superior level of abstraction. This representation is used for the generation of test vectors. In order to obtain these vectors, models of faults are defined that describe the effect of the physical defects in the behavior of the circuits [91] [58]. The modeled faults can be made at different levels of abstraction, such as electrical, logical or functional. The model of faults must have the following properties [10, 68]:

- It must be adapted to the type of circuit where it is going to be applied.
- The complexity of the faults does not have to imply an excessive effort and calculation.
- The model of faults must reflect the behavior of the physical faults with an acceptable precision.

The fault model more widely used is the **Stuck-at**. This model assumes that a certain node of a circuit always behaves as a “1” or “0” logic as a result of the presence of a defect. With the use of this model a structural test for the detection of faults can be made in the logic circuits. This model considers a circuit like a coupling of boolean gates, and therefore it is assumed that the fault affects couplings between gates. The model *Stuck at* considers two possible cases of fault for each node [26]:

1) fixed node permanently to ”1” logical one (*stuck-at-1*).

2) fixed node to ”0” logical (*stuck-at-0*).

In a circuit several *stuck-at* faults can be presented simultaneously. A circuit with *n* lines would have $3^n - 1$ possible states stuck-at. This is obtained considering the

possible combinations states of the circuit where each line can be to stuck-at-0, stuck-at-1, or free of fault. Obvious, this would take to a great number of states of fault in the circuit. Therefore, it is common to model single fault *stuck-at* at the same time (*non-multiple faults*). In this way a circuit with *n* lines will have $2n$ *stuck-at* faults. This number of faults is even reduced more by the compacted faults that exists between equivalent faults. The following considerations in the modeled *stuck-at* are included.

a) Single line has fault.

b) The line with fault this permanent to 0 or 1 logical.

c) The fault can be to the input or output of a gate.

Some of the characteristics of this model are [69]:

1.- Many different physical defects can be modeled with the same logic [70].

2.- The complexity is significantly reduced.

3.- The *stuck-at* model is independent of the technology.

4.- A test using a simple stuck-at fault covers a great percentage of not modeled physical defects.

In spite of the great advantages of the stuck-at model, it has been found that do not represent some defects in CMOS technologies [26] [27] [90]. Due to this other fault models have been proposed [82] [84].

Figure 2.1 shows the basic defect model proposed in this work. Although basic, this model can be extended to other gate(s) and consider any number of coupling signals as will see explained in next chapters. The model (see figure 2.1) shows different capacitive couplings that affect the voltage at the floating node (V_{if}).

Overlap capacitances of transistor Pmos are C_{gsop}, C_{gdop} and C_{pw}. Where C_{gsop} is overlap capacitance between *gate-source*, C_{gdop} is overlap capacitance between gate-drain and C_{pw} the poly-well capacitance. Nmos transistor present C_{gson}, C_{gdon} and C_{pb} overlap capacitances. Where C_{gson} is overlap capacitance between *gate-source*, gate-drain overlap capacitance is defined by C_{gdon} and C_{pb} is the poly-bulk capacitance. In this model routing capacitances also affect the voltage at the floating node. C_r^1 and C_r^0 are those capacitances that run over the well and substrate respectively. Using this

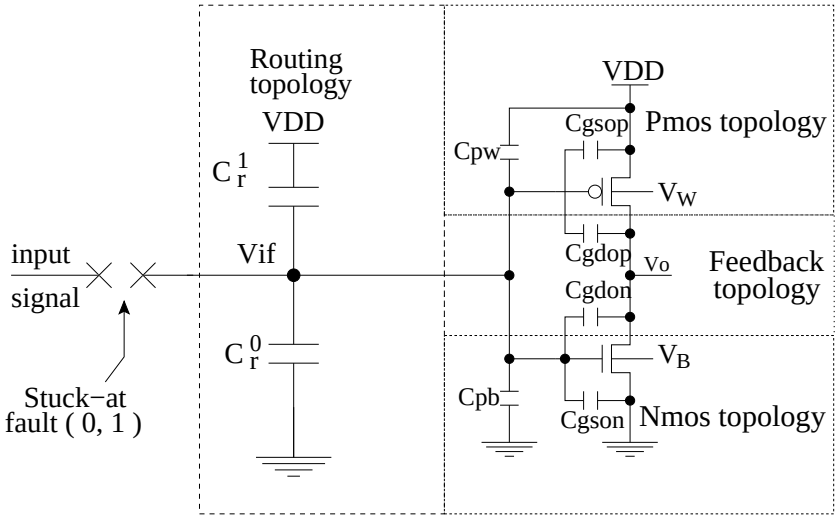


Figure 2.1: Basic electrical model proposed

model, simulation results showing the voltage at the floating node V_{if} when the power supply is are shown in figure 2.2. The principal goal of the simulation is to show the effect on the floating node caused by the surrounding topologies to the open defect. We use TSMC 0.18 μm SPICE LEVEL 49 CMOS technology.
Three different cases have been considered simulations.

1 .- CMOS inverter with $W_p = Wn$.

2 .- CMOS inverter with $W_p >> Wn$.

3 .- CMOS inverter with $W_p << Wn$.

Plots in figures 2.2, 2.3 and 2.4 shows 4 different curves, that correspond to the power supply voltage V_{dd} and 3 different voltages at the floating node $V_{if_1} = 0.35V$, $V_{if_2} = 0.55V$ and $V_{if_3} = 0.75V$. Let's analyze the equal sized CMOS inverter (see figure 2.2). It is possible to appreciate that the voltage at the floating node is increased when being increased the voltage V_{dd}. As a first order approach voltage is induced at the floating node due to the Pmos overlap capacitance (C_{gsop}) and the poly-well capacitance (C_{pw}) (See figure 2.1). The voltage at the floating node is influenced by the sizes (Wn and Wp) of Nmos and Pmos transistors as will see in next figure 2.3. Plot of figure 2.3 have same characteristics to the previous plot. In this case, the difference resides that the channel width (Wp) of Pmos transistor is longer than channel width (Wn) of Nmos transistor. As we can see in figure 2.3 the final voltages for different V_{if} have been

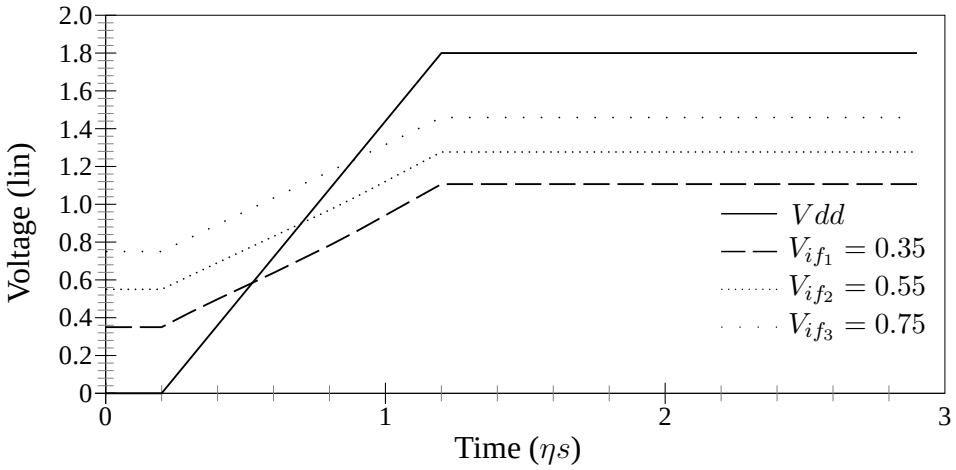


Figure 2.2: Floating voltage node analysis of symmetric CMOS inverter $Wp = Wn$

increased. In a first order approach this behavior is due to the higher values of C_{gsop} and C_{pw}.

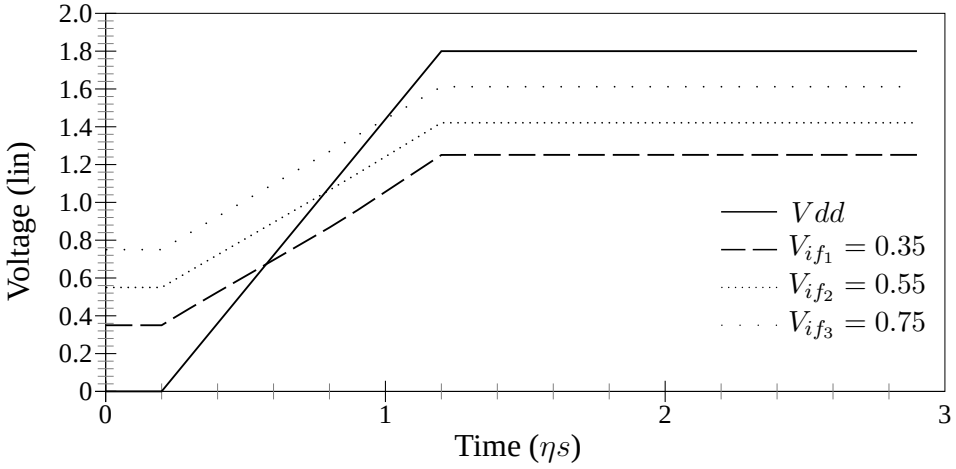


Figure 2.3: Floating voltage node analysis of symmetric CMOS inverter $Wp >> Wn$

Figure 2.4 shows the case $Wp << Wn$. It is possible to see that the final voltages for different V_{if} is lower than exposed at previous cases. The induced voltage at the floating node is lower, due the smaller C_{gsop} and C_{pw}.

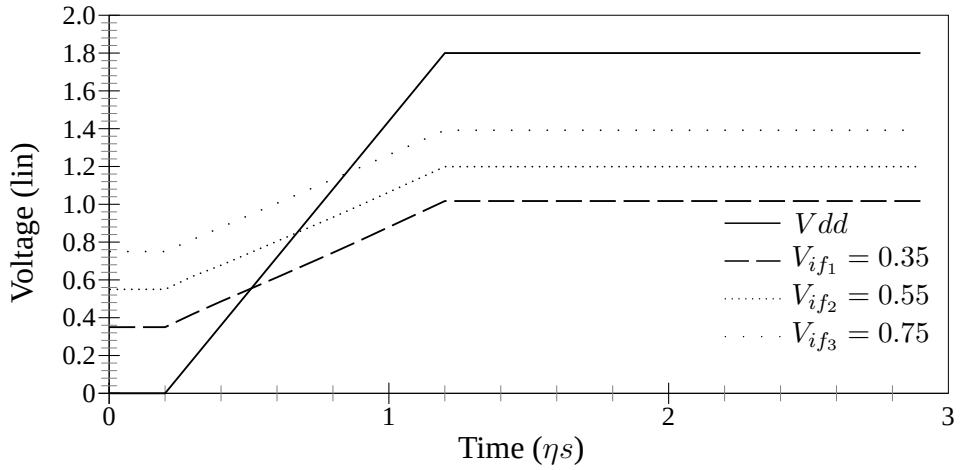


Figure 2.4: Floating voltage node analysis of symmetric CMOS inverter $Wp << Wn$

2.3 Coupling effects

The floating line can be influenced by signals running at adjacent coupling lines and/or by lines located above/below the floating line. In this section coupling effects on the floating node are studied. Different simulation results considering one and more than one capacitive couplings on defective line are depicted. The floating node voltage (V_{if}) depends on the transistor structure of the affected gate(s) modeled by its gate charge, the surrounding capacitances to the floating line and the trapped charge during the fabrication process.

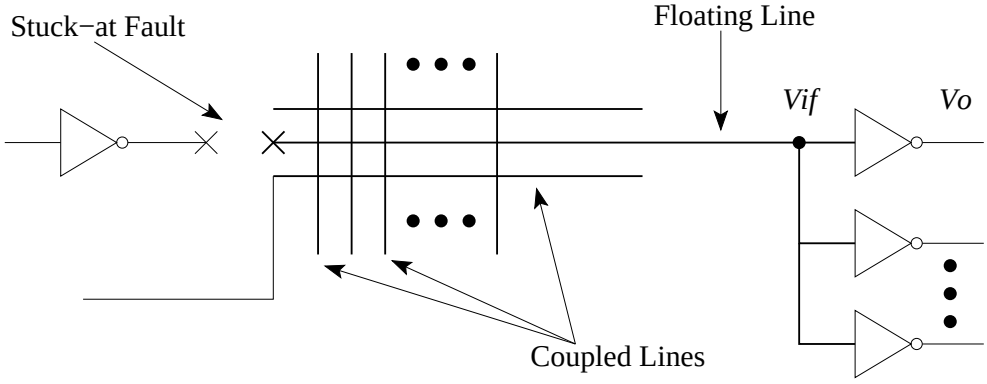


Figure 2.5: A typical defective circuit topology

Figure 2.5 shows an inverter gate with *n* number of coupling lines. We will initiate the study of the effect on the floating node due to one coupling line. Adding a coupled

line to the floating node of the circuit in figure 2.1, the circuit shown in figure 2.6 is obtained. A more simplified circuit shown in figure 2.7. Three different values of capacitive couplings have been considered and one input signal (pulse) applied.

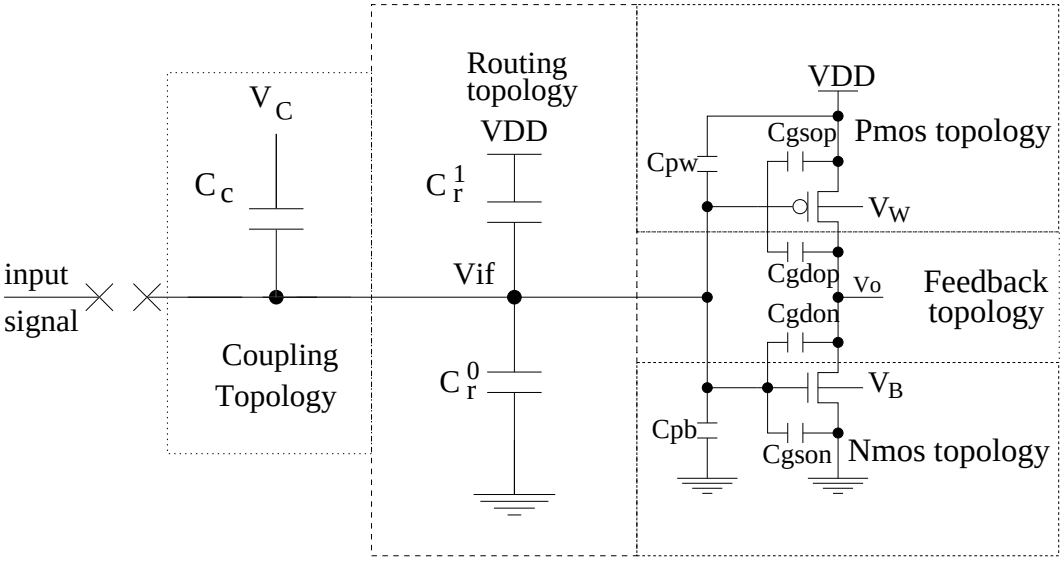


Figure 2.6: Basic electrical model proposed

Plot depicted on figure 2.8 shows the simulation results. A Stuck-at 0 fault has been considered on the defective line. To detect this fault it is necessary to set the input signal to "1" logic and coupling signal to "0" logic (Input C_C). Initially a voltage on the floating node of 0.3 volts is assumed. The first coupled line considered is $C_{C_1} = 0.4fF$, this value correspond to 20% of the sum of $C_{Vdd} + C_{Gnd} = 1.5fF + 0.5fF$ (*selection factor*). A signal (pulse) has been applied on input C_C. This pulse goes from "0" to "1" with time delay of 2 ηs, the rise time is 0.1 ηs and fall time 0.1 ηs. Due to the capacitive coupling connected to defective line V_{if} increases its voltage when the pulse at C_C is at a high state. Plot in figure 2.8a shows input signal on C_C. In figure 2.8b is depicted different voltages on the floating node for different capacitive values. It can be seen that during the delay time (0-2 ηs), the voltage on defective line is increased due to the different parasitic capacitances of Nmos and Pmos transistors. This effect, explained in section 2.2, causes that voltage on defective line goes from $0.3V$ to $0.55V$ depending on the coupled capacitance value. The voltage on defective the defective line stays on this value until the effect of capacitive coupling (due to the input C_C) increases this value. Behavior of floating line is determined by the input C_C. When stimulus signal goes from $1.8V$ to $0V$, voltage on floating line returns to lower values.

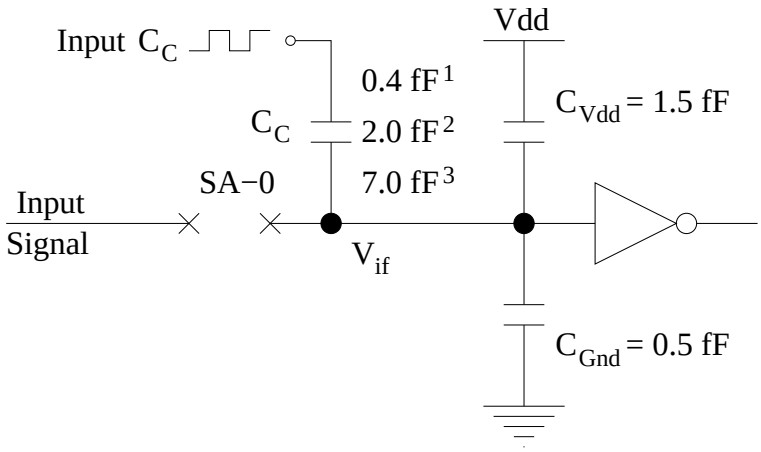


Figure 2.7: Stuck-at 0 fault

As were explained before, the value of $C_{C_1} = 0.4fF^1$ corresponding to 20% of the sum of C_{Vdd} and C_{Gnd}. It can be seen that the effect produced by this capacitive coupling is relatively small. However, this increment on the voltage of the defective line can cause that stuck-at 0 fault can not be detected. Considering, that the V_{th} voltage of Nmos transistor for $0.18\mu m$ CMOS technology is $0.39V$. The effect of the capacitive coupling on floating line (inverter input) can be interpreted by the CMOS inverter as "1" logic. If we want to detect stuck-at 0 fault, we need to apply a high logic value on the input signal terminal. Other capacitive couplings have been considered, in order to see the effect of different capacitive values. $C_{C_2} = 2fF^2$ and $C_{C_3} = 7fF^3$ capacitances have been simulated under the same conditions. In figure 2.8b it is possible to see the effect of these two capacitances on the floating node. The effect of this two bigger capacitances is clearly well known. The voltage V_{if} reach higher voltages when stimulus signal is applied.

Another important situation to consider is when more than one coupled line influences the voltage at the floating node. For this case, the circuit showed in figure 2.9 for stuck-at 0 fault has been considered. In this case three different coupled signals are influencing to the defective line and 3 different stimulus signals for each coupling have been applied. Simulation results are shown in figure 2.10. Input signals for each coupled line have been applied, considering the capacitive values, the following cases appear:

Case 1.- Consider the effect of all coupling lines to "0" or "1" (desirable condition depending on the fault, SA-0 or SA-1). (1)

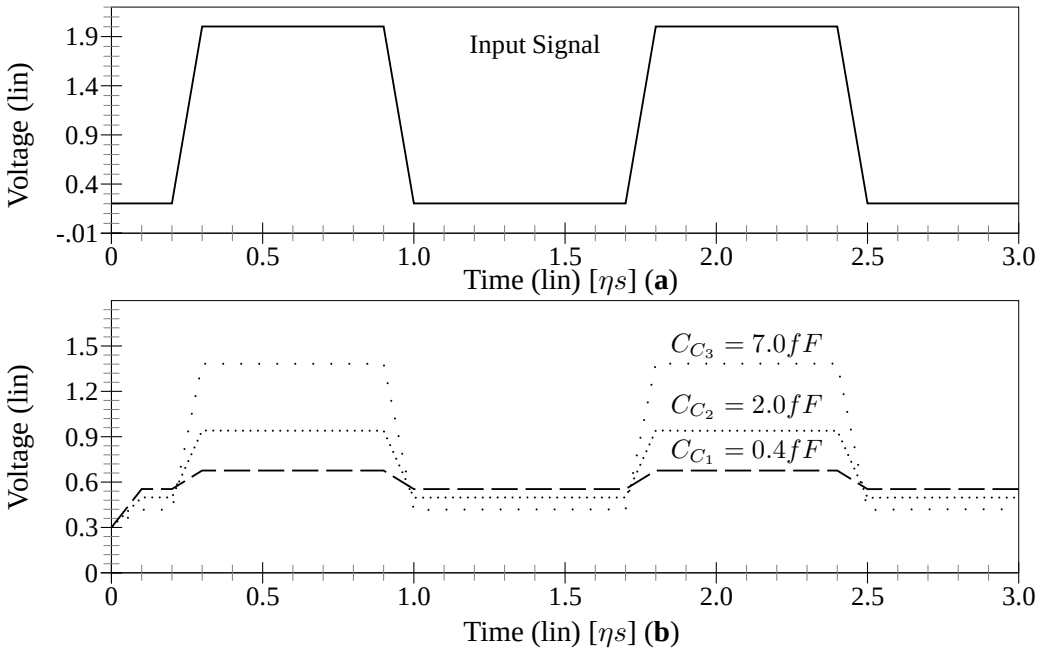


Figure 2.8: Coupling effect on the floating line

Case 2.- Consider the effect of smaller couplings. It is important to identify if couplings that were not considered as critical can influence the voltage at the floating node, and make that defect undetectable. (2)

Case 3.- Consider the effect of high coupling capacitances. (3)

Case 4.- Consider the non-favorable conditions of all capacitive couplings at same time (non-desirable condition). (4)

Voltage V_{if} from 0 to $0.5\ \eta s$ is due to the parasitic capacitances and power supply voltage (see figure 2.10 (plot **e**)) (1). During this time the voltage on floating node is low, however when coupling signals of C_{C_1} and C_{C_2} (plots **a** and **b**) change from 0 to 1 this value is increased (2). Capacitive values of $C_{C_1} = 0.4fF$ and $C_{C_2} = 2.0fF$ influence the voltage on defective line producing an increase. In this lapse of time ($0.5\eta s$ to $1.0\eta s$) we can see the effect of two capacitive couplings with non favorable coupling signal to detect stuck-at 0 fault. In spite of, these two capacitive couplings (C_{C_1} and C_{C_2}) (plots **a** and **b**) are not highest couplings. Signal of capacitive coupling $C_{C_3} = 7fF$ (plot **c**) present the case when coupling signals have not been generated favorable. In this case, it is possible to see that two of the three coupled signals (C_{C_1}

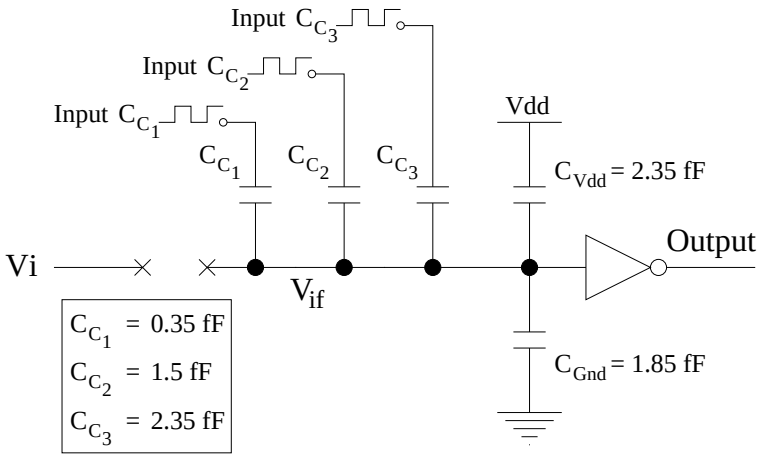


Figure 2.9: Stuck-at 0 fault with 3 coupled lines

and C_{C_2}) have been generated favorable. However, C_{C_3} (plot **c**) present a non-favorable coupling signal, producing an increase on the floating node voltage. This influence can be seen at lapse of time from $0.9\eta s$ to $1.5\eta s$ (3). Due to influence of C_{C_3}, V_{if} reach $1V$ approximately. Finally, the case when none coupled signal have been generated favorably is showed in figure 2.10**e** (4). In this case influence of all capacitive couplings (voltage induced) is reflected on defective line. It is possible to see that V_{if} voltage is $1.2V$ approximately. Voltage induced on floating node, due to the effect of coupling signals, produce that the output inverter change from "1" logic to cero during (4) see plot (**d**). It is important to take account the number of coupling lines that have been generated favorable. The relation of capacitive values with the number of couplings generated favorably is an important measure that we will see in chapter 4.4.2. Simulation results show the importance to get the most favorable test vectors. This condition is achieved when all the couplings lines can be forced to logic states that help to fault detection.

2.4 Sensitization gates

In this section, the detectability conditions for interconnection opens considering that not all the gates affected by the open are sensitized, is investigated. Different simulation results considering non sensitized gate are presented. The effect of non-sensitized gates with different conditions are considered.

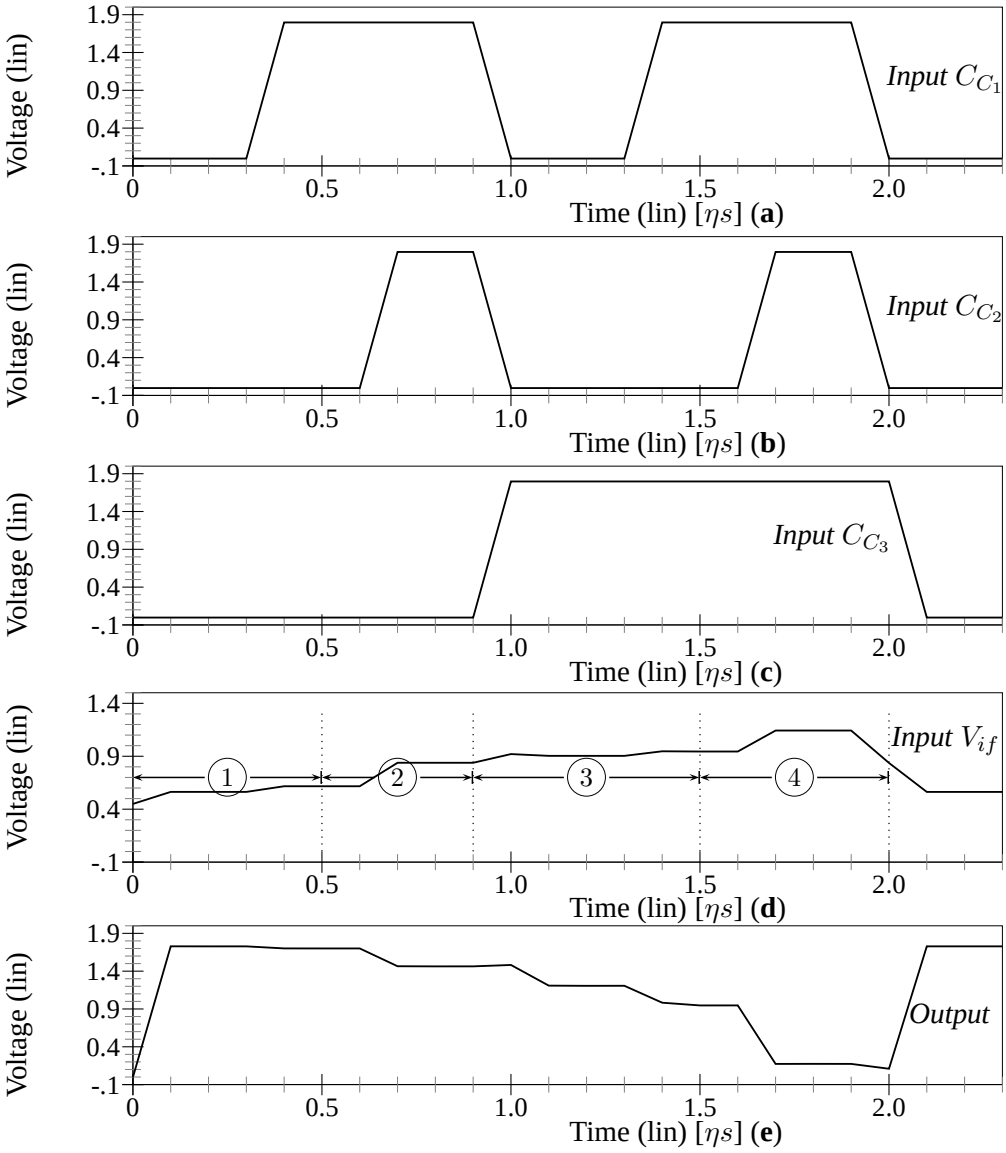


Figure 2.10: Different coupled lines for stuck-at 0 fault.

2.4.1 Topology of an non-sensitized gate

Non-sensitized gates can appear as a consequence of the applied input vector. Due to the unsensitized gates the voltages at the drain/source terminals of the transistors of the affected gates are unknown for the actual input vector. This impacts the charge at the gate of the affected transistors. Hence the detectability regions of the interconnection

opens are also impacted. A circuit with sensitized and unsensitized gates is shown in figure 2.11. Figure 2.11 shows four gates affected by the interconnection open. Two of them, inverter and Nor gates are sensitized by the input vectors. However, the Nand on the input Nor gates (see Figure 2.11) remain unsensitized for the applied input vector. For the sensitized gates the power supply and ground are connected through the defective transistors (see Figure2.12 (a)).

Analytical expressions are used to determine the testability regions of interconnection opens (see section 4.4.3). These regions are defined by two voltages at the floating node: a)$V_{if} = V_{TN}$ and b)$V_{if} = V_{DD} - |V_{TP}|$.

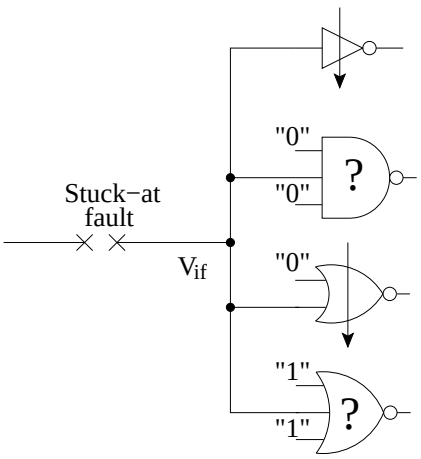


Figure 2.11: Sensitized and unsensitized gates

For sensitized gates, using the two previous conditions it can be known the voltages at the drain-source terminals of the transistors affected by de open. Using this, the charge of the floating transistors are estimated. For unsensitized gates, the voltages at the drain-source terminals may depend on the history of the gate. This is shown in figure 2.12 (b) for a three input Nand gate. The voltage at node V_X can not be determined by the actual input vector.

A schematic representation of a CMOS circuit with transistors affected by the open is given in figure 2.13: The Nmos and Pmos networks can be composed of series-parallel connected transistors it is assumed that the input vector do not sensitized the open. Because this, the voltages at the drain-source terminals of the transistors affected by the open are unknown. These conditions will be considered in the proposed capacitive model of the interconnection open. The resulting topology is shown in figure 2.13.

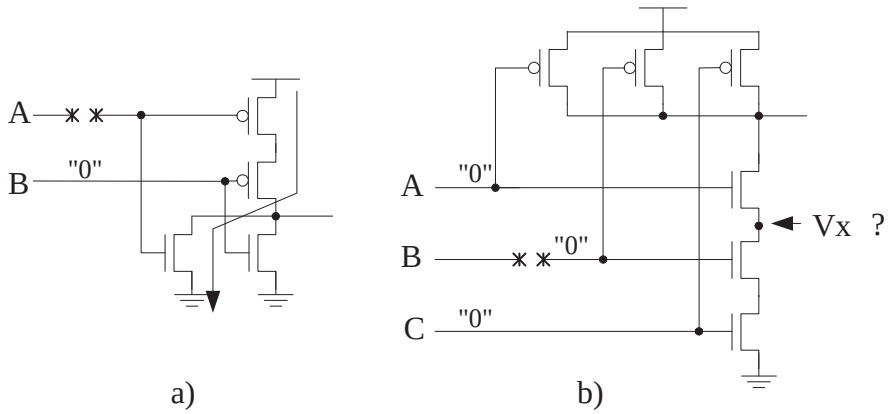


Figure 2.12: Example of sensitized and unsensitized gates.

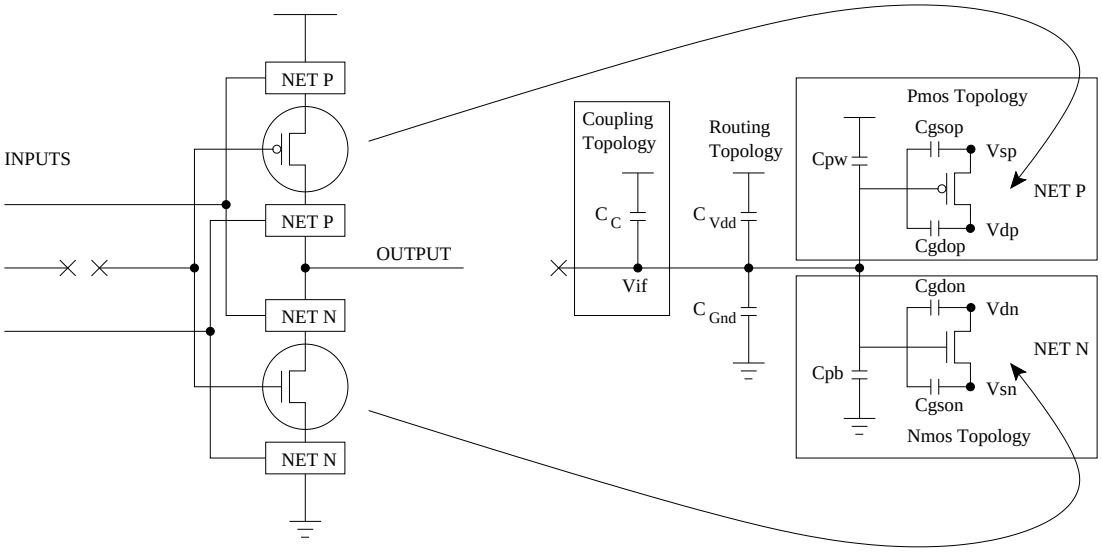


Figure 2.13: Capacitive model for Pmos, Nmos general unsensitized network [70].

Figure 2.14 shows a circuit with inverter gate sensitized and nand3 gate depending on its input. The floating node presents a capacitive coupling to C_C. It has been considered a capacitive value $C_C = 2fF$. Different input signals are applied for Nand3 inputs, and capacitive coupling line. Simulation results for a stuck-at 0 fault are depicted in figure 2.15.

Nand3 inputs are showed in plots a) and b). Coupling signal is depicted in plot c). Voltage V_X is showed on figure 2.15 (see plot (d)). Floating node voltage (V_{if}) is depicted on plot (e). Finally nand3 output is showed in plot (f). For voltage V_X it can be seen that the input vector A=0, C=0 and coupling signal C_C=0 produce a low voltage

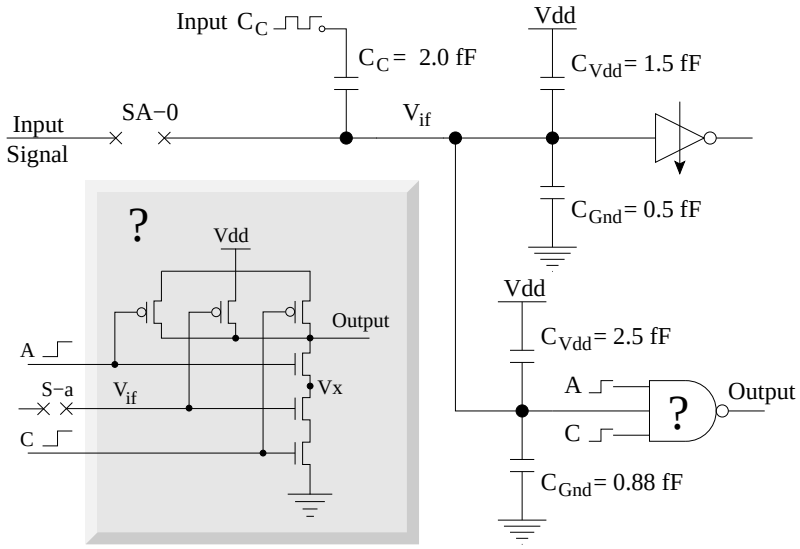


Figure 2.14: Sensitization and unsensitization gates effects.

level in V_X and V_{if}. Then, A=1, C=0 and C_C=1 produce an increase of voltage on V_X node and V_{if} node. This is due to a path from G_{nd} to V_X node (lapse time from 0.5ηs and 1ηs). The floating node voltage (V_{if}), in the same lapse of time, presents a voltage of 1 volt. This voltage is produced for the high voltage value on the coupling signal.

The highest voltage at the node V_X appears when input A has a high state and the input C is at logical 0, under this condition a path from the nand3 output to the node V_X appears, charging this node (lapse of time from 0.5η s to 1.0η s). Input vector given from $1.0\eta s$ to $1.5\eta s$ cause a decrement of voltage V_X. Next input vector A=1, C=1 and coupling signal C_C remain to high voltage value, produce a strong increment on V_X. However, these conditions do not allow that node V_{if} be considered like "0" logic. If we want to detect a stuck-at 0 fault, and under these conditions it could be difficult to detect, due to the high voltage present on V_{if}. This voltage can make that nand3 output could be considered like "0" logic. Hence, avoiding to detect the stuck-at 0 fault. Nevertheless, voltage V_X depends strongly on the history of the gate inputs. Voltage V_X can vary widely and depending on the different conditions (input vectors, coupling signals, capacitive values) produce sensitization or un-sensitization gates. Because of this, it is important to considered the effects of sensitized and unsensitized gates.

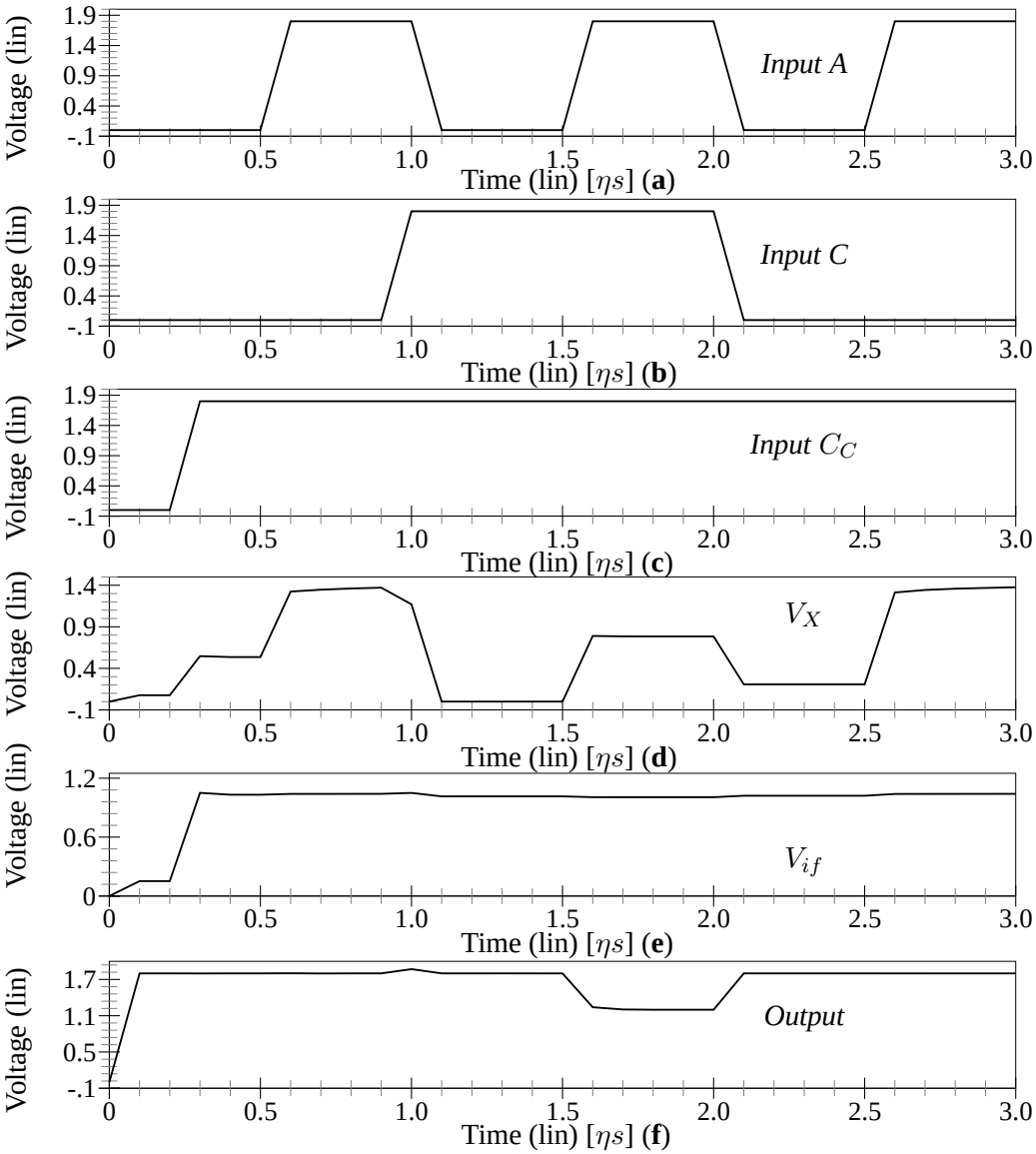


Figure 2.15: Simulation of Sensitized and unsensitized gate effects.

2.5 Trapped gate charge

Another important factor influencing the voltage at the floating node is the trapped gate charge Q_{tr}. This trapped gate charge is deposited during fabrication process. The behavior of the interconnection open defect is determined by the structure of the affected devices, the trapped charge on the floating node and the coupling capacitances related to the floating node [38, 42, 43, 53, 54, 56, 71, 91]. It has been found that the trapped

charge influences significantly the behavior of interconnection opens [41, 44]. Some circuits with this defects may work logically correctly at low frequencies, but fail at higher frequencies [38, 54]. Other researchers have observed a stuck-at behavior and negligible quiescent current values for an inverter with a given interconnection open defect [91]. Makki et al. [66] have made measurements on intentionally-designed defective circuits. They have found defect coverages of 90.9% and 90.6% for I_{DDQ} and transition fault logic testing, respectively. Konuk [42] have analyzed the testability of interconnection opens under a voltage (stuck-at) and current based test. Using Spice pre-simulations and analytical expressions the detectability of interconnection opens is investigated. Interconnection opens may also present oscillations and sequential behavior [43] under certain conditions. The influence of the coupling signals in the test of opens by delay testing is analyzed by Moore et al. [53]. The detectability of full opens in the interconnections assuming certain conditions at the coupling signals is analyzed by Zenteno et al. [71]. The expression that describes the voltage at floating node including the trapped gate charge term Q_{tr} is as follows, the other terms will be defined on section 4.4.1:

$$\begin{aligned} V_{if} &= \frac{C_{pw}^T V_{DD}}{C_T} + \frac{C_r^1 V_{DD}}{C_T} - \frac{Q_{GT}^T}{C_T} + \frac{(C_{gsop}^1 V_{1P} + \cdots + C_{gsop}^n V_{nP})}{C_T} \\ &+ \frac{(C_{gson}^1 V_{1n} + \cdots + C_{gson}^n V_{nn})}{C_T} + \frac{(C_{gdon}^1 + C_{gdop}^1)V_{O1} + \cdots + (C_{gdon}^n + C_{gdop}^n)V_{On}}{C_T} \\ &+ \frac{C_{C1}V_{C1} + \cdots + C_{Cn}V_{Cn}}{C_T} + \frac{Q_{tr}}{C_T} \end{aligned} \tag{2.1}$$

Where:

$$C_T = C_{gson}^T + C_{gdon}^T + C_{gdop}^T + C_{gsop}^T + C_{pw}^T + C_{pb}^T + C_r^0 + C_r^1 + C_{C_1} + \ldots + C_{Cn}$$

$$C_{gson}^T = \sum_{n=1}^{t} C_{gson}^n \qquad C_{gsop}^T = \sum_{n=1}^{t} C_{gsop}^n$$

$$C_{gdon}^T = \sum_{n=1}^{t} C_{gdon}^n \qquad C_{gdop}^T = \sum_{n=1}^{t} C_{gdop}^n$$

$$C_{pw}^T = \sum_{n=1}^{t} C_{pw}^n \qquad Q_{GT}^T = \sum_{n=1}^{t} Q_{GTN}^n + Q_{GTP}^n$$

In equation (2.1) can be observed the terms related with the effect of the sensitized and unsensitized gates. Where V_{1P} to V_{nP} are the *source* voltages for every PMOS transistor, V_{1n} to V_{nn} are the *source* voltages for every NMOS transistor and V_{O1} to V_{On} are the common voltages at drain terminal between PMOS and NMOS transistors.

Nand 2 gate have been considered to simulate the effect of trapped gate charge (Q_{tr}). From this, initials voltages for nand2 inputs have been proposed. Coupling signal at input "B" has been applied. Figure 2.16 shows a nand2 gate with one capacitive coupling at its input "B". Simulation results are depicted in figure 2.17.

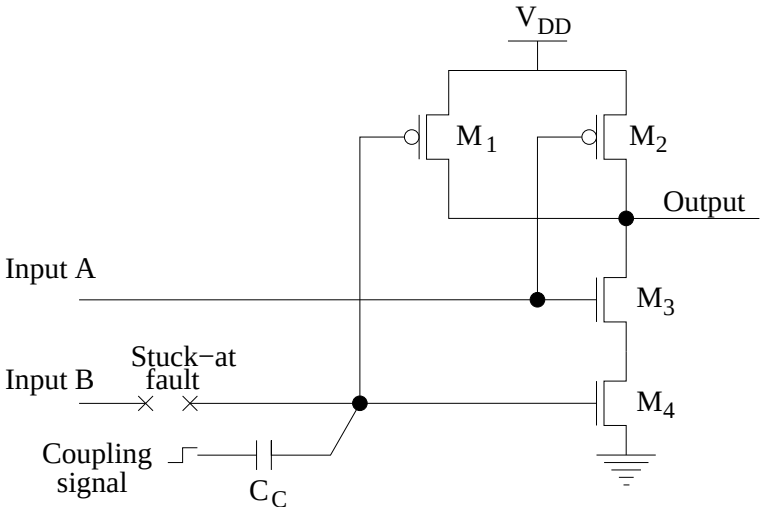


Figure 2.16: Trapped gate charge effects in nand2 gate

The first case to consider is when both inputs (*A and B*) are to zero logical. From this, it can be seen the voltage of *input A* on plot (a) (see figure 2.17) goes from cero to almost 0.3 volts. However, the voltage of *input B* follows coupling signal due to capacitive coupling. In spite of, input B is interpreted like "1" logical (*some periods of time*) by the M_4 (nMOS gate), input A is considered like "0" logical all the time. These conditions set, the transistor M_3, OFF and allow to the conduction through the transistor M_2. Therefore the nand2 gate output, plot (d), always present a high voltage. Even though, the nand2 gate inputs have been fixed to zero volts, present an increase from the beginning of simulation.

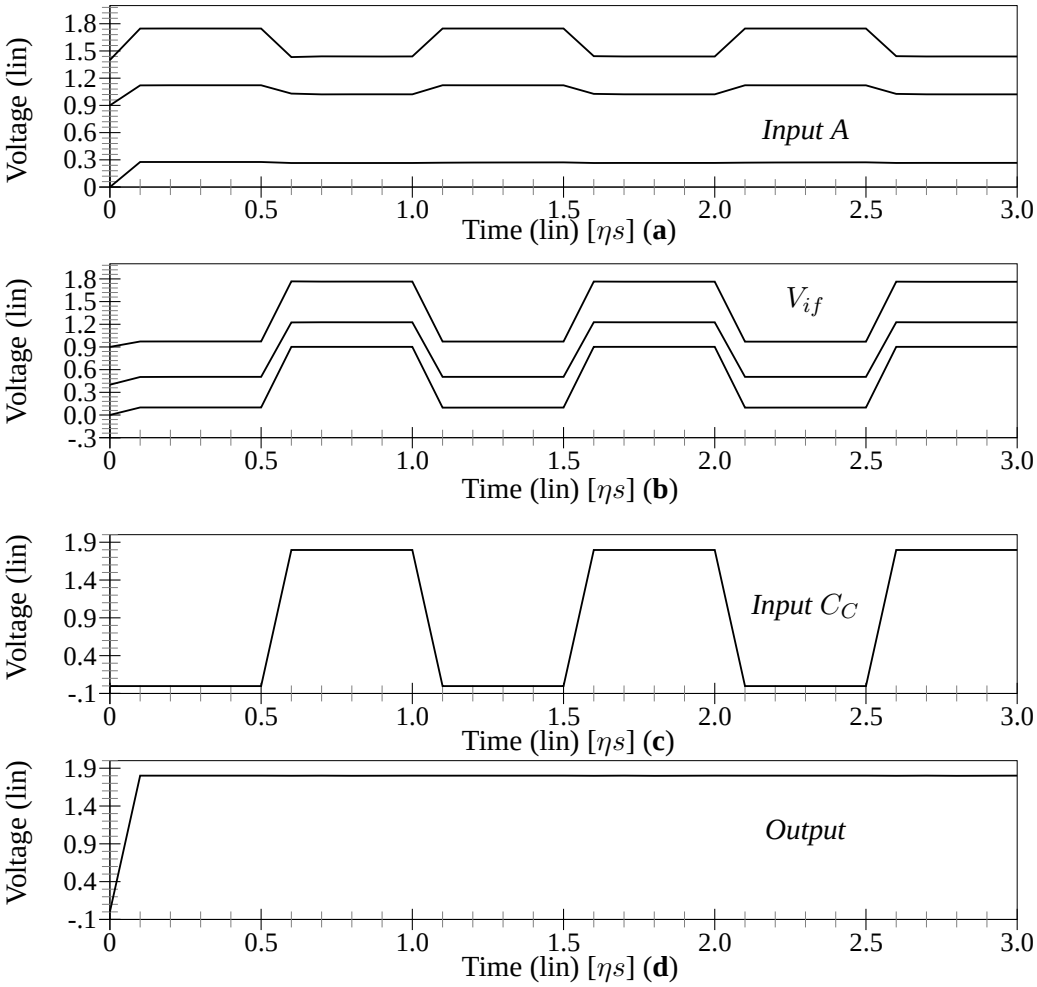


Figure 2.17: Trapped gate charge effects, Input A=0 V, Input B=0 V.

2.6 Proposed test framework for interconnection opens

It has been demonstrated that there is a high probability in VLSI circuits that interconnection opens exist [94]. For example, the great amount of Vias in modern circuits can cause that faults happen [10] [30], due to the several levels of metal and to the same complexity of the circuit [81]. Due to the scale of the technology some tendencies will affect the present methods of test [59] [4]. Some faults can escape to the used conventional methods. Of such form that will be more and more necessary to use non-conventional methods of test [61] [47]. These methods must allow to obtain in addition a high fault coverage, quality, minor cost and reduced times of test.

In this work large breaks are considered so there is non-significant influence from the input signal over the floating node. Actually high resistive opens are also covered. Further research will be devoted to define more clearly the detectability of these opens. The proposed test framework for interconnection opens is shown in figure 2.18.

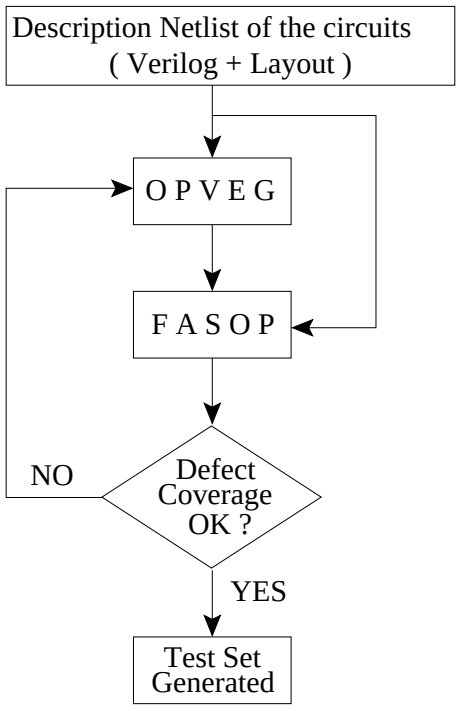


Figure 2.18: Proposed test framework for interconnection opens

Two CAD tools are proposed in this work. OPVEG is a tool to generate favorable test vectors for interconnection open defects. FASOP is a fault simulator for these opens. OPVEG generates test vectors in two stages. It attempts to generate favor-

able test vectors for the most favorable conditions at the coupling signals for a given selection factor. If the defect coverage evaluated by FASOP is adequate the process ends. Otherwise, OPVEG attempts to find a test vector for another selection factor. In other words, it attempts to generate a test vector considering lower values of coupled capacitances.

Chapter 3

Opens vector generator (OPVEG)

3.1 Introduction

In this chapter the basic design of a CAD tool called OPVEG (Opens Vectors Generator) oriented to generate favorable test vectors for opens is presented using data obtained from layout and circuit logic description, favorable test vectors considering capacitive couplings between adjacent nodes are obtained. These vectors can be used to improve the detectability of interconnection opens.

The operation of the tool is based on the extraction of parasitic capacitances of a circuit, ordering of data, calculation of parameters and generation of test vectors considering coupling effects. This is obtained from the interaction of two commercial CAD tools (CADENCE [14]) and TetraMAX [79]. With the information obtained from the extraction of electrical parameters of the designed circuits it is carried out an analysis based in methods and models proposed on this work which are used to filtrate, to process and selection of information through different routines. Since it has been observed, the capacitive effects between interconnection lines of a circuit can cause negative effects in the tests of integrated circuits when using the model of faults *stuck-at*. Nevertheless this situation can be improved looking for the suitable conditions so that the fault coverage is affected in smaller amount by capacitive effects. These depend on the controllability and observability that has of them.

The designed CAD tool has the possibility of generating these favorable conditions if previously they are established. The generation of test vectors uses conditions or restrictions (*constraints*) that define the logical states that some nodes of the circuit

must fulfill to generate favorable test vectors. Within this generation process cases of partial controllability or noncontrollability may appear. Hence vectors that do not fulfill the favorable conditions totally or cases where they no can be generated appears. In addition, the conditions for the generation of test vectors are shown. Effects of different coupled lines from a floating node are explained [19] [52] [69]. The basic form of the algorithm doing a search combinations of critical couplings is showed as well as the detection ranges.

Results of tests made to four circuits ISCAS'85 using OPVEG tool are presented. Comparative tables between conventional ATPG and OPVEG tool of defect coverage and times of calculation are shown.

3.2 Vector detection conditions

Testability is a characteristic that influences in several costs associated with the tests of circuits. DFT (Design for Testability) Techniques imply a design effort to improve test characteristics of a device of circuit. Two important attributes related to the testability exist: controllability and observability [3]. Controllability is the capacity to establish the specific value on a signal of each node of the circuit applying values at the primary inputs. Observability is the ability to determine the value of the signal at any node exciting the inputs of the circuit and observing the output(s). In general, a node of a circuit has low controllability if it requires a unique input vector to establish the state of that node. A node also has low controllability if an extensive sequence of inputs is required to establish its logical state. Circuits that are typically difficult to control are decoders, circuits with feedback, oscillators, and clock generators. A circuit has a poor observability if it requires a unique input vector of test or an extensive sequence of test vectors to propagate the state of one or more nodes to the outputs of the circuit.

A possible interconnection open defect at the floating node can be influenced by different coupled lines. The figure 3.1 shows the input of an inverter.

Let's use a boolean test method based in the stuck at fault model to detect this open. The fault must be sensitized and propagated a primary output. The logic state at the coupled lines influence the voltage at the floating node. Hence the detection of the open can be missed depending on the value of this voltage. Because of this the logic states at the coupled lines influences significantly the open. Therefore the process of generation of the vector becomes more complex. The possible vectors of excitation for

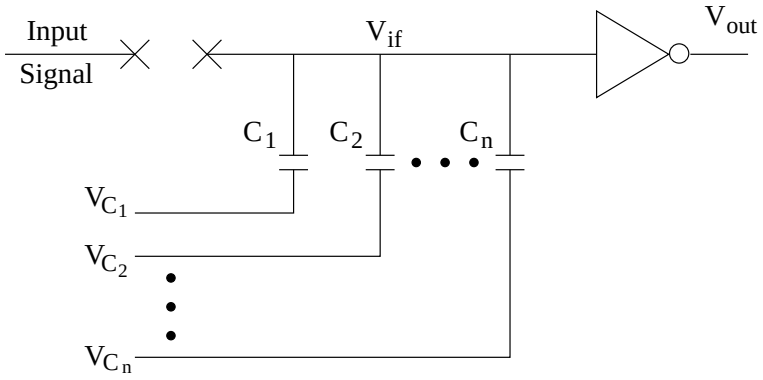


Figure 3.1: Floating node with multiple coupled lines

stuck-at fault model depend to a great extent on the topology of the circuit. The possible test vectors, considering that the coupled lines can be controlled simultaneously to 1 or 0 are shown in table 3.1. The detection ranges [70] are also showed.

Input Signal	$V_{C1}...V_{Cn}$	Detectable range V_{if}	Fault
0	0	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
0	1	$[V_{DD} - \|V_{TP}\|, V_{DD}]$	SA-1
1	0	$[0, V_{TN}]$	SA-0
1	1	$[0, V_{TN}]$	SA-0

Table 3.1: Possible test vector condition

All the test vectors for the detection of a fault that appearing in the previous table can be generated. However differences in the conditions of each of them exist although they are destined to detect the same fault. For a Stuck-at 1 vector high levels on the signals V_{cn} help to detect stuck-at 1 faults at the floating node because in this case the voltage at the floating node tends to a higher value. Nevertheless, low levels would help to a behavior without fault; that would cause in some cases that the open does not detected. Similarly, for a stuck-at 0 fault the favorable value of V_{cn} to detect would be 0. High logic levels do not favor the defect detection.

Let's show an example (See figure 3.2). In order to detect stuck-at 0 fault it is necessary to apply logical "0" at the input inverter. This would cause a high logic level on the faulty line with that would allow its sensitization. The open is detectable if the voltage at the floating node is sufficiently low that is interpreted as logical 0 by inverter 2. This voltage must be in the range [0, V_{TN}] (see Table 3.1) to guarantee that it is interpreted

like 0 logical. It is observed that the adjacent lines (aggressor Lines) present a coupling with the floating line. The capacitive couplings may play an important role in the open detection because they induce voltage at the line with the open. As a consequence the line does not remain in zero logic although exists an open defect and a logical level 1 is obtained. This would cause that the output of inverter 2 goes to logical 0. Therefore the open is not detected because of this favorable conditions should be applied at the coupled lines to increase the likelihood of detection of the open. Most favorable conditions to detect the open would occur when having a zero logical in the adjacent lines as is observed in figure 3.2.

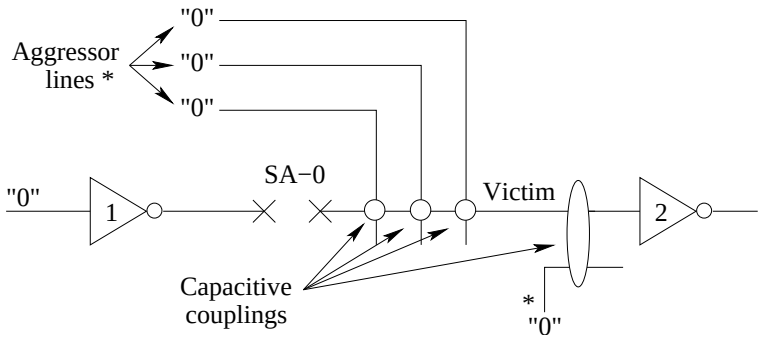


Figure 3.2: Effect of capacitive couplings

Candidated lines (victim) are those line with its coupled lines can be obtained from layout information. However, it is not necessary to consider all the lines of a circuit. The strengths of the drivers handling a line under analysis and the coupled lines are not important when a full interconnection open is considered. ***Critical nodes*** are those lines that have at least one coupled line of capacitive value greater or equal than the sum of this capacitive values of the line to G_{ND} and V_{DD} multiplied by a factor. Then, the ATPG tool attempts to obtain an input vector forcing (*constraint*) proper input values at the coupled signals of the selected critical lines. Conditions are only imposed on those coupled lines with significant coupling capacitance. A simple algorithm is used for running ATPG for the different constraints of a critical line. The algorithm gives priority to the signals with higher coupling capacitance [1]. The used algorithm is presented with more detail in appendix B.

When attempting to generate a test vector situations can be presented where the generation of favorable vectors is not possible or partial [69–71]. As follow some of the possible situations are analyzed next.

- Full controllability.
- Partial controllability.
- Non Controllability.
- Non Observability.

3.2.1 Full controllability

For this case all the logical states of the coupled lines can be set to the desired states. As it was depicted in figure 3.2, the floating node presents a stuck-at 0 fault, favorable condition that help to detect is when all the coupled lines can be set to logical 0. This is called full controllability.

3.2.2 Partial controllability

In this case, not all the coupling signals can be controlled simultaneously at 1 or 0 logic. Hence some of the most favorable conditions (see table 3.1) to test the interconnection opens can not be generated. A simple circuit illustrating a situation where controllability for certain conditions can not be generated is shown in figure 3.3.

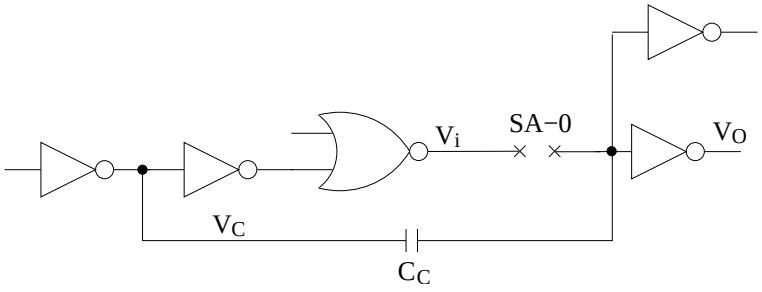


Figure 3.3: Partial controllability case [69]

For this circuit, the vectors V_i V_C=00, 01, 11 can be generated. However, the vector V_i V_C=10 can not be generated. It must be noted that this vector is the mos favorable condition for a stuck-at 0 fault at the open.

3.2.3 Low controllability

In this case the two most favorable conditions of table 3.1 can not be generated. A circuit example is shown in figure 3.4.

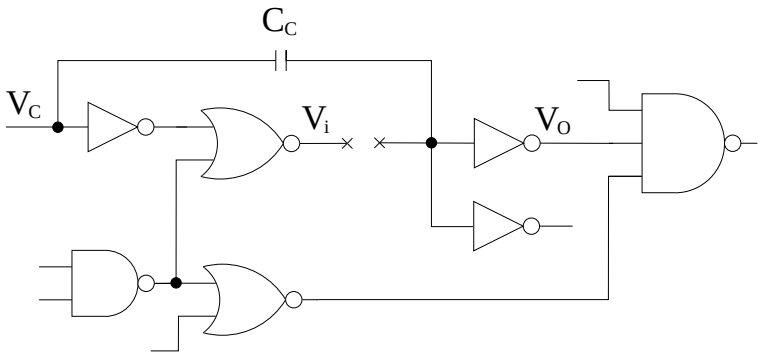


Figure 3.4: Non controllability case [69]

For this circuit, the vectors that establish the following values $V_iV_c = 00, 11$ can be generated. Nevertheless, the most favorable vectors for $V_iV_c = 01, 10$ can not be generated.

3.2.4 Non observability

In this case the effect of the open can not be propagated with the most favorable condition. Next an example of non-observability is shown. Consider the following circuit (figure 3.5).

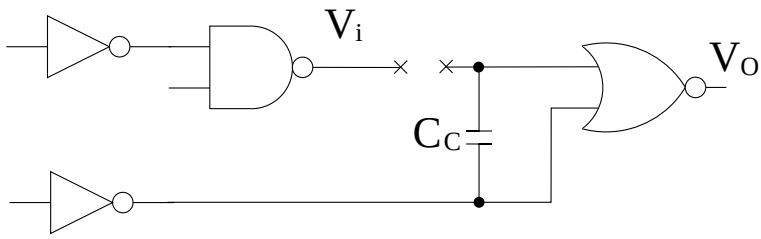


Figure 3.5: Non observability case [69]

For this case, all the combinations V_iV_c can be controlled (00, 01, 11, 10). However, the most favorable vector for a test *stuck-at 1* at the open is $V_iV_c = 01$, which will make to the output gate V_O to remain in "0" independently of the value of V_i. In this case V_iV_c is possible to control the values but the behavior of a fault cannot be observed. Using $V_iV_c = 00$ will be able to be detected the fault, but it will not be adequate considering possible capacitive couplings, reason why also the detection probability will be reduced.

3.3 OPVEG Tool description and flow algorithm

It has been developed a test framework, called OPVEG, to obtain favorable test vectors for interconnection open defects in the presence of coupling signals. It also allows to identify those critical cases which have non-favorable conditions. Using this information, DFT techniques can be applied for improving detectability for interconnection open defects. The signals at the coupling lines may have a high logic value (V_{DD}) or low logic value (GND). The value at the coupling signal impacts significantly the detectability of the interconnection open defect. Let's consider the circuit shown in Figure 3.6. For testing an Stuck-at 0 at the interconnection open, a value of 0 logic at the coupling signal favors detection of the open defect. This is because the coupled signal(s) pulls to a lower level the voltage at the floating node. Hence, the signal can be interpreted as a low logic level which is the wrong logic value. In the other hand a value of 1 logic at the coupling signal makes the open more difficult to detect. This is because the coupled signal(s) pulls to a higher level the voltage at the floating node. Hence, the signal can be interpreted as a high logic level which is the correct logic level. The same is true for testing an Stuck-at 1 at the interconnection open but the logic values are opposite.

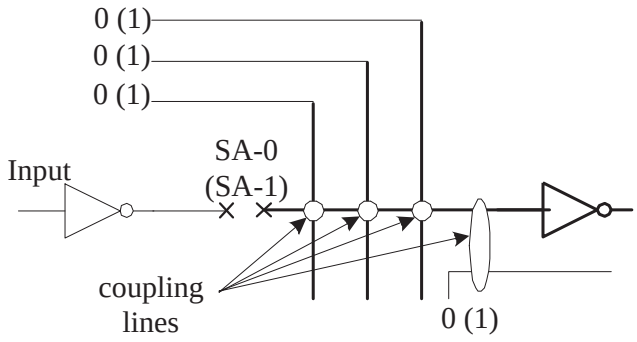


Figure 3.6: Favorable signals coupling influence for detection of an interconnection open

A simplified flowchart of OPVEG tool is given in Figure 3.7. OPVEG uses information obtained from a circuit layout and a commercial ATPG tool.

The input files are the Verilog circuit description, coupling extracted capacitances and node equivalences between the Verilog and Cadence files. The coupling capacitances have been obtained from the circuit layout using Cadence design tools. In the first step (See Figure 3.7) the coupling capacitances to each node are identified. Also,

the capacitances of each node to VDD and GND are obtained. In second step, the critical nodes affected by significant values of coupling capacitances are selected. The nodes influencing to the critical nodes are also identified. In the third step, Tetramax ATPG tool is run for the selected critical nodes imposing constraint values for the signal values coupled to the critical nodes. The constraint values correspond to the most favorable conditions to detect the interconnection opens. In this way a test vector set for testing interconnection opens under favorable conditions is obtained. This set of vectors complements the set obtained using conventional ATPG.

The code of the program was made in language C (structured) in an operating system Solaris Version 5.8 (UNIX atmosphere) with a compiler GCC version $2.95.1$. The program is made up of several subprograms that are executed in sequential form. Within the process archives with commands are generated to manipulate in automatic form tool the CAD tool used for the generation of test vectors (TetraMAX).

In order to better understand the developed CAD tool (See Figure 3.7), the different steps of the simplified OPVEG flowchart are further explained. The generated files and some of the subprograms and routines that composes the complete system are described. Some of the required input files for the operation of the tool are obtained from the extraction of electrical parameters and generation of netlist of layout of the designed circuits. Another input file is the netlist description in high-level language (Verilog) of the circuits. In summary, the input information is made up of three files.

- List of capacitive connections between nodes of circuit (netlist).
- List of equivalences between real nodes of the circuit and labels assigned by the generator of netlist (Spectre).
- Description of the complete circuit in Verilog language. This circuit description is used by the design and ATPG tools.

Let's further comment the three main steps shown in figure 3.7.

STEP 1.- The first step in the flow of the tool, is the ordering of the information. A subprogram makes ordering and format of the netlist. This uses the list of equivalences of the nodes to classify the information stored in the list of couplings of the circuit. Three files are obtained:

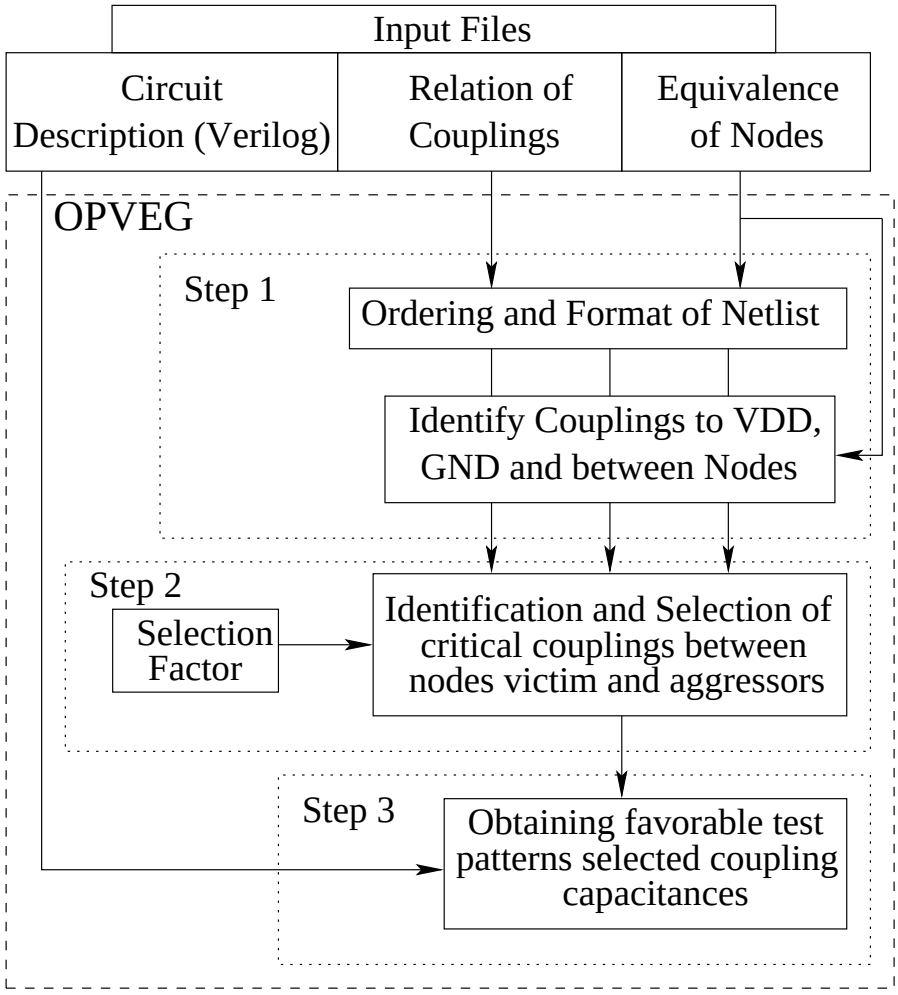


Figure 3.7: Simplified Flowchart of OPVEG

- One file contains the nodes with couplings to V_{DD}.
- The second the nodes with couplings to G_{ND}.
- The third files contains the couplings between non-global nodes.

In this step it is also made the replacement of the labels that are assigned in the creation of netlist (CADENCE extraction) by the real names of the nodes (original in Verilog and used by CADENCE at schematic level). Those nodes that correspond to internal points of logic gates are not considered.

STEP 2.- In the second step, the critical couplings between victims and aggressors nodes are identified and selected. The critical nodes (lines) are those that have at least one coupled line with its capacitive value greater or equal than the sum of the capacitive values to G_{ND} and V_{DD} multiplied by a "***Selection Factor***". The critical nodes are considered for attempting to generate a favorable test vector. In this step an output file containing the list of nodes victim with its corresponding aggressors is obtained. Only those critical nodes according to the selection factor appear on this file.

STEP 3.- In this step, test vectors with favorable logic conditions at the coupling signals are obtained. In the previous step the critical nodes (lines) and also the couplings of these nodes are obtained. Using *TetraMAX* a test vector is obtained for each critical lines forcing favorable constraints at the coupling signals. A simple algorithm is used for running ATPG for the different constraints of a critical line. The algorithm gives priority to the signals with higher coupling capacitance [1]. This is further explained in the next subsection. A list of test vectors for faults *stuck-at-0* and *stuck-at-1* of those nodes considered as critical is obtained.

3.4 Experiments and results

OPVEG has been used to obtain favorable test vectors for interconnection opens in four $ISCAS'85$ benchmark circuits. These circuits have been designed using standard design layout techniques [1]. *Chip Assembly Router* from Cadence [14] has been used for automatic place and route. First, a conventional ATPG has been run for the four ISCAS'85. The ATPG is run for the selected critical nodes imposing the favorable conditions in the signal values coupled to the critical nodes. Different selecting factors

have been considered. In TetraMAX [79], the default number for maximum number of allowed iterations has been used. For analyzing the results metrics for OPVEG have been defined. These are explained next:

Critical (lines) are those lines that have at least one coupled line of capacitive value greater or equal than the result of multiplying a factor (**Selection Factor**) to the sum of the capacitances to Gnd and V_{DD} of the floating line. In other words for a line to be considered as critical one of its coupled lines must satisfy.

$$C_C^{CL} \geq f(C_{GND}^{CL} + C_{V_{DD}}^{CL}) \tag{3.1}$$

- **Possible Faults**.- Is the maximum number of considered faults obtained for a given selection factor.
- **Generated Vectors**.- Vectors generated with at least one favorable condition.
- **Vectors 100% Ok**.- This metrics gives the number of vectors generated with all the favorable conditions. For a specific line with some coupling lines (aggressors) obtained for a " selection factor ", all the coupled lines had logic states that help to detect the open.
- **Repeated Vectors**.- One favorable vector can be able to cover more than one fault. This vector would be repeated in the set of favorable vectors in case of covering several faults. Nevertheless, it is necessary to consider only a single vector for all these faults. Repeated vectors is the set of vectors for those faults having already generated a favorable test vector.
- **Vectors Contained in conventional test**.- The vectors generated with OPVEG tool can also appear in the set of vectors obtained from the conventional ATPG process. The vectors that already are contained in the set of conventional vectors of test can be deleted in the set of vectors obtained with OPVEG tool.
- **Compacted vectors**.- This set of vectors is obtained eliminating repeated vectors and vectors that already contained in the set of vectors obtained with conventional ATPG.
- **Percentage of aid to the conventional test**.- The conventional test of circuits needs a certain set vectors. This set of vectors has a certain coverage of faults

(Above of 95% in the analyzed circuits) for the total faults. The capacitive effects can cause non-detection of faults or a reducing the actual coverage. According to this, the the number of faults that can be seen affected in a conventional test is obtained, the corresponding percentage of conventional coverage is also obtained . It is considered that this percentage will be covered by the vectors generated with OPVEG (Percentage of Aid). The amount of faults covered by OPVEG corresponds to the number of vectors obtained by OPVEG, without deleting repeated vectors, and do not taking into account the conventional test vectors. This percentage of aid is obtained with the following expression.

$$Percentage \quad of \quad Aid = C - \left(\frac{(TF - FC)C}{TF} \right) \tag{3.2}$$

Where
TF: Total number of faults stuck-at of the circuit.

C: Conventional coverage of faults.

FC: Total faults covered considering OPVEG capacitive couplings (Number of vectors generated with OPVEG).

- **Time of selection of nodes**. Is the time that takes the tool (OPVEG) to select all the victim and aggressor nodes of the circuit depending on the *selection factor* provided by the user.

- **ATPG Time**.- It is the amount of time that OPVEG uses to make the ATPG considering capacitive couplings. Besides to consider the time that takes ATPG program (TetraMax) in generating vectors, it takes into account the file generation of control for ATPG tool; generation, reading and analysis of output archives and selection of vectors with the most favorable conditions.

3.4.1 Logic Effectiveness

Logic Effectiveness.- This definition gives a metric about how successful is the process of test generation for all the considered critical lines and favorable constraints in all the considered coupled signals. It is calculated as follows:

$$Log_{eff} = \frac{\sum_{n=0}^{t} \frac{G_n}{P_n}}{t} x100 \tag{3.3}$$

where:

G_n: is the total number of couplings of a critical line for which it was found successfully a test vector under a favorable constraint.

P_n: is the total number of couplings of a critical line.

t: is twice the total number of critical lines. Note: a vector is generated for every critical line for both stuck-at 0 and stuck-at 1 faults.

The results obtained using OPVEG for the four ISCAS'85 benchmark circuits are given in Tables 3.2-3.13. Three tables are given for each ISCAS'85. Tables 3.2, 3.3 and 3.4 shows the obtained results of the C432 circuit. The results of the C499 are presented in tables 3.5, 3.6 and 3.7. In tables 3.8 to 3.10 the results of C1908 are showed. Finally tables 3.11, 3.12 and 3.13 present the results of C2670.

Let's begin with the results for the ISCAS'85 C432 (See tables 3.2, 3.3 and 3.4). In Table 3.2 the row at the top gives the number of faults considered by a conventional ATPG stuck-at (*Total Faults*) process. Different selection factors (from 20% to 100%) have been considered (first column). Data separately for stuck-at-0 and stuck-at-1 faults is given for each selection factor. Also the data considering the total number of possible faults (*stuck- at 0 and stuck-at 1*) is given. Second column gives the number of possible faults for the critical lines according to the selection factor. It is observed that the number of possible faults decreases as the selection factor increases. This is because when increasing the selection factor the value of the coupling capacitances to define a critical line increases.

It has been found than a significant number of vectors (**Generated Vectors**) are generated with at least one favorable constraint at the coupling signal. For the considered selection factors, the number of vectors obtained with all the most favorable test conditions (**Vectors 100$\%$ OK**) are depicted in column 4. This depends on the type of analyzed circuit as you will see in the results given for the other benchmark circuits. The *logic effectiveness* gives a more realistic metric of the impact of the generated favorable constraints. This is high for the analyzed ISCAS'85 benchmark circuits. It can be seen that for a selection factor of the 20% the effectiveness is 84%.

Total Faults = 364				
Selection Factor	**Possible Faults**	**Generated Vectors**	**Vectors 100% OK**	**Logic Effectiveness**
20%	320			
Stuck-at-0		148	82	73%
Stuck-at-1		150	147	95%
Total		298	229	84%
40%	201			
Stuck-at-0		78	66	73%
Stuck-at-1		95	95	94%
Total		173	161	83.5%
60%	88			
Stuck-at-0		34	28	71%
Stuck-at-1		40	39	91%
Total		73	67	81%
80%	52			
Stuck-at-0		20	17	71%
Stuck-at-1		23	23	88%
Total		43	40	80%
100%	32			
Stuck-at-0		13	10	72%
Stuck-at-1		14	14	88%
Total		27	24	79.7%

Table 3.2: Results of Circuit C432 a)

In the second table (See Table 3.3), due to completeness of the tables, is repeated the information of number of **generated vectors** for both stuck-at 1 and stuck-at 0 faults. Depending on the selection factor the number of generated vectors goes from 298 (for 20% selection factor) to 27 (for 100% selection factor). Also, it is given the number of **repeated vectors**. *Repeated vectors* in table 3.3 shows 72 vectors of a total of 298 generated vectors with a selection factor of 20%. These values decrease as the selection factor increase. As it can be seen in the last row, for a selection factor of 100% the number of repeated vectors is 0. Column 4 (*Contained vectors in conventional test*) shows the number of those process vectors generated with OPVEG tool which were

also generated with conventional ATPG. For this case, independently of the selection factor the number of *contained vectors in conventional test* is 0. The number of vectors after compaction (**compacted vectors**) are shown in column 5. The number for compacted vectors goes from 226 to 27 for 20% and 100% of selection factor respectively. Finally, the sixth column contains the *percentage of aid to the conventional test*. It is possible to see that this percentage is between 81.19% and 7.35% for different selection factors.

Selection Factor	**Generated Vectors**	**Repeated Vectors**	**Contained Vectors in Conventional Test**	**Compacted Vectors**	**Percentage of Aid to the Conventional Test**
20%	298	72	0	226	81.19%
40%	173	29	0	144	47.13%
60%	73	2	0	71	19.89%
80%	63	0	0	63	11.71%
100%	27	0	0	27	7.35%

Table 3.3: Results of Circuit C432 b)

In the third table (See Table 3.4) the computer time for obtaining favorable test vector conditions is given. The time data are in minutes and seconds (m:s). For every time of processing (Selection of Nodes and ATPG) is the percentage of use of used CPU. The time of ATPG divides in *stuck-at-0* and *stuck-at-1*. Table 3.4 shows different selection factors in first column. In second column *time of selection of nodes* is depicted. These values (expressed in minutes and seconds m:s) is the time that takes the OPVEG tool to select all the victim and aggressor nodes of the circuit. The third column gives the percentage of CPU usage that correspond at the time of ATPG. Time of ATPG is divided in *stuck-at-0* and *stuck-at-1*. It is possible to observe for selection factor of 20% correspond 16:11 (m:s) of time of ATPG. As the selection factor increases the time of ATPG decreases. This is because the number of nodes considered as critical is smaller for a high selection factor (100%) than the number of nodes considered as critical for a low selection factor (20%). It can be seen in columns 5 and 7 the CPU usage time of ATPG. This value increases when the selection factor decreases. The percentages goes from 93% (Selection factor 20%) to 89% (selection factor 100%) in column 5. In column 7 the percentages of CPU usage of stuck-at 1 is between 92% and 76%.

Results for the C499 ISCAS'85 are showed in tables 3.5, 3.6 and 3.7.

Selection Factor	**Time of selection of Nodes (m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-0(m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-1(m:s)**	**CPU Usage**
20%	00:42	47%	16:11	93%	06:09	92%
40%	00:57	34%	04:15	92%	03:22	92%
60%	00:45	45%	01:59	90%	01:31	92%
80%	00:45	43%	00:65	89%	00:41	85%
100%	00:46	42%	00:48	89%	00:28	76%

Table 3.4: Results of Circuit C432 c)

Total Faults = 486				
Selection Factor	**Possible Faults**	**Generated Vectors**	**Vectors 100% OK**	**Logic Effectiveness**
20%	412			
Stuck-at-0		180	151	83%
Stuck-at-1		207	159	91%
Total		387	310	87%
40%	252			
Stuck-at-0		104	99	82%
Stuck-at-1		125	114	90%
Total		229	213	86%
60%	154			
Stuck-at-0		60	57	78%
Stuck-at-1		77	72	90%
Total		137	129	84%
80%	91			
Stuck-at-0		34	34	72%
Stuck-at-1		45	43	89%
Total		79	77	80.5%
100%	45			
Stuck-at-0		14	14	67%
Stuck-at-1		24	23	88%
Total		38	37	77.5%

Table 3.5: Results of Circuit C499 a)

In Table 3.5 the row at the top gives the number of faults considered by a conventional ATPG stuck-at (*Total Faults*) process (In this case 486). Different selection factors (from 20% to 100%) have been considered (first column). The number of possible faults is 412. The total of generated vectors (*stuck-at 0* and *stuck-at 1*) is 387 for a selection factor of 20%. This number decreases to 38 generated vectors for 100% of selection factor. A similar behavior to the C432 is observed in column 4 (Vectors 100% Ok). For a selection factor of 20% 310 of total vectors 100% Ok are found. As the selection factor increase this number decrease to 37 for a selection factor of 100%. The *logic effectiveness* gives an important metric of the number of test constraints that were successfully generated. It can be seen that for a selection factor of the 20% the total OPVEG effectiveness is 86%. This mean that a high number of values of coupled signals are forced successfully to aid to detect the defect. In other cases the value of OPVEG effectiveness for different selection factors are between 82% and 88%.

Table 3.6 repeats the information of the number of **generated vectors** for both stuck-at 1 and stuck-at 0 faults. Depending on the selection factor the number of generated vectors goes from 387 (for 20% of selection factor) to 38 (for 100% of selection factor). Also, the number of **repeated vectors** is given. *Repeated vectors* in table 3.6 shows 104 vectors of a total of 387 generated vectors with a selection factor of 20%. These values decrease as the selection factor increase. As it can be seen in the last row, for a selection factor of 100% the number of repeated vectors is 4.

The number of contained vectors in the conventional test for the C499 circuit (3.6) is between 44 and 11. This behavior is different to that observed for the ISCAS'85 C432 (See Table 3.3). The number of compacted vectors (column 5 in table 3.6) is between 240 and 23. Finally the percentage of aid to the conventional test is between 78.15% and 7.50%. It is possible to observe than these percentages are lower than those observed in table 3.3.

Table 3.7 shows the time and CPU usage for different selection factors. These times are longer than those obtained with the previous benchmark circuit. this is because the number of detected faults is higher and takes more time to generate the vectors. The times are between 19:04 and 1:00 (m:s) for time of ATPG stuck-at 0 and 8:25 and 0:39 (m:s) for time of ATPG stuck-at 1.

Table 3.8 shows the obtained results for the circuit C1908. The row at the top gives gives the number of faults considered by a conventional ATPG stuck-at (*Total Faults*)

Selection Factor	**Generated Vectors**	**Repeated Vectors**	**Contained Vectors in Conventional Test**	**Compacted Vectors**	**Percentage of Aid to the Conventional Test**
20%	388	104	44	240	78.15%
40%	229	77	35	117	45.66%
60%	137	35	30	72	27.31%
80%	79	16	20	43	15.75%
100%	38	4	11	23	7.50%

Table 3.6: Results of Circuit C499 b)

Selection Factor	**Time of selection of Nodes (m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-0(m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-1(m:s)**	**CPU Usage**
20%	01:44	41%	19:04	93%	08:25	92%
40%	01:34	46%	05:17	93%	04:16	91%
60%	01:26	49%	03:16	92%	02:29	89%
80%	01:26	50%	01:55	91%	01:20	85%
100%	01:25	50%	01:00	89%	00:39	75%

Table 3.7: Results of Circuit C499 c)

process (For C1908 circuit 578). The possible faults for different selection factors are between 428 and 20. The total of generated vectors goes from 421 to 17 (for 20% and 100% selection factors) respectively.

Total Faults = 578				
Selection Factor	**Possible Faults**	**Generated Vectors**	**Vectors 100% OK**	**Logic Effectiveness**
20%	428			
Stuck-at-0		212	185	93%
Stuck-at-1		209	183	92%
Total		421	386	92.5%
40%	204			
Stuck-at-0		95	90	91%
Stuck-at-1		95	90	91%
Total		190	180	91.0%
60%	104			
Stuck-at-0		46	45	88%
Stuck-at-1		49	47	92%
Total		95	92	89.9%
80%	50			
Stuck-at-0		22	21	86%
Stuck-at-1		23	22	90%
Total		45	43	88.0%
100%	20			
Stuck-at-0		8	8	80%
Stuck-at-1		9	9	90%
Total		17	17	85.0%

Table 3.8: Results of Circuit C1908 a)

The total number of vectors 100% OK is between 386 (20% selection factor) and 17 (100% selection factor). It can be observed in this circuit that the number of faults considered as critical is higher respect to previous circuits. Column five (See table 3.8) gives the different percentages of the logic effectiveness. These values goes from 92.5% (20% selection factor) to 85% (100% selection factor).

The number of repeated vectors are given in table 3.9 for the C1908 circuit. The

number of these vectors goes from 94 to 0. Similarly to the C432 circuit, the number of contained vectors in conventional test for the C1908 circuit is very low. Column 5 gives the number of compacted vectors that goes from 326 to 17 for different selection factors. The percentages of aid to the conventional test are given in column 6. For a selection factor of 20% correspond 72.58%. This percentage decreases as the selection factor increases. A percentage of 2.93% is obtained when 100% of selection factor is selected.

Selection Factor	**Generated Vectors**	**Repeated Vectors**	**Contained Vectors in Conventional Test**	**Compacted Vectors**	**Percentage of Aid to the Conventional Test**
20%	421	94	1	326	72.58%
40%	190	33	0	157	32.75%
60%	95	13	0	82	16.38%
80%	45	3	0	42	7.75%
100%	17	0	0	17	2.93%

Table 3.9: Results of Circuit C1908 b)

Table 3.10 gives the different times obtained for C1908 circuit. The different percentages of CPU usage are also given. In table 3.10 can be observed that the time of selection of nodes has been increased considerably respect to the previous analyzed circuits. For 20% of selection factor the time to select the nodes is 03:12 m:s. This time decreases as the selection factor increases the time to select nodes at 100% is 03:00 m:s.

Selection Factor	**Time of selection of Nodes (m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-0(m:s)**	**CPU Usage**	**Time of ATPG Stuck-at-1(m:s)**	**CPU Usage**
20%	03:12	41%	11:28	93%	11:14	94%
40%	02:45	47%	03:42	92%	03:41	91%
60%	02:56	44%	01:41	93%	01:41	93%
80%	02:57	45%	00:46	92%	00:47	91%
100%	03:00	43%	00:19	86%	00:20	91%

Table 3.10: Results of Circuit C1908 c)

Time of ATPG stuck-at 0 is given in column 4. The necessary times for different selection factors goes from 11:28 m:s to 00:19 m:s. The percentage of CPU usage for

stuck-at 0 is between 93% and 86%. Time of ATPG stuck-at 1 and its CPU usage show similar values that obtained in stuck-at 0.

Finally de results obtained for the C2670 circuit are shown in tables 3.11 to 3.13. Generated vectors, vectors 100% and logic effectiveness results are given in table 3.11. In this case it is possible to observe that the number of total faults has increased significantly showing 2204 faults. Different selection factors have been considered. For every selection factor the number of possible faults goes from 1442 to 206 (for 20% and 100% of selection factor) respectively. The total number of generated vectors is between 1318 (20%) and 197 (100%). The selection factor increases as the number of generated vectors decrease.

Total Faults = 2204				
Selection Factor	**Possible Faults**	**Generated Vectors**	**Vectors 100% OK**	**Logic Effectiveness**
20%	1454			
Stuck-at-0		686	591	89%
Stuck-at-1		632	539	81%
Total		1318	1130	85.2%
40%	682			
Stuck-at-0		304	273	85%
Stuck-at-1		309	285	88%
Total		613	558	86.4%
60%	408			
Stuck-at-0		183	170	87%
Stuck-at-1		190	185	92%
Total		373	355	89.6%
80%	270			
Stuck-at-0		121	111	87%
Stuck-at-1		131	127	96%
Total		252	238	91.3%
100%	206			
Stuck-at-0		95	87	89%
Stuck-at-1		102	100	98%
Total		197	187	93.3%

Table 3.11: Results of Circuit C2670 a)

Vectors 100% Ok in column 4 give those vectors generated with all the favorable conditions. In this column the total number of *vectors 100% Ok* is between 1130 and 187. This means that a high number of vectors were generated favorable to detect faults. In other hand, logic effectiveness could achieve good percentages. Percentages of logic effectiveness for different selection factors are between 85.2% and 93.3%. Table 3.12 gives the total generated vectors for different selection factors. Column 2 in table 3.12 gives the repeated vectors that goes from 251 to 42. Contained vectors in conventional test is zero for all cases of the selection factors. The values of compacted vectors is between 1067 and 155. Finally, different percentages obtained for percentage of aid to the conventional test are showed in column 6. These values go from 57.41% to 8.58%. Doing a comparison of the obtained results for the previous circuits with obtained from C2670 circuit it is observed that the percentage of aid to the conventional test is lower for this case. In table 3.13 different values of percentage of CPU usage and times of selection factors and ATPG stuck-at 0 and stuck-at 1 are depicted.

Selection Factor	**Generated Vectors**	**Repeated Vectors**	**Contained Vectors in Conventional Test**	**Compacted Vectors**	**Percentage of Aid to the Conventional Test**
20%	1318	251	0	1067	57.41%
40%	613	124	0	489	26.70%
60%	373	63	0	310	16.25%
80%	252	43	0	209	10.98%
100%	197	42	0	155	8.58%

Table 3.12: Results of Circuit C2670 b)

It is possible to see that the time of selection of nodes is significantly higher than for the previous analyzed circuits. This circuit (C2670) is the circuit that present a great amount of interconnections due to the great number of gates. The time of selection of nodes goes from 43:40 m:s to 52:48 m:s. The times of ATPG stuck-at 0 and stuck-at 1 are large and also its CPU usage. Time of ATPG stuck-at 0 is between 49.17 m:s and 04:22 m:s. Percentages of CPU usage of both cases (stuck-at 0 and stuck-at 1) are greatest obtained from the 4 analyzed circuits ISCAS'85.

From the obtained results showed in tables, it is possible to observe in all cases that the percentages generated by OPVEG tool in comparison with the percentages generated by conventional ATPG are better. One of the obtained results of great importance

Selection Factor	Time of selection of Nodes (m:s)	CPU Usage	Time of ATPG Stuck-at-0(m:s)	CPU Usage	Time of ATPG Stuck-at-1(m:s)	CPU Usage
20%	43:40	48%	49:17	94%	46:04	94%
40%	48:15	44%	18:39	94%	17:48	94%
60%	50:53	41%	11:15	86%	09:53	89%
80%	49:38	41%	07:43	81%	06:28	90%
100%	52:48	34%	04:22	94%	04:08	93%

Table 3.13: Results of Circuit C2670 c)

for this work is to guarantee if the set of generated vectors with a conventional ATPG contains the most favorable test vectors considering capacitive couplings. The results showed that the percentage of guaranteed favorable vectors obtained by a conventional ATPG is very low or zero in 3 of the circuits (C432, C1908 and C2670). Single in the analysis of the C499 circuit the case appears where more of 11 of the obtained vectors of conventional form capacitive couplings are favorable to detect faults considering (**Vectors Contained in the Conventional Test**).

Another registered important data is the percentage of **Aid to the Conventional Test** with OPVEG tool. It is possible to observe that in all the cases when the selection factor decreases the percentage of aid to the conventional test increases. Nevertheless, this is inversely proportional to the number of generated vectors compacted that are those that helps to complement the cover of conventional test. In these two measures it is observed that a commitment exists because when having more vectors of test the time of crucial test in the design of the circuits rises, but increased to the percentage of aid.

With respect to the times that are used for the data manipulation and generation of test vectors, it is observed that the selection of nodes consumes a similar time for all the selection factors. This must to that although the number of critical nodes is reduced with the selection factor, the search is done in the same list of data and analyzing all the nodes. In the case of the time of ATPG, it increases with the selection factor and the size of the circuit when varying the number of victim and aggressor nodes. This made vary the times of the processes from tens of seconds to almost 1 hour.

3.4.2 Coupling capacitance effectiveness

The benefits of OPVEG in terms of the amount of coupling capacitance having a logic condition favoring the open detection by stuck-at vectors analyzed. Two metrics have been defined to analyze the OPVEG results. The first metric obtains the amount of favorable coupling capacitance of interconnection opens separately for both stuck-at 1 and stuck-at 0 vectors. This metric is calculated as follows:

$$C_{eff}^{sa} = \sum_{n=0}^{t} \frac{C_n^0}{C_T} + \sum_{n=0}^{t} \frac{C_n^1}{C_T} \tag{3.4}$$

Where:
C_n^0: is the amount of the coupling capacitance of a critical line having a favorable logic condition for the stuck-at 0 vector.
C_n^1: is the amount of the coupling capacitance of a critical line having a favorable logic condition for the stuck-at 1 vector.
C_T: is the total amount of coupled capacitance to a critical line.
t: is the number of interconnection opens.

The results obtained for the ISCAS'85 benchmark circuits are given in the third column of table 3.14 for different selection factors. It can be observed that the favorable coupling capacitance increases for a lower value of the selection factor. For C432 circuit (Table 3.14) it can be observed that the coupling capacitance effectiveness is in the range between 70.33% and 80.52% and for C499 circuit the coupling capacitance effectiveness is in the range between 78% and 85%. Again, for C1908 circuit the coupling capacitance effectiveness is in the range between 78% and 85%. Finally, the percentage range of coupling capacitance effectiveness is in the range between 68% and 80%.

The second metric gives a better approximation of the real benefits of OPVEG. This is because for each interconnection open, only one of the stuck-at vectors is selected (stuck-at 0 or stuck-at 1). The vector with the highest effectiveness is selected. This metric is calculated as follows:

$$C_{eff}^{sa*} = \sum_{n=0}^{t} \frac{C_n^{0/1}}{C_T} \tag{3.5}$$

Where:
C_{eff}^{sa*} is amount of coupling capacitance of a critical line for the most favorable stuck-at vector (stuck-at 0 or stuck-at 1).

The results obtained for the ISCAS'85 benchmark circuits are given in the fourth column of table 3.14 for different selection factors. Again, the favorable coupling capacitance increases for a lower value of the selection factor. The coupling capacitance effectiveness increases significantly with this metric than for the previous one. Actually, this metric gives a more realistic measure.

Circuit	Selection factor	$C_{eff}^{sa} = \sum_{n=0}^{t} \frac{C_n^0}{C_T} + \sum_{n=0}^{t} \frac{C_n^1}{C_T}$	$C_{eff}^{sa*} = \sum_{n=0}^{t} \frac{C_n^{0/1}}{C_T}$
C432	100%	89.01%	65.40%
	80%	89.78%	67.58%
	60%	89.97%	69.35%
	40%	90.90%	74.10%
	20%	93.52%	74.68%
C499	100%	89.18%	73.18%
	80%	89.77%	74.18%
	60%	90.95%	75.86%
	40%	91.00%	77.62%
	20%	94.07%	79.13%
C1908	100%	81.25%	72.73%
	80%	84.42%	73.63%
	60%	86.06%	75.74%
	40%	88.16%	76.62%
	20%	84.63%	78.70%
C2670	100%	75.01%	65.55%
	80%	81.69%	67.43%
	60%	85.13%	70.37%
	40%	87.10%	71.56%
	20%	89.42%	73.81%

Table 3.14: Capacitance effectiveness of four benchmark circuits ISCAS'85.

In general, table 3.14 shows the results obtained for four circuit ISCAS'85. In this,

it can appreciated that the percentage for the amount of favorable coupling capacitance of interconnection opens separately for both stuck-at 1 and stuck-at 0 (Eq. 3.4) vectors goes from 70% and 85%, and the percentages obtained for equation 3.5 showed in column 4, goes from 97% to 100.00%.

Table 3.15 shows the results obtained for conventional ATPG vectors. From this, obtained results with conventional vectors applying the previous metrics, it is possible to see that percentages depicted in 3.15 are smaller that results for OPVEG vectors. This results were obtained for selection factor of 100%. For this case, the percentage for the amount of favorable coupling capacitance of interconnection opens separately for both stuck-at 1 and stuck-at 0 (Eq. 3.4) vectors goes from 55% and 69%, and the percentages obtained for equation 3.5 showed in column 4, goes from 70% to 85%.

Circuit	$C_{eff}^{sa} = \sum_{n=0}^{t} \frac{C_n^0}{C_T} + \sum_{n=0}^{t} \frac{C_n^1}{C_T}$	$C_{eff}^{sa*} = \sum_{n=0}^{t} \frac{C_n^{0/1}}{C_T}$
C432	72.17%	57.59%
C499	81.80%	64.67%
C1908	73.69%	65.86%
C2670	67.54%	57.17%

Table 3.15: Capacitance effectiveness for conventional vectors. Selection factor of 100%.

3.5 Conclusions

A test methodology has been proposed to obtain favorable test vector conditions to detect interconnection open defects. This methodology apply proper logic states at the coupled lines to enhance the defect detectability. A tool named OPVEG has been developed to allow to generate favorable test vectors for these defects. This tool uses circuit logic description, layout information and a stuck-at test pattern generator.

The operation of the tool is based on the extraction of parasitic capacitances of a circuit, ordering of data, calculation of parameters and generation of test vectors considering coupling effects. This is obtained from the interaction of two commercial CAD tools (CADENCE [14]) and TetraMAX [79].

Some metrics have been defined to illustrate the performance of OPVEG. Logic effectiveness, this metric indicates that so effective is the fault coverage of the generated favorable vectors with OPVEG (depending on the obtained favorable conditions). Other metric presented was percentage of aid to the conventional test, this metric gives the percentage of fault coverage for favorable test vectors that it guarantees an improvement in the cover of the conventional vectors.

OPVEG has been applied to four ISCAS85 benchmark circuits. The results indicate that the test vectors obtained using OPVEG present more favorable logic states at the coupled lines than those obtained with conventional ATPG process. From this it is expected that the defect coverage of interconnection opens increases.

The logic effectiveness for the four analyzed ISCAS benchmark circuits goes from 77% to 93%. Using a conventional ATPG process the logic effectiveness is in the range of 46.8% and 54.4% for a selection factor of 100%.

The percentage of aid that is provided to a conventional test increases as the selection factors decreases. For the ISCAS C432 this metric is 7.35% for 100% selection factor. The aid to conventional test increases to 81.19% for 20% selection factor.

The benefits of OPVEG in terms of the amount of coupling capacitance having a logic condition favoring the open detection by stuck-at vectors analyzed. Again some metrics have been defined to illustrate the performance of OPVEG. For C432 circuit it can be observed that the coupling capacitance effectiveness is in the range between 70.33% and 80.52% and for C499 circuit the coupling capacitance effectiveness is in the range between 78% and 85%. Again, for C1908 circuit the coupling capacitance effective-

ness is in the range between 78% and 85%. Finally, the percentage range of coupling capacitance effectiveness is in the range between 68% and 80%.

Chapter 4

Fault Simulator for Opens (FASOP)

4.1 Introduction

In this chapter a Fault Simulator for Interconnection Opens is presented which is able to evaluate the defect coverage of interconnection opens. FASOP also gives useful information to evaluate the detectability of these defects. Based on this information better test vectors may be generated to improve the defect coverage or DFT measures can be undertaken. FASOP uses circuit logic description and layout information as inputs. The former comes from the netlist description of the circuit in a high level language and the latter is a file containing layout information given by Cadence. The test vectors to evaluate the defect coverage may be the set of vectors generated by OPVEG or vectors obtained by a traditional ATPG process. FASOP considers the effect of the coupling lines and the sensitized and un-sensitized gates influencing the floating line of the interconnection open. FASOP also evaluates the defect coverage considering the gate trapped charge. FASOP gives the extremal conditions of trapped gate charge in order to detect the open. This is made for both stuck-at 1 and stuck-at 0 vectors. In this case, it is evaluated its range of detection due to the uncertainty of the value of the gate trapped charge.

The rest of the chapter is organized as follows. In section 4.2 the general working environment of FASOP is presented. In section 4.3 the structure of FASOP is described. In section 4.4 the methodology to estimate the range of detection of interconnection opens is presented. This is the core of our methodology. In section 4.5, FASOP is used to evaluate the defect coverage of some ISCAS benchmark circuits. In section 4.6 FASOP is used for making detectability analysis. This may be used to further improve

the detectability of interconnection opens. Finally in section 4.7 the conclusion of the chapter are given.

4.2 General environment for FASOP

In this section the general environment under which FASOP works is briefly described. FASOP mainly receives as inputs a circuit logic description and a layout extracted file. The input vectors could come from our developed OPVEG tool or a conventional ATPG process. Using this information FASOP evaluates the defect coverage of the interconnection opens for the set of input of vectors.

When OPVEG is used a possible test strategy consists on generating the most favorable conditions at the coupling signals for a certain value of coupled capacitance. This is made defining a given Selection Factor. If the defect coverage is not adequate it can be improved by two means: a) applying constraints to those coupled signals with a lower coupled capacitance value, and b) sensitize more than one gate connected to the floating line.

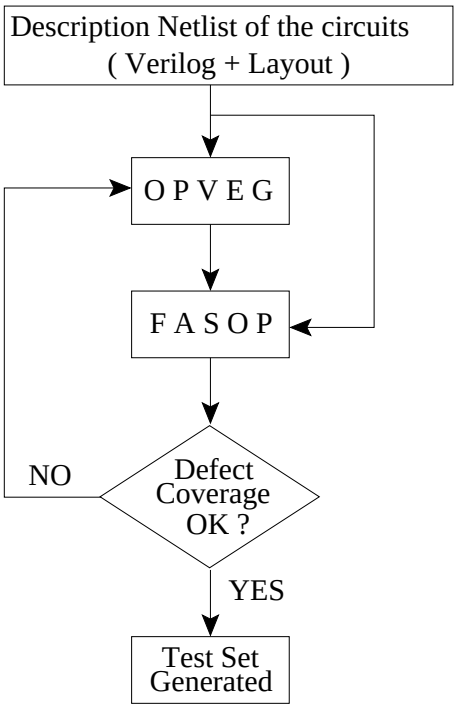


Figure 4.1: Proposed test framework for interconnection opens

4.3 Description of FASOP

This section describes the basic structure of FASOP. FASOP has been built using C language (structured) in an operating system Solaris Version 5,8 (UNIX atmosphere) with a compiler GCC version 2.95.1. The program is made up of several subprograms that are executed sequentially. Different factors that influence the voltage at floating node are taken into account. Figure 4.2 shows a simplified flowchart of FASOP.

FASOP is based in a circuit logic description and layout information. FASOP estimates the range of detection for each fault. Using this the defect coverage of interconnection opens is evaluated. FASOP includes tasks to determine the number of transistors affected by each one of the critical nodes. ***Critical nodes*** are those lines that have at least one coupled line of capacitive value greater or equal than the sum of this capacitive values of the line to G_{ND} and V_{DD} multiplied by a factor.

The different blocks composing FASOP tool are explained below. A simplified flowchart of FASOP is given in figure 4.2 which allows in broad strokes shows the flow of information and the output information. For the rest of the chapter it is assumed that OPVEG is used to generate the set of input vector unless otherwise noted. However, FASOP can also evaluate the defect coverage using a different set of input vectors.

- **STEP 1**.- The first block shown in the figure 4.2, after the input files, is the step of search and simulation. In this block the first critical node of the file generated by OPVEG is selected (critical nodes). In the extraction file generated by CADENCE, all those devices related to the critical nodes with their respective topology characteristics (*W and L*) are identified.

  This process is carried out for each critical node that affects at least one logic gate. The search of the dimensions (W and L) has as main intention to obtain the overlap capacitances (C_{gson}, C_{gdon}, C_{gsop} and C_{gsop}) for all the transistors affected by the critical node. This information is used to calculate the error regions and will be seen with greater detail in section 4.4 on page 68.

  At the same time that is made the searching of affected transistors and its dimensions, a logical simulation using a commercial ATPG tool is carried out. In this work *TetraMax* is used. The goal of the logic simulation is to obtain all the logical states of the lines coupled to the critical nodes and also all the the voltages in the terminals of transistors affected by critical nodes. This allows to identify which affected gates are sensitized or unsensitized due to the state of the critical

nodes (see section 4.4 on page 73). Until this point step 1 carry out the task of compiling the information and to give format contained in different files. All this information will be used to calculate the region of error in the next step.

- **STEP 2**.- Step 2 processes all the information obtained through the previous step. The main task of the first block of step 2 consists principally of calculating (depending on fault stuck-at 1 or stuck-at 0), by means of the expressions described in the section 4.4, the maximum or minimum floating routing capacitance (C_r^1 or C_r^0) allowed to have at least $V_{DD} - |V_{TP}|$ or V_{TN} respectively. The information is processed for each critical node and stores temporarily in arrays.

- **STEP 3**.- In the block of step 3, the evaluation of the coverage of the defect is carried out, this stage consists of determining if the examined critical node is within the detectability range or not. The processing of this information carries out a subroutine to it contained in the main program which is explained to detail in the appendix. Finally the program determines the percentage of detection for each node (SA-0 and SA-1 faults) and obtains a general result of nodes analyzed for each selection factor, which is stored in file results.

4.4 Computation of the Defect Detection Conditions

Opens in interconnections produce NMOS and PMOS transistors of the affected gate(s) to float. The behavior of a gate(s) with an interconnection open is determined by the voltage at the floating node (V_{if}). This voltage depends on the transistor structure of the affected gate(s), the surrounding coupling capacitances to the floating line and the trapped gate charge during the fabrication process.

In this section, the basic procedure to estimate the range of detectability of a given interconnection open is described. This process is described starting from a basic electrical model of an interconnection open until to analyze the full model. Analytical equations for each considered model have been developed. First, the basic model is considered. Coupling is considered as a lumped model, one gate is sensitized and it is assumed zero trapped gate charge. Next, the effect of individual coupling capacitances is added to the basic model. Next the effect of the different possible sensitization gates is added to the previous model. Finally, the effect of the gate trapped charge is added to the previous model. This is the full model of the interconnection open defect.

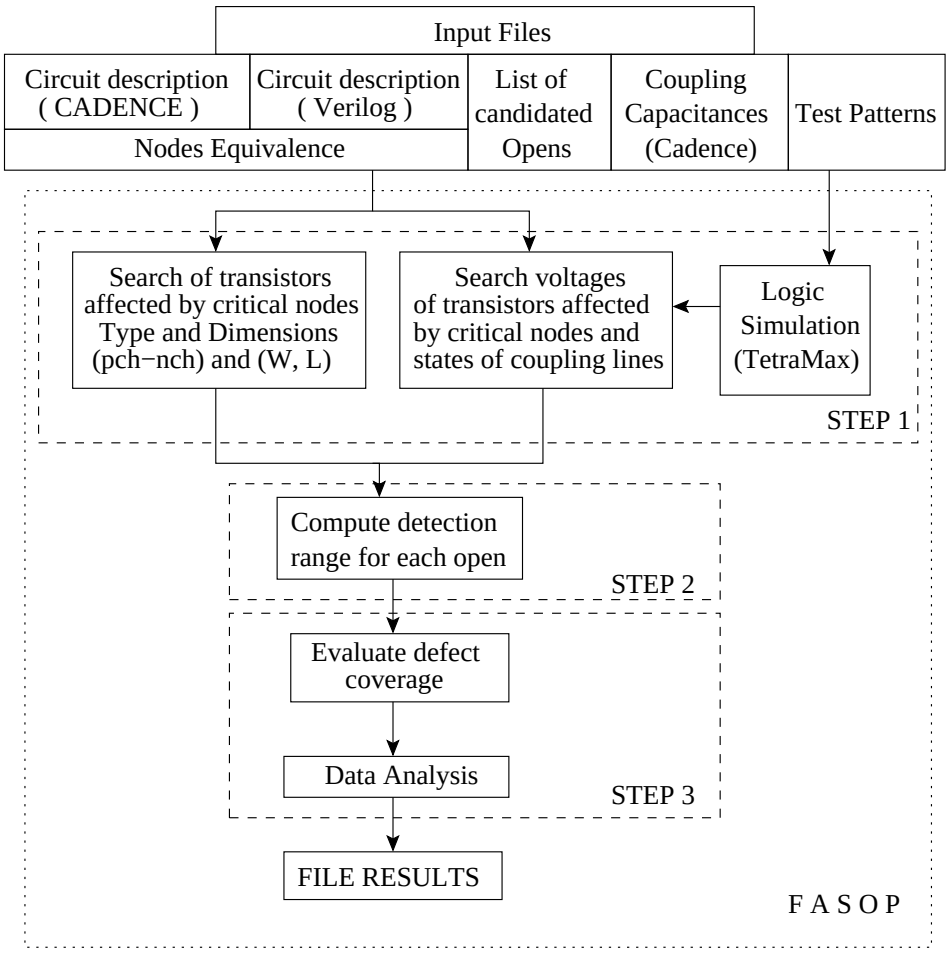


Figure 4.2: Simplified Flowchart of FASOP

4.4.1 Basic detection computation

The basic electrical model for an interconnection open is shown in figure 4.3. In this model, the effect of coupling capacitances to the floating line is considered as a lumped model, only one gate is sensitized and zero trapped gate charge it is assumed. Five topologies are identified in this model:

- **The Nmos topology** is formed by the gate-source Nmos overlap capacitance (C_{gson}), the poly-bulk capacitance (C_{pb}) of the floating line and the influence of the intrinsic part of the Nmos transistor.
- **The Pmos topology** is formed by the gate-source Pmos overlap capacitance (C_{gsop}), the poly-well capacitance (C_{pw}) of the floating line and the influence of the intrinsic part of the Pmos transistor.

- **The feedback topology** that takes into account the gate-drain Pmos overlap capacitance (C_{gdop}) and the gate-drain Nmos overlap capacitance (C_{gdon}).
- **The coupling topology** that takes into account the effect of the coupling capacitance from neighbor lines.
- **The routing topology** that takes into account the running metal layer capacitance of the floating line. One part of this capacitance runs over the well and the other one over the substrate.

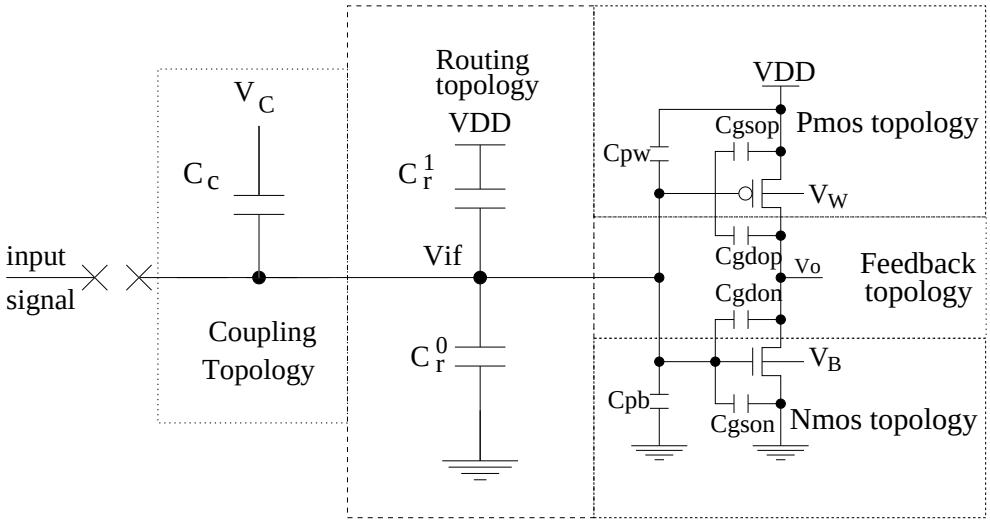


Figure 4.3: Basic electrical model for an inverter

Using the basic electrical model of the interconnection open an equation (4.1) has been obtained that express the voltage on the floating node as a function of the different factors that influence it.

$$V_{if} = \frac{C_{gsop} + C_{pw}}{C_T} V_{DD} + \frac{C_{gdon} + C_{gdop}}{C_T} V_o - \frac{Q_{GT}}{C_T} + \frac{C_r{}^1}{C_T} V_{DD} + \frac{C_c}{C_T} V_C \qquad (4.1)$$

Where:

$$C_T = C_{gson} + C_{gdon} + C_{gdop} + C_{gsop} + C_{pw} + C_{pb} + C_r^0 + C_r^1 + C_C$$

and C_{gsop}, C_{gdon}, C_{gdop}, are the overlap capacitances, C_{pw} is the poly-well capacitance, Q_{GT} is the induced charge at the floating gates by the intrinsic part of the transistors, C_r^1 and C_C are the related charges to the break position, where C_r^1 corresponds

to the floating routing capacitance that may have one terminal connected to the bulk which is biased to V_{GND} and the other part to the well which is biased to V_{DD}. The coupling capacitance to the floating line C_C can influence significantly the voltage at the floating line. The signals at the adjacent lines may have a high logic value (V_{DD}) or a low logic value (V_{GND}).

The previous equation can be re-arranged to obtain expressions to determine if a given interconnection open is detectable or not. One equation is developed to assure a stuck-at 0 condition (guaranteed V_{TN}) and the second to assure a stuck-at 1 condition (guaranteed $V_{DD} - |V_{TP}|$) at the floating line.

Guaranteed V_{TN}

From the equation described above are obtained the necessary conditions to assure an induced voltage at the floating node non greater than the threshold voltage of the n-channel transistor. This condition assures that the interconnection open behaves as a stuck-at 0 fault. It is assumed that the n-channel transistor operates in the cut-off region. Relating the charges to the capacitances and the voltage across them, after substituting $V_{if} = V_{TN}$ in equation (4.1) an explicit expression can be obtained to estimate the minimum value of capacitance to ground of the floating line (C^0) to have at most an induced voltage of V_{TN} at the floating line. This gives the following equation:

$$C^0 \geq \frac{C_{DD}(V_{DD} - V_{TN})}{V_{TN}} - \frac{C_{gson}V_{TN}}{V_{TN}} - \frac{Q_{GT}}{V_{TN}} + \frac{C_C(V_C - V_{TN})}{V_{TN}} \qquad (4.2)$$

where:

$$C_{DD} = C_{gson} + C_{gdon} + C_{gdop} + C_{pw} + C_r^1 + C_C$$
$$Q_{GT} = Q_{GTN} + Q_{GTP}$$
$$C^0 = C_r^0 + C_{pb}$$

Guaranteed $V_{DD} - |V_{TP}|$

In a similar way an expression to estimate the minimum value of the capacitance to V_{DD} of the floating line (C^1) to have at least an induced voltage of $V_{DD} - |V_{TP}|$ can be obtained. This condition assures that the interconnection open behaves as a stuck-at 1 fault. This gives the following equation:

$$C^1 \leq \frac{C_{GG}(V_{DD}-|V_{TP}|)}{V_{DD}-|V_{TP}|} - \frac{C_{gsop}(|V_{TP}|)}{V_{DD}-|V_{TP}|} - \frac{Q_{GT}}{V_{DD}-|V_{TP}|} + \frac{C_C V_C}{V_{DD}-|V_{TP}|} \tag{4.3}$$

where:

$$C_{GG} = C_{gson} + C_{gdon} + C_{gdop} + C_{pb} + C_r^0 + C_C$$
$$C^1 = C_r^1 + C_{pw}$$

4.4.2 Including Coupling Effects

A floating line can have a high number of coupled signals which influence significantly its behavior. The coupled signals may take different logic values. This is taken into account in the circuit model shown in figure 4.4 where a coupling topology has been defined.

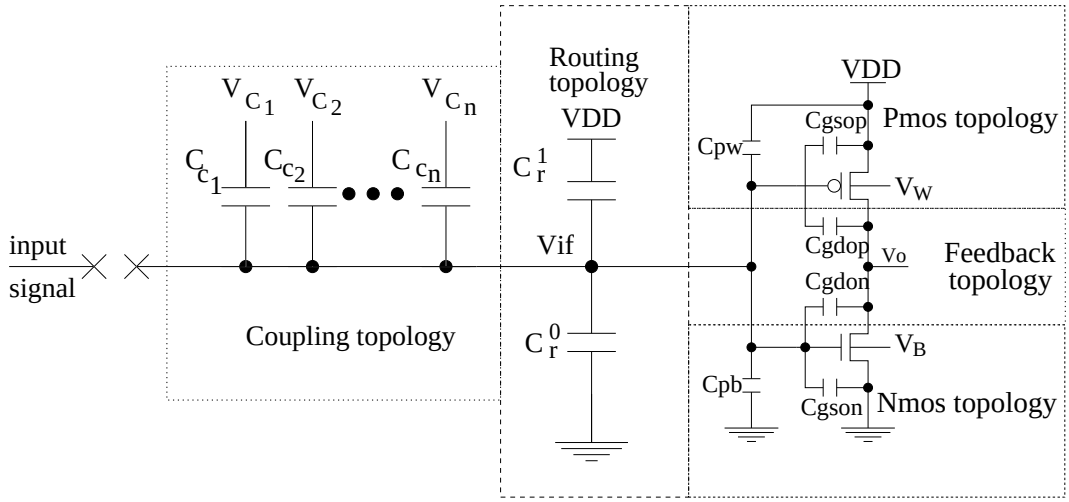


Figure 4.4: Basic Electrical model for an inverter with coupling lines at its input

Using this enhanced electrical circuit model of the interconnection open an equation 4.4 has been obtained that express the voltage on the floating node as a function of the different factors that influence it:

$$V_{if} = \frac{C_{gsop}+C_{pw}}{C_T}V_{DD} + \frac{C_{gdon}+C_{gdop}}{C_T}V_o - \frac{Q_{GT}}{C_T} + \frac{C_r^1}{C_T}V_{DD} + \frac{C_{C_1}V_{C_1}+\ldots+C_{C_n}V_{C_n}}{C_T} \tag{4.4}$$

In this expression the terms modeling the coupling capacitances and its voltage values can be observed. Different states of the coupling signals are considered (V_{C1} to V_{Cn}). They can take values of V_{DD} ($G_{ND} = 0$V) for the 1 (0) logic value at the coupled signal.

Let's define next the assured detectable conditions.

Guaranteed V_{TN}

Relating the charges to the capacitances and the voltage across them, after substituting $V_{if} = V_{TN}$ and $V_O = V_{DD}$ an explicit expression can be obtained to estimate the minimum capacitance to ground (C_0) of the floating line to have at most an induced voltage of V_{TN} at the floating line. This gives the following expression:

$$\begin{aligned} C^0 \;\geq\; & \frac{C_{DD}(V_{DD}-V_{TN})}{V_{TN}} - \frac{C_{gson}V_{TN}}{V_{TN}} - \frac{Q_{GT}}{V_{TN}} \\ + \; & \frac{C_{C_1}(V_{C_1}-V_{TN}) + \cdots + C_{C_n}(V_{C_n}-V_{TN})}{V_{TN}} \end{aligned} \tag{4.5}$$

Guaranteed $V_{DD} - |V_{TP}|$

In a similar way an expression to estimate the minimum value of the capacitance to V_{DD} of the floating line to have at least an induced voltage of $V_{DD} - |V_{TP}|$ at the floating line has been obtained. This gives the following expression.

$$C^1 \;\leq\; \frac{C_{GG}(V_{DD}-|V_{TP}|)}{V_{DD}-|V_{TP}|} - \frac{C_{gsop}|V_{TP}|}{V_{DD}-|V_{TP}|} - \frac{Q_{GT}}{V_{DD}-|V_{TP}|} + \frac{C_{C_1}V_{C_1} + \cdots + C_{C_n}V_{C_n}}{V_{DD}-|V_{TP}|} \tag{4.6}$$

4.4.3 Including sensitization gates

In this section the effect of sensitized and un-sensitized gates is taken into account. More than one gate can be connected to the affected floating line (See figure 4.5). Depending on the input vector one or more gates can be sensitized. A sensitized gate has a conducting path from V_{DD} to ground through the transistors affected by the floating line. For the sensitized gates the voltages at the transistor terminals can be known. However, for unsensitized gates the voltages at drain-source terminals of the transistors

of the affected gates are unknown for the actual input vector. This impacts the charge at the gate of the affected transistors. Hence, the detectability of the interconnection open. The used model to analyze the effect of sensitized and unsensitized gates is shown in the figure 4.5.

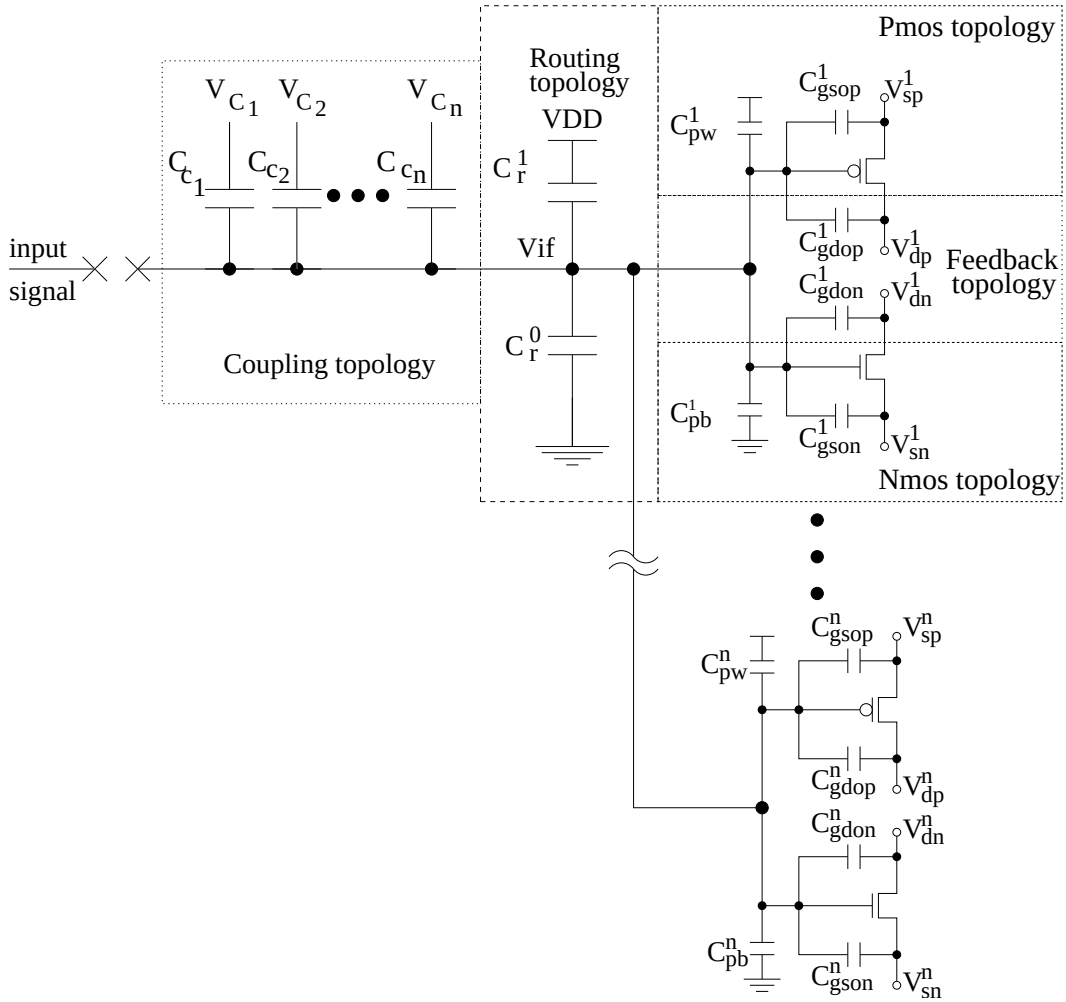


Figure 4.5: Electrical model for an inverter with sensitized and unsensitized gates

In the circuit shown to illustrate the effect sensitized and unsensitized gates, the inverter and the Nor gates are sensitized by the input vectors. However, the two Nand gates are not sensitized for the applied input vector.

For the sensitized gates the power supply and ground are connected through the defective transistors. Analytical expressions are used to determine the testability regions of interconnection opens. These regions are defined by two voltages at floating node (V_{if}): a) $V_{if} = V_{TN}$, and b) $V_{if} = V_{DD} - |V_{TP}|$. For sensitized gates, using the two

previous conditions it can be known the voltages at the drain-source terminals of the transistors affected by the open. Using this, the charge of the floating transistors is estimated. For unsensitized gates, the voltages at the drain-source terminals may depend on the history of the gate.

The expressions described previously can be modified to account for sensitized and unsensitized gates. Using the model shown in the figure 4.5 an expression that describes the voltage at the floating node V_{if} considering the effect of the sensitized and unsensitized gates on the floating line can be obtained. This gives the following expression.

$$\begin{aligned} V_{if} &= \frac{C_{pw}^T}{C_T}V_{DD} + \frac{C_r^1}{C_T}V_{DD} - \frac{Q_{GT}^T}{C_T} \\ &+ \frac{C_{gsop}^1 V_{sp}^1 + \cdots + C_{gsop}^n V_{sp}^n}{C_T} + \frac{C_{gson}^1 V_{sn}^1 + \cdots + C_{gson}^n V_{sn}^n}{C_T} \\ &+ \frac{C_{gdon}^1 V_{dn}^1 + \cdots + C_{gdon}^n V_{dn}^n}{C_T} + \frac{C_{gdop}^1 V_{dp}^1 + \cdots + C_{gdop}^n V_{dp}^n}{C_T} \\ &+ \frac{C_{C_1} V_{C_1} + \cdots + C_{C_n} V_{C_n}}{C_T} \end{aligned} \tag{4.7}$$

Where:

$$C_T = C_{gson}^T + C_{gdon}^T + C_{gdop}^T + C_{gsop}^T + C_{pw}^T + C_{pb}^T + C_r^0 + C_r^1 + C_{C_1} + \ldots + C_{Cn}$$

$$C_{gson}^T = \sum_{n=1}^{t} C_{gson}^n \qquad C_{gsop}^T = \sum_{n=1}^{t} C_{gsop}^n$$

$$C_{gdon}^T = \sum_{n=1}^{t} C_{gdon}^n \qquad C_{gdop}^T = \sum_{n=1}^{t} C_{gdop}^n$$

$$C_{pw}^T = \sum_{n=1}^{t} C_{pw}^n \qquad Q_{GT}^T = \sum_{n=1}^{t} Q_{GTN}^n + Q_{GTP}^n$$

$$C_{pb}^T = \sum_{n=1}^{t} C_{pb}^n$$

In equation (4.7), it can be observed the terms related with the effect of the sensitized and unsensitized gates. For this case, the pertaining voltages to the overlap capacitances are considered of each transistor affected by the floating node. Where

V_{sp}^1 to V_{sp}^n are the *source* voltages for every PMOS transistor, V_{sn}^1 to V_{sn}^n are the *source* voltages for every NMOS transistor and V_{dn}^1 to V_{dn}^n are the common voltages at drain terminal between PMOS and NMOS transistors.

The expression to estimate the detecting conditions to assure stuck-at 0 and 1 behavior are presented next.

Guaranteed V_{TN}

Relating the charges to the capacitances and the voltage across them, after substituting an explicit expression can be obtained to estimate the minimum capacitance to ground of the floating line to have at most an induced voltage of V_{TN}. This gives the following equation:

$$\begin{aligned} C^0 \geq & \frac{-V_{TN}(C_{gson}^T + C_{gdon}^T + C_{gdop}^T + C_{gsop}^T + C_{pw}^T + C_r^1 + C_{C_1} + \cdots + C_{C_n})}{V_{TN}} \\ & + \frac{V_{DD}(C_{pw} + C_r^1)}{V_{TN}} + \frac{Q_{GT}^T}{V_{TN}} \\ & + \frac{C_{gsop}^1 V_{sp}^1 + \cdots + C_{gsop}^n V_{sp}^n}{V_{TN}} + \frac{C_{gson}^1 V_{sn}^1 + \cdots + C_{gson}^n V_{sn}^n}{V_{TN}} \\ & + \frac{C_{gdon}^1 V_{dn}^1 + \cdots + C_{gdon}^n V_{dn}^n}{V_{TN}} + \frac{C_{gdop}^1 V_{dp}^1 + \cdots + C_{gdop}^n V_{dp}^n}{V_{TN}} \\ & + \frac{C_{C_1} V_{C_1} + \cdots + C_{C_n} V_{C_n}}{V_{TN}} \end{aligned} \tag{4.8}$$

Where: $C^0 = C_r^0 + C_{pb}^T$

Guaranteed $V_{DD} - |V_{TP}|$

In this case conditions to assure a voltage no lower than $V_{DD} - |V_{TP}|$ at the floating node are obtained.

$$
\begin{aligned}
C^1 \;\leq\; & \frac{-(V_{DD}-|V_{TP}|)(C^T_{gson}+C^T_{gdon}+C^T_{gdop}+C^T_{gsop}+C_{C_1}+\cdots+C_{C_n})}{V_{DD}-|V_{TP}|} \\
+ \; & \frac{V_{DD}(C^0_r)}{V_{DD}-|V_{TP}|}+\frac{Q^T_{GT}}{V_{DD}-|V_{TP}|} \\
+ \; & \frac{C^1_{gsop}V^1_{sp}+\cdots+C^n_{gsop}V^n_{sp}}{V_{DD}-|V_{TP}|}+\frac{C^1_{gson}V^1_{sn}+\cdots+C^n_{gson}V^n_{sn}}{V_{DD}-|V_{TP}|} \\
+ \; & \frac{C^1_{gdon}V^1_{dn}+\cdots+C^n_{gdon}V^n_{dn}}{V_{DD}-|V_{TP}|}+\frac{C^1_{gdop}V^1_{dp}+\cdots+C^n_{gdop}V^n_{dp}}{V_{DD}-|V_{TP}|} \\
+ \; & \frac{C_{C_1}V_{C_1}+\cdots+C_{C_n}V_{C_n}}{V_{DD}-|V_{TP}|}
\end{aligned}
\tag{4.9}
$$

Where: $C^1 = C^1_r + C^T_{pw}$

4.4.4 Including trapped gate charge

Another important factor influencing the voltage at the floating node is the trapped gate charge Q_{tr}. This trapped gate charge is deposited during fabrication. The expression that describes the voltage at floating node including the trapped gate charge term Q_{tr} is as follows:

$$
\begin{aligned}
V_{if} \;=\; & \frac{C^T_{pw}V_{DD}}{C_T}+\frac{C^1_rV_{DD}}{C_T}-\frac{Q^T_{GT}}{C_T} \\
+ \; & \frac{C^1_{gsop}V^1_{sp}+\cdots+C^n_{gsop}V^n_{sp}}{C_T}+\frac{C^1_{gson}V^1_{sn}+\cdots+C^n_{gson}V^n_{sn}}{C_T} \\
+ \; & \frac{C^1_{gdon}V^1_{dn}+\cdots+C^n_{gdon}V^n_{dn}}{C_T}+\frac{C^1_{gdop}V^1_{dp}+\cdots+C^n_{gdop}V^n_{dp}}{C_T} \\
+ \; & \frac{C_{C1}V_{C1}+\cdots+C_{Cn}V_{Cn}}{C_T}+\frac{Q_{tr}}{C_T}
\end{aligned}
\tag{4.10}
$$

In this equation (4.10) it can be observed the term related with the effect of the trapped gate charge Q_{tr}. This term is used to consider the variation for the trapped gate voltage. The value of the trapped gate charge depends strongly on the technology

used and on the topological considerations. The amount of actual trapped gate charge deposited during fabrication can not be predicted. Because of this our fault simulator does not assume any particular value of the trapped gate charge. Instead, it calculates the range of trapped gate charge which would be detectable.

Guaranteed V_{TN}

In this case high negative trapped gate charges help to the interconnection open to have a stuck-at 0 behavior. For the stuck-at 0 vector, the interconnection open is detected from infinite negative trapped gate charges to a lower value of negative (or maximum positive) trapped gate charge. Hence, an expression to estimate the lower negative (*or maximum positive*) of trapped gate voltage $V_{Q_{tr}}^{SA0}$ to assure a stuck-at 0 behavior can be obtained:

$$\begin{aligned} V_{Q_{tr}}^{sa0} \geq & \frac{V_{TN}(C_{gson}^T + C_{gdon}^T + C_{gdop}^T + C_{gsop}^T + C_{pb}^T + C_r^0 + C_r^1 + C_{C1} + \cdots + C_{Cn})}{C_T} \\ + & \frac{(-C_{pw}^T + C_r^1)V_{DD}}{C_T} + \frac{Q_{GT}^T}{C_T} \\ - & \frac{C_{gsop}^1 V_{sp}^1 + \cdots + C_{gsop}^n V_{sp}^n}{C_T} - \frac{C_{gson}^1 V_{sn}^1 + \cdots + C_{gson}^n V_{sn}^n}{C_T} \\ - & \frac{C_{gdon}^1 V_{dn}^1 + \cdots + C_{gdon}^n V_{dn}^n}{C_T} - \frac{C_{gdop}^1 V_{dp}^1 + \cdots + C_{gdop}^n V_{dp}^n}{C_T} \\ + & \frac{(C_{c1}V_{c1} + \cdots + C_{cn}V_{cn})}{C_T} \end{aligned} \tag{4.11}$$

Guaranteed $V_{DD} - |V_{TP}|$

In this case high positive trapped gate charges help to the interconnection open to have a stuck-at 1 behavior. For the stuck-at 1 vector, the interconnection open is detected from infinite positive trapped gate charges to a lower value of positive (or maximum negative) trapped gate charge. Hence, an expression to estimate the lower positive (*or maximum negative*) of trapped gate voltage $V_{Q_{tr}}^{SA1}$ to assure a stuck-at 1 behavior can be obtained:

$$
\begin{aligned}
V_{Q_{tr}}^{sa1} \leq & \frac{(V_{DD}-|V_{TP}|)(C_{gson}^{T}+C_{gdon}^{T}+C_{gdop}^{T}+C_{gsop}^{T}+C_{pb}^{T}+C_{r}^{0}+C_{C1}+\ldots+C_{Cn})}{C_T} \\
+ & \frac{Q_{GT}^{T}}{C_T}-\frac{(|V_{TP}|)(C_{r}^{1}+C_{pw}^{T})}{C_T} \\
- & \frac{C_{gsop}^{1}V_{sp}^{1}+\ldots+C_{gsop}^{n}V_{sp}^{n}}{C_T}-\frac{C_{gson}^{1}V_{sn}^{1}+\ldots+C_{gson}^{n}V_{sn}^{n}}{C_T} \\
- & \frac{C_{gdon}^{1}V_{dn}^{1}+\ldots+C_{gdon}^{n}V_{dn}^{n}}{C_T}-\frac{C_{gdop}^{1}V_{dp}^{1}+\ldots+C_{gdop}^{n}V_{dp}^{n}}{C_T} \\
+ & \frac{C_{C1}V_{C1}+\ldots+C_{Cn}V_{Cn}}{C_T}
\end{aligned}
\tag{4.12}
$$

Figures 4.7-4.12 show the detectability ranges for different $ISCAS'85$ benchmark circuits. They have been obtained for a selection factor of 100%. *Stuck-at 0* and *stuck-at 1* vectors are considered for each open. For the *stuck-at 1* vectors, in X-axe appears the minimum (*or maximum negative*) value of trapped gate voltage detectable for each vector. The stuck-at 1 vector is able to detect large positive trapped gate voltages. This is because the voltage at the floating gate increases as the positive gate trapped becomes higher. Hence, the open is detected as a stuck-at 1 fault. However, there is a minimum (*or maximum negative*) value of trapped gate voltage which it is not detected. A similar behavior appears for for the stuck-at 0 vector. In this case higher negative trapped gate voltages are detectable for the stuck-at 0 vector. There is a lower negative (*or maximum positive*) trapped gate voltage which will be detected by stuck-at 0 vector.

Let's analyze ISCAS C432 (See Figure 4.7). Sixteen opens have been considered according to the selection factor. For the open "1", the stuck-at 1 vector is able to detect trapped gate voltages in the range $[+\infty, 0.12V]$. The stuck-at 0 vector is able to detect trapped gate voltages in range $[-\infty, 0.51V]$. Because both ranges intersect, this open is detectable no matter the value of the trapped gate voltage.

For the open "3", the stuck-at 1 vector is able to detect trapped gate voltages in the range defined $[+\infty, -0.21V]$. The stuck-at 0 vector is able to detect trapped gate voltages in the range $[-\infty, -0.78V]$. In this case the open is not completely detected in the range of trapped gate voltage $[-\infty, +\infty]$. Assuming that the range of trapped gate voltage is known a probabilistic measure of the defect coverage of this open can be obtained. This can be obtained as follows (see (4.13), (4.14)):

$$V_{Qtr}^{SA0}\% = \begin{cases} 0.0 & \text{if } V_{Qtr}^{SA0} \leqq R^{-} \\ \dfrac{V_{Qtr}^{SA0} - R^{-}}{2|R^{-}|} & \text{if } R^{-} < V_{Qtr}^{SA0} < 0 \\ 50 & \text{if } 0 \leqq V_{Qtr}^{SA0} \end{cases} \tag{4.13}$$

$$V_{Qtr}^{SA1}\% = \begin{cases} 0.0 & \text{if } R^{+} \leqq V_{Qtr}^{SA1} \\ \dfrac{R^{+} - V_{Qtr}^{SA1}}{2R^{+}} & \text{if } 0 < V_{Qtr}^{SA1} < R^{+} \\ 50 & \text{if } V_{Qtr}^{SA1} \leqq 0 \end{cases} \tag{4.14}$$

Where:

$\mathbf{V_{Qtr}^{SA0}}$ and $\mathbf{V_{Qtr}^{SA1}\%}$**:** *percentage obtained from (V_{Qtr}^{SA0},V_{Qtr}^{SA1}).*
R: *is the total range of V_{Qtr}.*
$\mathbf{V_{Qtr}^{SA0}}$**:** *is the voltage of trapped charge for $SA0$ test vector.*
$\mathbf{V_{Qtr}^{SA1}}$**:** *is the voltage of trapped charge for $SA1$ test vector.*
$\mathbf{R}^{-}$ and $\mathbf{R}^{+}$**:** *is the negative and positive range of the voltage of trapped charge.*

A case is considered to illustrate the exposed in the equations (4.13) and (4.14). Taking as example open 3 from the C432 benchmark circuit ISCAS'85, is observed that the voltage $V_{Qtr}^{SA1} = -0.21V$ covers the 60.5% of the established range, whereas $V_{Qtr}^{SA0} = -0.78$ V covers the 11% of the established range. Adding the percentage generated by V_{Qtr}^{SA1} and V_{Qtr}^{SA0} is equal to 71.5% (see figure 4.6).

Figure 4.7 shows V_{Qtr}^{SA0} and V_{Qtr}^{SA1} voltages for the benchmark circuit ISCAS'85 C432. The case of 100% selecting factor for OPVEG has been considered. For the stuck-at 0 (1) vector condition it can be observed that some V_{Qtr}^{SA0} (V_{Qtr}^{SA1}) voltages crosses to positive (negative) values. This means that these opens are detectable in the entire range of possible negative (positive) trapped gate voltages. They are detectable

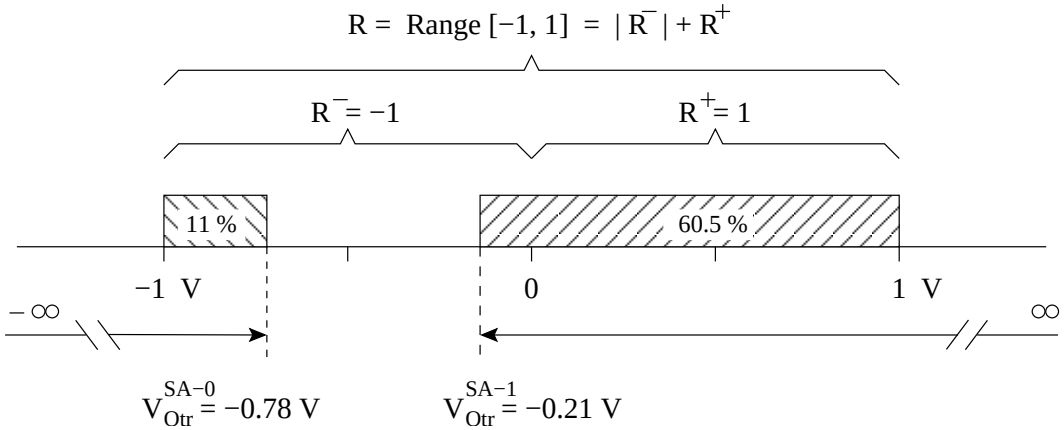
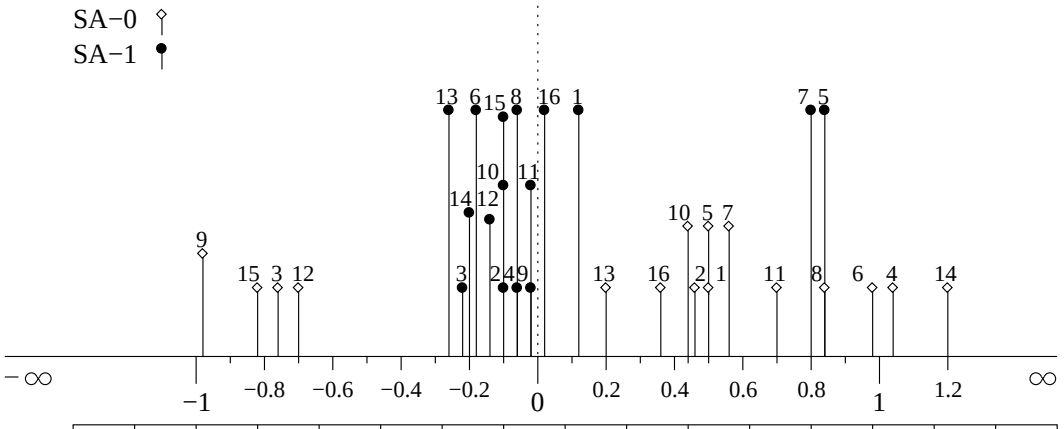


Figure 4.6: Range for voltage V_{Qtr}

in the positive (negative) part depending on the stuck-at 1 (0) vector condition.



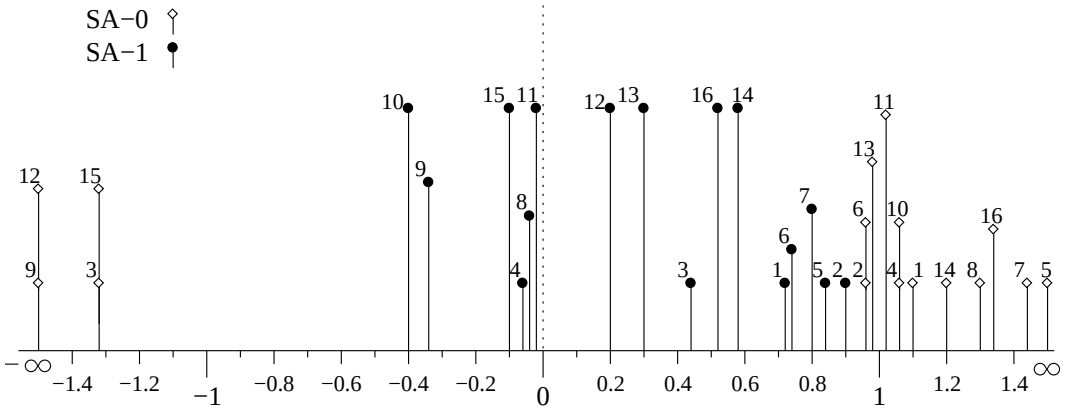
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SA−0	0.51	0.45	−0.78	1.09	0.49	0.97	0.55	0.84	−0.97	0.43	0.71	−0.71	0.20	1.22	−0.82	0.37
SA−1	0.12	−0.09	−0.21	−0.05	0.85	0.19	0.81	−0.04	−0.01	−0.08	−0.01	−0.16	−0.25	0.21	−0.10	0.01

Figure 4.7: Detectable ranges for ISCAS C432 with non-zero values of the trapped gate voltage, Selection factor of 100% *OPVEG*

For those opens with V_{Qtr}^{SA0} (V_{Qtr}^{SA1}) in the negative (positive) side their detectability depends also in the stuck-at 1 (0) vector. Similarly are the data collected for conventional vectors. The data of the tests made for conventional vectors are shown in figure 4.8.

The figure depicted in 4.8 shows the trapped gate voltages for conventional test vec-

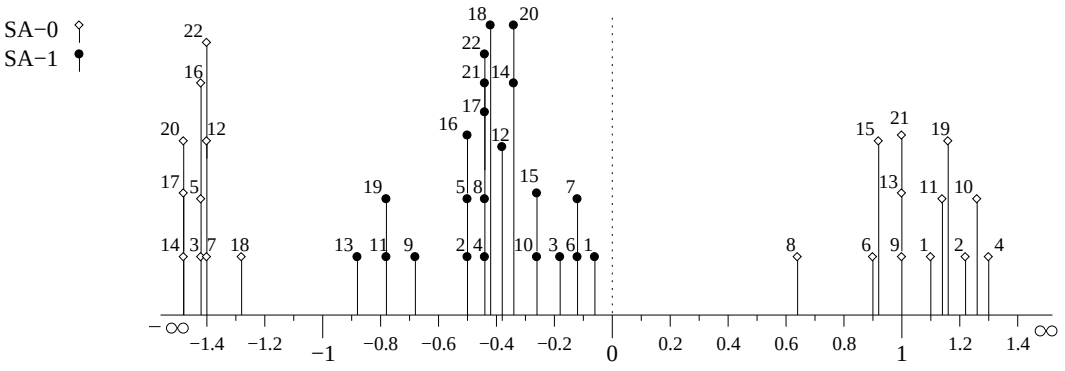
tors. The figure shows a different distribution than those found using the set of inputs vectors obtained by OPVEG. It is possible to observe that exists a smaller number of crossings between values of V_{Qtr}^{SA-1} and V_{Qtr}^{SA-0}.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SA−0	1.13	0.95	−1.36	1.09	1.62	0.97	1.50	1.31	−1.44	1.13	1.07	−1.42	0.99	1.22	−1.36	1.36
SA−1	0.73	0.92	0.43	−0.05	0.85	0.75	0.81	−0.04	0.35	0.40	−0.01	0.20	0.33	0.58	−0.10	0.55

Figure 4.8: Detectable ranges for ISCAS C432 with non-zero values of the trapped gate voltage, Selection factor of 100% *Conventional*

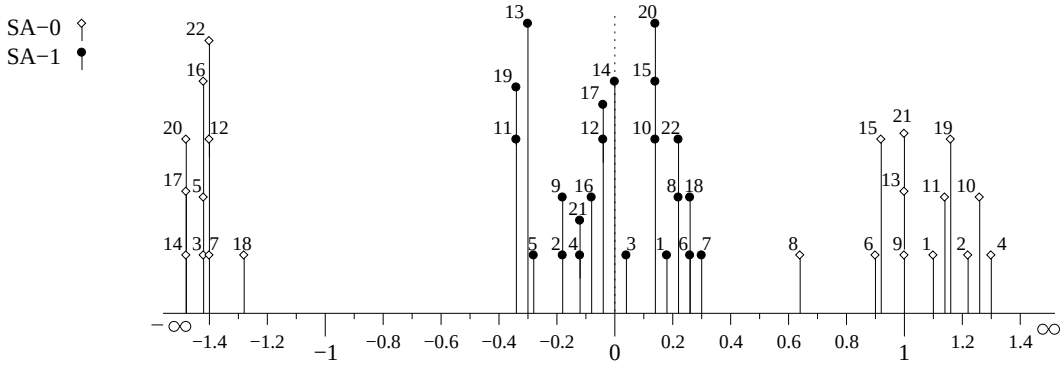
Let's assume that the trapped gate voltage is in the range [-1V, +1V]. In figure 4.8 it is possible to observe that a higher number of opens are in the range established by the voltage V_{Qtr}. As a consequence the defect coverage using the OPVEG vectors is greater than for conventional vectors.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
SA−0	1.16	1.23	−1.43	1.31	−1.41	0.90	−1.40	0.67	1.03	1.27	1.15	−1.40	1.02	−1.42	0.92	−1.40	−1.42	−1.27	1.18	−1.45	1.01	−1.40
SA−1	−0.06	−0.50	−0.19	−0.43	−0.52	−0.16	−0.17	−0.45	−0.69	−0.26	−0.79	−0.39	−0.88	−0.36	−0.28	−0.50	−0.45	−0.41	−0.79	−0.36	−0.44	−0.42

Figure 4.9: Detectable ranges for ISCAS C499 with non-zero values of the trapped gate voltage, Selection factor of 100% *OPVEG*

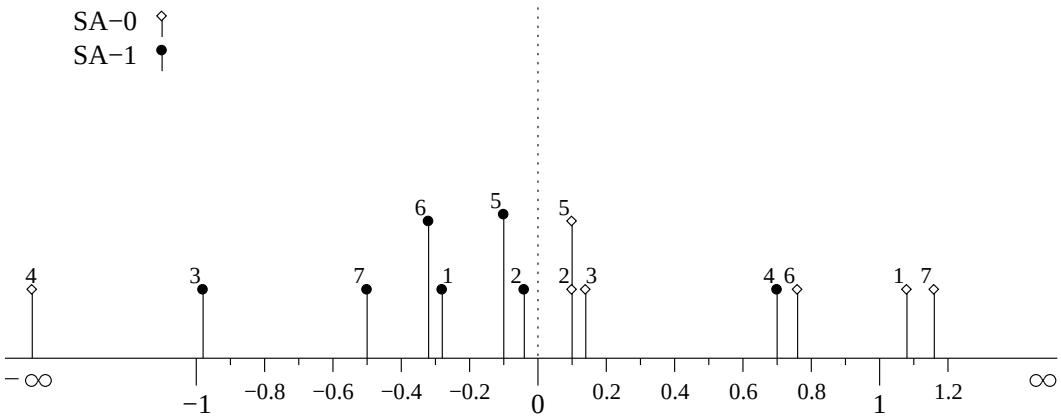
The figures 4.9 and 4.10 shows the voltages for the C499 benchmark circuit ISCAS'85. It is observed that the distribution of V_{Qtr}^{SA-1} for OPVEG, is more negative than the distribution for conventional vectors. The previous thing indicates that the percentage covered in the defined range $[-1, 1]$ is greater by the vectors generated by OPVEG, than the conventional vectors.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
SA−0	1.16	1.23	−1.43	1.31	−1.41	0.90	−1.40	0.67	1.03	1.27	1.15	−1.40	1.02	−1.42	0.92	−1.40	−1.42	−1.27	1.18	−1.45	1.01	−1.40
SA−1	0.19	−0.18	−0.06	−0.15	−0.28	0.26	0.30	0.22	−0.17	0.16	−0.31	−0.02	−0.29	−0.008	0.14	−0.09	−0.05	0.23	−0.36	0.15	−0.13	0.23

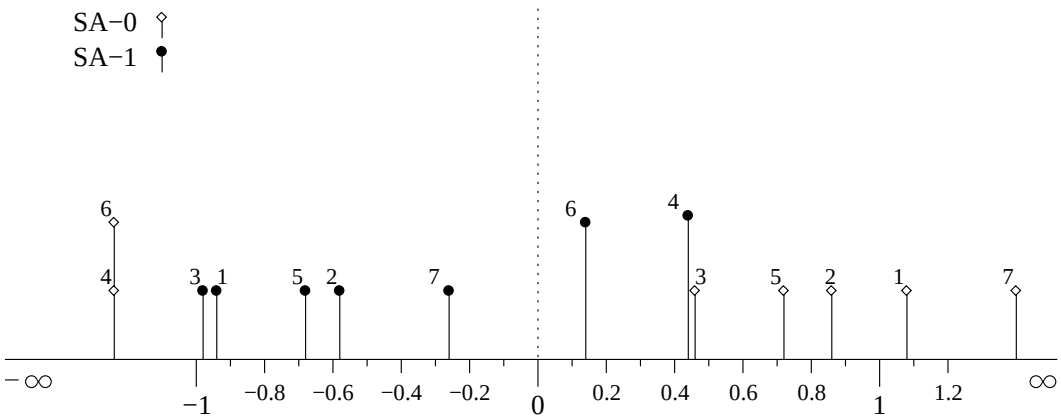
Figure 4.10: Detectable ranges for ISCAS C499 with non-zero values of the trapped gate voltage, Selection factor of 100% *Conventional*

The figures 4.11 and 4.12 show the voltages obtained for the $C1908$ benchmark circuit $ISCAS'85$. Which is appraised that the voltages obtained with OPVEG present a greater number of crossings by 0, this represents a greater percentage of coverage. In addition it is possible to be observed that two of faults *SA-0* have a total coverage (*faults* 1 *and* 7). Whereas two of the faults *SA-0* (*faults 4 and 6*) obtained with conventional vectors (see figure 4.12) do not contribute any percentage.



	1	2	3	4	5	6	7
SA−0	1.07	0.10	0.11	−1.75	0.10	0.75	1.17
SA−1	−0.29	−0.04	−0.97	0.73	−0.09	−0.31	−0.50

Figure 4.11: Detectable ranges for ISCAS C1908 with non-zero values of the trapped gate voltage, Selection factor of 100% *OPVEG*



	1	2	3	4	5	6	7
SA−0	1.07	0.86	0.46	−1.25	0.72	−1.27	1.42
SA−1	−0.93	−0.58	−0.97	0.44	−0.68	0.15	−0.25

Figure 4.12: Detectable ranges for ISCAS C1908 with non-zero values of the trapped gate voltage, Selection factor of 100% *Conventional*

4.5 FASOP Evaluation

In this section the results of applying FASOP to four benchmark circuits ISCAS'85 are presented. First the results obtained for benchmark circuits ISCAS'85 C432, C499, C1908 and C2670 using conventional and OPVEG vectors for zero value of the trapped gate charge ($Q_{tr} = 0$) are presented. Next, the results assuming a certain range for trapped gate charge are presented. The metrics used to obtain the total trapped voltage $V_{Q_{tr}}^{T}$ coverage are presented and a fault of the C432 circuit is analyzed as example.

Let's analyze first the case of zero trapped gate charge. These results are given in Tables 4.1, 4.2, 4.3 and 4.4. Selection factors of 100%, $80\% \ldots 20\%$ have been considered. The tables are divided in four columns, the first column considers different selection factor. The second column contains the information concerning the number of analyzed opens. In column 3 the results using vectors obtained with a conventional ATPG process are presented. Finally, in the last column, the results obtained with the vectors obtained with our developed tool (OPVEG) are presented. The tables 4.1, 4.2, 4.3 and 4.4 showed in this section, present the obtained results of the tests made with OPVEG vectors and compared with the results obtained with conventional test vectors.

Table 4.1 shows the defect coverage of interconnection opens for ISCAS C432. As expected the number of opens increases as the selecting factor has a lower value. For the considered selecting factors, the defect coverage using conventional vectors is between 50% and 69.8%. The defect coverage using OPVEG vectors increases significantly. In this case, the defect coverage is between 68.75% and 79.5%.

$C432$			
Selection factor	# of Opens	Conventional ATPG	OPVEG
100%	32	50.00%	68.75%
80%	50	64.33%	70.00%
60%	88	66.00%	74.20%
40%	200	69.50%	78.00%
20%	314	69.81%	79.54%

Table 4.1: Defect coverage for interconnection opens for zero value of the trapped gate charge.

Table 4.2 shows the results for the ISCAS C499. In the same way as the previous case, the expected number of opens increases as the selecting factor has a lower value. For the considered selecting factors, the defect coverage using conventional vectors is between 52.2% and 71%. The defect coverage using OPVEG vectors increases significantly. In this case, the defect coverage is between 77.3% and 83%.

$C499$			
Selection factor	# of Opens	Conventional ATPG	OPVEG
100%	44	52.27%	77.27%
80%	88	63.76%	78.98%
60%	138	68.77%	80.68%
40%	218	69.31%	81.19%
20%	352	71.01%	82.95%

Table 4.2: Defect coverage for interconnection opens for zero value of the trapped gate charge.

Table 4.3 shows the results obtained for circuit C1908 for zero value of the trapped gate charge. As it can be observed the defect coverage using conventional vectors is between 52.50% and 71.4%, whereas the obtained coverage using OPVEG vectors is between 69.8% and 85.7%.

$C1908$			
Selection factor	# of Opens	Conventional ATPG	OPVEG
100%	14	52.50%	69.78%
80%	40	63.18%	74.17%
60%	90	66.66%	80.00%
40%	182	68.55%	80.00%
20%	388	71.42%	85.71%

Table 4.3: Defect coverage for interconnection opens for zero value of the trapped gate charge.

Table 4.4 shows the defect coverage for the ISCAS C2670. For the case using conventional vectors the defect coverage is between 53.15% and 70.8%, whereas the obtained defect coverage using OPVEG vectors is between 65.3% and 78.7%.

$C2670$			
Selection factor	# of Opens	Conventional ATPG	OPVEG
100%	222	53.15%	65.31%
80%	280	58.57%	73.24%
60%	394	62.94%	73.57%
40%	628	69.84%	74.89%
20%	1406	70.85%	78.68%

Table 4.4: Defect coverage for interconnection opens for zero value of the trapped gate charge.

In the previous results it can be clearly observed than the defect coverage using OPVEG process is significantly improved with respect to the case using a conventional ATPG process. This shows that the effect of controlling properly the coupling signals play an important role in the detectability of interconnection opens.

Tables 4.5 - 4.8 show the obtained results considering a range for the trapped gate charge. Two cases for the range of trapped gate voltages have been considered. Tables 4.5, 4.6, 4.7, 4.8 shows the cases of a trapped gate voltage range of $[-1V, 1V]$ and $[-0.5V, 0.5V]$. The tables are divided in seven columns. The column 1 shows the ISCAS'85 circuits analyzed. The second column considers different selection factors that goes from 100% to 20%. The third column contains the information concerning to the number of analyzed opens. In column 4 the results obtained using OPVEG are presented. The column with the results obtained using conventional ATPG vectors are presented in column 5. Columns 6 and 7 shows the results using OPVEG and conventional ATPG vectors with trapped gate voltage bounded between -0.5 and 0.5.

Expression 4.15 can be used to calculate the defect coverage for the entire set of considered interconnection opens assuming that the range of trapped gate voltage is known. This expression is used for both conventional test and OPVEG test vectors. This expression is as follows:

$$D_{Q_{tr}}^{T} = \frac{\sum_{n=1}^{N} [V_{Qtr_n}^{SA0} + V_{Qtr_n}^{SA1}]}{2N} \times 100 \quad (4.15)$$

Where:

$D_{Q_{tr}}^{T}$ is the total defect coverage for trapped gate voltage range given in percentage (%).
$V_{Qtr_n}^{SA0}$ is the trapped gate voltage coverage for stuck-at 0 test vector between $-\infty$ and 0.
$V_{Qtr_n}^{SA1}$ is the trapped gate voltage coverage for stuck-at 1 test vector between $+\infty$ and 0.
N is the half of the number of faults (*Number of faults*).

Table 4.5 shows the results for the ISCAS'85 C432. The first column shows the circuit under test. In second column the selecting factors from 100% to 20% are showed. The third column shows the number of opens which increases as the selection factor decreases. The defect coverage using OPVEG and conventional ATPG vectors within $[-1V, 1V]$ range is showed in fourth and fifth columns respectively. For the considered selection factors, the defect coverage using conventional vectors is between 84.75% and 90.45%. Furthermore, the defect coverage using OPVEG vectors increases. In this case, the defect coverage is between 89.34% and 95.33%.

			$V_{Q_{tr}}$ **(-1V, 1V)**		$V_{Q_{tr}}$ **(-0.5V, 0.5V)**	
Circuit	Selection Factor	Number of Opens	OPVEG	Conventional ATPG	OPVEG	Conventional ATPG
C432	100%	32	89.34%	84.75%	85.57%	81.99%
	80%	50	90.12%	85.19%	87.68%	84.80%
	60%	88	91.68%	86.92%	91.37%	85.43%
	40%	200	93.45%	91.00%	92.68%	87.09%
	20%	314	95.33%	90.45%	94.85%	89.92%

Table 4.5: C432 For Non-zero values (**bounded**) of the trapped charge.

The defect coverage for the circuit C432 using a gate trapped voltage of $[-0.5V, 0.5V]$ is shown in table 4.5 (columns 6 and 7) . The defect coverage using conventional vectors is between 81.99% and 89.92%. Whereas, the obtained defect coverage using

generated OPVEG vectors is between 85.57% and 94.85%. It can observed that the defect coverages in columns 6 and 7 are smaller than those obtained in columns 4 and 5 (see table 4.5). This is because a lower number of opens are covered for a reduced range of the trapped gate voltage. This will be further explained later.

For table 4.6, are showed the results of C499 circuit ISCAS'85 for ranges of V_{Qtr} $[-1V, 1V]$ and $[-0.5V, 0.5V]$. For the results showed in table 4.6, the defect coverage using conventional test vectors is between 76.64% and 82.63%. Using OPVEG vectors the defect coverage is between 85.97% and 96.13% (columns 4 and 5 in table 4.6). However, the defect coverage in columns 6 and 7 at table 4.6 using conventional vectors is between 75.03% and 80.85%. Whereas, coverage using OPVEG vectors increases significantly. In this case, the defect coverage is between 87.78% and 94.47% (columns 6 and 7).

			$V_{Q_{tr}}$ **(-1V , 1V)**		$V_{Q_{tr}}$ **(-0.5V, 0.5V)**	
Circuit	Selection Factor	Number of Opens	OPVEG	Conventional ATPG	OPVEG	Conventional ATPG
C499	100%	44	85.97%	76.64%	82.78%	75.03%
	80%	88	92.45%	79.90%	90.02%	75.86%
	60%	138	93.12%	80.79%	91.46%	76.02%
	40%	218	94.59%	81.96%	92.65%	79.47%
	20%	352	96.13%	82.63%	94.47%	80.85%

Table 4.6: C499 For Non-zero values (**bounded**) of the trapped charge.

The results of the columns four and five in tables (4.5, 4.6), shows a greater percentage than showed in columns 6 and 7. This must that mainly the range $[-1V, 1V]$ contains a greater number of faults, than the range $[-0.5V, 0.5V]$. Therefore, when being within the established range they cover a certain percentage with the predetermined range.

In table 4.7 are the defect coverage for the C1908 circuit. It is possible to observed like in the results obtained previously for the C432 and C499 circuits , the defect coverage using OPVEG vectors is greater than obtained percentage using conventional vectors. In this case, the defect coverage is between 81.41% and 85.10% using conventional vectors. Comparing these results against the obtained results using OPVEG vectors the difference is significantly greater.

In table 4.7 are the defect coverage for the C1908 circuit. It is possible to observed

			$V_{Q_{tr}}$ **(-1V, 1V)**		$V_{Q_{tr}}$ **(-0.5V, 0.5V)**	
Circuit	Selection Factor	Number of Opens	OPVEG	Conventional ATPG	OPVEG	Conventional ATPG
C1908	100%	14	87.64%	81.41%	85.71%	77.11%
	80%	40	91.71%	80.72%	90.72%	78.26%
	60%	90	93.06%	82.90%	91.30%	82.22%
	40%	182	95.32%	83.34%	93.51%	82.85%
	20%	388	95.56%	85.10%	94.69%	83.56%

Table 4.7: C1908 For Non-zero values (**bounded**) of the trapped charge.

like in the results obtained previously for the C432 and C499 circuits , the percentage of detection cover using OPVEG vectors is greater than obtained percentage using conventional vectors. In this case, the defect coverage is between 81.41% and 85.10% using conventional vectors. Comparing these results against the obtained results using OPVEG vectors the difference is significantly greater.

For the different selecting factors, the defect coverage using conventional vectors is between 87.78% and 92.64% showed in table 4.8. Whereas, the defect coverage using OPVEG vectors is between 92.46% and 94.12%.

			$V_{Q_{tr}}$ **(-1V , 1V)**		$V_{Q_{tr}}$ **(-0.5V , 0.5V)**	
Circuit	Selection Factor	Number of Opens	OPVEG	Conventional ATPG	OPVEG	Conventional ATPG
C2670	100%	222	92.46%	87.78%	89.21%	85.20%
	80%	280	93.38%	89.03%	91.71%	86.35%
	60%	394	92.07%	90.17%	89.38%	86.54%
	40%	628	93.02%	91.51%	89.43%	88.01%
	20%	1406	94.12%	92.64%	92.29%	89.55%

Table 4.8: C2670 For Non-zero values (**bounded**) of the trapped charge.

In columns 6 and 7 are depicted the results of the C2670 circuit for voltage range V_{QTR} between $[-0.5, 0.5]$. It is observed that when decreasing the selection factor increases the defect coverage. Using conventional vectors, the defect coverage is between 85.20% and 89.55%. Using OPVEG vectors the defect coverage is between 89.21% and

92.29%.

For a smaller range of the trapped gate voltage there is a higher number of faults that will not be detected. The results show a difference of defect coverage when reducing the range of the trapped gate voltage. With the objective to explain as the percentage shown in the tables are obtained, we will take the example shown in figure 4.6 from section 4.4.4 (see page 81). Taking $V_{Qtr}^{SA-1} = -0.21V$ ($V_{Qtr}^{SA-1} = 60.5\%$), $V_{Qtr}^{SA-0} = -0.78V$ ($V_{Qtr}^{SA-0} = 11\%$) and making $N = 1$, applying and replacing in 4.15:

$$D_{Q_{tr}}^{T} = \frac{[0.110 + 0.605]}{2} \times 100 = 31.75\%$$

The previous is supposing that single a fault SA-0 and SA-1 is had. The results shown in the tables are for 16 faults SA-0 and 16 faults SA-1 with a selecting factor of the 100%.

4.6 Detectability Analysis

In this section the actual coupling detectability conditions with FASOP (4.6.1) and the effort for generating vectors depending on the values of the coupling capacitances with OPVEG (4.6.2) are evaluated. In experiments 100% of selection factor is assumed. Some opens have 100% defect coverage and others a lower coverage. For both of them logic status at the coupling lines is found. Using this information, it is possible to determine (using FASOP) if for the detected faults, the coupling lines were at the most favorable exciting conditions or not. Also, the logic status at the coupling lines for the non-detected faults are evaluated. This is evaluated for vectors generated with OPVEG tool. Plots with the faults in x-axes and capacitance coupling values in y-axes, for each fault indicate the total value of coupling at 1 and 0 logic level.

On the other hand, using OPVEG for a high coupling factor (100%) the number of faults is fixed. The fault coverage for the condition of 100% of selection factor for the coupling lines is evaluated 4.6.2. While the number of faults remain fixed, the fault coverage for the conditions of selection factor lower than 100% for the coupling lines is examined. This experiment allows to investigate how the fault coverage increases depending on the values of the coupling capacitances with the use of OPVEG for generating favorable test vectors.

4.6.1 Evaluation of actual coupling detectability conditions

In this subsection the states of the coupling lines with the test vectors generated by OPVEG is further investigated. The logical states (1 or 0) at the coupling lines affect the voltage at the floating node. Actual circuits present a high number of couplings. Some of them may have a favorable condition and others not. FASOP is able to give data statistics of the state of all the coupling of the considered interconnect opens. FASOP also gives the defect coverage of each one of the considered opens. This information may be used for attempting to improve the defect coverage of some defects or to take DFT measures.

This is analyzed for the ISCAS benchmark circuit C432 and C19081. A *Selection factor* of 100% is used. The results shown in figures 4.13 - 4.16 are presented as follow: The bar charts represents the number of coupling lines in y-axis. The x-axis represents the considered opens for a selection factor of 100%. Two different bars are depicted in figures 4.13 - 4.16. The white bars are the coupling signals with favorable condition. The black bars are those coupling lines with non-favorable condition.

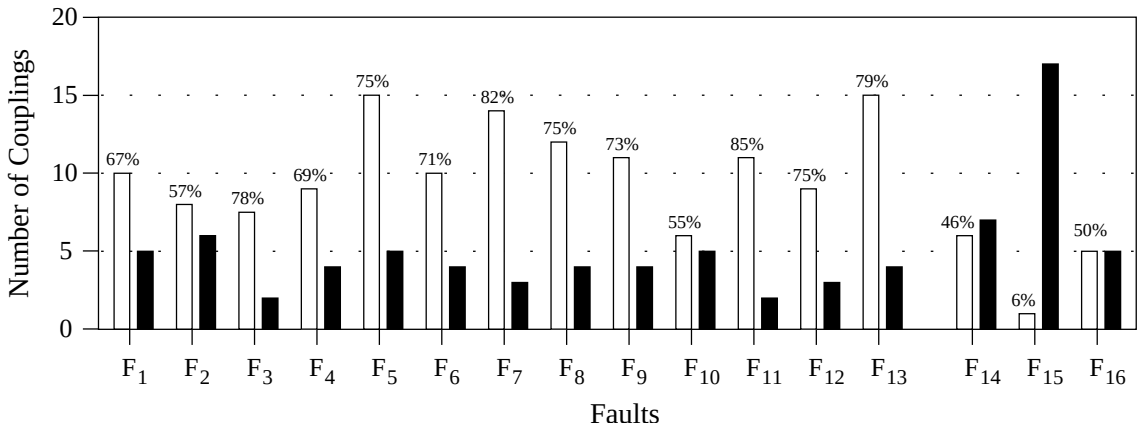


Figure 4.13: C432 stuck-at 0

Sixteen opens are considered for a *Selection factor* of 100%. The number of favorable and non-favorable couplings of each open for the stuck-at 0 case is given in Figure 4.13 The defect coverage for each open is also given. It can be observed that for high number of opens (opens F1 to F13) the number of couplings with favorable conditions is larger than the number of couplings with non-favorable conditions. The defect coverage of the opens tends to be higher as the number of couplings tends to be higher However, for some opens (opens F14 to F16) the number of couplings with

non-favorable conditions is higher than with favorable conditions. These opens tends to have a lower defect coverage. Furthermore open F15 which has a significant higher number of non-favorable conditions than favorable conditions presents a poor defect coverage.

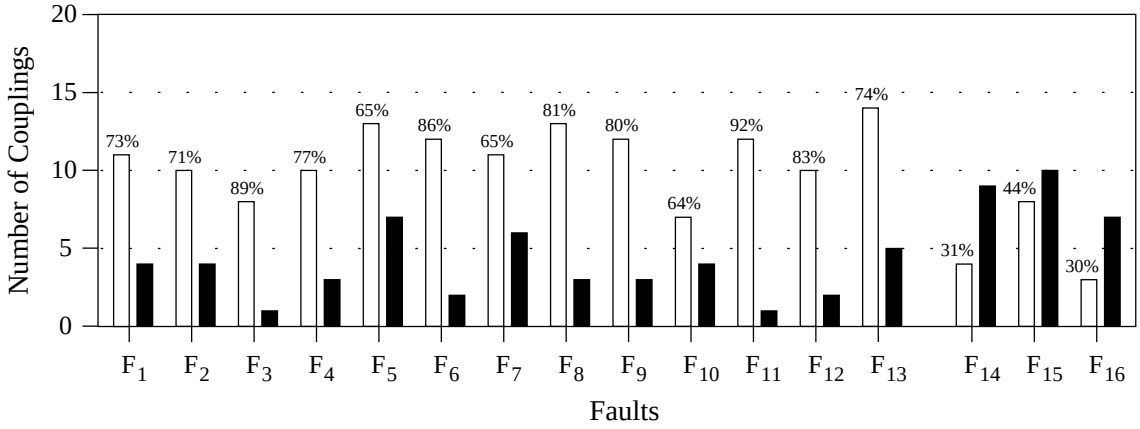


Figure 4.14: C432 stuck-at 1

The number of favorable and non-favorable couplings of each open for the stuck-at 1 case is given in Figure 4.14. A similar behavior to that described for the previous case is observed. Those opens having higher defect coverage present also a high number of couplings with favorable conditions. The last three opens (F14 to F15) also present a higher number of coupling with non-favorable conditions than favorable conditions. The defect coverage is low for these opens.

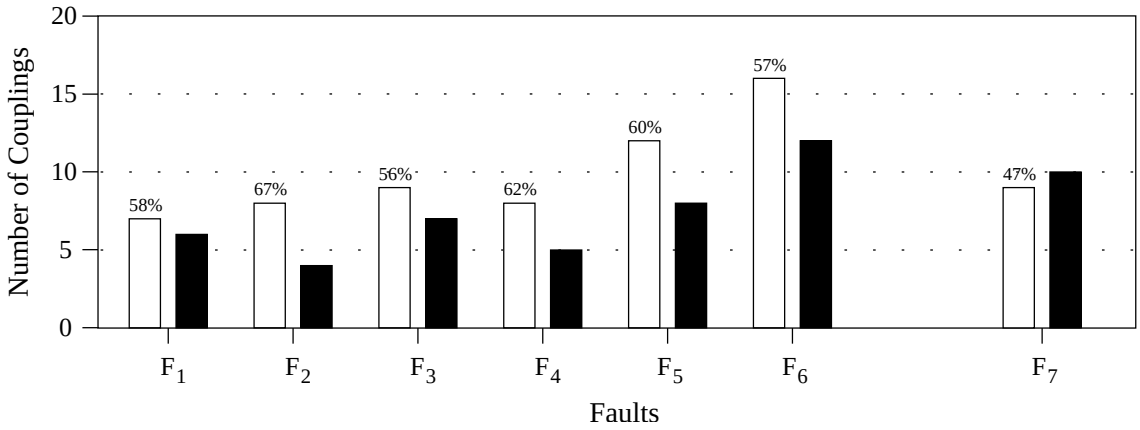


Figure 4.15: C1908 stuck-at 0

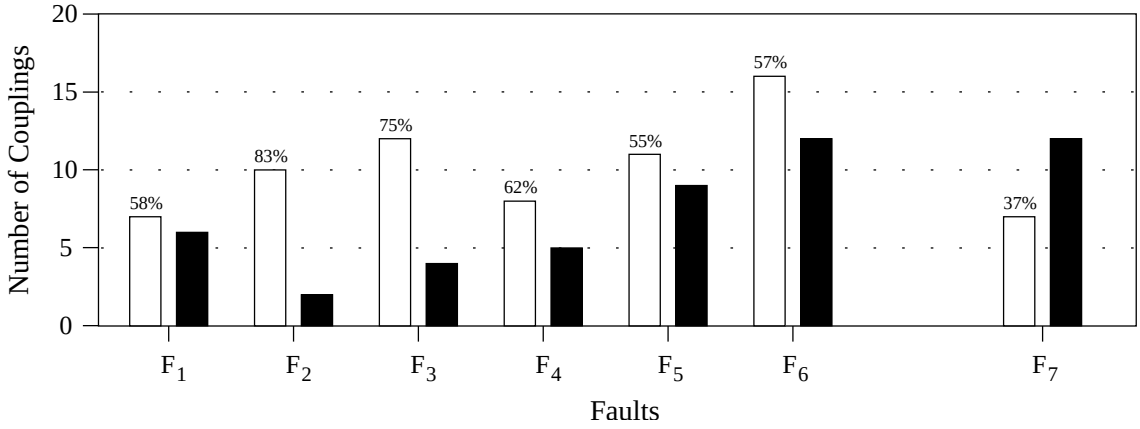


Figure 4.16: C1908 stuck-at 1

Figures 4.15 and 4.16 shows the results of the circuit C1908 for the stuck-at 0 and 1 cases, respectively. Using a *Selection factor* of 100% seven opens are considered. A similar behavior to the circuit C432 is also observed. Opens having couplings with more favorable conditions than non-favorable present higher defect coverages. However, open F7 present more non-favorable conditions than favorable. This open presents a low defect coverage for both stuck-at 0 and 1 cases.

The previous results suggest that the defect coverage may be improved trying to generate better test vectors for those cases presenting low defect coverage. This can be carried-out attempting to generate favorable test vectors, using OPVEG, for couplings with lower coupling capacitance values. This is further investigated in the next subsection.

4.6.2 Evaluation of the effort for generating vectors

In this subsection the benefits of considering more coupling capacitances to generate favorable test vectors is investigated. Until now the *Selection factor* allows to obtain the set of interconnections which are considered by OPVEG. This factor also determine the couplings that are considered by OPVEG. As a consequence some coupling signals may have non-favorable conditions for detection. Because actual circuits present a large number of couplings the benefit, in terms of defect coverage, of the effort (computational time) to consider more coupling signals to attempt to generate a favorable condition needs to be evaluated. To accomplish this the *Selection factor* is used to fix the set of interconnection opens which are used by OPVEG. This tool attempts to

generate favorable test vectors for this set of opens for different *Selection couplings*. Those coupling signals with its capacitive coupling greater or equal than the sum of the capacitance to GND and VDD multiplied a *Selection coupling* are considered by OPVEG.

A *Selection factor* of 100% is used with different values of *Selection Coupling* (100% to 20%).

In table 4.9 are showed the percentage obtained for the critical node $M3/XEC0/Y$ of the C432 circuit ISCAS'85.

The following definitions are used:

- **% Total Favorable**: It gives the relation between the total number of coupling lines with favorable conditions and the total number of capacitive couplings.

$$\%\quad Total\quad Favorable\quad =\quad \frac{Favorable\quad generated}{Total\quad Coupled}\times 100 \tag{4.16}$$

- **% Selected Favorable**: This represents the relation between the number of coupling lines considered by *Selection factor* having favorable conditions and the total number of Selected coupling lines

$$\%\quad Selected\quad Favorable\quad =\quad \frac{Selected\quad Favorable\quad generated}{Total\quad Selected}\times 100 \tag{4.17}$$

- **% Non-Selected Favorable**: This represents the relation between the number of couplings not considered by the *Selection factor* having favorable conditions and the total number of Non-Selected coupling lines.

$$\%\quad Non-Sel\quad Favorable\quad =\quad \frac{Non-Sel\quad Favorable\quad generated}{Total\quad Non-Selected}\times 100 \tag{4.18}$$

An example to illustrate how these definitions are used is given next. Figure 4.17 shows an inverter gate that presents an open at its input. The stuck-at 1 case is considered. The input line of the inverter gate (*floating line*) has 10 coupled lines C_1, C_2,...,C_{10} (***total coupled***). Let's assume a selection factor of 60%. For this factor two critical lines C_1 and C_2 are selected). The remaining coupled lines (C_3, C_4,...,C_{10})

are non-selected. The favorable (non-favorable) states of the coupled lines that favor (unfavor) the detection of SA1 fault are the high (low) logic states.

The figure 4.17 also shows 8 coupling signals generated with favorable conditions. There are a total of 10 coupling lines. From the previous paragraph and applying (4.16) we obtain:

$$\% \quad Total \quad Favorable \quad = \quad \frac{8}{10} \times 100 = 80\%$$

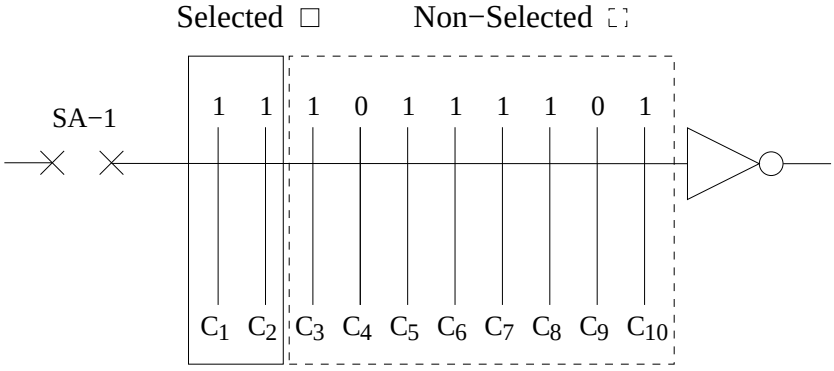


Figure 4.17: Example

In figure 4.17 can be observed that two selected lines were generated with favorable conditions. The percentage obtained, applying (4.17) and replacing the information, is 100%. Finally to obtain the percentage ***non-selected favorable***, it is necessary to count the non-selected lines that were generated with favorable conditions. The figure shows that 6 out of 8 coupled lines non-selected were generated with favorable conditions (C_3, C_5,C_6, C_7,C_8 and C_{10}). C_4 and C_9 . Replacing in (4.18) we obtain the following result:

$$\% \quad Non - Selected \quad Favorable \quad = \quad \frac{6}{8} \times 100 = 75\%$$

Tables 4.9, 4.10, 4.11 and 4.12 shows the obtained results for two opens. These are opens $M3/XEC0/Y$ and $InTbus[7]$ from the C432 and C2670 benchmark circuits ISCAS'85, respectively. The tables are divided in five columns. The column 1 considers different *Selection Couplings* that goes from 100% to 20%. The second column

contains the information concerning to the percentage of *total favorable*. In column 3 the results of *selected favorable* are presented. The column fourth presents the non-selected favorable results. Finally, the coverage of the defect for the particular *Selection Coupling* is give in columns 5.

$C432$ **M3/XEC0/Y**				
Selection factor	% Total Favorable	% Selected Favorable	% Non-Selected Favorable	% Qtr
$f_{100\%}$	46.15%	100%	41.66%	72.95%
$f_{80\%}$	46.15%	100%	41.66%	74.93%
$f_{60\%}$	53.84%	100%	50.00%	75.89%
$f_{40\%}$	53.84%	100%	50.00%	76.01%
$f_{20\%}$	61.53%	100%	54.54%	79.38%

Table 4.9: Evaluation of the effort for generating vectors SA-0.

In table 4.9 ($M3/XEC0/Y$ SA0) is observed that the number of total favorable conditions increases (from 46.15% to 61.53%) as the selection coupling increases (from 100% to 20%). This is because more couplings are considered for the selection coupling to attempt to generate a favorable test condition. OPVEG is able to generate the favorable test conditions for all the couplings in all these cases showed in column 3. Hence, the number of total favorable conditions increase. Column fourth shows the coverage in percentage for those coupling lines that were not selected and OPVEG could generate favorable test conditions (logic states that help to detect the defect). The coverage of *Non-selected favorable* is between 33.33% and 81.81% for different selection factors that go from 100% to 20% respectively. The coverage of the defect is depicted in column 5 ($\%Qtr$). The way of the obtaining is explained at detail in section 4.4.4 on page 81.

Table 4.10 shows the results of node $M3/XEC0/Y$ for stuck-at 1 fault. The results have a similar behavior to the stuck-a 0 fault. In the same way as the previous case, the number of total favorable increases as the selecting factor has a lower value. Selected favorable is 100% for all the considered selection couplings. Non-selected favorables is between 33.33% and 81.81%. The defect coverage also increases as the *Selection coupling* is decreased.

Tables 4.11 and 4.12 shows the results for open $InTbus[7]$ of $ISCAS'85$ *bench-*

$C432$ **M3/XEC0/Y**				
Selection factor	% Total Favorable	% Selected Favorable	% Non-Selected Favorable	% Qtr
$f_{100\%}$	38.46%	100%	33.33%	54.50%
$f_{80\%}$	46.15%	100%	41.66%	59.54%
$f_{60\%}$	46.15%	100%	41.66%	60.66%
$f_{40\%}$	61.53%	100%	58.33%	61.19%
$f_{20\%}$	84.61%	100%	81.81%	63.67%

Table 4.10: Evaluation of the effort for generating vectors SA-1.

$C2670$ **InTbus[7]**				
Selection factor	% Total Favorable	% Selected Favorable	% Non-Selected Favorable	% Qtr
$f_{100\%}$	63.63%	100%	60.00%	54.89%
$f_{80\%}$	68.18%	100%	65.00%	55.08%
$f_{60\%}$	72.72%	100%	68.42%	55.57%
$f_{40\%}$	77.27%	100%	70.58%	64.11%
$f_{20\%}$	81.81%	100%	73.73%	69.20%

Table 4.11: Evaluation of the effort for generating vectors SA-0.

mark circuit C2670. The obtained results are similar to the previous analyzed open. The defect coverage increases as the *Selection coupling* is decreased.

$C2670$ **InTbus[7]**				
Selection factor	% Total Favorable	% Selected Favorable	% Non-Selected Favorable	% Qtr
$f_{100\%}$	54.54%	100%	50.00%	45.44%
$f_{80\%}$	59.09%	100%	55.00%	45.82%
$f_{60\%}$	63.63%	100%	57.89%	47.93%
$f_{40\%}$	68.18%	100%	58.82%	52.86%
$f_{20\%}$	72.72%	100%	60.00%	56.50%

Table 4.12: Evaluation of the effort for generating vectors SA-1.

4.7 Conclusions

In this chapter a general environment under which a CAD tool called FASOP works is described. FASOP has been built using C language (structured) in an operating system Solaris Version 5.8 (UNIX atmosphere) with a compiler GCC version 2.95.1. The program is made up of several subprograms that are executed sequentially. Different files as a circuit logic description and also a layout extracted files are the principal inputs. FASOP take into account different factors that influence the voltage at floating node. Using this information FASOP can evaluate the defect coverage of interconnection opens. A simplified flow chart of FASOP is described.

Also, the different factors that influence the voltage at the floating node are studied. The basic charge equation have been exposed and procedures to estimate the range of detectability of a given interconnection open are described. This process is described starting from a basic electrical model of an interconnection open and five topologies have been identified. Analytical equations for each considered model have been developed. Two basic equation have been developed to assure a stuck-at 0 condition (guaranteed V_{TN}) and a second equation to assure a stuck-at 1 condition (guaranteed $V_{DD} - |V_{TP}|$).

The effects of different coupling lines that affect the voltage of floating line (V_{if}) are considered. Different equations that describe the behavior of this effects are obtained. Section 4.4.3 is oriented to study and analyze the effects of sensitization and unsensitization gates. More than one gate can be connected to the floating line. Depending on the actual input vector it is possible to have a sensitization and unsensitization gates. For the sensitized gates the voltages at the transistor terminals can be known. However, for unsensitized gates the voltages at drain-source terminals of the transistors of the affected gates are unknown for the actual input vector. This impacts the charge at the gate of the affected transistors. As same way, the respective equations of this effect are developed. The trapped gate charge (Q_{tr}) is another important factor influencing the voltage at the floating node. For this reason has been considered the importance to know the effects on the voltage of the coupling line. Different metrics have been developed to obtain the results on C432, C499 and C1908 circuits exposed in 4.4.4.

In section 4.5 the exposed in previous sections is applied. The results using conventional and OPVEG vectors for zero value for the trapped gate charge ($Q_{tr} = 0$) are presented. Cases of study are exposed in comparative tables. The defect coverage obtained from the tests made to four circuits ISCAS'85 with conventional vectors is

between 69% and 71%. The same test using OPVEG vectors gives a defect coverage between 78% and 85%. It can be seen that the defect coverage using OPVEG is higher than obtained whit conventional vectors, from this, it is important to improve conventional ATPG's. Another important test is considering non-zero value for the trapped gate charge. In this results it is possible to see that the results obtained with OPVEG vectors has a higher percentage for all the cases than obtained with conventional vectors.

Finally the actual detectability conditions with FASOP and the effort for generating vectors depending on the values of the coupling capacitances with OPVEG (4.6.2) were evaluated. Cases of study are depicted in histograms and its respective metrics explained. An example applying those metrics is exposed. In addition, tables exposing the effort for generating vectors depending on the values of the coupling capacitances with OPVEG are showed.

Chapter 5

Conclusions

In this thesis a test framework to improve the detectability of interconnection open defects has been proposed. First a test methodology based in applying proper logic states at the coupled lines is proposed. This methodology has been implemented in a CAD tool called OPVEG. Second a fault simulator for interconnetion open defects has been developed. This simulator allows to estimate the defect coverage for these defects.

OPVEG allows to obtain favorable test vectors for interconnection opens using a boolean based test. The tool OPVEG uses layout information and a commercial ATPG (TetraMAX [79]. The main characteristics contained in OPVEG are:

- The operation of the tool is based on the extraction of parasitic capacitances of a circuit.
- OPVEG generate test vectors considering coupling effects using a commercial ATPG. The generation of test vectors uses conditions or restrictions (*constraints*) that define the logical state that some node of the circuit must fulfill for the generation of this vector.
- OPVEG can be used for any combinational circuit. The tool has been applied to four ISCAS'85 benchmark circuits (C432, C499, C1908, C2670).

The OPVEG CAD tool developed was applied to 4 ISCAS'85 benchmark circuits. Test vectors with favorable conditions at the coupled signals were generated.

Several selection factors have been considered. It was found that the logic effectiveness of the tests for all the cases goes from 70% and 90% depending on the topology of the circuit. Another obtained result was to determine if a set of vectors obtained by a

conventional ATPG guarantees a cover of faults that considers capacitive couplings. It was observed that providing a higher percentage of aid to the conventional test (depending on the selection factor) requires a higher number of test vectors, this increases the test time. Therefore, a commitment between the aid to conventional test that provides and the required of number of test vectors.

The time of calculation of the tool considers the ordering of the collected data of the extraction of the parasitic capacitances of the circuits. It also includes the calculation of the selection factor, the identification and the selection of critical couplings. This time also considers the search of the favorable conditions of test making the automatic manipulation of a tool ATPG. This manipulation includes determining the conditions of generation of vectors, accomplishment of the ATPG, reading of results and comparison of such for each critical coupling. Therefore, a smaller selection factor requires a greater time of calculation of the tool because the number of critical couplings increases considerably.

The time of calculation can be higher when the tool is applied to circuits of high complexity (million transistors). In this case a restrictive factor important can be the time of ATPG for an elevated number of constraints. A possible strategy is to consider only those cases of faults in interconnections where the capacitive coupling is important. That is to say, would be taken a high selection factor(e.g. 50% or greater). Another strategy would be to apply OPVEG tool to certain logical blocks of an integrated circuit. The selection of OPVEG could consider blocks that have important routing that it is possible to be translated in significant capacitive couplings. Additionally, also the capacitive coupling is more severe when the routing becomes in superior metal levels.

With the results of the tool cases could be analyzed in which it is not possible to obtain favorable test vectors which they consider capacitive effects. Examples of cases of non-controllability appeared and non-observability. In the first case the suitable logical values in the nodes can not be obtained because this does not allow to obtain the logical value in the node with necessary fault for its detection. In the second case, it is possible to obtain the suitable logical values in the node with fault and the nodes that present couplings with this. Nevertheless, these values do not allow to propagate the fault to the output of the circuit so that it is observed.

The results of the tool OPVEG mainly are focused to the obtaining test vectors, nevertheless, the analysis of the generated data can be useful to identify cases like the described ones previously. With this information focused DFT techniques can be

applied to avoid negative effects in the tests caused by the couplings. For example, when identifying the lines with critical couplings the separation can be increased of the lines in the design of layout to decreases the effect.

The other CAD tool developed was FASOP (Fault Simulator for Interconnection Opens). It was mentioned previously, FASOP was built using C language (structured) in an operating system Solaris Version 5.8 (UNIX atmosphere) with a compiler GCC version 2.95.1. The program is made up of several subprograms that are executed sequentially. The tool is able to evaluates the defect coverage of interconnection opens. Aditionally FASOP also gives useful information to evaluate the test quality of these opens. Based on this information better test vector may be generated to improve the defect coverage of opens or DFT measures can be undertaken. As same way like OPVEG, FASOP uses circuitlogic description and layout information as inputs. The former comes from a high level layout description and the latter from CADENCE [14]. The used test pattern to evaluate the defect coverage may be the vectors generated by OPVEG or vectors obtained by a traditional ATPG process. Some of the principal characteristics contained in FASOP are the follows:

- FASOP is based in a circuit logic description and layout information. FASOP estimates the range of detection for each fault. Using this the defect coverage of interconnection opens is evaluated.

- FASOP includes tasks to determine the number of transistors affected by each one of the critical nodes (***critical nodes. are those that have at least one coupled line with its capacitive value greater or equal than the sum of the capacitive values to*** G_{ND} ***and*** V_{DD} ***multiplied by a "Selection Factor***".)

- FASOP is able to evaluates the defect coverage of interconnection opens. Form this, DFT measures can be undertaken.

- Detectability Analyisis determine if for the detected faults the coupling lines were at the most favorable exciting conditions or not.

Different metrics and analytical expressions have been used to obtain the results showed. Comparatives tables between conventional ATPG and CAD tools developed in this work were exposed. *Trapped gate charge, sensitization and un-sensitization gate effects*, have been considered to determine the voltage on the floating node. Files as a

circuit logic description and also a layout extracted files are the main inputs of the developed CAD tool. Different factors that influence the voltage at floating node are taken into account by FASOP. Using this information FASOP evaluates the defect coverage of interconnection opens. The basic charge equation were exposed and procedures to estimate the range of detectability of a given interconnection open are described. This process was described starting from a basic electrical model of an interconnection open to the full complex model. Analytical equations for each considered model have been used to compute the voltage on the floating node.

Depending on the actual input vector it is possible to have a sensitization and un-sensitization gates. These effects are considered for the developed CAD tool. However, for un-sensitized gates the voltages at drain-source terminals of the transistors of the affected gates are unknown for the actual input vector. This impacts the charge at the gate of the affected transistors. The trapped gate charge (Q_{tr}) is another important factor influencing the voltage at the floating node. For this reason has been considered the importance to know the effects on the voltage of the coupling line. Different metrics were developed to obtain the results on C432, C499 and C1908 circuits exposed in 4.4.4.

The results using conventional and OPVEG vectors for zero value for the trapped gate charge ($Q_{tr} = 0$) are presented. Cases of study are exposed in comparative tables. The defect coverage obtained from the tests made to four circuits ISCAS'85 with conventional vectors is between 50% and 71%. It can be seen that the defect coverage using OPVEG and applying FASOP is higher than obtained with conventional vectors the coverage is between 65% and 85%, from this, it is important to improve conventional ATPG's.

Finally the actual detectability conditions with FASOP and the effort for generating vectors depending on the values of the coupling capacitances with OPVEG (4.6.2) were evaluated. Cases of study are depicted in histograms and its respective metrics explained. An example applying those metrics was exposed. In addition, tables exposing the effort for generating vectors depending on the values of the coupling capacitances with OPVEG are showed. In general, OPVEG and FASOP have been designed that can used for any combinacional circuit independently of their technology.

Appendix A

Gate Charge Equations

The used equations to calculate the charge gates are shown in this section. The equations are obtained from model BSIM level 13 of HSpice Mosfet Models (Synopsis). With the objective to simplify the calculations made by tool CAD (FASOP), the transistors affected by the open interconnections just consider two states either OFF or ON (Vgs$\leq$Vtho , Vgs$>$Vtho respectively). The equations that describe the different regions of operation of the transistor to determine the charge gate are described as follows.

Accumulation Region,vgs$\leq$ vtho, vgs$\leq$zvfb-vsb

$$Q_g = cap \cdot (vgs - vzfb + vsb) \tag{A.1}$$

$$Q_b = -Q_g \tag{A.2}$$

$$Q_s = 0 \tag{A.3}$$

$$Q_d = 0 \tag{A.4}$$

Subthreshold Region, vgs$\leq$ vtho

$$Q_g = \frac{cap \cdot zk1}{2} \left([zk1^2 + 4 \cdot (vgs - zvfb + vsb)]^{\frac{1}{2}} - zk1 \right) \tag{A.5}$$

$$Q_b = -Q_g \tag{A.6}$$

$$Q_s = 0 \tag{A.7}$$

$$Q_d = 0 \tag{A.8}$$

Triode Region, vgs> vtho, vds≤vpof

$$Q_g = cap \cdot (vgs - zvfb - zphi - 0.5 \cdot vds + vds \cdot argx) \tag{A.9}$$

$$Q_b = cap \cdot (-vtho + zvfb + zphi + (1 - body) \cdot (0.5 - argx) \cdot vds) \tag{A.10}$$

$$Q_d = -cap \cdot (0.5 \cdot (vgs - vtho) - body \cdot vds \cdot (0.75 - 1.5 \cdot argx)) \tag{A.11}$$

$$Q_s = -(Q_g + Q_b + Q_d) \tag{A.12}$$

Saturation Region, vgs> vtho

$$Q_g = cap \cdot \left(vgs - zvfb - zphi - \frac{vgs - vtho}{3 - body} \right) \tag{A.13}$$

$$Q_b = cap \cdot \left[zvfb + zphi - vtho + (1 - body) \cdot \frac{vgs - vtho}{3 - body} \right] \tag{A.14}$$

$$Q_d = 0 \tag{A.15}$$

$$Q_s = -Q_g - Q_b \tag{A.16}$$

The different parameters used in the equations are calculated by the tool and introduced in the equations. The tool collects the data of different subprograms and routines including into the main program, when it has collected the data makes the calculations necessary to determine the charge gates affected by faults SA-0 and SA-1.

Appendix B

Algorithms Desription

B.1 Algorithm Description of OPVEG

In the flowchart of the figure B.2 the procedure to obtain the favorable test patterns for those lines considered as critical is depicted. The ATPG tool TetraMAX is used. The input is a file with a list of victims and aggressors nodes. First a victim node is selected (1). Next the number k of aggressors of the selected node is counted. In this way all the possible combinations that can exist to apply constraint conditions at the aggressor lines in the test generation process are obtained (2). The number of possible combinations is $2^k - 1$. Next the test vector is generated. This stage begins with the selection of combinations of constraints in importance order (3). A simple algorithm is used for running ATPG for the different constraints of a critical line. The algorithm gives priority to the signals with higher coupling capacitance [1].

A victim node can have diverse couplings. At the time of the ATPG these coupled lines must remain in certain logic value to favor the detection of defects. Nevertheless, not always all the aggressor nodes can be controlled to aid the detection of a fault. In spite of this, some of the conditions of the aggressor nodes can be fulfilled, reason why must determine of some form as they will be most favorable. The algorithm is based on a method of tree search. In this method priority will occur to the greater capacitive couplings of the aggressor nodes that can be controlled. The following example shows of one more a simpler way the procedure:

Let's suppose a victim node with 4 coupled lines (aggressor lines) ordered of greater to minor according to its magnitude of coupling.

$A1$, $A2$, $A3$, $A4$, with $C_{A1} > C_{A2} > C_{A3} > C_{A4}$

Where C_{A1} is the coupling value of aggressor node $A1$, C_{A2} is the coupling value of aggressor node $A2$ and so on. The operation of the algorithm is showed in figure B.1 where are possible $2^n - 1$ combinations of couplings.

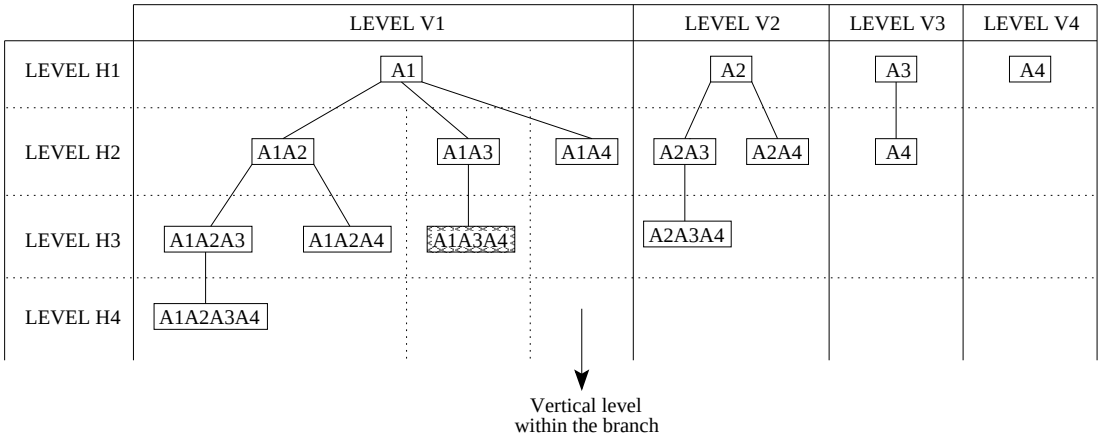


Figure B.1: Example of algorithm search of combinations

In the search, initially priority occurs to the greater couplings (vertical levels of $V1$ to $V4$ or vertical levels within each branch), beginning by the first horizontal level ($H1$). If the proven condition can be fulfilled and it can generate vector (by tool ATPG) advances at the following horizontal level ($H2$ to $H4$). If a condition cannot be fulfilled it advances at the following vertical level. This criterion is applied until arriving at the end of each ramification. Supposing the case in which the aggressor nodes that can be controlled to generate a vector are $A1$, $A3$, $A4$. Initially, proves the condition of $A1$ (level $V1$ and $H1$). This must be fulfilled successful (the ATPG generates vector). Immediately advances at the $H2$ level, where test first combination $A1A2$. In this case vector will not be able to be generated reason why it advances at the following vertical level within $V1$. Of this form the following combination to prove is $A1A3$. In this case a vector will be able again to be obtained reason why it advances in horizontal direction. The following and only combination to prove is $A1A3A4$. In this case vector will be able to be generated and it is the last combination in the branch, therefore it is considered most favorable. In order to find this combination 4 tests of the 15 possible were made. In this algorithm to generate favorable test vector for those capacitive couplings of greater value is searched. If vector for greater value is not obtained it continues in the search of the favorable vector for the following couplingn of smaller value. If it is

possible to be fulfilled (in the example) condition $A2A3A4$ and condition $A1A4$, priority to $A1A4$ will occur to contain a greater coupling ($A1$) in spite of containing less aggressors. This algorithm reduces the number of tests that is made to find the combination most favorable, being very important, since each test of combination means a ATPG. The case in that can be presented the sum of considered capacitive couplings of smaller value in the combination does not surpass the value of capacitance of individual greater couplings. In order to identify these cases a storage of all the conditions can be made that can be generated and be compared the sum of capacitive couplings of all the aggressors in each case. This requires a greater time of processing, a greater time of ATPG (when proving more combinations) and a greater storage of data.

Continuing with the flow of the program B.2 and knowing the node name with fault and constraints that is due to apply it creates a manipulation file that it activates to the $TetraMax$ tool and that indicates the conditions for the ATPG (4). Of course, cases will exist in which it is not possible to be generated the vector with the most favorable conditions due to the topology and operation of the circuit (cases of non-controllability and non-observability). Therefore, the combinations of constraints for each ATPG of a node must be proven and be replaced one by one of such form that identifies that vector that presents more favorable conditions, giving priority to couplings that are greater. Of such form that stops each node can be made more of a ATPG.

The most favorable vector is stored in an exit file (5). If is not vector for any condition it indicates single the name of victim node, and if the single vector fulfills some constraints are indicated as they are. Finally a set of vectors for stuck-at 0 and stuck-at 1 faults of each node will be obtained that could be covered by the ATPG. These vectors will be most favorable considering effects of capacitive couplings.

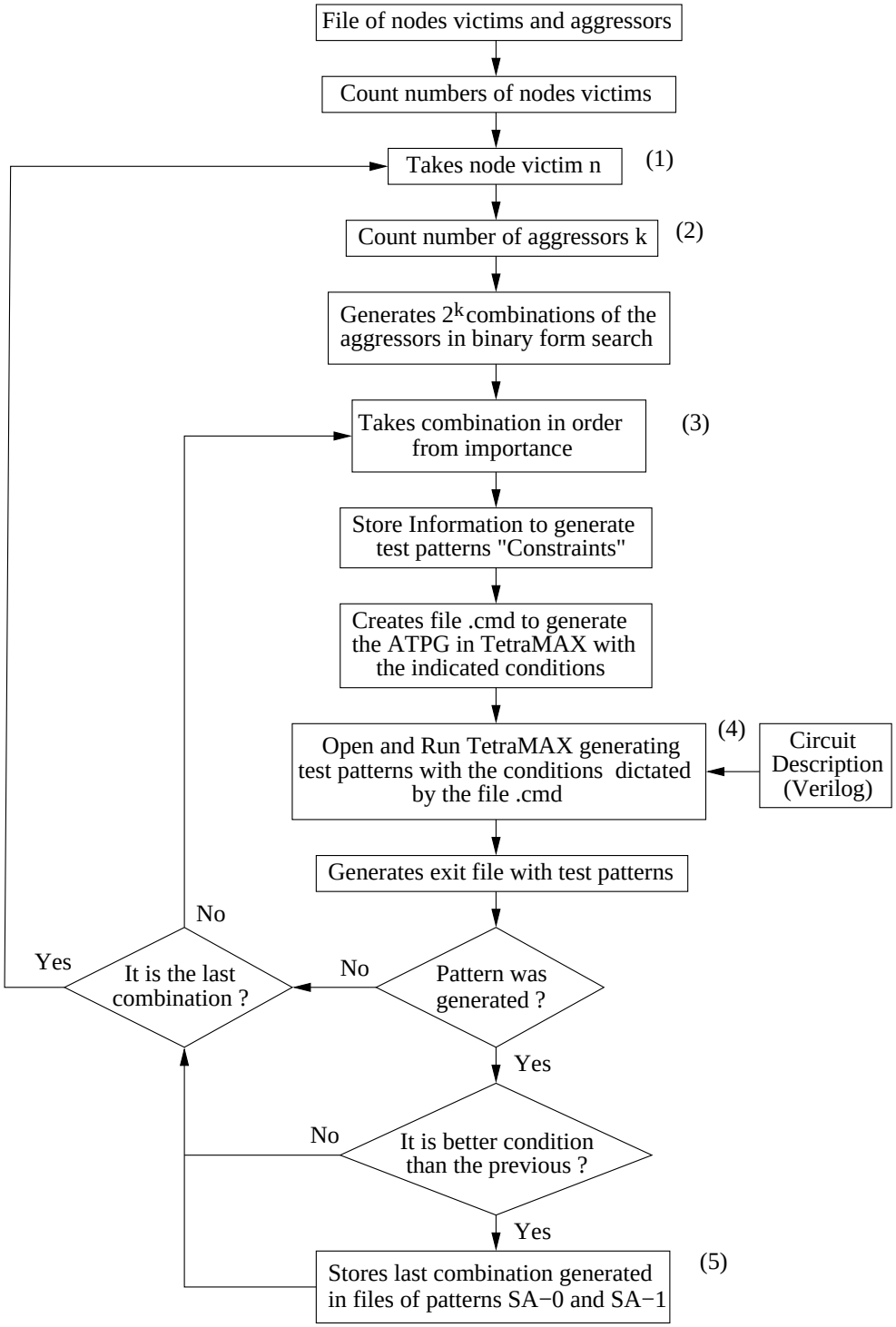


Figure B.2: Sub-program of OPVEG

B.2 Algorithm Description of FASOP

The stages shown in figure 4.2 contain different programs that carry out different tasks. These programs allow to obtain the information of different files later to process it. The algorithm shown in figure B.3 gives the different rutins from operation of this program. The operation is described immediately.

Of the file that contains the critical nodes, a list is created that is stored temporarily in an array. Of the matrix of critical nodes, is selected to the first element (critical node n=0) and it is come to look for all the transistors affected by that node.

With the first node of the array, the search in the file begins that contains the dimensions of the transistors (W and L). This search begins for the first critical node. In case that it does not exist transistors affected by the critical node is returned to the file of critical nodes and another node is selected. For the case that are transistors affected by the critical node it stores the information temporarily and this process is repeated until any other transistor affected by node *n* does not exist. The process is repeated until critical nodes do not exist. Finally the compiled information is stored. A second stage of this program is depicted in the figure B.4. This stage must like objective to obtain the voltages of the transistors affected by the critical nodes. Previously the critical nodes, the affected transistors and their dimensions in an array were stored. The data flow initiates taking the first transistor from first node, and later file of voltages is open and the corresponding relation looks for, when the voltages of the looked for transistor are detected, the corresponding information is stored. This operation is carried out until any other affected transistor does not exist. The program selects a new node and the operation is repeated. Finally all the information is stored temporarily in a file. The following pseudo-algorithm describes the behavior of tool FASOP.

$GetCriticalNode_{init-to-final}$($CriticalNode_{init}$ to $CriticalNode_{final}$)
Begin
WHILE($init \leq final$)
  DO
  {
   WHILE (*Affected Transistors by* $CriticalNode_{init}$ = **TRUE**)
     DO
     {
      Search $Dimensions_{W,L}$ *for each transistor*

```
        }
        ARRAY-A == Store information of affected transistors
      WHILE (Affected Transistors by CriticalNode_init ≤ ARRAY − A)
        DO
        {
         Search Voltages for each transistor
        }
        ARRAY-B == Store information of voltages of transistors
    }
        Increase init
Begin
WHILE(init ≤ final)
    DO
    {
     FOR (Vector_n to Vector_N)
        DO
        {
         FaultSimulationVector_n
         Compute Detection Range
        }
        Increase n
    }
     Evaluate Defect Coverage
```

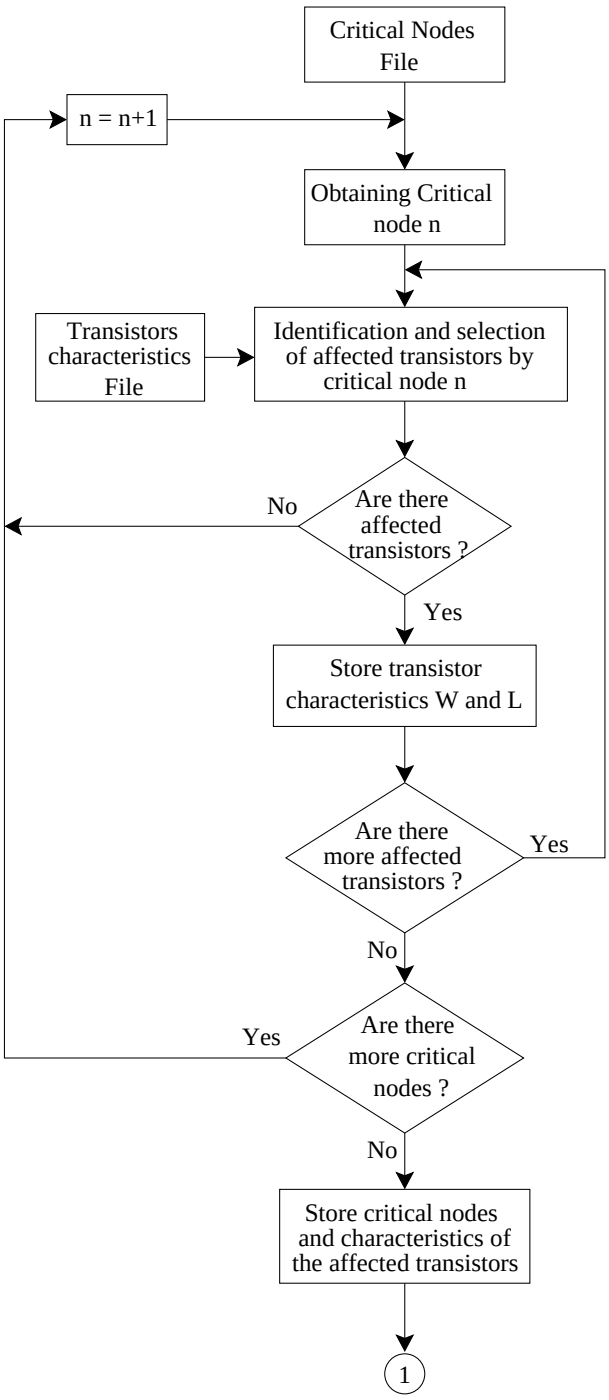


Figure B.3: Flowchart (a)

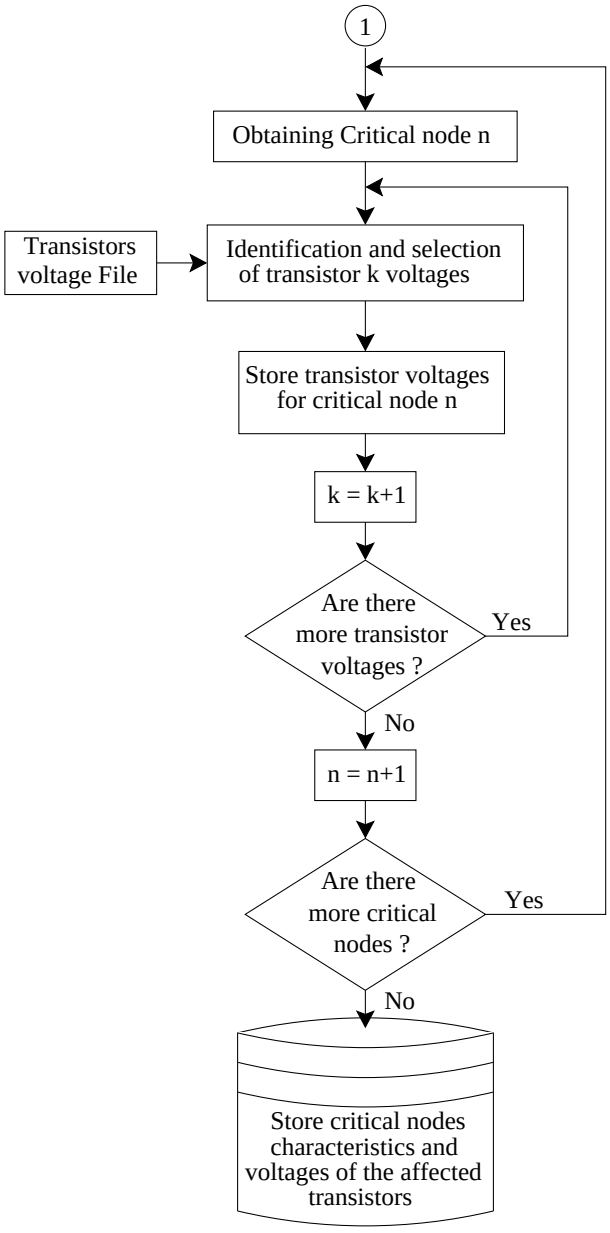


Figure B.4: Flowchart (b)

Resumen

En esta tesis se ha propuesto un ambiente de pruebas para mejorar la detectabilidad de defectos de aberturas en interconexiones. Bajo este ambiente de trabajo se proponen dos metodologías, que en conjunto, permiten determinar si los casos considerados como críticos (líneas de interconexión que presentan al menos un acoplamiento capacitivo) pueden ser detectados o no-detectados considerando sus valores capacitivos , estados lógicos, compuertas afectadas (compuertas sensibilizadas y no-sensibilizadas), además de las dimensiones de los transistores afectados por la abertura en la interconexión. Esta metodología se ha puesto en ejecución por medio de una herramienta CAD llamada OPVEG. La segunda metodología consta de un simulador de fallas para defectos de aberturas en interconexiones (FASOP). Este simulador permite estimar la cobertura del defecto para este tipo de fallas.

Como se mencionó previamente, la finalidad es detectar aquellas fallas que pudieran presentar cierto grado de dificultad para ser detectadas. Por lo que los pasos a seguir para la etapa correspondiente a la herramienta CAD llamada OPVEG serían los siguientes:

- El primer paso que se realiza en el flujo del funcionamiento de la herramienta, una vez con los archivos de entrada correctos, es el ordenamiento de los datos. Un sub-programa de **ordenamiento y formato de la netlist** utiliza la lista de equivalencias de nodos para clasificar los datos almacenados en la lista de acoplamientos del circuito obteniendo tres listas o archivos diferentes. Estos archivos son: Un archivo donde aparecen los nodos con acoplamientos a "vdd", otro donde se muestran acoplamientos de los nodos a "gnd" y por último el que registra acoplamientos entre nodos no globales. En esta parte se realiza también el reemplazo de las etiquetas que se asignan en la creación de la $netlist$ (dada por la extracción de $CADENCE$) por los nombres reales de los nodos (originales en Verilog y usados por $CADENCE$ a nivel esquemático) y la eliminación de

aquellos nodos que corresponden a puntos internos de compuertas lógicas, los cuales no serán considerados.

- En segunda instancia se continúa con el sub-programa que **identifica los acoplamientos críticos** entre nodos víctima y agresores que se determinan de acuerdo al análisis de datos dependiente de los valores de acoplamiento. En este caso se aplica la siguiente metodología:

  Se elige un determinado nodo víctima, se obtiene su acoplamiento con "vdd" y "gnd". Ambos acoplamientos se suman y de esta cantidad se elige un porcentaje determinado (factor de acoplamiento). Si una capacitancia de acoplamiento al nodo víctima supera este valor de referencia, esta capacidad es considerada como acoplamiento crítico.

- Como parte importante de la herramienta se encuentra la **obtención de vectores de prueba** favorables para la detección de fallas *Stuck-at* considerando la existencia de acoplamientos capacitivos. Esta etapa tiene como parte primordial el uso del programa $TetraMAX$. Con la información del nodo víctima que se tenga y los diversos acoplamientos con otros nodos se realizará el ATPG del nodo aplicando "$Constraints$" (limitantes o condiciones) adecuadas dictadas por los nodos agresores. De esta forma se intenta generar el vector más favorable para probar esa falla. Pueden haber casos donde no sea posible generar el vector más favorable debido a la topología del circuito y a la controlabilidad y observabilidad de las fallas. La herramienta obtiene el vector más favorable para cada nodo del circuito en el mejor de los casos. Finalmente se obtiene una lista de vectores para las fallas *stuck-at-0* y *stuck- at-1* de los nodos determinados como críticos.

La herramienta OPVEG permite aumentar la cobertura para defectos de aberturas en interconexiones. Como consecuencia el número de escapes (defectos que las pruebas no detectan) se reduce. Algunas de las principales características de OPVEG son las siguientes:

- La operación de las herramienta esta basada en la extracción de capacitancias parásitas de los circuitos analizados.

- La herramienta OPVEG genera vectores de prueba considerando los efectos capacitivos empleando una herramienta comercial de ATPG. La generación de vectores de prueba emplea condiciones o restricciones que definen los estados lógicos de algunos nodos del circuito.

- OPVEG puede ser empleado en cualquier circuito combinacional. Durante este trabajo la herramienta fue aplicada a cuatro circuitos ISCAS'85 (C432, C499, C1908, C2670).

Para los resultados obtenidos de las pruebas realizadas a los diferentes circuitos ISCAS'85 se consideraron diferentes factores de selección. De los resultados obtenidos se encontró que la efectividad lógica de las pruebas para todos los casos se encontraba entre el 70% y 90% dependiendo de la topología del circuito. Otro resultado obtenido era determinar si un sistema de vectores obtenidos por medio de un ATPG convencional garantiza una cubertura de defectos que considere acoplamientos capacitivos. Se pudo observar que aplicando un porcentaje más alto de ayuda a la prueba convencional (dependiendo del factor de selección) requiere un número más alto de vectores de prueba, y por lo tanto se aumenta el tiempo de cómputo para la prueba.

La tiempo de cálculo de la herramienta incluye el ordenamiento los datos obtenidos de la extracción de las capacitancias parásitas de los circuitos analizados. Dentro de este tiempo también se incluye el cálculo del factor de selección, identificación y seleccin de acoplamientos críticos. También considera la búsqueda de las condiciones favorables de prueba haciendo la manipulaci'on automática de la herramienta ATPG. Esta manipulación incluye la determinación de las condiciones para la generación de vectores, de la realización del ATPG, de la lectura de resultados y de la comparación de estos para cada acoplamiento crítico. Por lo tanto, un factor de selección más pequeño requiere un mayor tiempo de cómputo de la herramienta, debido principalmente a que el número de acoplamientos críticos aumenta considerablemente.

El tiempo de cómputo puede ser más alto cuando la herramienta se aplica a los circuitos de mayo complejidad (millones de transistores). En este caso un factor restrictivo importante puede ser el tiempo del ATPG para un número elevado de resticciones (constraints). Una estrategia posible es considerar solamente esos casos de defectos en interconexiones donde se presentan importantes acoplamientos capacitivos. Es decir, se consideraría un factor de selecció alto (e.g. 50% o mayor). Otra estrategia sería aplicar la herramienta de OPVEG a ciertos bloques lógicos de un circuito integrado.

La selección de OPVEG podría considerar los bloques que tienen interconexiones importantes las cuales se pueden traducir como posibles acoplamientos críticos. Además, también el acoplamiento capacitivo es más severo cuando la interconexión se encuentra en niveles de metal superiores.

Con los resultados obtenidos con la herramienta OPVEG podrían ser analizados los casos en los cuales no es posible obtener los vectores favorables de prueba que consideran los efectos capacitivos. Se presentaron casos de no-controlabilidad y no-observabilidad. En el primer caso los valores lógicos convenientes en los nodos no pueden ser obtenidos porque éste no permite obtener el valor lógico en el nodo con falla, necesario para su detección. En el segundo caso, es posible obtener los valores lógicos convenientes en el nodo con la falla y los nodos que presentan acoplamiento capacitivos con éste. Sin embargo, estos valores no permiten propagar la falla.

Los resultados de la herramienta OPVEG se enfocan principalmente a obtener los vectores prueba, sin embargo, el análisis de los datos generados puede ser útil para identificar casos como los descritos previamente. Con esta información las técnicas enfocadas de DFT se pueden aplicar para evitar efectos negativos en las pruebas causadas por los acoplamientos. Por ejemplo, al identificar las líneas con los acoplamientos críticos se pueden separar y aumentar la distancia entre las que presentan un mayor acoplamiento capacitivo y de esta forma disminuir el efecto capacitivo.

La otra herramienta CAD desarrollada fue FASOP (simulador de fallas para aberturas en interconexiones). FASOP fue desarrollado usando lenguaje de programación C estructurado (versin 5.8) con un sistema operativo Solaris de UNIX (versin 2.95.1). El programa se compone de varios subprogramas que se ejecuten secuencialmente. La herramienta puede evaluar la cobertura del defecto de aberturas en interconexiones. Adicionalmente FASOP también da información útil para evaluar la calidad de la prueba de las aberturas. Basado en esta información mejores vectores de prueba pueden ser generados para incrementar la cobertura de los defectos o medidas de DFT pueden ser implementadas. De igual forma que OPVEG, FASOP emplea como archivos de entrada la descripción lógica de los circuitos e informción del layout. Lo anterior proviene de archivos generados por medio de una extracción de capacitancias parásitas obtenidas con una herramienta comercial CADENCE [14]. El patrón de prueba usado para evaluar la cobertura del defecto pueden ser los vectores generados por OPVEG o vectores obtenidos por medio de un ATPG convencional. Algunas de las características principales contenidas en FASOP son las siguientes:

- FASOP esta basado en la descripción lógica del circuito e información del layout. FASOP estima el rango de detección de cada falla. usando esto, la cobertura del defecto puede ser evaluada.

- FASOP incluye tareas para determinar el número de transistores afectados por cada uno de los nodos críticos (***nodos críticos. son aquellos que tienen al menos una línea acoplada de valor capacitivo más grande o igual a la suma de los valores capacitivos de*** G_{ND} ***y*** V_{DD} ***multiplicado por un "Factor de Selección***".)

- FASOP es capáz de evaluar la cabertura del defecto de aberturas en interconexiones. A partir de esto, se pueden aplicar medidas de DFT .

- Análisis de Detectabilidad determina sí para las fallas detectadas las líneas acopladas tuvieron las condiciones de exitación más favorables o no.

Diversas métricas y expresiones analíticas se han utilizado para obtener los resultados demostrados en los diferentes capítulos de este trabajo. Se obtuvieron tablas comparativas entre los resultados del ATPG convencional y las Herramientas CAD desarrolladas en este trabajo. *Cargas atrapadas de la compuerta*, *efectos de compuertas sensibilizadas y no sensibilizadas*, han sidos considerados para determinar el voltaje en el nodo flotante. Archivos como la descripción lógica del circuito y archivos de extracción son las entradas principales de la herramienta CAD desarrollada. Diversos factores que influyen en el voltaje del nodo flotante son considerados por FASOP. Usando esta información FASOP evalúa la cobertura del defecto de aberturas en interconexiones. Las ecuaciones básicas de la carga fueron expuestas y los procedimientos para estimar el rango de detectabilidad de una interconexión abierta. Este proceso fue descrito partiendo del modelo eléctrico básico hasta un modelo más complejo. Las ecuaciones analíticas para cada modelo considerado se han utilizado para calcular el voltaje en el nodo flotante.

Dependiendo del vector actual de entrada es posible tener compuertas sensibilizadas y no-sensibilizadas. Estos efectos son considerdos por la herramienta cad desarrollada (FASOP). Sin embargo, para compuertas no-sensibilizadas los voltajes en las terminales de drenaje-fuente de los transistores de las compuertas afectadas son desconocidos para el vector de entrada. Esto afecta la carga en la compuerta de los transistores afectados. La carga atrapada de la compuerta (Q_{tr}) es otro factor importante que influencia el voltaje en el nodo flotante. Por esta razón se ha considerado la importancia de

conocer los efectos sobre el voltaje de la línea acoplada. Diversas métricas fueron desarrolladas para obtener los resultados en los circuitos C432, C499 y C1908 expuestos en 4.4.4.

Se obtuvieron resultados usando vectores de prueba generados con un ATPG convencional y vectores de prueba generados con APVEG para valores de cargas atrapadas igual a cero ($Q_{tr} = 0$). Diferentes casos de estudio fueron expuestos en tablas comparativas. La cobertura del defecto obtenida de las pruebas hechas a cuatro circuitos ISCAS'85 con vectores convencionales estuvo entre el 50% y el 71%. Se pudó observar que la cobertura del defecto usando OPVEG y aplicando FASOP fue más alta que los resultados obtenidos empleando vectores convencionales, la cobertura obtenida estuvo entre el 65% y el 85%. De lo anterior se puede conlcuir que es de gran importancia mejorar los métodos convecionales de prueba para circuitos integrados y la detección de fallas en estos.

Finalmente las condiciones reales de detectabilidad con FASOP y el esfuerzo para generar vectores de prueba dependiendo de los valores de las capacitancias del acoplamiento con OPVEG (4.6.2) fueron evaluados. Los casos de estudio son presentados en histogramas con sus respectivas métricas. Así, como tablas obtenidas con OPVEG que exponen el esfuerzo para generar vectores dependiendo de los valores de las capacitancias acopladas. En general, las herramientas OPVEG y FASOP han sido diseñadas para poder ser empleadas en cualquier circuito combinacional independientemente de la tecnología.

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