Identifying and Characterizing the Impact of High-Order Effects in the Signal Propagation on PCB Interconnects

by

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Abstract

High-speed electronic systems are demanding reliable interconnections to serve as communication channels not only inside a chip, but also between chips. For this reason, studying the performance of these interconnects is mandatory these days for optimizing the corresponding structures. As the frequency of operation of electronic systems increases, however, this task is becoming more complicated due to the high-order effects that occur within interconnects at these frequencies. For this reason, studying the most important high-order effects in interconnects is the purpose of this thesis.

Thus, within this project several prototypes were fabricated to carry out an exhaustive analysis of the origins of resonances, parasitic mode excitation and propagation, and other sources of signal degradation in a practical interconnect implemented on PCB. The analysis includes experimental study of these structures but also full-wave simulation of 3D models corresponding to the devices under examination.

From the obtained results effects in the proper propagation of high-speed signals within a practical channel, is observed the dramatic impact of the high-order, which provides valuable insights about the physical phenomena associated with the electrical behavior of interconnects, from simple transmission lines to complex packages.

Contents

Chapter 1 Introduction

CURRENT requirements for faster data processing have lead to a considerable technology evolution of the electronics industry. For instance, the improved fabrication processes and materials have made. The development of transistors that work within electronics systems operating at high-frequencies possible. However, the interconnects used in these systems introduce effects that degrade the quality of the transmitted signals [1]. For this reason, nowadays, some of the most important challenges are those related with the correct operation of the interconnection channels, and the corresponding improvement is a field of opportunities for microwave engineers.

As is well known, the number of transistors that conforms an integrated circuit (ICs) increases in accordance to Moore's Law, which is depicted in Fig. 1.1 This may also be interpreted as an increase in the data processed by the electronic systems. Nevertheless, the transistors represent only about 10% of the ICs, whereas the other 90% consists of elements like resistors, capacitors, inductors, and transmission lines that serve as interconnection elements [2]. All these elements must also be optimized when implementing high-frequency systems.

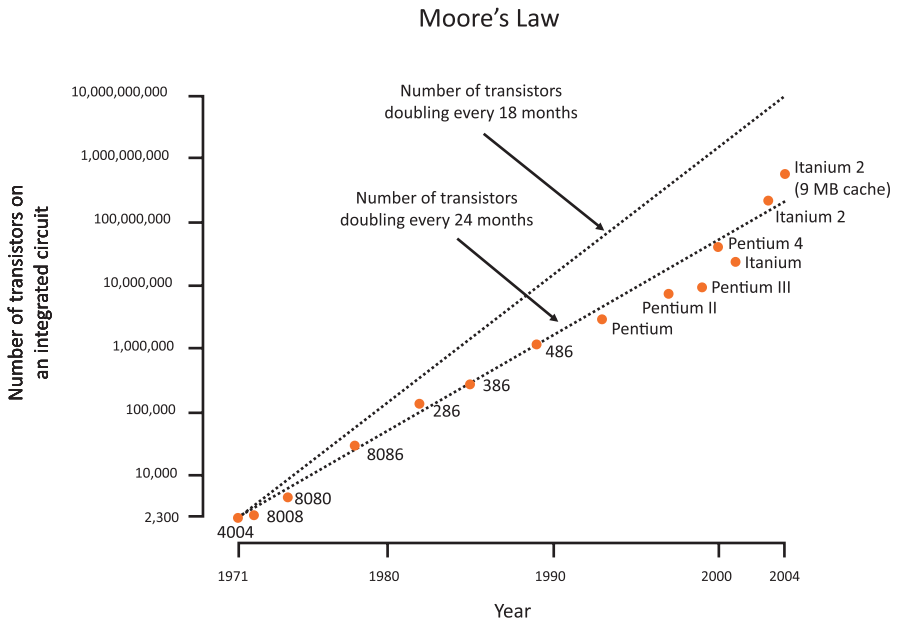


Figure 1.1 Moore's Law (two different interpretations).

Notice, for instance, in Fig. 1.2 that the interconnection channel that guides the signal within an electronic system has to be capable of operating at a such speed that the appropriate communication between a source (transmitter) and a load (receiver) can be achieved.

Figure 1.2 Basic communication system.

Due to the limitations introduced by the losses associated with the materials and structures used in current technologies, the interconnection channels are considered as the bottleneck in the transmission of high-frequency signals. So, among the interconnection effects that degrade the signal quality are reflection, crosstalk, ground bounce, and resonances, just to mention some of the most representative [3, 4]. Furthermore, the complexity of the advanced structures and the increasing density of the devices complicate the analysis and design tasks. These are some of the reasons why the characterization and modeling of this type of structures become mandatory from a signal integrity point of view.

1.1 Chip-to-Chip Interconnection

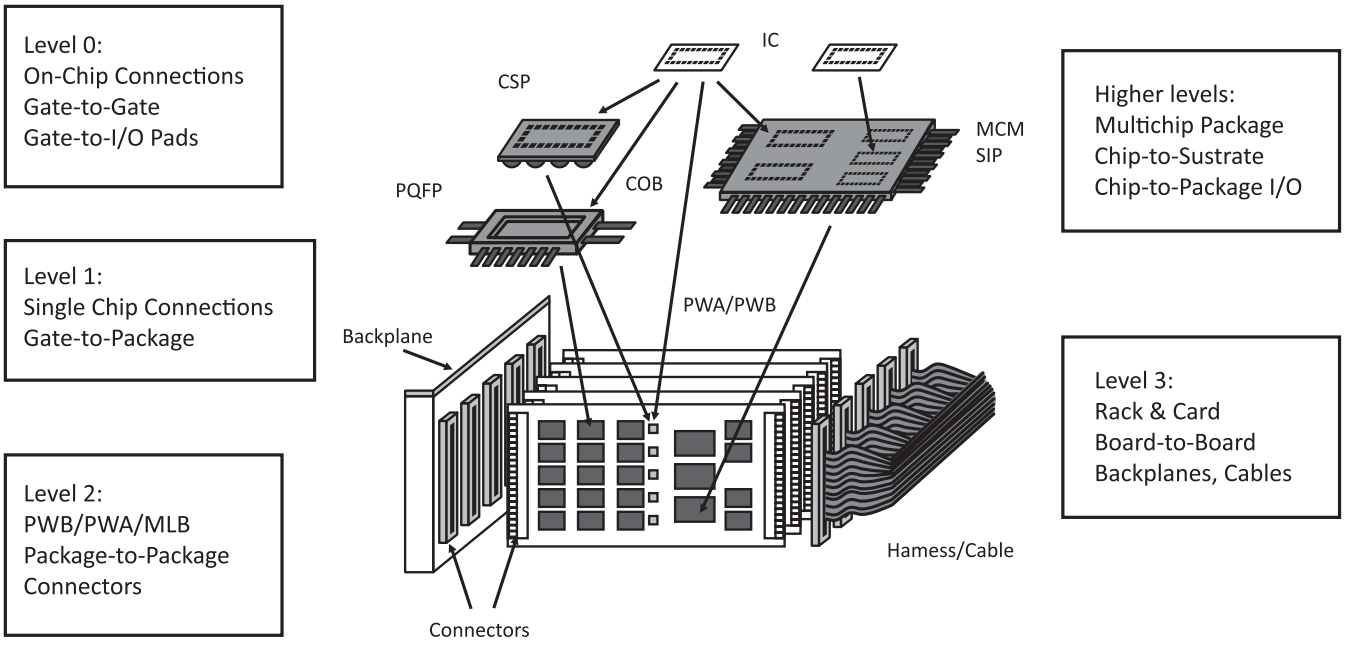
At high-frequencies, the design of the interconnections between chips is more complex than at relatively low-frequencies. Some of the reasons are the increasing density of components (passive and active), the shrinking in the wavelength of the electromagnetic signals, and the several sections composing the interconnection. Thus, in order to distinguish the different interconnection levels within a system, these are classified into different categories referred to as "Levels of Integration". These levels start with the ICs and involve the assembly of the bare die and the packaged components [5, 6], and go from Level 0 to Level 3:

- Level 0: Includes the interconnections of gate-to-gate and gate-to-I/O pads (i.e. all the interconnections inside the chip).
- Level 1: This level refers to the assembly of the die to a package or substrate. Note: when multiple dies are connected to packages or a substrate, there is an intermediate, Level 1.5.

- Level 2: Includes the printed circuit board (PCB) interconnections and relates the connection of multiple bare die or packages through a substrate. Thus, this level represents the interconnections between groups of chips, and between chips and other components like capacitors, resistor, inductors, filters, etc.
- Level 3: Refers to the shell of a small piece of equipment, board-to-board, backplanes, rack&card and cables. In some textbooks this level is also divided into three different sub-levels.

When the corresponding effects associated with each level are appropriately taken into consideration when designing a system, it results in a good performance of the final product. This final product is known as printed circuit board, and provides the mechanical support, electrical interconnection, thermal dissipation, power distribution, and signal path necessary to the adequate functioning of the system (see Fig. 1.3). Some important aspects of this interconnection technology are briefly discussed afterwards.

Figure 1.3
Interconnection levels [4].



1.1.1 Required Bandwidth and Portability

Hi-tech electronics demand high-speed data processing in applications such as video and voice communications, internet, and computing. This drives the development of new devices that allow to complianol with industry requirements. So, thanks to the technology evolution of system architectures, passive and active structures, and materials, it is possible to implement products operating at the required frequencies. In fact, state-of-the-art microprocessors work at tens of gigahertz, which has required the careful design of the electrical channels used to carry out the corresponding interconnections within a system. Thus, when designing these interconnects it is necessary to keep the signal distortion at minimum, and different criteria can be established for this purpose [7]. In this regard, one of the most commonly used criterion is that dictating that a given interconnect has to be capable of transmitting at least up to the third harmonic of the highest speed digital signal, which means that the physical bandwidth necessary to transmit a digital signal of X Gbps (gigabits per second) is roughly 1.5X GHz [8].

Another important aspect associated with current electronics is the portability. Thus, products like the smart cell phones demand good performances in small spaces, which leads to the improvement of the electrical structures to achieve the requirements of integration, cost, and operation. A clear example of this is the

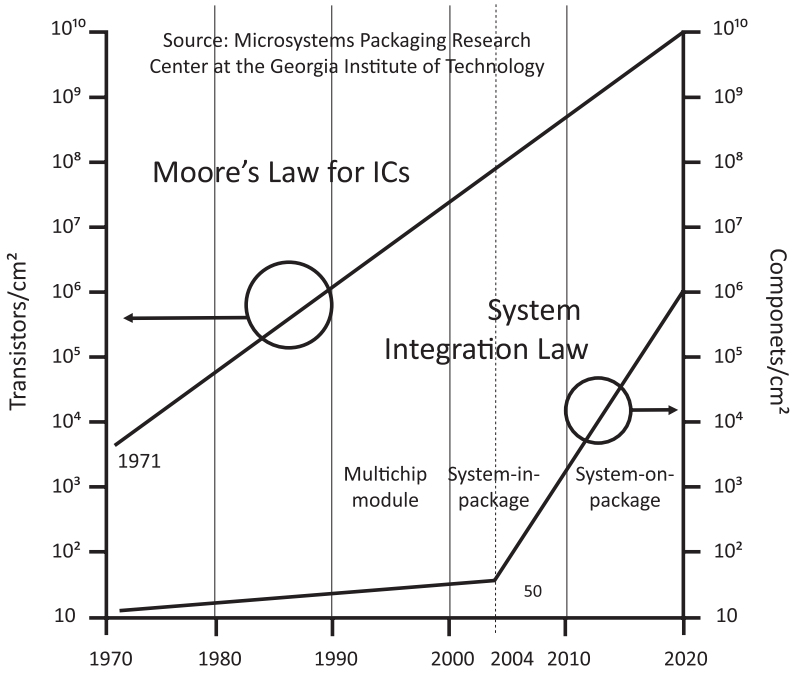


Figure 1.4 Moore's Law and System Integration Law [2].

evolution in the fabrication technology for active devices, which surpassed the 100-nm node this decade [9]. With this accomplishment, the number of transistors on a chip has been considerable increased [2] and a reduced space is occupied for advanced systems, which is so far aligned with Moore's Law as can seen in Fig. 1.4. Moreover, following this concept of compacting a system, other improvements have been made for advanced systems and new integrated structures have been proposed like System-on-Chip (SiC) and System-on-Package (SoP). These proposals introduce the concept of integrating systems inside small substrates an even reaching chip dimensions [10]. However, similarly as in the case of ICs, the interconnections represent the bottleneck in these systems due to the degradation of the signals at high-frequencies. For this reason, in order to solve this problem, new interconnection schemes, multilayer PCBs, multi-integration within packages, and increased interconnection density have been used. In consequence, more advanced modeling and characterization methodologies have to be developed to allow identifying and representing the effects that become important as a result of shrinking the system size.

In addition to the high-speed and compact space requirements, there are other areas where research efforts have to be dedicated. This is the case, for instance, of the thermal dissipation, which is studied using concepts of Thermodynamics. Regarding the electrical part, with the evolution in the techniques used for the fabrication of electronic systems at different integration levels, the introduction of optical signal paths [11], and even quantum computing [12], achieving future requirements seems feasible.

1.1.2 Printed Circuit Board Technology

As mentioned before, the purpose of a PCB used in current electronics systems is providing, among other things, mechanical support for the system components, thermal heat dissipation, and robust interconnection channels between chips and other components. Thus, a PCB can be seen as a substrate which is made of interleaved layers of metal and insulating materials. The insulating material is usually composed of fiber glass with epoxy resins, ceramic, plastic or other dielectric materials, whereas the metal that is commonly used for the electrical interconnects is either cooper or aluminum, but for some applications gold and silver can also be used.

There are several ways of classifying a PCB; for example, taking into consideration the board fabrication techniques, the board selection standards, or the realizable density of the wiring. Thus, when cataloguing the PCB only by the substrate type and the number of layers, a simplified classification is shown in the Table 1.

Table 1
Classification of a PCB.

CLASSIFICATION	CATEGORY	USES
Substrate type	1. Rigid printed circuit board.	Motherboards, communication products, portable devices, etc.
	2. Flexible printed circuit board.	Very compact devices where space and weight are critical.
Number of layers	1. Single- sided and double-sided.	Cost-effective applications (usually, simple circuits)
	2. Multi-layer.	Used in the fabrication of systems requiring large amount of interconnects (e.g. computing systems)

On the other hand, with the increment in the complexity of the electronics systems and the increased density of the corresponding wiring, different schemes of stacking up multiple-layer PCBs have been proposed [13, 14], such as the horizontal arrangement of different sections of a system (2D integration) that may include vertical stacks of layers (3D integration) [9]. Thus, in the multi-layer PCBs used in modern technology, active (transistors, amplifier, etc.) and passive (resistors, inductor, capacitors, etc.) components are interconnected in more complicated but also in a more efficient way. In this case, a typical multilayer PCB is connected with the aid of vias and connectors [15]. Thus, some of the metal layers are etched to form transmission lines or traces that interconnect different components at the same level, but there are other cases where these traces are placed on different layers, and vertical metal posts known as vias are used to connect these traces. In addition, with the aid of vias, the interconnection of ground and voltage planes, as well as the interconnection of components in different layers can be achieved.

In accordance with this discussion, all the interconnects in a PCB, like the ground and voltage planes, the signal traces, vias, and connectors provide a complete electrical path to the transmitted signal, to and from the electrical components. Nowadays, however the design of these PCBs is becoming a more complex

task, due to the non-ideal effects presented in the board, such as magnetic and electrical coupling associated with the closeness of the traces or the imperfections of the return path. In fact, previously, these effects did not represent a problem. Conversely, these days can not be neglected anymore during the design process of a reliable PCB. Several ways to minimize the impact of the imperfections that degrade the PCB performance, have been proposed using an optimized distribution of the active components such as avoiding 90° bends in the traces that can cause signal reflection, avoiding placing parallel traces where electromagnetic coupling (EMC) may occur, or even introducing elements such as decoupling capacitors to control the noise originated by the active devices placed on the PCB [4, 16].

Taking one step further, the future of the PCB technology will be dominated by concepts like the High Density Interconnection (HDI) and the integration inside packages, which are emerging due to three main goals: portability, performance and parts. Thus, the evolution of the PCB is driving the development of new technologies like HDI that makes it possible to implement very small-sized boards presenting the same characteristic as a conventional PCB. Moreover, the trend of integration is accomplished by the integration in 2-dimension or 3-dimension systems mentioned in previous paragraphs. Examples of 2D integration include System-on-chip (SoC) and Multichip Modules (MCM), whereas 3D integration examples are System-on-Package (SoP) [17], System-in-Package (SiP), and System on Wafer (SoW) [8].

1.1.3 Packaging Technology

It is well known that, due to the inherent limitations (such as high dielectric losses), the current trend of "Convergent Systems" [9] will not be satisfied using actual PCB technology. Thus, the evolution of components like packages provides a solution to the necessity of high density interconnection from the new high-speed devices. Up until now, the packages have been seen as the intermediary between the ICs and the PCB, supplying protection and the interconnections necessary from the ICs to a PCB. In this regard, the design of a package involves a series of considerations such as the frequency of operation, materials to be used, cost of implementation, and types of integrated circuits which will be placed on. Nowadays, however, the size of the packages is getting smaller and approaching the chip dimension as in the case of the Wafer-Level-Packages (WLP) [10]. Therefore, the small size of advanced packages implies shorter distances between input-out-

put ports from IC to the PCB paths, improving the performance of the transmission at high frequencies. Furthermore, it makes sense to think that eventually, all the system components will be included within the package and there will be no need for using a PCB. In fact, this is the concept introduced by SoP technologies. In order to point out the fact that a package can be seen as a scaled down version of a PCB, some of the main functions of a package are listed hereafter:

1. Signal distribution, mainly topological and electromagnetic considerations.
2. Power distribution, involving electromagnetic, structural and material aspects.
3. Heat dissipation, structural and material considerations.
4. Mechanical, chemical and electromagnetic protection of components and interconnections.

The packaging technology is continuously evolving taking into consideration all the previously enumerated requirements, and the improvement that these components have undergone in the last decade is remarkable. The package application was initially restricted to serve as an interconnection interface, but now a package may be used to design the complete system [17], which includes passive and active devices. In this regard, SoP seeks to integrate multiple functions into one light-weight compact, thin profile, low-cost and high-performance package system as depicted in Fig. 1.5. One of the most important aspects accompanying the evolution of the electronic packages is the demand for reliable performance at high-frequencies. However, there still are challenges to be faced during the evolution of the structures of the packages, like using materials with low dielectric losses, using cost-effective fabrication processes (e.g. lead-free solder), and including considerations associated with the shock condition requirement. All these effects considerable influence the design process and performance of the system [19].

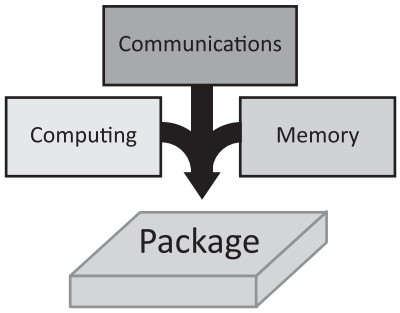


Figure 1.5
Multiple functions inside a package.

1.2 Elements Composing an Interconnection Channel

So far, it has been explained that the electronic systems consist of several levels going from the chip to the PCB level. Within these levels, an interconnection channel suffers several transitions that impact the integrity of the signals that need to be transmitted from one point to another within the system. These transitions can be understood once that the different types of interconnects composing a complete channel are identified. These concepts are briefly discussed in this section.

1.2.1 Transmission Lines

This work is focused on the transmission of high speed digital signals on PCB, and the traces used to interconnect the chips together on a PCB have to be considered as transmission lines due to the high frequencies involved with the data transmission. The most common planar lines used in PCB technology are microstrip and striplines. The main difference between microstrip and stripline is the reference plane. The microstrip presents one reference plane below (or above) the line, whereas the stripline presents two reference planes, one below and one above the line. In consequence, these two structures present a different distribution of the electromagnetic fields, which originates that these lines present different electrical behavior (e.g. different characteristic impedance). The electromagnetic waves travel through these lines in a quasi-TEM (Transverse Electro-Magnetic) propagation mode. Fig. 1.6 shows a cross section view for the case of a microstrip

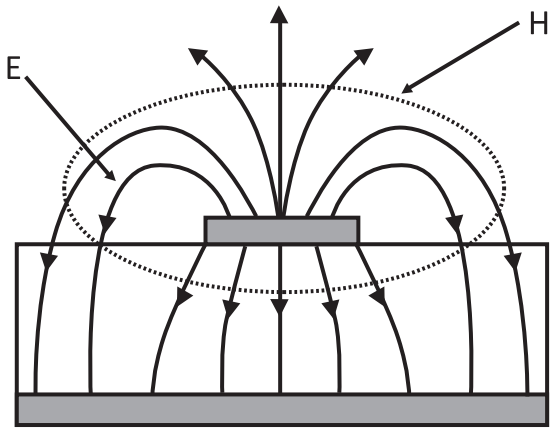


Figure 1.6
TEM field in a microstrip transmission line.

transmission line depicting the lines associated with the electric and magnetic fields [20]. As can be found in basic textbooks, these lines can be modeled at high-frequencies using the well known transmission line model consisting of a series of lumped elements in cascade as can be seen in Fig. 1.7. The resistor R represents the losses due the finite conductivity of the metal trace, G represents conductance associated with the dielectric losses, L allows to represent the magnetic field generated by the current in the signal line, and finally C allows to represent the electric field between the signal line and the references plane. This representation is known as the RLGC model of a transmission line [15]. Thus, as the signal is propagated though the line, attenuation and delay mechanisms occur. Understanding these mechanisms is of great importance when designing a chip-to-chip channels in order to identify the critical effects degrading the integrity of the transmitted signal.

A point to be mentioned here is the fact that, the most important characteristics of a transmission line are associated with two parameters: the characteristic impedance Zc and the propagation constant γ. The information provided by these parameters allows one to predict the performance of the transmission line, and consequently to establish criteria for carrying out an optimization process. Among the improvements that can be carried out while analyzing the characteristics of a transmission line through the experimental γ and Zc are:

1. The development of new materials with a low dielectric constant, to reduce the losses by dielectric materials [18].
2. Proposal of new schemes of signaling, like the one using differential traces [21].
3. Proposal of new structures and fabrication schemes [22]

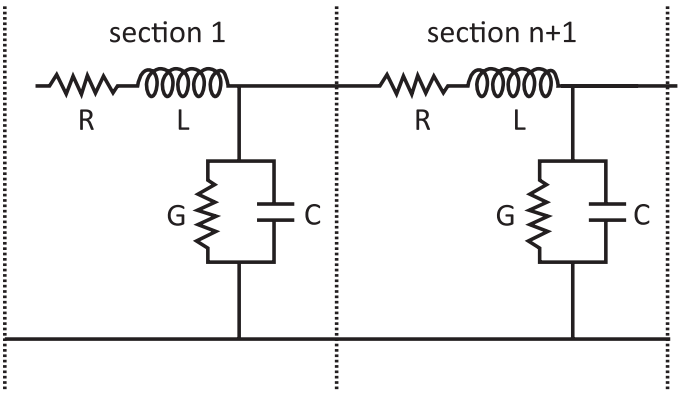


Figure 1.7
Lumped model of a transmission line.

1.2.2 Connectors

The connector is a necessary element to join an IC with the package, or the package with the PCB, and is usually present at the Level 1.0 and Level 2.0 of integration. The connectors serve as intermediary between components because the size of the traces on the PCB considerably differs from those corresponding to the I/O ports of the ICs and the packages. These days, the connectors have evolved from a basic passive device to a very sophisticated element in high-speed circuits [19]. In fact, in the past, the performance of a connector was evaluated by taking into account only the resistive behavior and the current-voltage capacity. Conversely, in today's technologies the design of connectors for high-speed circuits involves impedance matching, crosstalk, insertion loss and propagation delay, which are the effects that influence the corresponding performance at high frequencies since they represent the common causes of poor quality in signal transmission [15].

There are different requirements for the connectors depending on the application. Thus, the connectors can be permanently interconnecting devices (e.g. those using solder ball arrays) or give the possibility of interchangeability (e.g. the pin-grid-array or PGA sockets) [23]. In this regard, when interconnecting chips it is common to find solder ball I/O and wirebonds (see Fig. 1.8) [19], both connectors have a good performance at high frequencies and provide additional shielding to control the system noise and crosstalk.

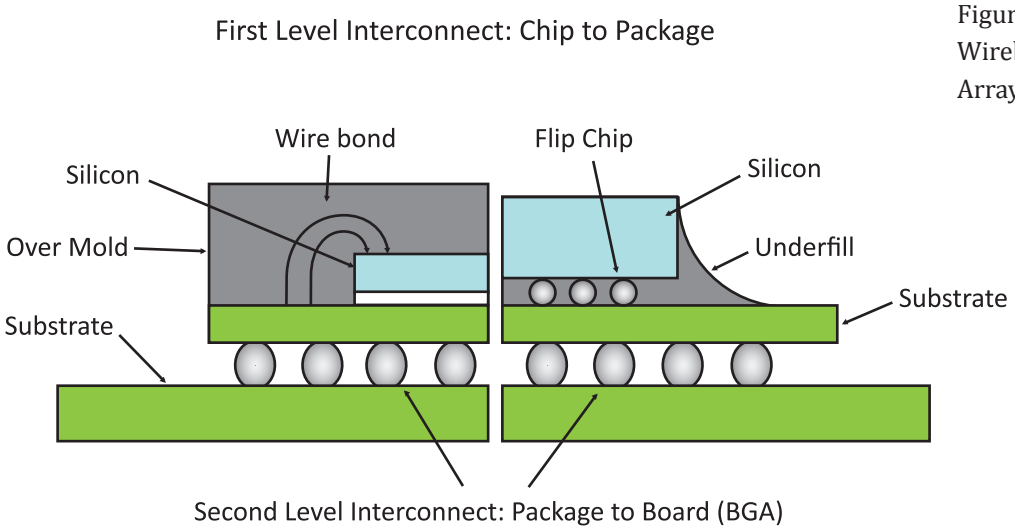


Figure 1.8
Wirebond and Ball Grid Array connectors.

From the fabrication perspective, using wirebonds implies a simple process. However, as the frequency of the transmitted signal increases, a thorough understanding of the metallurgy, thermodynamics, and chemistry involved in the process of fabrication is required to understand the actual behavior of these interconnects [24]. For this reason, several models for wirebonds have been proposed involving several parameters such as the length of the wire, the ground plane, and the bond-finger space. When optimizing a design, these parameters should be selected so that low loss, low inductance, and impedance matching in the connector can be achieved.

Another popular connector is that using solder balls, which are tiny globes of solder that provide the contact between chips, chip-to-package, package-to-package, and to the PCB. A solder ball can be found in many types of arrays; for instance, in the most popular packaging for devices with high density of input/output interconnections, which is the Ball Grid Array (BGA). The small size of a BGA makes it possible to fit into a smaller footprint within a board, decreasing the pitch spacing and thus allowing higher density of input/output interconnects. Moreover, the fabrication of devices using BGAs like the Flip Chip (FC) allows to considerably reduce the length the electrical path at the interface and consequently reduces the corresponding inductance, which is one of the effects that degrades the quality in the transmission of high frequency signals. The application of the solder balls can be found in microprocessors, memory, and other chipsets [25]. Fig. 1.8 shows a simplified sketch of BGA and wirebond connectors, whereas in the Table 2 a simple performance comparison is presented.

Table 2
Performance comparison between the Wirebond and Ball Grid Array.

	WIREBOND	FLIP CHIP
Inductance	High	Low
Cost	Low	High
Crosstalk	High	Null
Mechanical	Good	Regular
Thermal Dissipation	Good	Bad
Size	Big	Small

1.2.3 Return Path

Another important part composing any interconnection channel is the return path, which is briefly discussed here. The loop through which the current flows is conformed by two sections (see Fig. 1.9), one is from the source to the load, known as the "signal path" and the other is from the load to the source. The latter is the so called "return path" or "ground path", which is ideally considered as a perfect conductive path but in an actual implementation can be defined as a "low impedance path for the current to return to the source" [26]. This means that the ground plane presents a finite impedance that changes with the frequency and should not be ignored during the design of devices operating at high-frequency.

There are many causes for the return path to present adverse effects, such as the gap between the ground and power planes in multi-layered boards, the meshes used for these planes in ICs, the interactions between signal and power delivery networks, electrical transitions, and many other. All these effects degrade the signal transmission, and can be categorized as originated by a poor grounding, and may yield:

1. High insertion loss.
2. Poorly matched input ports.
3. Unwanted radiation.
4. Crosstalk.
5. High inductance.
6. Poor isolation between Input and Output Terminals.
7. Increased electromagnetic interference (EMI).

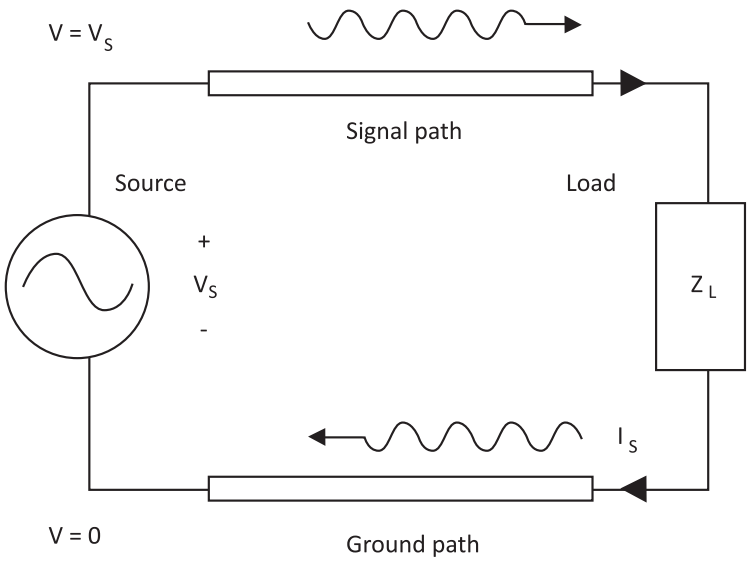


Figure 1.9
Sketch illustrating the signal and return paths in a generic electrical circuit.

Fortunately, several actions can be taken to improve the return path and minimize the associated signal degradation [27]:

1. Introduction of a shielding plane.
2. Placement of vias to short-circuit planes.
3. Using differential signaling schemes.
4. Dividing ground planes with electromagnetic gaps to avoid unwanted propagation.
5. Using decoupling capacitors.
6. Dividing the PCB in sections to avoid coupling between DC and HF devices.

In fact, nowadays a variety of tools can be used to model the current path, which allows identifying and minimizing the corresponding adverse affects through a design optimization. Thus, bear in mind that all these effects should be taken into account when carrying out physically-based designs employing the 3D tools since idealized models do not consider effects like the finite conductivity and the finite impedance of the actual materials, or some defects in the layout of the structures.

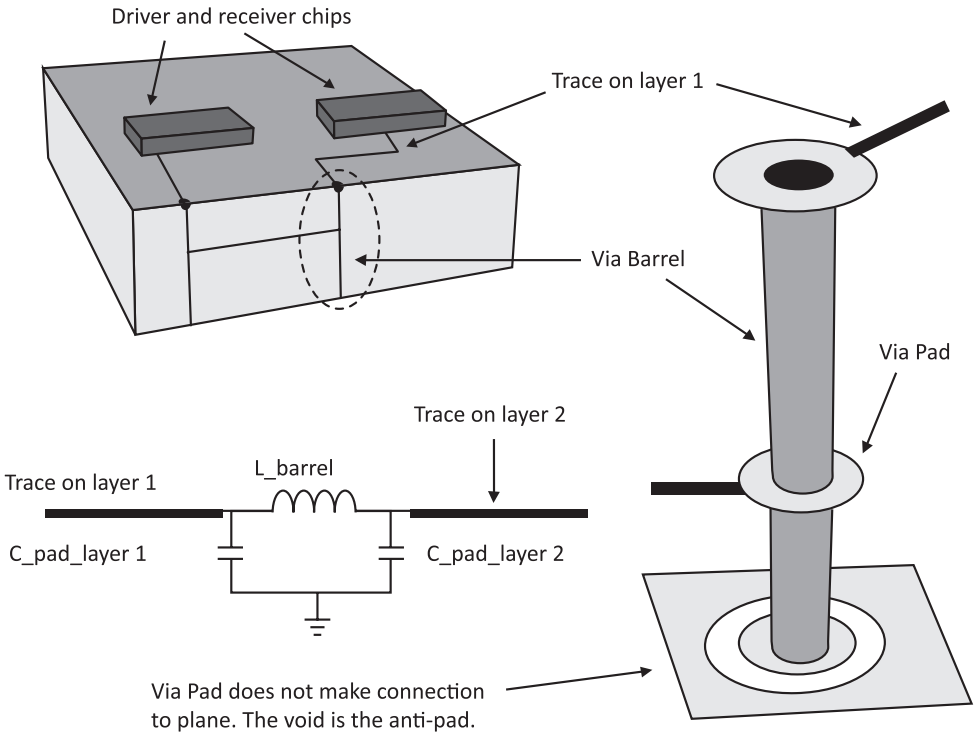


Figure 1.10
Equivalent circuit of a through-hold via [15].

1.2.4 Vias

Vias are vertical interconnects that are present inside chips, packages and PCBs and their function is to carry signals from one level to another. A via typically consists of a barrel, a pad and an antipad as can seen in Fig. 1.10. The most common via is the through hole via, which is made by drilling a hole between layers and filling, it with a metal or conductor to make the connection; other types of vias are the blind via, the step via, the buried via, the stacked via and the microvia. All these are illustrated in Fig. 1.11.

Within an electronic system, the vias are used with the following proposes:

1. Mounting a through-hole component to a board.
2. Interconnecting traces on different metal layers.
3. Short-circuiting metal planes to keep the potential as close as possible between layers.

Electrically, the vias are often modeled with a lumped pi-model, having an inductive and capacitive parasitic value. This model (shown in Fig. 1.10) is valid when the time delay associated with the via is considerably larger than the edge rate associated with the signal. In this model, each lumped element represents a parasitic effect physically observed in the structure. These effects can be modified by changing the via dimensions; for example, a small via pad will present a relatively small capacitance, whereas a short-length via will present a low inductance. In addition, it is important to mention that the effects originated by the vias

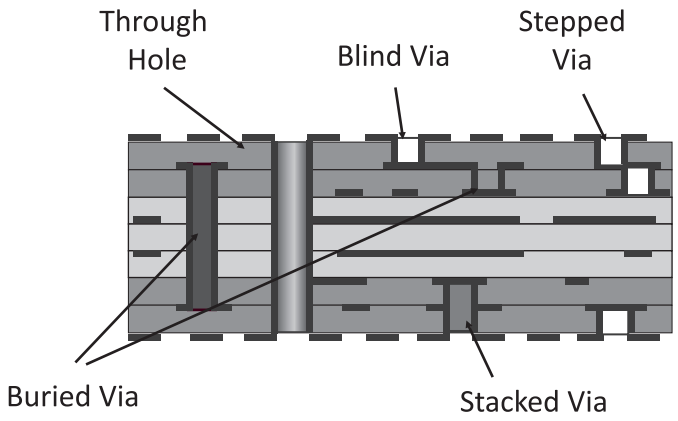


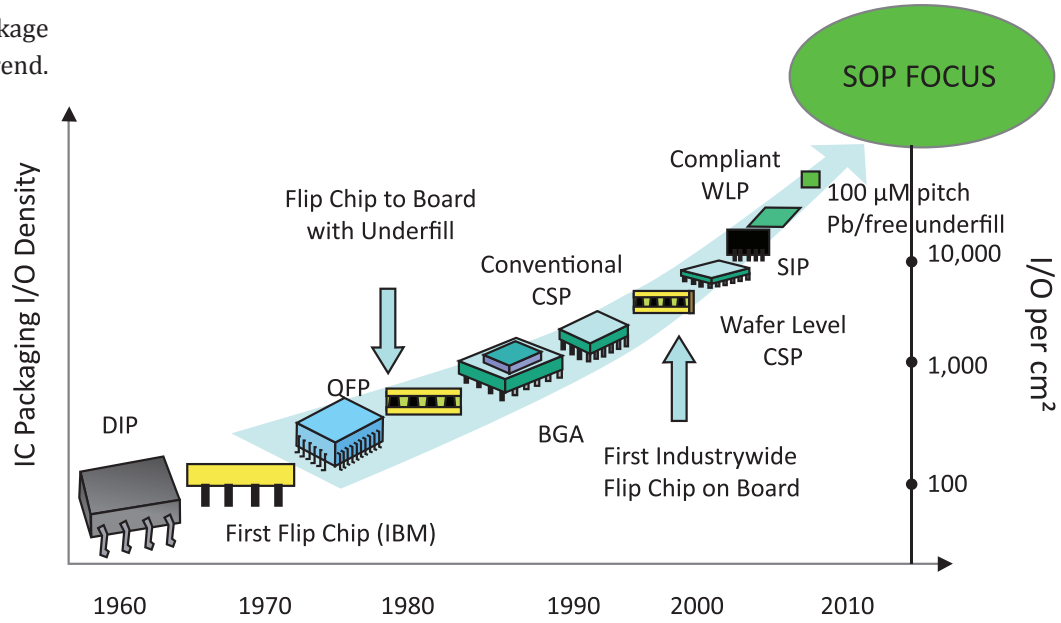
Figure 1.11
Types of vias.

cause unexpected impedance discontinuities that cause transmission problems, whereas the capacitance also slows down the rising time of the propagated digital signals. Although both effects degrade the signal transmission, the inductance effect is more accentuated in the via design and there are some actions that can be taken to minimize it; for example [28]:

1. Using the upper layers for high-priority supplies.
2. Avoid using long vias that can behave like stubs.
3. Decreasing the distances that the current travels through the vias,
4. Placing ground planes to shield the transmission and avoid unwanted propagation at high frequency.
5. The high-speed signal traces should be routed on as few layers as possible, thus limiting the number of vias.

Since the interconnection technologies are evolving to using HDI, and the principal difference between HDI and PCB is the technique of fabrication of vias, these components are becoming very important within an electronic system. Thus, several advances are occurring in this direction. For instance, to have thinner dielectric layers the HDI technologies have introduced the fabrication of small vias named microvias (vias with diameters of 150 μm or less). Furthermore, there are new and exotic fabrication techniques in the microvia building, like laser ablation, photoimageable dielectric (PID), plasma etching, and others [29].

Figure 1.12 Package evolution trend.

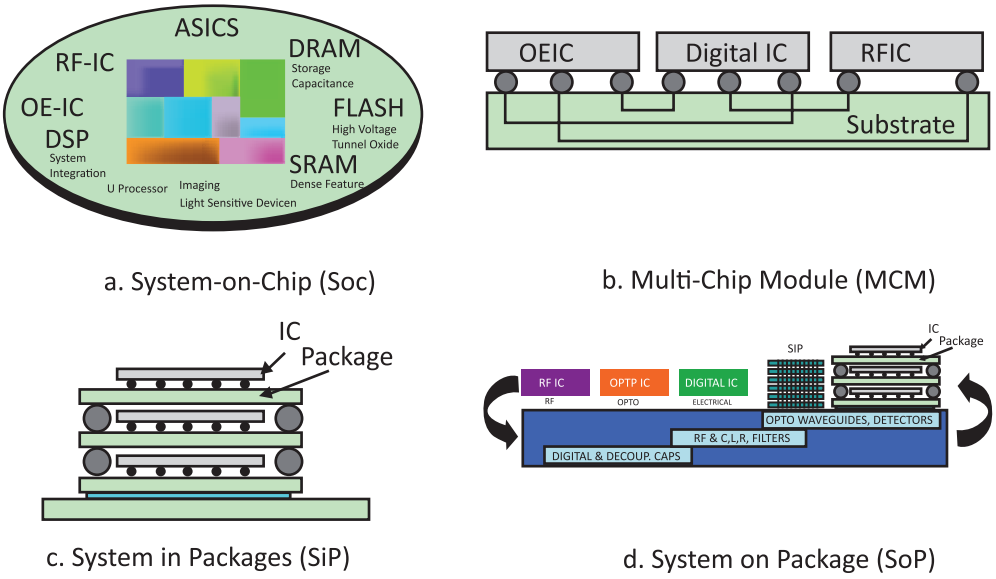


1.2.5 Packages

In many ways, the package can be considere it as the core of an interconnection channel within an electronic system since it provides the interface between the semiconductor devices and the PCB. Being more specific, a package has two basic functions; one is providing input/output interconnection to and from an IC, and to interconnect active and passive components inside a packaged system [10]. As shown in Fig. 1.12, the packages have evolved very fast, and it is expected that this evolution will continue in the coming years since these components play an important role in the 3D integration technologies, which is leading to the implementation of complete single-chip systems.

This technology trend is based on the heterogeneous integration that can be implemented within the packages. For instance, System-on-Chip (SoC) seeks to include all the components of a system inside of one chip, or Multi-Chip Module (MCM) which is an alternative to SoC. However, the two most important examples of similar and dissimilar components within a package are the System in Packages (SiP), limited to use in low power ICs (with simple design and minimal time to market), and System on Package (SoP) that overcomes the limitation in other integration schemes having global wiring as well as RF, digital, optical, active and passive components integrated inside. All these devices are part of the so called "convergent systems" [17], (see Fig. 1.13).

Figure 1.13
Convergent Systems.



1.3 Challenges in the Modeling of Interconnections

As mentioned in the previous section, the signal path is conformed by all the elements between the output of the transmitter and the input of the receiver. What this means is that packages, traces, bends, vias, connectors, etc. introduce parasitic effects that degrade signal transmission. At low frequency some effects in the signal path are negligible, but as the frequency increases, these effects become more important, and at the same time, the complexity in the design increases. Hence, the goal is to have a close idea of the corresponding physical behavior, as the signal is traveling through the interconnection channel. Thus, finding out the transmission problems in early stages of the design to avoid the costly re-design of structure is desirable.

There are different approaches or methods to model the components in the interconnection channel, such as the following:

1. Circuit oriented: Modeling the structures with equivalent-circuit networks, which are analyzed using SPICE-like simulators.
2. Analytical method: Solving Maxwell Equations for the dominant mode of transmission.
3. Full wave method: Solving Maxwell Equations for 3D structures.
4. Hybrid method: Combine 2D and 3D simulations with measurements.

In the case of simple channels, meaning just a transmission line without transitions, it is not complicated to determine the characteristics that predict its behavior at high frequency. There are several well developed methods to obtain the characteristic impedance Zc [30, 31] and the propagation constant γ of a transmission line [32], even more complicate channels involving transitions can be analyzed using methods that help to understand the behavior of the components at high frequency [33]. Usually, this type of approach relies on analytical methods, rich in mathematical processes and modeling the fields within the structures by means of lumped elements.

In some cases, it is enough to employ simulators such as ADS and H-Spice, with short simulation times and accurate results. Another advantage of these types of tools is the flexibility in partitioning the structure in sections, combining measurements and simulations at the same time. However, nowadays, the evolution to 3D integration offers much more freedom in the process design; but on the other

hand leads to more complex signal routing. Thus, in many cases it is necessary to use powerful tools such as full wave simulators to predict the electromagnetic behavior within the structure. It is true that these simulators are very accurate; however, there is always a tradeoff between accuracy and time of simulation. Among the full wave simulators available, the ones used in this work are CST Microwave Studio and High Frequency Structural Simulator (HFSS), both programs have good accuracy at high frequency, with the right boundary conditions and the proper specification of the material characteristics. Also bear in mind that all the effects present at high frequency, such as skin effect, roughness of the traces, and complex permittivity of the dielectric material, have to be considered in the models to keep the results accurate. In any case, the correlation between simulations and experiments is the best way to be sure of the results obtained.

1.4 Purpose of This Work.

The purpose of this work is to contribute to the study of signal integrity issues on PCB through the identification and analysis of high-order non-desired effects occurring in interconnects at high-frequency. This identification is carried out by means of a theoretical understanding of the physical phenomena occurring in the interconnects, and is supported in exhaustive and systematic simulations and measurements.

The contributions range from the study of non-ideal effects in simple interconnects, to the analysis of parasitic propagation in complex structures such as packages.

Chapter 2
Basics for the Modeling of Interconnection Channels

In this chapter, the description of the electrical performance of interconnection channels from simple homogeneous transmission lines to complex links such as those used in packages is presented. For this reason, several aspects regarding the basic concepts required to analyze transmission lines are revised throughout this chapter.

One of the first concepts to be discussed is the non-ideal behavior on an actual interconnect. Thus, ideally, an interconnection channel is lossless, with a great performance at each operation frequency, presents linear behavior, and satisfies the superposition principle. However, the interconnection channels used in high-speed devices are complex, present several electrical transitions, and employ non-ideal materials that present physical losses. So, this chapter also includes a short description of the losses associated with the dielectric and conductor materials. Furthermore, with the review of the scattering parameters presented afterwards it is pointed out the usefulness of these network parameters to identify the origin of the signal degradation in the transmission of high-speed signals through actual interconnects.

2.1 Material Losses

The transmission lines commonly used in PCB technology are microstrip and striplines, but in this section the losses associated with two-conductor interconnects are discussed considering a generic transmission line. In this case, the losses can be classified into two categories: conductor and dielectric losses. These adverse effects introduce frequency-dependent attenuation of the transmitted signal, which originates the reduction in the operation bandwidth of an interconnect. Thus, for a practical interconnect it is desirable to keep the material losses

as low as possible to approximate the corresponding behavior to that of an ideal transmission line at least within the operation range for a given application.

The conductor loss is related to the finite conductivity of the metal traces used to build an interconnect, whereas the losses that involve the dielectric are result of the complex nature of the permittivity. The description of these two mechanisms that are associated with the losses attributable to materials is depicted afterwards for giving an idea of the corresponding impact on the transmission of high-frequency signals through an interconnect.

2.1.1 Conductor Resistance and Inductance

In theory, an ideal conductor presents infine conductivity. However, an actual material presents a resistivity that may also be dependent on the frequency of the transmitted signals. In fact, the conductor losses can be broken down into two components: dc and ac losses [15]. The dc losses basically depend on the resistivity of the metal used in the fabrication process, the geometry of the trace and the distribution of the current flow in the cross section of the line. However, as the frequency of the transmitted signals increases, other phenomena that introduce a frequency-dependent resistance of the transmission line becomes apparent, the so-called skin effect, which is related to the ac losses.

The ac losses can be explained as follows. Under dc regime the current flows in the cross-sectional area of the trace. As the frequency increases, however, the current is confined near the surface of the conductor trace, reducing the effective area through which the charge carriers are flowing, yielding an increase of the transmission line resistance. Only the magnetic field inside the trace forces the current to flow only the periphery or “skin” of the traces. Moreover, this skin, which is in fact the distance from the surface of the conductor at which a considerable fraction of the total current is flowing, is frequency dependent. As the reader may infer, the skin effect is characterized by a resistive and inductive mechanism related to the variation of the electromagnetic fields applied to the traces. It means that any change in the distribution of the current flow within the cross section of the trace produces changes in the inductive and resistive properties of a transmission line. The parameter that allows to assess this effect is known as the skin depth and is defined as:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{\rho}{\pi f \mu}} \text{ [meters]} \tag{2.1}$$

where **ω** is the frequency in rad/s, **μ** is the permeability of the material and **σ** represents the conductivity of the material. So, one skin depth is the distance from the surface of the conductor to the attenuation of 63% in the electromagnetic waves within the conductor material [15]. Moreover, since the skin effect presents an onset frequency, ω_δ, it means that above and below the onset frequency, the current flows in different areas of the trace [29].

Regarding the total inductance ($\mathbf{L_T}$) of a trace, this is originated by the distribution of the magnetic field through the structure, which is in turn dependent on the current flow. So, at low frequencies the current is uniformly flowing within the trace, following the lower resistance path. In consequence, for a solid cylindrical conductor of radius *R* it is possible to imagine a hypothetical loop with radius *r*<*R* enclosing the current within the conductor, whose path is approximately followed by a magnetic field inside the conductor. Thus, the inductance associated with this magnetic field is called internal inductance $\mathbf{L_i}$. On the other hand, an additional loop with r>R can be imagined and the corresponding magnetic field taking place outside the conductor is associated with the external inductance $\mathbf{L_e}$. Notice that as the frequency increases the internal inductance is reduced since the current is confined near the surface of the conductor. Mathematically, the total inductance is equal to the algebraic sum of both inductances as in the equation (2.2).

$$L_T = L_e + L_i \tag{2.2}$$

Particularizing for a microstrip structure, the corresponding resistance can be determined from the resistance of the line by considering the geometry of the trace. Thus, when ignoring the resistance of the return path and assuming that the current flows inside of one skin depth, the resistance for a microstrip line is calculated using equation (2.3).

$$R_{\mu L} \approx \frac{\rho L}{Tranversal\ area} = \frac{\rho L}{\delta a} = \frac{L\sqrt{\rho\pi\mu f}}{a} \tag{2.3}$$

Where $R_{\mu L}$ is the total resistance of the microstrip line, ρ is the conductor resistivity, α is the line width, and finally L is the length of the microstrip line. As can be inferred, the current distribution changes as the frequency increases, yielding an increase in the resistance, in accordance to (2.3) with the square root of the frequency. In contrast, the total inductance drops down to the corresponding high-frequency value or external inductance, as depicted in Fig. 2.1.

When designing a practical transmission line it is necessary to take into account these important effects to assess the corresponding impact on the electrical performance of a communication link between electronic devices. In the following section, the losses associated with the dielectric are discussed to complement the idea of the "physical losses" associated with the materials forming a transmission line.

2.1.2 Dielectric Losses

Now, the losses in the dielectric material will be briefly reviewed. As the frequency increases, the loss associated with the finite conductivity and polarization effects of the dielectric material become important in contributing to the attenuation of high frequency signals travelling through a practical interconnect. The

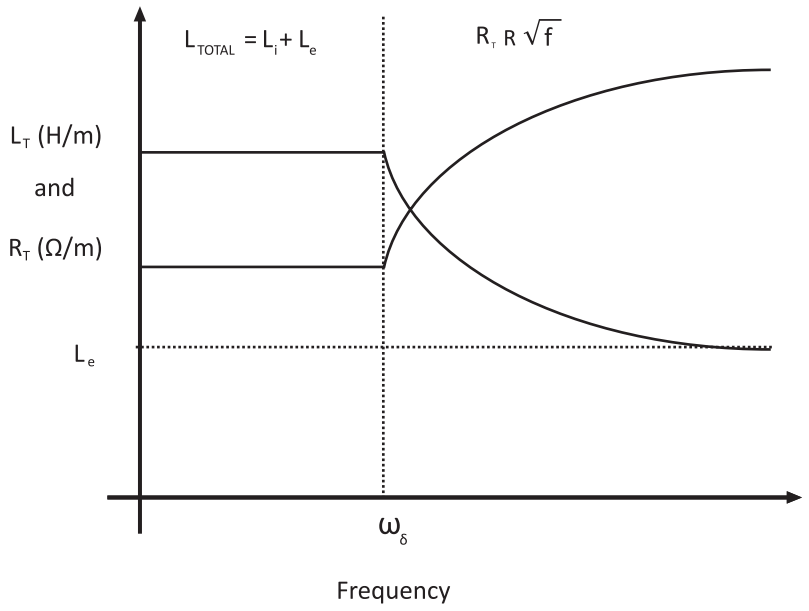


Figure 2.1 Qualitative trend of the total inductance and resistance of a PCB transmission line.

basic mechanism in the dielectric loss is the alignment with the electric field of the dipoles that represent the dipolar moment of the particles that compose the material [15]. Thus, when the dipoles oscillate with a time-varying field some energy is dissipated, originating a loss that impacts the integrity of the signal that is carried by the electromagnetic fields.

In general terms, the dielectric loss mechanism can be modeled by using Maxwell Equations. In this case, Ampere's law can be written in the frequency domain involving a complex permittivity $\hat{\varepsilon}$; see equation (2.4).

$$\nabla \times \boldsymbol{H} = \sigma \boldsymbol{E} + j\omega\varepsilon \boldsymbol{E} = j\omega \underbrace{\left(\varepsilon - j\frac{\sigma}{\omega}\right)}_{\text{Complex permittivity}} \boldsymbol{E} = j\omega\varepsilon_r \boldsymbol{E} \tag{2.4}$$

where the real part ε is the typical value of the permittivity when assuming lossless materials, whereas the imaginary part $\frac{\sigma}{\omega}$ represents the frequency dependent losses (notice that the conductivity σ is not constant with frequency). In fact, an important figure of merit for comparing different dielectrics can be defined using equation (2.4); this parameter is the loss tangent (tan δ), which is the ratio between the imaginary part and the real part of the complex permittivity. Thus, for a good insulator material tan δ presents dimensionless values much lower than 1. Typical nominal values for PCB substrates are below 0.02 within the gigahertz range. The mathematical definition of tan δ is shown in the following equation:

$$\tan\delta = \frac{\sigma}{\omega\varepsilon} \tag{2.5}$$

From this discussion, it is worthwhile to explicitly mention that the two most important figures of merit associated with the materials that allow the fabrication of a transmission line are the conductivity of the metal used to form the traces and the tan δ of the dielectric substrate. Bear in mind, however, that other parameters should also be taken into consideration such as the effective permittivity of the structure, which determines the speed of the electromagnetic fields along the transmission line.

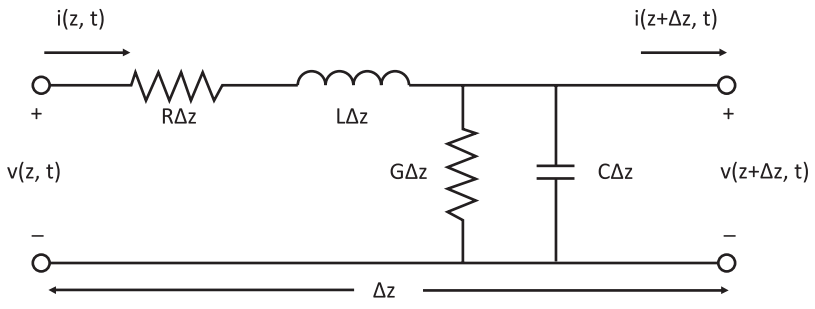
2.2 Transmission Line Modeling

Once that the losses have been discussed, one question arises: How are these losses considered when modeling an interconnect? The answer is: using Transmission Line Theory. As mentioned in the previous chapter, there are different approaches used to analyze transmission lines. In all of them it is necessary to understand the physics behind the models. One of the most widely used physically-based approaches is using the telegrapher equations, which are deduced from Maxwell Equations and allow representing the loss and delay effects using simple lumped components connected in a cascade configuration. The corresponding theory is presented afterwards.

2.2.1 Introduction to the Model of a Transmission Line

As is well known, the most important concepts of a transmission line are the characteristic impedance and, the propagation constant. These parameters allow to represent the propagation and coupling effects of any transmission line and can be obtained using Transmission Line Theory. In order to analyze the behavior of a segment of transmission line with length Δz using this theory, a model consisting of lumped elements is employed; this is depicted in Fig. 2.2. In this case, it is possible to apply the voltage and current Laws of Kirchhoff to deduce the equations that represent the behavior of a generic transmission line [34].

Figure 2.2
Lumped model
of a transmission line.



From the Kirchhoff Voltage Law the following equation is obtained:

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial \mathrm{t}} - v(z+\Delta z,t) = 0 \tag{2.6a}$$

whereas the Kirchhoff Current Law allows to obtain:

$$i(z,t) - G\Delta z v(z+\Delta z,t) - C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial \mathrm{t}} - i(z+\Delta z,t) = 0 \tag{2.6b}$$

After dividing (2.6a) and (2.6b) by Δz, taking the limit of $\Delta z \rightarrow 0$, and simplifying, the result are the telegrapher equations, given by:

$$\frac{dV(z)}{\mathrm{dz}} = -(R + j\omega L)I(z) \tag{2.7a}$$

$$\frac{dI(z)}{\mathrm{dz}} = -(G + j\omega C)V(z) \tag{2.7b}$$

Deriving again by z it is possible to obtain:

$$\frac{d^2V(z)}{\mathrm{d}z^2} - \gamma^2 \mathrm{V}(z) = 0 \tag{2.8a}$$

$$\frac{d^2I(z)}{\mathrm{d}z^2} - \gamma^2 I(z) = 0 \tag{2.8b}$$

where γ represents the ***complex propagation constant***, which is defined as:

$$\gamma = \sqrt{(R + j\omega L) + (G + j\omega C)} = \alpha + j\beta \tag{2.9}$$

As can be seen in (2.9), the complex propagation constant is a function of frequency and can be expressed as the sum of a real number and an imaginary number [20]. The real number α represents the attenuation that the electromagnetic wave suffers while travelling along the transmission line, and has units of nepers-per-meter. The imaginary number β represents the phase delay given in radians-per-meter. Notice that γ includes all the propagation effects associated with a homogeneous transmission line.

When assuming that the transmission line is fed by a signal applied at one of its extremes using a stimulus "source" while the other extreme is terminated with a complex impedance known as the "load", the telegrapher equations can be

written in a final form as:

(2.10a) $$\mathrm{V}(z) = V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}$$

(2.10b) $$I(z) = I_0^+ e^{-\gamma z} - I_0^- e^{\gamma z}$$

In (2.10a), $V_0^+ e^{-\gamma z}$ where are represents a voltage wave traveling in the +z direction (from the source to the load), whereas $V_0^- e^{\gamma z}$ represents a voltage wave traveling in the -z direction (from the load to the source). Similarly, (2.10b) includes terms representing current waves travelling along the transmission line in forward and backward directions.

In order to obtain an analytical expression to define the impedance of the line, the current of the line can be obtained by substituting (2.10a) in (2.7) and solving for *I(z)*, which yields:

(2.11) $$I(z) = \frac{\gamma}{R + j\omega L}\left[V_0^+ e^{-\gamma z} - V_0^- e^{\gamma z}\right] = \frac{1}{Z_0}\mathrm{V(z)}$$

Thus, the ***characteristic impedance*** is defined as:

(2.12) $$\mathrm{Z_0} = \frac{\mathrm{R} + \mathrm{j}\omega\mathrm{L}}{\gamma} = \frac{V_0^+}{I_0^+} = \frac{V_0^-}{I_0^-}$$

As previously mentioned, (2.9) and (2.12) describe the two most important parameters of a homogeneous section of transmission line, which can predict the behavior of the line at any frequency. For this reason, the accurate determination of these parameters play a primary role when characterizing and modeling composed channels that include homogeneous interconnects. Thus, reliable techniques to obtain these and other important parameters such as the complex permittivity and conductivity have to be used by signal integrity engineers, which are dedicated to optimize the links used to transmit signals within an electronic system. In this regard, one of the most important tools is that provided by the network-parameters, which allow to implementing models such as that described in this section. Afterwards, these parameters will be introduced in the context of this thesis.

2.2.2 Network Parameters

In practice, when measuring, characterizing, and modeling the high-frequency behavior of many electronic devices Linear-Network Theory is commonly used. In fact, assuming linear behavior of a particular device under certain conditions allows to use network-parameters to represent this device. In this regard, the most commonly used network-parameter sets are Z, Y, ABCD, H and T, which are defined in terms of voltages and currents. However, the measurement of voltage and current-based parameters at high frequencies presents several difficulties because of the required experimental conditions. For instance, for measuring Z-parameters, open-circuit conditions have to be guaranteed at the input and output ports of the network, which represents a challenge due to the capacitive behavior of a practical open-circuit. For this reason, instead of directly measuring voltage and current-based parameters at high frequencies, the scattering parameters or S-parameters are experimentally obtained, which allow to describe a device under test (DUT) in terms of the incident and reflected power waves seen at each port.

The S-parameters are easy to obtain using a Vector Network Analyzer (VNA); furthermore, the S-parameters are simple to work with at high frequencies and in many cases provide intuitive information of the behavior of a device. For instance, this parameter set can be directly used to compare the losses associated with different transmission lines as will be shown later. Another advantage of the S-parameters is the possibility of determining the electrical parameters (R, L, G, C, γ and Zc) associated with the model of a line straightforwardly from a mathematical analysis of measurements. In Fig. 2.3 the illustration of the conceptual definition of the two-port S-parameters corresponding to a microwave junction is shown.

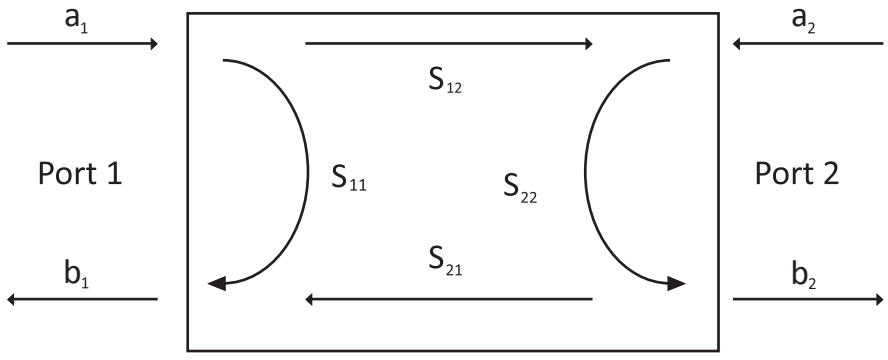


Figure 2.3
Two-port junction and corresponding S-parameters [34].

21

Mathematically, the S-parameters are defined through a set of lineal equations that describe the relation between power waves reflected and transmitted when a power wave is applied to a device that is represented by means of a network. These parameters can be expressed using matrix notation containing four variables, two variables associated to the stimulus and two with the response of the network; this is:

(2.13)
$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} * \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$
$$b = S*a$$

where:

a_i	power wave applied to the network at port *i*
b_i	power wave reflected back at port *j*
$S_{11} = \frac{b_1}{a_1}\Big\|_{a_2=0}$	power reflected at port 1 (for a transmission line →**RETURN LOSS at port 1**)
$S_{12} = \frac{b_1}{a_2}\Big\|_{a_1=0}$	power transmitted from port 2 to port 1 (for a transmission line → **INSERTION LOSS**)
$S_{21} = \frac{b_2}{a_1}\Big\|_{a_2=0}$	power transmitted from port 1 to port 2 (for a transmission line → **INSERTION LOSS**)
$S_{22} = \frac{b_2}{a_2}\Big\|_{a_1=0}$	power reflected at port 2 (for a transmission line → **RETURN LOSS at port 2**)

The common parameters to identify the losses of a transmission line (and more generally speaking of any interconnection channel) are S_{11} (return loss) and S_{21} (insertion loss). Where S_{11} represents the power reflected at the port 1 due to impedance mismatches, discontinuities, and transitions; whereas S_{21} represents the loss introduced by physical and structural imperfections of the channel. Once that the S-parameters of a transmission line have been determined, several figures-of-merit can be obtained; among these are: gain, reflection coefficient, propagation delay, and attenuation. Furthermore, there are easy ways to identify the validity of S-parameter measurements performed to passive channels such as any interconnect. This type of DUTs must satisfy the following conditions [15]:

Symmetric Condition	In symmetric systems like homogeneous PCB traces	$S_{11} = S_{22}$ and $S_{12} = S_{21}$	(2.14)
Passivity Condition	In systems with losses	$\|S_{11}\|^2 + \|S_{12}\|^2 = 1 - \|power\ losses\|^2$	(2.15)

Notice that verifying that the conditions mentioned in the previous equations are satisfied allows to determine additional information about a certain interconnect. For instance, the power losses included in (2.15) may be associated to radiation, parasitic mode propagation, resonances, etc. For this reason, these parameters are widely used in many of the analyses presented throughout this thesis.

An important point to be remarked here is the fact that the S-parameter set can be converted to any other network parameter set with the same dimension (e.g. 2x2 for a 2-port network). This allows the simplification of many calculations, for instance when determining equivalent circuits for a specific device.

Finally, since this thesis is focused in interconnects, the steps to carry out the design of the experiment for carrying out the determination of the S-parameters associated with a transmission-line-based channel are listed below [35]:

1) Building interconnect prototypes for microwave testing.
2) Characterizing and subtracting measurement errors of the system (calibration).
3) Extracting the transmission line impedance and propagation constant.
4) Additional processes for the subtraction of pad parasitic effects and other possible transitions.

The measurement process and other aspects related to the experimental determination of the S-parameters are detailed hereafter.

2.2.3 Experimental Set-Up for Performing High-Frequency Measurements

In the next paragraphs, an overview of the process to measure transmission lines and composed interconnects at high frequencies is presented. Within this context, the techniques used to remove the systematic errors caused by the measurement instrument are also mentioned and briefly discussed.

As mentioned in the previous section, a VNA is the instrument used to obtain the experimental S-parameters of a DUT. Fig. 2.4 depicts a typical setup of this measuring equipment. As can be seen, cables, connectors, and other electrical transitions are used to interconnect the equipment with the DUT. Thus, to obtain accurate and realistic S-parameters of any DUT when using a VNA, it is necessary to eliminate the systematic errors that can introduce uncertainties to the measurement. This type of systematic errors is related to the port mismatches and other parasitic effects occurring in the electrical path from the VNA to the DUT. So, independently of the technique used to measure the S-parameters (e.g. with coaxial connectors or with micro-probes), the corresponding errors have to be taken into consideration. Fortunately, these errors can be removed using a calibration procedure, which is explained in the following lines.

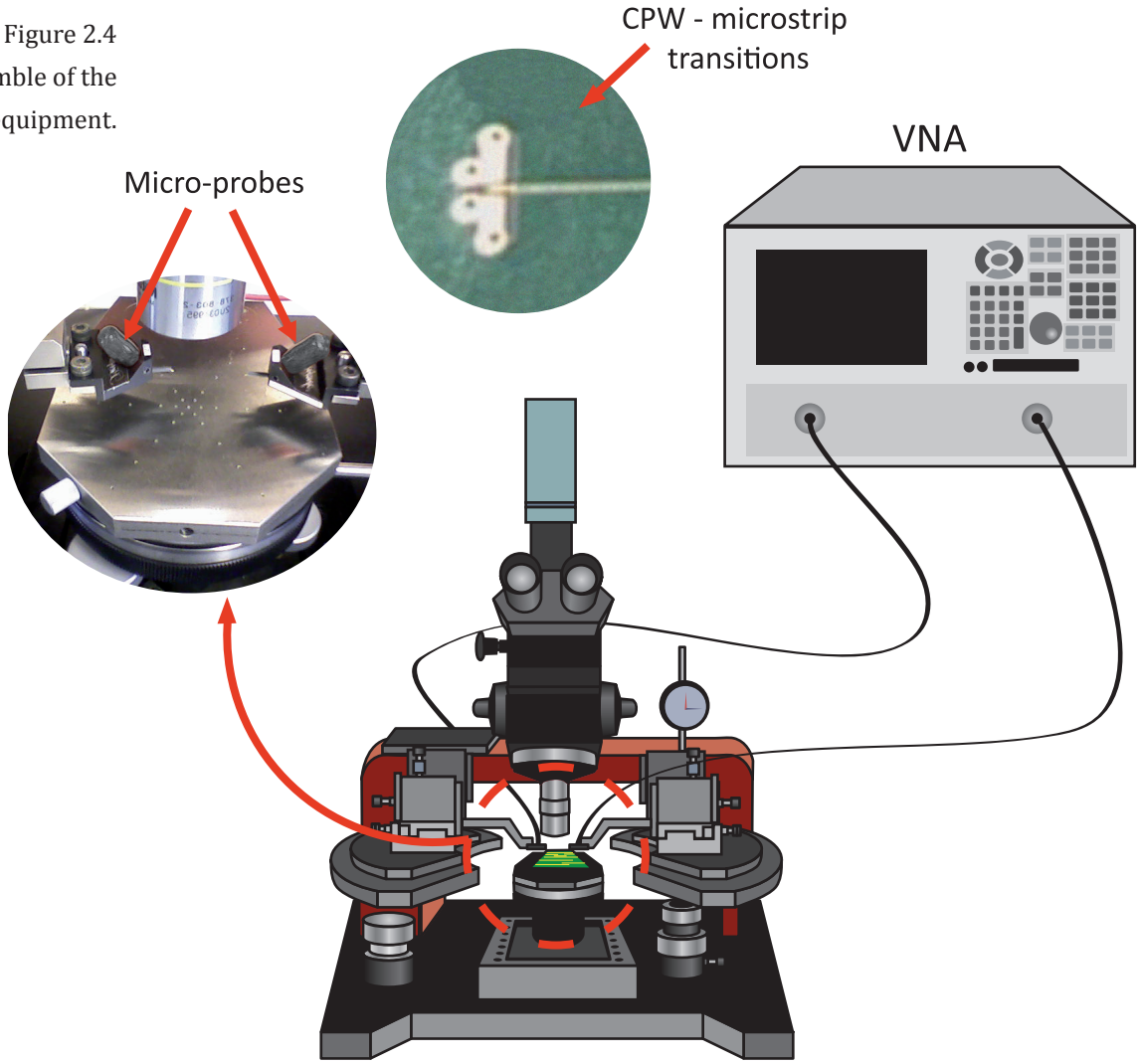


Figure 2.4
Assemble of the measuring equipment.

The calibration technique is the characterization and elimination of systematic errors through the measurement of several standard structures with well known electrical characteristics. Among the typical standards are: SHORT, OPEN, LOAD, LINE and THRU (see Fig. 2.5). The short and the open elements are used for reflection measurements, while the thru and the load elements are used for transmission and coupled measurements respectively. Depending on the type of calibration is the set of structures that is necessary to measure. Also, the mathematical processing of the collected data considerably varies from procedure to procedure. The most popular calibration technique is the so-called Short-Open-Load-Thru (SOLT) [27], which uses SHORT, OPEN, THRU and LOAD standards. Although up to relatively low microwave frequencies this technique is reliable, it presents some constraints above 20 GHz since it relies on the fact that the standards can be represented by means of equivalent circuits with lumped elements. Unfortunately, this assumption lacks of validity as the frequency increases and more complicated topologies would be required to represent the standards. Another disadvantage of SOLT is the fact that using previously measured standards introduces errors due to variations of the corresponding electrical parameters from those specified by the manufacturer. For this reason, alternative calibration techniques have been proposed such as the Line-Reflect-Match (LRM) and the Thru-Reflect-Line (TRL) techniques [36-40], in which the used standards are LINE, REFLECT, MATCH and THRU. So, the TRL technique, which is based on transmission line standards, and not requiring precise knowledge of these, represents a powerful tool in the calibration process.

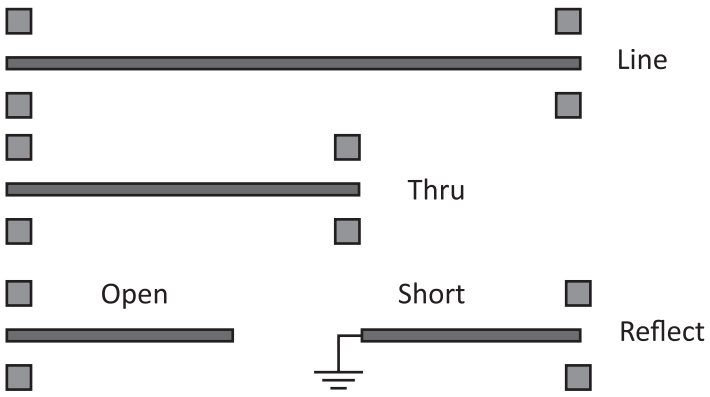


Figure 2.5
Sketch showing some typical calibration standards.

In the case of measurements carried out with micro-probes (see Fig.2.4), the calibration technique removes the systematic errors presented in the measurements from the VNA to the tips of the probes (see Fig. 2.6). Nonetheless, as long as the appropriate standards are available, the calibration techniques can be applied to any RF structure like coaxial, coplanar waveguide (CPW) and microstrip, etc. Bear in mind, however, that the conventional calibration techniques as the ones mentioned in this section assume single mode propagation [27], and additional processing and calibration standards may be needed when multi-mode propagation is occurring, such as in the case of waveguides or structures presenting parasitic propagation modes. This topic will be discussed later for transmission lines presenting inappropriate or non-optimized transitions. At the moment it is worthwhile to mention that additional correction procedures have to be applied when measuring a this type of device. Since the measurement of the DUT is not carried out in a direct way but additional test fixtures have to be fabricated to access the device using for instance probes, the measurement plane has to be shifted to the desired measuring point by means of a de-embedding procedure. This is mentioned in a following section.

A final remark in this regard is that even when using the best calibration standards and procedures available, there still are unwanted effects in the collected measurement of the DUT that are not easily removable. For instance, the errors associated with the environment variations (e.g. temperature, humidity, etc.) or the human errors (e.g. landing of the probes). Thus, special guidelines have to be followed when measuring at high frequencies to minimize these errors to obtain meaningful measurements.

2.3 Homogeneous Transmission Lines and Complex Interconnects

In this section, an overview of the behavior of simple and composed channels based on transmission lines is presented. Speaking in general terms, an interconnection channel may fall into two categories: homogeneous lines (microstrip and striplines) without neither electrical transitions nor changes in impedance, and composed interconnection channels including vertical transitions, such as vias and packages. Thus, in order to model either simple or composed channels it is necessary to know their corresponding features well. This allows to carry out an adequate structure optimization to keep the losses at minimum. As mentioned

before, a handy tool to perform the required analysis and acquiring information about the structures are the S-parameters. For this reason, the S-parameters associated with different interconnection channels are shown in this section.

The following paragraphs begin with the description of homogenous lines (used as a simple channel); then, the technique to obtain the characteristic impedance and propagation constant is described, and finally the composed channel is described with the aid of experimental data associated with links including packages.

2.3.1 Homogeneous Lines: Basic Theory

A homogenous section of transmission line is the simplest case of an interconnect. However, even for this case, there exist insertion and reflection losses that degrade the quality of the signal. As it was mentioned before, the insertion loss is originated by the physical and structural losses that occur along the channel, whereas the return loss is originated by the reflections occurring at the electrical transitions within the channel, and also because of the changes in the distribution of the electromagnetic fields. Thus, when working with homogeneous lines, the physical losses (i.e. dielectric and metal losses) will contribute to an increase in the insertion loss, whereas the impedance mismatches at the terminations of the transmission line will contribute to the return loss. Fig. 2.6 shows a homogeneous line (microstrip line) with coplanar-waveguide (CPW) transitions, which are implemented as test fixtures to access the line using coplanar micro-probes.

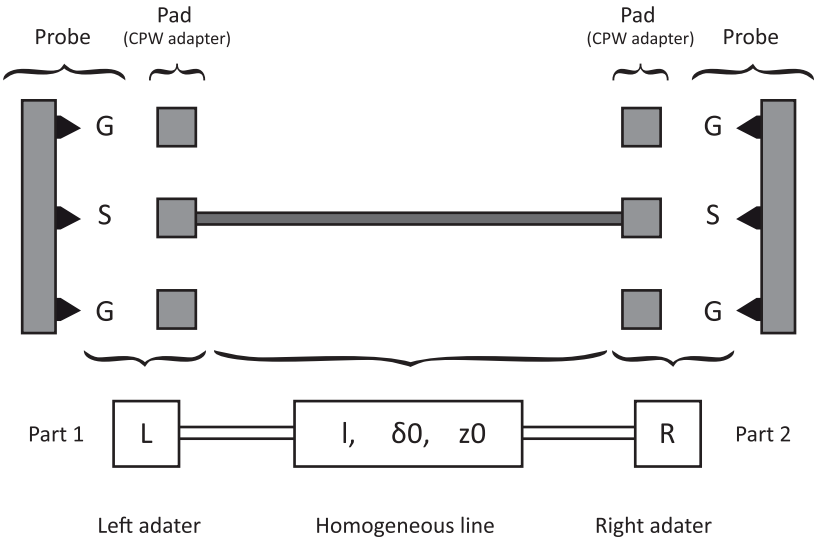


Figure 2.6 Homogeneous line embedded between two CPW adapters.

In this case, the homogeneous line can be modeled as a non-reflecting line embedded between two symmetrical and reciprocal transitions [32].

When characterizing homogeneous lines, the impact of the transitions used to perform the corresponding measurements have to be removed. For instance, in the case of the CPW-microstrip-CPW structure shown in Fig. 2.6, the CPW-to-microstrip transitions introduce unwanted effects, which will be removed by the mathematical process according to a given calibration procedure. Thus, the calibration process removes the systematic errors from the measurement, shifting the reference plane to the tips of the probes (see Fig. 2.6). However, in order to determine the experimental data associated with the transmission line itself, the effects from the test fixtures have to be removed by an additional process called deembedding. This process defines new reference planes closer to the DUT, removing the effects of the test fixtures in the measurements. There are many reported techniques to perform the deembedding of the test fixtures[41-43], and in the frequency domain the vast majority of the techniques make use of wave cascade matrices (WCM) to represent every section of the structure, which are obtained from either measured or computed S-parameters.

The advantage of employing WCM matrices is the fact that the associated parameters can be "cascaded", like the ABCD parameters. The WCM parameters are obtained from the S-parameters using the transformation defined in equation (2.16).

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \frac{1}{S_{21}} \begin{pmatrix} -\Delta & S_{11} \\ -S_{22} & 1 \end{pmatrix} * \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \tag{2.16}$$

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = R * \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}$$

In order to obtain the matrices associated with the homogeneous section of transmission line in Fig. 2.6, two deembedding structures are used: THRU and LINE, which are described in terms of MCW parameters. These structures are defined in the following way:

(2.17)	$THRU = R_A * R_B$	Connecting the test fixtures directly.
(2.18)	$LINE = R_A * R_L * R_B$	A coupled line of a specific length inserted between the test fixture.
(2.19)	$R_L = \begin{pmatrix} e^{-\gamma L_i} & 0 \\ 0 & e^{\gamma L_i} \end{pmatrix}$	

where T_A and T_B represent the left and right transitions between which the homogeneous line (represented by T_L) is embedded. Also, L_i represents the length of the transmission line.

Thus, with the aid of an additional REFLECT structure, the matrices T_A and T_B can be determined by solving a simple eigenvalue problem. However, remember that any homogeneous line can be completely characterized once that the propagation constant and the characteristic impedance are known[44-48]. Thus, the first step is determining γ and there are many reported ways to obtain this parameter using the definitions shown in equations (2.17)-(2.19) [36]. Among these procedures, the multiline method is the simplest and most accurate reported to date. In this case, the S-parameters from two lines with the same impedance but different length (L_1 and L_2) are required; these lines can be the THRU and an additional line. So, the WCM parameters of these two lines, can be expressed as:

$$\begin{aligned} M_{L_1} &= T_A T_{L_1} T_B \\ M_{L_2} &= T_A T_{L_2} T_B \end{aligned} \tag{2.20}$$

Through a series of matrix products, substitutions, and matrix properties, a linear system of equations can be solved to obtain the value of λ (eigevalue), from which the propagation constant can be calculated using the length of the used lines; mathematically:

$$\lambda = e^{\gamma(L_2 - L_1)} \tag{2.21}$$

$$\gamma = \frac{1}{L_2 - L_1} \ln(\lambda) \tag{2.22}$$

Once that the propagation constant is known, the impedance of the line can be determined using simple Transmission Line Theory and assuming that the dielectric substrate presents relatively low losses. This approach relies on the fact that the distributed resistance, inductance, conductance, and capacitance per unit length associated with the equivalent circuit model of a transmission line can be related to the product and quotient of γ and Z_c as:

$$\gamma Z_C = R + j\omega L \tag{2.23}$$

$$\frac{\gamma}{Z_C} = G + j\omega C \tag{2.24}$$

Thus, assuming that the lines are fabricated on a lossless substrate (i.e. G=0), the complex Z_c can be obtained after solving (2.25); this is:

$$Z_C = \frac{\beta}{\omega C} + j\frac{\alpha}{\omega C} \tag{2.25}$$

In this equation, γ has already been determined from measurements performed to two lines of different lengths and C can be estimated either from a curve fitting at low frequencies or calculating the capacitance of the lines using geometrical dimensions.

Another possible way to obtain the characteristic impedance of a homogeneous line is through the transformation of the S-parameters of the homogeneous line (after removing the effect of the pads) to the corresponding ABCD matrix. In this case, it is possible to obtain Z_C as shown in equations (2.26) and (2.27).

$$\mathrm{ABCD} = \begin{pmatrix} \cosh(\gamma L_i) & Z_c \mathrm{senh}(\gamma L_i) \\ \frac{1}{Z_c}\mathrm{senh}(\gamma L_i) & \cosh(\gamma L_i) \end{pmatrix} \tag{2.26}$$

$$Z_c = \sqrt{\frac{B}{C}} \tag{2.27}$$

2.3.2 Homogeneous Lines: Experimental Data

In order to visualize the trend of the curves associated with the parameters of typical transmission lines fabricated on PCB technology, experimental S-parameters corresponding to several lines were processed and the results are shown in this section.

The lines under study in this section were fabricated with silver over Rogers RT/Duroid 5880 substrate material (nominal relative permittivity of 2.2 and loss tangent of 0.0009). The width of the lines is 350 μm and the thickness of the dielectric is about 127 μm (5 mil). A photograph of the test board that includes these lines is shown in Fig. 2.7. The lengths of the lines are 0.5, 1, 2 and 4 in, and notice that CPW-to-microstrip transitions were added to allow the measurement using ground-signal-ground (GSG) configured micro-probes. The S-parameters of these lines were measured at the High-Frequency Intel Lab in Guadalajara using a previously calibrated VNA with extended frequency range up to 110 GHz. Fig. 2.8 shows part of the set-up used to measure these structures.

Firstly, the calibration procedure was selected by comparing the measurements performed after calibrating the VNA with SOLT and LRM procedures. As can be seen in Fig. 2.9, for the line with a length of 4 in the difference in the mea-

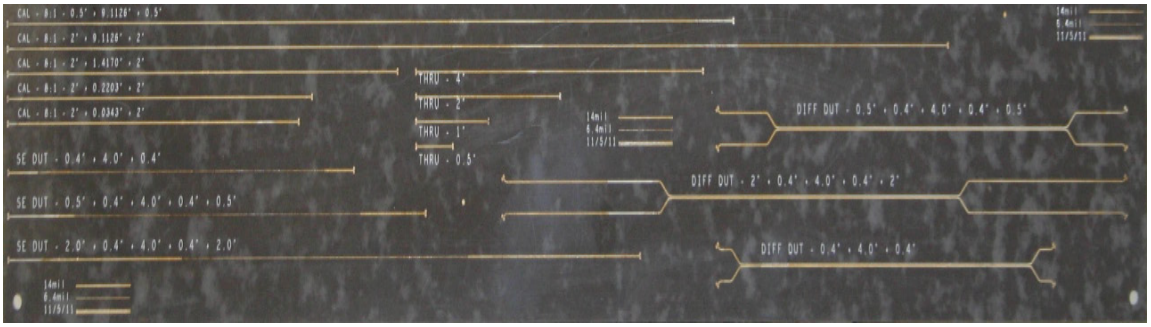


Figure 2.7
PCB board including the lines studied in this section.

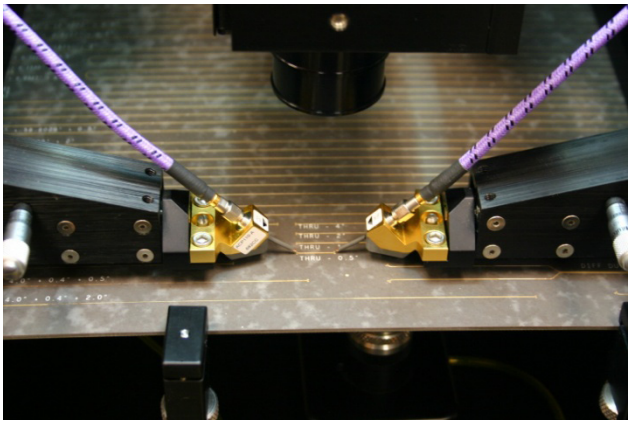
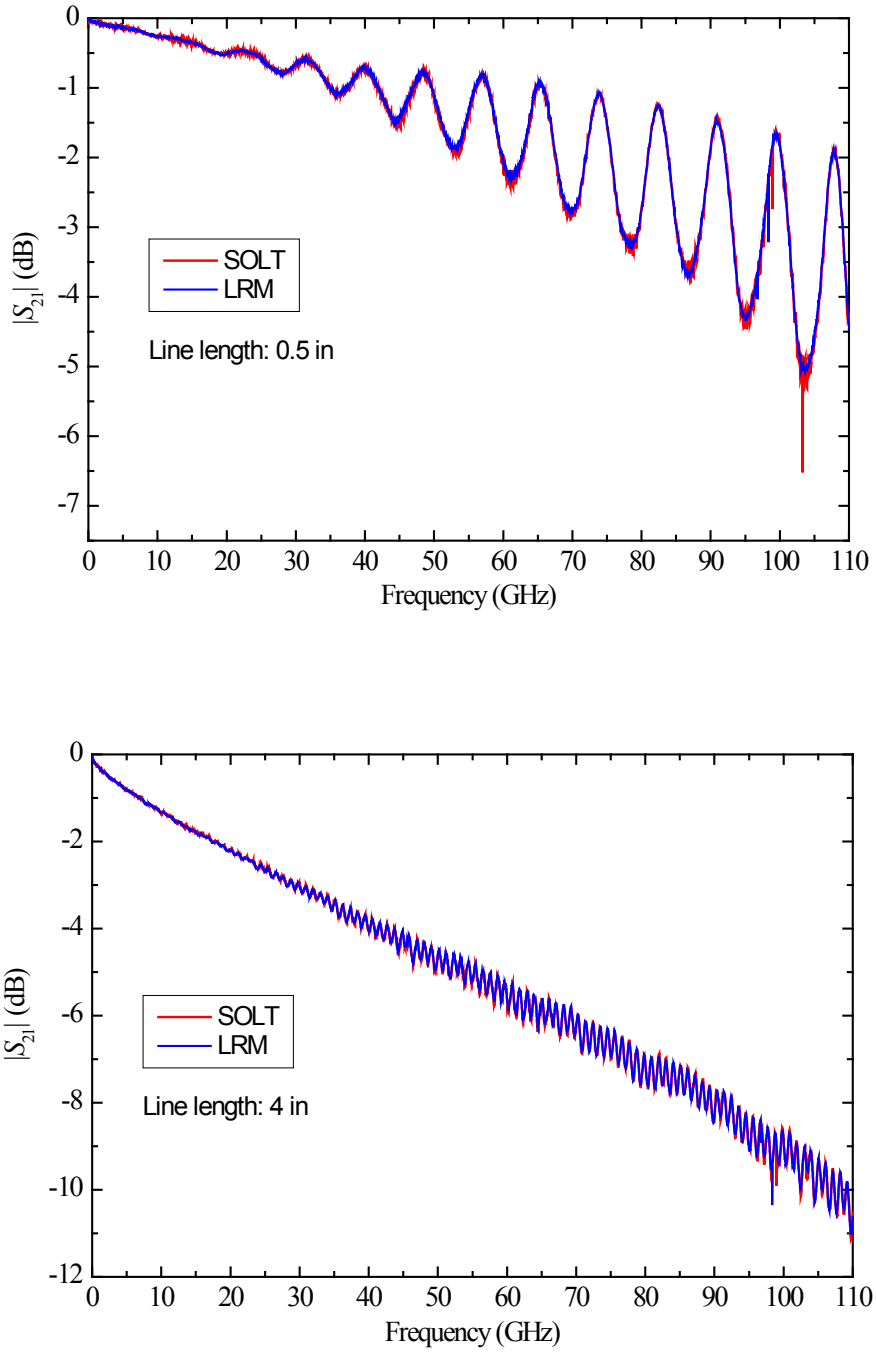


Figure 2.8
Set-up used to measure the homogeneous transmission lines.

sured $|S_{21}|$ parameter is not considerable when applying both procedures. However, for the shortest measured line (length of 0.5 in) $|S_{21}|$ becomes noisy as the frequency increases. This is due to the fact that SOLT assumes that the calibration standards are perfectly represented by lumped equivalent circuits, whereas LRM only assumes that the standards present reflective behavior (or perfectly coupled as in the case of the MATCH standard). The error becomes more important as the DUT becomes smaller and the imperfections of the equipment are comparable to this device. Thus, from the simple inspection of measurements shown in Fig. 2.9, the LRM calibration was selected for performing the rest of the measurements.

Figure 2.9. Measured insertion loss for two lines showing the difference in the experimental data when applying SOLT and LRM calibrations.



Once that the S-parameter measurements have been performed, the experimental propagation constant and characteristic impedance of the lines were obtained using the approaches explained in the previous section. The corresponding results are shown in the figures 2.10 and 2.11.

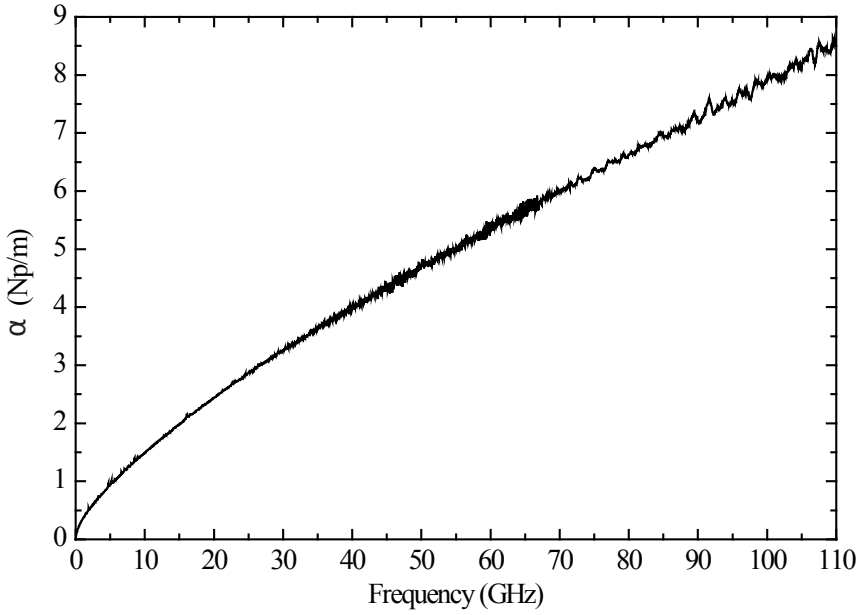


Figure 2.10
Experimental
propagation constant.

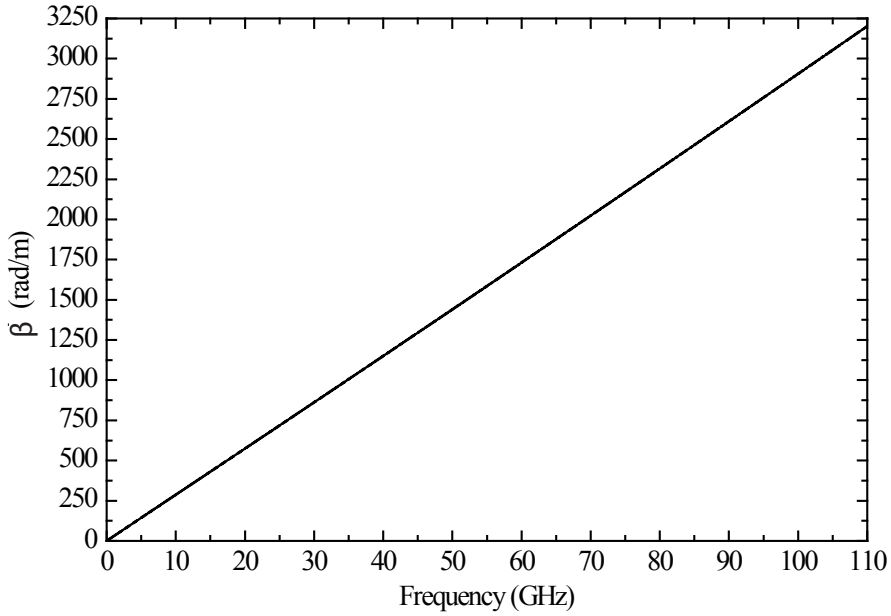
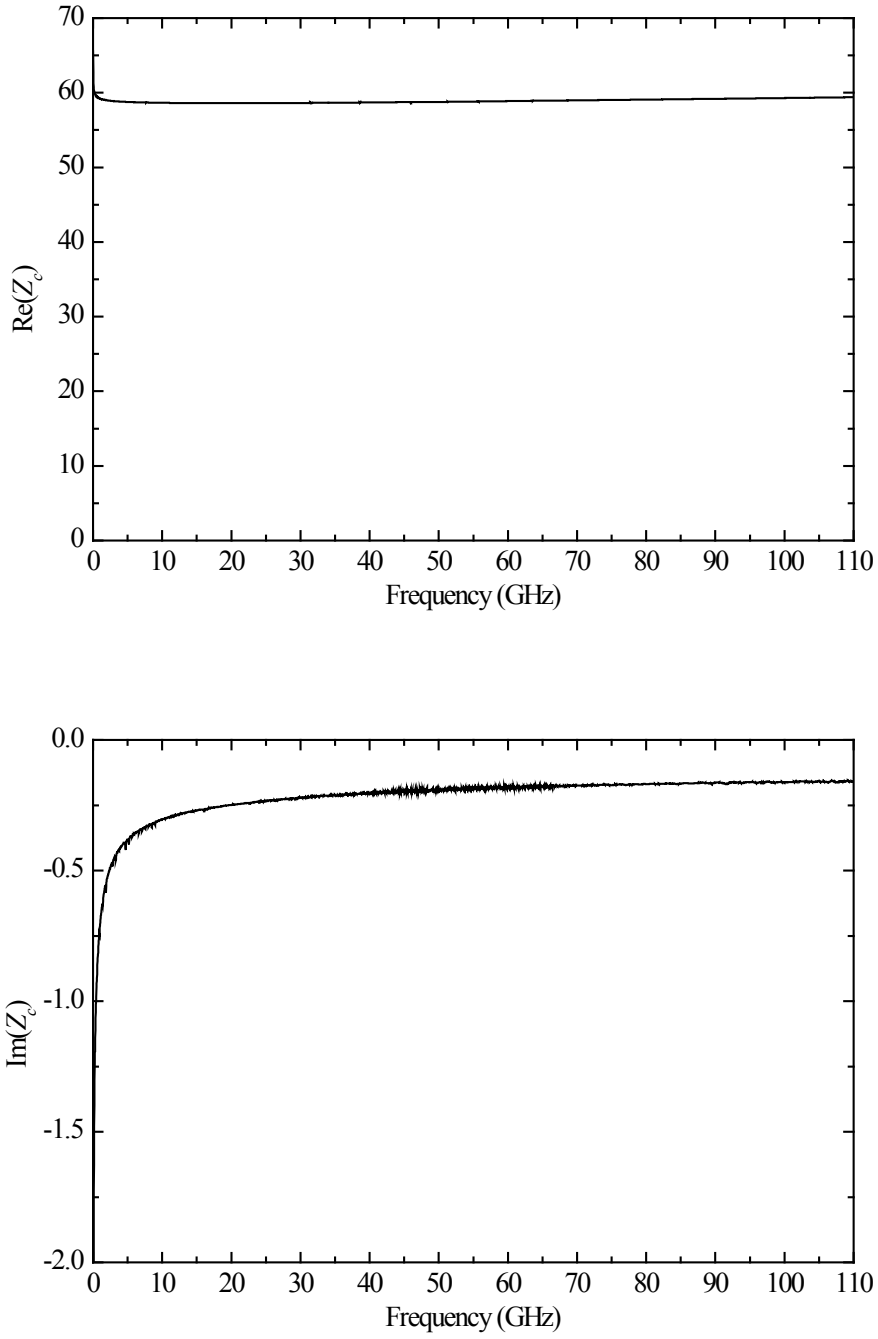


Figure 2.11 Experimental characteristic impedance.



Now, with the propagation constant and the characteristic impedance already determined, it is possible to obtain the S-parameters of a homogeneous line by constructing an ABCD-parameter model based on (2.26) and performing the cor-

responding ABCD-to-S transformation. In this case, a comparison of the data corresponding to lines with and without the effect of the pads can be carried out. This is shown in the figures 2.12 and 2.13 for lines with lengths of 4 and 0.5 in respectively.

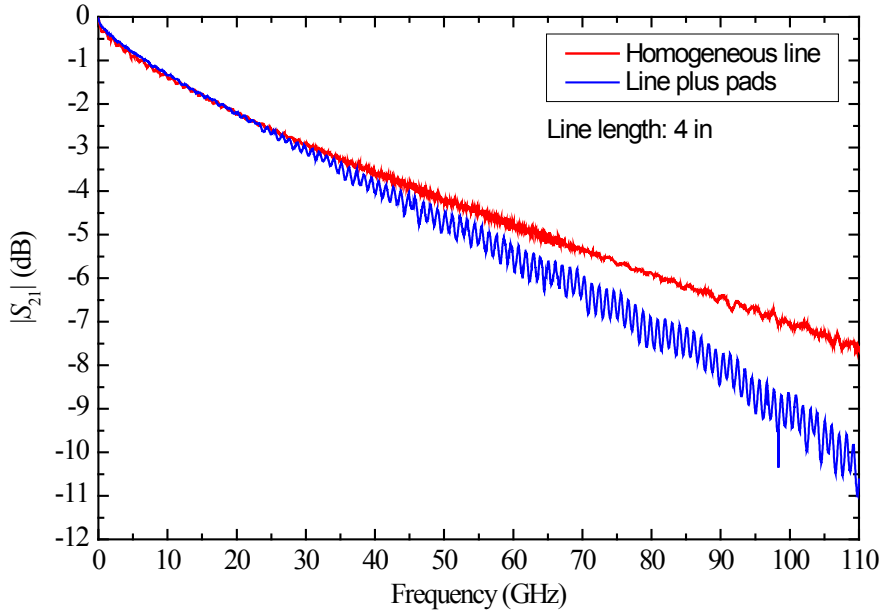


Figure 2.12
Magnitude and phase corresponding to a line with length of 4 in, before and after removing the effect of the pad parasitics.

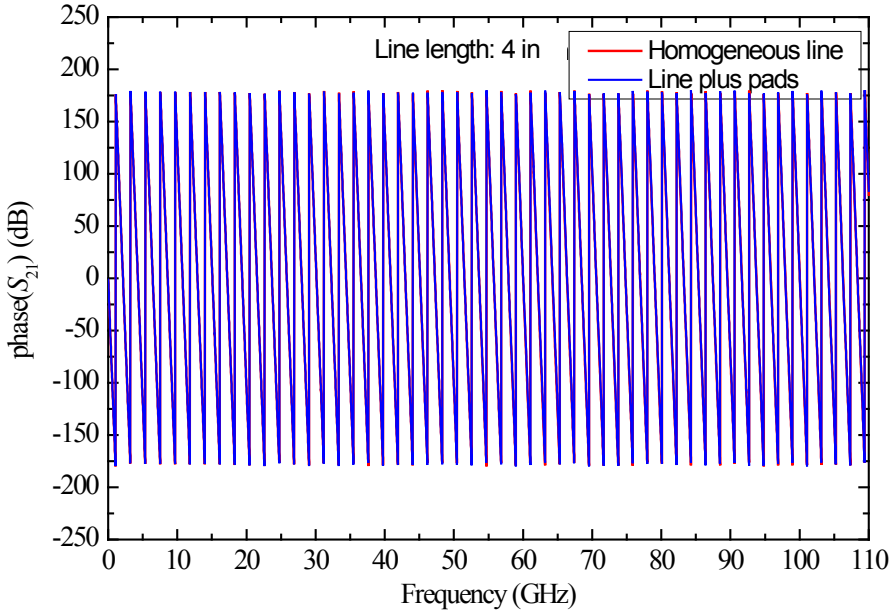
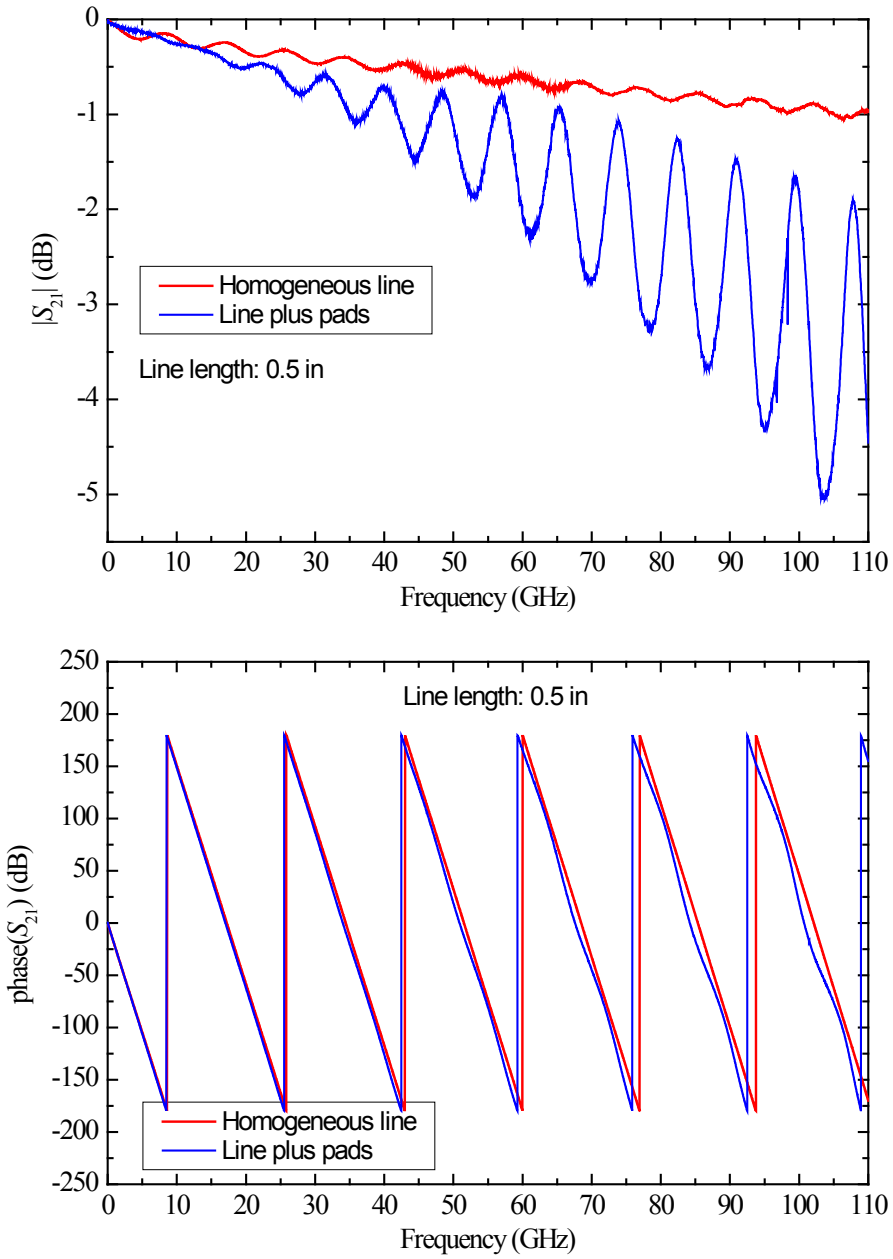


Figure 2.13 Magnitude and phase corresponding to a line with length of 0.5 in, before and after removing the effect of the pad parasitics.



As can be noticed in figures 2.12 and 2.13, the effect of the pads considerably affects the transmission of the line, which is more accentuated in the shortest line. Even though the CPW-microstrip transition is optimized to reduce the corresponding effect in the measurements, certain imperfections reflected in the measurements are introduced. Then, it is expected that more complicated transitions such as that presented in packages will have a higher impact on the overall performance on a practical channel.

2.3.3 Composed Channel

Up until now, the structures that have been analyzed were simple transmission lines, without transitions. However, the technology evolution has resulted in developing more sophisticated ways to electrically join devices together. Then, many types of interconnection structures have been designed inside smaller spaces and in different layers. In this regard, when simple traces are not enough for proper interconnecting devices, composed channels are used in structures like packages or multilayer PCBs, joining together different elements through layers of PCB or even inside the packages that contain the integrated circuits. This is one of the main topics to be discussed throughout this thesis. However, as a first introduction to the topic, one of the most popular interconnection channels used in current electronics technology is briefly revised here.

Chip-to-chip interconnections using packages is an example of a composed channel[49-50], where the signal path is formed by micro-vias, vias, transmission lines, and other transitions that are placed in different layers. This is shown in Fig. 2.14. In this case, the description of the transmission path is as follows: the signal first encounters a coplanar transition on the top of the package, then finds the second part which is a series of vertical transitions that include the core or the principal vertical transition, finally the signal reaches the a homogeneous microstrip line. So, such as in the case of simple transitions, this type of composed transitions can be represented by WCM matrices as suggested in equation (2.24).

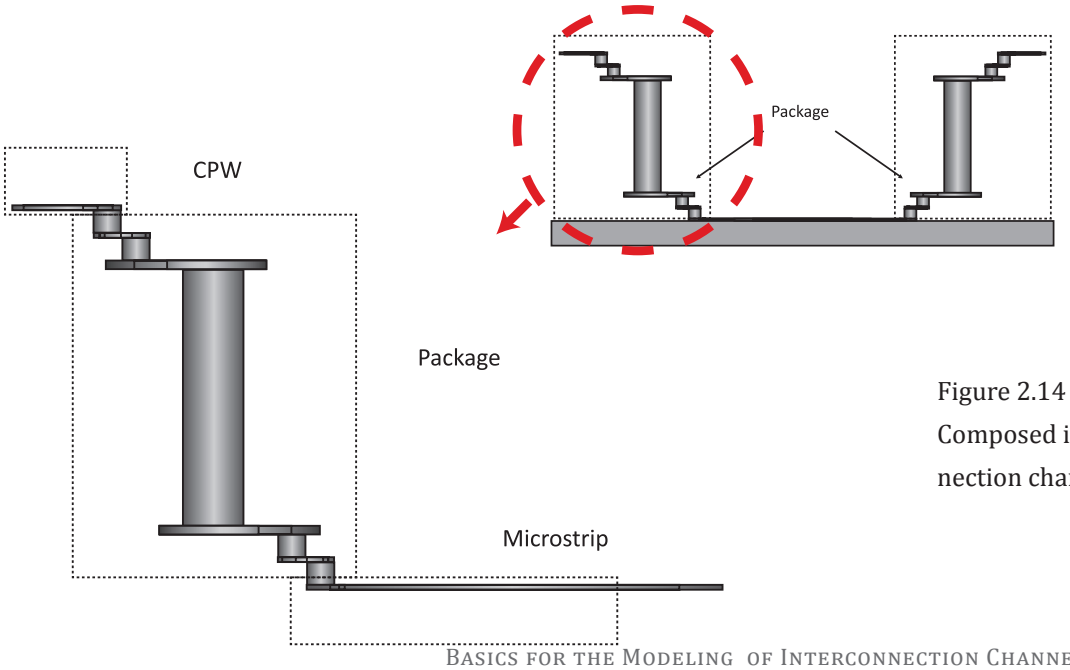


Figure 2.14
Composed interconnection channel.

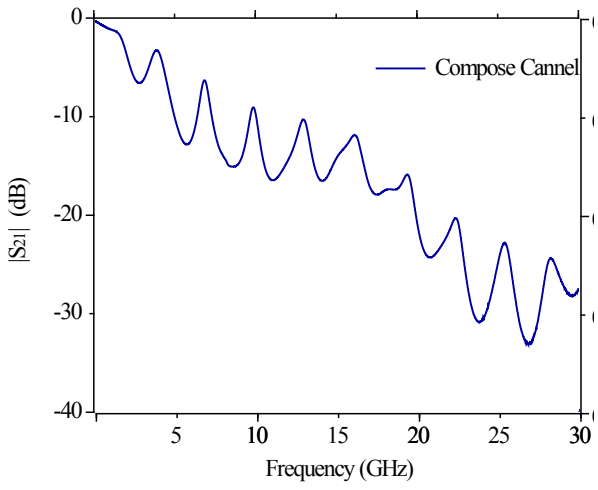
(2.24)

$$M_{Composed\_channel} = T_{left\_package} * T_{homogenous\_line} * T_{right\_package}$$

In this case, the determination and separation of the multiple matrices representing a composed channel is not an easy task and several data processing techniques have to be followed even relying on the feasibility of using full-wave simulations as will be shown in Chapter 4. Moreover, it is obvious that the transmission is not ideal and presents considerable return and insertion losses as a result of the complexity of the channel. In fact, notice in Fig. 2.15a that the insertion loss presents an irregular trend due to the fact that this data corresponds to a channel that includes vias.

In some cases, the S-parameters do not provide much information; however, with tools like Advanced Design System (ADS) the time-impedance profile can be obtained to have an idea from TDR (time domain reflectometry) of the discontinuities occurring along the channel; data of this type are shown in Fig. 22b. To obtain the TDR data, a direct conversion of the measured S-parameters into time domain data was performed using a fast Fourier transform algorithm. In this case, the time-impedance profile provides information about the parasitic effects in the transition as depicted in Fig. 22b. The first valley in the curve represents a capacitive effect, then a change in impedance from 50 to about 57 ohms occurs, afterwards a very large capacitive effect takes place and the final part of the curve shows a line with impedance close to 50 ohms. Observe that, even though this curve provides qualitative information about a channel, it represents a valuable tool when developing equivalent circuit models for a practical interconnection channel.

Figure 22.a
Insertion loss of a compose channel.



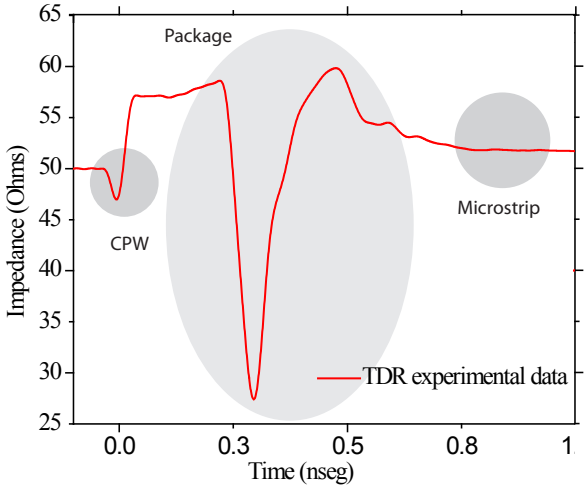


Figure 22.b
Time-impedance profile of the composed channel.

2.4 Conclusions

This chapter introduces the basis of the theory that will be used during the analysis carried out throughout this thesis. The main physical losses occurring in interconnects were presented and discussed. These included the skin effect and the dielectric losses at high-frequencies, which are responsible for the attenuation of the signals. The model used for representing transmission lines by applying the telegrapher equations was also revised and the way the losses are taken into consideration within this model was also discussed. With this theory, it is possible to accurately represent any homogeneous transmission line and developing more complicated models from either experimental or simulated S-parameter data, which is included in the contents of the following chapters.

Chapter 3
Signal Propagation on Interconnects: High-Order Effects

An analysis of the high-order effects that occur in typical chip-to-chip links used in PCB technology is presented in this chapter. These effects include those related to the discontinuities introduced by the electrical transitions between different transmission lines (e.g. CPWs, microstrip, striplines, etc.), in vertical and horizontal transitions (e.g. signal and ground vias, packages, changes in width, etc.), and in test-fixtures (e.g. CPW adapters, coaxial connectors, etc.). In practical interconnection channels these discontinuities are common and, when not properly designed, may yield high return losses, resonances, parasitic mode propagation within the channel, undesirable coupling between signal paths (and even between signal paths and power/ground planes). For this reason, identifying these effects in chip-to-chip channels is required when carrying out the design and optimization of these structures for high-speed applications.

One of the main unwanted effects that will be exposed within this chapter is the parasitic mode of propagation originated by the excitation of waveguide modes by vertical transitions. As will be shown here, this provides a clear idea of the effects that may occur in complex transitions such as packages. Another effect that will be studied is that related to the resonance that is originated in simple transmission lines when the CPW-to-microstrip transitions used for probing are not properly designed. A discussion about the origin of these resonances is also presented based on the obtained experimental propagation constant of the traces.

3.1 Propagation of Parasitic Modes on Interconnects

When a transmission line is measured in the laboratory (as depicted in Fig. 2.4), different types of transitions can be used. These include, coaxial-to-microstrip/stripline, coaxial-to-rectangular waveguide, CPW-to-microstrip/stripline, and many others. The most commonly used to test single-ended interconnection channels (i.e. those with the input and output referenced to the same ground terminal) are the

CPW adapters and the coaxial connectors for probing using coplanar micro-probes and coaxial cables respectively [49-50]. These adapters are depicted in Fig. 3.1.

Thus, for instance, when the adapter shown in Fig. 3.1a is used to probe a microstrip line, the coplanar micro-probes inject a signal that is propagated through the pads (ignoring the effect of the ground vias) in a grounded CPW (GCPW) mode, as depicted in Fig. 3.2a. Thus, at the CPW-to-microstrip transition an electrical discontinuity occurs, which in accordance with basic Transmission Line Theory will originate that part of the energy is injected into the microstrip line in the corresponding propagation mode (shown in Fig. 3.2b), whereas part of the energy will be reflected back in the GCPW mode mentioned before [51]. This is the ideal case. However, other modes can be excited at the transitions originating an energy "leakage" that is neither reflected back nor recovered at the end of the microstrip. For instance, in this example, a quasi-parallel-plate waveguide mode can

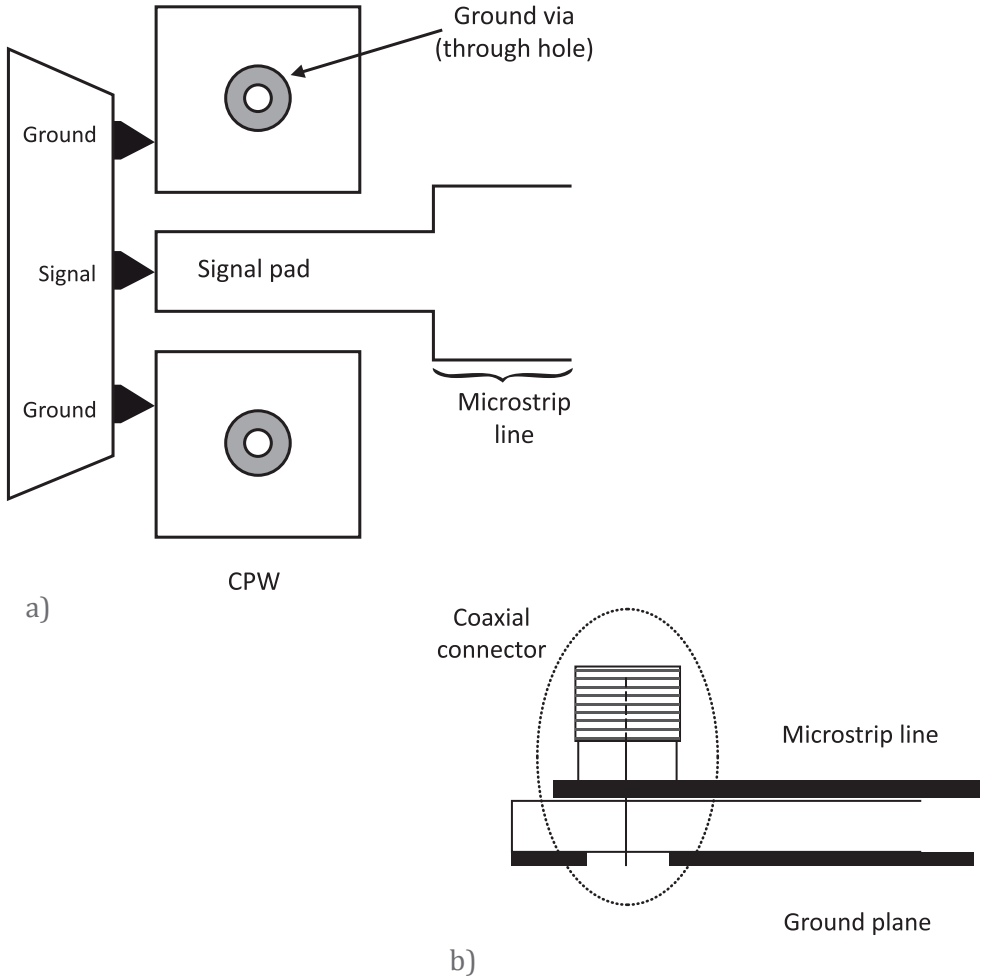


Figure 3.1 Adapters typically used to test single-ended interconnection channels: a) CPW adapter (top view), and b) coaxial connector (side view).

also be excited when the signal is travelling from the CPW to the microstrip (see Fig. 3.2c). In consequence, the energy that is "injected" into the microstrip will be divided into two components: i) the desired microstrip mode, and ii) the parasitic parallel-plate mode. That latter is not recovered at the end of the interconnection and represents an energy loss due to parasitic mode excitation.

In general, any electrical transition may introduce the undesirable effects associated with parasitic mode propagation that influence in a negative way the integrity of the transmitted signal, and these effects are common in practical interconnects within a PCB or in packages [3]. Fortunately, in simple structures like test fixtures used for probing transmission lines it is relatively easy to identify these adverse effects introduced by the transitions, whereas specific prototypes have to be fabricated to identify the signal degradation associated with this type of effects in more complex structures. Some of the most common parasitic modes occurring in PCB and package interconnects are listed below and discussed in the following subsections:

- slotline mode,
- surface wave mode, and
- parallel plate mode.

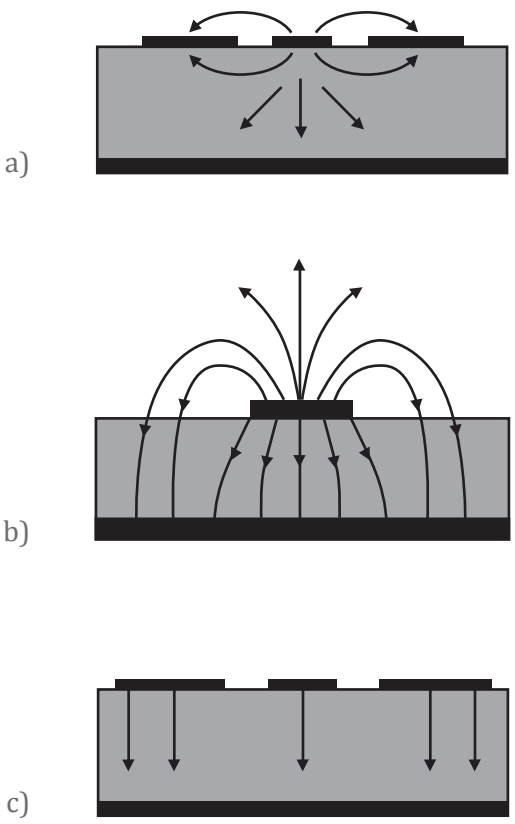


Figure 3.2
Mode occurring in a CPW-to-microstrip transition: a) GCPN mode, b) microstrip mode, and c) parasitc mode. The arrows represent electric field lines.

Since these effects are not considered in the transmission of an ideal isolated transmission line, enhanced models are required to represent the corresponding behavior. Moreover, for not being considered in conventional representations of transmission-line-based interconnection channels, these effects are classified within a category referred to as "second order effects" or "high order effects". In fact, nowadays, second order effects are frequently found in interconnects as a result of the high frequency of operation, the continuous dimension reduction and the increase in the density of the devices. That is why the analysis of the transmission channels is an important research topic studied to improve the performance of electronic systems. For this reason, some of the most important second order effects will be revised in this chapter through an analysis of experimental data.

Notice that previously neglected phenomena associated with signal propagation through an interconnect are now taking importance. In fact, many of these non-idealities in the signal path are closely involved with the presence of second order effects during high-speed data transmission. However, some improvements can be carried out in an interconnection channel to reduce the undesirable effects related with parasitic mode propagation. Among the imperfections in the channel that can be corrected are the impedances mismatches, gaps on the return path, bad terminations, bends, transitions between layers (e.g. ground vias) and edges in the structures, just to mention some of the most representative.

As mentioned before, the main constraint introduced by second-order effects is the loss of energy in the desired path resulting in a low quality of the signal transmission, and in a reduction of the corresponding bandwidth. Fig. 3.3 shows how an interconnection channel can be represented using a 3-port network when parasitic mode propagation is occurring [51-52]. Ideally, the network presents only two ports; however, a third port represents the energy that is "leaking away" due to parasitic mode propagation.

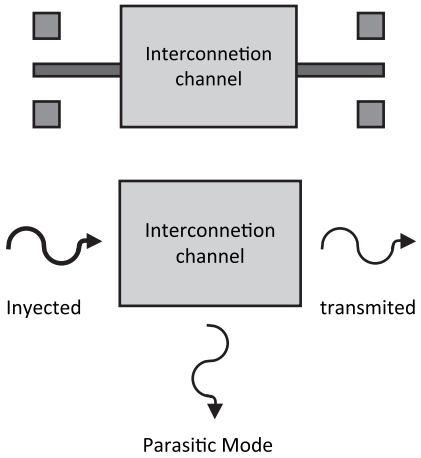


Figure 3.3
Simple representation of an interconnection channel where parasitic mode propagation is occurring [51].

3.1.1 Slotline Mode

In current PCB designs it is a common practice to divide the return and power planes in a digital and an analog section to avoid interference between the corresponding devices [27]. However, the horizontal spacing between conductive planes introduces undesirable effects such as the excitation of slotline propagation modes that typically affect the microstrip lines that cross above a gap in the return or power planes as illustrated in Fig. 3.4. As it was mentioned in the previous section, the signal should follow a path from the source to the load and, if reflections occur, part of the signal travels back to the source. When slotline mode occurs, however, the gap modifies the signal path and the electromagnetic energy leaks away perpendicularly to the desired direction of propagation (along the gap). This effect can be partially represented assuming that the slotline mode introduces an inductance in the device interconnect. In a rigorous analysis, the slotline modes can be described using the displacement current flowing onto the second ground plane [53, 54].

In order to avoid crossing of gaps on power/ground planes, isolation transformers, optical isolators, or metalized bridges can be used. However, a combination of solutions can be required to improve the performance of the system by diminishing the impact of these gaps. Thus, full-wave simulations are commonly carried out to perform the corresponding optimization of the structure.

To model this effect using lumped elements, the problem is thought from a physically-based point of view. Thus, when the signal reaches a discontinuity like

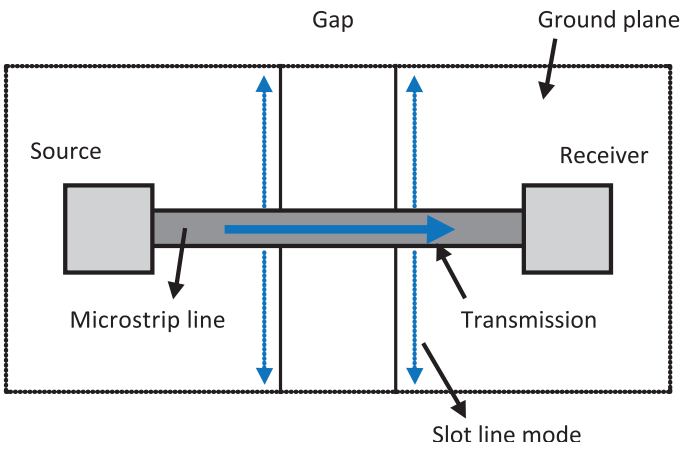


Figure 3.4
Sketch illustrating the signal propagation associated with a microstrip passing above a gap in the ground plane. Slotline propagation mode is occurring.

a gap in the power/ground plane, part of the energy will be converted into a propagation mode for which the trace is not designed to transmit. In consequence, a model like the one shown in Fig. 3.5 can be developed. In this model, the impedance of the transmission line encounters the gap that originates a parasitic slotline mode that has another impedance associated, which represents the electrical discontinuity between the sections of the interconnect. With the aid of this model, the power loss, reflection, radiation and resonance effects that degrade the transmitted signal can be acceptably modeled when the corresponding impedances are appropriately determined. Coupling between traces (crosstalk) or coupling with other unwanted propagation modes associated with different structures can also be modeled but using more complete representations.

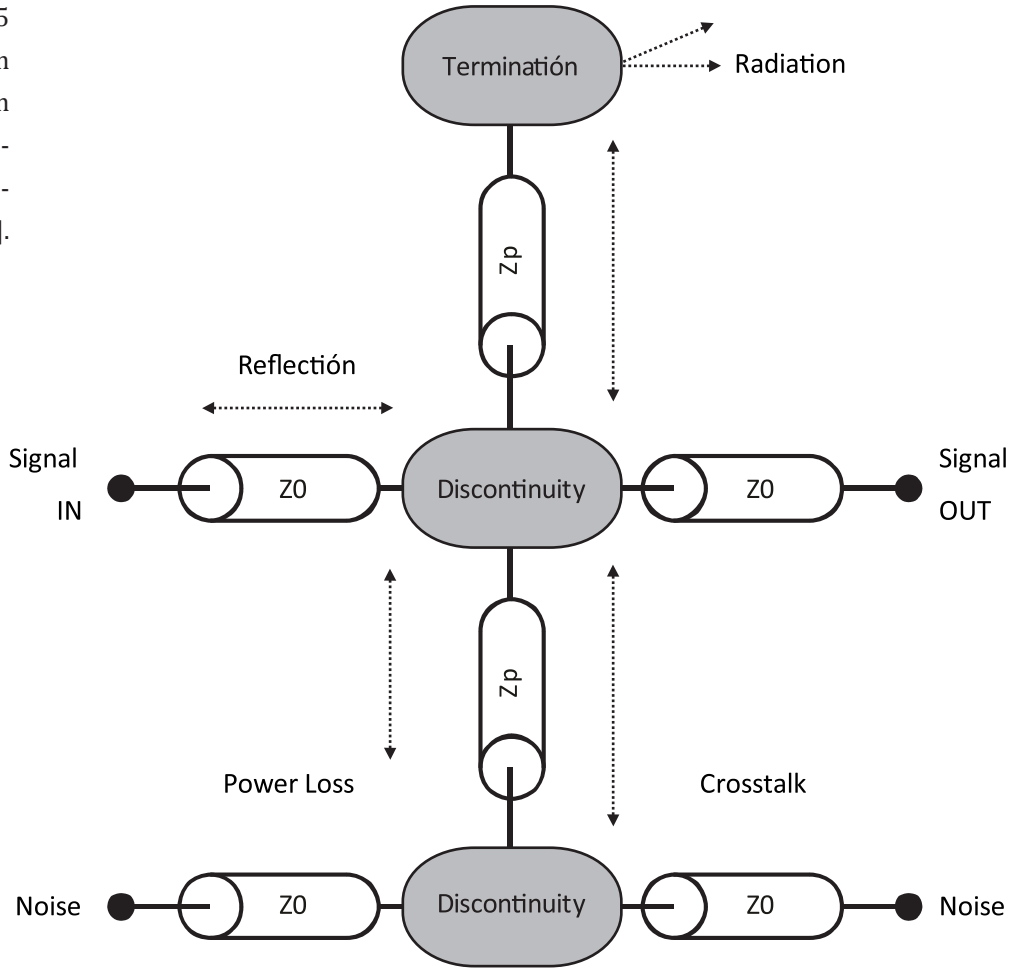


Figure 3.5
Simple representation of an interconnection channel where parasitic mode propagation is occurring [3].

3.1.2 Surface Wave Mode

Structures fabricated in multi-layer PCBs in which several dielectric planes with power/ground planes at different levels present truncation or discontinuities that are sensitive to the excitation of electromagnetic waves which are not supposed to be propagated. Among the parasitic modes of this type are the trapped modes (non-radiating waves), slow-wave modes (low phase velocity) and the surface-wave (SW) modes (which present exponential attenuation) that are usually present on microstrip lines embedded between different layers of dielectric and metal within a PCB [3]. One reason to analyze the SW modes is because the corresponding cutoff frequency is zero, which implies that its effect is present at all frequencies.

This SW mode is excited in the direction of the longitudinal axis of the stub and bend discontinuities [55]; thus, modes like this may have a narrow bandwidth. At the edge of a structure like a stub or a bend some of the signal propagated is radiated and some is reflected back to the source. In this case, when the truncation is made to the edge of the dielectric or metal planes, the reflected signal is guided by the substrate, which produces unwanted effects like crosstalk, radiation or resonances traduced in low quality transmitted signals. In addition, the SW modes make the signal to behave as a plane wave at low frequencies, and the dominant loss is radiation. In this case, the trapped signal does not represent a considerable loss. However, as the frequency increases, the part of the signal that is configured in this mode is trapped near the surface. Hence, a change in the reflection coefficient occurs when the SW-mode changes its behavior from "quasi-plane-wave" to "trapped". Fig. 3.6 depicts this mode of propagation. To control this type of mode propagation the use of thin dielectrics and materials with low permittivity is recommended.

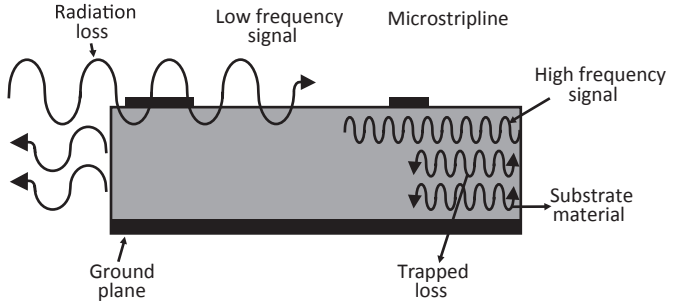


Figure 3.6
Illustration of the surface wave mode propagation.

3.1.3 Parallel Plate Mode

Current multilayer structures are built in low-loss substrates to reduce the dielectric losses [56]. However, low-loss dielectric and the parallel metal planes used as ground-planes in interconnects are the ideal environment to develop second order effects. One of these is the propagation of the parasitic parallel plate mode, which is very common in packages[57-58]. In this case, a via guiding the signal from one level to another may behave like an antenna exciting a parallel-plate mode between the ground layers within a package. This is illustrated in Fig. 3.7. For this reason, the analysis of this type of propagation has been necessary to improve the performance of interconnects where multiple vias and metal layers are used.

In general, the parallel plate mode (PPM) is excited when the signal vertically crosses parallel planes disposed horizontally[3]. This discontinuity considerably reduces the performance of vertical transitions since much of the energy leaks away from the desired propagation path as shown in Fig. 3.7. Thus, the PPM mode of excitation is accompanied by a considerable power loss. Notice in Fig. 3.7 that the propagation of the PPM is radial with a decreasing amplitude as the distance from the exciting element increases. This radial nature of the parasitic interconnect (i.e. the parallel-plate waveguide formed by the planes) makes the corresponding impedance change with position, which requires to perform a formal analysis of the effect using radial transmission line concepts [52, 59].

As can be noticed, placing vias in structures like a package usually excites PPM, which clearly means that the vias are very good emitters of this type of propagation modes. In consequence, inadequate designs including vias may cause that the propagation of these second order effects originate ground bounces or simultaneous switching noise within the structure. For this reason, the fluctuation of

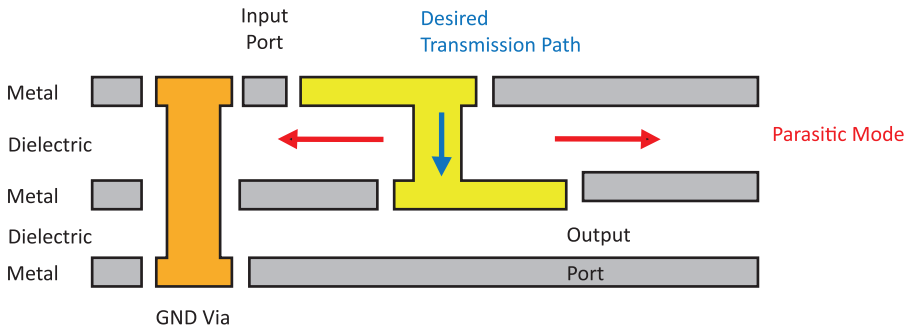


Figure 3.7. Sketch of the side view of a package that conceptually illustrates the origin of the PPM excitation.

voltage between the planes produced by the PPM, plus the fact that the parallel planes form a resonator with a high Q, make it possible for the presence of resonances, which is the worst effect originated by the propagation of PPM.

Another important factor that influences the propagation of PPM within the PCB are the edges of the board [52]. This is because sooner or later the propagation reaches the edges of the board where part of the energy will be radiated to the free space and part will be reflected. In this regard, there are three basic cases of edge structures:

- finite size planes: the signal "sees" the edges of the package and originates resonances,
- infinite metal planes: PPM becomes evanescent and no resonance occurs, and
- electric wall (short circuit): the signal is confined and no resonance occurs.

As the reader may infer, the geometry of the structure plays an important role in defining the conditions at which PPM will occur and there are different techniques to keep the propagation of PPM under control, among these are[29, 60]:

- placing bypass capacitors near to the vias, trying to keep the capacitive coupling between all the references planes, and maintain the high frequency traces in the same plane;
- reducing the dielectric thickness so that the parasitic modes occur at frequencies so high that fall outside the range of operation;
- using an adequate configuration of ground vias that confines the energy using the concept of electric-walls.

These effects will be studied in detail inthe next chapter, and at the moment only preliminary concepts have been mentioned.

3.2 Experimental Analysis of Parasitic Mode Propagation on Microstrips

As mentioned in the previous section, many types of parasitic modes may occur within an interconnect. This section is dedicated to identifying and characterizing the parasitic modes propagation occurring in simple microstrip terminated with CPW adapters. Other parasitic propagation modes taking place in more complicated structures will be discussed in Chapter 4.

In order to understand the impact of the unwanted propagation modes in a simple transmission line test structure, several microstrip lines with different lengths and a width of 0.18 mm (7.2 mil) and terminated with CPW adapters, such as that depicted in Fig. 3.8, were measured up to 110 GHz using an LRM-calibrated VNA. The lines were formed with copper over a dielectric substrate

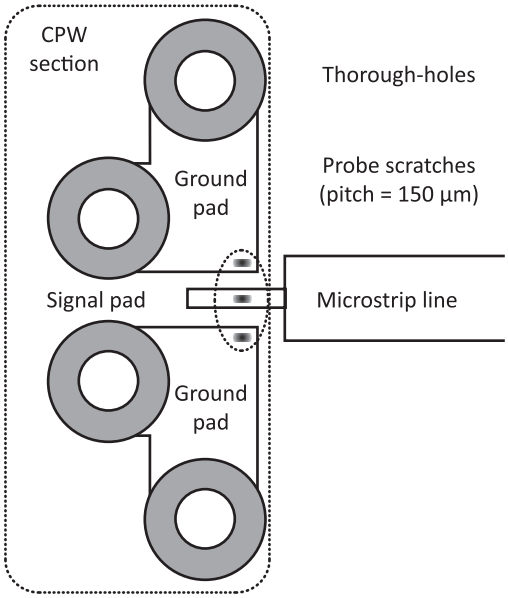


Figure 3.8
CPW-to-microstrip transition used to measure the transmission lines studied in this section.

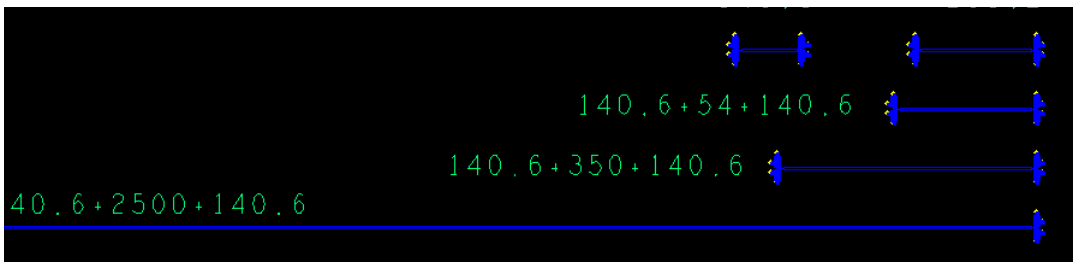


Figure 3.9
Partial view of the layout of the prototype board where the measured lines were included.

made of Rogers RT/Duriod 5880 material with a thickness of 0.79 mm (31mil). This material presents a nominal relative permittivity and loss tangent of 2.2 and 0.0017 respectively. Fig. 3.9 presents a partial view of the layout of the prototype board where the measured lines were included.

Fig. 3.10 shows the measured return and insertion lcmcmcmcmosses for three microstrip lines including the impact of the CPW-to-microstrip transitions. As can be seen in this figure, below approximately 50 GHz the $|S_{11}|$ and $|S_{21}|$ curves follow the expected trend of a homogeneous line with impedance discontinuities at the

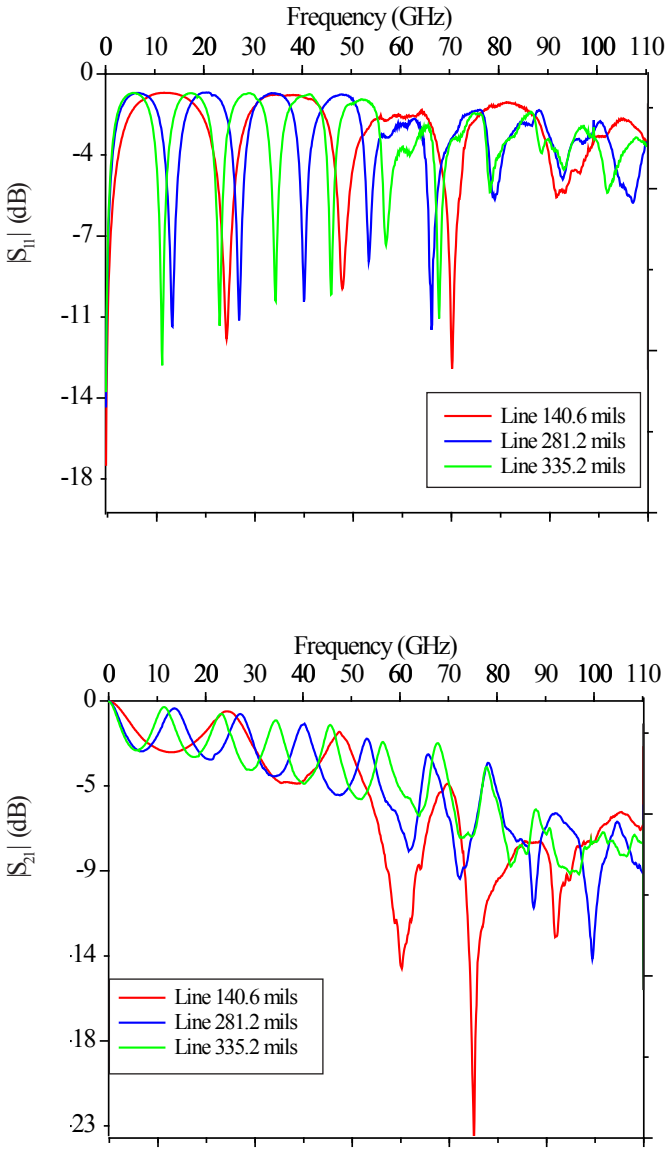


Figure 3.10 Experimental a) return and b) insertion losses for three microstrip lines included in the prototype board.

extremes. Thus, below this frequency, the curves present well defined periodic behavior; notice that in the case of $|S_{21}|$, the corresponding curves also drop with frequency since the lines are lossy. However, as the frequency increases above 50 GHz, the signal transmission is degraded, which is reflected in these curves since unexpected fluctuations occur. This is associated with an inappropriate design of the CPW-to-microstrip transition as is explained hereafter.

If assuming that the unexpected trend followed by the $|S_{11}|$ and $|S_{21}|$ curves is due to misbehavior of the CPW-to-microstrip transition, when applying a deembedding procedure to remove the corresponding effect, the complex propagation

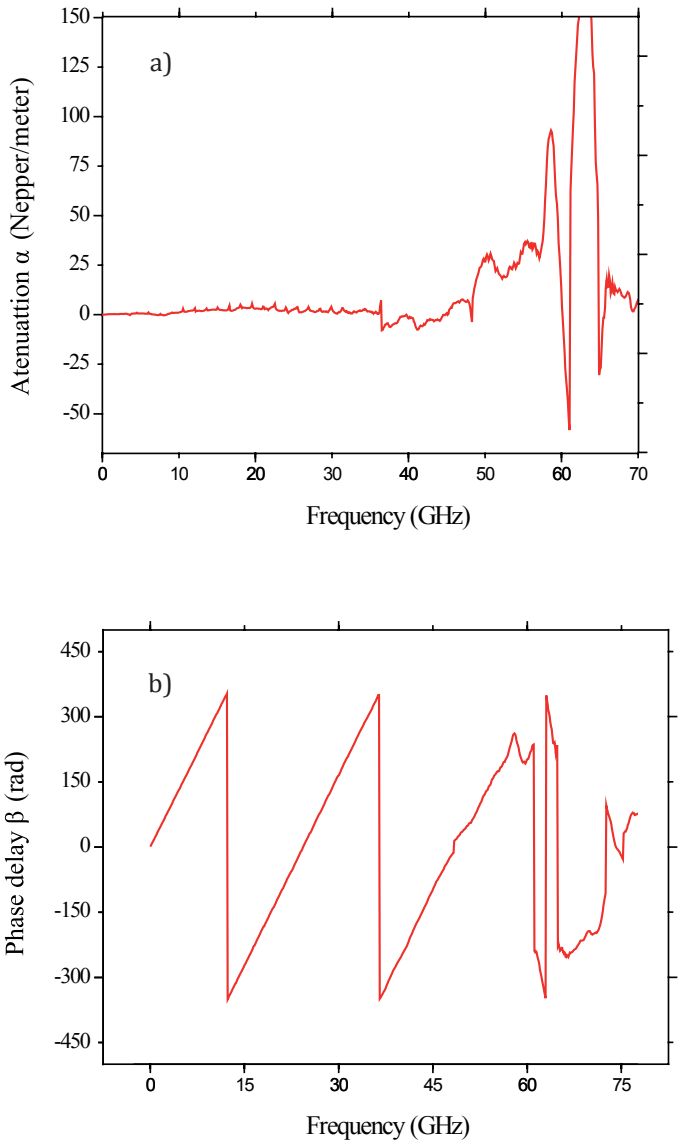


Figure 3.11 Experimental complex propagation constant for the studied lines. a) Atenuattion Constant. b)Phase Delay .

constant can be determined and the associated curves should be smooth when plotted versus frequency. As can be seen in Fig. 3.11 this is clearly not the case. Notice that α and β are very noisy (even when determined using different lines), which means that no single mode of propagation is taking place and that the energy is either being propagated in a multimode way or leaking away from the desired signal path. Thus, concluding this paragraph: the problem is that the CPW-to-microstrip transition is exciting undesired modes of propagation. In order to verify this, the following model implementation was carried out [46, 49, 58].

A CPW-to-microstrip transition can be represented by means of an equivalent circuit such as that shown in Fig. 3.12a. However, this simple model does not allow the proper representation of a transition in which parasitic propagation modes

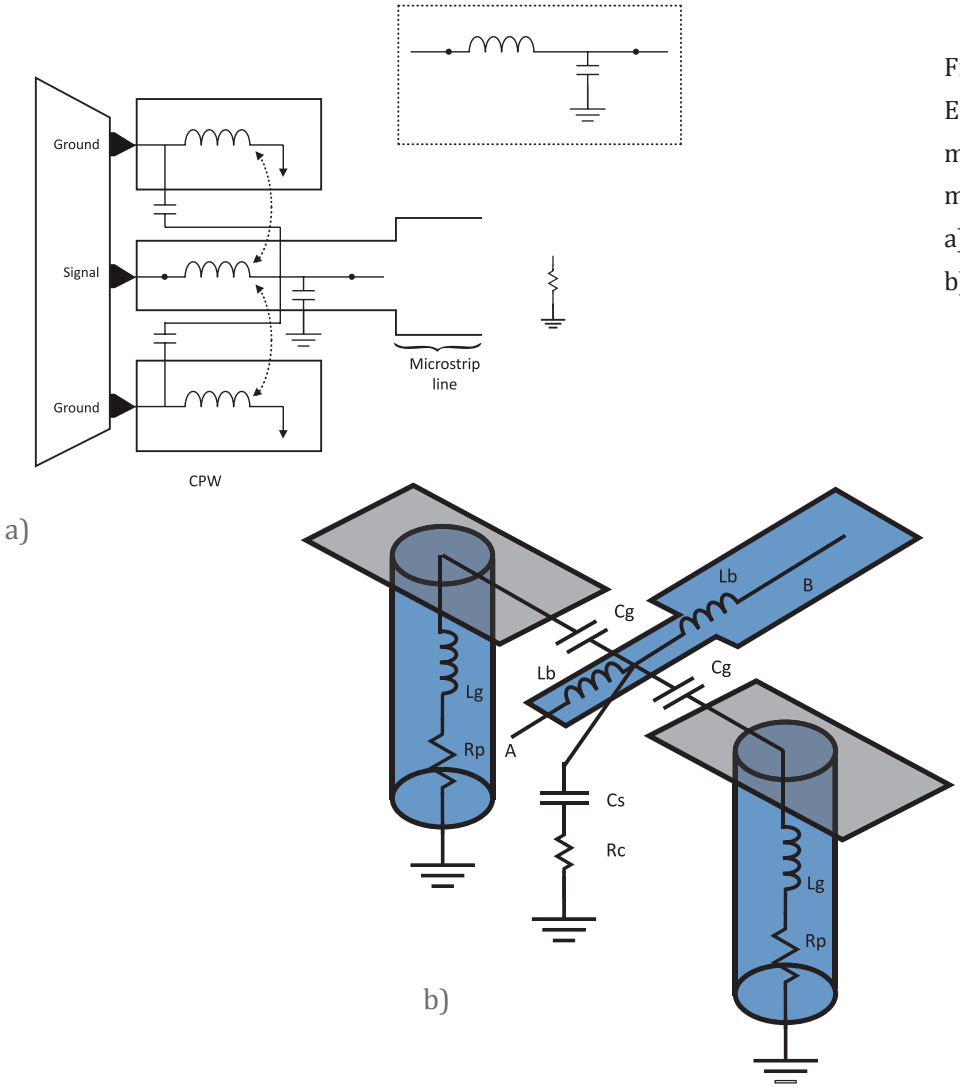
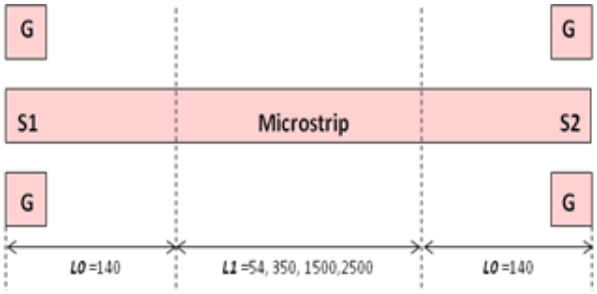


Figure 3.12
Equivalent-circuit models for a CPW-to-microstrip transition: a) simple model, and b) more complete model

are being excited. Thus, using an improved model (Fig. 3.12b) and determining the corresponding parameters, a simulation of the complete test structure including the homogeneous line and the transitions was carried out with Agilent's Advanced Design System (ADS) circuit simulator for the microstrip line with a length of 705 mils and 7.2 mils width. The reason why this line was selected was because the impact of the transitions is more accentuated when the line is made shorter (the DUT and the parasitics become comparable), and this is the shortest line available for analyzing.



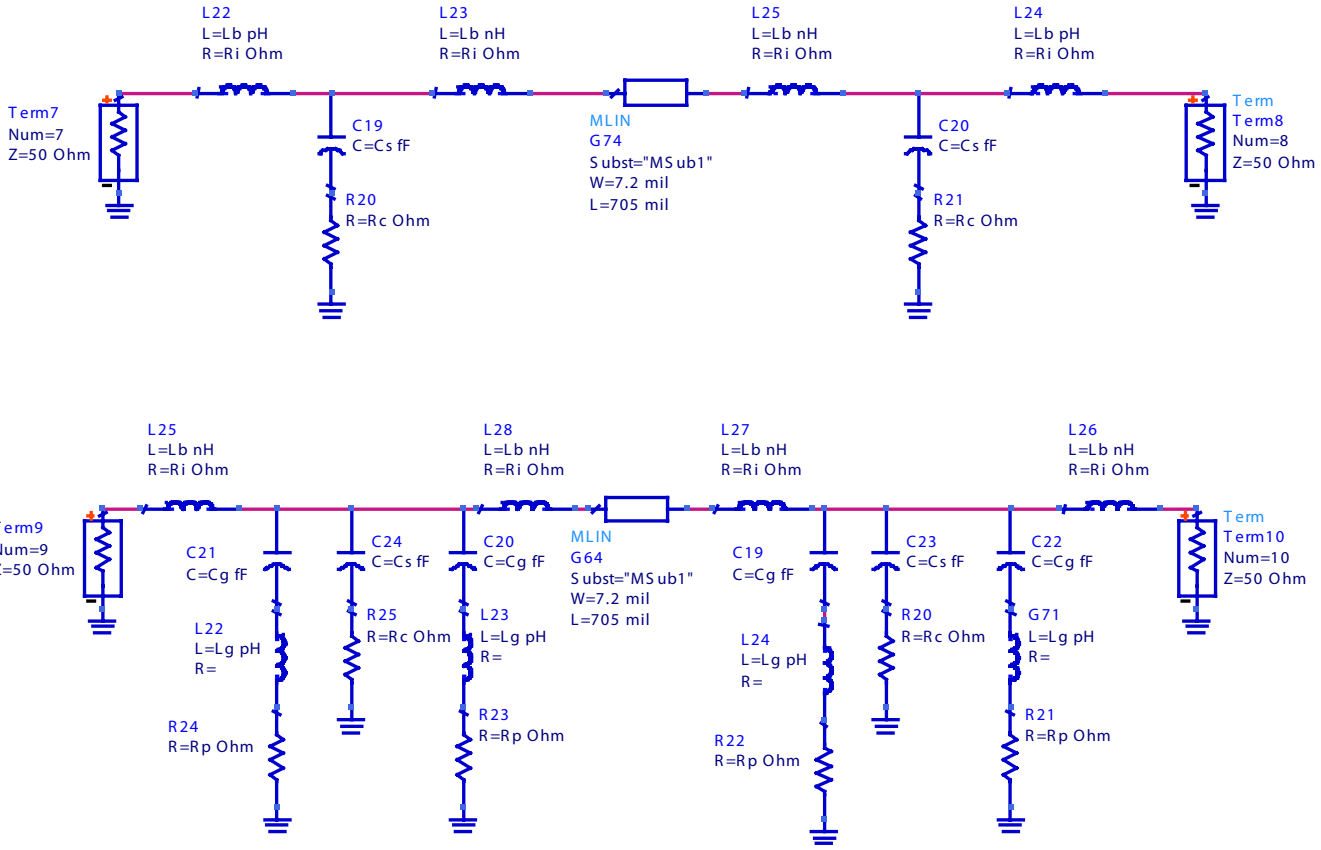


Figure 3.13 Models for the CPW-to-microstrip transition, a) squematic model, b) first approximation, c) second approximation in ADS.

To start with the synthesis, the equivalent-circuit model for the complete test structure was implemented in ADS as depicted in Fig. 3.13. This model includes the lumped elements associated with the transition and a model that describes the behavior of a homogeneous microstrip line (labeled as MLIN). In addition, the simple model of Fig. 3.12b was implemented, to see the associated limitations when representing a transition in which parasitic propagation modes are occurring. The lumped elements were obtained after a process of optimization to finally reach the correlation with the measurements; the values of the lumped elements are shown in Table 3.1. It is worthwhile to mention that analytical determination procedures for these structures when parasitic propagation modes occur are currently under development to further complement this research project.

Parameter	Value	Unit
Lb	0.1	pH
Lg	40	pH
Cs	26	fF
Cg	15	fF
Rc	20	Ω
Rp	3	Ω
Ri	1.5	Ω

Table 3.1
Values for the lumped elements in the model of Fig. 3.16 for a microstrip with 705 mils length.

The correlation between the simulated and experimental S-parameters is shown in Fig. 3.14 and some differences are observed between the proposed transition model and the simple one that neglects the higher order effects. For instance, the simple transition model does not take into consideration the effects introduced by the vias; thus, the signal attenuation that the signal suffers at high frequencies is underestimated by this model. Conversely, the complete model includes this effect, which allow for the proper representation of the transition as the frequency increases. In consequence, a better simulation-experiment correlation is achieved as can be seen in Fig. 3.14.

From these obtained simulation results, it is clear that the transition excites unwanted propagation at high-frequencies and even becomes the dominant loss

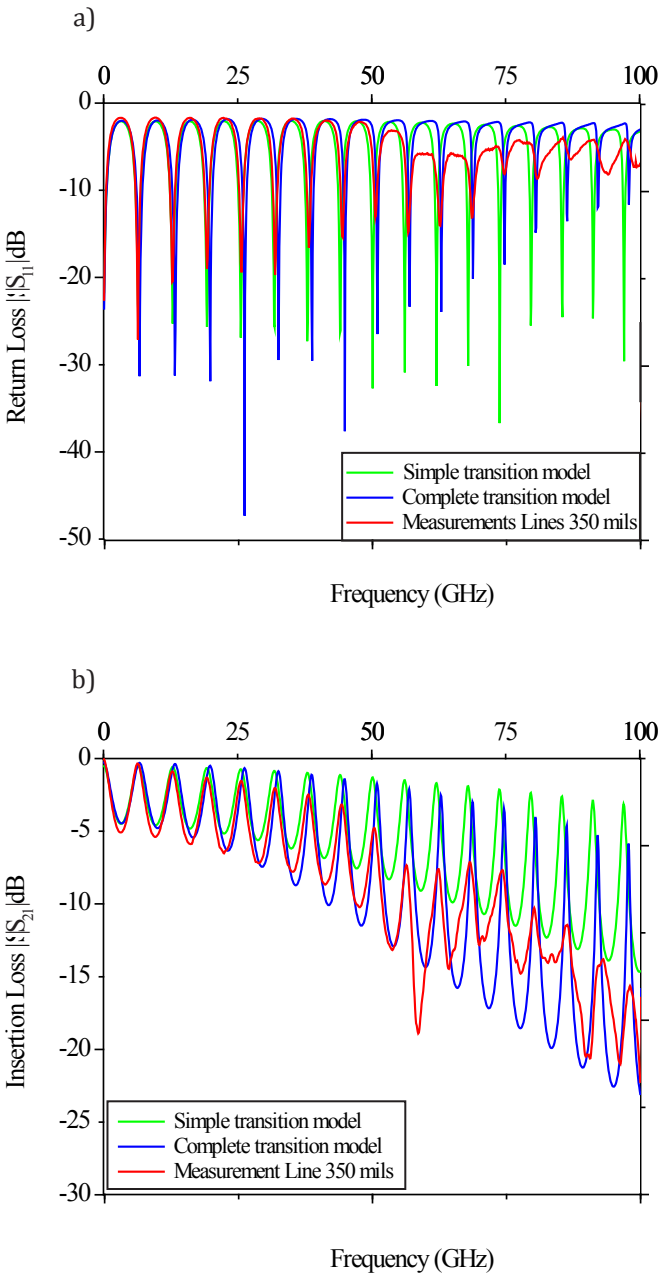


Figure 3.14 Correlation between the simulated and experimental S-parameters corresponding to the microstrips studied in this section (up to 100 GHz). a) Return Loss, b) Insertion Loss.

mechanisms; however, at relatively low frequencies the effect is difficult to observe as can be seen in the limited-range plot shown in Fig. 3.15. This is one of the reasons why some structures that are useful and adequate at low frequencies are implemented in extended bandwidths with no success.

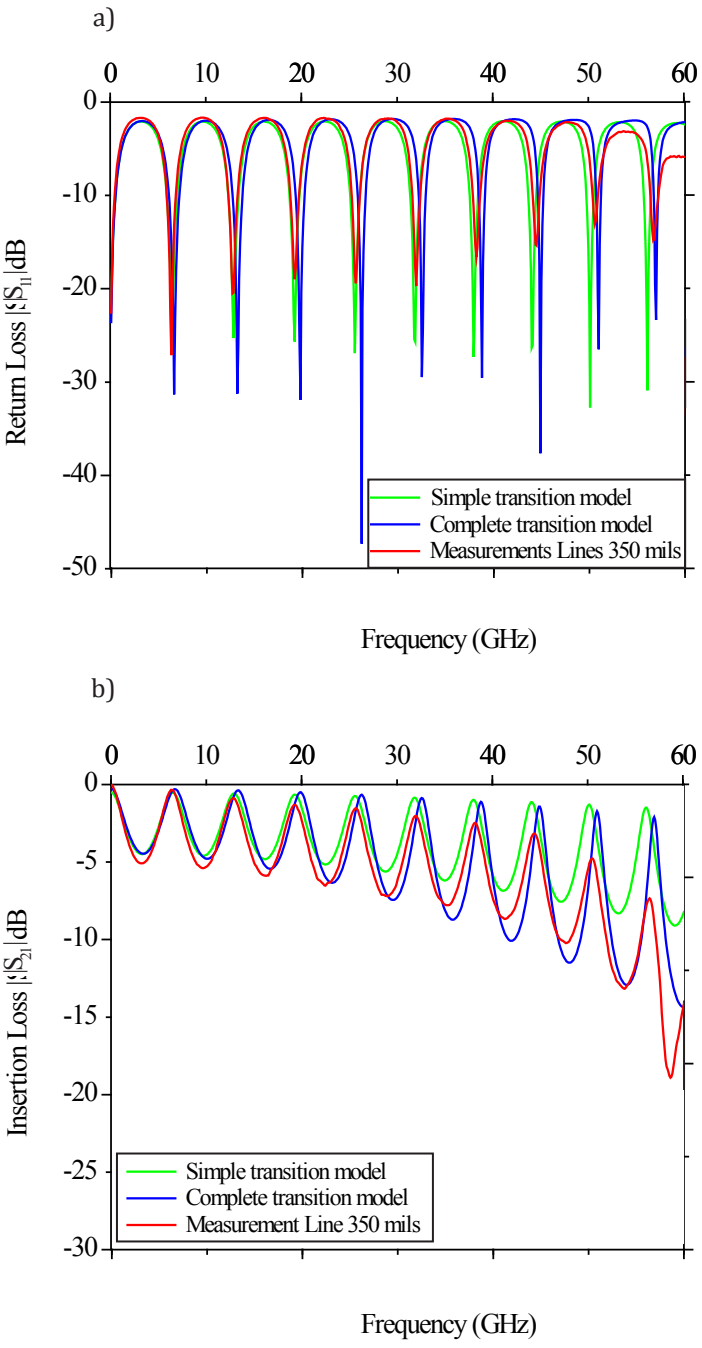


Figure 3.15 Correlation between the simulated and experimental S-parameters corresponding to the microstrips studied in this section (up to 60 GHz). a) Return Loss, b) Insertion Loss

3.2.1 Resonances in Simple Transmission Lines

This electromagnetic effect is frequently found at relatively high frequencies and is due to the fact that at certain frequencies the parasitics associated with a transition may behave as a reflective element (i.e. either an open or a short circuit). Thus, an interconnect (or part of the interconnect) can be seen as an energy-storage-structure at given frequencies. In this case, there are several factors involved in the excitation of resonant modes, among these can be found the imperfection on the signal and return path, imperfections in the termination of the structures (stub, vias, edges, etc.) and the behavior of resonant cavities inherent in planes of packages and PBCs with the induced displacement current from signal transmission or switching noise [61, 65].

The process to excite resonant modes is as follows: the signal travels from a signal source until finding a discontinuity or edge in the signal path, where part of the signal is reflected to the source where it comes from. At this point there are two cases: i) the reflected signal can be added to a new signal if the signals are in phase, or ii) it can be eliminated if the signals are out of phase. This process is repeated each time the transmitted signal is switched. Fortunately, there are some techniques to reduce the excitation of resonances such as: terminating the traces matching the impedance of the line, adding sufficient distributed loss to the signal path to control the Q of the structure, as well as avoiding the placement of stubs or vias that cross trough the structure layer that can excite the parallel plate mode of propagation (see Fig. 3.16).

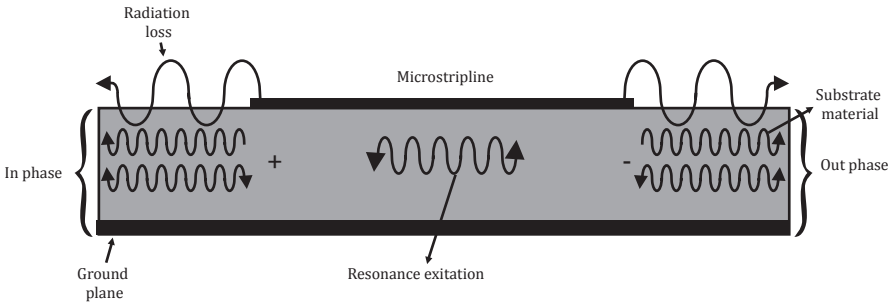


Figure 3.16
Sketch illustrating the resonance excitation of a microstrip line, when the travel signals are in-phase the resonance is presents in the transmission; however, when the travel signals are out-phase no resonance is presents.

The resonances cause huge damage to the performance of high speed interconnection channels. In this section, the occurrence of resonances in a set of microstrip lines with lengths ranging from 1" to 7" fabricated in a PCB is shown. For these lines, the substrate is made of FR4 epoxy dielectric material with a loss tangent of 0.02 and relative permittivity of ϵ_r=4.4. The thickness of the dielectric layer is 31 mil. Details about the structure of these lines are given in Fig. 3.17.

The microstrip lines studied in this section present resonances at 38 GHz as can be seen in the insertion and return loss plots shown in Fig. 3.18, which is due to the fact that the parasitic effects associated with the electrical transition from the probes to the lines behave as a resonant circuit at that specific frequency. As is well known, the resonance increases the losses at certain frequencies which is pointed out by the abrupt reduction in the transmission of the lines, as can be seen

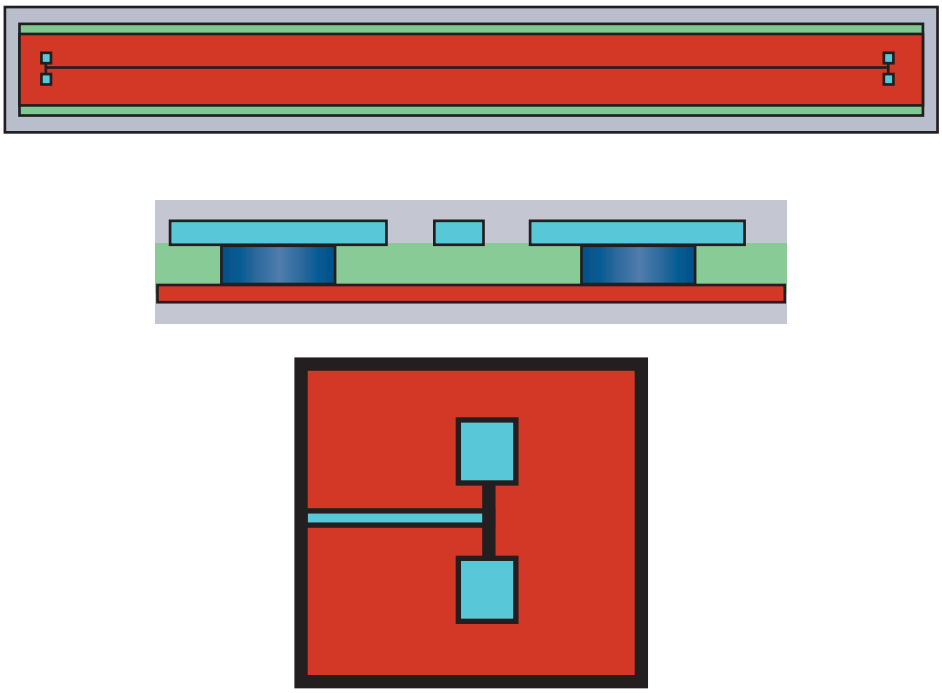


Figure 3.17 Details of the structure of the microstrip lines used during the study of resonance effects.

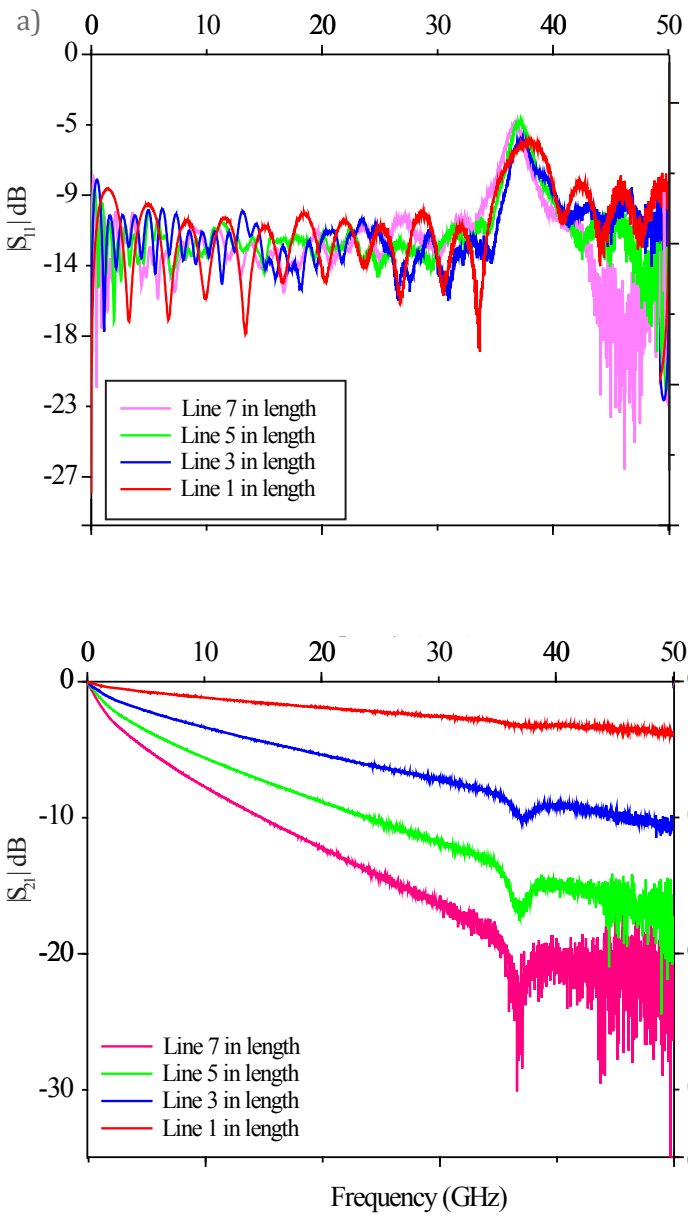


Figure 3.18
a) Insertion and b) Return losses showing that the resonance occurs at the same frequency independently of the line length.

in Fig. 3.18b; besides, the return loss presents an increment at 38 GHz, which indicates that the energy of the signal at that specific frequency is reflected. Thus, the resonance makes the structure to behave as a filter with a sharp bandwidth, this type of filter is known as notch filter. Notice in Fig. 3.18 that the length of the lines is not related to the frequency at which the resonance occurs. This is because the "resonant circuit" is associated with the transition used to probe the structure.

To find out how the resonance affects the basic parameters of the microstrip lines, the constant of propagation was determined for the measured lines using a line-line extraction method (a pair of lines are used to determine γ). In this case, when calculating the propagation constant of the traces, an abrupt increment in the real part of the propagation constant (α attenuation) is observed, which is a result of the resonant behavior in the traces (Fig. 3.19a). However, the imaginary part β of the propagation constant, the phase delay does not present any considerable change as can be seen in Fig. 3.19b. This means that the speed of the signal is not affected by the resonance.

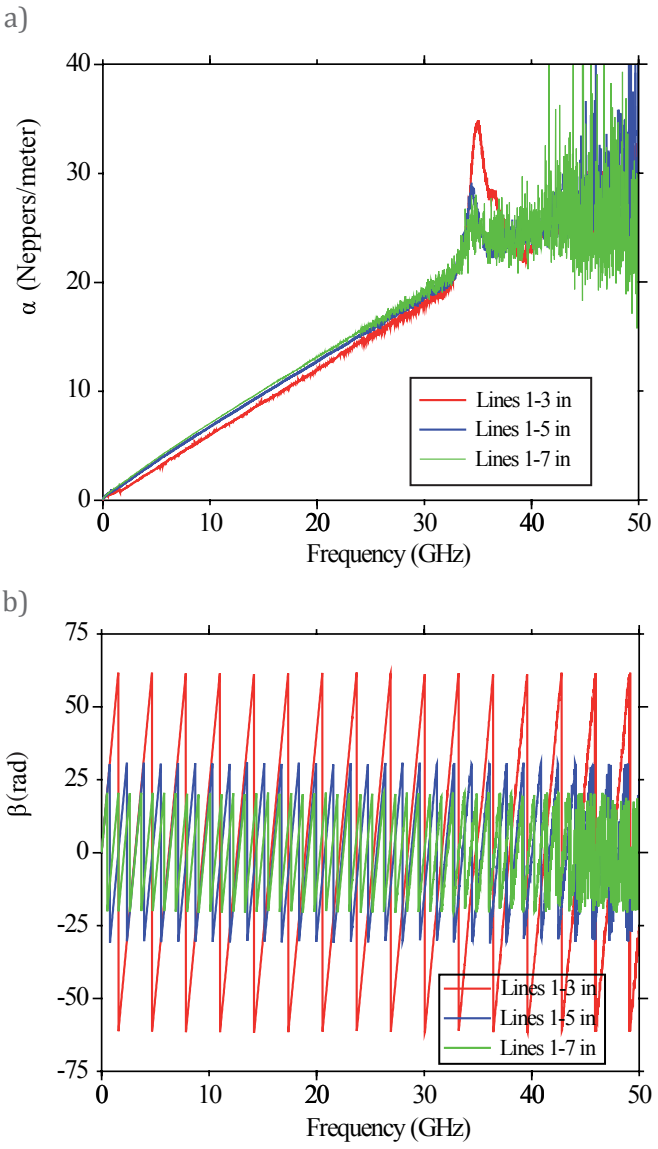


Figure 3.19 Complex propagation constant (a)attenuation and b) phase delay) extracted using different pairs of lines. The impact of the resonance effect is seen in α at the same frequency for every pair of lines.

Again, the extracted γ shows that the resonance is present at the same frequency, no matter the length of the microstrip lines. This is concluded from the fact that different pairs of lines were used to obtain the complex propagation constant and the peak in the attenuation occurred at the same frequency. However, lower impact of the resonance was observed when characterizing the longest line (7 inches). This is due to the fact that the parasitic effects are better seen in relatively small test structures where the DUT is comparable to the parasitics.

In the particular case studied in this section, the discontinuities in the signal path introduced by the CPW transition are the source of the resonance in the transmission to the microstrip lines. The change in the propagation mode between the CPW transition and the microstrip line affect signal integrity; hence, there will be energy leakages.

Finally, Fig. 3.20 shows the experimentally obtained attenuation for different pairs of lines and the function:

$$\alpha = constant_1 \sqrt{f} + constant_2 f \tag{3.1}$$

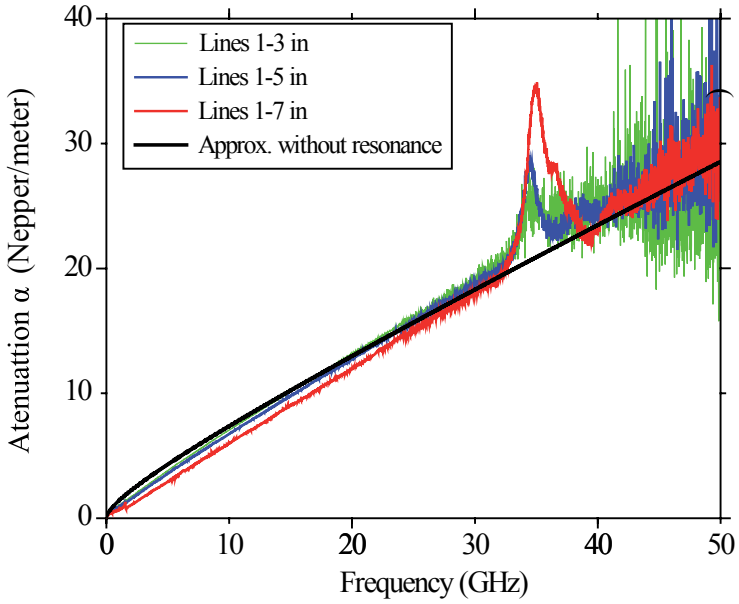


Figure 3.20
Experimental and fit using (3.1)

which describes the behavior of the attenuation for a line fabricated on PCB. The first term in the second member of this equation represents the metal losses (proportional to the square root of frequency due to the skin effect), and the second term represents the dielectric losses (approximately proportional to frequency). Using a simple regression, the experimental attenuation versus frequency curves can be fitted. Thus, after implementing the model of a transmission line using the corresponding characteristic impedance and propagation constant the resonance effect can be isolated and studied separately.

3.4 Conclusion

The complex design and the high frequencies required in the currents structures excited the propagation of second order effects or high order effects which represents energy that cannot be recovered at the end of the transmission path. Thus, in order to improve the performance of the devices it is necessary to study the sensitivity of a particular structure to effects that become apparent at high-frequencies. In this chapter, some of the most representative effects occurring in interconnects when used for high-speed signal propagation where studied. Although these effects were studied in relatively simple structures, a good insight about the possible consequences in the propagation of signals in more complicated channels was given in perspective.

Chapter 4
Signal Propagation on Packages

This chapter presents some details about the signal propagation in interconnection channels including packages. As will be shown, these structures may considerably degrade the performance of a chip-to-chip link not only by increasing the return and insertion losses, but also introducing undesirable effects such as resonances and parasitic mode excitation. For this reason, this chapter is completely dedicated to analyzing packages from both experimental and simulation points of view. Firstly, the problem of parasitic mode generation is presented by comparing the operation of packages with that of quasi-rectangular waveguides fabricated in PCB technology to show the mechanism of generation of non-desirable signals within a package. After carrying out this comparison, the package structure is studied using full-wave simulations in order to point out the impact of the configuration of the ground-vias in the performance of this type of structures. This analyses will allow to establish the dependence of the size of the package with the frequency at which the parasitic mode of propagation occurs, and provide guidelines for the proper design of this type of structures.

4.1 Comparison Between Packages and SIWs

In general terms, a package is a multilayer structure with several vertical transitions that allows the interconnection of bare dies with a PCB[65]. In addition to the signal path, this structure includes many ground vias that interconnect the different ground layers and prevent the propagation of parasitic modes (to avoid leakages), see Fig. 4.1 [64, 66-68]. Unfortunately, the complex design of the package presents several high-order effects. One of this is the propagation of parasitic modes within the structure, which degrades the corresponding performance of the interconnect in which the package is embedded.

Before starting with the analysis, it is necessary to briefly describe the structure of a package (see Fig. 4.1). A typical package includes a signal via that will

carry the signal from an upper to a bottom layer. Thus, the signal via crosses through several ground planes that ideally present the same potential. However, every interconnect should include a return path that is achieved by interconnecting all the ground planes within the package using ground vias. An additional function of these vias is avoiding the excitation of parasitic modes such as the parallel plate mode, as shown in Fig. 4.2a. In this regard, the objective of the vias is to serve as an electric wall to prevent energy leakage, thus withdrawing any possibility of developing electromagnetic effects that could degrade the signal transmission (see Fig. 4.2b).

After this brief introduction, it is clear than there are some similarities between the structure of a package and a rectangular waveguide excited by means of a monopole antenna[48]. Thus, the ground vias of the package can be seen as the walls of the waveguide, whereas the signal via is seen as the monopole that is exciting the waveguide structure. In fact, in PCB technology, a way to form a rectangular waveguide is by placing parallel plates of conductor material between a layer of dielectric material, whereas the walls are formed by means of metallic posts placed close enough to avoid the signal leakage or at least to keep this at a minimum level. This structure is known as a substrate integrated waveguide (SIW) and is depicted Fig 4.3. This figure also shows the equivalence between an SIW and an actual rectangular waveguide. In fact, there are several techniques to calculate the appropriated distance between posts in an SIW for specific frequencies of operation [69]. Furthermore, a thumb rule is that the distance between post should be smaller that the wavelength λ of the signal at the maximum frequency of operation. Notice also in Fig. 4.3 that for practical proposes, an SIW can be seen as a rectangular waveguide with an effective width.

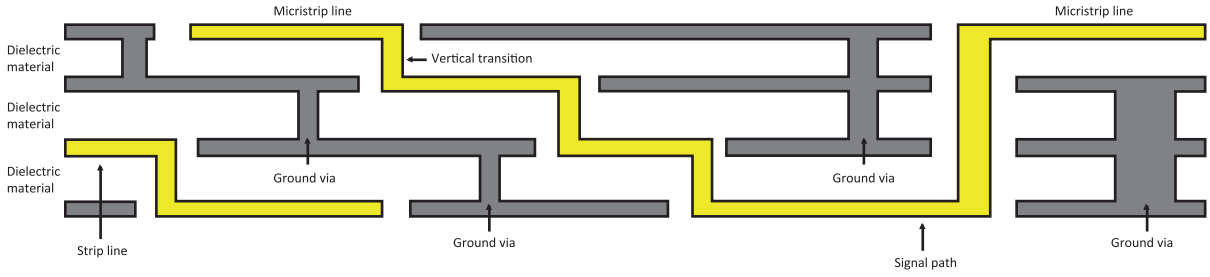


Figure 4.1
Basic structure of a generic pa ckage.

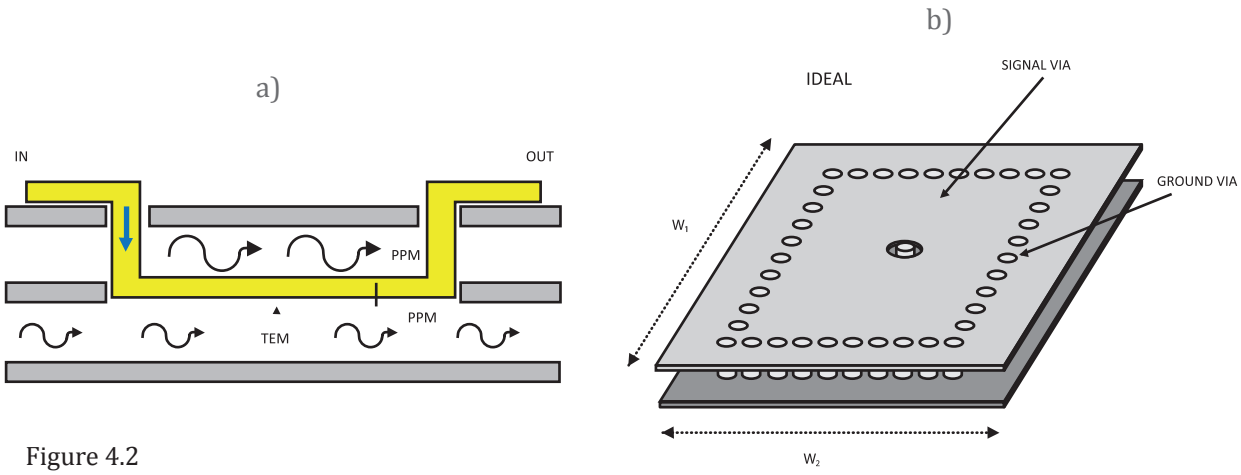


Figure 4.2
Structure of a package: a) side view showing the parallel plate mode propagation, and, b) ideal via fence to avoid parasitic propagation within the package.

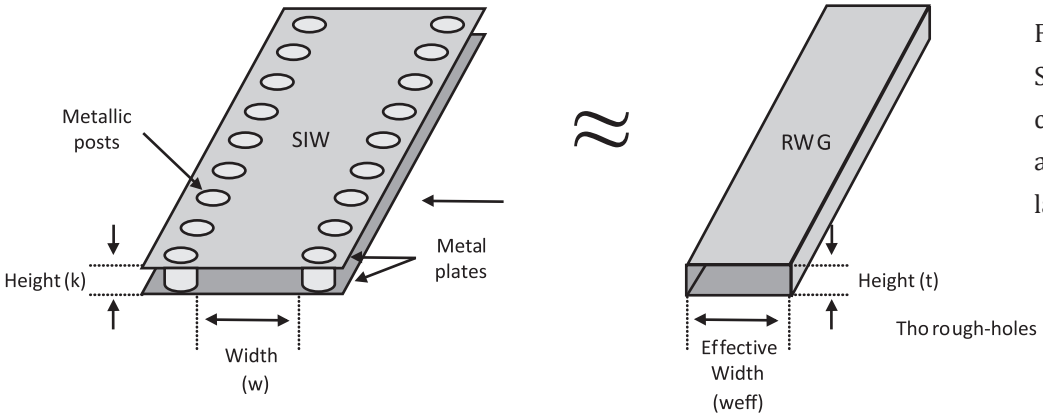


Figure 4.3
Sketch of an SIW compared with an actual rectangular waveguide.

In order to obtain the cutoff frequencies of an SIW, it can be used the known formula for rectangular waveguides (4.1) assuming that the effective width of the SIW is given by (4.2).

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{w_{eff}}\right)^2 + \left(\frac{n\pi}{t}\right)^2} \tag{4.1}$$

$$w_{eff} = w - \frac{d^2}{0.95b} \tag{4.2}$$

In (4.1), *m* and n are the mode indexes, ε and μ are the material permittivity and permeability respectively, *t* is the waveguide dielectric thickness, and w_{eff} is the effective width. In (4.2), *d* is the posts diameter, *b* the center-to-center post distance, and *w* is the width defined. Fig. 4.4 shows in a more specific way how a package can be seen as an SIW. The signal via acts as the exciting element and is commonly located at the middle of the structure. In this case, odd propagation modes will occur and the one with the smallest cutoff frequency is the TE_{10} mode; the configuration of the electric field for this mode is depicted in Fig. 4.5.

Thus, after the cutoff frequency corresponding to the fundamental propagation mode (in this case TE_{10}) is reached, the signal transmission will start. Notice that whereas in the case of an SIW the transmission is desirable, when analyzing a package assuming that the ground vias behave as the walls of an SIW, the transmission in horizontal way is undesirable. Thus, when reaching the corresponding cutoff frequency, parasitic modes of propagation will occur.

Figure 4.4 Comparison between the structure of a package and a SIW

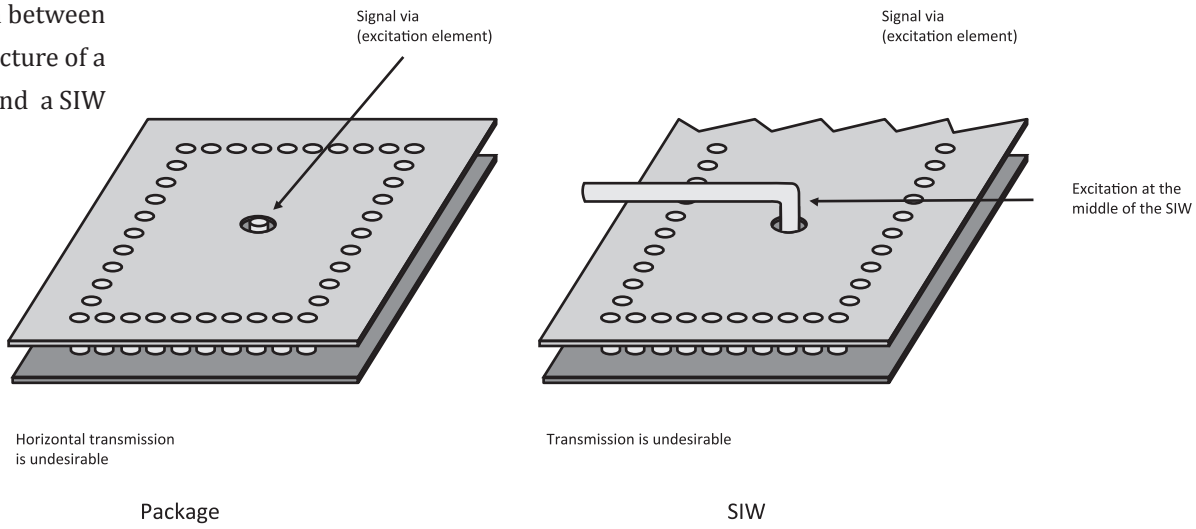
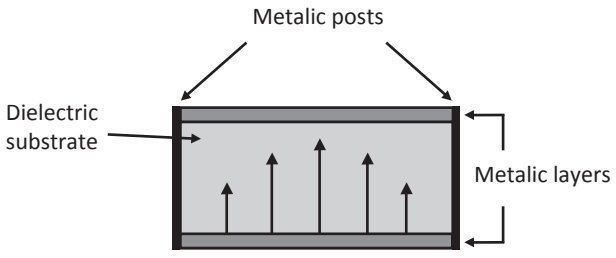


Figure 4.5 Cross section of an SIW illustrating the configuration of the E-field in TE_{10} mode.



4.1.1 Experimental Analysis of SIW Structures

In order to show how the size of an SIW determines the cutoff frequency of the fundamental propagation mode and how this may help in determining the optimal size of a package, several measurements were performed. In this regard, a set of SIWs was fabricated on a PCB made of Rogers RT/Duriod 5880 as dielectric material, with a dielectric thickness of 0.79 mm (31 mils), and the nominal relative permittivity and loss tangent for this material at 50 GHz is ε=2.2 and tanδ=0.0017 respectively. The dimensions of the SIWs is 5 inches of length, different widths ranging from 1.6 mm to 4.06 mm (64 to 160 mils), the diameter of the metal post is 0.48 mm (18.8 mil), and the center-to-center distance between posts is 0.68 mm (27 mils). For these structures, the corresponding S-parameter measurements were taken up to 110 GHz using CPW probres with an LRM-calibrated VNA.

In order to perform the measurements of the SIWs structures a monopole antenna was used as the exciting element placed at both edges in the middle of the structure's width. This can be seen in Fig. 4.6. It is important to mention that a deembedding process was not performed in this case because it is not necessary to remove the effect of the monopole antenna; thus, the measurement presents the effects of the text fixtures (the pads are placed as close as possible to the exciting post).

The transmission of the SIWs structures was obtained from the measurement of the S_{21} parameter. In this case, it is expected that the transmission of the structures changes as the width of SIWs is made smaller. In fact, the SIW presents a higher cutoff frequency as the structure is narrower. This effect is shown in Fig. 4.7. Hence, the signal must have a relatively smaller wavelength to be transmitted in a narrow SIW structure. Notice, however, that the transmission of a narrow SIW is not as "good" as the transmission of a wide SIW. In fact, the transmission presents low quality and more insertion loss as the SIW is made narrower.

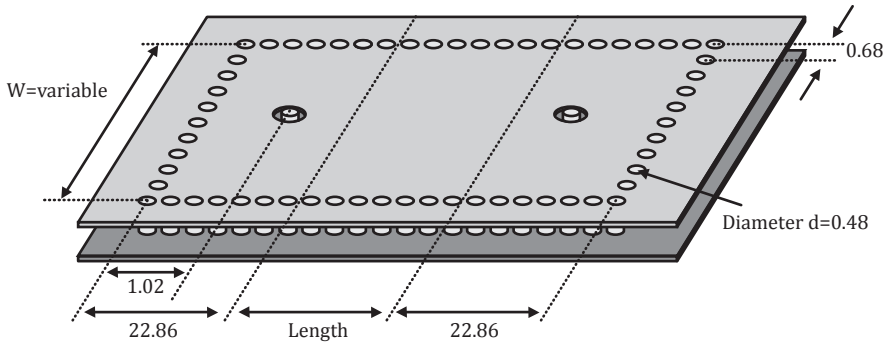


Figure 4.6
Dimensions (in mm) of the measured SIWs. a)squematic model, b) picture.

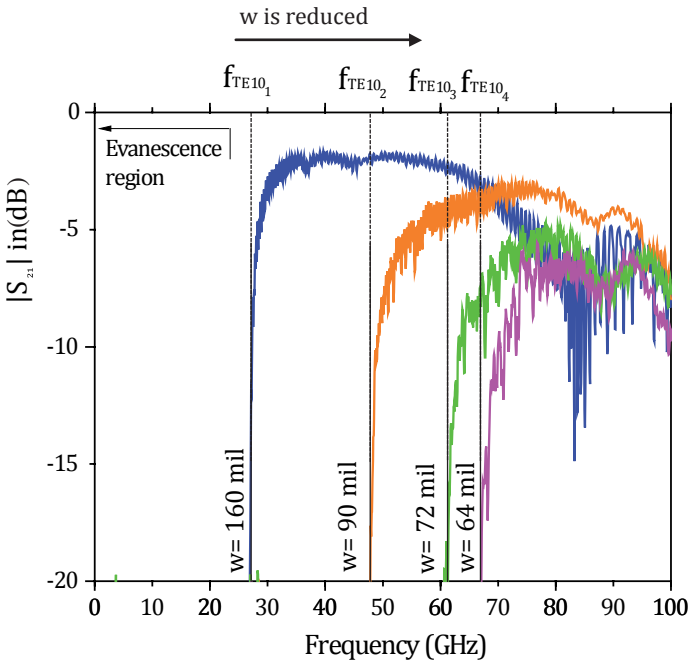


Figure 4.7 Insertion loss (S_{21}) for the measured SIW's showing that the cutoff frequency presents higher values when the structure is made narrower.

4.1.2 Experimental Analysis of a Package Structure

The vias are an important part in the design of package structure, because these are employed to interconnect power and ground planes to keep the corresponding potentials as close as possible at different levels within the structure. This withdraws any possibility of exciting unwanted modes of propagation. However, placing ground vias inside structures like packages introduce new boundary conditions, which in some cases originate a waveguide behavior, like the one depicted in Fig. 4.8, where the ground vias form a hypothetical waveguide around the vertical transition of the packages. Thus, in accordance with this figure and from the measurements of the SIWs, it can be concluded that, in order to avoid the waveguide mode of propagation inside of the packages the corresponding width and length should be small. This sends the cutoff frequency of the TE_{10} mode to higher frequency where the structure will not be practically used.

An additional experiment carried out as part of this project consists in modifying the configuration of the ground vias of a package to expose the waveguide behavior that this structure presents. The package to modify is referred to as a "thin package" because the main vertical transition (the core via) has a length of 60 µm, where usually the length of this center via is 800 µm. The vertical transi-

tion is composed of vias, microvias and pads, whereas the core of the package is a plated-through-hole (PTH) which interconnects the superior vertical transitions with the bottom vertical transitions which conform the signal path. Additional vertical transitions are placed between layers to interconnect the ground plane. A side view of the package is shown in Fig.4.9a, where the signal path and the surrounding ground vias can be observed.

From a 3D-simulation of the package, the obtained S-parameters showed a resonance effect near 27 GHz, as can be seen in Fig. 4.9b. To analyze the package, it was divided in to three sections to investigate the origin of the resonance: the first and third sections are composed by the microvias, while the second section is the layer where the core via is placed. After the simulation of each section and the whole package structure, the results show that the section that is responsible for the resonance effect is the second section, or principal layer of the package.

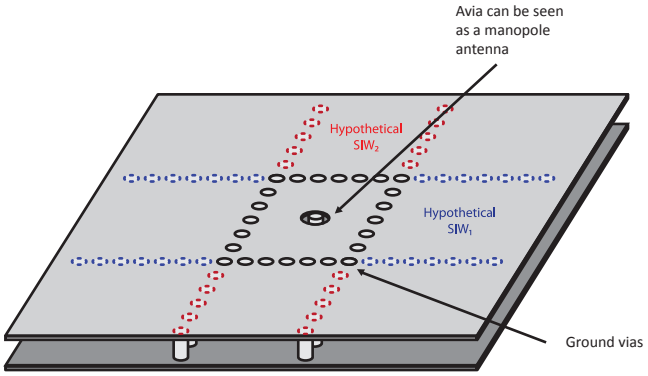


Figure 4.8 Hypothetical SIWs in a package structure.

a) b)

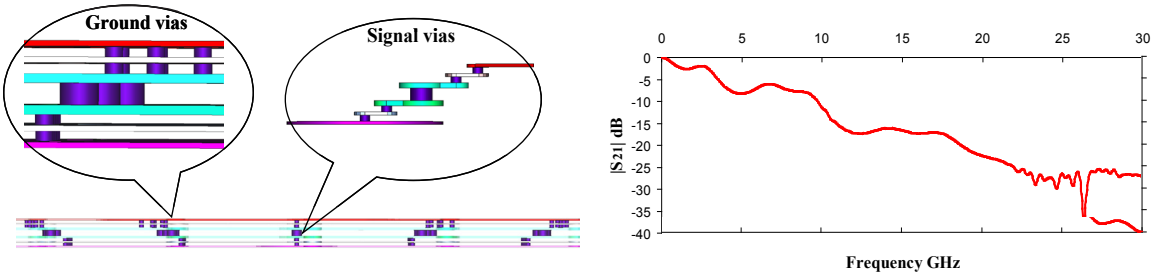


Figure 4.9 a) Side view of a package model implemented in a 3D electromagnetic solver, zoom in to show the ground and signal vias. b) Corresponding insertion loss (S_{21} parameter) for this structure.

This means that the ground vias placed in this layer have an influence on the resonance effect, to prove that, the number and place of the ground vias was changed, and the changes on the resonance effect after these modification was systematically observed. The ground vias on the core layer can be seen in Fig. 4.10a where there are red circles forming two concentric squares of different side lengths. The core layer with all the ground vias presents a resonance at 29 GHz, with a magnitude of -1.48 dB.

The first step was eliminating the ground vias that conform the smaller square, whose side length was 2.85 mm (112.2 mils) see Fig. 4.10b, this changes modified the frequency and amplitude of the resonance; now the resonance is near to 15 GHz and with a magnitude of -0.9 dB. The second step is eliminating the bigger square whose side length is 5.4 mm (212.59 mils), see Fig. 4.10c. In this case, the change modified the resonance frequency to higher value close to 30 GHz, with a magnitude of -1.4 dB. To explain these changes in the transmission of the core layer, Parallel Plate Waveguide (PPW) propagation was assumed and analyzed [61].

The third step is comparing the cutoff frequency of the PPW formed by the ground on the core layer with the frequency at which the resonance occurs using (4.10).

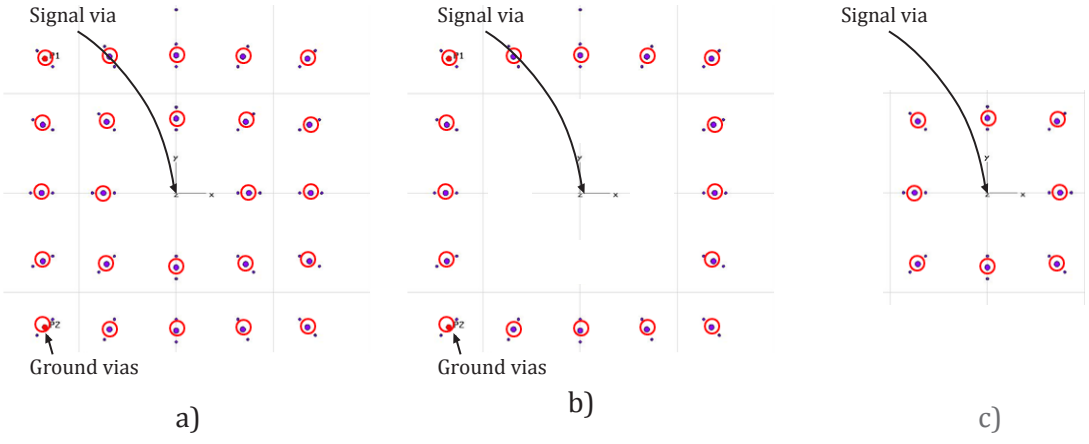


Figure 4.10
Zoom to the front view of the package model to show the ground vias.
a) Original configuration of ground vias on the core layer,
b) Large square configuration of ground vias on the core layer,
c) Small square configuration of ground vias on the core layer

The result of calculating the cutoff frequency of the PPW and comparing with the frequency at which the resonance occur, was that the frequencies match so the core layer behaved like a sort of a waveguide. In this case, the associated cutoff frequency corresponds to that at which the presence of the resonance occurs. That means that, when reaching the cutoff frequency of the PPW, the structure starts to transmit a new mode of propagation which affects the original transmitted signal. This process is qualitatively shown in Fig. 4.11.

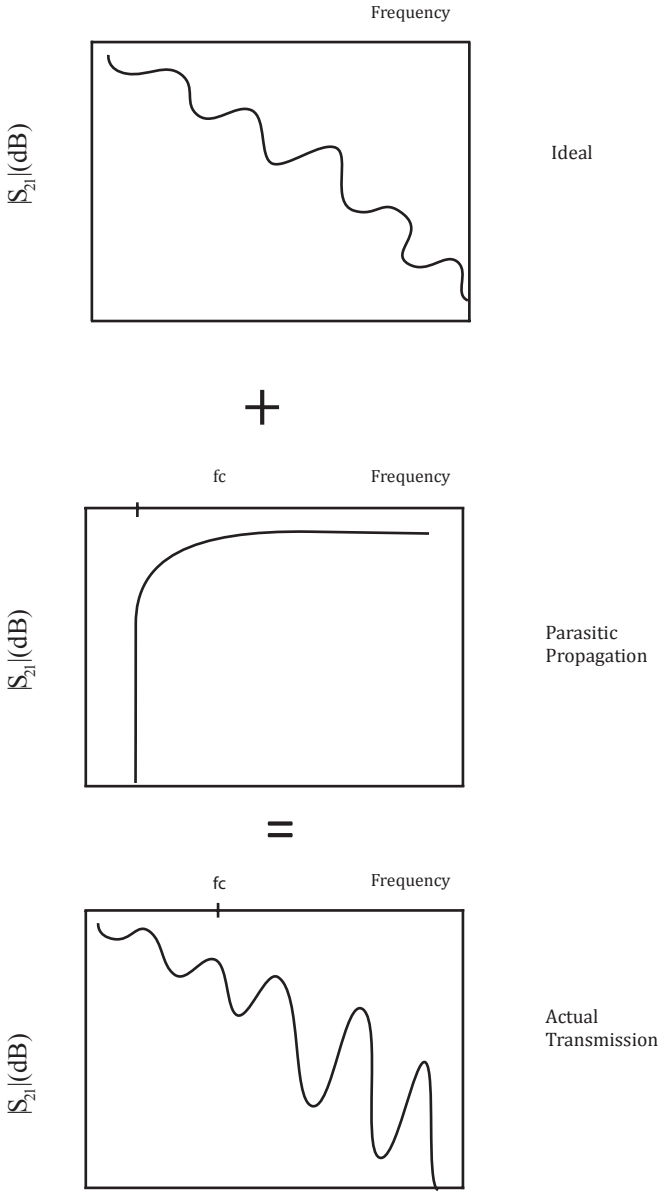


Figure 4.11
Hypothetical superposition from differents propagation modes in the package transmission.

4.2 Impact of the configuration of ground vias on the performance of vertical transitions used in electronic packages

The analysis presented in this section provided a better understanding between the ground vias and undesired effects (e.g. resonances) presented in the electrical response of packages. Fig. 4.9a gives an idea about the complexity of the structure of a package. These types of structures present many effects that degrade the integrity of a signal. Thus, in order to perform the analysis of the impact of parallel-plate propagation modes in a package, a typical vertical transition that is used to implement packages was studied. This structure consists of two parallel-plates, signal via, microstrip lines where the stimulus is applied, and the ground vias used to short-circuit the parallel-plates, see Fig. 4.9. All the analysis is based on full-wave simulations using commercial electromagnetic simulators. In all the implemented models, the boundary conditions were defined as open or absorption to avoid errors in the simulations, and the frequency range of our simulations was from 0 to 50 GHz, necessary frequency range to transmit up to the third harmonic from the desing central frequency, to keep the signal distortion at minimum.

4.2.1 Methodology of analysis

Fig. 4.9b shows the simulated insertion loss of a vertical transition surrounded by ground vias were a resonance at 27 GHz was observed. Since the origin of this resonance is associated with the presence of parasitic parallel-plate modes in the structure, a series of simulations were carried out to verify the effect introduced by the ground vias. To simplify the analysis, a basic structure used in practical packages was studied, which is a single vertical transition as depicted in Fig. 4.11. This structure consists of two copper parallel-plates with a surface of 1800 μm x 2115 μm, and a thickness of 15 μm. The signal path consists of a via with a radio of 31 μm and is terminated with pads with a radii of 66 μm and a thickness of 25 μm. This structure is fed with a microstrip line with a length of 147.4 μm and a width of 26 μm. The thickness used for the dielectric is 70 μm, and the corresponding relative permittivity (ε_r) is 3.41. The return path is formed by ground vias, and consists of three cylindrical structures with radii of 33 μm, 66 μm and 33 μm. In this structure, the resonance occurs at 17.8 GHz.

The objective of performing the simulations is to obtain information on how the location of the ground vias influences the magnitude and frequency at which

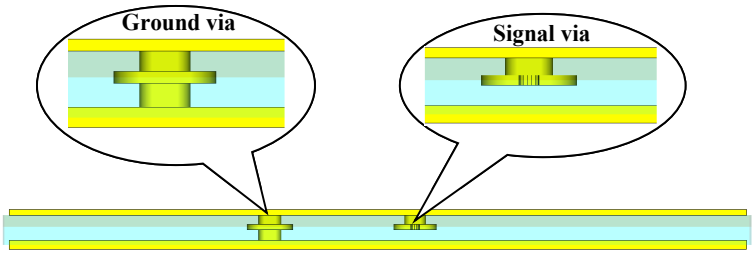
the resonances occur in the simulations, which varies in a systematic way by changing the:

a. distribution of the ground vias,
b. distance between the ground vias and the signal via.

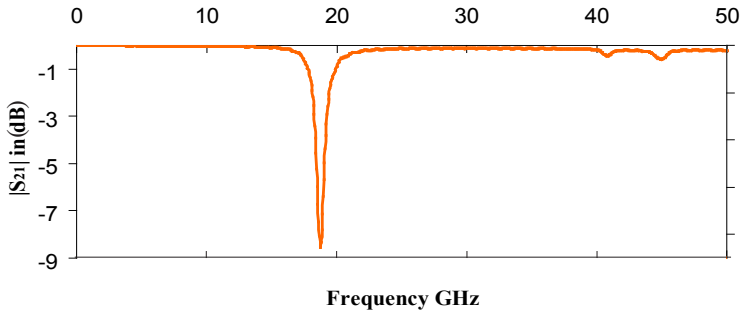
These simulations will provide information about the electric and magnetic fields, and also about the transmission characteristics of the structure from the insertion loss (S_{21}).

a. Distribution of the ground vias

The objective of this simulation approach is to observe the impact of modifying the separation between the ground vias by changing their distribution around the signal via. Specifically, this will provide information on how this affects the frequency at which the resonance occurs. Firstly, a structure including only one



a)



b)

Figure 4.12
a) Side view of the transition implemented in a 3D electromagnetic solver.
b) Corresponding insertion loss (S_{21} parameter) for this structure.

ground via located at a distance of 590 μm from the center of the signal via was simulated. The 3D model for this structure is depicted in the Fig.4.12 a and b. As can be seen in Fig. 4.12b, the resonance in this case appears at 18 GHz with a peak loss of −8.5 dB. Afterwards several different patterns for the ground vias were implemented: triangle (three ground vias), square (four ground vias), hexagon (six ground vias) and circle (twelve ground vias). In Fig. 4.13, a comparison of the insertion loss (S_{21}) obtained for each one of these structures is shown. In all cases the ground vias keep the same distance from the signal via.

Our simulation results agree with the investigation presented in [61], and show that as the number of ground vias increase (reducing the separation between ground vias) the peaks in S_{21} (which are associated with resonances) occur at higher frequencies and show lower insertion loss. This strongly suggests that the dependence between the signal wavelength and the separation between ground vias can be inferred from the simulations, thus, as the separation between the ground vias is made smaller the wavelength of the signals that may leak away the structure will be smaller, which implies that the resonance will occur at higher frequencies. The ideal case to avoid signal leakage is a metallic wall (i.e. an electric wall, Fig. 4.2b) interconnecting the ground plates and surrounding the signal via, which can be practically implemented in a PCB by means of closely spaced ground vias, in which case no resonance has been reported.

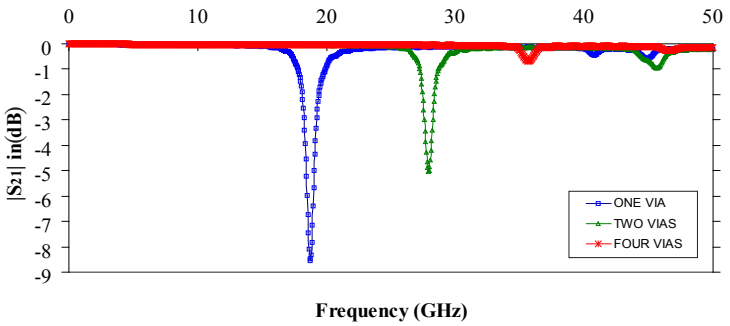


Figure 4.13 Insertion loss ($|S_{21}|$) versus frequency curves for structures with different number of ground vias. The extreme values are one (blue curve) and four (red curve).

b. Distance between the ground vias and the signal via

Once a specific geometric pattern is selected, the next step is varying the distance between the ground vias and the signal via whereas the same distance between ground vias is kept constant. In accordance with the simulation results shown in Fig. 4.14, the frequency at which the resonance occurs changes when this separation is modified. In [61], it was pointed out the fact that as the ground vias are located closer to the signal via, the resonance will occur at a higher frequency. However, we have observed that the trend is not linear since when the ground vias are located very close to the signal via, the resonance is presented at low frequencies and with a considerable insertion loss (S_{21}) due to a direct interaction between the signal and ground vias associated with electromagnetic coupling. As the distance between the signal and ground vias is increased, the resonance frequency moves to higher values, until a given point where the dependence starts following the trend described in [61]. The presence of a second resonance is the result of the propagation of higher order modes, which have a higher cutoff frequency than the principal mode of propagation, which is why the insertion losses are lower at the second resonance.

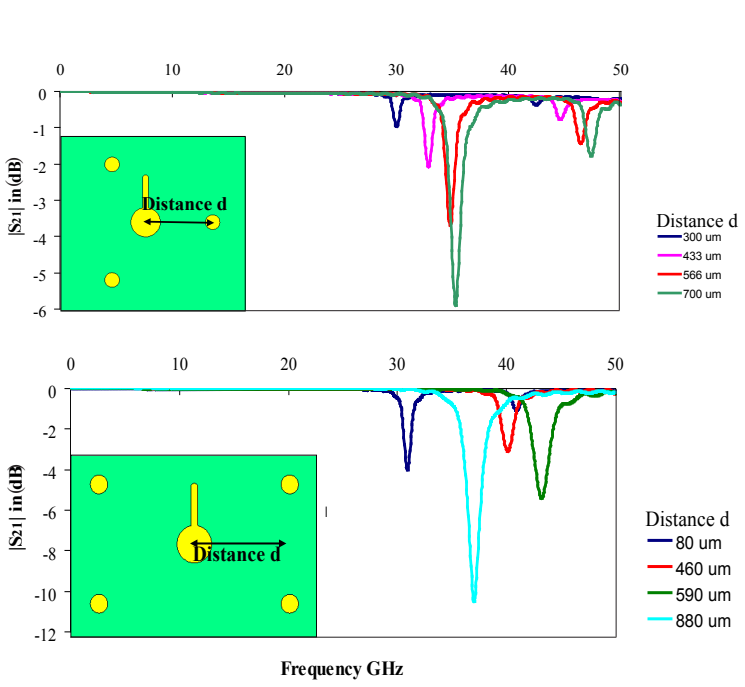
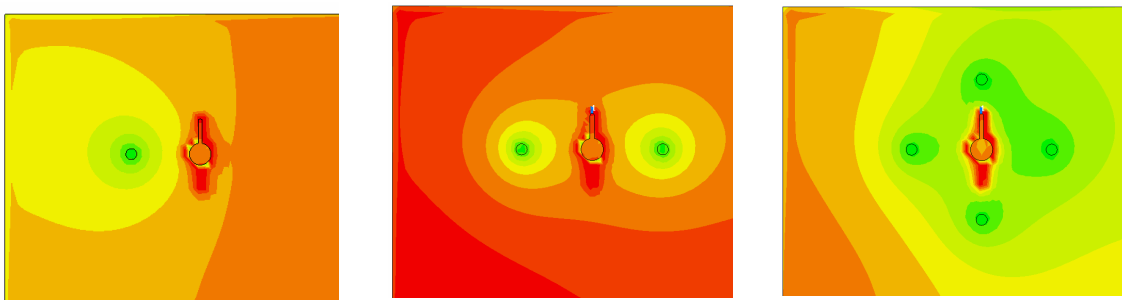


Figure 4.14 Insertion loss ($|S_{21}|$) versus frequency curves for structures with different configuration of vias: a) triangle (center-to-center distance between the signal and ground vias varying from 300 to 700 um), b) square (side varying from 80 to 880 um).

4.2.2 Results and discussion

As is well known, when a signal travels along a structure, the electromagnetic field lines are spatially distributed in different ways so that the signal can be propagated, these configurations are the propagation modes. Unfortunately, not all the propagation modes that take place in an electrical channel are desirable, since some of these may take the signal away of its destination or may degrade the integrity of the signal in many other ways (e.g. originating signal distortion). For this reason, these modes are known as parasitic modes. One of the most common parasitic modes occurring in a package-like structure is the parallel-plate mode. In this case, the metal planes at different levels that serve as ground within a package can be seen as parallel-plate waveguides, which support the propagation of signals from DC to high frequencies. Analyzing the presence of this parasitic mode in electronic packages plays an important role in advanced PCB technologies since this mode is responsible for the resonances occurring in the structure at specific frequencies. In order to prevent and keep under control the propagation of this parasitic propagation mode, the adequate design of the ground vias is necessary to form an electric wall that confine the signal inside the structure.

Some of the studied configuration and corresponding Electric field distribution are shown in Fig. 4.15. In the Fig. 4.15 can be observed that the ground vias tend to block or to confine the radial propagation of Electric field inside the electric wall, meanwhile the number of ground vias is increasing the Electric field is confined to the area inside the ground vias. In the second case the center to center



a) b) c)

Figure 4.15 Electric field distribution with different number of ground vias a) One ground via, presented a resonance at 17.8 GHz, b) Two ground vias, presented a resonance at 27.8GHz. c) Four ground vias, presented a resonance at 35.6GHz.

distance between ground and signal vias varied from 300 to 700 um as despite Fig. 4.16, originating leakage of the Electric field that produces electromagnetic coupling between signal and ground vias modifying the distribution of Electric field.

Thus, the simulations carried out in the previous section point out the fact that there is a strong dependence between the frequency at which the resonance occurs and the location of the ground vias. Thus, this dependence is analyzed in this section to figure out the physical phenomena associated with the excitation of the parasitic propagation modes originating these resonances.

Intuitively it is easy to imagine that the larger the distance between ground vias, the larger the wavelength of the signal that may leak away from the electric wall, which implies that the resonance associated with the parasitic propagation mode will occur at lower frequencies. One way to avoid signal leakage is surrounding the signal via with more closely spaced ground vias or moving these vias closer to the signal via. However, Fig. 4.14 shows that a second resonance may appear in a vertical transition at higher frequencies which, in addition with the corresponding dependence with the configuration of the ground vias, also requires an explanation. Now the simulation results allow to observe the distribution of the electric and magnetic fields along the structure as the signal is propagated, see Fig. 4.15 and 4.16. Something to bear in mind is the fact that the parallel-plate mode presents an impedance Z_{pp} that presents a frequency dependent complex value. In addition, since the parallel-plates and vias form a resonator [3], that also affects the integrity of the transmitted signals. Thus, when Z_{pp} have the maximum value the transmission has the minimum, which is equivalent to the behavior of a notch-

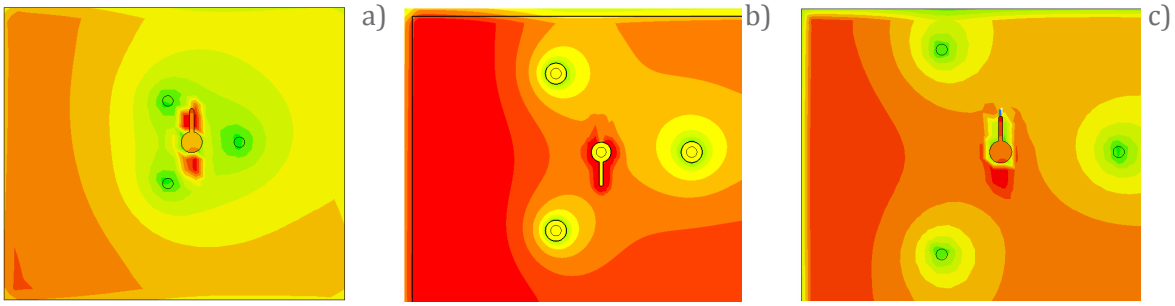


Figure 4.16 Electric field distribution on the structure with three ground vias, at frequency which resonance occurs: (a) triangle (center-to-center distance between the signal and ground vias equal to 300 um) at 29.9GHz, (b) triangle (center-to-center distance between the signal and ground vias equal to 566 um) at 34.8GHz. (c) triangle (center-to-center distance between the signal and ground vias equal to 700 um) at 35.3GHz.

filter (i.e. filter that passes all frequencies without changes, however attenuates those in a specific range). The relation between Z_{pp} and the signal transmission can be observed from the S-parameters through S_{21}. All the information about the port excitation and boundaries conditions (i.e. ground vias and structure edge) are contain in Z_{pp}. A very important parameter to Z_{pp} and for the propagation of parasitic modes is boundary condition, which are classified in three special cases [52]: 1) Perfect Electric Conductor (PEC), has shorted boundaries and finite plane size. 2) Perfect Magnetic Conductor (PMC), has open boundaries and finite plane size. 3) Perfect Mach Line (PML) considered infinite size of the planes.

Now we focus in the case of PCM, because that is the way the studied structure end, originating changes in the phase of the electric field and causes resonances. A way to modify the boundary condition and improve the transmission in the structures is to place ground vias, however to introduce the ground vias originated a mix of PEC and PMC that makes very difficult the determination of Z_{pp} since the new established conditions by the boundaries. Now include the problem of the geometry of the vias, reason why determinate Z_{pp} is very difficult. There are proposed analytical [52] and semi-analytical [64] ways to model packages with vias, but this not the case we just try to show how change boundaries condition modified Z_{pp} and at the same time the signal transmission. Place ground vias to form an electric wall is approximates to shorted boundaries, this improves the transmission thanks to the signal is confined inside the electric wall avoiding the signal to escape, and propagate as a parasitic mode. The transmission on the signal via is similar to the Radial Transmission Line (RTL) [52] that depends on radio as well the signal via does. This dependence can be appreciated with the results from the second part of the simulations, as well the difference between the fields configuration, see Fig. 4.16, in the cases of place the ground vias close to the signal pad o far away. This changes cause that the fields keep inside when the ground vias are close to the signal pad, but when the ground vias are far from the signal pad the fields can be found outside of the electric wall, hence the fact that change the resonance frequency behavior. Thus, we can explain the results simulations, by two facts:

a. The electric wall formed by the ground vias, change the boundaries condition, so Z_{pp} is modified.
b. The distance between the ground vias and signal vias originate different field configurations. That changes the resonance frequency, because one is relating to the electric wall (close) and the other one to the structure edges (far).

4.3 Conclusion

Thus, to intend model the transmission in a structure like the one studied here, it necessary to understand how the signal is related to each part of the structure and how it affects the impedance Z_{pp}, a way to do it is separate the transmission by sections:

1) Transmission on the microstrip line and strip line (in our case), where were defined the excitation ports.
2) Trans-mission related to the signal via and boundaries condition (structure edges and ground vias).
3) Interaction between ground vias, because there will be coupling and field reflections between them.

Once done, is possible to star to develop a transmission model with the information provided by Z_{pp}. That is why try to determinate the impedance Z_{pp} is a procedure that requires deep knowledge about electromagnetic theory and signal integrity theory, we just focus on the changes in the transmission through the S-parameters while the boundary condition was changed, by the ground vias and boundary definition on full-wave simulator.

After the physical origin of Z_{pp} is well understood, the problem will be solve, and could improve the transmission in the structure with just change the boundary condition, with placing ground vias in the right places. Other thing that helps to avoid the excitation of parasitic mode is the symmetry, while more symmetry has the structure relating to boundaries and excitations Z_{pp} presents more linear behavior. Also, placed four or more ground vias surrounding the signal via, helps to a better confined to the signal inside the electric wall. That reason why an ideal case is a cylinder, which in this case no resonance is presence, because has shorted boundaries and good symmetry, so the impedance Z_{pp} is well behave.

Chapter 5
Conclusion

An exhaustive analysis to identify the impact of high-order effects on the propagation of high-frequency signals on PCB was carried out in this thesis. This analysis includes the study of several interconnection structures using two different approaches: experimental-based, and through full-wave simulations. Some important conclusions and observations resulting of the performed analysis are presented in this final chapter.

5.1 Impact of High-Order Effects

Several high-order effects were identified throughout this thesis. It was found that a bad design of the adapters required to probe interconnection channels may introduce the undesirable effects associated with parasitic mode propagation of signals. In this case, multi-mode signal propagation occurs, which impedes using conventional calibration and deembedding procedures to determine the S-parameters associated with every section of the channel, which even difficulties the processing of data associated with simple homogeneous transmission lines. Hence, proper design of the prototypes taking special care in the adapters required to carry out high-frequency measurements plays an important role when characterizing any high-speed interconnect.

Another important studied effect is that associated with resonances within an interconnection. This effect makes a simple interconnect to behave as a reflective element, impeding the signal propagation at certain frequency points. For this reason, this effect makes useless an interconnect. Fortunately, this effect is commonly associated only with a small section of the channel, and can be corrected by identifying and optimizing the electrical transition at which the resonance is occurring.

Perhaps the most important topic studied in this thesis was that associated with the parasitic mode propagation of signals in packages. This is one of the most important areas studied for signal integrity engineers these days due to the importance of packages in today's electronics industry. It was found that alternative test-vehicles such as synthetic rectangular waveguides can be used to analyze the principle of operation of complex structures such as packages. This gave important highlights about the impact of a proper selection of dimensions, materials and structures for avoiding undesirable propagation in packages.

5.2 Measurement-Based Analysis

Access to experimental data plays important role in practical analysis of interconnects. For this reason, high-frequency S-parameter measurements should be taken with great care for guaranteeing accuracy and precision so that the data is meaningful. In this regard, the process of measurement starts with a proper design of prototypes including the additional structures that will be required for calibration and deembedding processes. In fact, also the selection of a proper calibration for specific structures and frequency ranges should be considered before starting with the measurements. For the frequency ranges used within this paper, it was observed that LRM procedures is better that SOLT due to the fact that LRM is not very sensitive to the accurate definition of the calibration structures. In fact, physically expected experimental data were obtained in this thesis up to 110 GHz.

The main advantage of using measurements is the fact that what is measured is what is actually happening. Unfortunately, not every structure can be directly measured and sometimes some sections composing a complex channel are not accessible for probing. In this case, deembedding procedures may be implementing. However, when the structures to be studied are relatively small when compared with the measured prototype the accuracy of the corresponding determined data becomes noisy and in some cases useless. In this case, it is important to have access to simulation software, as explained in the next section.

5.3 Simulation-Based Analysis

When measurements cannot be directly performed to a section of an interconnection channel or when additional effects (e.g. electromagnetic field distribution) are necessary for understanding the electrical behavior of a given structure, full-wave simulators represent a powerful tool. In this case, it is possible to observe in detail the interaction of a signal with structures even at the material level. Thus, a full-wave simulator requires a 3D model of the structure and divides the model in thousands or even millions of several segments for which the Maxwell Equations are solved assuming given boundary conditions. In this regard, in order for the simulation results to be meaningful, realistic and appropriate boundary conditions should be defined considering also simulation time.

An important point to be mentioned here is the fact that full-wave simulations are of great help when carried out systematically and with care. In order to do so it is necessary that the models are calibrated by correlating simulations with measurements and the interpolating and extrapolating the results. Furthermore, the simulations also have to take into consideration the variation of the physical parameters for specific ranges of frequency. For instance, the frequency dependence of the permittivity and the loss-tangent of the dielectric materials. In this case, using this type of tools leads to adequate and realistic conclusions about the behavior of a particular structure; otherwise, the results may either be misinterpreted of yield erroneous conclusions.

5.4 Challenges in Optimizing Interconnects

Several aspects were studied throughout this thesis and many effects occurring in practical links have been pointed out. The main challenge to be faced regarding this is the fact that the frequency of operation is continuously increasing as predicted by Moore's Law. Thus, the materials that have traditionally been used for implementing PCBs for high-speed applications are reaching the corresponding technological and physical limits. This is because the signals are not only relatively too slow but also effects that have previously been ignored are now taking considerably importance. Thus, new materials will have to be developed in order to rise the speed of the signals, for instance by reducing the relative permittivity of dielectrics and loss tangent. In addition, improved structures will have to be implemented, perhaps incorporating waveguides.

Regarding the sensibility to high-order effects, improved structures will have to be proposed to avoid as much as possible these effects. In the case of packages, where thousands of vertical transitions are required, an optimal design of the return path has to be carried out. This represents a huge challenge due to the complexity of these structures. For this reason, is it expected that studied regarding the distribution of the ground vias will result in many publications worldwide in the near future.

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