Analysis and Detection of Wear-Out Failures in Nanometer Technologies

By

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Summary

In this work an analysis and detection of wear-out failures in nanometer technologies has been presented. Wear-out failure mechanisms depends on stress conditions and workload during circuit operation.

Electromigration and self heating are the major interconnect wear-out failure mechanisms.

On the other hand, the probability of an open defect at vias and interconnects increases as technology scales. Weak resistive opens producing small delays are an issue in nanometer technologies. The number of vias, that is in order of billions, exceeds significantly the number of interconnects in a chip. Therefore resistive vias are the most common cause of test escapes in nanometer technologies causing reliability issues in circuits. Defective vias and interconnects are more prone to suffer electromigration which can lead to a chip failure.

Negative Bias Temperature Instability and Hot Carrier Injection (HCI) are the major sources of transistor aging causing a slow response of circuits. Transistor aging phenomena is also considered a reliability issue according to International Technology Roadmap for Semiconductors.

On-line testing techniques are employed to detect wear-out failures in order to improve reliability. The testing is done by collecting information, during normal operation, about the evolution of some system parameters, for instance, circuit delay, over time and hence be able to determine when the system fails the design specifications. The collection of a parameter information could be done by on-line

sensors.

In the first chapter, the evolution of MOSFETs transistors and interconnects as technology scales are presented. An analysis of the impact of technology scaling on reliability is also done. The more important wear-out failure mechanisms are explained. Interconnect open defects on nanometer technologies are described. Moreover, the state of the art of on-line techniques to detect wear-out failures are presented.

In the second chapter, wear-out on signal interconnects due to manufacturing defects is performed. Electromigration physics is described. Defective vias located in signal paths and conducting paths have been considered for the analysis. Electrical characterization and reliability evaluation for resistive vias have been done. The metric used for reliability evaluation is the Mean Time to Failure of the via as function of voiding due to defect. The reliability analysis is extended to redundant via insertion techniques.

In the third chapter, a system to detect wear-out failures due to resistive defects at vias/interconnects has been proposed. A Negative Skew Sensor and a Positive Skew Sensor have been proposed based on the addition of complementary signals and in the electrical behavior of resistive interconnects at the node before and after the defect. The two-sensor-system is in order to differentiate small delays due to process variations.

In the fourth chapter, transistor aging due to NBTI and HCI is described. A built-in aging sensor is presented. The monitoring strategy consists on verify the delay generated due to aging in a combinational circuit. The proposed built-in aging sensor is inserted in parallel to the flip-flop connected to the output of a combinational circuit in order to detects a signal transition during a guardband interval. This situation occurs when there is a significant delay at combinational circuit due to aging aging. Nevertheless, the flip-flop will still continue to capture the correct logic value from the combinational logic. Considering this, the

detection strategy can be considered a circuit failure prediction technique.

Finally, in the fifth chapter the conclusions are given.

Resumen

En este trabajo se realiza el análisis y la detección de fallas debidas a degaste en tecnologías nanométricas. Las fallas por desgaste dependen de las condiciones de estrés y carga de trabajo durante la operación del circuito. lectromigración y auto-calentamiento son los mecanismos de falla de desgaste más importantes en interconexiones. Electromigración y auto-calentamiento son los mecanismos de falla de desgaste más importantes en interconexiones.

Por otro lado, la probabilidad de existencia de un defecto en vias e interconexiones aumenta a medida que la tecnología se escala. Defectos resistivos débiles producen pequeños retardos y son un gran problema en tecnologías nanométricas.

El número de vias (en el orden de los billones) excede considerablemente al número de interconexiones en un circuito integrado. Es por esta razón que un gran número de vias defectuosas escapan de las pruebas de test y constituyen serios problemas de confiabilidad en tecnologías actuales.

Vias con defecto, son más suceptibles de sufrir electromigración, lo cual puede llevar a una falla total del circuito.

Negative Bias Temperature Instability y Hot Carrier Injection (*electrones calientes*) son as fuentes de envejecimiento más importantes en transistores PMOS. El fenómeno de envejecimiento es también considerado un serio problema de confiabilidad de acuerdo a la International Technology Roadmap for Semiconductors.

Técnicas de test on-line, son empleadas para detectar fallas debidas a desgastem, con el objetivo de mejorar la confiabilidad. El testing es realizado

recolectando información de manera periódica de algún parámetro del sistema en operación. Esto es para observar la evolución de dicho parámetro y ser capaz de determinar cuando el sistema falla. La recolección de información es mediante sensores.

De esta manera, la tesis está organizada como sigue: en el primer capítulo, se muestra el escalamiento de la tecnología en transistores e interconexiones y su impacto en la confiabilidad del circuito. Asimimo, se explica brevemente sobre las causes de defectos en interconexiones y sobre las fallas debidas a desgaste. Adems se presenta el estado del arte sobre técnicas que detectan fallas de desgaste.

En el segundo capítulo, se explica el degaste en interconexiones debido a defectos de manufactura. Se explica la física del mecanismo de electromigración. Se analiza la confiabilidad, en función del tiempo de via del dispositivo (MTF), en vias, considerando su ubicación: en camino de señal o en caminos unidireccionales. Además, se expande el análisis para las técnicas de vías redundates.

En el tercer capítulo, se presenta el sistema propuesto para la detección de fallas por desgaste en interconexiones. Se propone el uso de dos sensores: un sensor de skew positivo y un sensor de skew negativo. La detección está basada en la suma de señales complementarias. El estrategia de detección explota el comportamiento eléctrico de un defecto en la interconexión.

En el cuarto capítulo, se explican los mecanismos de envejecimiento en transistores y su impacto en el rendimiento de circuitos digitales. También se propone un sensor de envejecimiento. El sensor propuesto tiene la característica de ser predictivo.

Finalmente, en el quinto capítulo, se dan las conclusiones.

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.

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Preface

Spatial and automotive industries are considered long-term reliability applications. This is due to their circuits are intended to operate correctly for long periods of time, for example 10 years. Nevertheless, due to the workload and field stress conditions, circuits may wear-out. As a consequence, circuit lifetimes degrade until a catastrophic failure will occur.

The major wear-out failure mechanisms affecting circuit reliability are *Electromigration*, *Negative Bias Temperature Instability (NBTI)* and *Hot Carrier Injection (HCI)*. *Electromigration* is the transport of mass in metal lines under an applied current density. *NBTI* and *HCI* consist in the interaction between carriers from the channel of transistors with $Si-H$ bonds at the $Si-SiO_2$ interface, which lead to the formation of traps, which makes transistor threshold voltage decreases, degrading the circuit performance. These mechanisms, will be severer as technology scales.

On the other hand, interconnect or via weak open defects are also an issue in nanometer technologies. This is due to they escape from test and become a serious reliability concern. Defective interconnects or vias are more prone to suffer electromigration.

Therefore, in this work an analysis of wear-out failures is presented. Furthermore, periodic-monitoring systems are proposed in order to detect wear-out failures at interconnects and circuits.

Acronyms

CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SCE	Short Channel Effects
DIBL	Drain Induced Barrier Lowering
GIDL	Gate Induced Drain Leakage
SOI	Silicon On Insulator
FDSOI	Full Depleted Silicon On Insulator
DGMOSFET	Double Gate Metal Oxide Semiconductor Field Effect Transistor
BOX	Buried Oxide
***Fin*FET**	Fin Field Effect Transistor
VLSI	Very Large Scale Integration
ITRS	International Technology Roadmap for Semiconductors
CD	Critical Dimensions
NBTI	Negative Bias Temperature Instability
HCI	Hot Carrier Injection
TDDB	Time Dependent Dielectric Breakdown
EM	Electromigration
MTF	Mean Time to Failure
AR	Aspect Ratio

CMP	Chemical Mechanical Polishing
OPC	Optical Proximity Correction
SUT	Signal Under Test
Sref	Signal Reference
CASP	Concurrent Autonomous chip self test using Stored test Patterns
DFT	Design For Testability
BIST	Built In Self Test
NSS	Negative Skew Sensor
PSS	Positive Skew Sensor
CHE	Channel Hot Electron
DAHC	Drain Avalanche Hot Carrier
SGHE	Secondary Generated Hot Electron
GBG	Guard Band Generator
TSD	Transition Discriminator
GB	Guard Band
CUT	Circuit Under Test

Chapter 1

Introduction

1.1 Technology Scaling and Its Impact on Reliability

1.1.1 Device Scaling

Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry and has provided a path toward both denser and faster integration [1][2][3]. The transistors manufactured today are 20 times faster and occupy less than 1% of the area of those built 20 years ago [1].

The number of devices per chip and the system performance has been improving exponentially over the last two decades. But the power density, total circuits per chip, and the total chip power consumption has been increasing. The need for more performance and integration has accelerated the scaling trends in almost every device parameter, such as lithography, effective channel length, gate dielectric thickness, supply voltage, device leakage and so forth. Some of these parameters are approaching fundamental limits, and alternatives to the existing material and structures may need to be identified in order to continue scaling [1].

In 1965, Gordon Moore of Intel observed that the number of transistors in an

IC grew at an exponential rate over time [4]. His law states that the number of transistors on a semiconductor device will double every 18 months. He expected this growth rate to continue into the future and history has proven him to be correct. Even today, the growth rate of transistors in future devices is expected to continue following Moore's Law [5]. Figure 1.1 shows the Moore's Law reflected by the number of transistors used in Intel MPUs.

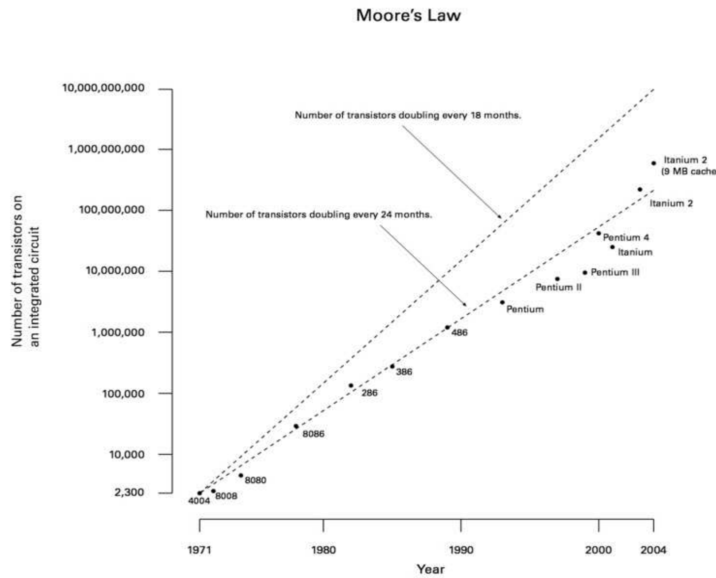


Figure 1.1: Moore Law in Intel MPUs.

One commonly used set of transistor scaling rules is that for constant electric field scaling proposed by [6]. The principle of this rule is that device voltages and dimensions are scaled by the same factor (k) such that the electric field (ε) remains constant. Figure 1.2 illustrates the MOSFETs scaling for constant electric field.

The dimensions of L, W, t_{ox}, x_j and the voltage supply, V_{DD} are reduced k times.

This methodology has been working well for years. However, the scaling of transistor parameters is more difficult for nanometer technologies. Non ideal

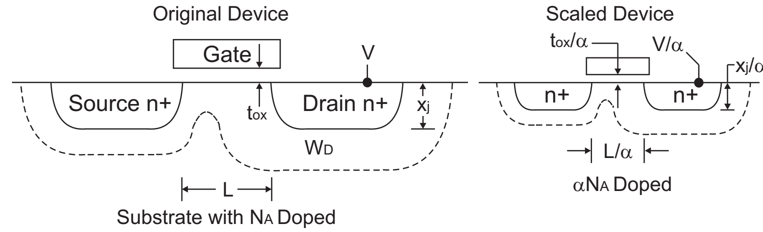


Figure 1.2: MOSFET scaling for constant electric field.

effects start to become non-negligible for these technologies. These effects are called Short-Channel Effects (SCE). SCE translates into reduction of transistor threshold voltage. Short-channel devices needs less voltage at the gate to generate the same channel depletion charge. This is due to that fact that a part of the channel depletion charge is generated by voltage (electric field lines) at the drain and source.

The most important SCEs in nanometer technologies are [7]:

- Drain Induced Barrier Lowering (DIBL): A potential barrier exists between the source and the channel region in the weak inversion regime whose height is a result of the balance between drift and diffusion current. The height of this barrier should be controlled only by the gate voltage to maximize transconductance. DIBL occurs when the barrier height for channel carriers at the edge of the source reduces due to the influence of drain electric field, resulting from the application of a high drain voltage and the proximity of this terminal to the source (See Figure 1.3). This increases the number of carriers injected into the channel from the source contributing to an increased drain off-state current. If this happens, then the drain current is not uniquely controlled by the gate voltage, but also by the drain potential. DIBL causes a threshold voltage reduction depending on the drain voltage.

- Leakage Currents: Leakage currents are dependent on threshold voltage. Figure 1.4 [8] shows the leakage mechanisms on nanoscale transistors. I1 is

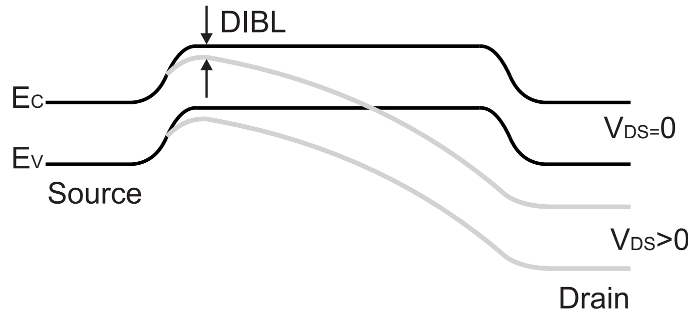


Figure 1.3: DIBL Effect.

the sub-threshold current. It generates when gate voltage is below V_{TH}. I1 increases due to DIBL. Drain and source formed PN union (diode) with bulk inverted-polarized. I2 is the leakage current due to inverted-current of PN union. It is produced by tunneling. I3 is the Gate Induced Drain Leakage (GIDL). It originates in the region of the drain that is overlapped by the gate. It is due to high drain voltage when gate is grounded (NMOS). In this region PN union is inverted polarized. Carriers introduce to substrate by tunneling. I4 is the gate leakage. It originates due to high electric fields in thinner gate oxides by tunneling.

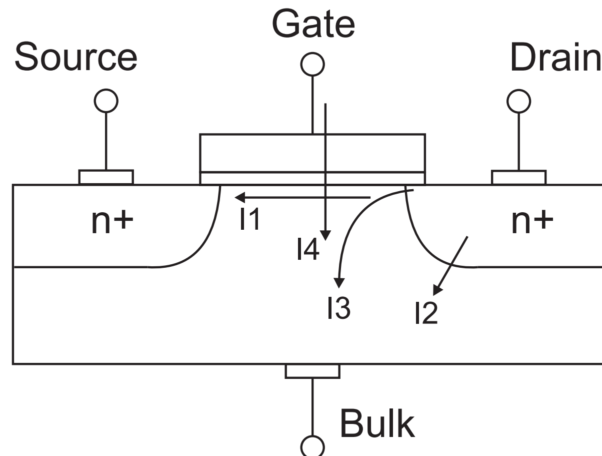


Figure 1.4: Leakage current mechanisms.

In order to reduce the issue of tunneling currents in the gate of scaled-devices,

High-K dielectrics (high dielectric constant) are introduced. High-K dielectrics generates a high capacitance between gate and the channel even when their thickness is bigger than SiO_2 dielectric. The bigger thickness of high-K dielectrics minimizes tunneling current [9]. Nevertheless, carriers mobility degrades if poly-Si gate is used together with high-K dielectrics [10]. The use of metal gates improve this issue [11]. Currently, Intel reported the fabrication of processors: Core2Duo, Core2Quad and Xeon based on metal gates and high-k technologies with 45nm process [12].

New devices have been studying to improve SCE of CMOS devices. The use of Fully Depleted Silicon On Insulator (FDSOI) and Double Gate MOSFET (DGMOSFET) devices has been considered. In FDSOI devices, drain/source electric field lines propagate to buried oxide (BOX) before to reach the channel, reducing SCE effects. DGMOSFETs have an electrostatic control over inversion channel, reducing SCE. One DGMOSFET devices is the FinFet.

1.1.2 Interconnect Scaling

As VLSI technology scales, interconnects are becoming the dominant factor determining system performance and power dissipation [13][14][15].

The ever increasing demand for speed and functionality of Si-based VLSI system has caused an aggressive scaling of devices.

This trend has lead to a dramatic reduction of interconnect pitch, an increase in the number of interconnect metal levels.

Figure 1.5 shows the number of metal levels and interconnect pitch trends. The number of metal level increase from 6 metal levels at 180nm node to 13 metal levels at 16nm node [16]. On the other hand, the interconnect pitch decreases as technology scales.

Since the number of interconnect levels increases, the number of contacts and vias increases even further. In nanometer technologies the number of con-

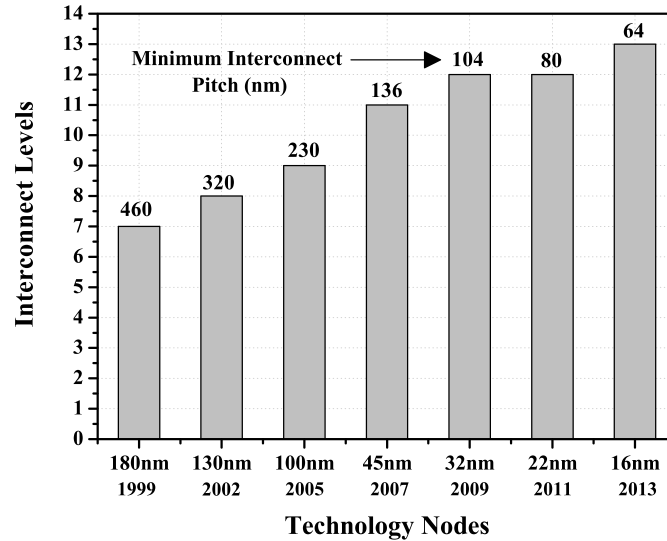


Figure 1.5: Increasing of interconnect metal levels and reduction of interconnect pitch as technology scales.

tacts/vias are in the order of billions. Figure 1.6 shows an estimated maximum number of vias per square centimeter per layer for various ITRS technology nodes [18].

Furthermore the critical dimensions of contact/vias are also decreasing [13][16]. Figure 1.7 shows this trend for different technology nodes [13].

A consequence of reduction of interconnect dimensions, current density increases as technology scales. Figure 1.8 shows current density trend for different technology nodes [16]. Nevertheless, due to the cross sectional area of contact and vias are smaller than interconnects, their current density increases as much faster rate than that for interconnects as technology scales [19].

In addition, in order to improve performance and speed specifications in nanometer technologies, Low-K dielectrics with small dielectric constants has been used instead of SiO_2 dielectric. Since neighboring interconnects have gotten closer as technology scales, SiO_2 dielectrics are thinned to the point where

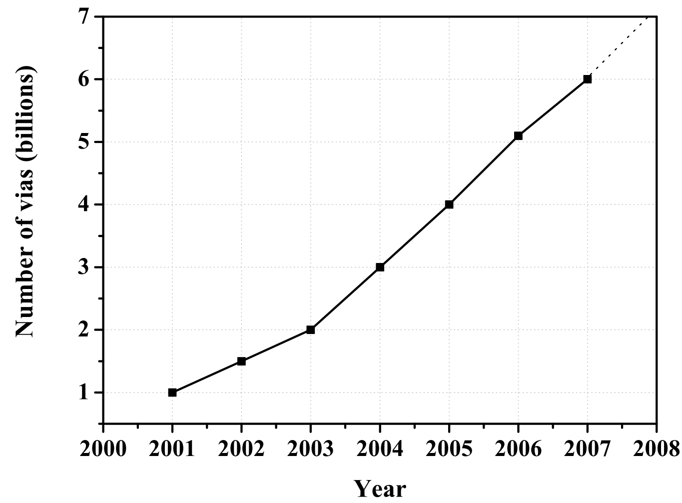


Figure 1.6: Estimated maximum via per square centimeter [18].

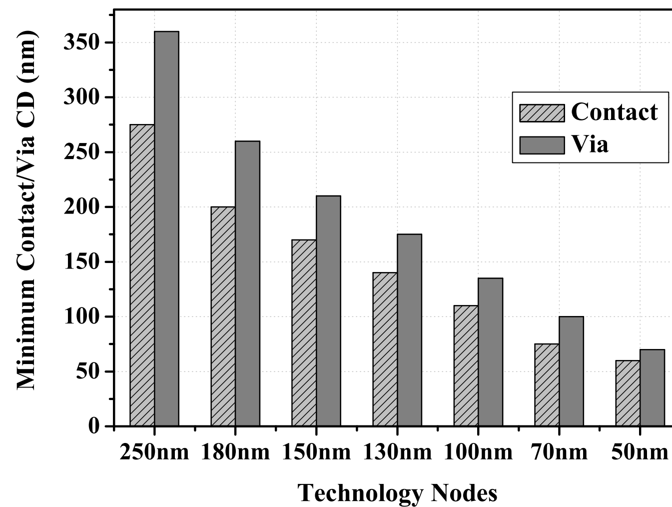


Figure 1.7: Critical Dimensions (CD) of vias for different technology nodes [13].

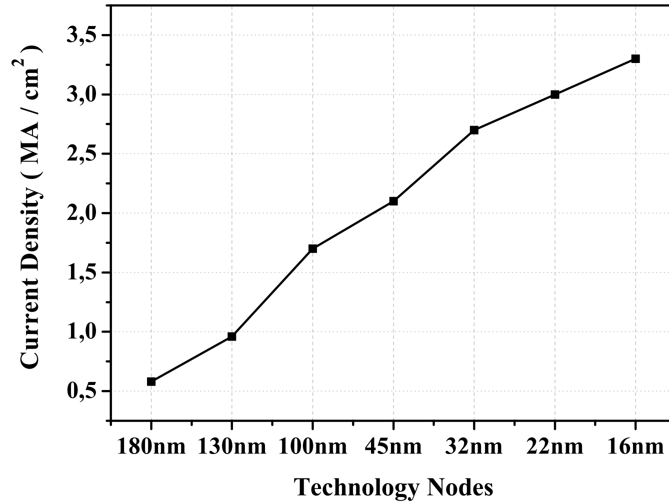


Figure 1.8: Current Density trend as technology scales.

charge build up and crosstalk (coupling capacitance) degrading the performance of the device. Therefore, Low-K dielectrics are intended to be used for reducing coupling capacitances between neighboring conductors which reduces crosstalk and enabling speed performance. Nevertheless, Low-K dielectrics has lower thermal conductivity. Figure 1.9 shows thermal conductivity and dielectric constants (K) of some insulating materials used in high performance circuits [13][20].

In spite of speed performance and functionality obtained, reliability is compromised due to scaling. The impact of scaling on reliability is presented next.

1.1.3 Impact on Reliability

In semiconductor perspective, reliability is the ability of a device to perform its required functions under stated conditions for a specified period of time [21]. Reliability is an important part of semiconductor industry and should be improved with each scaled generation of technology in order to enhance yield.

A semiconductor device has failed when response parameters from the device can no longer perform its intended function. The failure may have been caused

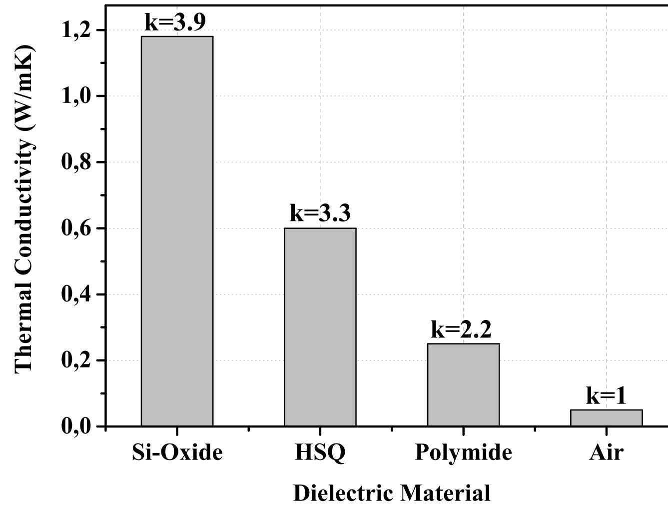


Figure 1.9: Thermal conductivity and dielectric constants of insulating materials.

by degradation of the device during operation in the field which translates into physical changes of the device over time that alter its response. Wear-out device occurs when degradation reaches the point where the device is considered to have failed [22].

Nevertheless, device failure may occur at any point of device's lifetime. The failure rate is represented by the "*Bathtub curve*" (See Figure 1.10). This is a hazard rate and is measured as the number of failures per unit time [22][23]. The *Bathtub curve* is widely used in reliability. The curve is divided into three phases:

- Early Failures phase or Infant Mortality: devices fail early due to manufacturing defects. Burn-in is often used to screen out devices which fail prematurely.

- Useful life phase: devices that survive to infant mortality phase. Devices enter a long period of relatively constant failure rate. Failure during this period are attributed to random failures resulting from random external events or early wear-out.

- Wear-out failures phase: Failures are as consequence of physical degradation of the device throughout its working life. They depend on the workload and stress operation conditions.

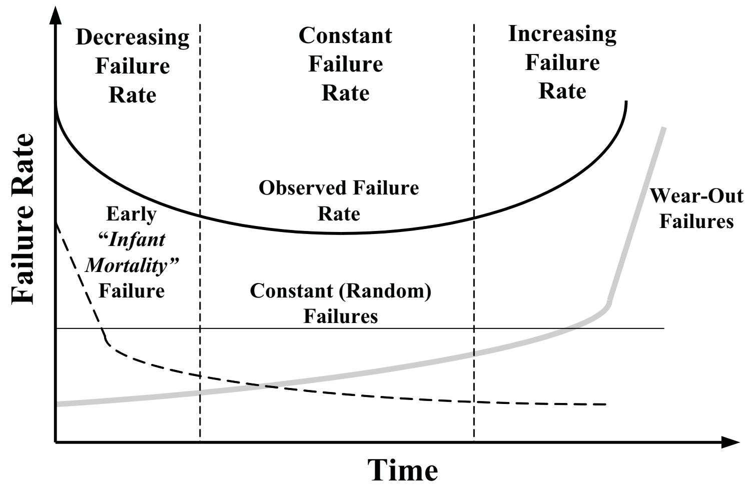


Figure 1.10: Bathtube Curve.

Current technologies reliability concerns include the following major wear-out failure mechanisms [24][25]:

- **Negative Bias Temperature Instability (NBTI)**: NBTI is a reliability issue of PMOS transistors under high temperatures conditions. Si-H bonds at the interface are broken and interface traps in the oxide are generated. NBTI manifest as an increase in the threshold voltage and consequent decrease in drain current and transconductance affecting circuit performance. The scaling of gate oxide enhances NBTI.

- **Hot Carrier Injection (HCI)**: HCI is one of the important degradation mechanism of MOSFET transistor that occurs when the transistor electric field at the drain-to-channel depletion region is too high given kinetic energy to free electrons. When the kinetic energy is high enough, impact ionization occurs at the channel, some carriers go into the substrate and other carriers

are injected into the gate oxide causing interface traps which lead to a threshold voltage shift and increment in gate current leakage. Similar to NBTI, HCI is enhanced as gate oxide scales.

- **Time Dependent Dielectric Breakdown (TDDB)**: TDDB is a failure mechanism in MOSFETs transistors when the gate oxide breaks down as a result of long time of moderate electric field at the gate. The breakdown is caused by formation of a conducting path through the gate oxide to substrate due to electron tunneling current at MOSFET operation.

- **Electromigration (EM)**: EM is the transport of mass in metal lines under an applied current density due to the momentum transfer between conducting electrons and diffusing metal atoms.

The aggressive scaling of oxide thickness without a corresponding reduction in the power supply voltage have increased oxide electric field significantly [26] which worsen NBTI reliability concern. Thus, a high oxide electric field is related with an increment in the number of charges at $Si - SiO_2$ interface generated by tunneling. This is due to the transmission co-efficient of the charges depends exponentially on the electric field [21]. The scaling of the gate oxide thickness also enhances the formation of the path between gate oxide and substrate due to defects at oxide layer, affecting TDDB reliability [20]. HCI reliability also decreases as transistor scales. Together with high oxide electric field and as well as channel length reduction and no significant reduction of voltage supply, HCI degradation increments [22]. EM reliability is also degraded for scaled technologies. The reduction of interconnect dimensions produces an increment of current density degrading its Mean Time to Failure (MTF). This issue is more significant for vias due to their critical dimensions. The tendency to use Low-K dielectrics instead of SiO_2 for reducing resistance-capacitance (RC) time delays, also compromised interconnects and vias reliability. This is due to the fact Low-K dielectrics have

lower thermal conductivity [13][20][17]. This issue enhances the impact of joule heating on MTF of interconnects.

The impact of technology scaling on wear-out failure mechanisms may cause failures during useful life phase of the *Bathtub curve* (See Figure 1.10). Figure 1.11 summarizes the failure rate trend as technology scales, where possible wear-out failures could occur earlier than expected.

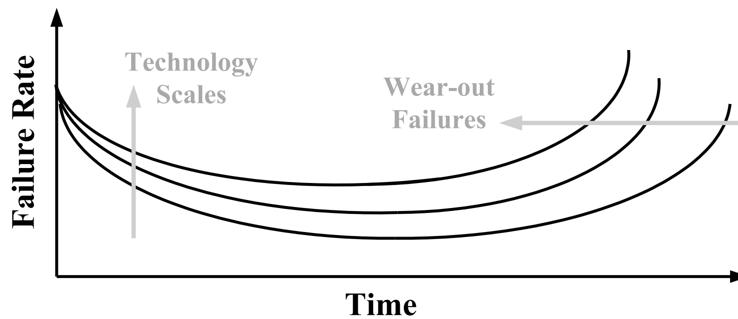


Figure 1.11: Bathtube Curve as technology scales [1].

1.2 Open Defects on Nanometer Technologies

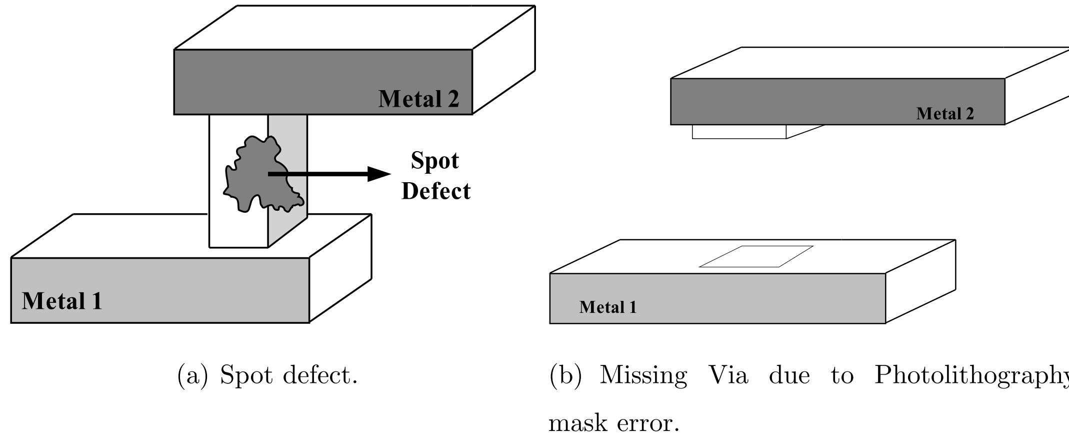
Interconnect based defects have become an important issue in nanometer technologies. An open may occur during several manufacturing process steps causing a discontinuity at any physical line that connects two nodes of the circuit that are connected in the original design [27] [28]. A full open in an interconnect or in a via occurs when the electrical connection between two nodes is completely eliminated. On the other hand, when the open defect does not completely eliminate the electrical connection between two nodes, the open defect is a weak resistive open defect. Resistive open defects have increased considerably in recent technologies, due to the presence of many interconnect layer and an ever growing number of contact/vias between each layer [29]. The number of vias could be in the order of billions (See Figure1.6) which has lead to an increase of their

probability of defect. Contacts/vias are a likely place for an open to occur [30]. Contact/vias have become an important yield detractor in modern technologies which have a high number of contact/vias due to the large number of metal levels [30] [31].

Opens can be caused by missing conducting material or extra insulating material. Among the open causes we can mention [7][30][32]:

- Undesired particles called spot defects may produce printing errors during the lithography process.
- Incomplete filled via
- Optical proximity effects which are a consequence of patterning features smaller that the wavelength of light
- Incomplete via etch or via foreign material
- Silicide agglomeration

The use of copper and damascene process has lead to think the way that metal defects are considered [32]. In opposition to the subtractive aluminum process, damascene process is an additive process. In damascene-copper process vias and metal are patterned and etched prior to the additive metalization. Because of this micromasking during the next lithography step can occur [33]. The open density in copper shows higher values than those found in aluminum [33]. Dishing, where overpolishing has occurred, and erosion, where insulator has been polished as well copper, can lead to opens. Scratches can also result in opens because the copper metal is soft and easily corroded [34]. In addition, voids are another important defect mechanism. The copper void defect mechanism shows dependence with temperature. Figure 1.12 illustrates some cases of interconnect resistive open defects.



(a) Spot defect.

(b) Missing Via due to Photolithography mask error.

Figure 1.12: Causes of opens in vias.

Weak resistive opens producing small delays are an issue in modern nanometer technologies. Small-delay defects are not properly covered by stuck-at and transition test sets [35]. Nigh et al. [36] have found that small delay defects due to resistive opens are an important group of defects that escape the tests. Furthermore, small delay defects can cause reliability issues in circuits [30][37][38][39].

For instance, random particles may narrow the area of a conductor. A narrowed conductor is more prone to suffer electromigration issues that can lead to a chip failure [40] [41].

1.3 Wear-Out Testing

High reliability is becoming a difficult challenge for nanometer technology devices [42][43][44].

Currently, the major reliability concerns are due to wear-out failure mechanisms, such as: Electromigration, NBTI and HCI. As mentioned before, these mechanisms dependent on workload and stress conditions during field operation. Moreover, they more prone due to the presence of defects that escape from wafer level testing.

This trend forces to adopt new test methods in order to improve reliability.

An alternative is periodic on-line testing techniques [43][44][45].

The principle of testing wear-out failures is to collect information, during normal system operation, about the evolution of some system parameters, specially delay, over time and hence be able to determine when system fails the design parameters.

Periodic on-line testing could be oriented to long-term reliability applications, such as automotive industry [46] or spatial applications [24].

Some on-line techniques to detect wear-out failures are presented.

In [45], FIRST (Fingerprints In Reliability and Self Test) has been proposed. It proposed at periodic testing (once daily) where the system is suspended and special test software runs to stress the system to detect the wear-out. It reduces the frequency of the processor. Signatures (fingerprint) of the system responses provide the detection of wear-out faults. It uses scan out chains.

Blome et al.[47] proposes an on-line circuit level wear-out detection unit. It monitors signal delay over time. The sampled delay values are used to calculate an exponential moving average (EMA) to predicts the system latency tendency. If the calculated delay exceeds a threshold value, it is due to a wear-out fault. Although, wear-out fault is detected, this technique has a high cost in area.

Razor technique, which is proposed in [48], is another technique to detect timing faults using double-sampled latches. When Razor detects a timing fault, the system is corrected in next clock cycle. The main disadvantage of Razor is that the system fails, while the objective to detect wear-out faults is prevent it.

Another alternative for on-line verification of wear-out failures, is the use of failure prediction built-in sensors [49]. In this case, interconnect wear-out sensors due to small defects and transistor aging sensors.

In [50][51][52], circuit-level sensors are proposed for monitoring electromigration at interconnects. They strategy consists on measure resistances changes at interconnects during lifetime operation. Despite the fact that electromigration

cause a resistance increment in interconnects for losing material (voiding), a significant shift interconnect resistance occurs when the interconnect is virtually broken.

Agarwall et al. [53] and Vazquez et al. [46], propose two aging sensors for digital circuits. They proposed an aging sensor located in parallel with the Flip Flop at the output of the combinational circuit. They define a guarband interval before the clock edge for which the flip flop capture the data from combinational circuit. Any transition of the combinational logic output inside the guardband corresponds to an exceed delay of the circuit due to aging. In [46] guardband is generated from a capacitor charge-current and in [53] guardband is generated from virtually AND function between clock signal and a delayed inverse clock signal.

Wear-out sensors must be OFF to prevent itself of wear-out. Therefore, they must not be turned on all the time. In this case, an on-line self test technique is needed to turn on sensors.

For example, for automotive application, each time that a car is turned on, the sensor could be activated by the on-line self test system for a period of time.

1.4 Justification of the Present Work

As technology scales, new issues affecting reliability and yield have appeared. In nanometer technologies, the probability of an open defect to occur in interconnects and vias is very high. Interconnects defects can produce small delays which may cause reliability issues due to electromigration. The reduction of transistors dimensions lead to the presence of high electric fields in the channel. This situation accelerates HCI and NBTI effects affecting circuit performance. Electromigration, HCI and NBTI are wear-out failure mechanisms that depend on workload and stress conditions.

Therefore, on-line wear-out built-in sensors for resistive interconnects and dig-

ital circuits are proposed. Reliability risk and transient behavior of weak resistive open defects at signal interconnects and vias have been taken into account. A negative and a positive skew sensor, located near the driver and the receiver respectively, are employed to detect small delays due to weak resistive defects at interconnects and vias considering process variations. Skew sensors have been implemented according to complementary signal addition. Finally, in order to monitor transistor aging in digital circuits due to NBTI and HCI, a sensor located in parallel with the flip flop at the output of a combinational circuit is proposed. Unlike [53] and [46], the guardband interval is an electrical signal. Delay shift due to threshold voltage degradation of PMOS transistors has been considered. Aging sensor detects any transitions at the output of a combinational logic within a guardband interval define for the clock signal before the edge triggered for which the flip flop captures the data of the combinational logic.

1.5 Organization of the Thesis

The remain of this work is organized as follows: The chapter 2 explains electromigration failure mechanism in interconnects due to manufacturing defects. Transient characterization of defective interconnects and vias is performed. Also, reliability risk of resistive interconnects and vias is evaluated. In chapter 3 a test strategy for wear-out interconnect monitoring is presented. A detection system with a negative and a positive skew sensors is proposed. Theory of complementary signal addition is considered for skew verification. Chapter 4 describes transistor aging mechanisms, HCI and NBTI, and their impact on circuits. Moreover, a built-in sensor for monitoring aging in digital circuits is proposed. Finally, in chapter 5 the conclusions of the present work are given.

Chapter 2

Wear-out on Vias and Interconnects due to Manufacturing Defects

Vias and interconnect structures in high speed circuits play an important role in nanometer CMOS technologies.

During manufacturing process of IC, e.g. the presence of spot defects induces extra and missing material on vias/interconnects causing circuit failures. When a spot defect induces missing material, vias/interconnect narrow without resulting in a complete open. This type of defect behaves as a weak resistive open defect. Weak resistive open defects may produce small delays difficult to detect. From the reliability point of view, weak resistive opens are potential hazards[28] because they can scape the logic testing stage. Furthermore, small delays due to resistive opens at vias/interconnects can cause reliability issues in circuits [37][54][30][38][39]. The Mean Time to Failure (MTF) of a defective via/interconnect is degraded due to Electromigration (EM) and Self Heating. Electromigration is widely regarded as a major wear-out or failure mechanism of VLSI interconnects[59]. EM is strongly influenced by defects, because they are

the site at which EM failures originate and accelerate EM damage[40]. Moreover, Self Heating in recent technologies can strongly impact the magnitude of the maximum temperature of the interconnect which will strongly affect the electromigration lifetime of vias and interconnects due to the exponential dependance of MTF on the inverse of the metal conductor temperature[59]. Since the number of vias exceeds enormously the number of interconnects in ICs and moreover their smaller dimensions, in this chapter an electrical characterization and reliability analysis for weak resistive defects in vias has been done. The results obtained are also available for interconnects. Electrical characterization has been performed using the interconnect HSpice model. MTF of vias has been used as a metric for reliability risk. The reliability analysis is also extended to redundant vias. The chapter is organized as follows: In section 2.1, physics of EM and self heating is explained. Section 2.2 explains the resistive via used for the analysis. In Section 2.3, vias located in signal paths are analyzed. Transient behavior of defective interconnects are performed. In the same way, reliability risk of the resistive vias is evaluated. Transient behavior and reliability risk of resistive vias located in conducting paths are presented in Section 2.4. While in Section 2.5 an analysis for redundant vias is done. The reliability risk of resistive vias for technology scaling is performed in Section 2.6. Finally, conclusions are given in Section 2.7.

2.1 Electromigration in Interconnect Integrated Circuits.

2.1.1 Electromigration and Joule Heating Problem

Electromigration is considered as the major interconnect wear-out failure mechanism in integrated circuits and has been the subject of intense study since its discovery threatened to stop integrated circuit industry [57].

Electromigration refers to mass transport in metal conductors under high stress conditions especially under high current densities and high temperatures (self heating). This causes open-circuit or short-circuit failures in VLSI interconnects. As current technologies scaling, the current density increases enormously [42]. Therefore, electromigration is a key problem for future interconnects.

When current flows through a metal line, thermal energy will be generated as a result of the collision between carriers and metal atoms. Such behavior is Joule Heating or Self Heating. If current is low, generated thermal energy will be dissipated immediately. However, at fairly high current densities, heating occurs and temperature gradients are found in integrated circuits[58]. Such temperature gradients cause significant metal atomic flux divergences and voids at metal line are produced. Hence, self heating always exists in electromigration mechanism and because of this, self heating is also a serious problem for current technologies.

2.1.2 Electromigration Physics

A metal crystal can be defined as an orderly array of an aggregate of metal ions which are held together by a binding force and opposed by a repulsive electrostatic force[55][77][70]. In a three dimensional array, each metal ion thermally vibrate within its potential well (atom) and exchange energy with the adjacent ions. At any given temperature, some of these ions may have sufficient energy to escape from the potential well that binds them in the lattice. When they reach the saddle point of the potential well, they are free of the lattice and become activated. The energy needed to achieve this state is known as the activation energy[70]. Since a metal line also contains a certain concentration of vacancies, these free ions can diffuse out of the lattice into adjacent vacancy. This process is called self diffusion. In absence of an electric current, the self diffusion process is isentropic[70], that means the probability for each nearest ion around the vacancy to exchange with the vacancy is equal. Under no concentration gradient, a random rearrangement

of individual ions takes place resulting in no mass transport[55][77][70].
When a current is applied, a metal ion is subjected to two forces, namely the frictional force and the electrostatic force. The frictional is due to the momentum exchange between the charge carriers (electrons) and the ions of the lattice. This force is in the direction of the electron flow and its magnitude is proportional to the current density. The electrostatic force is due to the interactions between the ion and the electric field and is in direction of that field. It is believed that because of shielding electrons[55][70], the frictional force is always greater than the electrostatic force. Figure 2.1 shows an ion under these two forces. Where the frictional force and electrostatic force are denoted by F_1 and F_2 respectively.

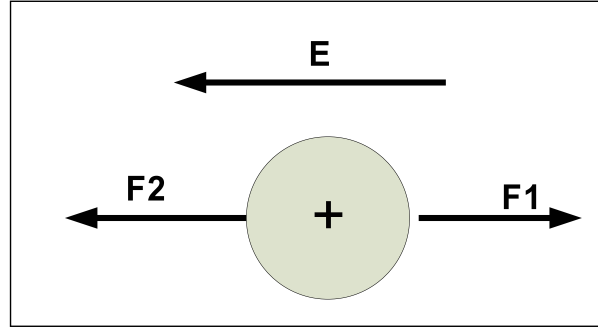


Figure 2.1: Metal Ion forces when a current is applied. F_1 is the frictional force and F_2 is the electrostatic force.

So, the total force over the ion, F, will be in the direction of F_1 and is given by,

$$F = F_1 - F_2 = (Z * e)E \tag{2.1}$$

Where the Z*e is the effective charge assigned to the migrated ion and E is the electric field.
Experimentally the force is not directly measurable but what may be observed is the ion flux or the effects of the ion flux produced by the force, such as the divergence of the ion flux. So, the ion flux due to the frictional force is given by,

$$\Psi_A = Nv \tag{2.2}$$

Where N is the density of atoms in the metal and v is the ion drift velocity. The drift velocity is related to the force by the Nernst-Einstein equation given by,

$$v = \mu F \tag{2.3}$$

Where μ is the mobility that is equal to

$$\mu = \frac{D}{fKT} \tag{2.4}$$

Where f is the correlation factor depending on lattice structure that in most cases is 1, K is the Boltzmanns constant, T is the temperature and D is the self diffusion coefficient and is given by,

$$D = D_0 exp(\frac{-E_a}{KT}) \tag{2.5}$$

Where E_a is the activation energy. Moreover, the electric field, E, is given by,

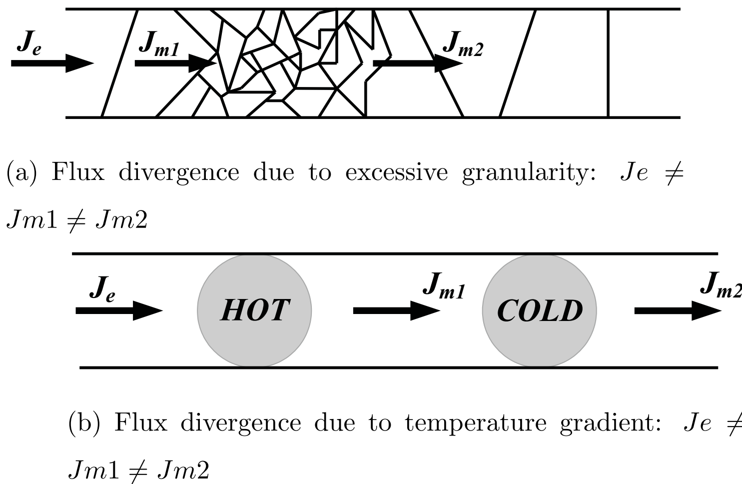
$$E = \rho J \tag{2.6}$$

Where ρ is the density of ions and J is the current density. Finally, utilizing the last equations, the ion flux is,

$$\Psi_A = (\frac{ND_0\rho J}{fKT}(Z * e) \times exp(\frac{-E_a}{KT}) \tag{2.7}$$

Metals need an imperfection or defect in the structure (lattice) that generates a divergence in the ion flux to begin the electromigration failure process[71]. According to Eq.2.7, a divergence of flux in more likely to occur under high current density conditions. If the divergence becomes significant, the original

isentropic self diffusion is perturbed and the ions moving along the current flow have a higher probability of exchanging positions with the vacancies. Hence, the original random process changes to a directional process. This directional effect causes ions to migrate or diffuse downstream in terms of electron wind direction and vacancies move upstream. The metal ions condense to form whiskers or hillocks whereas the vacancies condense to form voids. This process results in the change in the density of the metal ions with respect to time. Figure 2.2 shows two cases where flux divergence occurs[71]. One case is when exists a region in the metal line with too much granularity that provides many more paths to Al atoms to move in. The second case shows temperatures differences along the metal line. The hot region has a higher concentration of vacancies and Al atoms will diffuse more readily here than in the cold region.



(a) Flux divergence due to excessive granularity: $Je \neq Jm1 \neq Jm2$

(b) Flux divergence due to temperature gradient: $Je \neq Jm1 \neq Jm2$

Figure 2.2: Examples of flux divergences [71]

The formation of voids causes some of the metal lines to fail, forcing the current to go through the rest o the lines and resulting in an increase in the current density and joule heating. Joule heating can increase the local temperature and cause more lines to fail. Furthermore, as the hillocks forms, a concentration gradient is produced which may create a stress related force enhancing the mass transport process and causing more lines to fail. These processes continue as a

loop. This mechanism is shown in Figure 2.3.

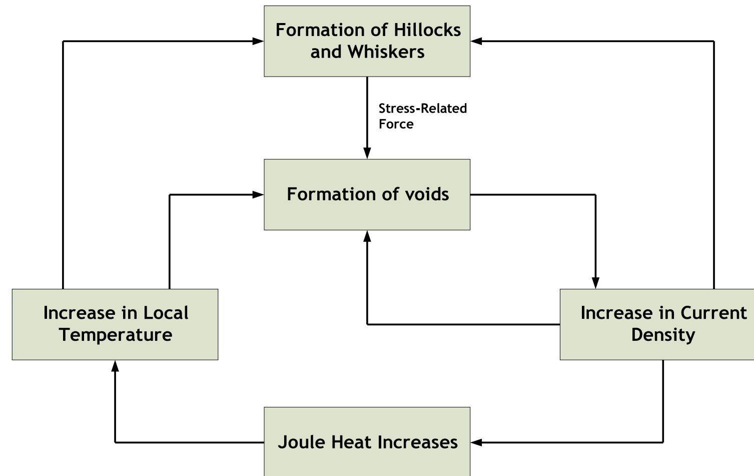


Figure 2.3: Loop mechanism of electromigration failure [70].

2.1.3 Black's Law

All interconnects are designed to guarantee a predefined Mean Time to Failure (MTF). Failure due to electromigration and self heating for an interconnect is usually expressed by empirical equation of Black, that is known as Black's Law[55], and is given by:

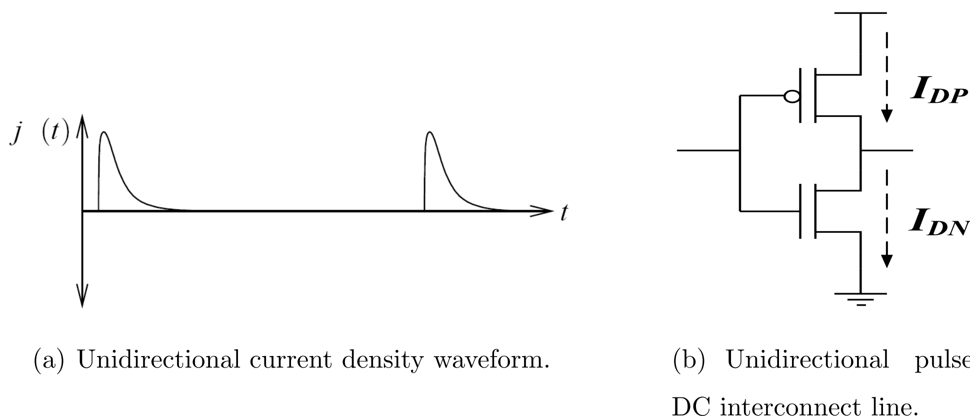
$$MTF = \frac{A_t exp(\frac{E_a}{K_B T_m})}{(J)^n} \tag{2.8}$$

Where A_t is a constant dependant of the interconnect's geometry, E_a is the metal's activation energy, K_B is the Boltzman's constant, T_m is the metal temperature due to self heating and J is current density of the interconnect line, n is a scaling factor between 1 and 2. According to [77], n is approximately 2. As is indicated in Eq.2.8, MTF is dependant on current density and metal temperature, therefore electromigration and self heating must be studied simultaneously because both limit current densities and interconnect lifetime[59].

As it will be shown in subsequent section, MTF is the metric for interconnect reliability evaluation.

2.1.4 Types of Electromigration according to current conditions

An interconnect line can drive three types of current waveforms[59][71][72][64]: Pure DC, unidirectional pulse currents with average DC value and bidirectional currents. Pure DC current do not appear in CMOS circuits that are fully static and fully complementary[71]. It is often in power grid interconnect lines(VDD, VSS). Unidirectional pulses have an average DC current that occurs in drain or source terminals. Positive current always enters the source of a PMOS transistor and exits the drain, whereas current always enters the drain of an NMOS transistor and exits the source. The transistor gate voltage turns source-drain current on and off. The average DC current is used as the stress parameter for electromigration. Figure 2.4 shows the waveform of the current density of a unidirectional pulse DC current. Figure 2.4 shows the case of unipolar current in an inverter, that could be a driver or load of an interconnect line.



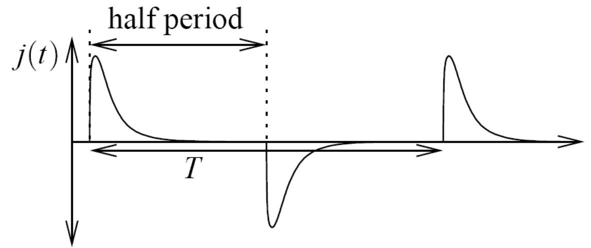
(a) Unidirectional current density waveform.

(b) Unidirectional pulse DC interconnect line.

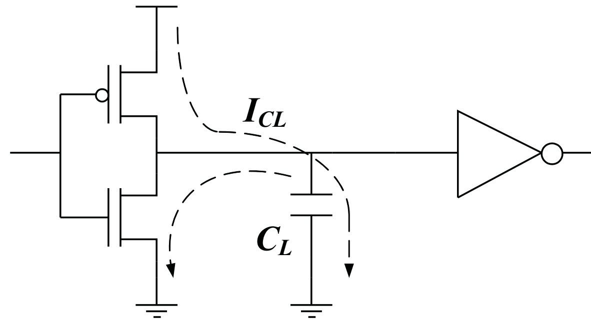
Figure 2.4: Unidirectional current conditions.

In interconnect signal lines current is bidirectional, positive and negative.

Currents enters the load gate interconnect, charging the capacitance during pull-up. The current reverses direction during pull-down. Figure 2.5 shows the current density waveform for a bidirectional current and the bipolar current in a signal line.



(a) Bidirectional current density waveform.



(b) Interconnect Signal Line

Figure 2.5: Bidirectional current conditions

According to current conditions, interconnect under pure DC current, MTF is considerably degraded if electromigration occurs. Then, for unidirectional pulsed-DC current, current density depends on duty cycle (r), an a average current density ($J_{average}$) is calculated. Hence, MTF for pulse DC conditions is greater than MTF for pure DC current conditions. Finally, for bidirectional current, average current density is supposed to be zero, that is no electromigration occurs. Nevertheless, healing property must be considered. It is the ability to recover in the negative cycle of current density of signal which was removed in the positive cycle. When healing is ideally perfect, effectively there is no electromigration. In accord with this, MTF under bidirectional (AC) conditions is greater than

pulse-DC conditions.

2.1.5 Effects of Open defects on interconnect Electromigration

During manufacturing process of IC, e.g. the presence of spot defects (such as dash particle) induces extra and missing material on interconnects and vias causing circuit failures. In this work, only the case for missing material is studied. When a spot defect induces missing material, interconnects or vias narrow without resulting in a complete open. This type of defect behaves as a weak resistive open defect. Figures 2.6 and 2.7 shows an interconnect and via, respectively, affected by a spot defect resulting in the formation of a narrow site.

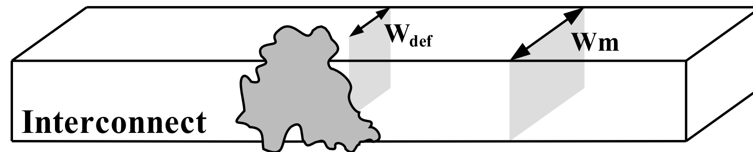


Figure 2.6: Defective interconnect due to a spot defect. There is narrow portion of interconnect (W_{def}). It makes high current densities.

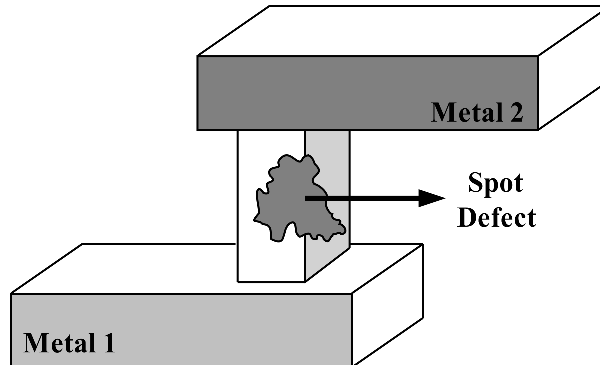


Figure 2.7: Defective via due to a spot defect. Via is narrowed. It makes high current densities.

These defective interconnects/vias represent a risk of chip failure in the field [73] because they are vulnerable to electromigration failure mechanism. Therefore the physical defects, in this case open defects, due to manufacture process variations are considered the site at which electromigration failures originate and accelerates electromigration damage[40].

This is the reason because a detailed transient analysis and reliability risk of weak resistive vias is performed in next sections.

2.2 Resistive Via Model

Vias located in signal paths connect two metal layers at different levels. The via is modeled as a cylinder (See Fig. 2.8) with a void size *1-X*. The distance X ($0 \leq X \leq 1$) represents the fractional increase in via voiding with respect to a good via (X=*0*). The modeled shrunken metal via has a diameter 1-X and represents the defect effective via diameter. For electrical simulations, the via is modeled as a variable temperature dependant resistor, R_{via} [60]. The resistance value of R_{via} is proportional to the void size (X).

Figure 2.8 shows the model of a via. D is the diameter of the via. The defective diameter as function of X void is shown. Also, the estimation of the via resistance is shown. The resistance value for a defect-free via is (where $D = 1$):

$$R_o = \frac{\rho_{Tvia}}{A_o}(h_{via}) \tag{2.9}$$

where A_o is the transversal area of the defect-free via (D=1), h_{via} is the via height and ρ_{Tvia} is metal resistivity that depends on the via temperature.

For a defective via, the transversal area decreases as the void size (X) increases. This modifies the via resistance and its dependence on the temperature. The via resistance for a given X value is given by:

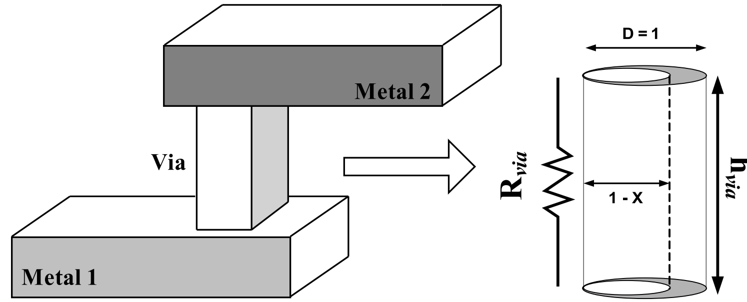


Figure 2.8: Model of a via used in the analysis. Diameter of a free-defect via is normalized to 1.

$$R_{via} = \frac{\rho_{Tm} h_{via}}{A_d} = \frac{\rho_{Tm} h_{via}}{\pi((1-X)D/2)^2} \tag{2.10}$$

2.3 Analysis for Vias Located in Signal Paths

The schematic diagram of the via interconnect system used to analyze the via behavior in signal paths is shown in Figure 2.9. The resistive via is modeled by a variable resistor.

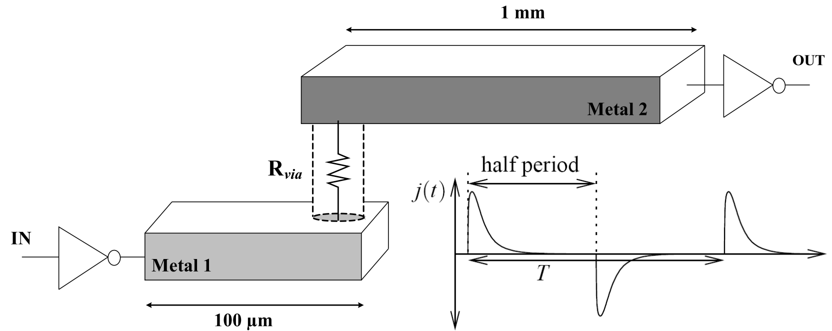


Figure 2.9: Schematic diagram of the system under analysis for a via in a signal path. Defective via is modeled as a variable resistor R_{via}.

The electrical simulations were done using HSpice with TSMC 0.18μm tecnology. The cascade buffer designed to driven the interconnect has a maximum beta of $\beta = 16/6$ with minimum channel length allowed by the technology. The

signal line width is 0.5μm. The current density per via is 0.2mA/via that is less than the maximum established by the technology design rule which is typically around 0.3mA/via. The interconnect line having the analyzed via is coupled at both sides by parallel lines. Parallel lines at both Metal 1 and Metal 2 (See Figure 2.9) are considered. Worst case signal coupling has been considered at the adjacent lines.

2.3.1 Transient Behavior

Figure 2.10 shows the behavior of the via resistance (R_{via}) as function of X void. The resistance value of the via does not increases significantly for a wide range of X void values. This resistance begins to increase significantly only when the X void is larger than 90%.

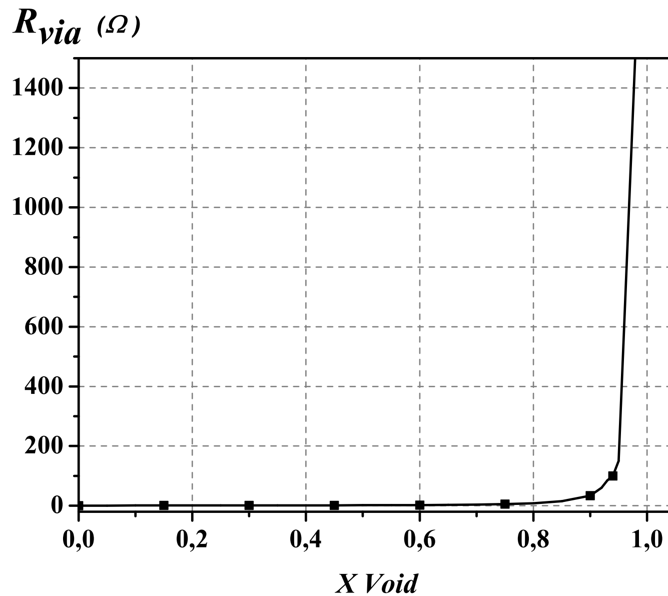


Figure 2.10: Resistance variation as a function of x void for bidirectional via

Figure 2.11 shows the electrical simulation results of the interconnect system. Input and output signals behavior are shown. It is observed despite of the X void

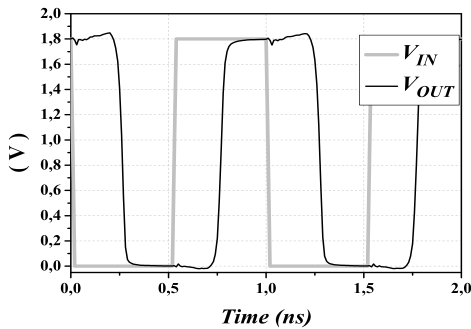
is 97%, the interconnect system gives the proper logic response. However, a delay with respect to the case with X void zero can be observed. For the simulated interconnect system, a logic error appears for X void of 99%(See Figure 2.11). Plotting the delay as function of X void (See Figure 2.12) allows a closer analysis. It can be observed that the delay begins to increase significantly when the defect represents more than 90% of the via. Small delays can be observed for X void less than 90%. Even more some of the delays for the X void larger than 90% may be considered small delays depending of the clock slack. Small delay defects are difficult to be detected for delay based test approaches [35]. These defects pose a reliability risk. Furthermore, in this work is shown that even X voids as low as 50% may also pose a reliability risk.

The results obtained until now, indicate that a more rigorous transient analysis must be done. Hence a behavior analysis of the signal through the interconnect, before and after the defect, is presented. For simplicity of explanation, let us consider the schematic diagram showed in Figure 2.13 to represent the system of Figure 2.9. R_{via} is the resistive open defect in the via, C_1 is the total coupling capacitance of the Metal 1 interconnect. C_2 is the total coupling capacitance of the Metal 2 interconnect. According to the simulated system (See Figure 2.9) since R_{via} is near the driver, $C_2 > C_1$. Let us define α as a proportional parameter used to model the coupling capacitances located before (αC=C_1) R_{via} and after R_{via}((1 − α)C=C_2). α serves to indicate the location of the resistive open defect.

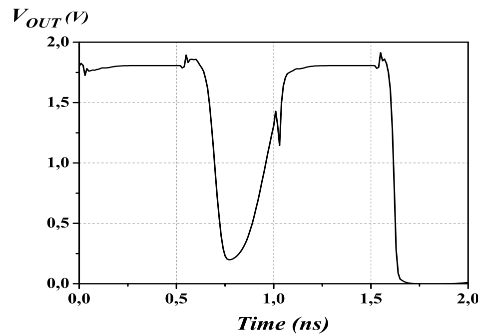
As R_{via} increases, the time of charge at nodes V_{before} and V_{after} are different. This is explained with the following simple relationships:

$$I_{R_{via}} = \frac{V_{before} - V_{after}}{R_{via}} \tag{2.11}$$

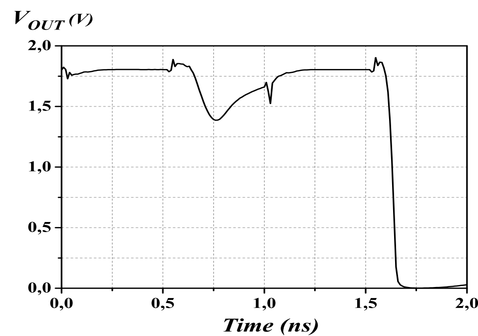
$$I_{Ron} = I_{\alpha C} + I_{R_{via}} \tag{2.12}$$



(a) Input Signal and system Output Signal. X Void=0



(b) System output signal. X Void = 97%.



(c) System output signal. X Void = 99%.

Figure 2.11: Output Signal of the system. It is observed the when X void is 99% the delay has a considerably increment in comparison to X=85%.

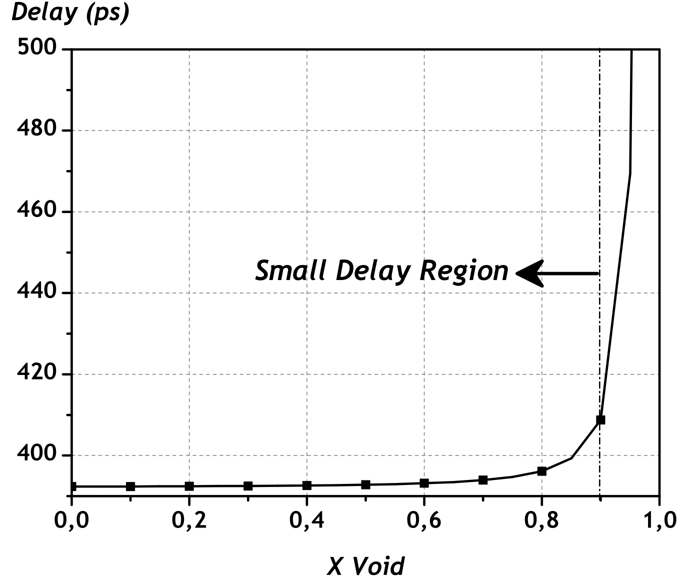


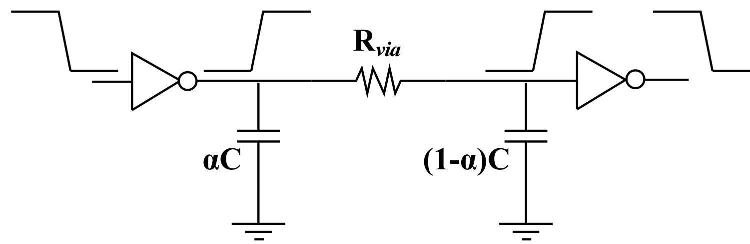
Figure 2.12: Behavior of the delay on via located in a signal path.

$$I_{\alpha C} = \alpha C \frac{\partial V_{before}}{\partial t} \tag{2.13}$$

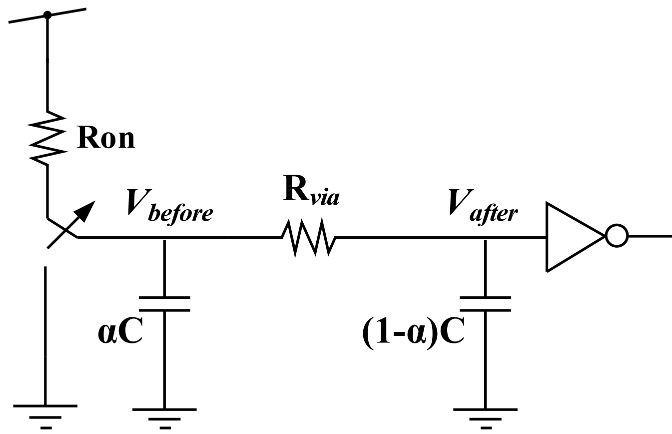
$$I_{(1-\alpha)C} = (1-\alpha) C \frac{\partial V_{after}}{\partial t} \tag{2.14}$$

From Eq.2.11, as R_{via} increases, $I_{R_{via}}$ decreases. I_{Ron} is the buffer current and is constant and according to Eq.2.12 if $I_{R_{via}}$ decreases due to R_{via}, $I_{\alpha C}$ increases in order to maintain the equality with I_{Ron}. As consequence of this and taken into account Eq.2.13, if $I_{\alpha C}$ increases, the time of charge at node V_{before} become faster. In the other hand, is obvious if $I_{R_{via}}$ decreases, $I_{(1-\alpha)C}$ also decreases and in accordance with Eq.2.14 the time of charge at node V_{after} become slower. On balance, the signal suffers a negative skew before the resistive open and suffers a positive skew after the resistive open. HSpice simulations validates these assumptions. Figure 2.14 shows this defective interconnect behavior.

Then, the delay shift increment as R_{via} increases is analyzed. The delay shift



(a)



(b)

Figure 2.13: Resistive Via model to transient analysis.

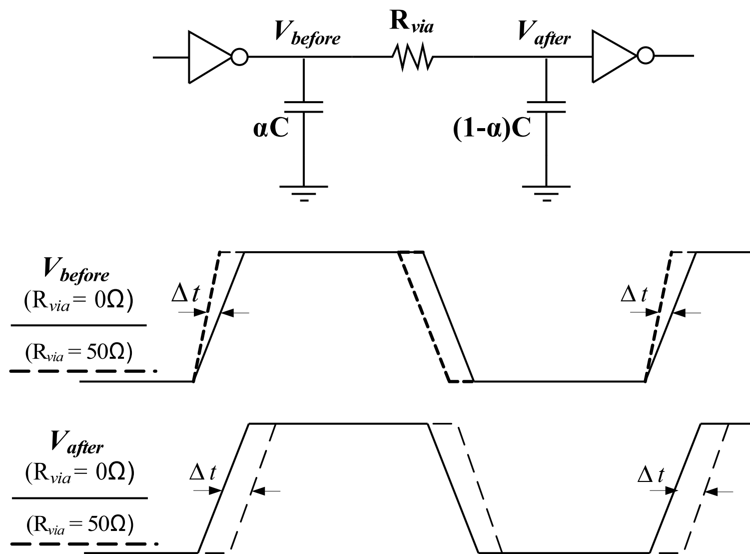


Figure 2.14: Behavior before and after resistive open defect.

is defined by,

$$\Delta t_{DS} = \frac{|td_{defect} - td_{free-defect}|}{td_{free-defect}} \tag{2.15}$$

Where $td_{free-defect}$ is the delay of the system for a free defect via and td_{defect} is the delay of the system for a defective via. It depends proportionally on the value of R_{via}.

Figure 2.15 shows the delay shift of a defective interconnect as a function of R_{via} at V_{before} and V_{after} nodes for different couplings conditions. It is observed that a greater delay shift variation is obtained when double coupling conditions exists.

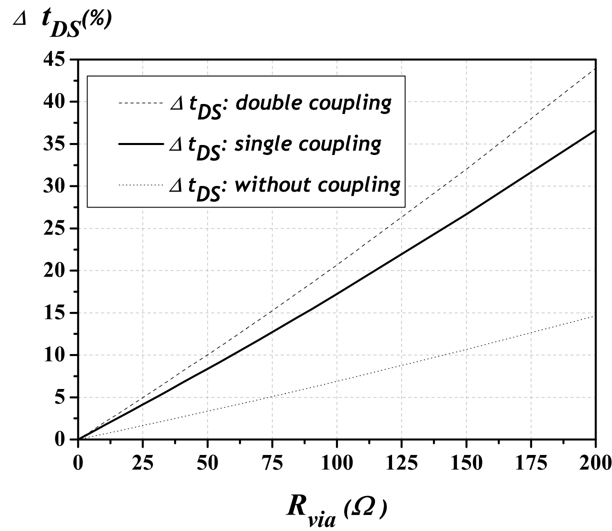
Figure 2.16 shows a comparison of delay shift of a defective interconnect at V_{before} and V_{after} nodes against R_{via} for double coupling conditions. It is observed that a greater delay shift variation is obtained at V_{before} node. This result will be taken into account to establish the test strategy proposed in this work.

It is observed for a range of R_{via} between 0Ω and 200Ω (weak resistive open defect region) that delay shift before the defect is slightly greater than delay shift after the defect. This means the node before the resistive open is more sensitive to delay shift (negative skew) making easy small delays detection. This is the test strategy principle which will be performed in next chapter.

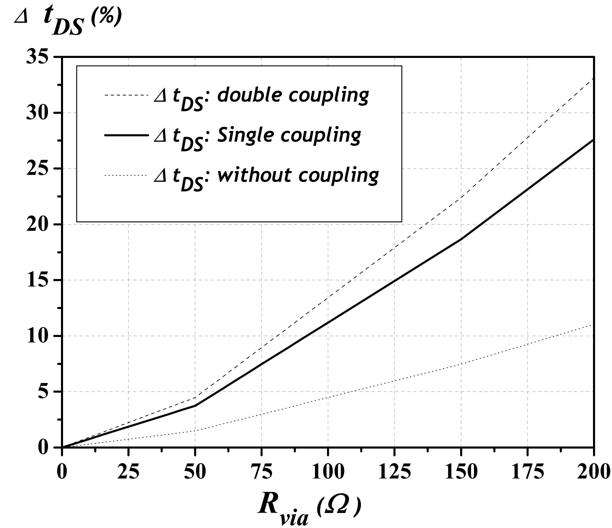
2.3.2 Reliability Risk for Vias Located in Signal Paths

As via voiding increases, via resistance and current density increase due to the shrunken of the effective volume of the via. They affect the electromigration risk. We will evaluate the reliability risk of vias against the fraction of via voiding. This analysis is particularly relevant to resistive via caused by small delay defects. Campbell et al reported a resistive contact that evolved to a clean open circuit while undergoing analysis in the failure analysis lab [78].

Lifetime reliability of metal interconnects is modeled by Black's equation [77]:



(a) Delay shift for different coupling conditions at V_{before}



(b) Delay shift for different coupling conditions at V_{after}

Figure 2.15: Interconnect resistive open defect model to transient analysis.

$$MTF = \frac{A_t exp(\frac{E_a}{K_B T_m})}{(J)^2} \tag{2.16}$$

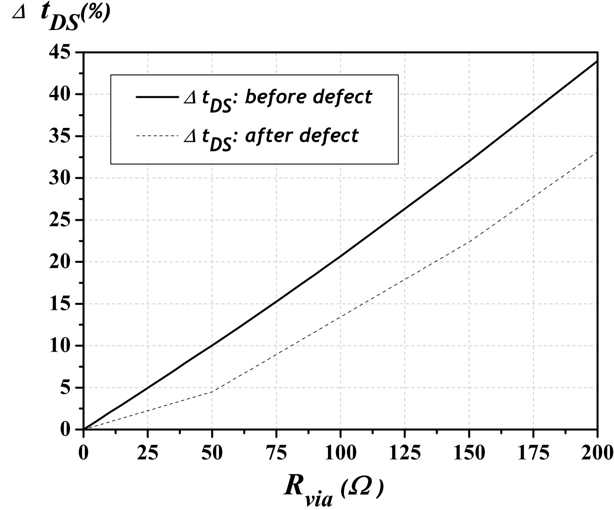


Figure 2.16: Delay shift comparison between the node before defect and the node after defect.

where A_t is a constant dependant on the interconnect's geometry, E_a is the metal's activation energy, K_B is the Boltzman's constant, T_m is the metal temperature due to self heating and J is the current density of the interconnect line.

Traditionally, EM and self heating are not simultaneously considered for generating EM lifetime for interconnects. Nevertheless, both EM and Self heating are two temperature dependent mechanisms that limit the current densities and lifetime of interconnects [59][13]. Therefore, the Mean Time to Failure for resistive vias will be evaluated considering simultaneously EM and Self heating [59][62].

Vias located in signal paths present bidirectional currents (See Figure 2.9). Electromigration is also an important issue for these vias [59] [65]. Conductors under bidirectional currents present the healing property. The healing property means the ability to recover material in the negative cycle of the current density signal which was removed in the positive cycle. Hence, the average current density for bidirectional vias (J_{bid}) is given by,

$$J_{bid} = \frac{1}{T}\left(\int_0^T |J_+|dt - R\int_0^T |J_-|dt\right) = J_{av+} - RJ_{av-} \tag{2.17}$$

Let us assume that the average current density in the positive and negative cycle are equal ($|J_{av+}| = |J_{av-}|$). Then, J_{bid} will be,

$$J_{bid} = (1 - R)J_{av+} \tag{2.18}$$

Hence, the equation 2.16 is modified to [59],

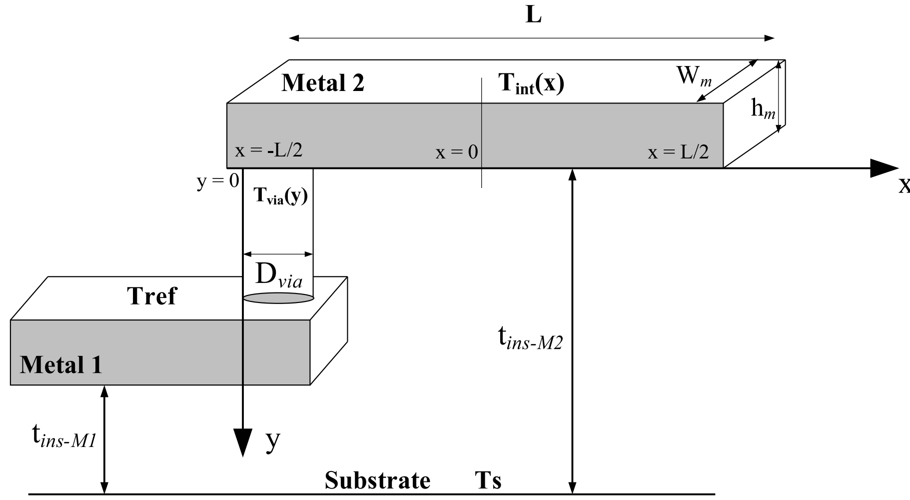
$$MTF_{bid} = \frac{A_t exp(\frac{E_a}{K_B T_{via}})}{(J_{bid})^2} \tag{2.19}$$

where R is the healing factor with $0 < R < 1$. We use R=0.5 [59].

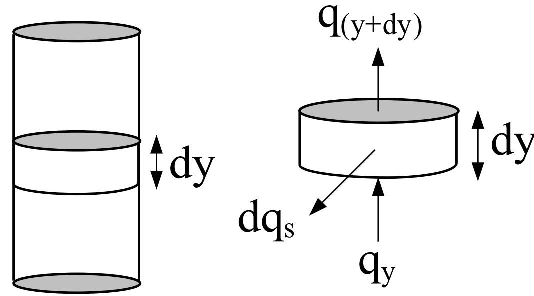
The via temperature T_{via} is equal to the reference temperature (T_{ref}) plus the temperature increase due to self heating (ΔT). In this case T_{ref} is fixed to the temperature of M1 interconnect (See Figure 2.17), and is 100.05^oC . In order to determine T_{via}, the model presented in [81] is used. Figure 2.17a shows the system used for thermal analysis. Via is modeled as a cylinder. Where W_m is the interconnect width, h_m is the interconnect height, h_v is the via height and D is the via diameter. A differential portion of a via, defined as control volume, is showed in 2.17b illustrating the energy balance inside the via. The conservation of energy [81][84] requires that the net heat flow into the control volume ($q_y - q_{y+dy}$) plus the volumetric rate of the thermal energy generation ($q^{'''}$) must equal the rate of energy transfer out of the control volume (dq_s).

The heat conduction within the M2 interconnect and the via is assumed to be one dimensional in the x and y directions respectively. According to [81][84], the energy balance equations for the interconnect and the via are given by,

$$\frac{d^2\theta_m(x)}{dx^2} - m_m^2\theta_m(x) = -\frac{q_m^{'''}}{k_m} \tag{2.20}$$



(a) System Model to thermal analysis.



(b) Energy balance of within the via/interconnect

Figure 2.17: System Model to thermal analysis.

$$\frac{d^2\theta_v(y)}{dy^2} - m_v^2\theta_v(y) = -\frac{q_v^{'''}}{k_v} \tag{2.21}$$

Where $\theta_m(x)$ and $\theta_v(y)$ are the temperature rises of the interconnect and the via with respect to the reference temperature. The reference temperature for M2 interconnect is the substrate temperature. k_m and k_v are the thermal conductivity of the interconnect and the via. Both are made of copper, hence $k_m = k_v$. m_m and m_v are defined by,

$$m_m = \sqrt{\frac{S_m k_d}{A_m k_m}} = \sqrt{\frac{S_m k_d}{W_m h_m k_m}} \tag{2.22}$$

$$m_m = \sqrt{\frac{S_v k_d}{A_v k_v}} = \sqrt{\frac{S_v k_d}{\pi D^2 k_v}} \tag{2.23}$$

Where A_m and A_v are the cross-sectional of the interconnect and the via respectively, k_d is the thermal conductivity of the dielectric and S_m and S_v are the shape factors per unit length of the interconnect and the via respectively. They are a function of geometry parameters which describes the multidimensional heat flow conduction from the metal surface into the medium [81] [83] and are given by [81][83][84],

$$S_m = 1.86 \left[log\left(1 + \frac{t_{ins}}{W_m}\right)\right]^{-0.66} \left(\frac{W_m}{h_m}\right) \tag{2.24}$$

$$S_v = \frac{2\pi}{ln(4h_v/D)} \tag{2.25}$$

Where t_{ins} is the thickness of the insulator underneath the interconnect. $q_m^{'''}$ and $q_v^{'''}$ are the volumetric heat generations due to joule heating in the interconnect and the via, and are given by [81],

$$q_m^{'''} = (J_{bid}^{int})^2 \rho_{Tint} \tag{2.26}$$

$$q_v^{'''} = (J_{bid})^2 \rho_{Tvia} \tag{2.27}$$

J_{bid}^{int} and J_{bid} are the bidirectional current density flowing through the signal path and the via. ρ_{Tint} and ρ_{Tvia} are the electrical resistivity of the interconnect and of the via respectively.

The effects of barrier and surface scattering are taken into account for via/interconnect resistivity estimation [59][82]. Due to high resistivity of the barrier in copper interconnects, all the current through the interconnect/via is carried by copper.

Therefore the effective area through which the current conduction takes place reduces, increasing the resistivity of the interconnect. Moreover, due to technology scaling the minimum interconnect dimensions become comparable to *mean free path of electrons* [59]. This is because surface scattering starts have a non-negligible contribution to resistivity. Furthermore, surface scattering also reduces the thermal coefficient of resistivity [59]. Hence, the effective resistivity is given by,

$$\rho_{Tm} = \rho_{eff}(1 + \alpha_{eff}(Tm - T_{ref})) \tag{2.28}$$

Where $\rho_{eff} = \gamma\rho_o$ and $\alpha_{eff} = \beta\alpha_o$. For copper, $\rho_o = 2.7x10^{-8}\Omega - m$ and $\alpha_o = 6.8x10^{-3}K^{-1}$. For 0.18$\mu$m technology, $\gamma = 1.0657$ and $\beta = 0.9527$ [59].

In order to solve equation 2.20, two boundary conditions are defined: the adiabatic condition at the center of interconnect (x=0) and the constant temperature rise at the beginning of the interconnect which corresponds at the junction between the line and the via, θ_j;

$$\frac{d\theta_m}{dx}|_{x=0} = 0, \theta_m(x = -\frac{L}{2}) = \theta_j \tag{2.29}$$

The boundary conditions for solving equation 2.21 are the constant temperature rise at the top of the via (y=0) and the zero temperature rise at the bottom of the via (y=hv).

$$\theta_v(y = 0) = \theta_j, \theta_v(y = h_v) = 0 \tag{2.30}$$

Hence the solutions for the temperatures raises for the interconnect and the via are,

$$\theta_m(x) = \theta_j \left(\frac{cosh(m_m x)}{cosh(m_m L/2)}\right) + \left(\frac{q_m^{'''}}{k_m m_m^2}\right)\left(1 - \frac{cosh(m_m x)}{cosh(m_m L/2)}\right) \tag{2.31}$$

$$\theta_v(x) = \theta_j \left(\frac{sinh(m_v(h_v - y))}{cosh(m_v h_v)}\right) + \left(\frac{q_v^{'''}}{k_v m_v^2}\right)\left(1 - \frac{sinh(m_v(h_v - y)) + sinh(m_v y)}{sinh(m_v h_v)}\right) \tag{2.32}$$

Considering the continuity equation (Eq.2.33) at the junction between the signal interconnect and the via, θ_j is:

$$-k_m A_m \frac{d\theta_m(x)}{dx} \mid_{x=-L/2} = -k_v A_v \frac{d\theta_v(y)}{dy} \mid_{y=0} \tag{2.33}$$

$$\theta_j = \frac{A_m \left(\frac{q_m^{'''}}{m_m}\right) tanh\left(\frac{m_m L}{2}\right)}{k_m A_m m_m tanh\left(\frac{m_m L}{2}\right) + k_v A_v m_v coth(m_v h_v)} + \frac{A_v \left(\frac{q_v^{'''}}{m_v}\right)(coth(m_v h_v) - csch(m_v h_v))}{k_m A_m m_m tanh\left(\frac{m_m L}{2}\right) + k_v A_v m_v coth(m_v h_v)} \tag{2.34}$$

According to this, the temperature increment in the via (See Appendix A for interconnects), $\theta_v(y) = \Delta T_{via} = T_{via}(y) - T_{ref}$, is dependent on its cross-sectional area, hence $\theta_v(y)$ depends on the via voiding (X-void) due to a defect.

Figure 2.18 shows the temperature distributions along the via for different values of via voiding (X). As X void increments, the temperature in the via raises. The major temperature raises is observed to be at middle of the via as X void increases. In order to determine the MTF of the via an average temperature is taken for each value of X void.

The normalized current density, using the cylindrical model for vias, is

$$\frac{J_{bid}^d}{J_{bid}^o} = \frac{1}{(1 - X)^2} \tag{2.35}$$

where J_{bid}^d is the current density of the defective via and J_{bid}^o is the current density of the defect-free via.

Equations 2.19, 2.35 and via average temperature (T_{via}) are used to estimate the normalized reliability risk for vias located in signals paths. The MTF of the

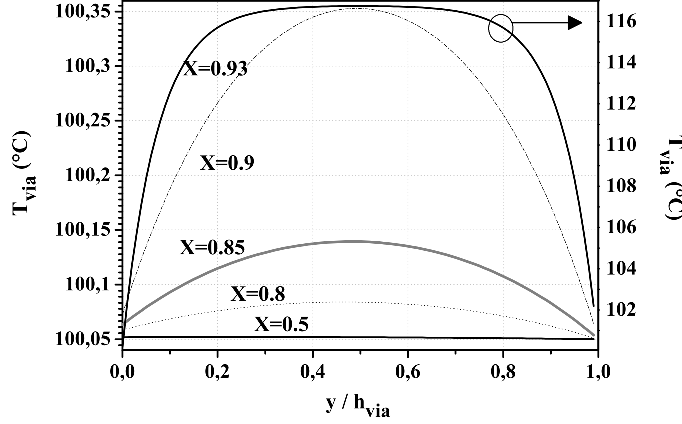


Figure 2.18: Temperature distribution along the via as function of X voiding. Considering TSMC 0.18μm, hv=1μm, D=0.26μm, L=1mm, $k_d = 1.5W/m-K, k_v = 400W/m-K$. $I_{bid} = (1-R)I_{av+} = 0.2mA$

defective via (MTF^d_{bid}) is normalized with respect to the MTF of the defect-free via (MTF^o_{bid}). This gives

$$\frac{MTF^d_{bid}}{MTF^o_{bid}} = (1-X)^4 exp(\frac{E_a}{K_B}(\frac{1}{T_{via}} - \frac{1}{T_{ref}})) \tag{2.36}$$

Figure 2.19 plots equation A.9 showing the estimated rapid reduction in the mean time to failure as the void size increases. The curve shows that if the fractional voiding is 20%, then the MTF has dropped to 40%. Furthermore, when the fractional void is 50%, the MTF has dropped to almost 4%. Contrary to our conclusion that resistive vias show little disturbance to the signal transmission until severe voiding occurs, the electromigration threat is significant for relatively small via voiding. The curve in Figure 2.19 shows the fragile nature of resistive vias converting to opens.

Actual vias in integrated circuits will have better MTFs than those predicted by Fig. 2.19. This is because some nodes have lower activity factor which leads

to lower density currents. However, vias located at those nodes presenting high activity factors would be compromised.

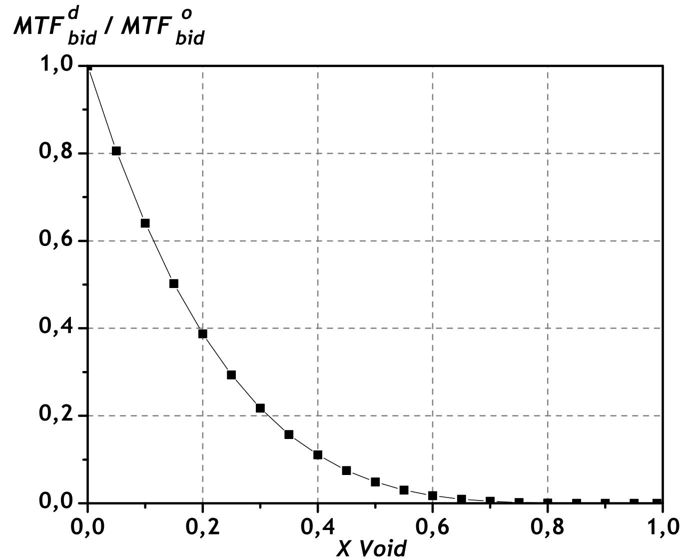


Figure 2.19: MTF reduction for one bidirectional via as a function of X void.

2.4 Analysis for Contacts/Vias Located in Conducting Paths

In this case we are dealing with contact/vias that are located between V_{DD} and ground. Vias located in conducting paths drive current densities with only one polarity (See Figure 2.20). The cylindrical vias model is also used for these contact/vias. The same inverters and interconnect system used for vias in signal paths (See figure 2.9) are also used for vias in conducting paths. Figure 2.20 shows a possible location of the conctact/via in a conducting path.

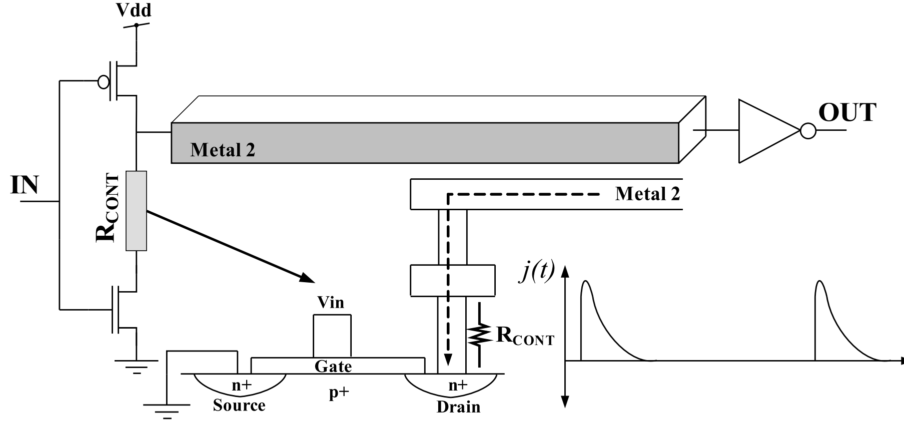


Figure 2.20: Schematic diagram of the system under analysis. Resistive via defect is in conducting path

2.4.1 Transient Behavior

The behavior of the via resistance and delay as via voiding increases is similar to the case for vias located in signal paths. This is shown in Figure 2.21. A wide range of X voids lead to small delays that may may escape test. However, they pose a reliability risk as shown next.

2.4.2 Reliability Risk for Vias located in Conducting Paths

The reliability risk for contact/vias in conducting paths can also be estimated using equation 2.16 replacing J_{uni} instead of J. J_{uni} is the average current density for unidirectional vias and is given by,

$$J_{uni} = \frac{1}{T}\int_0^T J dt = J_{av} \tag{2.37}$$

In this case the current flowing across a contact/via located in a conducting path has one polarity (See Figure 2.20) with no healing effect. The via temperature can also be estimated by the heat conduction equations presented before.

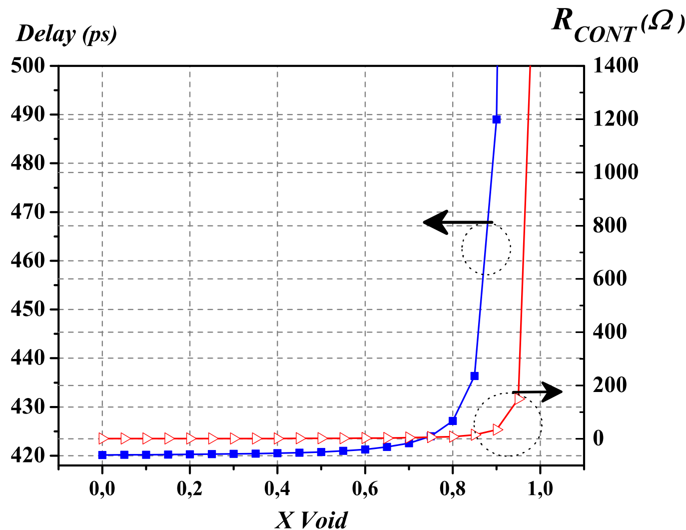


Figure 2.21: Behavior of the resistance and delay a via located un conducting path

The MTF of the defective via (MTF^{d}_{uni}) is normalized with respect to the MTF of the defect-free via (MTF^{o}_{uni}). This gives

$$\frac{MTF^{d}_{uni}}{MTF^{o}_{uni}} = (1 - X)^{4} exp(\frac{E_a}{K_B}(\frac{1}{T_{via}} - \frac{1}{T_{ref}})) \tag{2.38}$$

Figure 2.22 plots equation A.1 showing a significant MTF reduction as the void size increases. Similarly to vias in signal paths, these resistive vias also pose a reliability risk. This is because small delays are observed for a wide range of X voids which are difficult to detect.

2.5 Reliability Evaluation for Redundant Vias

Via doubling is a technique used to improve yield due to spot defects affecting vias [68][86][88][89][86].

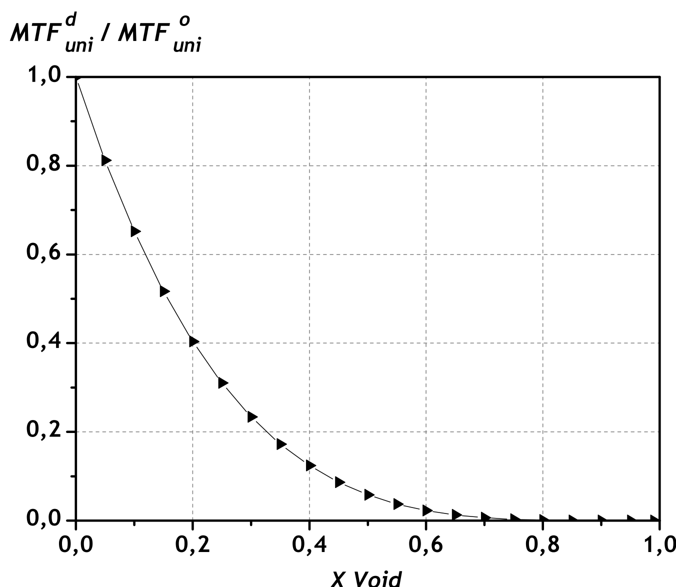


Figure 2.22: MTF reduction as a function of x void.

Double via insertion provides a redundant via which can serve as a fault-tolerant substitute for the failing one [90].

However, if the amount of inserted redundant vias is not well controlled, it may adversely worsen the yield and reliability of the design due to maximum via density violation rule which can lead to pattern distortion issues [90][89].

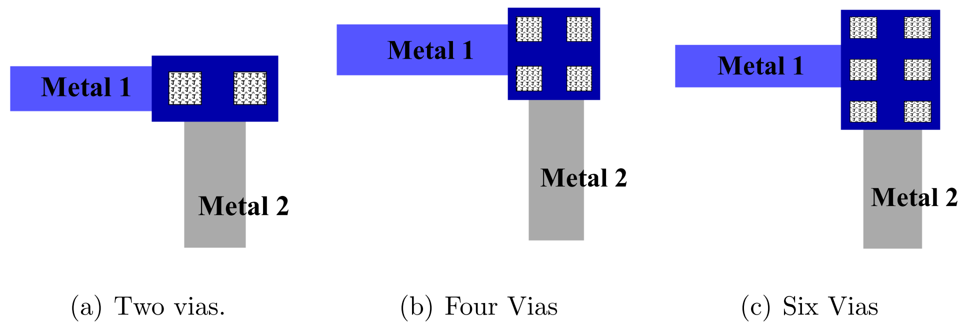
Via density is defined as the number of vias located within a rectangular region into a via layer in the chip. The maximum via density places an upper bound constraint, U, on the via density. Hence, this region violates maximum via density rule when U is exceeded [89]. For instance, Lee et all [88], define a region of 10.08μm x 8.4μm on a via layer and setting the maximum number of vias for this region to 30 considering a $0.18\mu m$ technology.

Via pattern distortion issues are a consequence of CMP process and optical lithography such as *Optical Proximity Correction-OPC* [87].

Pattern distortion of vias induced a contour distortion of vias. Kunishima

et al in [85], demonstrates that contour distortion of vias induces micro void formation affecting circuit reliability.

The reliability analysis for singles vias is extended to the case when more than one via is used to connect two different metal layers. This analysis is devoted for the case of vias located in signal paths. However, the results can also be applied to conducting paths. Figure 2.23 shows possible layouts when two, four and six vias are used to connect two different metal layers. When there is via duplication, the probability that the two vias are defective is very low [68]. Due to this fact, it is considered that only one via is defective.



(a) Two vias. (b) Four Vias (c) Six Vias

Figure 2.23: Layout when redundant vias are used.

The presence of two or more vias connecting two different-level conductors can modeled as an array of parallel resistor communicating the two conductors. The equivalent resistance of the via array is less than the resistance of one single via. For two vias connecting two different metal layers, when the resistance of one of them is higher than the other the equivalent resistance tends to the value of the via with the smallest resistance. In other words, the equivalent resistance will tend to the resistance value of the defect-free via. Because of this the delay is basically non modified when there are redundant vias and one of them has a resistive open. Figure 2.24 shows the behavior of the delay for two vias connecting Metal 1 and Metal 2 with one of them defective. No significant change on the delay occur.

Despite the delay is not significantly affected when one of the redundant vias

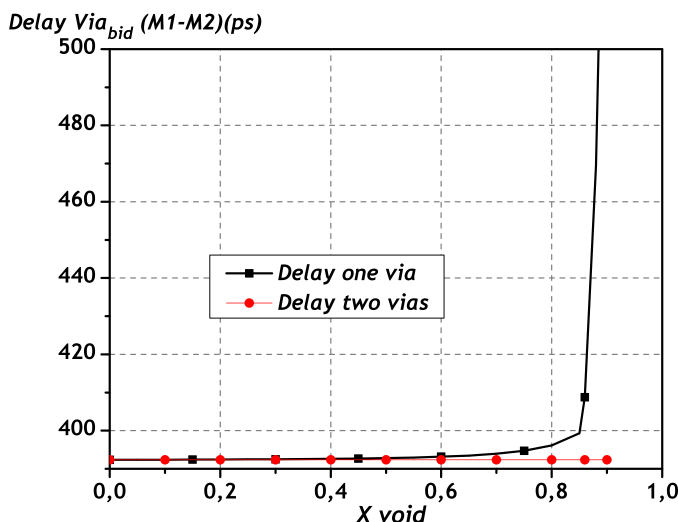
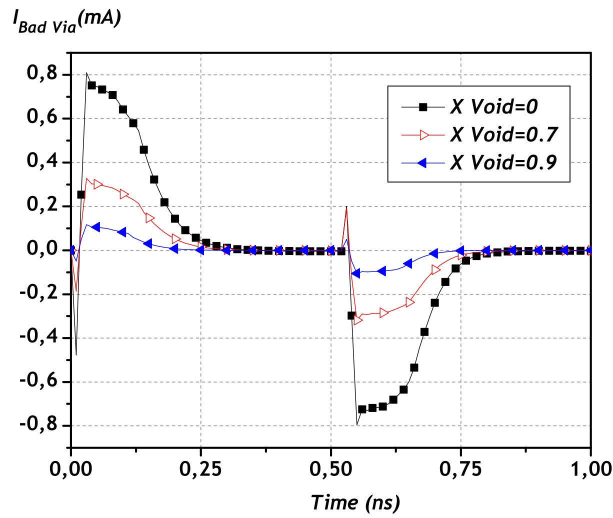


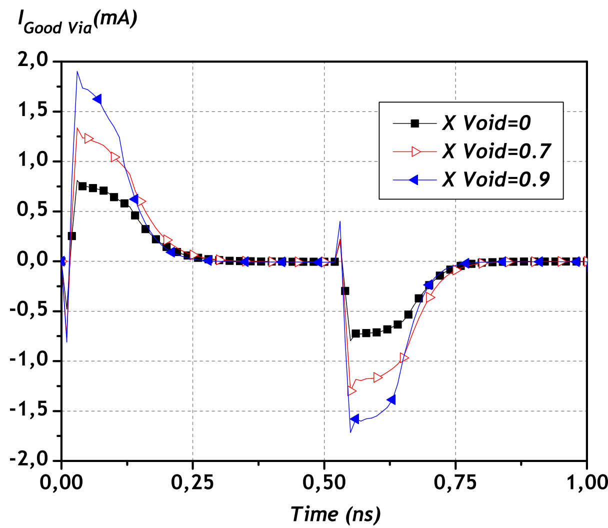
Figure 2.24: Behavior of the delay on vias located in signal paths. One via and two vias are considered

is defective, however, the presence of one resistive via may affect the lifetime of neighboring defect-free via(s). This is because less current flows through the defective via and more current flows through the defect-free via when the resistance value of the open increases. This means that the current density stress in defect-free vias increases as the void volume reduces. Figure 2.25 shows the current waveforms across defective via (bad via) and non-defective vias (good vias) when two vias are used to connect two different metal layers. It is observed that as the X void size increases more currents flows across good via(s), and at the same time less current flows across the bad via.

Figure 2.26 shows the normalized current density for good via(s) for 2, 4 and 6 redundant vias as function of the void size. J_n^{good} is the current density for the good via(s) in the presence of a bad via, and J_n^o is the current density of good via when no via is defective. n is the number of vias. When more than one via is used, the current density of the good via raises as the void size of the defective via increases. The increase in the current density is lower as more redundant vias



(a) Current waveforms through the bad via for different values of X void.



(b) Current waveforms through good via for different values of X void.

Figure 2.25: Current waveforms when two unipolar vias with one of them defective

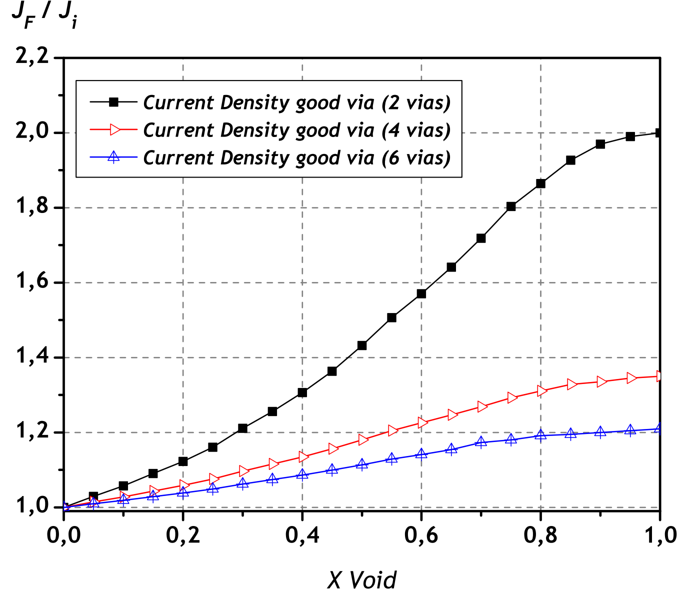


Figure 2.26: Behavior of the current density on good via(s) as a function of X void in defective via.

are used.

The increase in the current density affects the MTF of both the good and bad vias which is analyzed next. For redundant vias, equation A.9 is modified to obtain an expression for the MTF of the bad via (MTF_n^{bad}) normalized with respect to the MTF of the good via(s) when no via is defective (MTF_n^o). This gives

$$\frac{MTF_n^{bad}}{MTF_n^o} = \left(\frac{(1-X)^2\rho_{Tm}^g + (n-1)\rho_{Tm}^b}{n\rho_{Tm}^g}\right)^2 \times exp\left(\frac{E_a}{K_B}\left(\frac{1}{T_m} - \frac{1}{T_{ref}}\right)\right) \tag{2.39}$$

where n is the number of vias.

In a similar way, an expression for the MTF of the good via(s) (MTF_n^{good})

normalized with respect to the MTF of the good via(s) when no via is defective. This gives

$$\frac{MTF_n^{good}}{MTF_n^o} = \left(\frac{(1-X)^2\rho_{Tm}^g + (n-1)\rho_{Tm}^b}{n\rho_{Tm}^b}\right)^2 \times exp\left(\frac{E_a}{K_B}\left(\frac{1}{T_m} - \frac{1}{T_{ref}}\right)\right) \quad (2.40)$$

Equations 2.39 and 2.40 are plotted in Figures 2.27 and 2.28. Figure 2.27 shows the normalized MTF of the bad via when two, four and six redundant vias are used with one of them defective. The MTF of the bad via improves as more vias are used but MTF reduction continue to be significant. Figure 2.28 shows the MTF of the good via when two, four and six redundant vias are used with one of them defective. For two redundant vias, the MTF of the good via also decreases significantly as the void size increases. The MTF of the good via has reduced to 50% when the void size is 40%. The MTF of the good via(s) improves when more via redundancy is used, nevertheless, maximum via density rule must be taken into account. This is an important result showing that reliability risk issue should also be considered when via duplication techniques are used.

2.6 Influence of Technology Scaling

According to the scaling trend, vias connecting two different metal levels will continue to be scaled in future technologies. Due to the critical dimensions (CD) of vias, current densities in them increases at a much faster rate than for other interconnects as technology goes beyond 90nm [79] [42]. Furthermore, thermal effects will be a serious issue [67] [42] affecting the Mean Time to Failure of interconnects. Important self heating increment in vias has been reported in [79]. In this section, an analysis of via MTF reduction due to a manufacturing defect (X void), is investigated.

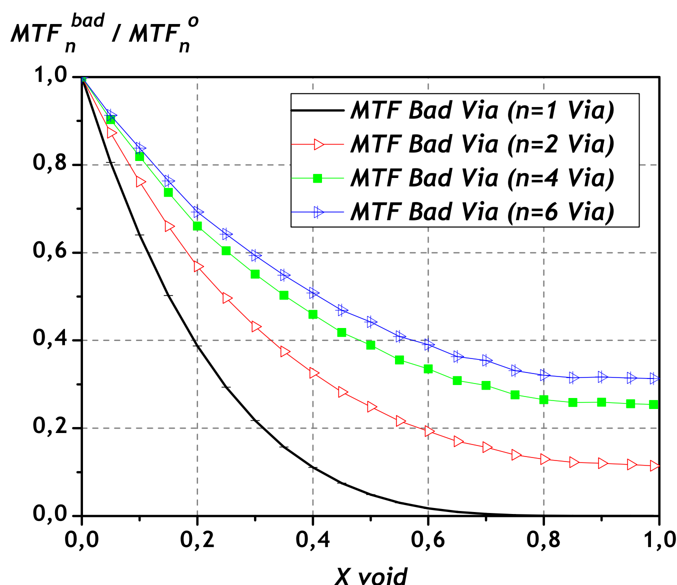


Figure 2.27: Bad via MTF as a function of X void for two, four and six redundant vias with one of them defective.

Table 2.1 shows data of CD vias for different technologies [13]. Data for aspect ratios (AR) and the maximum current ($Imax$) flowing through the vias [80] are also given. Using this information in the previous equations, the MTF behavior of the via as function of the void size (X) for different technologies has been obtained (See figure 2.29. The trend is that the MTF decreases as the technology scales. This is due to the fact that the current density increases.

Another important scaling technology issue is that Low-K dielectrics are replacing SiO_2 for reducing resistance-capacitance (RC) time delays. Nevertheless, one of the paramount reliability concerns of Low-K dielectrics is their lower thermal conductivity [42] [20] which makes more significant the impact of self heating. Figure 2.30 shows the temperature distribution along the via using a Low-K dielectric, with thermal conductivity of 0.25 W/m-K. It is observed that temperature increases. Moreover the MTF behavior as the technology scale us-

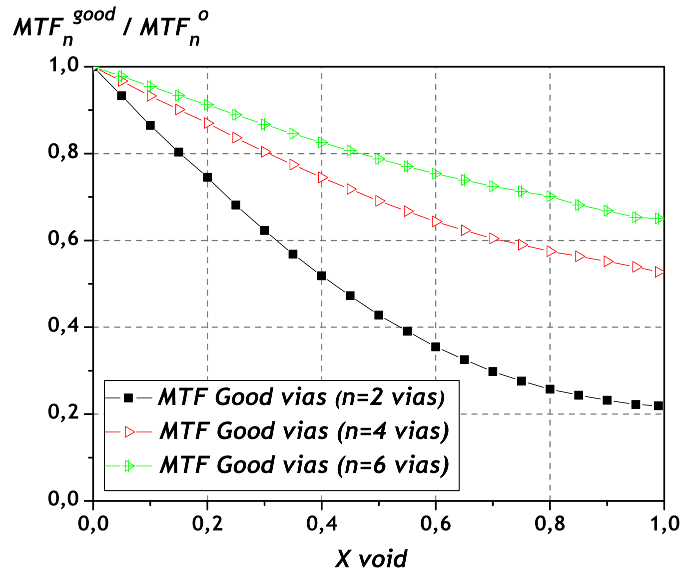


Figure 2.28: Good vias MTF as a function of X void for two, four and six redundant vias with one of them defective.

ing SiO_2 and a Low-K dielectrics has been obtained Figure 1.9. The results are shown for a given X void size. The MTF is significantly reduced when a Low-K dielectric is used.

2.7 Conclusions

The reliability risk posed by undetected small delays due to weak resistive open in signal interconnects and vias has been quantified. The Mean Time to Failure (MTF) considers both the effect of Electromigration (EM) and Self Heating. The data given here shows that the MTF for weak resistive opens is significantly degraded.

The analysis for vias considered vias located in signal and conducting paths. The MTF of good and bad vias has also investigated when techniques of vias redundancy are used. MTF degradation is quantified as function of via voiding

Table 2.1: Via scaling behavior [13] [80], AR=via height/via width

Technology Node	CD (nm)	AR	Imax(mA)
180nm	360	1.8	0.3
130nm	225	1.8	0.29
90nm	125	1.9	0.24
70nm	100	2	0.2
45nm	70	2.1	0.1

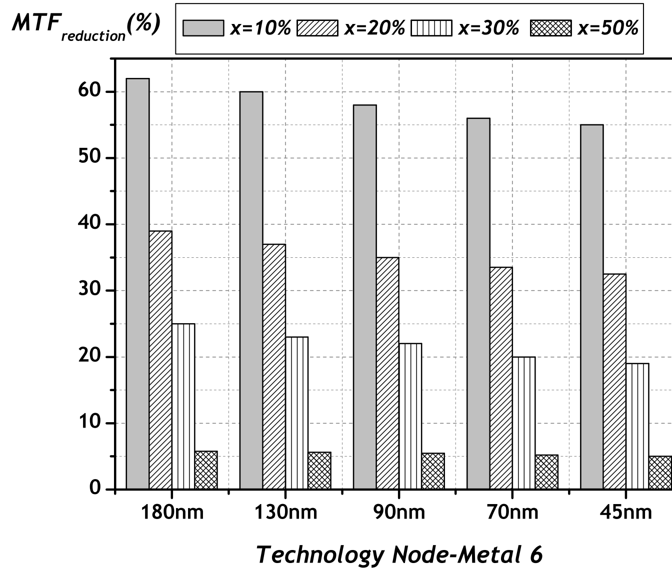


Figure 2.29: MTF reduction as function of scaling technology. X void considered: 10%, 20%, 30% and 50%

and the number of total vias. It has been found that the the reliability of good vias degrades due to the presence of a defective via. This is due to the fact that the defective via presents a higher resistance. Hence, the average current density for good vias increases. Strategies of vias redundancy, such as via duplication, should take into account not only critical area constraints, but also reliability

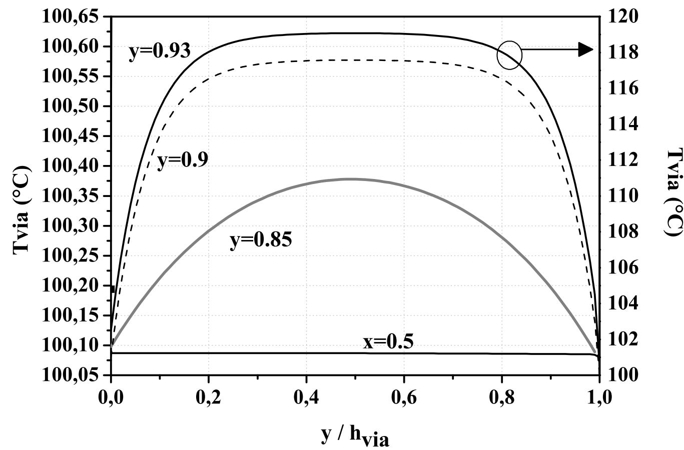


Figure 2.30: Temperature distribution along the via. The dielectric conductivity is thermal 0.25 W/m-K

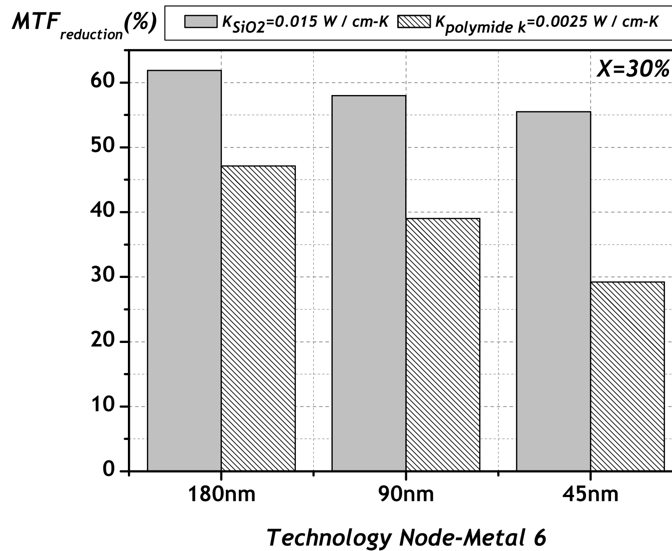


Figure 2.31: MTF reduction for different dielectric's thermal conductivity when X void is 30%

risk. From resistive vias behavior located in signal paths, signal experiments an speed-up before defect and a slow down after defect. This proper behavior will

be used to detect resistive open defects. The results obtained are available for signal interconnects.

Chapter 3

Test Strategy to detect interconnect wear-out using on-line sensors

As VLSI technology scales, interconnects are becoming the dominant factor determining system performance. Also, the probability of spot defects during manufacturing process considerably increases. A spot defect in interconnects behave as a resistive open defect. In previous chapter it was demonstrated weak resistive open defects produce small delays difficult to detect and considerably affect the interconnect reliability due to electromigration and self heating which can lead to a full open failure at interconnects. Therefore, in this chapter a test strategy to detect small delays before interconnect full open occurs is presented. The test schema is based on detect the defect by means of detecting the signal speed-up (negative skew) generated in defective interconnect before the resistive open. On-line negative skew sensor located at the beginning of interconnect is proposed. Timing verification uses the principle of complementary signals addition [91]. On-line self-test method is also needed to take control of neighboring coupling. Because of process variations delays, a modification of the test method

is necessary to assure small delay detected is only produced by a resistive open. For this, a positive skew sensor located at the end of interconnect is added.

The rest of the chapter is organized as follows: in section 3.1 the test schema is presented. The principle of complementary signals addition is discussed in section 3.2. Next, the proposed skew sensors are presented in section 3.3. In Section 3.4 Negative skew sensor characterization is performed. The test strategy to differentiate a defect small delay from process variations small delays is presented in section 3.5. In section 3.6 the cost of the proposed methodology is evaluated. Finally, the conclusions of the chapter are given in section 3.7.

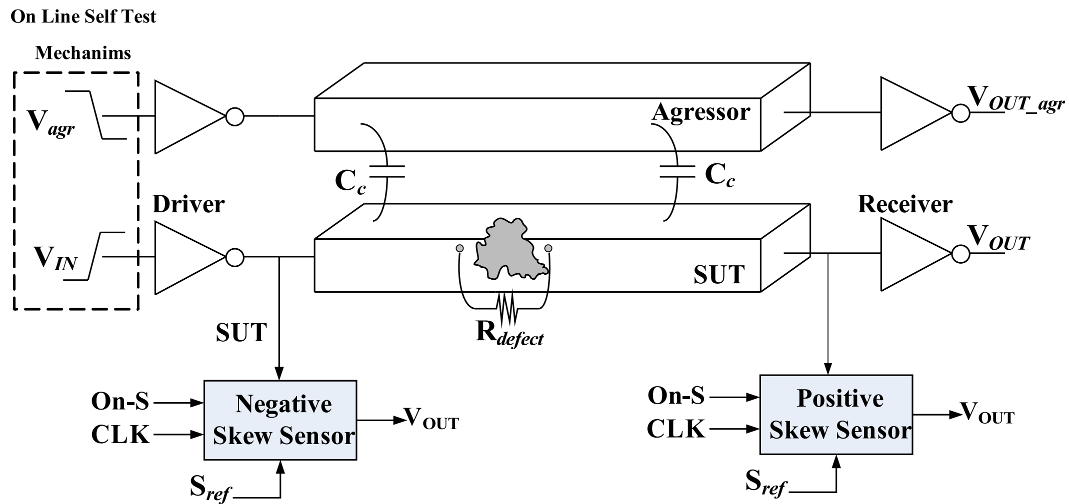
3.1 Test Schema

In a defective interconnect, the value of the resistive defect progressively grows up owing to workload causing interconnect wear-out by means of electromigration and self heating until produce a full open.

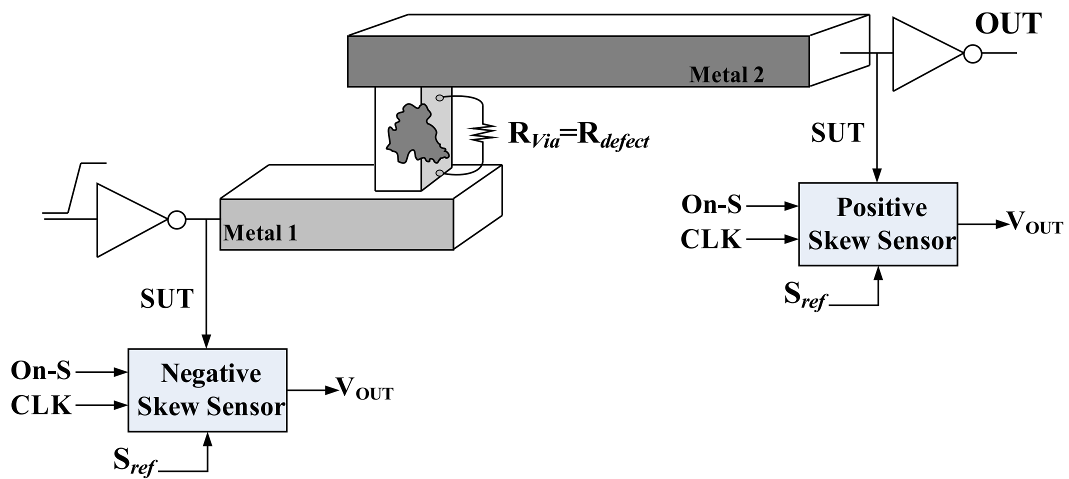
The objective is to detect the interconnect degradation due to defect before full open occurs. The detection is based on signal transient behavior before and after resistive defect with an adequate coupling of neighboring interconnects.

The proposed test strategy for on-line interconnect wear-out detection is shown in Fig 3.1.

Signal under test (SUT) flows through a defective interconnect. According to signal speed-up (negative skew) behavior before defect and signal slow down (positive skew) behavior after defect, a negative skew sensor is located near the interconnect driver and a positive skew sensor is located near the interconnect receiver. The small delay due to a weak defect could be detected by only negative skew sensor. Nevertheless, the small delay may also be generated by process variations, thus the use of the positive skew sensor is to differentiate small delay due to a weak defect from process variations. These topics are depicted in next sections.



(a) Interconnect System.



(b) System for Vias in signal paths

Figure 3.1: Proposed interconnect wear-out detection.

The coupling of neighboring interconnects are fixed in order to slow down SUT but is not critical. Hence, aggressors signal are complementary to SUT. Therefore, when a signal speed up is detected by sensor, it is due to a resistive open defect. Due to the fact that gradually wear-out of defective interconnects depends on workload and time-stress on field, the monitoring of the interconnects of a circuit or a system should be activated from time to time, in other words, should be periodic [49][45][92]. Considering this, sensor should have an on-off mechanism (See Fig. 3.1, On-S input.). These feature also prevents wear-out on the sensor.

To control neighboring couplings and on-off mechanism of the on-line sensor, an on-line self test method is needed. It is no part of this work. Many self test method has been performed in literature. According to test features mentioned before, the self test method suggested to used is CASP: Concurrent Autonomous chip self test using Stored test Patterns reported by [93]. CASP is a special kind of self test where a system test itself concurrently during normal operation. The main motivation for CASP is to enable robust system design with self-healing capabilities required to overcome major scaled CMOS reliability challenges such as transistors wear-out (aging, see chapter 4) and system infant mortality [93]. The basic idea is to store very thorough test patterns in non-volatile storage and provide architectural and system-level support for testing one or more cores in a multi-core system while the rest of the system continues operating normally. Major CASP features are [93]:

1. CASP is useful for circuit failure prediction, error detection based on periodic self test.

2. CASP applies high quality test-patterns with quantified test coverage.

3. CASP utilizes already existing on-chip Design for Testability (DFT) and test compression features.

4. CASP Test patterns can be changed according to application requirements and failure characteristics even after a system is deployed in the field.

5. CASP imposes significantly lower overhead compared to traditional redundancy techniques.

These are the reasons because CASP suits with the proposed wear-out detection.

The proposed On-line BIST interconnect wear-out monitoring, is oriented to automotive application. This is because of the complex electronics used in this area is intended to operate for long periods of time (i.e. 10 years). Therefore the presence of a spot defect in these circuits represents a high reliability risk degrading their Mean Time to Failure, which will be worsen as technology scales. Taken into account this application, the sensor could be activated by CASP at each moment that a car is turned on.

3.2 Sensor Verification Methodology

3.2.1 Timing Verification

According to results about transient interconnect resistive open behavior obtained in chapter 2, timing relationship between signal under test (SUT) and a signal reference (Sref) is analyzed in order to characterize the timing issue the proposed sensor will detect.

Two possible situations are considered:

1. The signal SUT is either later or earlier than Sref, see Fig. 3.2.

2. The edges of the SUT signal are different to Sref edges, see Fig. 3.3

Fig. 3.2 shows the case when delay shift (Δtd) is: $\Delta td > 0$ when SUT is late than Sref or $\Delta td < 0$ when SUT is earlier than Sref.

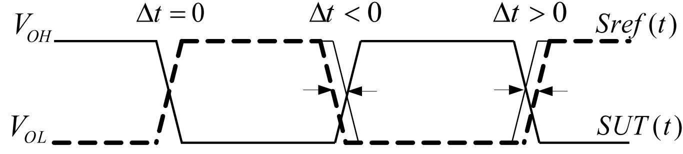


Figure 3.2: Time skew cases: $\Delta t < 0$ is a negative skew. $\Delta t > 0$ is a positive skew.

Fig. 3.3 shows the case when SUT and Sref have different time edges, that is when SUT and Sref rise and/or fall time are not equal. ϕt is the ratio of the edges duration of SUT with respect to Sref. When,

$$\phi t = \frac{t_{edge_{SUT}}}{t_{edge_{Sref}}}$$

, equals to unity, edges of both signals have the same duration. For $\phi_t > 1$ rise/fall time of SUT is greater than rise/fall time of Sref and contrary when $\phi_t < 1$.

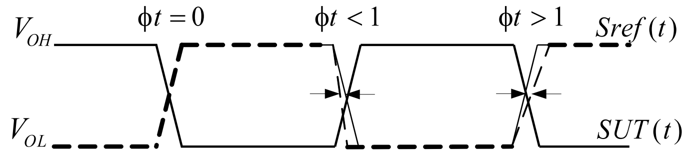


Figure 3.3: Skew due to different edges between SUT and Sref. $\phi t < 1$ is a negative skew. $\phi t > 1$ is a positive skew.

To sum up, five cases of skew problems (see table 3.1) must be taken into account for sensor detection.

3.2.2 Complementary Signals Addition

The proposed wear-out verification methodology is based on adding two complementary digital signals. This proposal is based in the fact that the resulting sum of two ideal complementary digital signals without skew between them gives a constant signature value.

Table 3.1: Possible skew problems between two signals, Sref is considered the reference signal, and SUT is the signal under test

Case number	Amount of skew	Situation between $x(t)$ and $y(t)$
I	$\Delta_t = 0$	no skew at all
II	$\Delta_t > 0$	SUT arrives later than Sref (Positive skew)
III	$\Delta_t < 0$	SUT arrives earlier than Sref (Negative skew)
IV	$0 < \phi t < 1$	$SUT_{edge} < Sref_{edge}$ (Negative skew)
V	$\phi t > 1$	$SUT_{edge} > Sref_{edge}$ (Positive skew)

When two complementary digital signals are verified, there are two regions of interest. Fig 3.4 shows this regions for SUT (solid line) and Sref (dashed line).

1. *Region 1*, this region is defined for the time of Sref falling edge and SUT rising edge.

2. *Region 2*, this region is defined for the time of Sref rising edge and SUT falling edge.

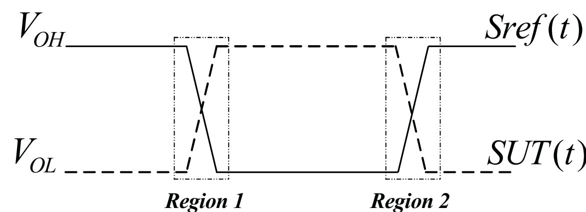


Figure 3.4: Skew regions under study.

From Fig 3.4 it is observed these regions are established from the moment when either edge (raising/falling) of one signal (SUT or Sref) begins to the moment when the corresponding opposite edge (falling/raising) ends.

A detail analysis for each skew cases of Table 3.1, will be presented.

Case I: Ideal complementary signals

This case corresponds to the situation when there is no skew between SUT(t) and Sref(t). Their edges, rise and fall times, start at the same time and have the same time duration.

From Fig.3.4, a zoom of the *Region 1* has been taken for the analysis (see Fig. 3.5). In this region, Sref(t) and SUT(t) can be described by

$$Sref(t) = V_{OH} + m_{Sref}t, \tag{3.1}$$

$$SUT(t) = V_{OL} + m_{SUT}t. \tag{3.2}$$

In Eqs. 3.1 and 3.2, the edges of the signals are represented as slopes of magnitude m_{Sref} and m_{SUT} for signals Sref(t) and SUT(t), respectively. These slopes can be defined as

$$m_{Sref} = \frac{V_{OL} - V_{OH}}{T_{f_{Sref}}}, \tag{3.3}$$

$$m_{SUT} = \frac{V_{OH} - V_{OL}}{T_{r_{SUT}}}. \tag{3.4}$$

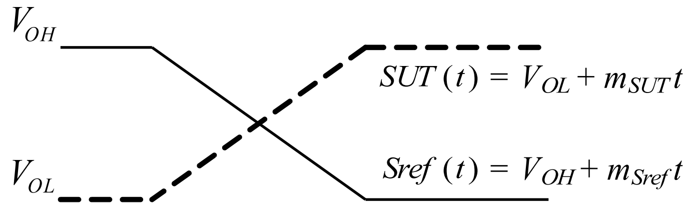


Figure 3.5: Zoom of region 1 used for analysis. SUT(t) and Sref(t) expressed as linear functions.

Where $T_{f_{Sref}}$ and $T_{r_{SUT}}$ stand for the fall and rise times of Sref(t) and SUT(t) respectively.

The sum (Vs(t)) of two signals Sref(t) and SUT(t) is given by

$$Vs(t) = Sref(t) + SUT(t) \tag{3.5}$$

Replacing Eqs. 3.3 and 3.4 in Eqs. 3.1 and 3.2, the sum of the addition of signals $Sref(t)$ and $SUT(t)$ gives

$$Vs(t) = V_{OH} + V_{OL}. \tag{3.6}$$

This equations means that the sum of two ideal complementary signals without skew between them gives a constant voltage value independently of the states of the signals. This will be called the *stable sum*.

For *Region 2* the same analysis could be done but considering a rising edge for Sref(t) and a falling edge for SUT(t). As a result, $Vs(t)$ value for *Region 2* is also $V_{OH} + V_{OL}$.

Case II: Positive skew, $\Delta t > 0$

This case corresponds to the situation where SUT(t) arrives later with respect to reference signal Sref(t). This is shown in Fig. 3.6. Δt is the amount of time that SUT is shifted to the right with respect to Sref. It is appreciate in both regions, *Region 1* and *Region 2*.

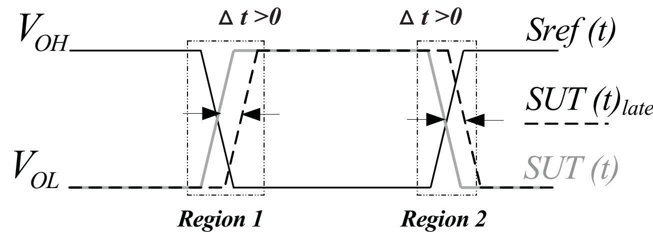


Figure 3.6: Case II: Positive Skew, $\Delta t > 0$. Two regions: *Region 1* and *Region 2*

First *Region 1* is analyzed and then *Region 2*. A zoom of *Region 1* is shown in Fig. 3.7a. This region can be divided in three sections:

- Section A: In this section only the signal Sref(t) changes with time.

- Section B: In this section both signals, Sref(t) and SUT(t), change with time.

- Section C: In this section only the signal SUT(t) changes with time.

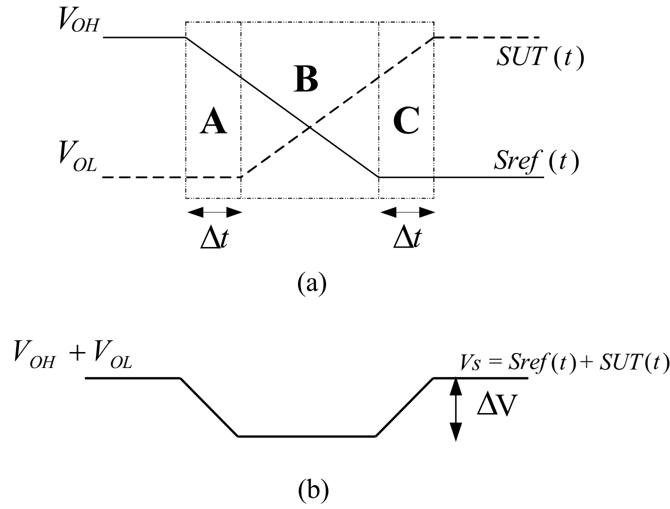


Figure 3.7: Zoom of *Region 1* used for analysis. SUT(t) arrives later than Sref(t). Three sections are observed.

For each one of the sections, first two equations are stated, one representing the reference signal Sref(t), and a second equation representing the signal under analysis SUT(t). Then, their sum resulting of the addition of the two signal is obtained.

1.- Section A: In this section signal Sref(t)changes with time while SUT(t) is constant. According to this, Sref(t) and SUT(t) are given by,

$$Sref(t) = V_{OH} + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}} t, \tag{3.7}$$

$$SUT(t) = V_{OL}; \tag{3.8}$$

Making addition of Sref(t) and SUT(t) their sum $Vs(t)$ gives

$$Vs(t) = V_{OH} + V_{OL} + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}}t, \tag{3.9}$$

In this case the sum deviates from the stable sum value according to the rightmost term in Eq. 3.9. This term represents the voltage deviation $\Delta V(t)$ from the ideal constant value. Because of this the sum decreases linearly with time (See Fig. 3.7b), the minimum value of this deviation (ΔV) occurs at the end of section A where t is equal to Δt. Thus

$$\Delta V = \lim_{t \to \Delta t} \Delta V(t) = \lim_{t \to \Delta t} \frac{|V_{OL} - V_{OH}|}{t_{f_{Sref}}}t = \frac{\Delta t}{t_{f_{Sref}}}|V_{OL} - V_{OH}|, \tag{3.10}$$

From Eq. 3.10 it can be stated that ΔV has a linear dependence with Δt whereas it is inversely proportional to the duration of the falling edge of the reference signal Sref(t).

2.- Section B : In this section both signals, Sref(t) and SUT(t), change with time (See Fig. 3.7a). It has also to be noted that we are dealing with ideal complementary signals. Because of this, it has been assumed equal fall and rise times for Sref(t) and SUT(t), respectively. The signal SUT(t) can be described by

$$Sref(t) = V_{OH} - \Delta V + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}}t, \tag{3.11}$$

and the signal SUT(t) can be represented by,

$$SUT(t) = V_{OL} + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}}t, \tag{3.12}$$

Making the addition of Sref(t) and SUT(t), and using the fact that the fall/rise times of Sref(t)/SUT(t) are equal, their sum gives

$$Vs(t) = V_{OH} + V_{OL} - \Delta V, \tag{3.13}$$

From this equation, it can be stated that the sum is a constant voltage level in Section B. This is illustrated in Fig. 3.7b. This is because the variations of Sref(t) and SUT(t), in this section, have the same slope magnitude but different sign. This has a cancellation effect of the variations.

3.- Section C: In this section signal Sref(t) is constant while signal SUT(t) changes with time. For this section, Sref(t) is described by

$$Sref(t) = V_{OL}, \tag{3.14}$$

Then, SUT(t) is given by,

$$SUT(t) = V_{OH} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t, \tag{3.15}$$

Making the addition of Sref(t) and SUT(t) gives:

$$Vs(t) = V_{OH} + V_{OL} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t, \tag{3.16}$$

According to this, in section C takes place an equal but opposite effect on $Vs(t)$ than in section A. $Vs(t)$ begins to increase with time in Section C as illustrated in Fig. 3.7. The final value for $Vs(t)$ could be estimated by,

$$\begin{aligned} \lim_{t \to \Delta t} \sigma(t) = \lim_{t \to \Delta t} V_{OH} + V_{OL} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t \\ = V_{OH} + V_{OL}, \end{aligned} \tag{3.17}$$

From this equation it can be stated that at the end of region C, $Vs(t)$ has been restored to the stable sum after a time equal to Δt. This is only valid when the fall and rise times of Sref(t) and SUT(t), respectively, have the same value.

Now *Region 2* of Fig. 3.6 is analyzed. Unlike *Region 1*, in *Region 2* rise/fall times of Sref(t)/SUT(t) are taken into account. A zoom of this region is shown in Fig. 3.8a. This region is also divided in three sections (A, B and C). A similar

analysis to *Region 1* can be made. The results are illustrated in Fig. 3.8b. In this case, the sum of the addition of Sref(t) and SUT(t) goes up in Section A, then is constant in Section B, and goes down in Section C. At the end of this section the sum has been restored to the stable sum value, $V_{OH} + V_{OL}$.

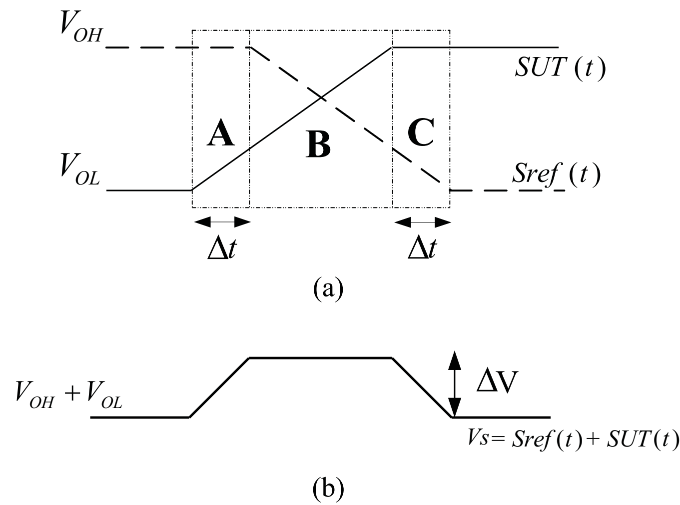


Figure 3.8: Zoom of Region 2 used for analysis. Three section is also observed.

Case III: Negative Skew, $\Delta t < 0$

This case represents a situation where the transitions of signal SUT(t) arrive earlier with respect to the reference signal Sref(t). The amount of time arriving earlier is called Δt and is considered less than zero. This is illustrated in Fig.3.9a where $SUT(t)$ (broken line) is shifted to the left with respect to its ideal edge. As with positive skew case, there are also two regions of interest, *Region 1* and *Region 2*. In this case, *Region 1* and *Region 2* are equivalent to *Region 2* and *Region 1* of positive skew situation respectively and the same analysis performed in previous cases can be made for this case. The results are illustrated in Fig.3.9b. In this case, the sum, $\sigma(t)$, goes up in *Region 1* and goes down in *Region 2* from its stable value in opposite way to Case II.

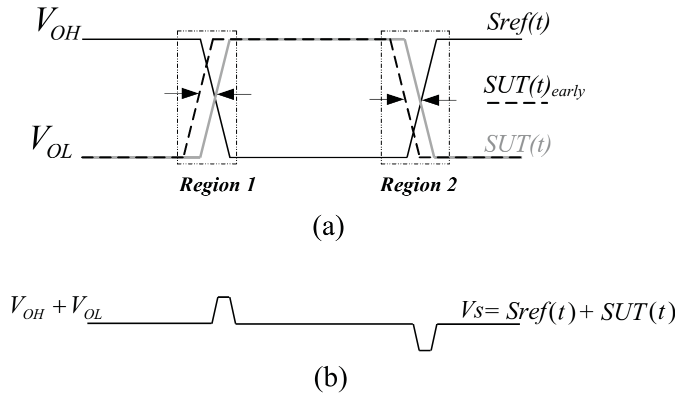


Figure 3.9: Sum behavior of two ideal complementary signals with negative skew

Case IV: $\phi t > 1$

This case represents the situation where SUT(t) has a rise/fall time greater than fall/rise time of Sref(t). Hence, SUT(t) arrives later than Sref(t). Fig 3.10 shows this case. For this case only *Region 1* is analyzed. This is due to in *Region 2* ϕt is not necessarily > 1. It could be 1 or < 1. Nevertheless, the positive skew introduced in *Region 1* will be appreciated in *Region 2*. Thus, a similar analysis to case II can be made. But, when ϕt will be $\neq 1$, the analysis of this case or of the next case (Case V) can be made.

A zoom of Region 1 is used for analysis. Unlike before cases, Region 1 is divided into two sections as is shown in Fig 3.11a.

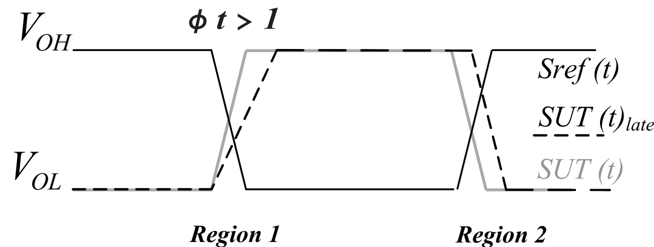
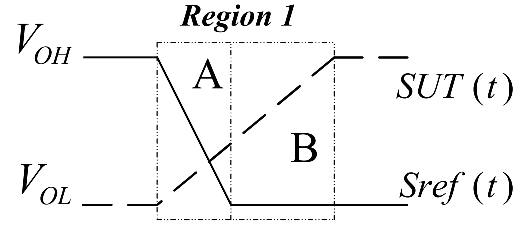


Figure 3.10: Situation when edges of SUT is greater than edges of Sref.

1.- Section A: In this section, both SUT and Sref change with time and are



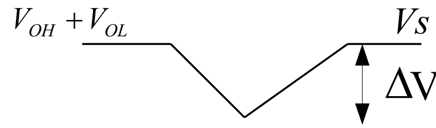


Figure 3.11: Zoom of Region 1 used for analysis and behavior of V_σ when $\phi t > 1$.

given by,

$$SUT(t) = V_{OL} + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t \tag{3.18}$$

$$Sref(t) = V_{OH} + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}} t \tag{3.19}$$

With $t_{r_{SUT}} > t_{f_{Sref}}$. Then, making addition of them, V_σ(t) is,

$$V_\sigma(t) = V_{OL} + V_{OH} + t[\frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}}] \tag{3.20}$$

Next, taking into account ϕt=$t_{r_{SUT}}/t_{f_{Sref}}$, V_σ(t) changes to,

$$V_\sigma(t) = V_{OL} + V_{OH} + \frac{t}{t_{f_{Sref}}}[\frac{V_{OH} - V_{OL}}{\phi t} + (V_{OL} - V_{OH})] \tag{3.21}$$

From this equation, the rightmost term is define as $\Delta V(t)$. V_σ decreases with time according to $\Delta V(t)$. Considering the duration of section A is equal to fall time of Sref, the minimum $\Delta V(t)$ is obtained from,

$$\Delta V = \lim_{t \to t_{f_{Sref}}} \Delta V(t) = \lim_{t \to t_{f_{Sref}}} \frac{t}{t_{f_{Sref}}}[\frac{V_{OH} - V_{OL}}{\phi t} + (V_{OL} - V_{OH})] = (V_{OL} - V_{OH})\left(1 - \frac{1}{\phi t}\right), \quad (3.22)$$

According to this, ΔV is inversely proportional to ϕt. Fig 3.12 shows the behavior of ΔV as function of ϕt.

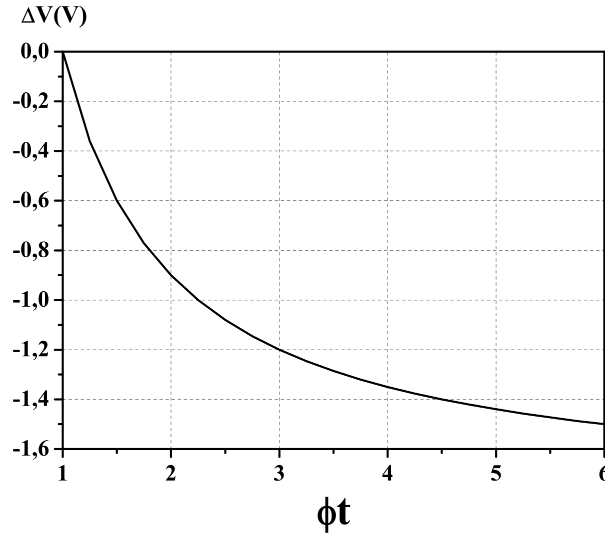


Figure 3.12: ΔV variation as function of ϕt when $\phi t > 1$.

2.- Section B:

In this section V_σ is restored to $V_{OH} + V_{OL}$ (See Fig 3.11b). Sref is V_{OL} and SUT is given by,

$$SUT(t) = V_{OH} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t \quad (3.23)$$

Then, V_σ is,

$$V_\sigma(t) = V_{OL} + V_{OH} - \Delta V + \frac{V_{OH} - V_{OL}}{t_{r_{SUT}}} t \quad (3.24)$$

The time duration of section B is given by:

$$\Delta t = t_{r_{SUT}} - t_{f_{Sref}} \tag{3.25}$$

Hence, the final value of V_σ is obtained from the limit of equation 3.24 when t tends to Δt defined in equation 3.25. Finally, making some operations, V_σ is given by,

$$\lim_{t \to \Delta t} V_\sigma(t) = V_{OH} + V_{OL}, \tag{3.26}$$

Case V: $\phi t < 1$

This case corresponds to the situation where SUT(t) has a rise/fall time smaller than fall/rise time of Sref(t). Hence, SUT(t) arrives earlier than Sref(t). Fig 3.13 shows this case. As previous case, only *Region 1* is analyzed.

A zoom of Region 1 is shown in Fig. 3.14. Similar to case IV, *Region 1* is divided into two sections.

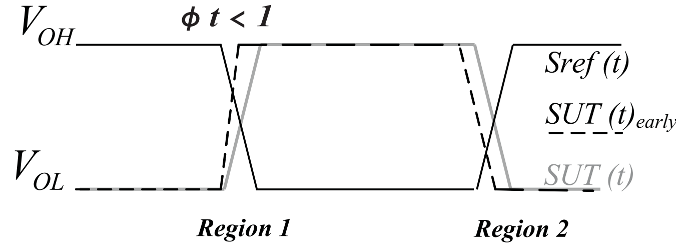


Figure 3.13: Situation when edges of SUT is faster than edges of Sref.

1.- Section A: In this section, both SUT and Sref change with time and are given by equations 3.18 and 3.19. Unlike section A of case IV, in this section $t_{r_{SUT}} < t_{f_{Sref}}$. Then, Vs(t) is also given by equation 3.21. Nevertheless, its behavior is opposite to case IV, Vs(t) increases with time as the rightmost term of equation 3.21, ΔV(t). This is shown in Fig 3.14b. Moreover, the time duration of section A is in this case equal to rise time of SUT(t). Then, taken into account the last consideration and that ϕt=$t_{r_{SUT}}/t_{f_{Sref}}$, the maximum value of ΔV(t) is,

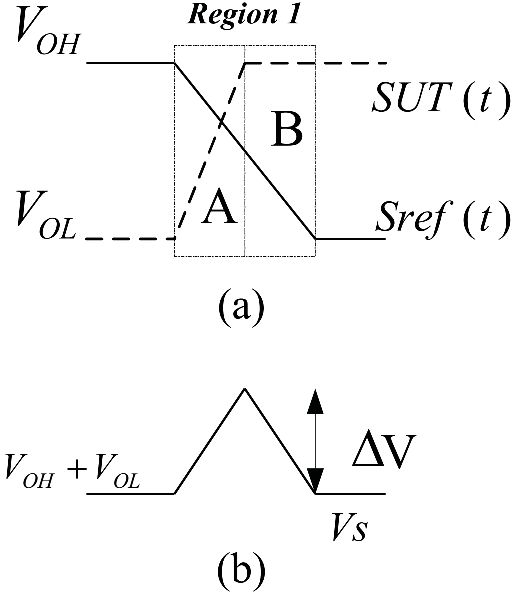


Figure 3.14: Zoom of Region 1 used for analysis and behavior of V_σ when $\phi t < 1$

.

$$\Delta V = \lim_{t \to t_{r_{SUT}}} \Delta V(t) = \lim_{t \to t_{r_{SUT}}} \frac{t}{t_{f_{Sref}}} [\frac{V_{OH} - V_{OL}}{\phi t} + (V_{OL} - V_{OH})] = (V_{OL} - V_{OH})(\phi t - 1), \tag{3.27}$$

According to this, ΔV is inversely to ϕt. Similar to case IV, Fig 3.15 shows the behavior of ΔV as function of ϕt.

2.- Section B: Similar to case IV, in this section Vs is restored to $V_{OH} + V_{OL}$. SUT is V_{OH} and Sref is given by,

$$Sref(t) = V_{OL} + \Delta V + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}} t \tag{3.28}$$

Then, Vs is,

$$Vs(t) = V_{OL} + V_{OH} + \Delta V + \frac{V_{OL} - V_{OH}}{t_{f_{Sref}}} t \tag{3.29}$$

The time duration of section B is given by:

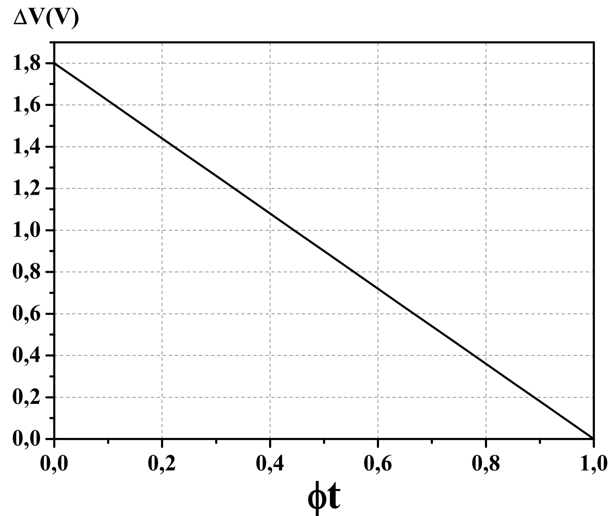


Figure 3.15: Zoom of region 1 used for analysis. SUT(t) arrives earlier than Sref(t). Three section is also observed.

$$\Delta t = t_{f_{Sref}} - t_{r_{SUT}} \tag{3.30}$$

Hence, the final value of Vs is obtained from the limit of equation 3.29 when t tends to Δt defined in equation 3.30. Finally, making some operations, Vs is given by,

$$\lim_{t \to \Delta t} Vs(t) = V_{OH} + V_{OL}, \tag{3.31}$$

3.3 On-Line Skew Sensor Implementation

A novel system detection of small defects is proposed. It consists of two skew sensors. A Negative Skew Sensor and a Positive Skew Sensor which are located near the driver and receiver respectively. This is in accord with the transient behavior of resistive interconnect presented in Chapter 2, where a signal flowing through a defective interconnect experiments a speed-up (negative skew, $\Delta td < 0$)

before the resistive defect and a slow down (positive skew, $\Delta td > 0$) after the resistive defect. This property is used to differentiate between small delays due to defective interconnects and small delays due to process variations. In this way, an interconnect gradual degradation due to a defect is only detected when both sensors detect at same time.

Figure 3.16 shows the schematic diagrams of the Negative and Positive Skew sensors. Both sensors are compounded by two stages: Skew Detector and Skew Discriminator.

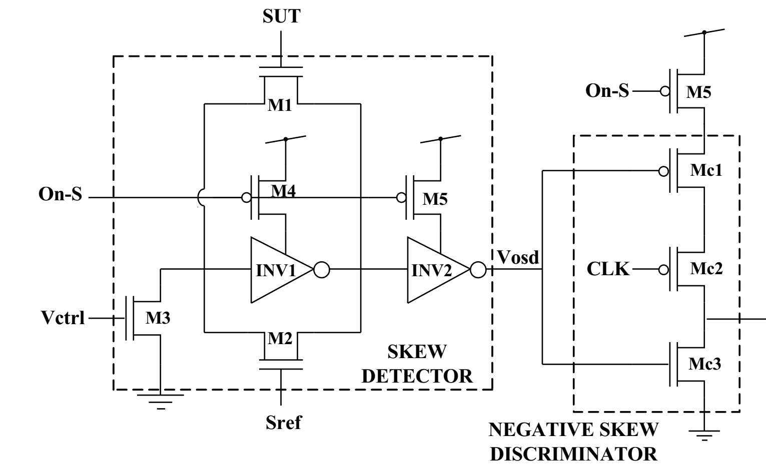
The topology is the same for both negative and positive skew sensor. The only difference is the use of the denied clock signal in the positive skew discriminator.

The skew detector is based on the addition of two complementary signals[91]. It is able to detect both positive and negative skew.

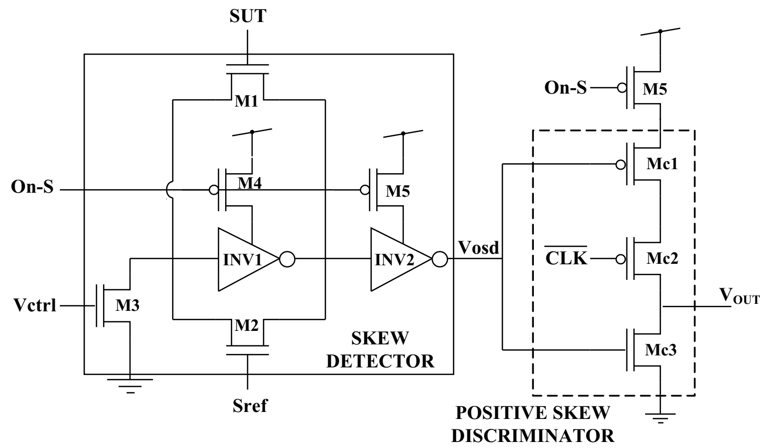
The negative skew discriminator stage synchronizes the output of skew detector with signal clock of system to identify when a negative skew, and no a positive skew, has been detected. On the other hand, positive skew discriminator is synchronized with the denied clock signal.

As the monitoring of interconnect is periodic and in order to prevent sensor to aging (See next Chapter), skew sensors have an on-off mechanism which are activated by on-line self test system. When On-S is logic '1', INV1(INV1p), INV2(INV2p), Mc1(Mc1p) and Mc2(Mc2p) are off, thus the output of negative(positive) skew sensor is 0. When On-S is '0', negative(positive) skew sensor is on and if a skew between SUT and Sref exist, a pulse from low to high is produced at its output.

The description of the operating of the negative skew sensor is now presented. The analysis is similar to Positive Skew Sensor. For the results that will be shown in next sections are valid when the sensor is on, hence On-S will be always 0 for next sections.



(a)



(b)

Figure 3.16: Schematic Diagrams of Negative and Positive Skew Sensors proposed.

3.3.1 Skew Detector Description

The skew detector[91] consists on a feedback inverter (INV1) operating as a linear amplifier [94], two NMOS sensing transistors (M1 and M2) that establish the dynamic behavior of the skew detector, a discriminating inverter (INV2) and a control transistor (M3). Figure 3.17 shows the schematic diagram of the skew detector.

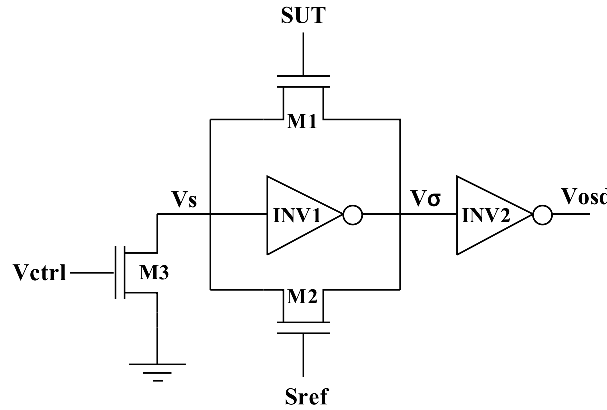


Figure 3.17: Schematic Diagram of the Skew Detector

Two ideal complementary signals, SUT(t) and Sref(t) are used at the gates of M1 and M2 respectively. Considering this, M1 and M2 never are on at the same time. When either M1 or M2 is on, it enters in triode region and inverter INV1 has a feedback loop. Under this conditions, voltages values at nodes Vs and V_σ (see Fig. 3.17) are approximately the same and around the threshold voltage (V_{TH}) of INV1. For a symmetric inverter V_{TH} is approximately VDD/2. Thus, PMOS and NMOS transistors of INV1 are operating in saturation region. According to this, CMOS inverter operates as a linear amplifier. If any AC variation at node Vs occurs, it will be amplified by INV1 at node Vσ. This situation will take place when a skew between SUT(t) and Sref(t) occurs, because the feedback loop of INV1 breaks.

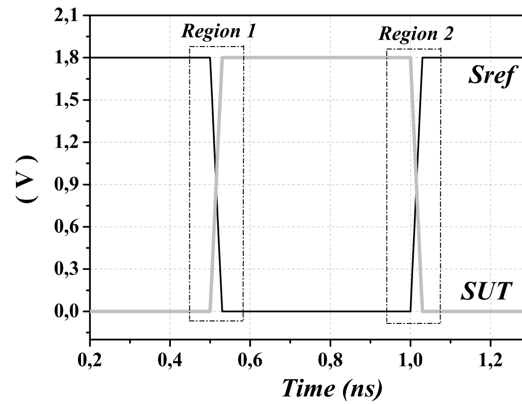
In order to give controllability to avoid a false detection because of Vs would be floating, M3 is added. M3 works as a active load with high resistance. It conforms

a resistive divider with sensing transistors and inverter on resistors. Therefore M3 slightly shifts down the level of Vs, but keeping inverter transistors in saturation region. Hence Vσ is shifted below threshold voltage of INV2 ($V_{TH}^{INV2} \approx VDD/2$). Thus, a critical skew window (W) is defined by Vσ and V_{TH}^{INV2}.

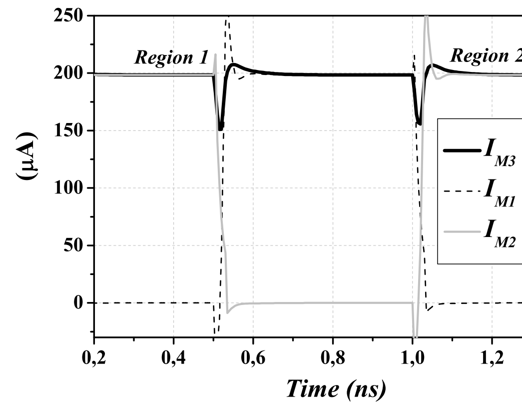
The addition of complementary signals, SUT and Sref, occurs at node Vs in function of currents of sensing transistors (M1 and M2) and control transistor (M3). The voltage value of Vs is fixed by resistive divider conformed by M3, M1/M2 and inverter transistors. Thus, the stable sum of SUT + Sref is Vs. When a skew between SUT and Sref occurs, Vs discharges and deviates from its stable value, according to the theory depicted in previous section. Considering this, the sum addition at node Vs for each skew cases (see Table 3.1) is now presented.

Ideal complementary signals: Case I

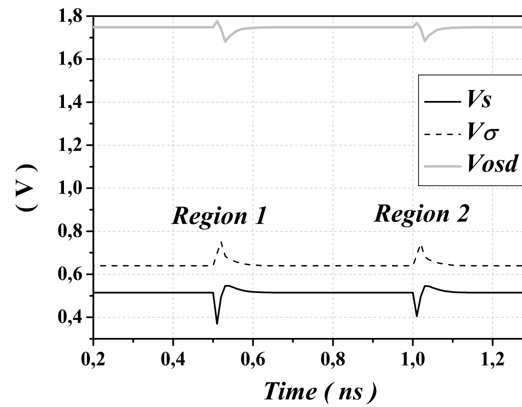
This case corresponds to when there is no skew between SUT and Sref. Under this situation, at the moment M2 (Sref) is turning off M1 (SUT) is turning on. The current decrease due to M2 turning off is compensated by current increase due to M1 turning on, thus the feedback loop of INV1 does not break and the current through M3 is practically constant and Vs remains stable in its stable value, although a very small undershoot could appear at Vs due to threshold voltage of M1 to turns on. Fig. 3.18 shows this situation. The input signals, SUT and Sref, with no skew are shown in Fig. 3.18a. Regions of interest, *Region 1* and *Region 2* are also depicted. Currents through M1, M2 and M3, for *Region 1* and *Region 2*, are shown in Fig. 3.18b. The voltage value at nodes Vs, V_σ and output of skew detector, Vosd are shown in Fig. 3.18c.



(a) Input Signals: SUT and Sref.



(b) Currents through M1, M2 and M3.



(c) Voltage at node Vs.

Figure 3.18: Signal Transient behavior at node Vs when $\Delta t = 0$.

Positive Skew: Case II

Figure 3.19 shows the situation when a positive skew ($\Delta t > 0$) between SUT and Sref takes place.

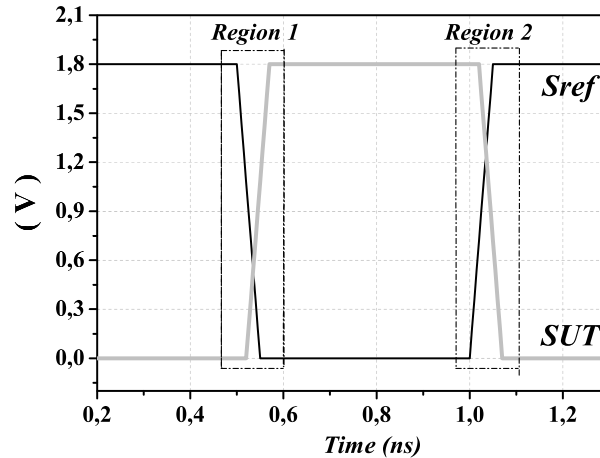
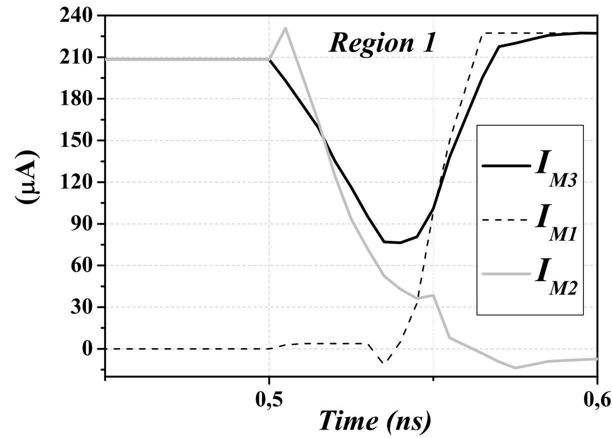


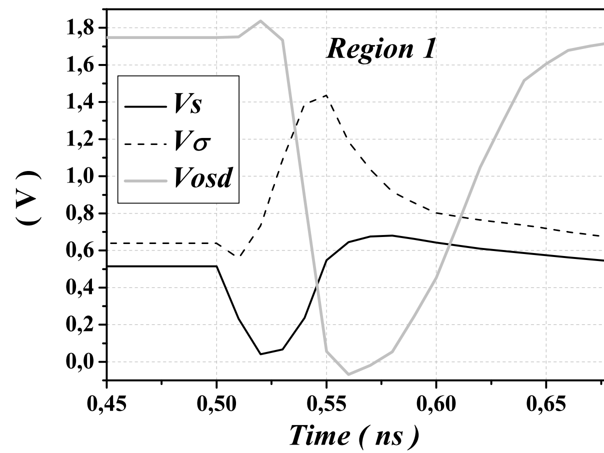
Figure 3.19: Input signals when $\Delta t > 0$.

As in previuos section, there are two regions of interest: *Region 1* and *Region 2*. First *Region 1* is analyzed. In this region, M2 is turning off when M1 is still off. As M2 is becoming a high resistance, its current decreases and as consequence current through M3 also decreases (See Fig. 3.20a). Therefore, under this situation the feedback loop of inverter breaks and an undershoot of value ΔVs appear at Vs. As inverter (INV1)operates as a linear amplifier with gain A_{INV1}, the undershoot produced at Vs is amplified by A_{INV1} at node V_{σ}. Thus, an overshoot of value ΔV appears at node V_{σ} (See Fig. 3.20b). If this overshoot has sufficient energy (height and width) over threshold voltage of discriminating inverter (critical window) the skew violation is detected. The undershoot appears until M1 turns on thus the feedback loop is established again and Vs is restored to its stable value.

For *Region 2* of Fig. 3.19, in opposite situation to *Region 1*, M2 is turning on when M1 is still on. Now, M1 and M2 operates as two parallel resistances, thus



(a) Currents through M1, M2 and M3.



(b) Voltage at node Vs.

Figure 3.20: Signal behavior at node Vs at Region 1 when $\Delta t > 0$.

current is divided between Ron_{M1} and Ron_{M2} proportionally. When both M1 and M2 are on ($Ron_{M1} = Ron_{M2}$), their currents are the same until M1 turns off. At that moment all current flows through M2. The feedback loop of INV1 does not break in any moment. Under this situation, current through M3 is almost constant with slightly fluctuations due to transitions. Thus, Vs tends to remain constant and as consequence V_σ also remains constant. Fig. 3.21 shows this situation. Currents through M1, M2 and M3 are shown in Fig. 3.21a. Voltage at node Vs, V_σ Vosd are depicted in Fig.3.21b.

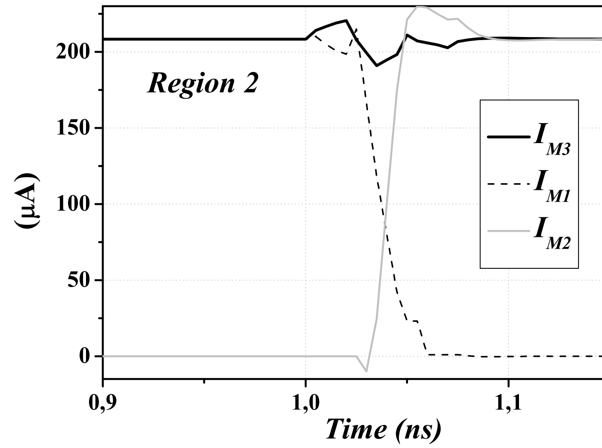
Negative Skew: Case III

When a negative skew between SUT and Sref occurs, as explained in previous section, *Region 1* and *Region 2* for this situation are equivalent to *Region 2* and *Region 1* of positive skew case respectively and the same analysis for Vs behavior performed above can be made for this case. Therefore, while for a positive skew case an undershoot is produced at Vs in *Region 1*, for a negative skew case it is in *Region 2*. Fig. 3.22 shows this situation. Input signals, SUT and Sref are shown in Fig. 3.22a. Voltage at Vs, V_σ and Vosd are shown in Fig. 3.22b. Currents are not depicted. Their behavior is similar to Figs. 3.20 and 3.21.

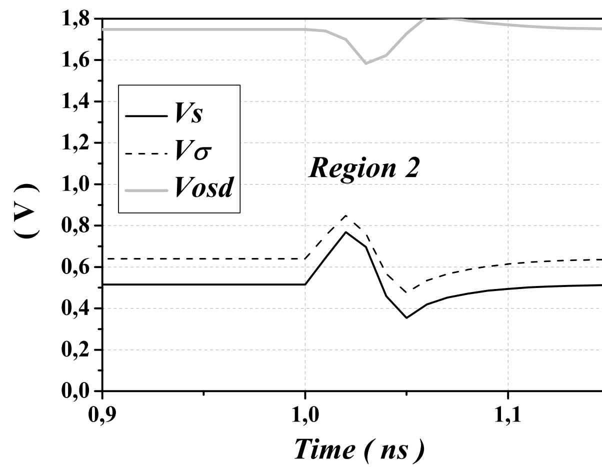
Different Edges: Case IV and Case V

According to theory performed in previous section, when $\phi t > 1$ or $\phi t < 1$ means that a positive skew or a negative skew exist between SUT and Sref, respectively. Thus, at the value VDD/2 for Sref and SUT, exists a Δt. Hence, the feedback loop of INV1 will break during Δt and Vs discharges at that moment. Therefore, the transient behavior of the sum at node Vs of addition of SUT and Sref, is similar to previous cases.

In summary, according to previous analysis, skew detector is able to detect both positive and negative skews in different periods of time. Moreover, due to

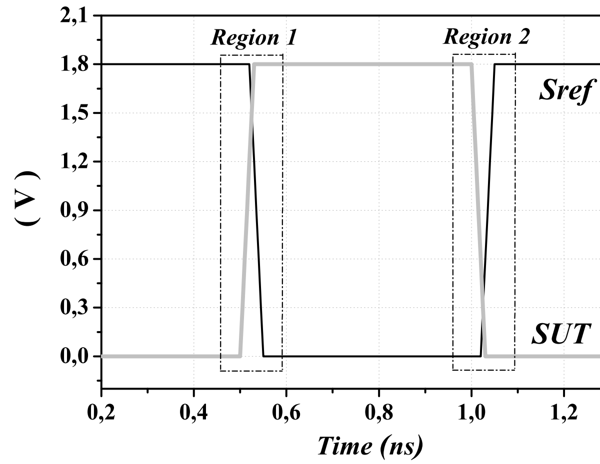


(a) Currents through M1, M2 and M3.

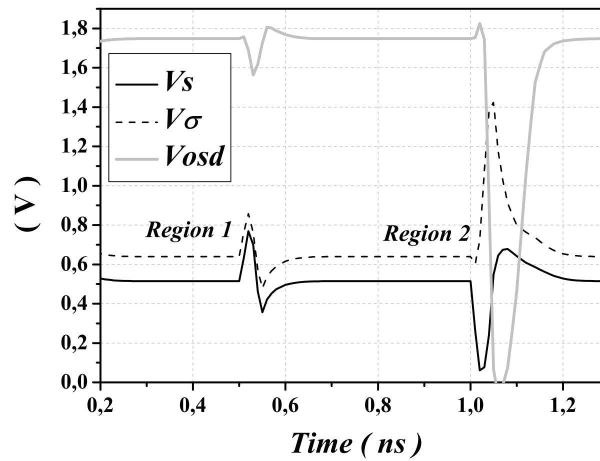


(b) Voltage at node Vs.

Figure 3.21: Signal behavior at node Vs at Region 2 when $\Delta t > 0$.



(a) SUT, Sref.



(b) Voltage at node Vs, V_σ and Vosd.

Figure 3.22: Signal behavior at node Vs when $\Delta t < 0$.

the greater gain of the CMOS inverter amplifier, skew detector is able to detect very small skews between complementary signals. Therefore, these properties are exploited to detect small defects on interconnects.

3.3.2 Negative Skew Discriminator Description

The Negative Skew Discriminator allows to know if the skew detected is negative. It consists on three discriminating transistors. Two PMOS and one NMOS (See Fig.3.16). Its output (V_{OUT}) is the drain of Mc3 transistor and also is the output of the complete sensor. The inputs of the discriminator are the output skew detector and the system clock signal. The clock enters to gates of Mc2. The skew detector output enters to the gate of Mc1 and Mc3. Fig. 3.23 illustrates the performance of the negative skew discriminator. Signals SUT(t) and Sref(t) presents a positive skew ($\Delta t > 0$) and a negative skew ($\Delta t < 0$) between them. The clock signal (CLK) is supposed to be on phase with SUT. When a positive skew between SUT(t) and Sref(t) occurs, the pulse (from high level to low level) generated at the output of skew detector ($Vosd$) takes place when clock (CLK) is high level. Thus, Mc2 and M1 are off and Mc3 is on and therefore V_{OUT} is a low level. An opposite situation happens when a negative skew is detected. It takes place when CLK is low. For this situation Mc1 and Mc2 are on and Mc3 is off, hence V_{OUT} change from low to high level.

3.4 Sensor Performance

3.4.1 Simulation Results

Taken into account the signal (SUT) transient behavior of a defective interconnect at node before the resistive defect explained in chapter 2, the negative skew sensor performance is characterized by a negative skew generated by ϕt < 1 (ϕt=$t_{(rise/fall)_{SUT}}/t_{(fall/rise)_{Sref}}$).

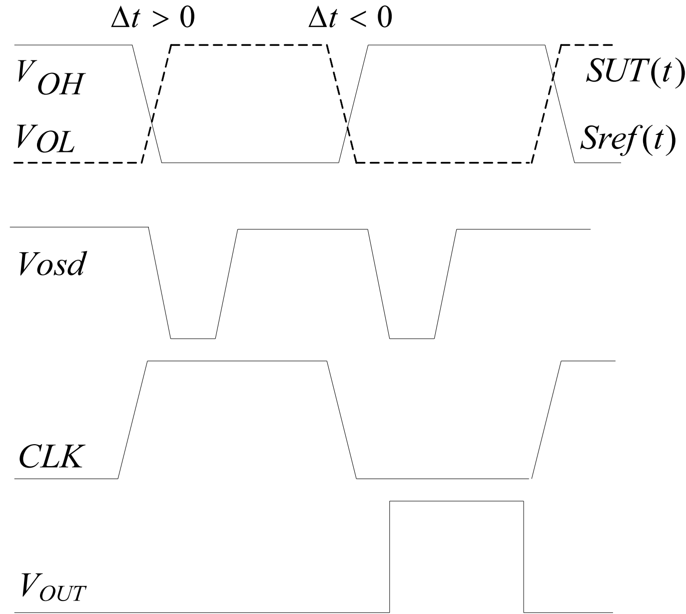


Figure 3.23: Performance of the Negative Skew Sensor

The sensor design effort has been focus on detecting, with high robustness to process and power supply variations, the minimum resistance value for the resistive defect because of its high reliability risk as has been demonstrated in chapter 2. This defect resistance value is associated with a minimum negative skew $|\Delta t|$ at the value of VDD/2 of SUT and Sref. In this work, the target is $|\Delta t|$=25ps, which corresponds to a resistive defect, $R_{defect} \approx 60\Omega$ and in terms of voiding at interconnect due to EM and self heating, it is about approximately 84%. Sensor transistors are sized in order to obtain this goal. TSMC 0.18μm CMOS technology is used to evaluate the sensor performance. The transistor channel widths are indicated in Table 3.2. Channel length for all transistors are the minimum allowed by the technology (0.18μm). Inverters (INV1, INV2) are symmetric. V_{ctrl} of M3 is fitted to 1.8V. Electrical simulations has been made in HSpice. Figures 4.15 shows the simulation results when $R_{defect} = 0\Omega$ and when $R_{defect} = 60\Omega$. The signal showed are: signal under test (SUT(t)), signal reference (Sref(t)), clock signal (CLK), output skew detector (V_{osd}) and sensor output (V_{OUT}). For the case when R_{defect} is 0Ω, there is not skew and non pulse is

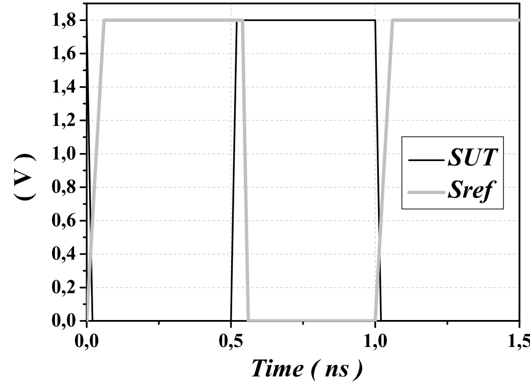
Table 3.2: Channel Widths of transistor of the Negative Skew Sensor, all the lengths are $0.18\mu m$

Device	Width (μm)
M1	1.08
M2	1.08
M3	0.28
Mc1	0.36
Mc2	0.36
Mc3	0.54
INV1	$\beta = \frac{1.62}{0.54}$
INV2	$\beta = \frac{1.62}{0.54}$

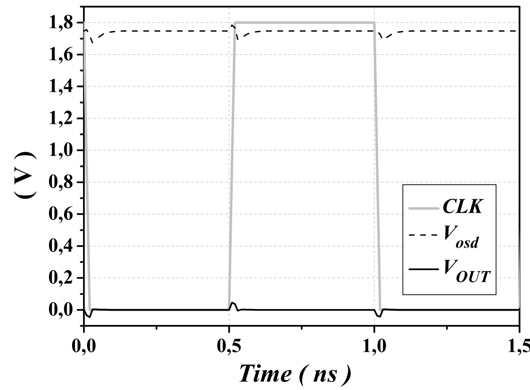
generated at the output of skew detector and sensor output remains low. For the case when R_{defect} is 60Ω, the negative skew generated is equivalent to Δt≈25ps. When a negative skew occurs, the pulse generated at the output of skew detector occurs when clock is low and a pulse from low to high happens at sensor output.

3.4.2 Monte Carlo Simulation

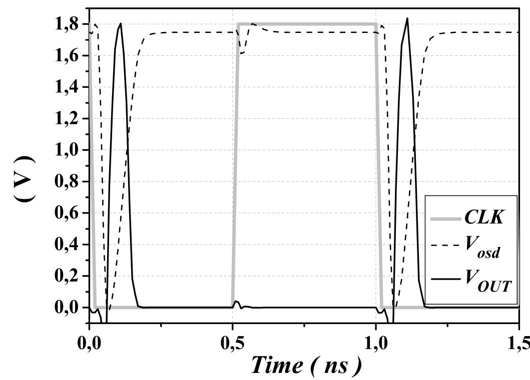
Monte Carlo analysis has been also performed. According to the information supplied by the technology of TSMC 0.18 μm and considering a gaussian distribution, the following tolerance parameters have been considered: threshold voltage (10%), gate oxide thickness (5%), transistor movilities (5%), channel width(10%) and channel length (10%). Figure 3.25 shows the results obtained for 40 Monte Carlo runs when $R_{defect} = 0\Omega$ and when $R_{defect} = 60\Omega$.



(a) Input Signal: SUT and Sref.

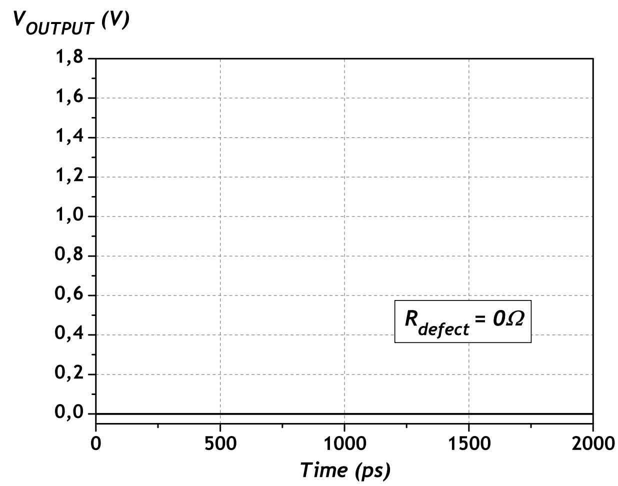


(b) V_{OUT} when $R_{defect} = 0\Omega$. Δt=0ps.

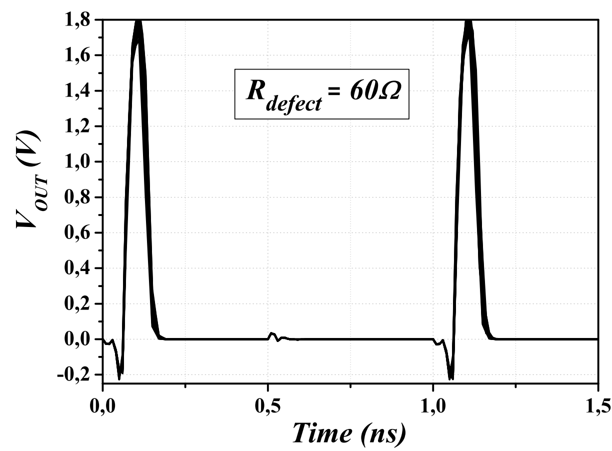


(c) V_{OUT} when $R_{defect} = 60\Omega$. Δt=25ps.

Figure 3.24: Simulation Result when $R_{defect} = 60\Omega$. ϕt < 1. Δt=25ps.



(a) V_{OUT} when $R_{defect} = 0\Omega$. Δt=0ps.



(b) V_{OUT} when $R_{defect} = 60\Omega$. Δt=10ps.

Figure 3.25: Monte Carlo Analysis. V_{OUT} when $R_{defect} = 0\Omega$ and when $R_{defect} = 60\Omega$.

3.4.3 Robustness to Power Supply Variations

For this work, the robustness conditions of the sensor to power supply variations are to avoid detect when there is no skew between SUT and Sref, and not lose a lot of resolution. Fig 3.26 shows a plot of the output voltage level of the sensor (V_{OUT}) against the skew between SUT and Sref for different voltage supply values values. It is observed the variation of sensor detection between the case for VDD $+10\%$ and VDD -10% is about 19ps. If another design specifications to VDD variations are required, the robustness could be improve adjusting the aspect ratio of control transistor, M3, β of feed backed inverter, INV1, and widths of sensing transistors, M1 and M2; in order to have major control over V_{σ}. Also, the length of PMOS and NMOS transistors of discriminating inverter could be increases. However, the resolution would be strongly compromised.

Fig. 3.27 shows the robustness of the sensor for process and power supply variations at the same time. 40 Monte Carlos runs have been performed. The upper bound is determined by the maximum variation to the left when VDD=1.98V (+10%). The lower bound is determined by the maximum variation to the right when VDD=1.62V (-10%). Thus, the total variation between the upper bound and the lower bound of the sensor detection is about 22ps.

3.4.4 Clock Feedthrough Analysis

One of the major issues coming from the use of CMOS switches us the called clock feedthrough effect[95][96][72]. This effect consists on the coupling of the clock signal transitions at output capacitance of the switch through its gate-drain or gate-source overlap capacitance. Fig 3.28 shows a MOS switch with overlap capacitor Cov and gnd capacitor Cgnd at node Vout. When clock signal undergoes from VDD to 0V, the switch are shutting off, Vout is high impedance and the capacitors Cov and Cgnd are isolated from the rest of the circuit. Hence, an error, ΔVe is introduced at node Vout and is given by,

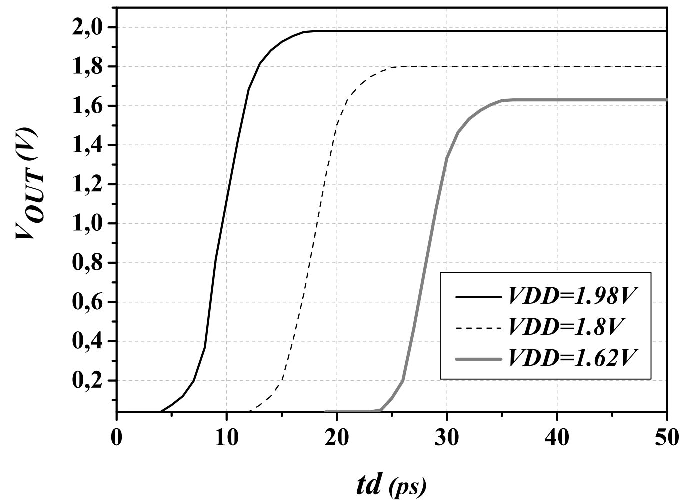


Figure 3.26: Resolution of the Negative Skew Sensor for different values of VDD. The variation between the case for VDD +10% and VDD-10% is about 15ps.

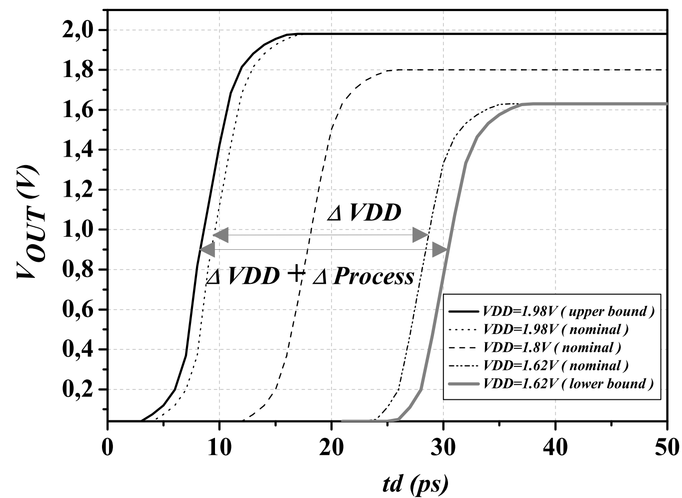


Figure 3.27: Resolution of the Negative Skew Sensor for process variations and VDD variations at the same time.

$$\Delta Ve = Vclk \frac{WCov}{WCov + Cgnd} \tag{3.32}$$

Where W is the width of MOS transistor and Cov is capacitance per unit width.

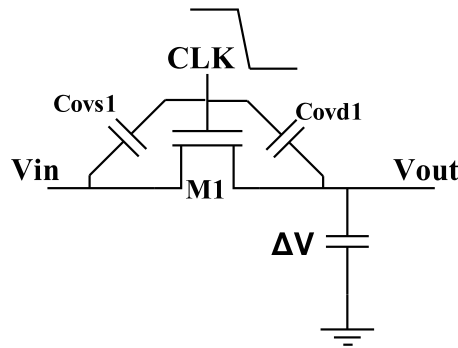


Figure 3.28: Clock feedthrough Effect.

Now, as the sensing transistors (M1 and M2) in the skew detector operates as switches, it is important to know if the clock feedthrough effect has a greater impact on V_σ. In order to know this, Figure 3.29 shows the system to analyze and is conforms by the two sensing transistors with their respective overlap capacitances (C_{ov1} and C_{ov2}). C_{inv} is the input capacitance to discriminating inverter. ΔVe is the error voltage introduced by clock feedthrough. The control signals for sensing transistors M1 and M2 are SUT and Sref respectively. The circuit of Fig 3.29 could be simplified by the circuit showed in Fig3.30. From this, ΔVe could be calculated by,

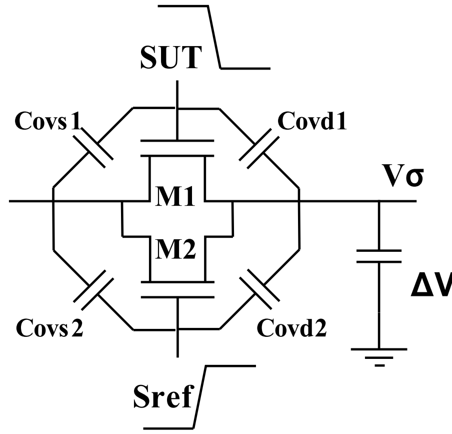


Figure 3.29: Clock Feedthrough analysis for sensing transistors.

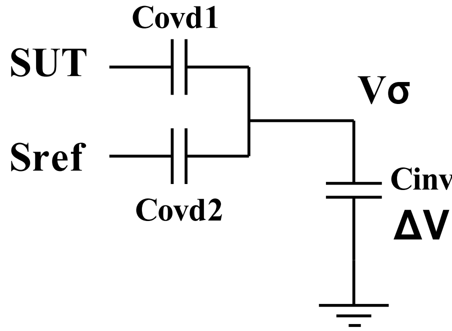


Figure 3.30: Circuit simplification for clock Feedthrough analysis for sensing transistors.

$$\Delta Ve = SUT\frac{W_{M1}C_{ov1}}{W_{M1}C_{ov1} + C_{inv}} + Sref\frac{W_{M2}C_{ov2}}{W_{M2}C_{ov2}} \tag{3.33}$$

Where W_{M1} and W_{M2} are the widths for M1 and M2 respectively. As W_{M1} = W_{M2}, doing $C_{ov1} \approx C_{ov2}$ and considering Sref = - SUT, ΔVe ideally cancels itself. Nevertheless, in real ΔVe is not zero, but because of small widths of sensing transistors (hence small overlap capacitances) and small C_{inv} due to small dimensions of discriminating inverter, ΔVe is not significant and practically does not affect V_σ value. Therefore in simulations performed, clock feedthrough is not appreciated.

3.5 Negative Skew Sensor Characterization

The minimum detectable skew between SUT(t) and Sref(t) could be modified by adjusting the design of sensor components.

In this section the sensor dependance on each component is presented.

3.5.1 Dependance on Discriminating Inverter

The threshold voltage of the discriminating inverter, V_{TH}^{INV2}, and the steady voltage at node V_σ, defines de acceptable skew window, W. Hence, V_{TH}^{INV2} is determined by β of INV2. Fig 3.31 shows this. It is observed how V_{TH}^{INV2} increases as β_{INV2} also increases. If a symmetric discriminating inverter is desired, β_{INV2} should be approximately 3.

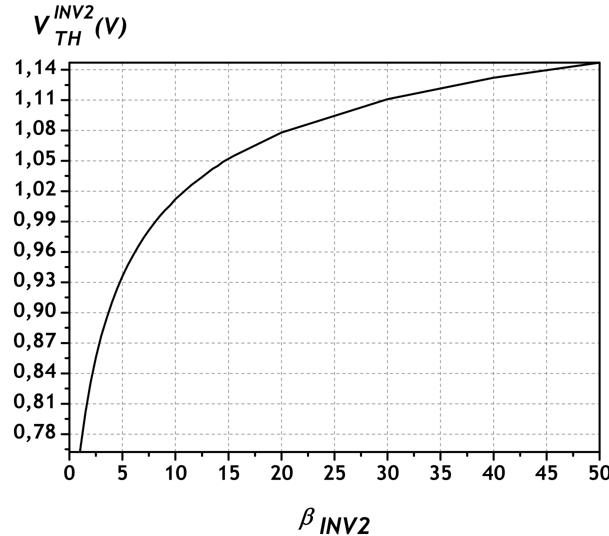


Figure 3.31: Relation between β_{INV2} with V_{TH}^{INV2}. As β_{INV2} increases, V_{TH}^{INV2} also increases. If β_{INV2} decreases, the minimum detectable skew also decreases.

As size of window W is determined by β_{INV2}, then, as a consequence the minimum detectable skew also depends on β_{INV2}, affecting the sensor resolution. Fig 3.32 shows a plot of the output voltage level of the sensor against the skew

between SUT and Sref for different β_{INV2} values. Also, the equivalent resistance value of defect (R_{defect}) associated with skew value is presented. Moreover, the corresponding percentage of void due to mass transport by electromigration is also showed. It is observed minimum detectable skew decreases as β_{INV2} decreases. This is due to the size of acceptable skew window decreases.

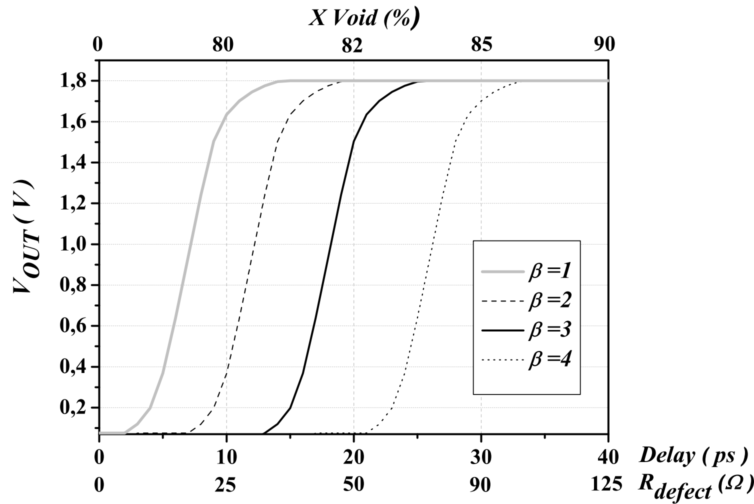


Figure 3.32: Sensor resolution against skew between SUT and Sref for different β_{INV2} values. Resolution is compromised as β_{INV2} increases.

3.5.2 Dependance on Feed Back Inverter

The β of the feed back inverter, INV1, sets the steady voltage level at node V_σ. Also, it influences on the gain of the skew detector because of INV1 functions as an amplifier. The gain of the skew detector defines the amount of ΔV voltage at node V_σ caused by the skew between SUT and Sref. Figure 3.33 shows the influence of β_{INV1} on node V_σ and on ΔV. It is observed V_σ increases as β_{INV1} increases. In the other hand, β_{INV1} has a lower impact on V_σ in spite of the influence on the gain of INV1.

According to this, β_{INV1} also affects the sensor resolution, due to the size of the

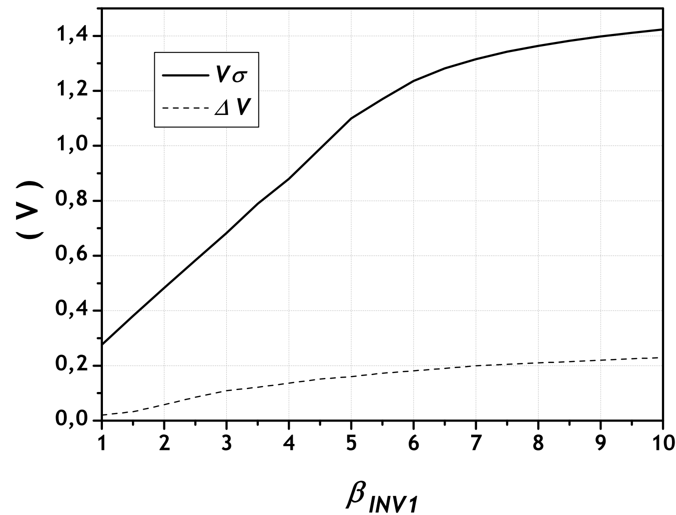


Figure 3.33: V_σ and ΔV dependance of β of INV1.

acceptable skew window is modified. Fig 3.34 shows this situation. As in Fig3.32, a plot of the output voltage level of the sensor (V_{OUT}) against the skew between SUT and Sref for different β_{INV1} values is plotted. Also, the equivalent resistance value of defect (R_{defect}) associated with skew value is presented. Moreover, the corresponding percentage of void due to mass transport by electromigration is also showed. It is observed minimum detectable skew increases as β_{INV1} decreases. This is due to the size of acceptable skew window increases.

3.5.3 Dependance on Sensing Transistors

Sensing transistors, Ms1 and Ms2, determine the speed of the skew detector. Also, V_σ is affected. If widths of M1 and M2 increases and due to the resistive divider, formed by resistance inverter, sensing transistor and control transistor, V_σ tends to decrease. Figure 3.35 shows the dependance of V_σ on widths of M1 and M2. In the same way, the dependance of ΔV with dimension of M1 and M2 is also shown in Figure 3.35. It is observed ΔV decreases slightly as dimensions of M1 and M2 increases and tends to a constant value.

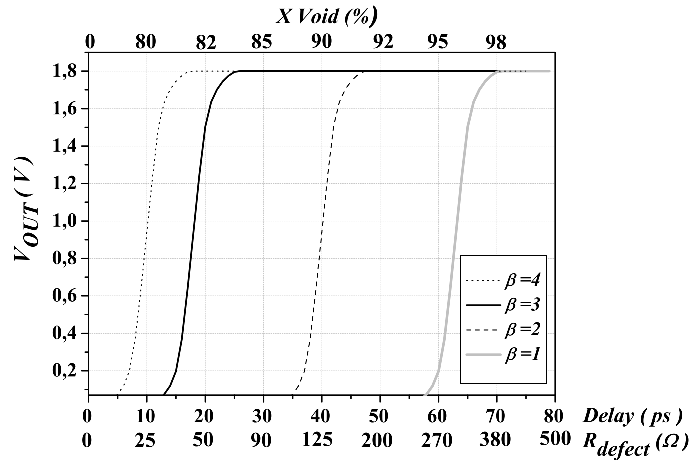


Figure 3.34: Sensor resolution against skew between SUT and Sref for different β_{INV1} values. Resolution is compromised as β_{INV1} decreases.

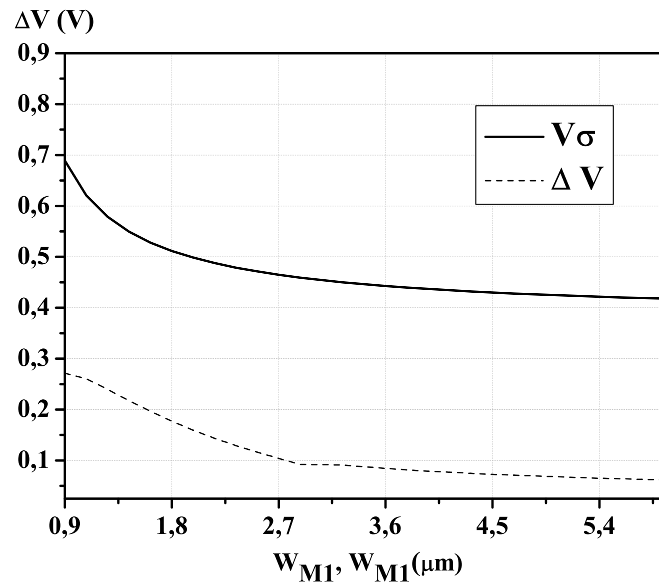


Figure 3.35: V_{σ} and ΔV dependance of dimensions of M1 and M2.

Figure 3.36 shows a plot of the output signal against the channel width of the sensing transistors. Each curve is constructed applying different skew conditions between the signals under analysis. It is observed for a desired detectable skew there is a maximum size of the sensing transistor allowing detection. This due to the fact that capacitance is added at both ends of the sensing transistors as their channel width increases. For channel widths less than 0.9μm, skew detector does not work correctly. Below this size the monitor detects both non acceptable and acceptable skews.

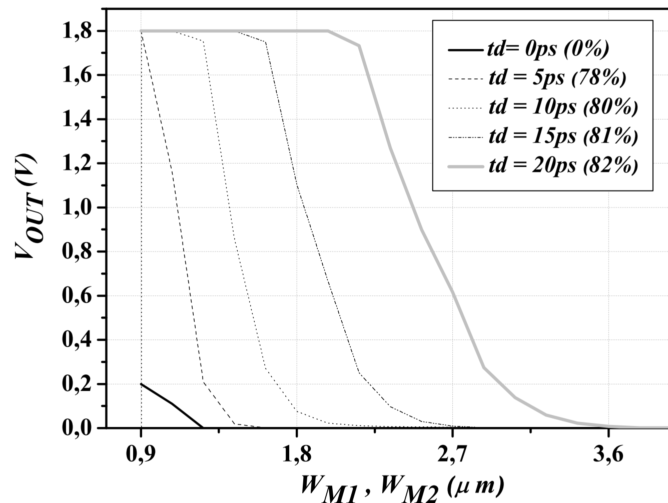


Figure 3.36: Sensor resolution against widths of sensing transistors. Resolution decreases as width increases. There is a tradeoff between speed and parasitic capacitances.

3.5.4 Dependence on the Control Transistor $M3$

As mentioned before, the control transistor, $M3$, influences the steady voltage value at node V_σ. Figure 3.37 shows this situation. It is observed, as aspect ratio (AR) of M3 increases, V_σ tends to be a constant value. This is due to Vds of M3 achieves a limit. This limit is because NMOS transistor of INV1 is off, V_σ always

will be charged to some level because of PMOS transistor of INV1.

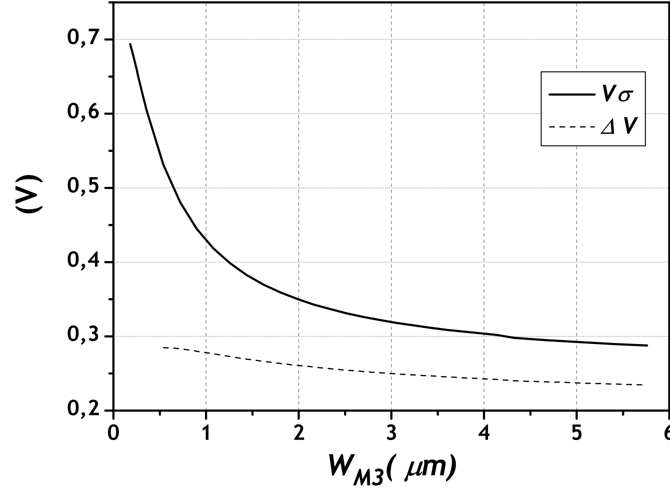


Figure 3.37: V_σ and ΔV dependance of dimensions of M3.

Also Figure 3.37 shows voltage (ΔV) at node $V\sigma$ has non significant dependence on the the control transistor. Fig 3.38 shows the voltage at the output of the sensor V_{OUTPUT} against the skew between SUT and Sref for different aspect ratios (AR) of the control transistor. Also, the equivalent resistance value of defect (R_{defect}) associated with skew value is presented. Moreover, the corresponding percentage of void due to mass transport by electromigration is also showed. It is observed as AR of M3 decreases (high resistance), the size of the acceptable skew window, W, also decreases and hence the minimum detectable skew decreases, improving the sensor resolution.

3.5.5 Dependence on Checking Transistors

The checking transistors charges the output of the skew detector affecting the resolution of the complete negative skew sensor. Figure 3.39 shows the voltage at the output of the sensor V_{OUT} against width of Mc1, Mc2 and Mc3 for different negative skew values between SUT and Sref. It is observed for a desired detectable

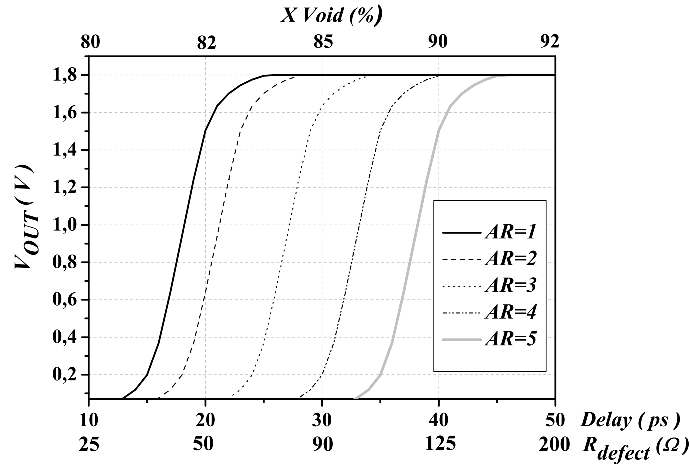


Figure 3.38: Sensor resolution against skew between SUT and Sref for different aspect ratios (AR)of M3. Minimum detectable skew increases as AR of M3 increases.

skew there is a maximum size of checking transistors allowing detection. This due to the fact that charge at output of skew detector increases as channel width of checking transistors increases.

3.6 Wear-Out Detection considering Process Variations Delay

The main reason for using two sensors is to differentiate small delays due to resistive defects from small delays due to process variations. Sref has been generated complementary to SUT and centered at a specific delay (td) value such that no skew exists with respect to SUT. Nevertheless, this case not always occurs owing to process variations. According to this, SUT and Sref delay could follow a normal distribution with same mean(μ_o) but different standard deviation (σ). *Sref* standard deviation (σ_{Sref})is considerably less than SUT standard deviation (σ_{SUT}) because of Sref is a signal reference. Fig 3.40 shows these distributions.

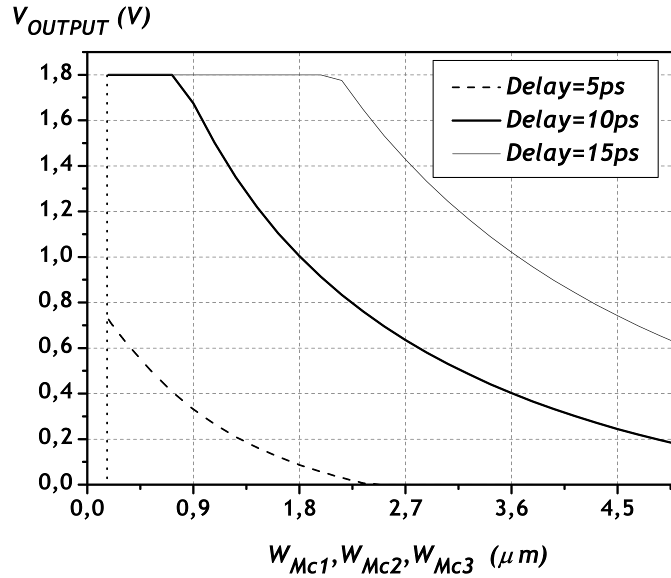


Figure 3.39: Sensor resolution against widths of checking transistors. Resolution decreases as width increases.

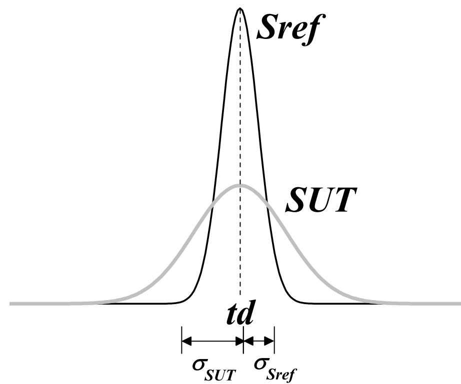


Figure 3.40: Delay Normal Distribution for SUT(t) and Sref(t). The mean are the same, td. But, $\sigma_{SUT} > \sigma_{Sref}$.

Taken into account SUT delay distribution at the just moment the circuit put on field , SUT delay may be any value on the left of *td* and if only Negative Skew Sensor is used, the sensor would detect an incorrect "wear-out" when there is

not any degradation. Remember that a defect generates a gradual interconnect wear-out due to workload and stress by electromigration and self heating. Fig 3.41 shows this case.

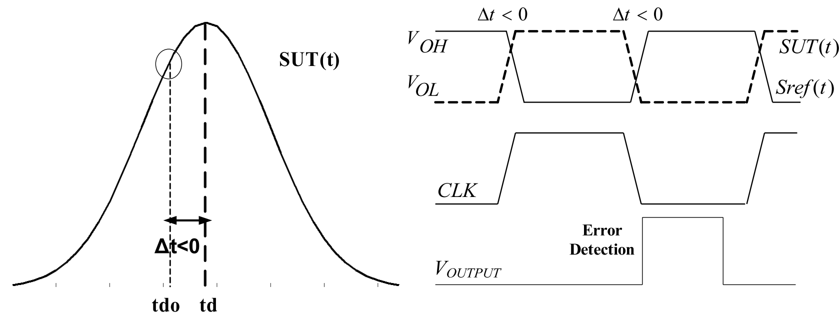


Figure 3.41: A case when an error detection of the negative skew sensor owing to process variations. Δt< 0 for this case is due to process variations and not to gradual degradation of a resistive defect.

Considering this detection condition, the resolution of the system could be compromised. Three possible cases could occur:

Initial SUT delay = *td*

In this case SUT delay is the mean value of its distribution and initially neither positive skew sensor nor negative skew sensor detect at all. According to defect transient behavior, as interconnect wear-out gradually increases, positive skew sensor detects first and after some extra workload time (resistive defect increases more), negative skew sensor also detects. When it occurs, interconnect wear-out is detected. Fig 3.42 shows the detectable region when both sensors are used. Under this conditions, the system with two sensors detect defects from $R_{defect} = 70\Omega$.

Fig 3.43 shows the full open predictable region when both sensors are used as function of remained lifetime (expressed in hours) of defective interconnect. It is observed the resolution of the system depends on the activity factor (α) of the node. Considering $V_{OUT} = 0.9V$ as a high logic level, for $\alpha = 1$ the system could

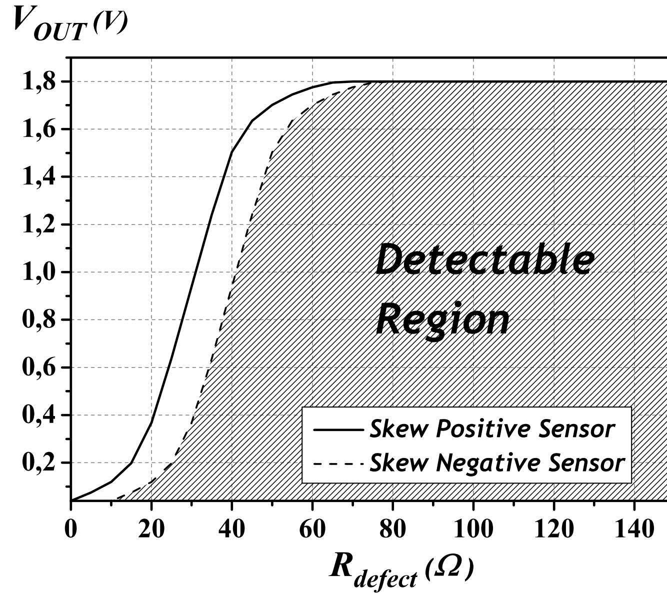


Figure 3.42: Detectable Region using the system with two sensors. Minimum detectable defect=70Ω

detect the defect approximately 100 hours before full open occurs. For $\alpha = 0.8$ the system detect the defect 200 hours before full open. For $\alpha = 0.6$ the defect is detected 350 hours before full open occurs and for $\alpha = 0.4$ the defect can be detected 700 hours before a full open occurs.

Initial SUT delay $<$ *td*

In this case SUT delay is less than mean value (see Fig 3.44). For this case, negative skew sensor always detects and as defect degradation gradually increases, delay (positive skew) at the end of interconnect (node after defect) will increase and thus the positive skew sensor will also detect. With respect to before case, a major defect degradation is necessary to be detected. Hence, the resolution is affected.

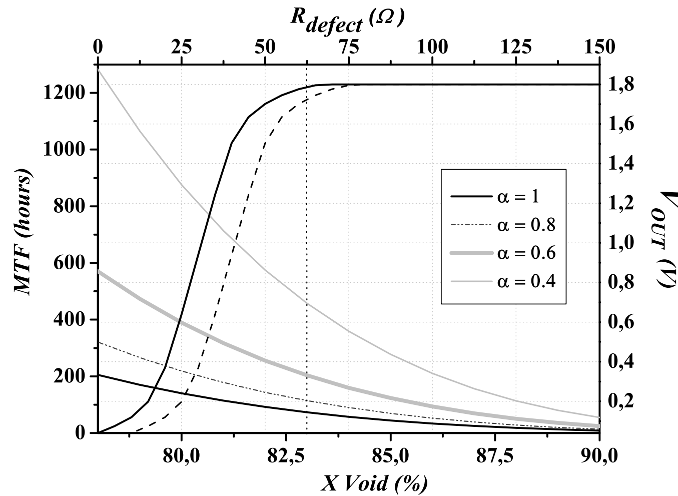


Figure 3.43: Predictable Region before a full open occurs for different activity factors.

Initial SUT delay > *td*

In this case SUT delay is greater than mean value (see Fig 3.45). For this case, positive skew sensor always detects and as defect degradation gradually increases, signal speed-up (negative skew) at the beginning of interconnect (node before defect) will increase and thus the negative skew sensor will also detect. Similar to before case, a major defect degradation is necessary to be detected and the resolution is also decreased.

Considering SUT delay due to process variations is a random variable, one way to estimate the resolution of the system is determining the detection probability of a continuous interval of resistance defect values when both positive skew sensor and negative skew sensor are used and taken into account SUT delay follows a normal distribution with mean in td. In other words, a probabilistic experiment is developed, where the random variable is SUT delay and an outcome is one wear-out detection (number of occurrences) of the system using both sensors for a specific resistance defect values interval. Hence, an histogram could be

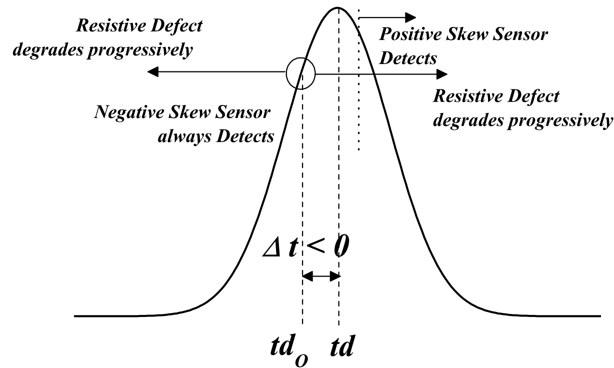


Figure 3.44: Case when initial SUT delay is less than td due to process variations. Negative skew sensor always detects.

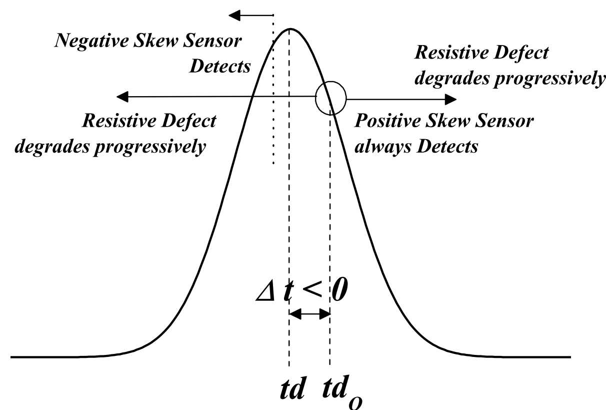


Figure 3.45: Case when initial SUT delay is greater than td due to process variations. Positive skew sensor always detects.

constructed and a probability for a specific defect interval could be estimated. To do this, a Montecarlo simulation was done to obtain random values of SUT delay. The mean of SUT delay distribution was 100ps with a standard deviation of 30%. The total of Monte Carlos was 300. Fig 3.46 shows the histogram constructed. From the results, the estimated probability the system detects from a resistance defect value between 65Ω and 85Ω (X void is approximately 85%)is 0.7, between 85Ω and 120Ω (X void is approximately 87%)is 0.4, between 120Ω and 150Ω (X void is approximately 90%)is 0.09 and between 150Ω and 200Ω (X void is more than 90%) is 0.03. According to this, using the system with two sensors, the resolution of detection of a specific resistive defect interval follows a Poisson process.

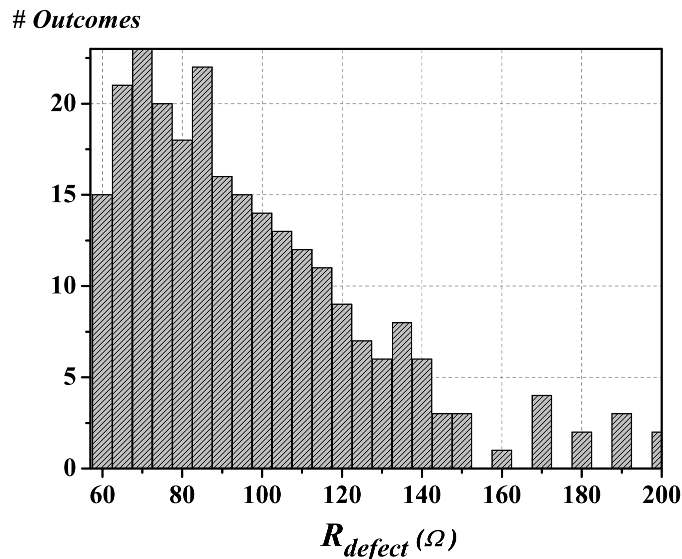


Figure 3.46: Histogram about resolution of the system when two sensors are used. The probability that system detect a defect in the interval between 65Ω and 85Ω is 0.7.

3.7 Cost of the proposed Wear-out Detection Methodology

The cost of the proposed wear-out detection methodology has been estimated in terms of delay penalization and area.

For delay penalization, two cases are considered: when only negative skew sensor is used and when both, positive skew sensor and negative skew sensor are used. Fig 3.47 shows the schematic diagram used for simulation. The interconnect capacitance per unit of length is 0.2fF/μm for TSMC 0.18μm. Interconnect lengths of 1mm, 2mm, 3mm, 4mm and 5mm are considered. The cascade buffer was designed to be able to drive an interconnect of 5mm (approximately 1000fF).

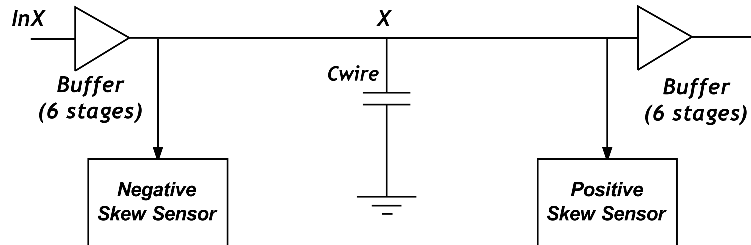


Figure 3.47: Schematic Diagram used to analyze the cost penalization of using one and two sensors

Table 3.3 shows the delay penalization in percentage for two cases mentioned. The delay penalization decreases for longer interconnect lines.

The area employed by each sensor is 12μm x 10μm (See Appendix B).

3.8 Conclusions

In this chapter a novel methodology for detecting small defects has been proposed. The verification strategy is based on the signal transient behavior in a defective interconnect at nodes before defect (negative skew) and after defect (positive skew). Therefore, under ideal conditions, a negative skew sensor based on addi-

Table 3.3: Delay penalization in % due to the implemented sensors

Length(mm)	One sensor	Two sensors
1	0.02436	0.0487
2	0.02011	0.0402
3	0.01781	0.0356
4	0.01637	0.0327
5	0.01536	0.0307

tion of complementary signals and located near the driver of interconnect (before defect node) has been proposed. The negative skew sensor is able to detect skews from 25ps in order to detect defects of 60Ω which represents approximately 83% of interconnect voiding due to gradual defect degradation owing to electromigration and self heating. Monte Carlo simulations, power supply variations and clock feedthrough analysis demonstrate the robustness of the sensor. In order to detect the exclusive behavior of a defect within a signal path, a positive skew sensor is added near the receiver. When both, negative and positive skew sensors are used, the detectable defect is 70Ω. In terms of Mean Time to Failure , the sensor is able to predict the defect before 100 hours before a catastrophic failure (full open interconnect) occurs when the node has an activity factor of 1; and 700 hours before when the node has an activity factor of 0.4. Considering process variations, the resolution on detecting small defects is compromised. Owing to randomness of process variations, the detection parameter change to be probabilistic, therefore the resolution of the sensor is estimated in a probabilistic way. Thus, the probability to detect defects less than 100Ω (approximately 86% of interconnect voiding) is 0.75. The cost of the proposed system verification strategy has been estimated in terms of delay penalization. For each sensing interconnect the added capacitance due to input gate capacitance of sensing transistor of the sensor is

about 3.6fF. Assuming a interconnect of 1mm the added delay due to one sensor corresponds to 0.02436% of the total signal delay; a for two sensors the added delay corresponds to 0.0487% of the total signal delay. Moreover, as interconnect length increases (2mm, 3mm, 4mm , 5mm), delay penalization decreases. Finally, the estimated area for each sensor is 12μm x 10μm.

Chapter 4

Transistor Aging Monitoring

The scaling trends of CMOS technology and operating conditions give rise to serious degradation mechanisms such as Negative Bias Temperature Instability (NBTI) and Hot Carriers Injection (HCI) in MOSFETs. These effects produce transistor aging and threat circuits lifetime. The aging phenomena is considered a major reliability issue according to International Technology Roadmap for Semiconductors (ITRS). MOSFETs age during operation due to stress and workload. NBTI and HCI degradation depends on field conditions: supply voltage, temperature and switching activity factor of the node. Therefore, in this chapter a novel built-in aging sensor is presented. The monitoring strategy consists on verify the delay generated due to aging in a combinational circuit. Output signals of combinational circuits are captured by storage elements, as flip-flops (FF). The proposed built-in aging sensor is inserted in parallel to the FF connected to the output of a combinational circuit in order to detects a signal transition during a guardband interval (T_g). This situation occurs when there is a significant delay at combinational circuit due to aging. Nevertheless, FF will still continue to capture the correct logic value from the combinational logic. Considering this, the detection strategy can be considered a circuit failure prediction technique.

The rest of the chapter is organized as follows: in section 4.1 transistor aging

sources are presented. HCI and NBTI physics are explained and their impact on circuit-level is discussed. Next, the proposed built-in aging sensor is presented in section 4.2. In Section 4.3 sensor performance is presented. In section 4.4 the cost of the proposed sensor is evaluated. Finally, the conclusions of the chapter are given in section 4.5.

4.1 Transistor Aging Sources

4.1.1 Hot Carrier Injection

Hot carrier damage has been one of the important degradation mechanism of MOSFET transistor [24]. It is one of the major oxide failure mechanisms, that occurs when the transistor electric field at the drain-to-channel depletion region is too high [71]. Hot Carrier Injection (HCI) is a systematic failure that compromised circuit timing performance of the IC. HCI can happen if the power supply voltage is higher than intended for the design, the effective channel lengths is too short, there is a poor oxide interface or poorly designed drain-substrate junctions [71][25][97][98][99]. Considering an NMOS transistor (See Fig. 4.1), the horizontal electric field in the channel (ε_{ch}) gives kinetic energy to the free electrons moving from the inverted portion of the channel (source) to the drain.

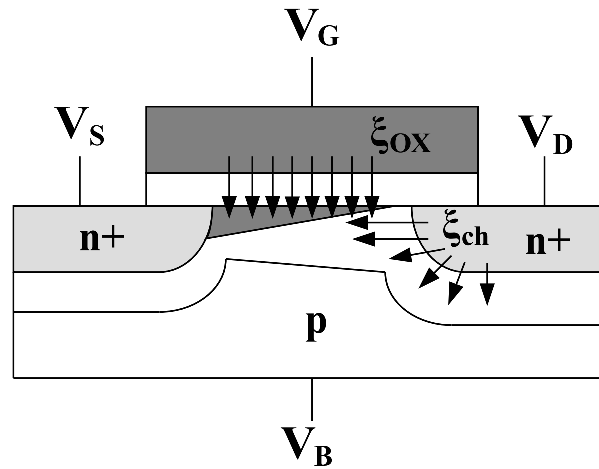


Figure 4.1: NMOS transistor and its internal electric fields.

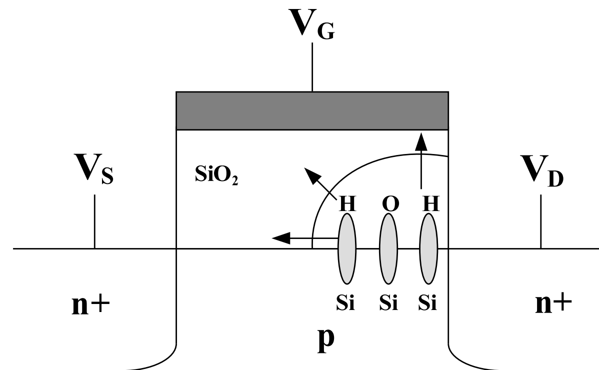


Figure 4.2: Traps originated at the region of the gate over the drain.

When the kinetic energy is high enough, electrons strike Si atoms around the drain-substrate interface causing electron-hole pairs by impact ionization. Some carrier (in this case holes) go into the substrate causing an increase in substrate current (I_{SUB}), and a small number of carriers (in this case electrons) have enough energy (3.1eV for electrons and 4.6 for holes [71])and can overcome the energy barrier at the Si-SiO_2 interface and be injected into the oxide causing threshold voltage shift and increment in gate current leakage (I_G). Some energetic injected carriers might break some Si-H bonds leading to acceptor-type (trivalent

Si) interface trap formation near the drain. If the silicon and hydrogen recombine, then no interface trap is created, but if hydrogen diffuses away, then an interface trap is created. Fig. 4.2 illustrates this. According to [24] there are three types of HCI modes:

1. *Channel Hot Electron (CHE) Injection*: This occurs when the gate voltage (V_G) is comparable to the drain voltage (V_D). Electrons from the channel can escape by obtaining sufficient energy to cross Si-SiO_2 interface without suffering any energy-losing collision (See Fig. 4.3). They forms the main part of gate current and cause a significant degradation of the oxide especially at ambient low temperature, where the mobility of electrons are greater.

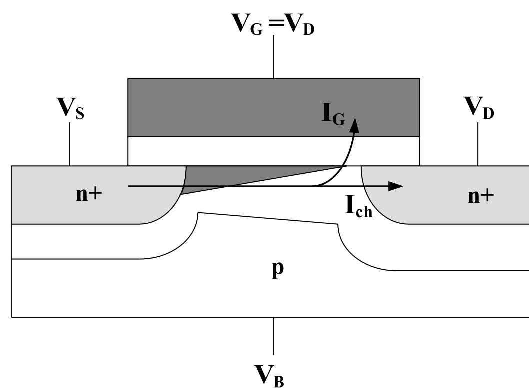


Figure 4.3: Channel Hot Electron Injection (CHE).

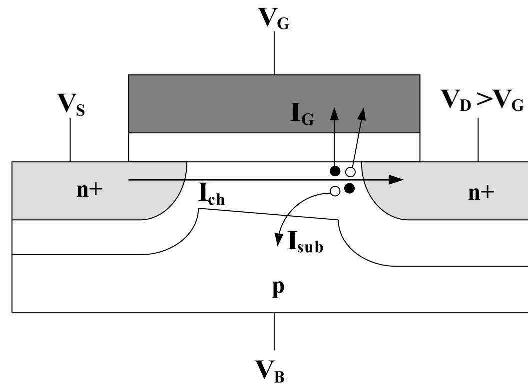


Figure 4.4: Drain avalanche hot carrier (DAHC)).

2. *Drain avalanche hot carrier (DAHC) injection*: This occurs when V_D is larger than V_G. The electric field at the drain intensifies to the point where avalanche multiplication due to impact ionization increasing the number of both, hot electrons and hot holes, and they are injected to oxide in the same way as CHE (See Fig. 4.4).

3. *Secondary generated hot electron (SGHE) injection*: This mechanism occurs when the electric field is very high and the generated hot carriers are able to cause secondary impact ionization in the depletion region during its journey to the substrate (See Fig. 4.5). The electrons generated due to secondary impact ionization can also be injected into the gate and cause degradation. It only becomes a problem in ultra-small devices.

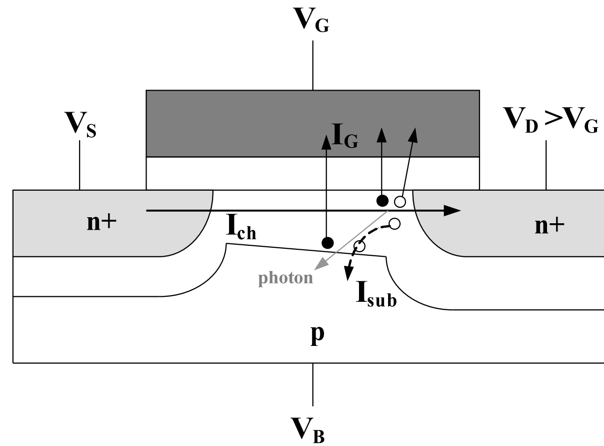


Figure 4.5: Secondary generated hot electron (SGHE)).

The transistor parameters affected due to HCI are: I_{Dsat}, transconductance (gm), threshold voltage (V_{TH}), weak subthreshold slope(S-I_{off} decreases) and increased gate induced drain leakage (GIDL). Fig. 4.6 shows the process of HCI.

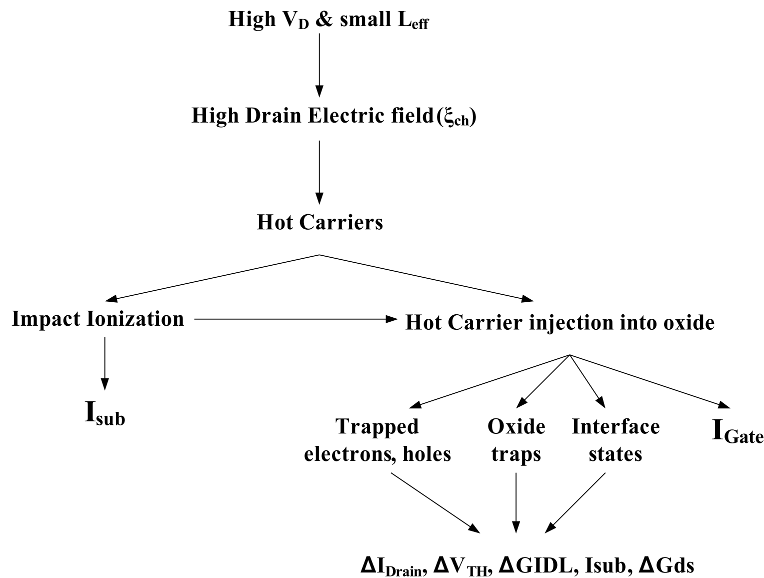


Figure 4.6: Hot Carrier Process.

In practice, the I_{Dsat} parameter is typically used to measure HCI degradation because it is the parameter that most closely approximates the impact on circuit

speed causing the decreases of maximum operating frequency (F_{max}). Nevertheless, the degradation of I_{Dsat} due to HCI is slightly [71]. This is owing to the oxide damage takes place dominantly in the oxide over the drain-depletion-substrate-depletion when the transistor operates in the saturation region (See Figure 4.2), and that only occurs during logic transitions (switching). Therefore, if HCI damage is present, i.e in a NMOS transistor oxide, then V_{THn} increases only in the drain depletion region which may affect F_{max} occurs when HCI is severe. In order to monitor hot carrier damage, I_{SUB} is measured because it reflects the energy of the hot electrons.

Finally, HCI oxide failure mechanism is severer for NMOS than for PMOS transistors [97][24][99][22] because electrons are more efficient in impact ionization [100] due to its mobility and longer free path owing to their lighter effective mass compared to holes.

4.1.2 Negative Bias Temperature Instability-NBTI

NBTI physics

Negative Bias Temperature Instability is a significant reliability concern for digital and analog circuits in current CMOS technologies [97]. NBTI occurs to PMOS devices under negative gate voltages ($V_{GS} < 0V$) at elevated temperatures and is a consequence of interface trap generation at the *Si/oxide* interface which increases the threshold voltage (V_{THp}), reduce the channel mobility due to scattering, induce parasitic capacitances in the transistors, and reduces the drain current (I_{on}) and transconductance (gm) of the PMOS transistor. The NBTI effect is severer for PMOS transistor than PBTI effect for NMOS transistor due to the presence of holes in PMOS inversion layer that are known to interact with the oxide states.

In conventional *Si* MOSFETs, transistors are annealed in hydrogen ambient in order to passivate the dangling *Si* bonds during manufacture [101][97]. Hence,

Si-H bonds are formed at *Si*-SiO_2 interface(See Fig.4.7).

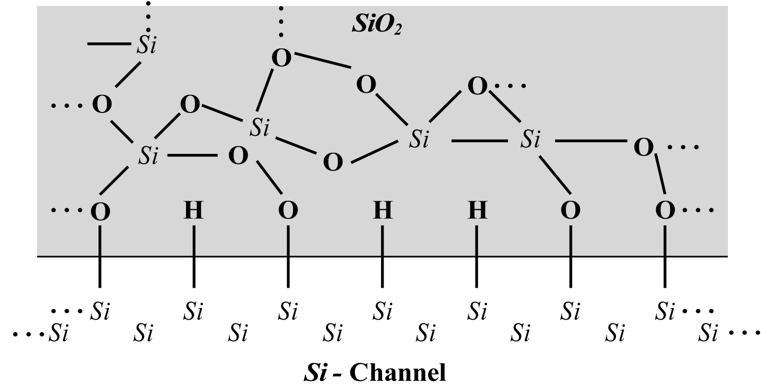


Figure 4.7: Schematic of the Si/SiO_2. Si-H bonds are formed.

In a PMOS device, the holes from the channel inverted layer can enter into the oxide through tunneling process and interact with *Si-H* bonds. This interaction may weaken these bonds. Due to higher operation temperatures, these bonds may break at the interface over time during device operation. This condition worsens with the scaling technology trends, such as the aggressive oxide thickness scaling which leads to higher oxide field and process modifications such as nitridation of oxides to prevent Boron diffusion from p+ poly gate. The electro-mechanical reaction which breaks *Si-H* bonds is explained by the Reaction-Diffusion (R-D) model [24][97][102][103], where the follow chemical reaction takes place,

$$Si\text{-}H + h^+ \longleftrightarrow Si^\star + H^0 \qquad (4.1)$$

In Eq. 4.1, an inversion layer hole, h^+, weakens *Si-H* bond and hydrogen is detached as a result of thermal vibration of the chemical bond [97][104][105]. The remaining *Si* dangling bond ($Si^\star$) acts as a donor interface trap (N_{IT})[97][99]. The hydrogen, H, diffuses away from the *Si*-SiO_2 interface freely or forms H_2 with another H, generating fixed positive interface charges (N_H). Fig.4.8 illustrates this R-D process.

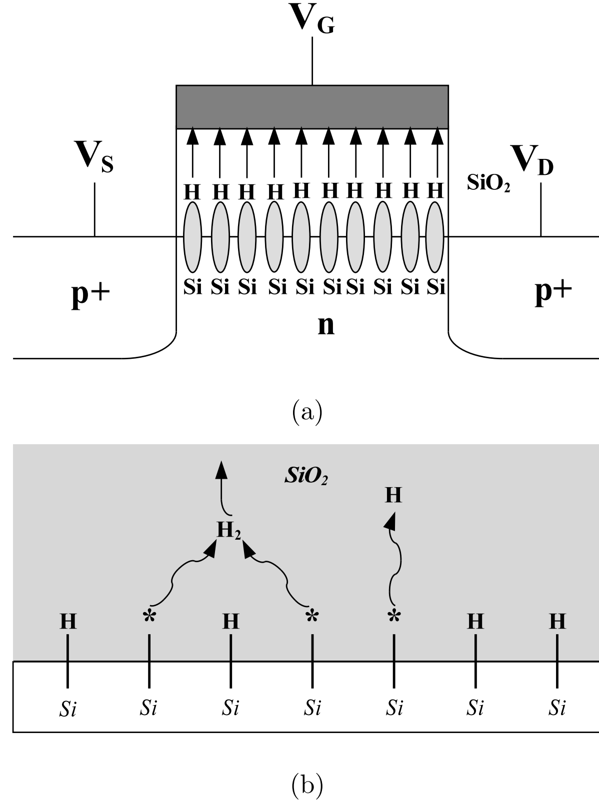


Figure 4.8: Hydrogen dynamics and traps originated when Si-H bonds breaks. $*$ represents traps.

According to [106], the threshold voltage for PMOS transistor is given by,

$$V_{THp} = V_{FB} - 2\phi_F - \frac{|Q_B|}{C_{ox}} \tag{4.2}$$

Where V_{FB} is the flat band voltage and is given by,

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} \tag{4.3}$$

Where Q_{it} is the interface trapped charge density and Q_f is the fixed oxide charge. Therefore, as consequence of NBTI, an increase of trapped charge density (N_{IT})and fixed positive charge density (N_H) lead to an increase of Q_{it} and Q_f respectively and thus and increase of the PMOS threshold voltage (more negative) V_{THp}.

NBTI impact on Circuits

NBTI primarily affects the PMOS devices and can result in up to 50mV shifts in threshold voltage over a period of ten years, translating to more than 20% degradation in circuit speed or in extreme in functional failures [107][108][109]. Also, in [110] it was demonstrated that NBTI degradation have a direct impact on the critical speed path (f_{max}) of a circuit. Therefore, an analysis of the impact of NBTI on digital and analog circuits are development in [111][109][97][112][103]. Nevertheless, an accurate prediction of circuit performance degradation due to NBTI should include the dependance on V_{DD} and temperature but more importantly, the switching activity factor of the node.

The drain current is important in analog and digital circuits. For instance, in digital circuits, with MOSFETS being switches, charging and discharging capacitors, higher drain current leads to faster capacitor charging and higher frequency operation. Hence, the delay (t_d) is given by [103],

$$t_d = \frac{C|V_{DD}|}{I_D} = \frac{2LC|V_{DD}|}{W\mu_{eff}C_{ox}(V_{DD} - V_{THp})^2} \tag{4.4}$$

Where C is the load capacitance and V_{DD} is the supply voltage. NBTI stress leads to μ_{eff} reduction and V_{THp} increases, hence the delay also increases. In analog circuits the drain current is also important but also the transconductance (gm) which is also affected by μ_{eff} reduction and V_{THp} increase. The fractional change of drain current due to threshold voltage change is [103],

$$I_D \approx \frac{W\mu_{eff}C_{ox}}{L}(V_{GS} - V_{THp})V_D \Rightarrow \frac{1}{I_D}\frac{dI_d}{dV_{THp}} = -\frac{\Delta V_{THp}}{V_{GS} - V_{THp}} \tag{4.5}$$

for PMOS transistors in the linear region and,

$$I_{Dsat} \approx \frac{W\mu_{eff}C_{ox}}{2L}(V_{GS} - V_{THp})^2 \Rightarrow \frac{1}{I_D}\frac{dI_d}{dV_{THp}} = -\frac{2\Delta V_{THp}}{V_{GS} - V_{THp}} \tag{4.6}$$

for the saturation region.

Another effect that occurs due to NBTI degradation is an increased gate-to-drain overlap capacitance due to generated interface traps. C_{DG} degrades analog circuits due to the Miller effect. For instance, C_{DG} increase degrades the frequency response of an operational amplifier. Hence, C_{DG} degradation is severer in analog circuits than digital circuits.

The one parameter that appears to be positively influenced by NBTI is the leakage drain current. The leakage current (I_{off}) for a PMOS is given by [103]

$$I_{off} = I_T exp\left(\frac{qV_{THp}}{nkT}\right) \tag{4.7}$$

Where I_T and K are constants and T is the temperature. As V_{THp} becomes more negative, I_{off} decreases.

In digital circuits, the effects of NBTI can be very complex. For example, delays of different paths on the same chip or different paths on different chips can degrade very differently. This can lead to changes in timing critical paths over time [53]. For instance, a critical path which is not timing critical right after manufacture may become timing critical later[53]. Moreover, the dominant NBTI degradation occurs during the static CMOS operation (steady-stage degradation) when PMOS transistor in ON [111][109]. Fig. 4.9 illustrates this. When VIN is 0, PMOS transistor is stressed and when VIN is VDD PMOS is off and is relaxed. This consideration is taken into account for the transistor aging sensor proposed in next section.

4.2 Transistor Aging Sensor

According to previous section, HCI and NBTI are the major sources of PMOS transistor aging, causing an increment in propagation delay in combinational circuit paths. Similar to wear-out at interconnects due to electromigration, on-line self test is needed in order to detect aging degradation in digital circuits.

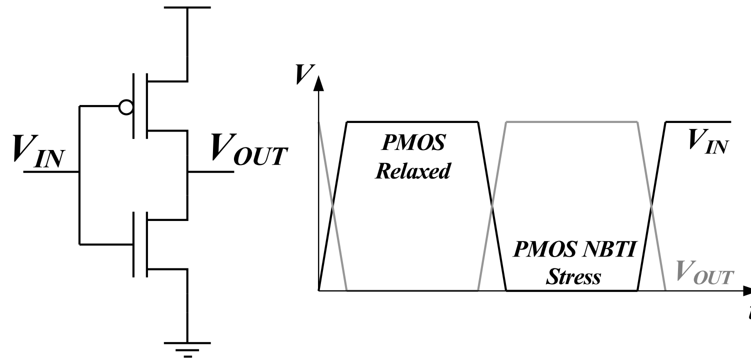


Figure 4.9: NBTI stress for digital circuits.

CASP [93], which was explained in previous chapter, is also the on-line self test system suggested to use for aging monitoring. CASP is in charge of to test on core while the rest of the system continues operating. When the core or circuit of interest is in test mode, CASP turns on aging sensors. In this chapter a new aging sensor is proposed. Similar to previous chapter, the aging monitoring is oriented to automotive application. Thus, the aging sensor could be activated by CASP at each moment that a car is turned on.

Output signals of combinational circuits are captured by storage elements, as flip-flops (FF). Similar to [53][46], the proposed built-in aging sensor is inserted in parallel to the FF connected to the output of a combinational circuit in order to detects a signal transition during a guardband interval (T_g). This situation occurs when there is a significant delay at combinational circuit due to transistor aging (guardband violation). Fig. 4.10 illustrate this condition. Assuming rise-edge triggered FF, it is observed from Fig. 4.10 that in spite of a guardband violation, the FF will still continue to capture the correct logic value from the combinational logic. Considering this, the detection strategy can be considered a circuit failure prediction technique [53][46].

Fig. 4.11 shows the block diagram of the proposed methodology. It is conforms by a guardband generator (GBG) and by a transition discriminator (TSD). The aging sensor have an ON-OFF mechanism by means of On-S signal. When On-

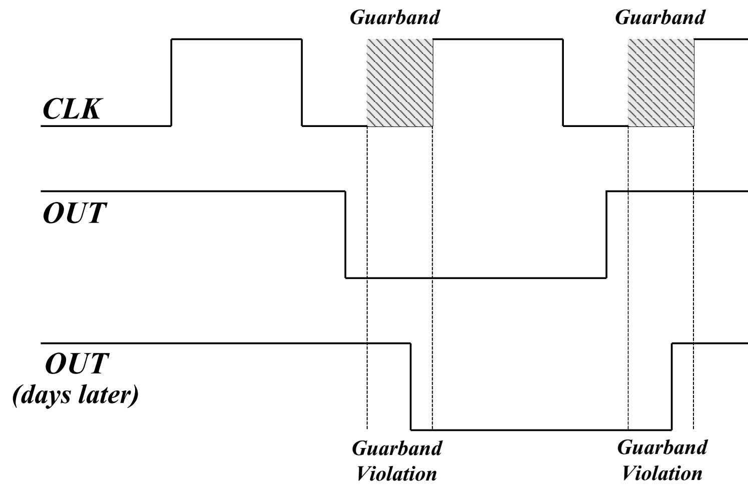


Figure 4.10: Transition of combinational logic output inside guardband.

S=1 the sensor is off in order the makes sensor itself resilient to aging. When On-S=0, sensor is on, guardband interval is generated by GBG and TSD is in charge of checking if the output of the combinational logic (OUT_{CL}) makes a transition during guardband interval. When a guardband violation occurs the out of the aging sensor (OUT) presents a pulse from high to low level.

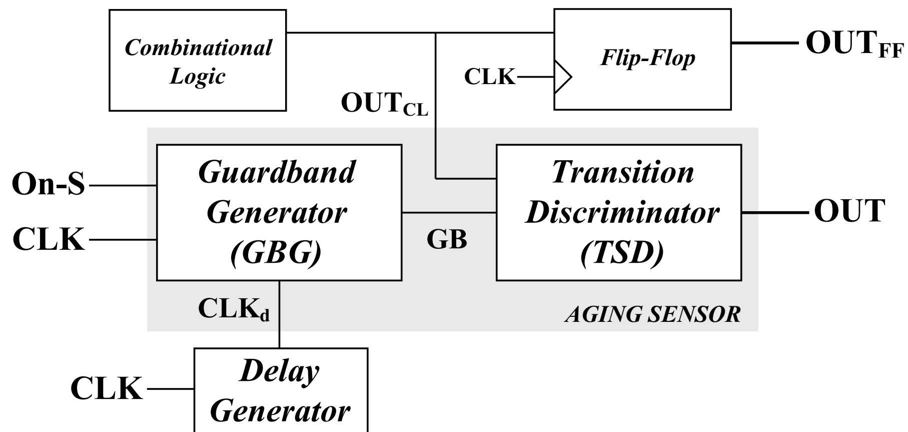


Figure 4.11: Proposed Aging Sensor.

4.2.1 Guardband Generator

The schematic diagram of the GBG is shown in Fig. 4.12. The skew detector described in chapter 3 is used, with the difference that INV2 is eliminated. The inputs to GBG are the signal clock (CLK) of the FF and a delayed clock signal (CLK_d) which can be generated from either delay generator. The skew between CLK and CLK_d makes the skew detector to generated a pulse (GB) exactly located before the rise edge of CLK. This pulse represents the guardband interval. For this, the CLK_d is delayed $T_{CLK}/2$ - T_g from CLK. T_g is defined according to the maximum delay propagation of the combinational circuit. In contrast to [53][46] (where the guardband interval is generated from a virtual and temporal XOR operation between $\overline{CLK}$ and delayed $\overline{CLK}$), the guardband is a electrical signal. This is in order to obtain a guardband with high robustness to PVT variations. Moreover, T_g will be low-dependant of PVT variations of the delay generator circuit. The GBG description is the same performed in Chapter 3 for the Skew Detector.

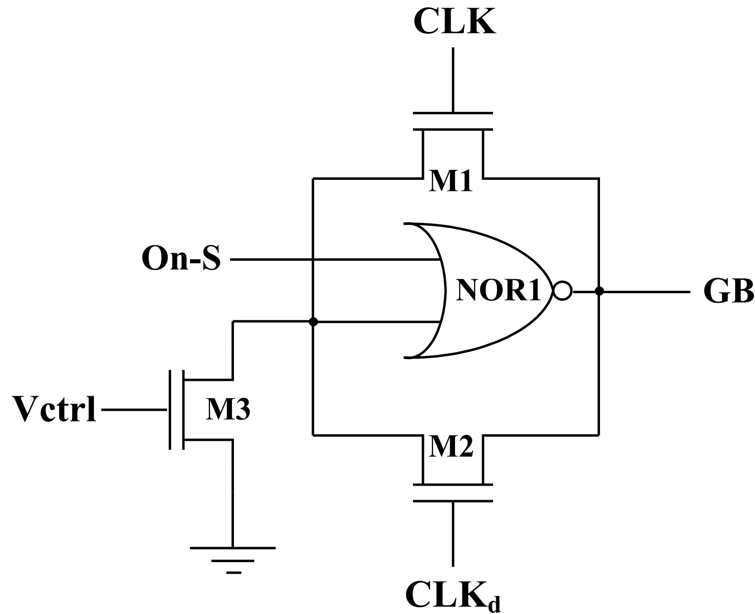


Figure 4.12: Schematic Diagram of Guardband Generator.

4.2.2 Transition Discriminator I

Fig. 4.13 shows the schematic diagram of the transition discriminator (TSD). TSD implementation is a simplified version of the stability checker presented in [53] and [46], due to guardband interval generation procedure. TSD can detect any transition at the output of the combinational circuit inside the guardband interval (T_g). The detection operation consists of two phases: *precharge phase* and *evaluation phase*. The *precharge phase* is established when T_g is set to 0. PMOS(NMOS) transistor M4(M6) and M5(M7) are ON(OFF), nodes a and b are set to VDD and the TSD output (NOR gate) is 0 (OUT=0). The *evaluation phase* starts when T_g=1. NMOS(PMOS) transistors M6(M4) and M7(M5) are ON(OFF). M8 and M9 receives at their gates the output of the combinational circuit (OUT_{CL}). Inverter INV4 allows TSD to detect both transitions. Thus, when OUT_{CL} transitions from 0 to 1 or from 1 to 0 once or multiple times, nodes a and b discharge to GND and OUT changes to 1 because of NOR gate.

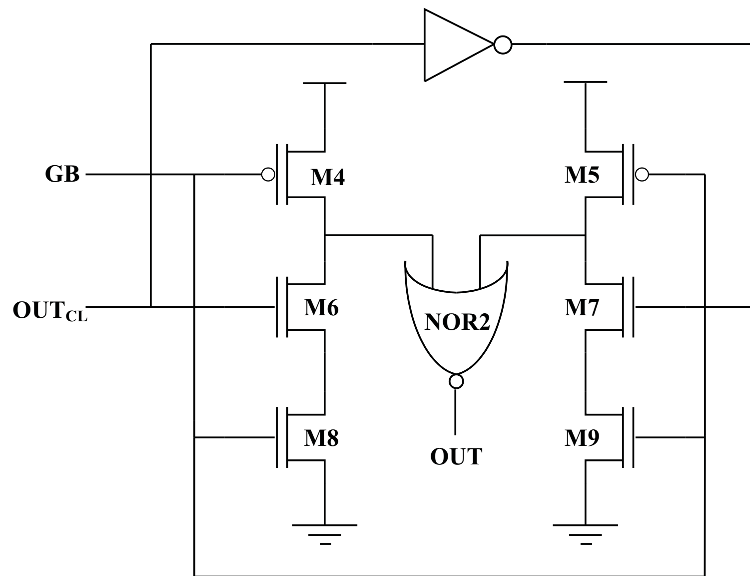
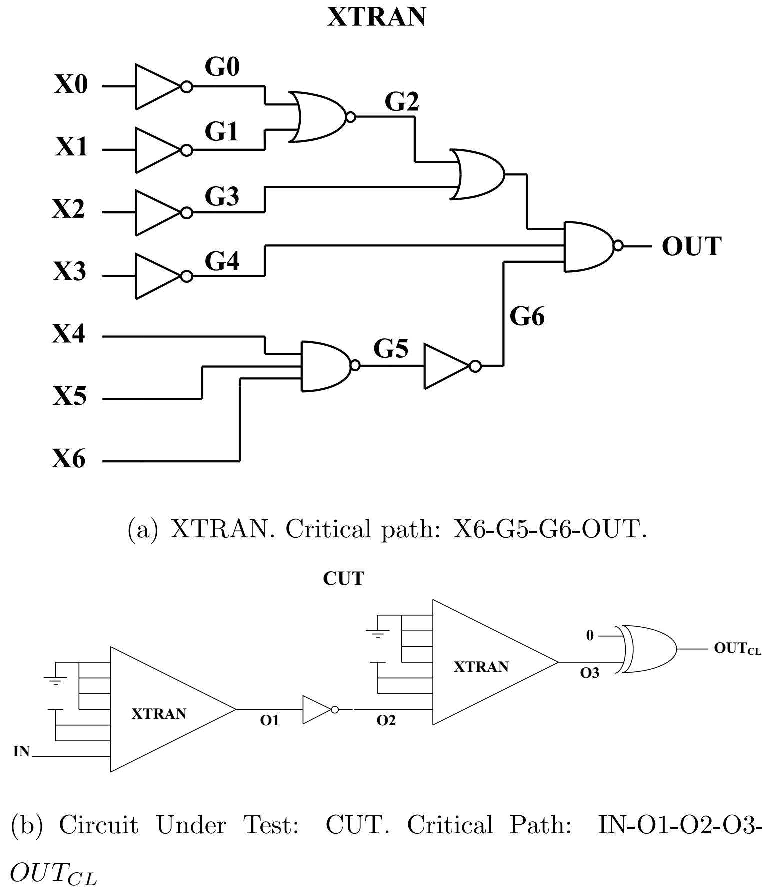


Figure 4.13: Schematic Diagram of Transition Discriminator.

4.3 Sensor Performance

In order to evaluate the proposed sensor, a simple combinational circuit, CUT (Circuit Under Test), based on a combinational cone of an industrial design XTRAN (a fleet management system from $Tecmic^{TM}$) is used. Fig. 4.14a and 4.14b show one XTRAN cone and CUT respectively. The critical of these two structures are also indicated.



(a) XTRAN. Critical path: X6-G5-G6-OUT.

(b) Circuit Under Test: CUT. Critical Path: IN-O1-O2-O3-OUT_{CL}

Figure 4.14:

The guardband interval (T_g) definition depends on the maximum propagation delay (critical path) of the CUT. Under normal VT conditions (VDD=1.8V, T=27C), the propagation delay time of CUT is t_{PLH} = 612ps in the critical path (t_{PLH} is the slowest transition). However, the maximum propagation delay is

defined under worst case VT conditions (VDD=1.62V, T=180C). Hence, $t_{PLH} =$ 1.16ns. The clock period is defined as $T_{clk} = \tau_0 + \tau_{slack}$, where $\tau_0 = t_{PLH} + t_{set-up}$, and t_{set-up} is the set-up time of the flip flop (FF) which is $50ps$. Taking into account process variations, the time slack was set to 30% of τ_0. Thus, T_{clk} is 1.6ns. Finally, the maximum T_g is given by $T_g = T_{clk}/2 - t_{PLH}$. Simulations were carried out to compute propagation delay degradation due to aging (NBTI, HCI). Therefore, the threshold voltage of PMOS transistors (V_{THp}) of the CUT have been varied and the impact on t_{PHL} has been evaluated.

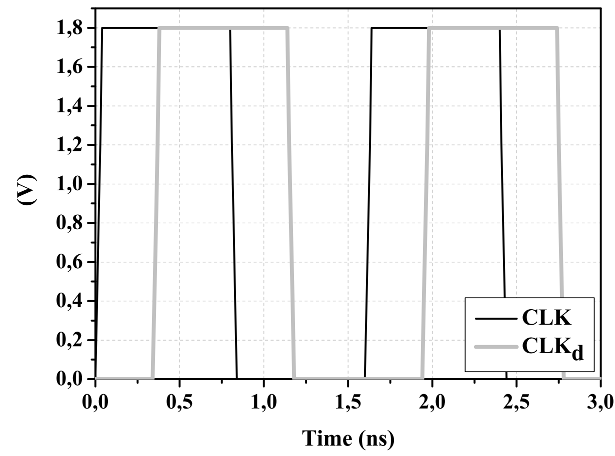
TSMC 0.18μm CMOS technology is used to evaluate the aging sensor performance. The transistor channel widths are indicated in Table 4.1. Channel length for all transistors are the minimum allowed by the technology (0.18μm). Inverters (INV1, INV2, INV3 and INV4) are symmetric. V_{ctrl} of M3 is fitted to 1.8V. Electrical simulations has been made in HSpice.

Table 4.1: Channel Widths of transistor of the Aging Sensor

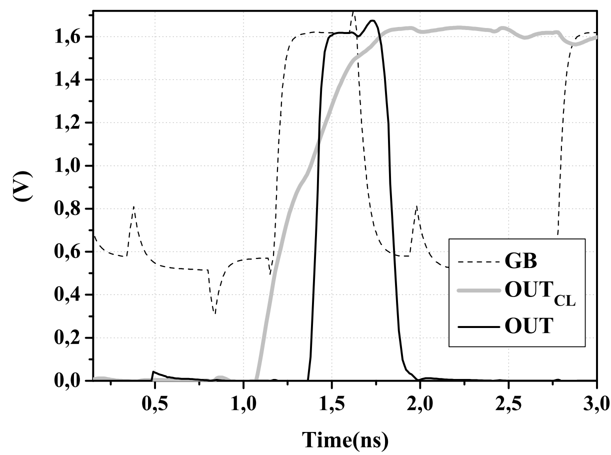
Device	Width (μm)	Device	Width (μm)
M1	1.62	M7	0.36
M2	1.62	M8	0.36
M3	0.28	M9	0.36
M4	0.36	NOR1	$\beta = \frac{1.62}{0.54}$
M5	0.36	INV3	$\beta = \frac{1.62}{0.54}$
M6	0.36	NOR2	$\beta = \frac{0.72}{0.36}$

Fig. 4.15 shows the simulation results for $\Delta V_{THp} = 15\%$ under worst case conditions (VDD=1.62V,T=180^oC). The signals showed are: clock signal (CLK), delayed clock signal (CLK_d), guardband interval (GB), combinational circuit output (OUT_{CL}) and TSD output (OUT). The delay propagation, t_{PLH}, is 1.36ns. Thus OUT_{CL} transitions inside GB makes OUT changes from 0 to 1.

Figure 4.16 shows the guardband interval (GB) variations due to VDD and



(a) Clock Signal: CLK and CLK_d.



(b) GB, OUT_{CL} and OUT

Figure 4.15: Simulation Result VDD=1.62V, T=180^oC.

Temperature variations for the proposed sensor. The maximum guardband variation is 27ps.

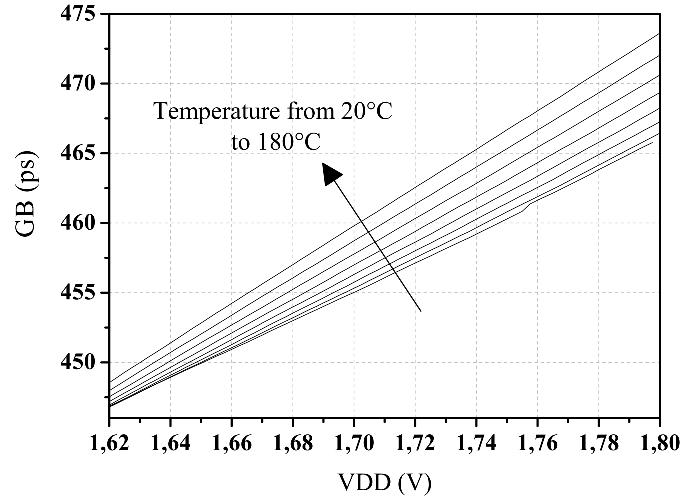
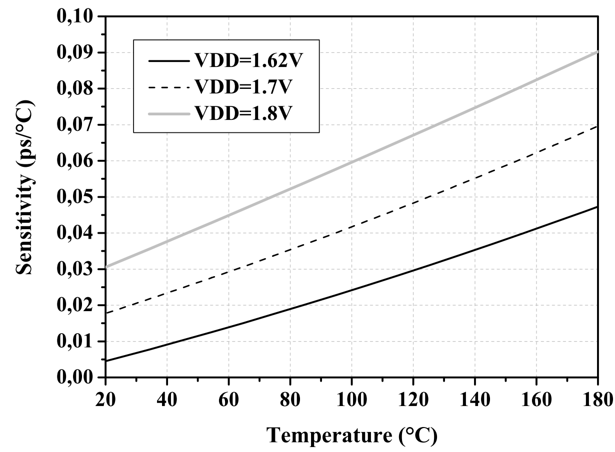


Figure 4.16: Guardband Interval under VDD and T variations.

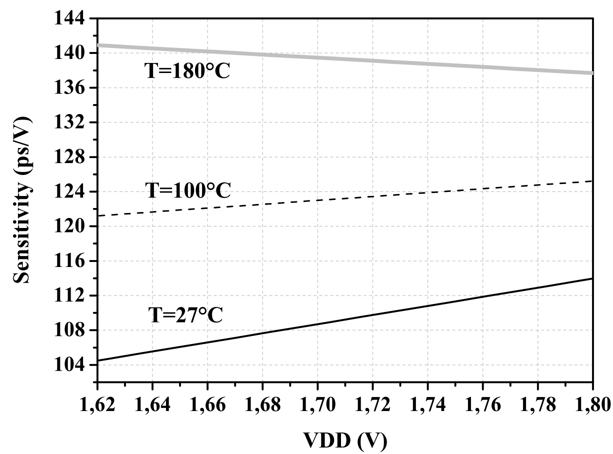
Figure 4.17 shows the guardbband sensitivity with respect to VDD and Temperature. The maximum guardband interval sensitivity to temperature is $0.09 ps/^oC$, and the maximum guardband interval sensitivity to supply voltage is $140 ps/V$.

Monte Carlo analysis has been also performed. According to the information supplied by the technology of TSMC 0.18 μm and considering a gaussian distribution, the following tolerance parameters have been considered: threshold voltage (10%), gate oxide thickness (5%), transistor movilities (5%), channel width(10%) and channel length (10%). Fig4.18 shows the results obtained for 30 Monte Carlo runs when $\Delta V_{THp} = 15\%$.

Finally, the estimated area for Guardband Generator is 6.7μm x 11μm and for Transition Detector is 10μm x 9μm (See Appendix B).

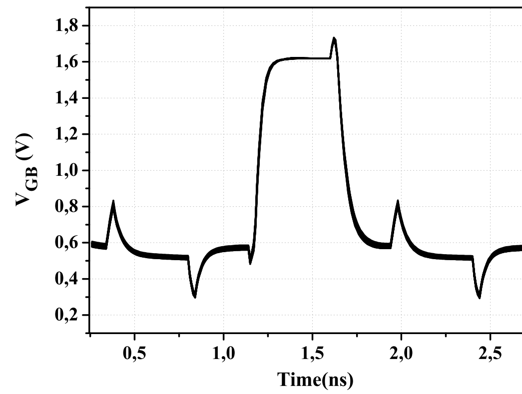


(a) Sensitivity on Temperature

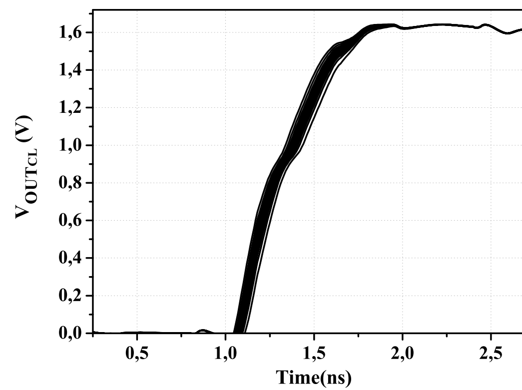


(b) Sensitivity on VDD

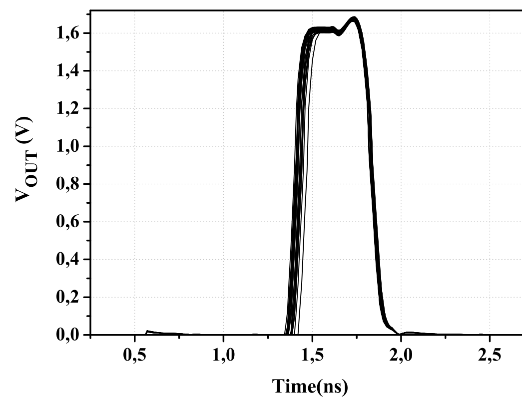
Figure 4.17: Guardband sensitivity to T and VDD.



(a) Guardband interval (GB)



(b) Combinational Logic Output (OUT_{CL})



(c) Sensor Output (OUT)

Figure 4.18: Monte Carlo Simulation. VDD=1.62V , T=180^oC. Runs=30.

4.3.1 Transition Discriminator II

In order to improve resolution of the aging sensor, a second transition discriminator circuit (TSD-II) is proposed. Figure B.4 shows the schematic diagram of TSD-II.

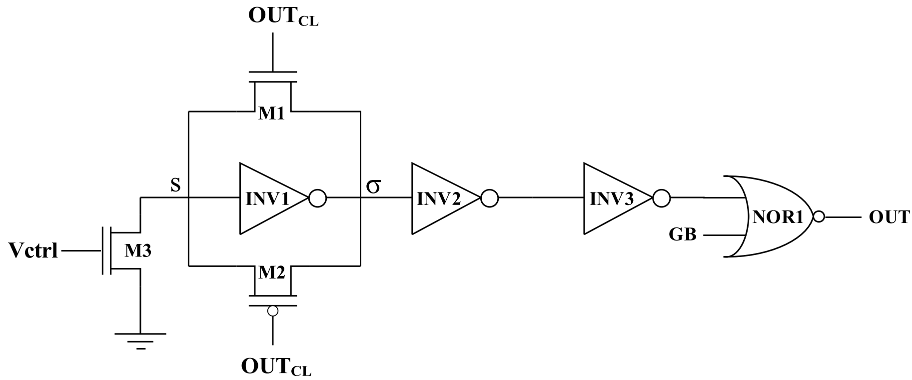
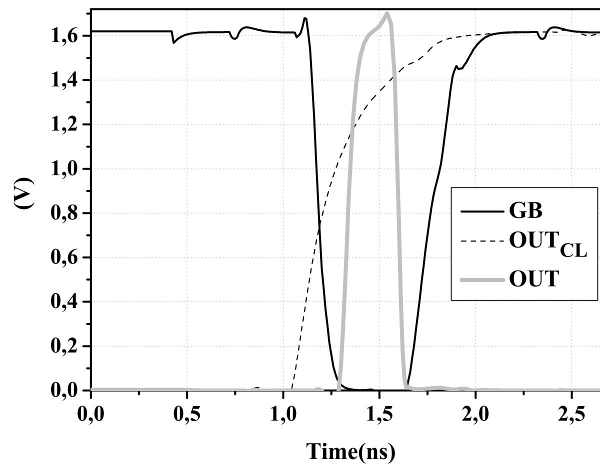
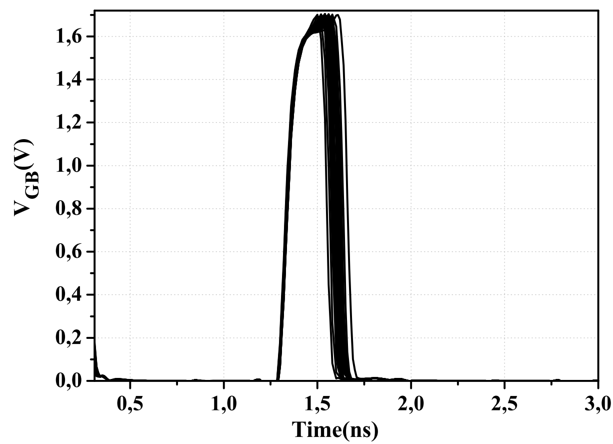


Figure 4.19: Schematic Diagram of Transition Discriminator II.

The topology is a modification of the skew detector presented in previous chapter. A PMOS and NMOS transistors are used as sensing transistors instead of two NMOS transistors. Furthermore, only one signal (OUT_{CL}) is used instead of complementary signals. In this case, at least one of the sensing transistors (PMOS or NMOS) is on. Nevertheless, as the transistors have the same dimensions, their resistances are different. PMOS on-resistance is higher than NMOS on-resistance. Hence, voltage level at node σ changes, over threshold voltage of INV2, when PMOS is on, and below threshold voltage of INV2 when NMOS is on. Therefore, when OUT_{CL} transitions, a logic level change occurs. NOR1 is in charge to discriminate the logic changes which take place inside the guardband (GB). The dimensions of TSD-II are the same used for skew detector of chapter 3 and guardband generator. Figure 4.20, shows the simulation result obtained for $\Delta V_{THp} = 5\%$ under worst case conditions (VDD=1.62V,T=180^oC). Also Monte Carlo analysis has been performed for the same conditions mentioned for implementation I.



(a) Simulation of the sensor with TSD-II.



(b) Monte Carlo Simulation using TSD-II

Figure 4.20: Simulation of the aging sensor using TSD-II. VDD=1.62V, T=180^oC, $\Delta V_{THp} = 3\%$.

Figure 4.21 compares the minimum $\Delta V_{THp}\%$ detected for the aging sensor using TSD-I ($\Delta V_{THp-min} = 15\%$) and the aging sensor using TSD-II ($\Delta V_{THp-min} = 5\%$). Hence, aging sensor implemented with TSD-II has a better resolution.

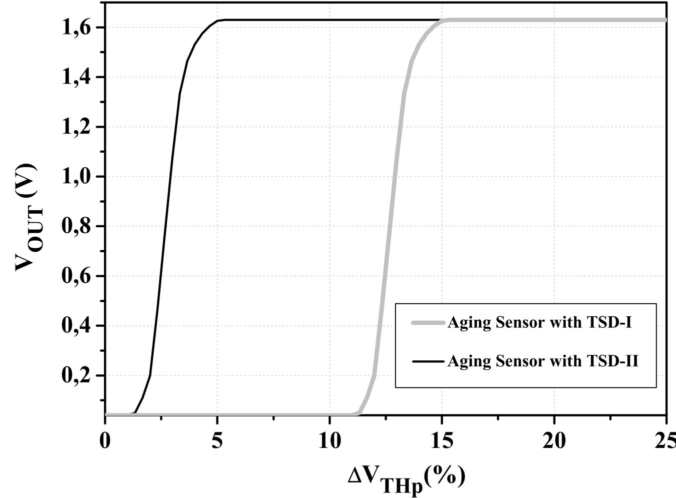


Figure 4.21: Resolution for Aging sensor using TSD-I and TSD-II.

Furthermore, the cost in percentage of delay penalization is improved with TSD-II. The cost for aging sensor implemented with TSD-I is 9% and for aging sensor implemented with TSD-II is 6%. Nevertheless, the estimated area for TSD-II is 11μm x 13μm which is bigger than TSD-I.

4.4 Conclusions

An aging sensor for digital circuits has been proposed. The sensor is located in parallel with the FF at the output of combinational logic. A guardband interval has been defined before the clock edge which corresponds to the instant of data-stored. Hence, any transitions of the output of the combinational circuit inside guardband, indicates an excess of delay due to aging. The maximum guardband interval sensitivity to temperature is $0.09ps/^{o}C$, and the maximum guardband

interval sensitivity to supply voltage is $140ps/V$.

Moreover, two transient discriminator (TSD) circuits are proposed. TSD is in charge to detect transitions of the combinational logic output inside the guardband interval. TSD circuit I, is a simplified version of the stability checker circuit proposed in [53] and [46]. The minimum delay detected under worst case operating conditions (VDD=1.62V and T=180^oC), corresponds to an increment of 15% of the threshold voltage of PMOS transistors of the CUT. The cost of TSD-I, expressed in percentage of delay penalization, is 9%.

In order to improve resolution and cost delay penalization, TSD circuit II has been proposed. TSD-II is a modified version of the guardband generator circuit. The minimum delay detected under worst case operating conditions (VDD=1.62V and T=180^oC), corresponds to an increment of 5% of the threshold voltage of PMOS transistors of the CUT. The cost of TSD-II, expressed in percentage of delay penalization, is 6%. Nevertheless, TSD-II requires more area than TSD-I.

Chapter 5

Conclusions

Electromigration is the major wear-out failure mechanism of VLSI interconnects and vias and it will be more serious as technology scales due to reduction of interconnect/vias dimensions which lead to major current densities. Moreover, introduction of Low-K dielectrics enhances joule heating due to their low thermal conductivity.

Narrowed interconnects and vias, due to resistive open defects, are more prone to suffer electromigration issues which can lead to a chip failure. Interconnect Mean Time to Failure degrades due weak resistive open defects.

On the other hand, Hot Carrier Injection and Negative Bias Instability Temperature are the major aging mechanisms for NMOS and PMOS transistors respectively. Threshold voltage is shifted degrading the performance of circuits.

Since all these wear-out failure mechanism depend on workload and stress operating conditions, on line periodic testing is needed to improve reliability.

In this thesis, on-line built-in sensors for monitoring defective interconnect wear-out and transistor aging in digital circuits have been proposed. They could be used inside on-line testing systems.

The reliability risk posed by undetected small delays due to weak resistive open in signal interconnects and vias has been quantified by MTF degradation

as function of interconnect/via voiding generated by defects. MTF considers both Electromigration (EM) and Self Heating. MTF for weak resistive opens is significantly degraded. MTF degradation depends on activity factor of the node.

Reliability analysis for resistive vias located at signal and conducting paths have been considered. Redundant vias techniques have been also taken into account. For this, reliability analysis for bad vias and good vias has been quantified as function of the total number of vias. MTF degradation of bad via improves as more redundant vias used. Nevertheless, the number of redundant vias for a node must consider the maximum via density rule. On the other hand, MTF of good vias degrades due to the presence of defective via. This is due to the fact that the bad via presents a higher resistance. Hence, the average current density for good vias increases.

Strategies of vias redundancy, such as via duplication, should take into account not only critical area constraints, but also reliability risk.

Table 5.1 shows a summary of small delay behavior and reliability risk of weak resistive open defects.

X void	**Delay Behavior**	**MTF Reduction**
0-0.2	delay does not increase	MTF reduces to 50%-20%
0.2-0.5	delay does not increase	MTF reduces to 20%-10%
0.5-0.6	delay does not increase	MTF reduces to 5%-1%
0.6-0.8	delay increases a little	MTF reduces to 0.5%-0.3%
0.8-0.9	delay increases lightly	MTF reduces to 0.2%-0.05%
0.9-1	delay considerably increases	MTF completely degraded

Table 5.1: Transient behavior and reliability risk of weak resistive defect

From interconnect resistive open transient behavior, signal experiments an speed-up before defect and a slow down after defect. Delay shift at node before defect is greater than delay shift at node after defect. This proper behavior

has been used to detect small defects. In order to this, the verification strategy consists of using two skew sensors. One sensor detects negative skews and is located near the driver while the other sensor detects positive skews and is located near the receiver. Skew detection is based on addition of complementary signals. Therefore, a signal reference complementary to SUT is needed. The use of two sensors is in order to detect small delays due to weak resistive open defects and not due to process variations. The sensors have been designed to obtain the detection of the smallest resistance defect value. If only negative skew is used, the minimum resistance defect value detected is 60Ω which represents approximately 83% of interconnect voiding due to gradual defect degradation. If both sensors are used, the minimum detectable defect is 70Ω. Furthermore, if the activity factor of the node is 1, the system with both sensors could detect the defect 100 hours before a catastrophic failure occurs, but with 700 hours before when the activity factor is 0.4. Taken into account process variations, the detection parameter change to be probabilistic, therefore the resolution of the sensor could be estimated in a probabilistic way. After random experiments, the probability to detect defects less than 100Ω (approximately 86% of interconnect voiding) is 0.75.

Due to in [50][51] and [52] there is not reported results, only a qualitative comparison is made. In these works, their sensors monitoring changes in interconnect resistance. But, as it has been demonstrated in chapter 2, a detectable interconnect resistance change occurs when the interconnect is virtually broken. In our work, monitoring signal skews at the begining and at the end of the signal interconnect let us to detect the wear-out failure some time before an interconnect full open occurs.

Finally, an aging sensor for digital circuits has been proposed. The sensor is located in parallel with the FF at the output of combinational logic. A guardband interval has been defined before the clock edge which corresponds to the instant

of data-stored. Hence, any transitions of the output of the combinational circuit inside guardband, indicates an excess of delay due to aging. The maximum guardband interval sensitivity to temperature is $0.09ps/^{o}C$, and the maximum guardband interval sensitivity to supply voltage is $140ps/V$.

Moreover, two transient discriminator (TSD) circuits are proposed. TSD is in charge to detect transitions of the combinational logic output inside the guardband interval. TSD circuit I, is a simplified version of the stability checker circuit proposed in [53] and [46]. The minimum delay detected under worst case operating conditions (VDD=1.62V and T=$180^{o}C$), corresponds to an increment of 15% of the threshold voltage of PMOS transistors of the CUT. The cost of TSD-I, expressed in percentage of delay penalization, is 9%.

In order to improve resolution and cost delay penalization, TSD circuit II has been proposed. TSD-II is a modified version of the guardband generator circuit. The minimum delay detected under worst case operating conditions (VDD=1.62V and T=$180^{o}C$), corresponds to an increment of 5% of the threshold voltage of PMOS transistors of the CUT. The cost of TSD-II, expressed in percentage of delay penalization, is 6%. Nevertheless, TSD-II requires more area than TSD-I.

The aging sensor proposed in this work, using TSD-II, is compared with the sensors proposed in [53] and [46] according to the data presented in [46] for both sensors with AMS 0.35 μm. Table 5.2 indicates the comparison results in guardband sensitivity, resolution and cost.

Table 5.2: Aging Sensors Comparison

Author	$\partial GB/\partial T(ps/^{o}C)$	$\partial GB/\partial V(ps/V)$	Min.V_{THp}%	Cost(%)
Agarwall	1.9	400	not reported	9
Vazquez	0.65	220	2	9
Ours	0.09	140	5	6

Appendix A

Interconnect Thermal Analysis

A.1 Interconnect Self Heating Estimation by thermal circuit

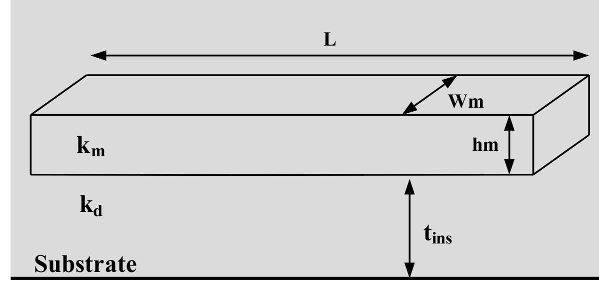
In order to establish a thermal circuit to estimate interconnect temperature a thermal-electrical analogous quantities is required. Figure A.1 shows the equivalence between the thermal and electrical variables.

Thermal		Electrical
Temperature T [K]	⟺	Voltage V [V]
Heat q' [J]	⟺	Charge Q [C]
Heat Flux q [W]	⟺	Current I [A]
Thermal Resistance R_T [K/W]	⟺	Electrical Resistance R [V/A]

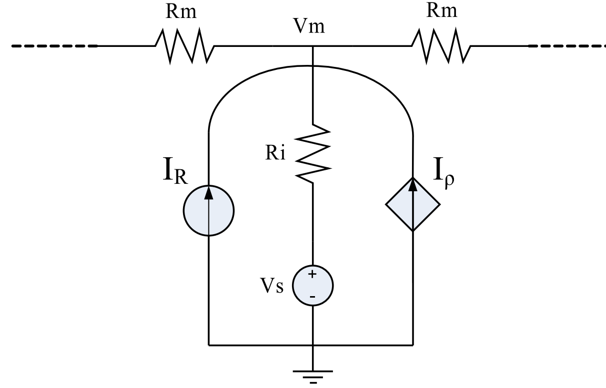
Figure A.1: Thermal-Electrical analogous quantities.

Consider an interconnect (Metal 1) embedded on an insulator showed in Figure A.2a. Where W_m is the width of the interconnect, h_m is the height of the interconnect, L is the length of the interconnect and t_{ins} is the insulator thickness underneath the interconnect. The thermal conductivity of the wire is K_m and

the thermal conductivity of the dielectric is K_d.



(a) Interconnect structure embedded in an insulator.



(b) Lumped thermal circuit of the interconnect

Figure A.2: Interconnect Thermal Model.

Figure A.2b shows the lumped thermal circuit of the interconnect. Vs and Vm represents the temperatures of the substrate and interconnect respectively. The self heating of the interconnect is divided into two sources: I_R which is a constant current source dependent on the current flowing through the interconnect (I), and I_ρ which is a voltage dependent (Vm) current source that represents the amount of joule heating due to resistivity increase caused by interconnect temperature. I_R and I_ρ are given by,

$$I_R = I^2 \rho_o \frac{L}{W_m h_m} \tag{A.1}$$

$$I_\rho = I^2 \rho_o \alpha \frac{L}{W_m h_m} Vm \tag{A.2}$$

α is the resistance temperature coefficient.

The thermal resistor along the interconnect, R_m, is given by,

$$R_m = \frac{1}{2} \frac{L}{k_m W_m h_m} \tag{A.3}$$

Then, the thermal resistor due to the dielectric underneath interconnect is,

$$R_i = \frac{t_{ins}}{kd_{eff} L W_m} \tag{A.4}$$

Hence, Vm is obtained resolving the circuit of Figure A.2b by a nodal analysis. The interconnect is assumed to be very long ($L \approx \infty$).

$$Vm = Vs + (I_R + I_\rho) Ri \tag{A.5}$$

Then, Tm due to self heating is [83],

$$Tm = Ts + \frac{J^2 \rho_o (1 + \alpha Ts)}{\frac{kd_{eff}}{h_m t_{ins}} - J^2 \rho_o \alpha} \tag{A.6}$$

Where Kd_{eff} is $Kd_{eff} = SK_d$, where S is the shape factor which describes the multi-dimensional conduction heat flow from the metal to the insulator. For this case, an isolated interconnect, S is given by,

$$S = 1.86 \left(log(1 + \frac{t_{ins}}{W_m}) \right)^{-0.66} \left(\frac{W_m}{h_m} \right) \tag{A.7}$$

Figure A.3 shows the case of parallel interconnects embedded in a insulator. The thermal coupling between interconnects is considered in S. Hence, S is given by,

$$S = \left[\frac{1}{2} ln(1 + \frac{d}{W_m}) + \frac{\frac{t_{ins}}{W_m} - \frac{1}{2}(\frac{d}{W_m})}{1 + \frac{d}{W_m}} \right]^{-1} \tag{A.8}$$

Where d is the distance between parallel interconnects.

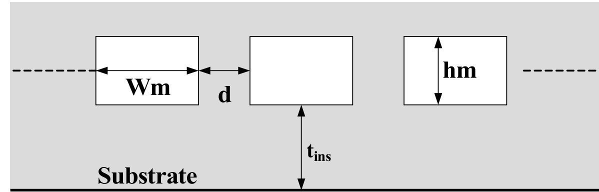
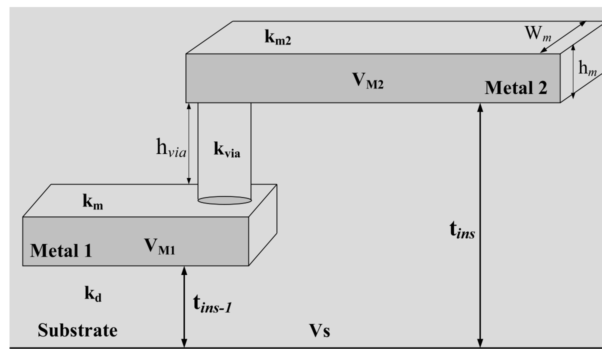


Figure A.3: Parallel Interconnects.

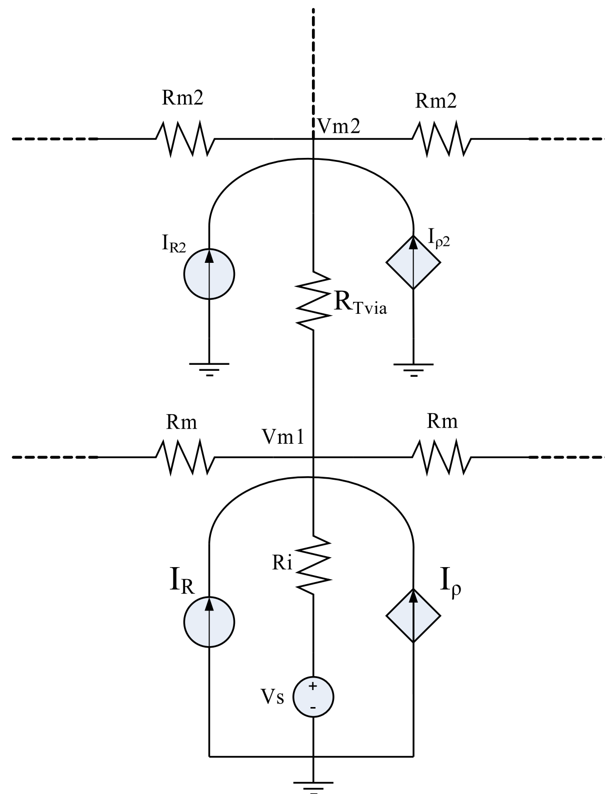
To estimate metal temperature of interconnect of upper layers, Figure A.4 shows the thermal model to be used to estimate metal temperature. Where R_{Tvia} is the thermal via resistance and is given by,

$$R_{Tvia} = \frac{h_{via}}{k_{via} A_{via}} \tag{A.9}$$

Where h_{via} is the height of the via, k_{via} is its thermal conductivity and A_{via} is its cross-sectional area.



(a) Interconnect structure with two metal levels embedded in an insulator.



(b) Thermal model

Figure A.4: Multilevel Interconnect Thermal Model.

A.2 Interconnect Temperature Distribution

In order to determine the temperature along the interconnect, equation obtained in Chapter 2 are used. These are:

$$\theta_m(x) = \theta_j \left(\frac{cosh(m_m x)}{cosh(m_m L/2)} \right) + \left(\frac{q_m'''}{k_m m_m^2} \right) \left(1 - \frac{cosh(m_m x)}{cosh(m_m L/2)} \right) \tag{A.10}$$

$$\theta_j = \frac{A_m \left(\frac{q_m'''}{m_m} \right) tanh \left(\frac{m_m L}{2} \right)}{k_m A_m m_m tanh \left(\frac{m_m L}{2} \right) + k_v A_v m_v coth(m_v h_v)} + \frac{A_v \left(\frac{q_v'''}{m_v} \right) (coth(m_v h_v) - csch(m_v h_v))}{k_m A_m m_m tanh \left(\frac{m_m L}{2} \right) + k_v A_v m_v coth(m_v h_v)} \tag{A.11}$$

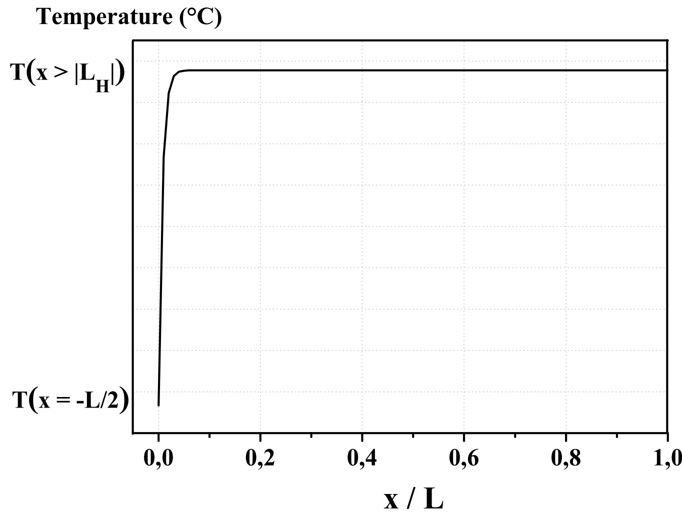


Figure A.5: Temperature distribution along the interconnect. L=1mm, Wm=0.5μm, tm=0.5μm.

All the parameters have been defined in Chapter 2. Figure A.5 shows the temperature distribution along the interconnect. The minimum temperature is

in the region of the via, this due to the via acts as a heat sink to the substrate. The length when the temperature of the interconnect become a constant, is known as *characteristic length* and is approximately $50\mu m$ [62].

Appendix B

Layouts

B.1 Negative/Positive Skew Sensor

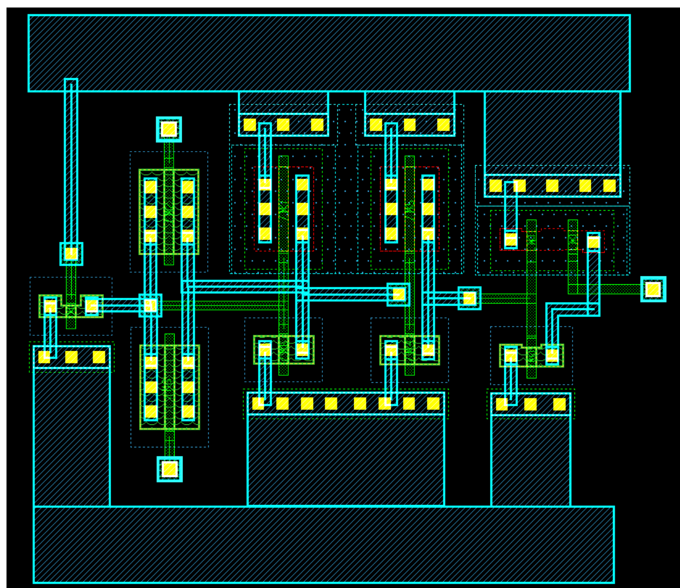


Figure B.1: Negative Skew Sensor: 12μm x 10μm.

B.2 Aging Sensor

B.2.1 Guardband Generator

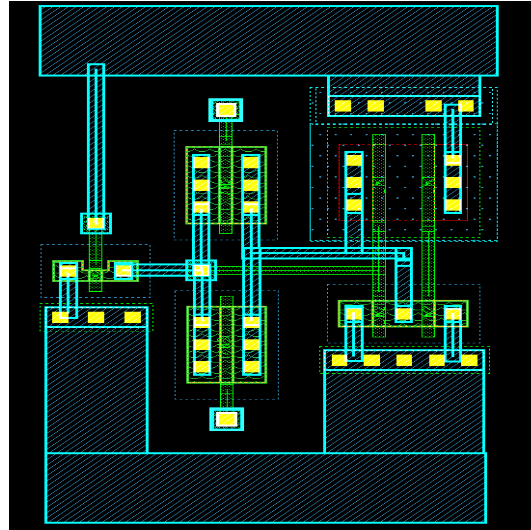


Figure B.2: GuardBand Generator(GBG): 6.7μm x 11μm.

B.2.2 Transition Detector - I

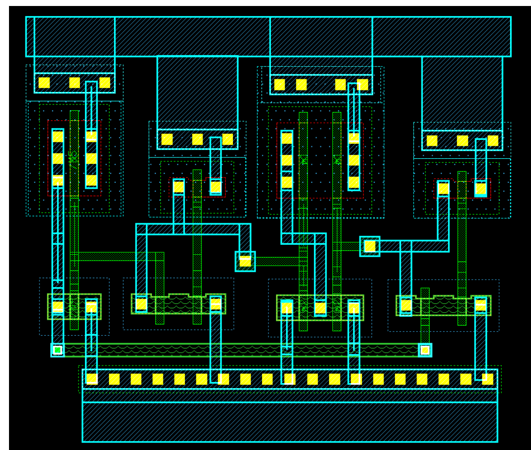


Figure B.3: Transition Discriminator I (TSD-I): 10μm x 9μm.

B.2.3 Transition Detector - II

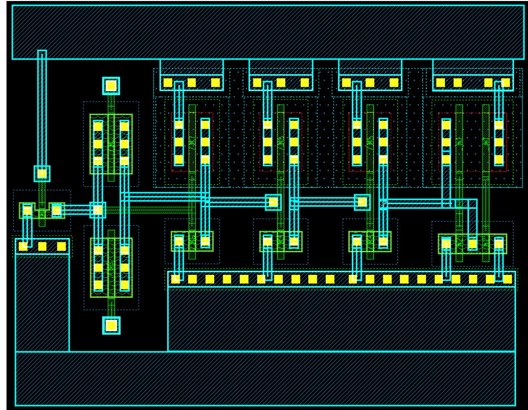


Figure B.4: Transition Discriminator II (TSD-II): 11μm x 13μm.

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