Design and Applications of CMOS Current Conveyors

by

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Abstract

A Current Conveyor (CC) is a minimum 3-terminals device which can perform many useful analog signal processing functions. The first generation CC was introduced in 1969, and more recently, it is a good alternative in Current-Mode design. Nowadays, the CCs can be classified as direct and inverted, and they are divided as first, second and third generation, where they can be positive-type, negative-type, multiple-output and/or current-controlled.

In this Thesis it is highlighted that the CC can be easily designed by combining the connection among different Unity Gain Cells (UGCs) as basic building blocks. Furthermore, from the characteristic equation of each kind of CC, they can be implemented just by superimposing or by cascading UGCs such as voltage (VF) and current followers (CF), and voltage (VM) and current mirrors (CM).

New Nullor equivalent representations for all CC topologies are introduced in this work, which are used to perform symbolic analysis of CC-based circuits by applying Nodal Analysis (NA). It is shown that the nullor is a very useful concept that helps the designer to easily analyze analog circuits. In this manner, by using this ideal concept, analytical equations (transfer functions) of CC-based circuits are calculated.

The realization of the UGC-based CCs begins by designing each UGC at the transistor level of abstraction. Each UGC has been designed as a symmetrical type circuit in order to allow superimposing or cascading connection to implement all kinds of CCs, both direct and inverted. Finally, some applications of the UGC-based CCs, like filtering, sinusoidal oscillator and inductance simulator, are presented to show their suitability and usefulness in the field of analog signal processing.

Resumen

El Current Conveyor (CC) es un dispositivo con un mínimo de tres terminales, el cual puede realizar diversas funciones de procesado analógico de señales. La primera generación de los CC fue presentada en 1969, y recientemente se ha visto como una buena alternativa en el diseño de circuitos en modo corriente. Los CC pueden ser clasificados como directos o inversos, divididos en primera, segunda y tercera generación, los cuales están subdivididos en positivos, negativos, múltiples salidas y/o controlados por corriente.

En el presente trabajo los CC son diseñados combinando diferentes celdas de ganancia unitaria (UGCs) como bloques básicos de diseño. Tomando la ecuación característica de cada tipo de CC, estos pueden ser implementados superimponiendo estas UGCs, tales como los seguidores de voltaje (VF) y corriente (CF), y espejos de voltaje (VM) y corriente (CM).

Se presentan nuevos equivalentes con nullor para todas las topologías de CC, los cuales son usados para realizar un análisis simbólico de circuitos basados en CC aplicando análisis nodal (NA). Se muestra que el nullor es un concepto muy útil que ayuda al diseñador a analizar fácilmente circuitos analógicos. De esta manera, utilizando este concepto ideal, se calculan las funciones de transferencia de varios circuitos basados en los CC.

La realización de los CC basados en UGCs comienza diseñando cada una de estas celdas a nivel transistor. Las UGCs fueron diseñadas como circuitos simétricos para poder superimponer cada una de estas celdas para implementar todos los tipos de CC, tanto directos como inversos. Finalmente, algunas aplicaciones de estos CC basados en UGCs son implementados, tales como filtros, osciladores sinusoidales o simuladores de inductancias para demostrar su utilidad en el campo

del proceso analógico de señales.

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Contents

Chapter 1

Introduction

Since the introduction of integrated circuits, the operational amplifier (opamp) has been the basic analog building block in circuit design, it has been evolved by introducing new analog integrated circuit applications and by changing the analog circuit requirements [1].

Early high-gain amplifiers were implemented using discrete thermionic valves which were inherently voltage-controlled devices with controlled voltage output allowed stages to be easily cascaded. Then the resulting voltage opamp architectures were translated to silicon with the development of integrated circuit technologies, and this device become ubiquitous to the area of analog signal processing [2].

The opamp has several attractive features, such as the differential pair input stage that is very good in rejecting common-mode signals. Moreover, this device only requires a single-ended output to provide a negative feedback and to drive a load, and its implementation is simpler than a fully differential or balanced output. But on the other side, it has negative issues, as its architecture that produces certain inherent limitations in both performance and versatility. The first one is limited by a fixed gain-bandwidth product and a slew rate whose maximum value is determined by the input stage bias current. The second one is constrained by the single-ended output, since the device cannot be easily configured in closed-loop to provide a controlled output current, because it is used for the implementation of closed-loop voltage-mode circuits [2].

Also, the performance of analog systems degrades because small size devices

cannot be used due to noise and off-set constraints. Often, low voltage operation leads to complex circuits with degraded performance, forcing the analogue designers to look for new circuit architectures. Toward this end, current-mode design techniques offer voltage independent and high performance analogue circuits like Current Conveyors (CCs) [3].

Due to these drawbacks, when low power consumption with low voltage operation and a large bandwidth are required, opamp-based circuits become too complex. An alternative for the realization of these voltage-mode circuits is to use current signals rather than voltage signals in signal processing circuits [4].

In current-mode design, MOS transistors are more suitable for processing current than voltage signals, because the output of this type of transistors is current, both in common-source and common-gate amplifier configurations. Common-drain amplifier configuration is useless at low supply voltages because its bulk-effect. A common application in current-mode for the MOS-transistors are the Current Mirrors, which are more accurate and less sensitive to process variations than those Current Mirrors based in bipolar transistors, because with the latter the base currents limit the accuracy of the circuit [1].

Current-mode circuits have some recognised advantages: They do not require a high voltage gain, so high performance amplifiers are not required. They do not need high precision passive components, so they can be designed almost entirely with transistors, making these circuits compatible with typical digital processes. And as mentionated before, they show high performance in terms of speed, bandwidth and accuray [4].

1.1 Problem Description

As an alternative for the voltage-mode, the Current Conveyor (CC) represented the first building block designed for current signal processing, which was published in 1968 by A. Sedra and K.C. Smith [6], and two years later, in 1970, they published a second version of a CC named Second Generation Current Conveyor (CCII) [7], but any of these circuits became popular because of the introduction of the integrated opamp at that time. It wasn't clear which advantages could offer

the CC over the conventional and well known opamp. The electronic industry was beginning its efforts on the application of the first generation of monolithic opamps, so without clear advantages of the CC over the opamp, the industry didn't have any motivation to develop a monolithic CC. In addition, integrated CCs were difficult to realise due to the lack of high performance pnp-devices on integration technologies in the 70's. In the 80's, fast vertical pnp-devices were introduced in bipolar integration technologies, but it wasn't until now that analogue designers discovered the advantages of the CC over the voltage-mode or opamp circuit designs [5].

A CC-based circuit can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions than a corresponding opamp-based circuit. In addition, CCs have been extremely successful in the development of an instrumentation amplifier which does not depend critically on the matching of external components; instead it depends only on the absolute value of a single component [5].

There are many kinds of CCs, which can be classified by their behavior, input terminal polarity, output current direction, number of input and/or output terminals, etc. The different generation and types of CCs that will be treated in this work are shown in Fig. 1.1, where three main groups can be appreciated: First Generation CC (CCI), Second Generation (CCII) and Third Generation CC (CCIII). Each main group is divided into two big groups: Direct CC (CC) and Inverted CC (ICC). Both groups have two main types of CCs: Positive CC (e. g. CCI+) and Negative CC (e. g. CCII-). These configurations can be: Current-controlled CC (e. g. CCCIII) and/or Multiple-outputs CC (e. g. MOICCII).

So the main question is: Which type of CC is going to be used?, or Which type of CC is the best? The hypothesis of this work is that there is no best CC, each type of CC is better than the others for a specific application. So, the topology for a specific application depends on the electrical characteristics of the CC that best match with the application that is being studied or designed.

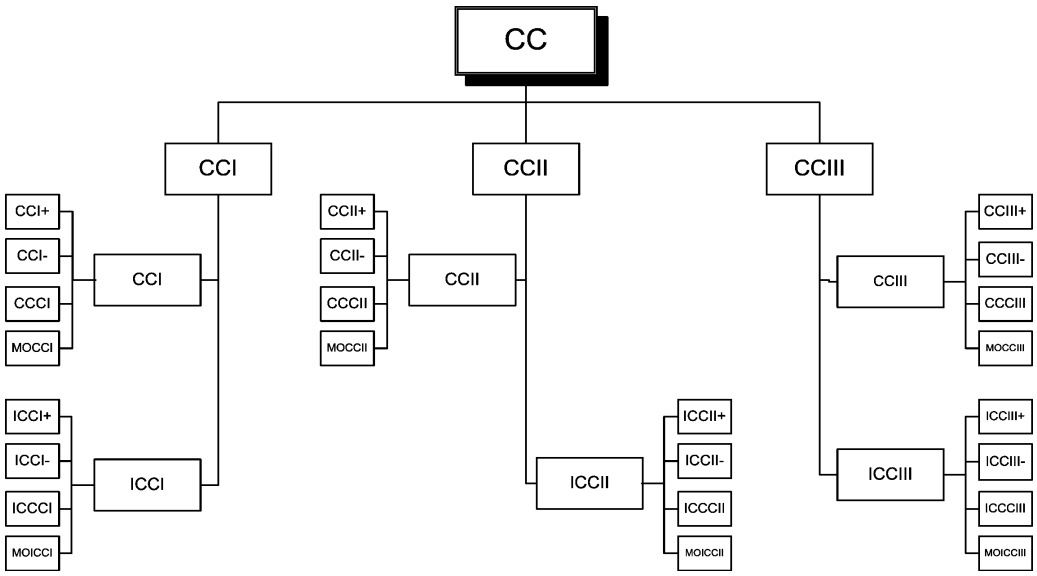


Figure 1.1: Different types of CCs.

1.2 History...

In 1966 A. Sedra was working on his Master's thesis project under the supervision of Prof. K. C. Smith at the University of Toronto. The goal of the project was to design programmable instruments for their implementation in a system for computer controlled experiments. His first task was to design a voltage controlled waveform generator, but at the end he designed a novel circuit, where the control variable was current and not voltage as it was required [8]. To solve this problem he designed the circuit shown in Fig. 1.2 where Q1 is the current source transistor, its emitter was connected via a resistor R to a control voltage Vc. Transistor Q2 is a compensating diode-connected transistor, its emitter was connected to ground. Transistors Q3, Q4 and Q5 form a two-output current mirror. The mirror provided a current to Q2 equal to that in Q1, thus making their Emitter-Base Voltage (V_{EB}) equal and making the voltage at the emitter of Q1 equal to zero. This in turn made the current in Q1 equal to Vc/R. The mirror supplied an equal current at the collector of Q5, at a high impedance level. Since Q3, Q4 and Q5 were discrete devices, their matching was not good and emitter resistors were added to improve the mirror performance. This circuit provided a solution to create a

precise voltage to current converter, with good results when it was incorporated into the circuit for a controlled oscillator [9].

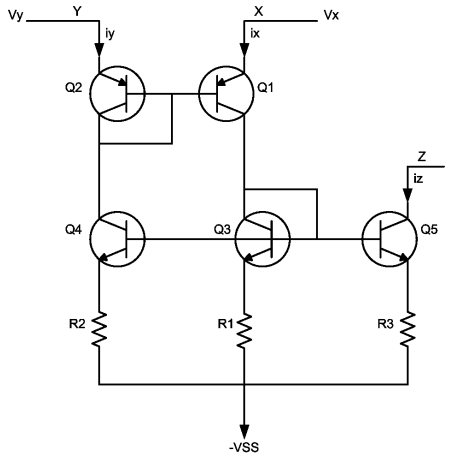


Figure 1.2: First Bipolar CC.

In Fig. 1.2 Q1/Q2 and Q3/Q4/Q5 are matched transistors. R1/R2/R3 are matched resistors. The authors observed that the Y-terminal didn't need to be grounded, and it could be connected to a voltage Vy, appearing an equal voltage in the X-terminal, independent of the current supplied into that terminal, exhibiting a virtual short circuit. Also, a current flow through the Y-terminal equal to the current supplied to the X-terminal, and it is independent of Vy, exhibiting a virtual open circuit. Finally, the current supplied to the X-terminal is conveyed to the output Z-terminal where the impedance level is very high. Moreover, the circuit operation is independent of the exact value of the negative voltage supply $-Vss$. This way, the result was the birth of the First Current Conveyor.

1.3 Objectives

The objectives of this work are:

- Design of symmetrical CC topologies based on unity gain cells.
- Propose new CC topologies based on unity gain cells.

- Introduce new Nullor equivalent representations for all CC topologies presented in this work.
- Show applications for CC-based circuits (like filtering, oscillation, inductance simulator applications).

1.4 Thesis Organization

The chapter distribution is as follows:
In Chapter 2 each type of CC, direct and inverted CCs as first, second and third generation is described, each one with their variables, as positives, negatives, multiple-output and current-controlled. All of this using unity-gain cells (UGCs) as simple building blocks.
In Chapter 3 nullor equivalents of all CCs are introduced and they are used to describe the analysis of CC-based circuits by applying Nodal Analysis (NA) and symbolic analysis.
In Chapter 4 the designs of UGCs in a transistor level are described.
In Chapter 5 the designs of Direct and Inverted CCs formed by UGCs in a transistor level are described.
In Chapter 6 some applications of the CCIs, CCIIs and ICCIIs to design active filters, oscillators and inductance simulators are shown.
In Chapter 7 the conclusions of this work are presented .

Chapter 2

Current Conveyor

The concept of the current conveyor (CC) was first presented in 1968 and further developed to a second version or generation in 1970. The CC is considered a general building block with practical applications. The opamp concept has been adopted since the late of 40's, so that it is difficult to get any other similar concept widely accepted. However, opamps do not perform well in applications where a current-output signal is needed, and consequently an application field for CC-based circuits arises. It is worthy to mention that since the CC operates without any global feedback, then it presents a different high frequency behavior compared to opamp-based circuits [1]. In this manner, this chapter describes the three main types or generations of CCs: First, Second and Third Generation. Each one divided into positive-type, negative-type, direct, inverse, multiple-outputs and current controlled.

A CC is a minimum 3-terminals device which, when is arranged with other electronic elements in a specific circuit, can perform many useful analog signal processing functions. The CC simplifies circuit design as the opamp does, due to the fact that the first one offers an alternative way of abstracting complex circuit functions. Moreover, the real behavior of a CC approaches its ideal behavior quite closely, implying that a designer can use CCs that will work at levels that are quite close to their predicted theoretical performance [5]. The CC can be classified in different ways, but the principal classification is for their Generation class. There are three types of generation, named First Generation CC or CCI,

Second Generation CC or CCII and Third Generation CC commonly named as CCIII. Each type of these different generations is divided in positive or negative CC, direct or inverted CC, Current Controlled CC, and Multiple-outputs CC. A graphical representation of these classifications was shown in Chapter 1, in Fig. 1.1. Furthermore, in this chapter their behavior and schematic representations are described.

2.1 First Generation Current Conveyor (CCI)

Basically, a CCI is a three port device which can be represented by the "black box" shown in Fig. 2.1. As it was mentioned in Chapter 1, the first CC appeared in 1968, invented by Sedra and K.C. Smith [6], and its behavior is described as follows: If a voltage is applied to the input Y-terminal, an equal potential will appear on the X-terminal. Similarly, an input current flowing through the X-terminal will generate an equal current flowing into Y-terminal, and another equal current will be conveyed to the output Z-terminal. The voltage in X-terminal, established by the voltage in Y-terminal, is independent of the current forced into X-terminal. In the same manner, the current through Y-terminal, which was established by the current through X-terminal, is independent from the voltage applied at the Y-terminal, due to the fact that the voltage in the X-terminal and the current through the Y terminal are processed by a Voltage Follower and a Current Mirror, respectively, independent between them. Thus, the CC exhibits a virtual short-circuit input characteristic at X-terminal and a dual virtual open-circuit input characteristic at the Y-terminal [5].

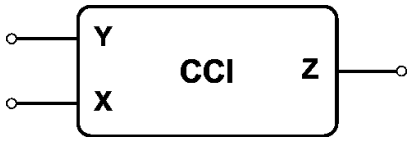


Figure 2.1: First Generation CC.

The input-output characteristics of a CCI can be described by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.1}$$

From Eq. (2.1) it can be determined that the current through the Y-terminal is equal to the current flowing through the X-terminal or $i_y = i_x$, on the other hand, the voltage in the X-terminal is equal to the voltage presented in the Y-terminal, which is represented by $v_x = v_y$. Finally, the current flowing through the Z-terminal is equal in value to that flowing through the X-terminal, but it can take two directions which generates two Z-terminal current polarities, depending if the CCI is positive or negative type ($i_z = \pm i_x$).

2.1.1 Positive/Negative CCI

A CCI can be positive or negative type, depending just on the Z-terminal current direction, with respect to the X-terminal current direction. If both currents in X and Z terminals enter or leave, the CCI is called Positive First Generation Current Conveyor or CCI+, but if the current flowing through Z-terminal has an opposite direction with respect to the one flowing through the X-terminal, the CC is called Negative First Generation Current Conveyor or simply CCI-. In a CCI+, the Z-terminal current has a phase equal to 180 with respect to the one flowing into the X-terminal. On the other hand, in a CCI- the Z-terminal current has the same phase as the current flowing through the X-terminal, in other words the Z-terminal current has a phase equal to 0 with respect to the X-terminal current. In Fig. 2.2 the CCI+ and CCI- are shown as "black boxes" with their current direction and phase, they are also shown as building-block circuits. As it is shown, the CCI+ is constructed by a Voltage Follower (VF) between the Y-terminal and the X-terminal in order to accomplish $v_x = v_y$, and two Current Mirrors (CM) between the X-terminal and the Y-terminal, and between the same X-terminal and the Z-terminal in order to accomplish $i_y = i_x$ and $i_z = i_x$, respectively. In the same manner, the CCI- is formed by a VF between the Y and X terminals, a CM

between the X and Y terminals and a Current Follower (CF) between the X and Z terminals in order to accomplish $i_z = -i_x$.

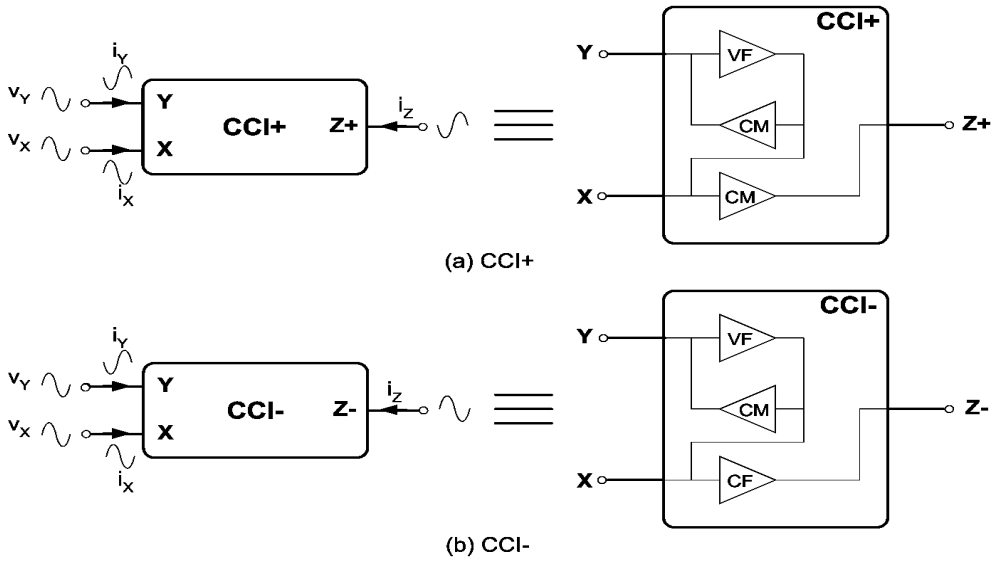


Figure 2.2: Block diagram of: (a)CCI+ and (b) CCI-.

2.1.2 Direct/Inverse CCI

A CCI can be classified as Direct or Inverse, depending on the polarity of the voltage in the Y-terminal. If the Y and X terminals have the same polarity, the CCI is called Direct First Generation Current Conveyor or CCI. If the voltage polarity in the X-terminal is opposite to the one in the Y-terminal, the CCI is called Inverse First Generation Current Conveyor or ICCI. The input-output characteristics of a CCI/ICCI can be described with Eq. (2.2)

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.2}$$

From Eq. (2.2) one can see that if $v_x = v_y$ one gets a CCI, but if $v_x = -v_y$ then one gets an ICCI. It is clear too that one can have both Direct CCI+ (CCI+)

and Inverse CCI+ (ICCI+) or both Direct CCI- (CCI-) and Inverse CCI- (ICCI-). In Fig. 2.3 the ICCI+ and ICCI- are shown as "black boxes" with their current direction and phase, they are also shown as block circuits.

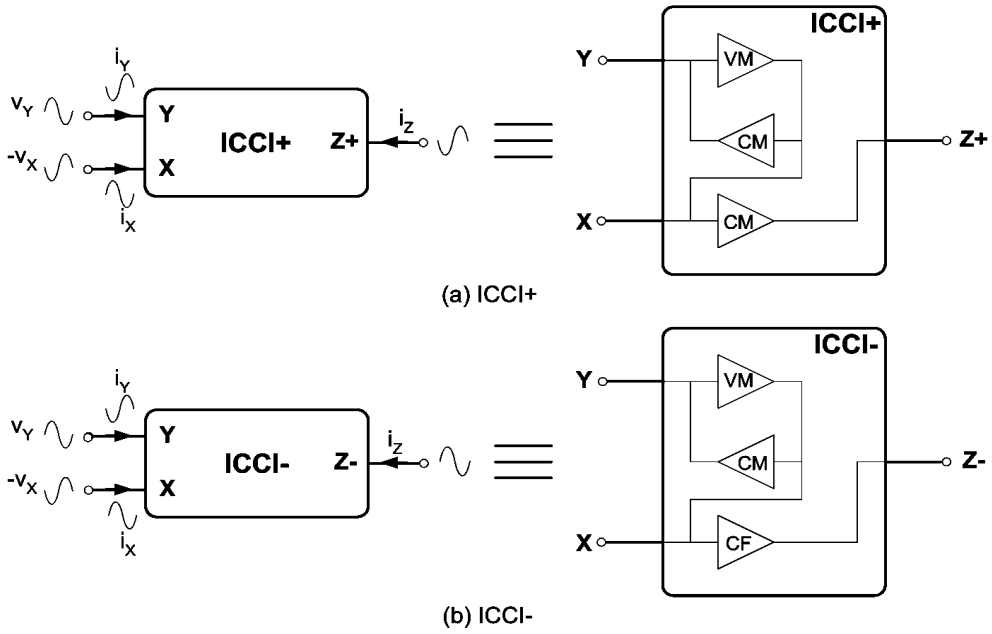


Figure 2.3: Block diagram of: (A) ICCI+ and (b) ICCI-

As it can be seen, the ICCI+ is constructed by a Voltage Mirror (VM) between the Y-terminal and the X-terminal in order to accomplish $v_x = -v_y$, and two Current Mirrors (CM) between the X-terminal and the Y-terminal, and between the same X-terminal and the Z-terminal in order to accomplish $i_y = i_x$ and $i_z = i_x$, respectively. In the same manner, the ICCI- is formed by a VM between the Y and X terminals, a CM between the X and Y terminals and a Current Follower (CF) between the X and Z terminals in order to accomplish $i_z = -i_x$.

2.1.3 Multiple-Output CCI

These types of CCIs have more than one output Z-terminal. These output terminals can be positive and/or negative. Moreover, these types of CCIs can be Direct or Inverse. In Fig. 2.4 the block diagrams of the Multiple-output Direct First Generation Current Conveyor (MOCCI) and Multiple-output Inverse First Generation Current Conveyor (MOICCI) are shown.

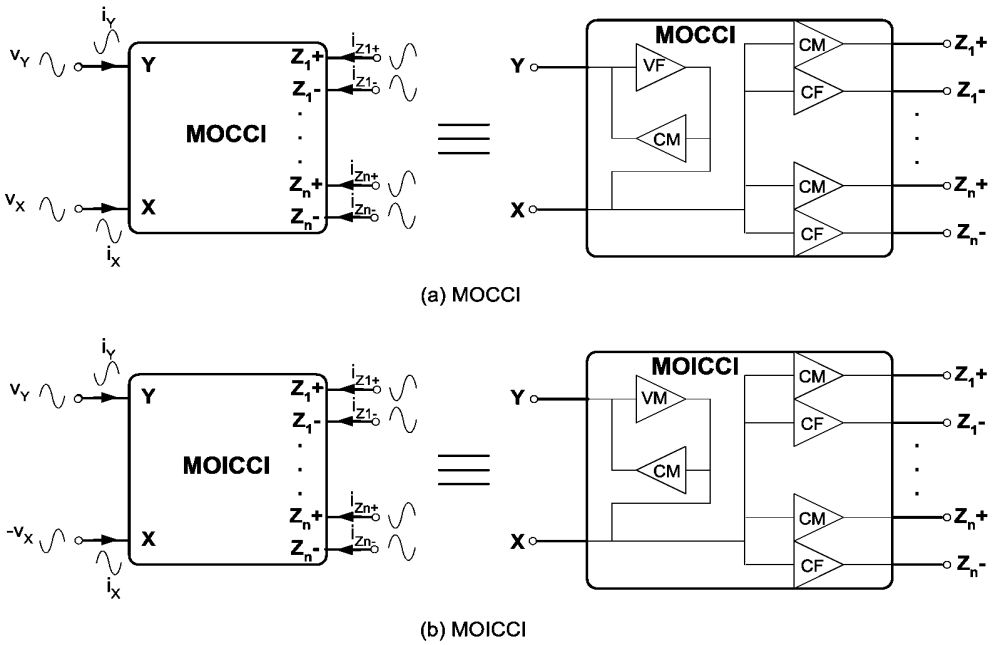


Figure 2.4: Block diagram of: (a) MOCCI and (b) MOICCI.

2.1.4 Current Controlled CCI

These types of CCIs are the same as those described before, with the difference that their bias current (Iref) can be controlled externally. In Fig. 2.5 the block diagrams of some CCIs are shown , in (a) an Inverse Current Controlled CCI+ (ICCC+) is shown, in (b) a Current Controlled CCI- (CCCI-), and finally in (c) a Multiple-output Current Controlled ICCI (MOICCCI).

2.2 Second Generation Current Conveyor (CCII)

To increase the versatility of the CCI, a second version appeared in 1970 proposed by the same authors Sedra and K.C. Smith [7], where no current flows in the Y-terminal. The CCII is described by Eq. (2.3), where the Y-terminal has an infinite input impedance. The voltage at the X-terminal follows the same one applied to the Y-terminal, thus the X-terminal exhibits a zero input impedance. The current supplied to the X-terminal is conveyed to the high output impedance at the Z-terminal [5].

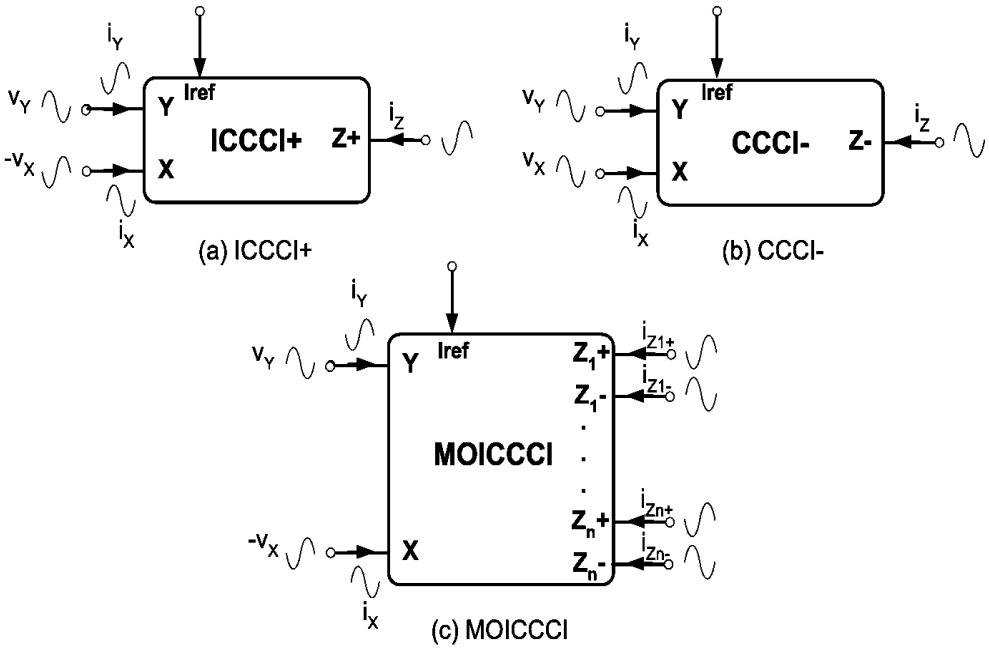


Figure 2.5: Block diagram of: (a) ICCCI+, (b) CCCI- and (c)MOICCCI.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.3}$$

From Eq. (2.3) one can see that the current through the Y-terminal is equal to zero, $i_y = 0$. The voltage in the X-terminal is equal to the voltage presented in the Y-terminal, which is represented by $v_x = v_y$. Finally, the current flowing through the Z-terminal is equal in value to that flowing through the X-terminal, but it can take two directions, depending if the CCII is positive or negative type, $i_z = \pm i_x$.

2.2.1 Positive/Negative CCII

As in the CCI, the CCII can be positive or negative, if currents in the X and Z terminals have the same direction, the CCII is called Positive Second Generation Current Conveyor or CCII+. If currents flowing X and Z terminals have opposite

directions, the CC is called Negative Second Generation Current Conveyor or CCII-. In the same manner, this classification is just based on the currents flow directions, but if the analysis is made in time domain, the concept is opposite to the one described by Eq. (2.3). In Fig. 2.6 the CCII+ and CCII- are shown, where the CCII+ is constructed by a Voltage Follower (VF) between the Y-terminal and the X-terminal in order to accomplish $v_x = v_y$, and a Current Mirror (CM) between the X-terminal and the Z-terminal in order to accomplish $i_z = i_x$. In the same manner, the CCII- is formed by a VF between the Y and X terminals, and a Current Follower (CF) between the X and Z terminals in order to accomplish $i_z = -i_x$.

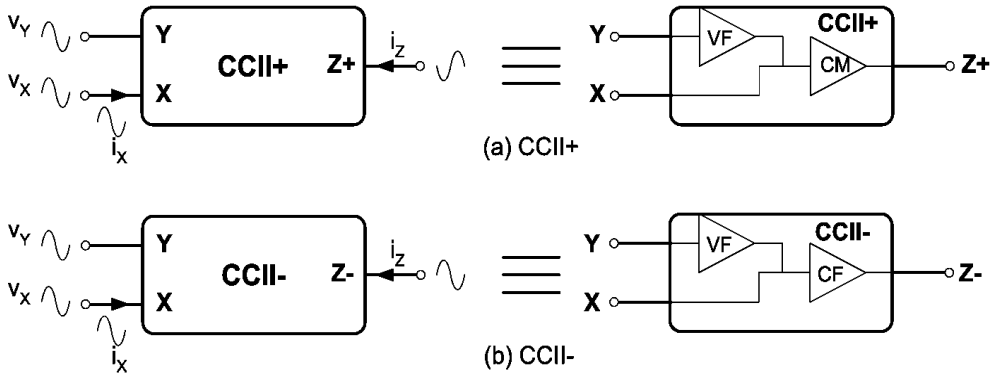


Figure 2.6: Block diagram of: (a) CCII+ and (b) CCII-.

2.2.2 Direct/Inverse CCII

The CCII can also be classified as Direct or Inverse. If Y and X terminals have the same voltage polarity it is obtained a Direct Second Generation Current Conveyor or CCII, and if the voltage polarity in X-terminal is opposite to the one in the Y-terminal, an Inverse Second Generation Current Conveyor or ICCII is obtained. The input-output characteristics of a CCII and an ICCII can be described with Eq. (2.4).

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.4}$$

From Eq. (2.4), when $v_x = v_y$ a CCII is obtained, but when $v_x = -v_y$ then an ICCII is obtained. In Fig. 2.7 the ICCII+ and ICCII- are shown.

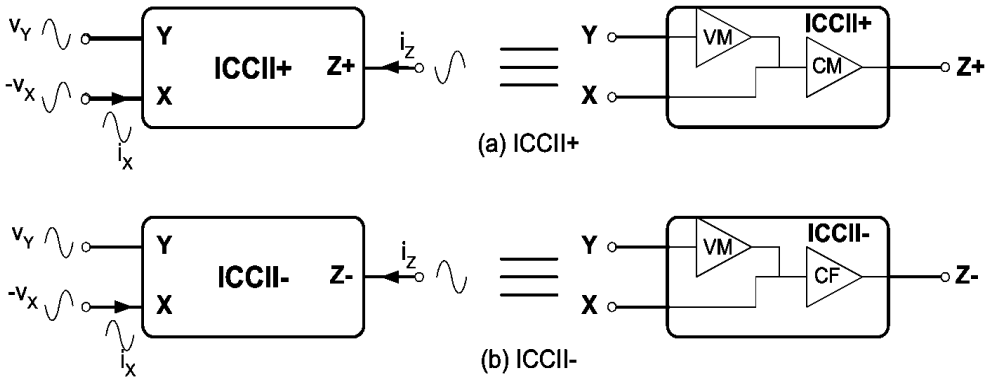


Figure 2.7: Block diagram of (a) ICCII+ and (b) ICCII-.

The ICCII+ is formed by a VM between the Y and X terminals in order to accomplish $v_x = -v_y$, and a CM between the X and Z terminals in order to accomplish $i_y = i_x$. In the same way, the ICCII- is formed by a VM between the Y and X terminals, and a CF between the X and Z terminals in order to accomplish $i_z = -i_x$.

2.2.3 Multiple-Output CCII

In Fig. 2.8 the block diagrams of the Multiple-output Direct Second Generation Current Conveyor (MOCCII) and the Multiple-output Inverse Second Generation Current Conveyor (MOICCII) are shown.

2.2.4 Current Controlled CCII

All CCIIs described before can be classified as Current Controlled ones if their current polarization Iref is externally varied. In Fig. 2.9, they are shown in (a) an Inverse Current Controlled CCII+ (ICCCII+), in (b) a Current Controlled CCII- (CCCII-) and in (c) a Multiple-output Inverse Current Controlled CCII (MOICCCII).

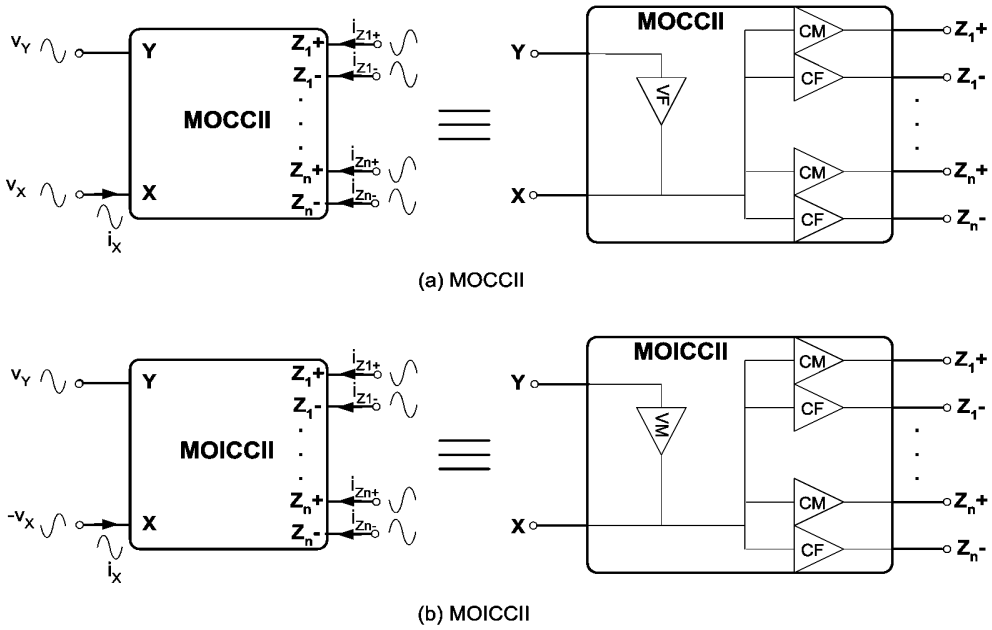


Figure 2.8: Block diagram of: (a) MOCCII and (b) MOICCII.

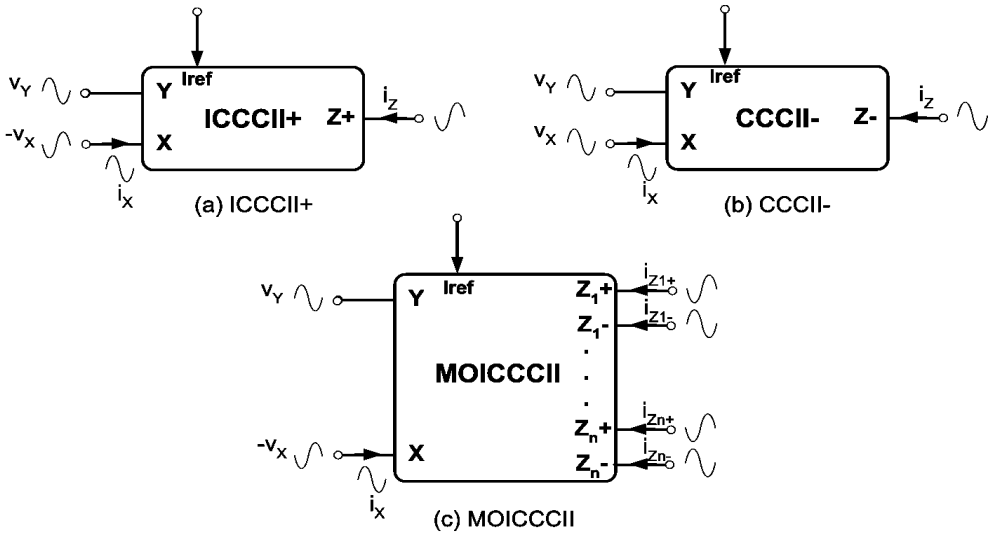


Figure 2.9: Block diagram of: (a) ICCCII+, (b) CCCII- and (c) MOICCCII.

2.3 Third Generation Current Conveyor (CCIII)

The Third Generation CC or CCIII appeared in 1995 designed by A. Fabre in [10]. Its operation is very similar to the CCI, with the difference that the current through the Y-terminal flows in an opposite direction than the current through

the X-terminal. The input-output characteristics of the CCIII are described by Eq. (2.5).

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.5}$$

From Eq. (2.5) one can see that the current through the Y-terminal is equal to the current through the X-terminal but with an opposite direction ($i_y = -i_x$). The voltage in the X-terminal is equal to the voltage in the Y-terminal, which is represented by $v_x = v_y$. Finally the current through the Z-terminal is equal in value to that flowing through the X-terminal, but it can take two directions, depending if the CCIII is positive or negative type, $i_z = \pm i_x$.

2.3.1 Positive/Negative CCIII

In the same manner as the CCI and CCII, the CCIII can be positive or negative. In Fig. 2.10 the CCIII+ and CCIII- block diagrams are shown. The CCIII+ is formed by a Voltage Follower (VF) between the Y-terminal and the X-terminal in order to accomplish $v_x = v_y$, and a Current Mirror (CM) between the X-terminal and the Y-terminal in order to accomplish $i_z = i_x$. In the same manner, the CCIII- is formed by a VF between the Y and X terminals, and a Current Follower (CF) between the X and Z terminals in order to accomplish $i_z = -i_x$.

2.3.2 Direct/Inverse CCIII

The input-output characteristics of the CCIII and ICCIII are described by Eq. (2.6).

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{2.6}$$

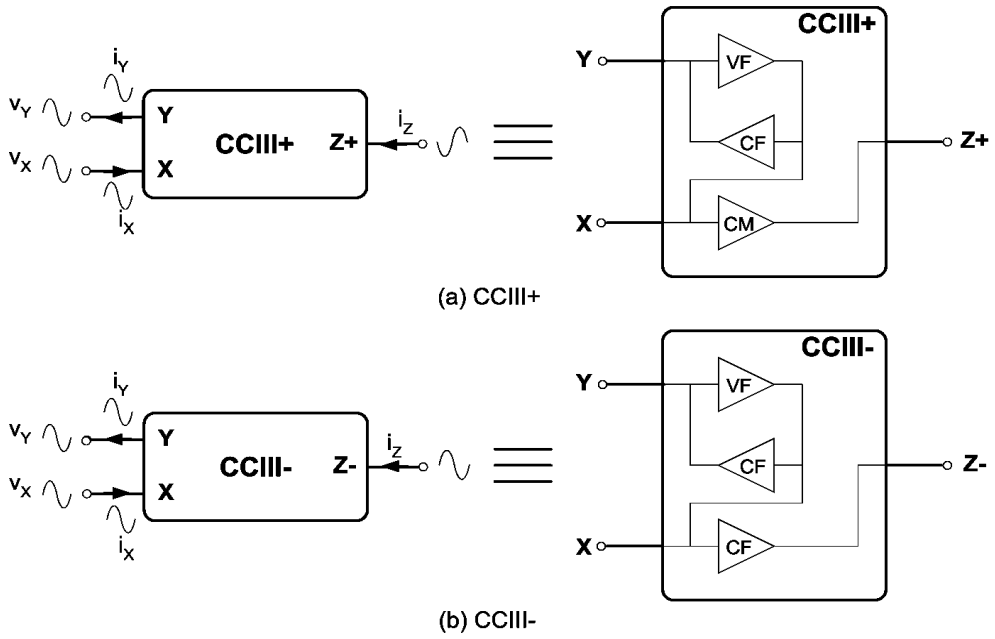


Figure 2.10: Block diagram of: (a) CCIII+ and (b) CCIII-.

Where, if $v_x = v_y$ one has a CCIII and if $v_x = -v_y$ then one have an ICCIII. In Fig. 2.11 the block diagrams of the ICCIII+ and the ICCIII- are shown.

From Fig. 2.11 it can be determined that the ICCIII+ is constructed by a VM between the Y and X terminals in order to accomplish $v_x = -v_y$, a CF between the X and Y terminals to obtain $i_y = -i_x$, and a CM between the X and Z terminals in order to accomplish $i_z = i_x$. In the same manner, the ICCIII- is formed by a VM between the Y and X terminals, a CF between the X and Y terminals and a CF between the X and Z terminals in order to accomplish $i_z = -i_x$.

2.3.3 Multiple-Output CCIII

In Fig. 2.12 the block diagrams of the Multiple-output Direct Third Generation Current Conveyor (MOCCIII) and Multiple-output Inverse Third Generation Current Conveyor (MOICCIII) are shown.

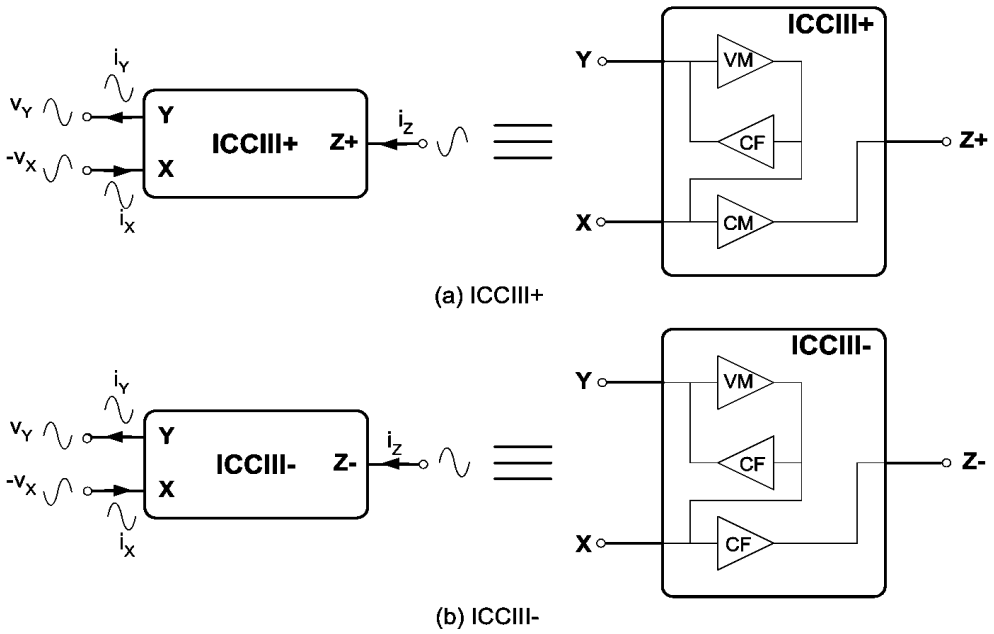


Figure 2.11: Block diagram of (a) ICCIII+ and (b) ICCIII-.

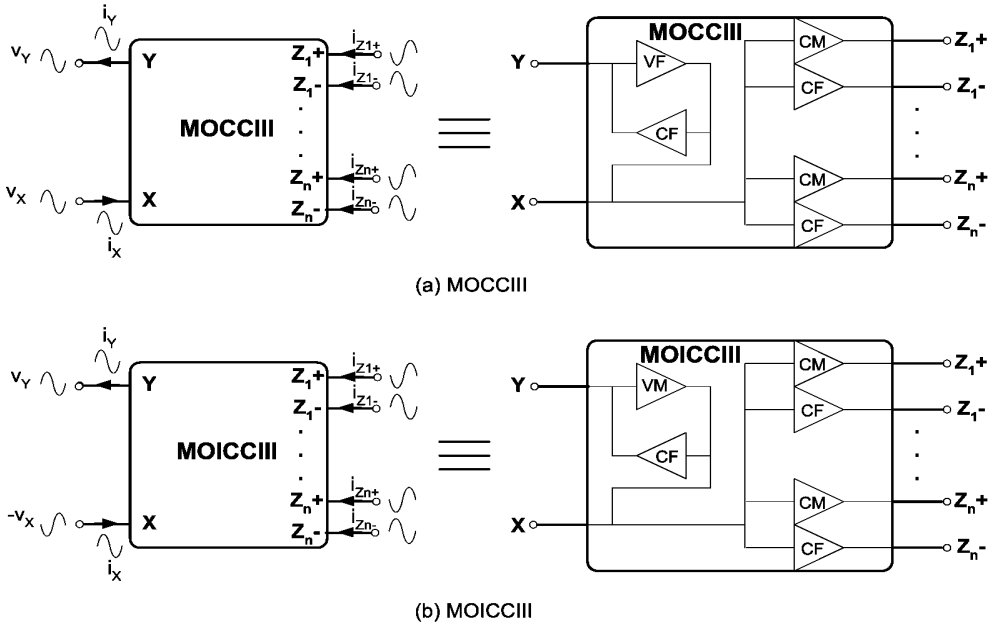


Figure 2.12: Block diagram of: (a) MOCCIII and (b) MOICCIII.

2.3.4 Current Controlled CCIII

In Fig. 2.13 it is shown in (a) an Inverse Current Controlled CCIII+ (ICCCIII+), in (b) a Current Controlled CCIII- (CCCIII-) and in (c) a MO Inverse Current

Controlled CCIII (MOICCCIII).

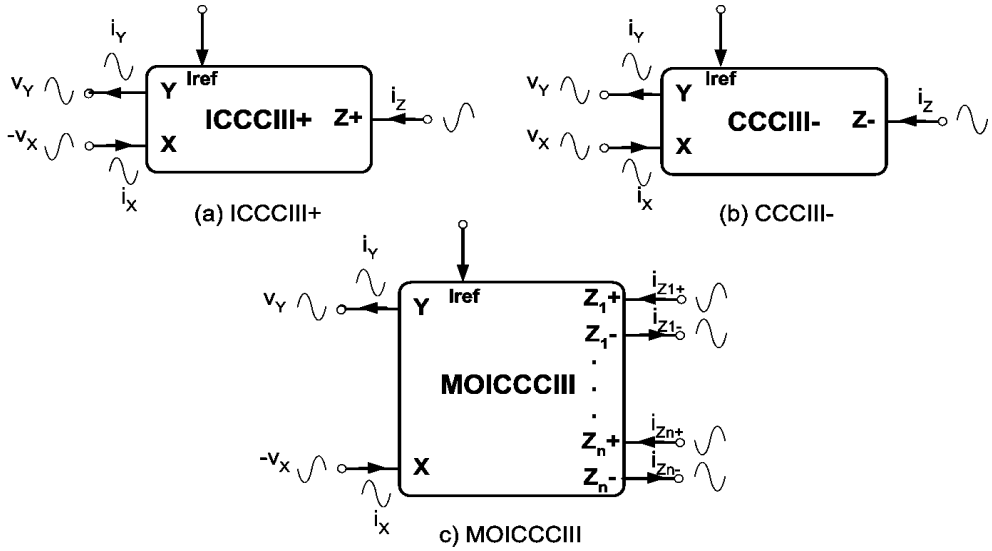


Figure 2.13: Block diagram of: (a) ICCCIII, (b) CCCIII- and (c)MOICCCIII.

Chapter 3

Nullor

The nullor consists of two basic elements named nullator and norator. These are theoretical devices that have been used in the analysis, design and synthesis of linear circuits [12, 13]. In 1954 Tellegen introduced the concept of "ideal amplifier" [14], as a general building block suitable for linear and nonlinear systems implementations, which exhibits an infinite power gain between input and output ports. Ten years later, Carlin introduced the "nullor" concept which was related to its realization consisting of a nullator at its input port and a norator at its output port. An important property is that as separated elements, the nullator has a voltage and current equal to zero. On the other hand, the norator element can take independently any voltage and current value at its output port, as a consequence the norator has not a constitutive equation. For these reasons, both elements have undefined impedances. Most important is that both the nullator and norator together as a nullor satisfies the Tellegen's definition of an ideal amplifier [2]. When a circuit is analyzed using the nullor concept, it must have always the same number of nullators and norators, in order to satisfy the branch voltage-current relationships [15]. For instance, in Fig. 3.1 the nullor symbol is shown and in Eq. (3.1) its matrix description, where the element formed by one elliptic symbol is the nullator and the element formed by two little joined circles is the norator.

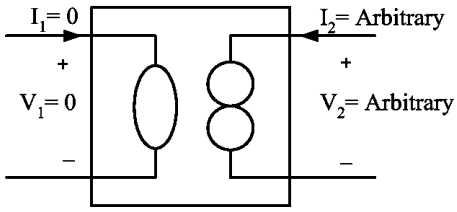


Figure 3.1: Nullor symbol.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.1}$$

3.1 Nullor Equivalents

The nullor element is a very ideal useful device for circuit analysis. This element can be connected in different ways to generate the model of an active device or circuit, in order to simplify the analysis process. Some basic nullor-equivalents are shown in Fig. 3.2, which can be applied in circuit analysis.

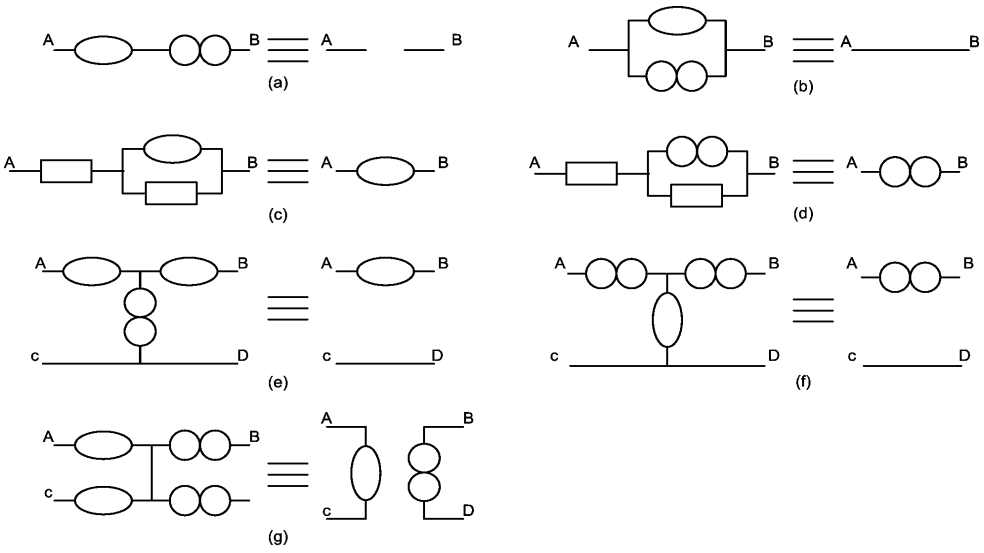


Figure 3.2: Basic nullor equivalents.

From Fig. 3.2 is clear in the case (a) that through the series connection of a nullator and a norator (from A to B) cannot flow any current because the nullator current is zero, so in this case an Open Circuit equivalent is obtained. In the case

(b) a current flows from A to B through the norator and the voltage between A and B is zero from the property of the nullator, so the result is a Short Circuit equivalent. In the case (c) no current flows from A to B because of the properties of the nullator where voltage across its terminals is zero, then a nullator with these two elements is equal to a single nullator. In the case (d) a current flows from A to B, but the voltage is not defined between the norator terminals, so that the circuit equivalent is equal to a single norator. In the case (e) the voltage difference between A and B is zero and no current flows through these terminals because of the nullator properties; the voltage between A-C and B-D is not defined and no current flows from C-D through the norator to A or B because there are two nullators blocking it. In the case (f) a current flows from A to B but no current flows through the nullator. Finally in the case (g) the voltage between A and C is zero, but no current flows between these two terminals. On the other hand, the voltage is undefined between B and D, but there is a current that flows through these terminals, so that the equivalent is the same as an ideal amplifier. By using the basic nullor equivalents, a nullor can be used to generate electrical equivalents of circuit elements. In Fig. 3.3 the equivalents of: (a) diode, (b) Bipolar Junction Transistor, (c) MOS transistor and (d) Independent Voltage Source are shown.

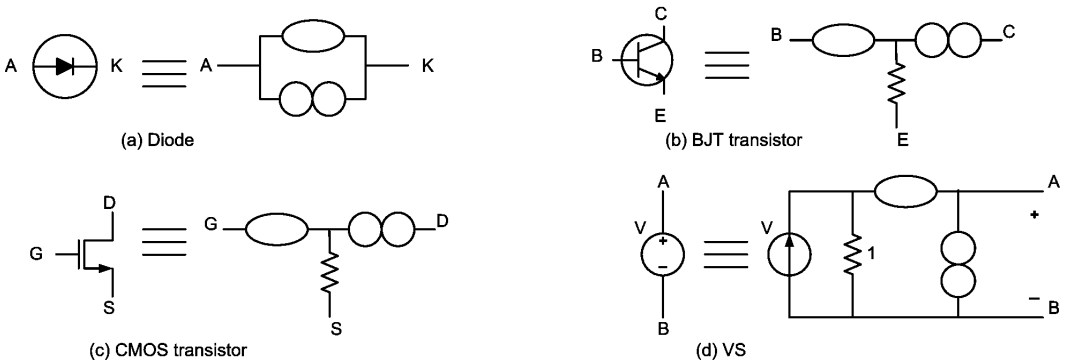


Figure 3.3: Nullor equivalents: (a) Diode, (b) BJT, (c) MOSFET, (d) VS.

The nullor concept is also useful to represent dependent voltage and current sources, due to its ideal characteristics. In Fig. 3.4 the electrical equivalents of: (a) Voltage Controlled Voltage Source (VCVS), where $V_2 = uV_1 = (g_1/g_2)V_1$; (b) Voltage Controlled Current Source (VCCS), where $I_2 = gmV_1 = gV_1$; (c) Current

Controlled Voltage Source (CCVS), where $V_2 = rI_1 = I_1/g$; and (d) Current Controlled Current Source (CCCS), where $I_2 = BI_1 = (g_2/g_1)I_1$ are shown.

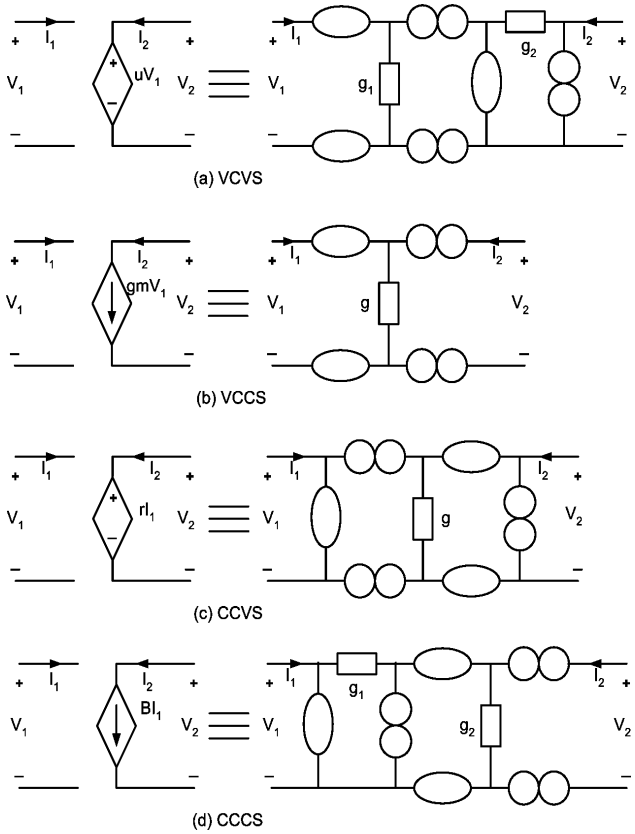


Figure 3.4: Nullor equivalents: (a) VCVS, (b) VCCS, (c) CCVS, (d) CCCS.

It is possible to represent ideal amplifiers with nullor equivalents [11]. For example, in Fig. 3.5 the equivalents of: (a) Opamp, where $Vout = Av(V_+ - V_-)$; (b) OTA (Operational Transconductance Amplifier), where $Iout = gm(V_+ - V_-)$; (c) OTRA (Operational Transresistance Amplifier), where $Vout = (I_+ - I_-)/gm$; and (d) COA (Current Operational Amplifier), where $Iout = Ai(I_+ - I_-)$ are shown. In [15] are more nullor equivalents and their equations.

3.2 Current Conveyor Nullor Equivalents

As one can infer, the nullor concept is quite useful to generate ideal equivalents of circuit elements. As a consequence one can generate the ideal equivalent of each

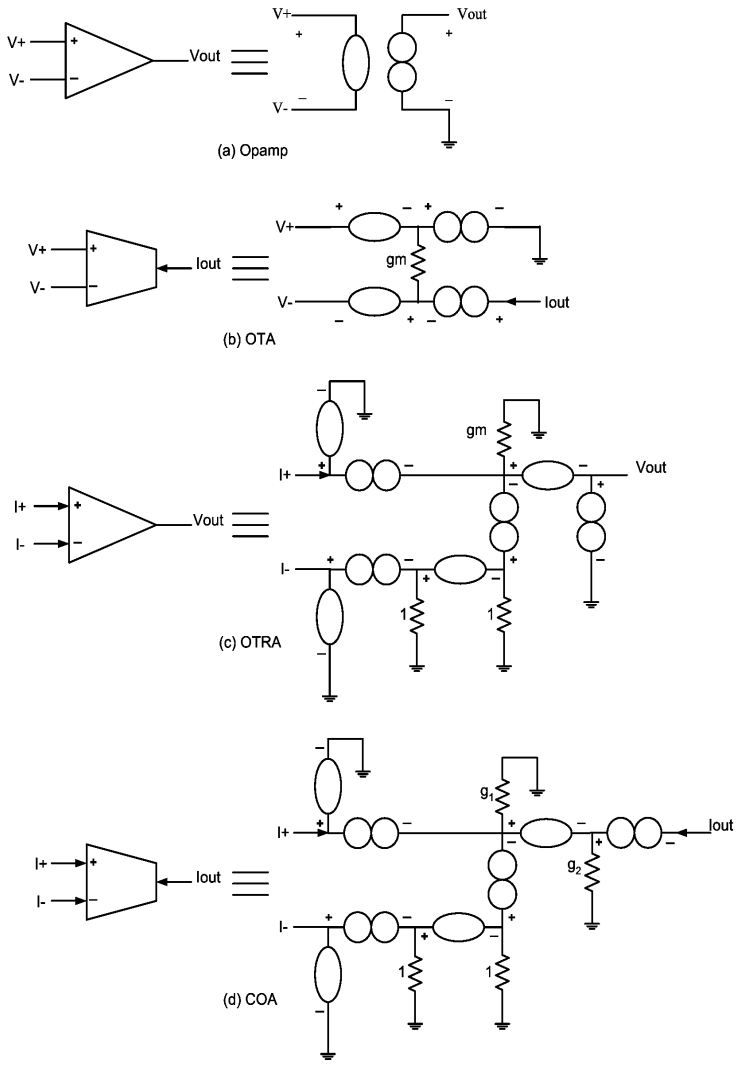


Figure 3.5: Nullor equivalents: (a) Opamp, (b) OTA, (c) OTRA, (d) COA.

CC-based circuit by using the nullor concept. Based on Eq. (2.2) for the CCIs, Eq. (2.5) for the CCIIs and Eq. (2.6) for the CCIIIs, one can construct each CC nullor equivalent. It is worthy to mention that the CCII- nullor equivalent has been already introduced in [2], but CCIs and CCIIIs nullor equivalents are contributions of this thesis. In the following ideal nullor equivalents, it was introduced the parasitic resistance Rx in the X-terminal, because its value changes as the bias current of the CCs is varied, modifying the behavior of the Current Controlled CCs.

3.2.1 CCI Nullor Equivalents

In this subsection the Positive/Negative Direct/Inverse nullor equivalents of the CCIs and as an example the equivalent of the MOICCI are shown.

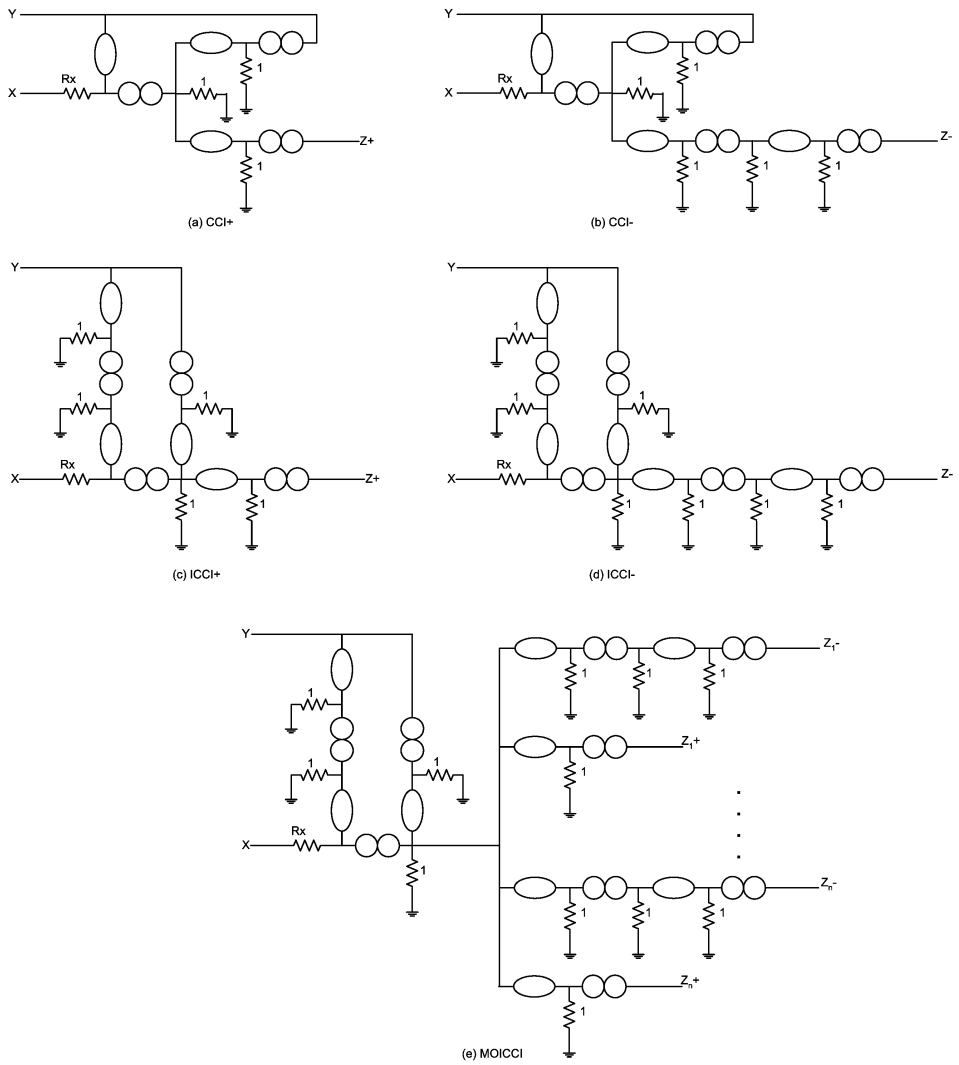


Figure 3.6: Nullor equivalents: (a) CCI+, (b) CCI-, (c) ICCI+, (d) ICCI-, (e) MOICCI.

In Fig. 3.6 the nullor equivalents of: (a) Direct Positive First Generation CC (CCI+), (b) Direct Negative First Generation CC (CCI-), (c) Inverse Positive First Generation CC (ICCI+), (d) Inverse Negative First Generation CC (ICCI-), and (e) Multiple-Output Inverse First Generation CC (MOICCI) are shown.

3.2.2 CCII Nullor Equivalents

In this subsection the Positive/Negative Direct/Inverse nullor equivalents of the CCIIs, and as an example the equivalent of the MOCCII are shown. In Fig. 3.7 the nullor equivalents of: (a) Direct Positive Second Generation CC (CCII+), (b) Direct Negative Second Generation CC (CCII-), (c) Inverse Positive Second Generation CC (ICCII+), (d) Inverse Negative Second Generation CC (ICCII-), and (e) Multiple-Output Direct Second Generation CC (MOCCII) are shown.

3.2.3 CCIII Nullor Equivalents

The CCIII is not a very popular topology in the literature currently found. It has been introduced in [10], and in this subsection the CCIIIs nullor equivalents are shown.

In Fig. 3.8 the nullor equivalents of: (a) Direct Positive Third Generation CC (CCIII+), (b) Direct Negative Third Generation CC (CCIII-), (c) Inverse Positive Third Generation CC (ICCIII+), (d) Inverse Negative Third Generation CC (ICCIII-), and (e) Multiple-Output Inverse Third Generation CC (MOICCIII) are shown.

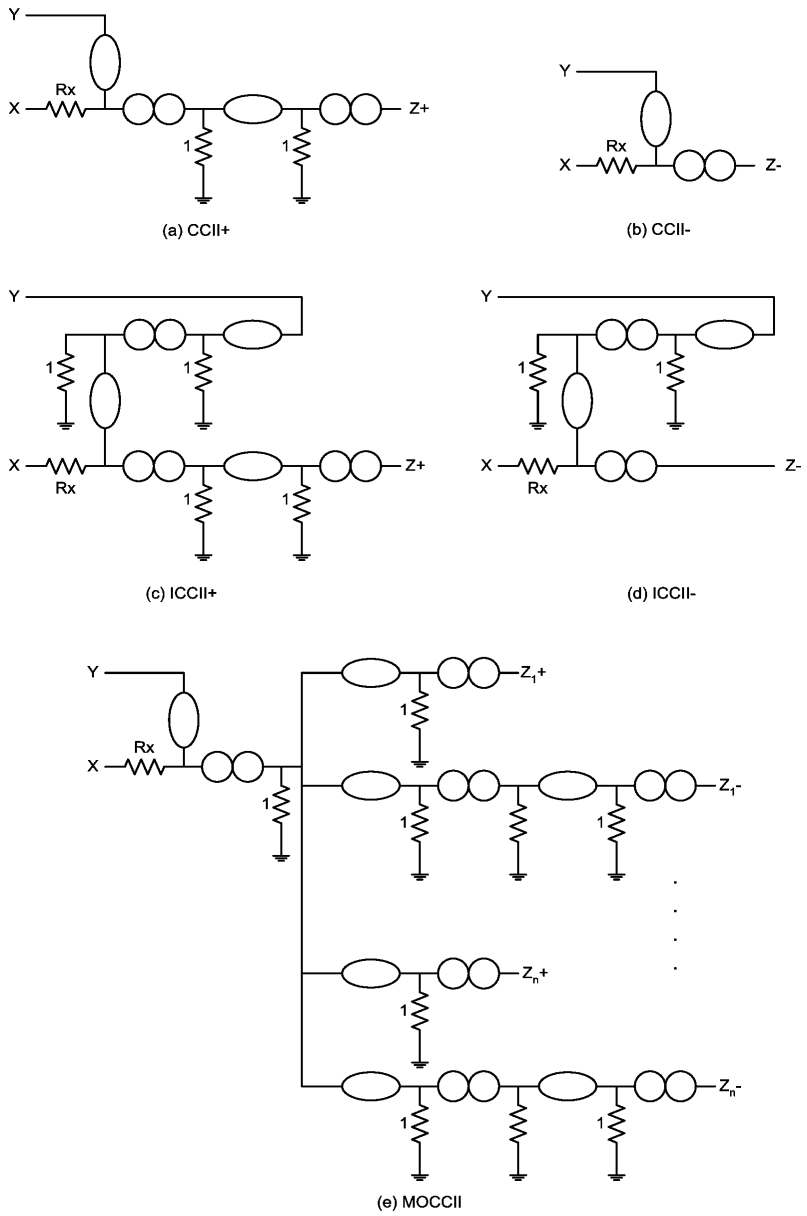


Figure 3.7: Nullor equivalents: (a) CCII+, (b) CCII-, (c) ICCII+, (d) ICCII-, (e) MOCCII.

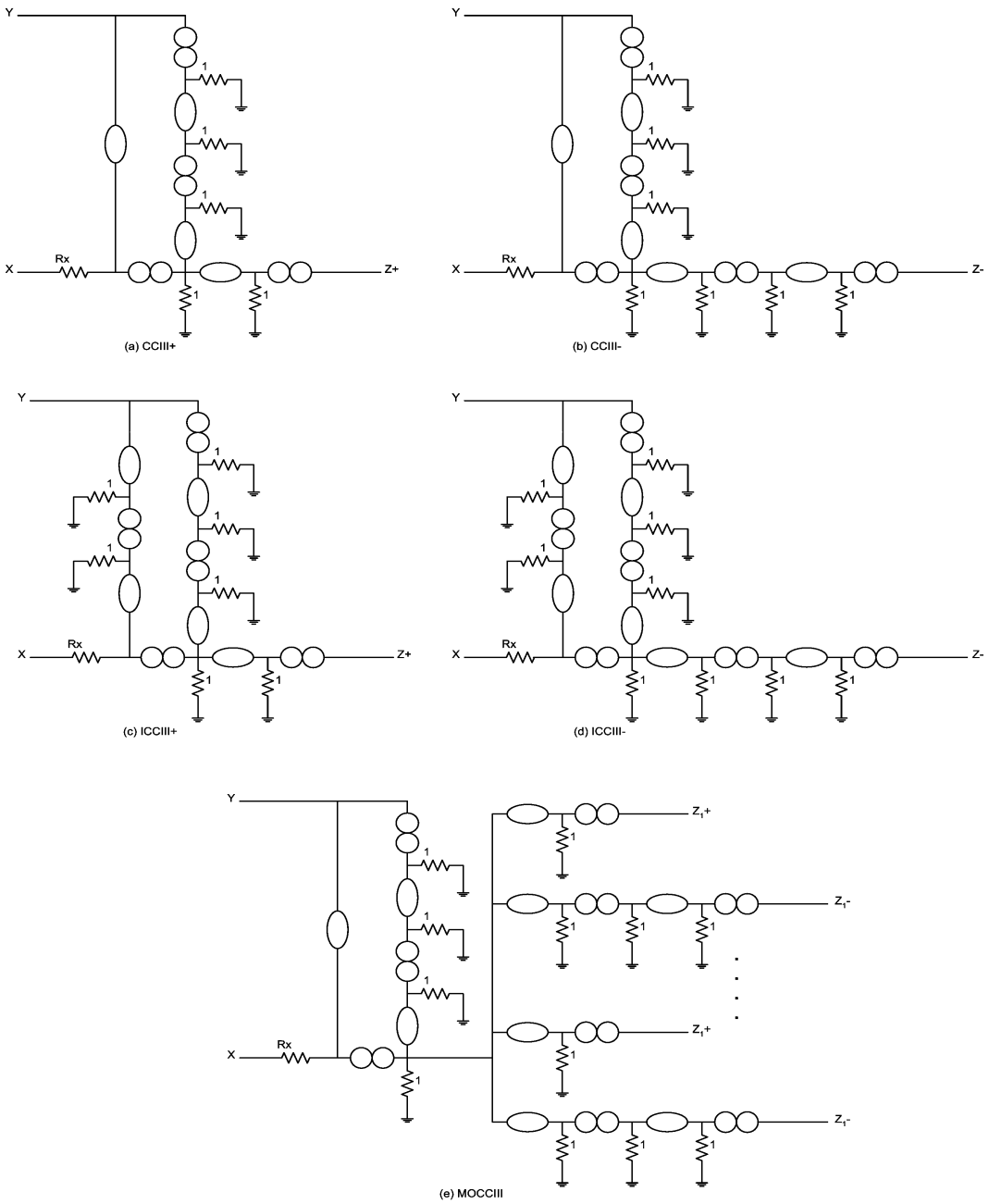


Figure 3.8: Nullor equivalents: (a) CCIII+, (b) CCIII-, (c) ICCIII+, (d) ICCII-, (e) MOICCIII.

3.3 Analysis of CC-Based Circuits

In the way to use the Nullor equivalents in circuit analysis, this subsection describes the Nodal Analysis (NA) applied to CC-based circuits. Although in [15] one can find all CCIIs nullor equivalents, in this work the CCIs and CCIIIs nullor equivalents are introduced.

3.3.1 Nodal Analysis (NA)

By applying symbolic techniques the NA is based on the idea of generating the fully symbolic circuit equations directly from the circuit description, and then putting them into the following general matrix form:

$$Ax = b \tag{3.2}$$

where A is a symbolic matrix of dimension n $\times$ n, x is a vector of circuit variables of length n, and b is a symbolic vector of constants of length n; n is the number of circuit variables: Currents, voltages, charges or fluxes. The analysis proceeds by solving Eq. (3.2) for x [15]. The first step in NA is to formulate the linear admittance matrix Y. The circuit variables are the voltage nodes which are included in the variable vector v, and vector i represents the values of all independent Current sources of the circuit. The i^{th} entry in i represents a current source entering in the i^{th} node. There will be nV voltage nodes, v and i dimensions will be of $nv \times 1$. After this, the nodal linear system of equations is represented in the following matrix form:

$$Yv = i \tag{3.3}$$

Row i of Y represents the Kirchhoff's Current Law (KCL) equation at node i. Y is constructed by writing KCL equations at each node, except for the datum node. The i^{th} equation then would state that sum of all currents leaving node i and is equal to zero. The equations are then set into the matrix form of Eq. (3.3). Building the linear admittance matrix of CC-based circuits, it is convenient to use the nullor equivalents to model the behavior of all CCs, and the NA is then performed as shown in the following section.

3.3.2 NA of CC-Based circuits using nullors.

Based in the NA described in [15, 16, 17], in this section some circuits consisting of CCI+s, ICC+s and ICCIII-s are analyzed, in order to verify the usefulness of the nullor equivalents. The NA can be summarized in the following steps:
Step 1: Obtaining the nullor circuit equivalent and label each node.
Step 2: Building the linear admittance matrix as it is done in [16].
Step 3: Reducing the admittance matrix:

a) Adding the columns that correspond to those nodes sharing a nullator element.

b) Adding the rows that correspond to those nodes sharing a norator element.

c) Eliminating those columns that correspond to a node connected to a grounded nullator.

d)Eliminating those rows that correspond to a node connected to a grounded norator.

Step 4: Solve the matrix system for v in Eq. (3.3).

CCI+ analysis:

Taking the circuit in Fig. 3.9(a), the nullor equivalent of the CCI+ is shown in Fig. 3.6, and the nullor equivalent of the independent voltage source is shown in Fig. 3.3, so that the nullor equivalent of Fig. 3.9(a) is shown in Fig. 3.9(b), where each node has a name inside a circle (Step 1).

By applying the NA method given in [16] to Fig. 3.9(b), one obtains the system given in Eq. (3.4) (Step 2):

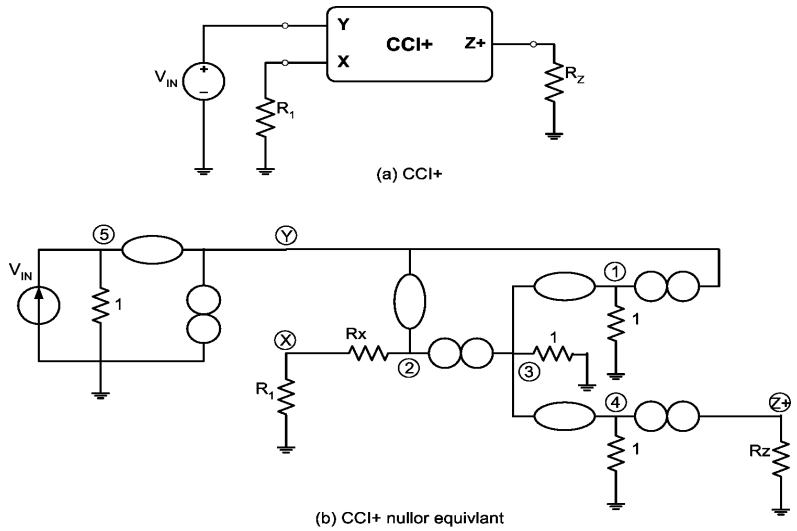


Figure 3.9: (a) CCI+ and (b) Nullor equivalent of (a).

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_{IN} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & gx & 0 & 0 & 0 & 0 & -gx & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -gx & 0 & 0 & 0 & 0 & gx+g_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & g_Z \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_Y \\ V_X \\ V_Z \end{bmatrix} \tag{3.4}$$

Reducing the matrix of Eq. (3.4) as Step 3 says:

a)Adding columns corresponding to nodes: 1-3-4, 2-Y-5:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_{IN} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & gx & -gx & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -gx & gx+g_1 & 0 \\ 0 & 0 & 0 & g_Z \end{bmatrix} \begin{bmatrix} V_{1,3,4} \\ V_{2,Y,5} \\ V_X \\ V_Z \end{bmatrix} \tag{3.5}$$

b) Adding rows corresponding to nodes: 2-3, 4-Z and eliminating the row corresponding to Y-1 due to the fact that they are connected to a grounded norator, one obtains the following reduced matrix system:

$$\begin{bmatrix} 0 \\ 0 \\ V_{IN} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & gx & -gx & 0 \\ 1 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & -gx & gx+g_1 & 0 \end{bmatrix} \begin{bmatrix} V_{1,3,4} \\ V_{2,Y,5} \\ V_X \\ V_Z \end{bmatrix} \tag{3.6}$$

Solving the Eq. (3.6) (Step 4) is obtained:

$$V_y = V_{IN} \tag{3.7}$$

$$V_x = \frac{gxV_{IN}}{gx+g_1} \tag{3.8}$$

If $g1 = 0S$, and substituting Eq. (3.7) in Eq. (3.8), is obtained:

$$V_x = V_y \tag{3.9}$$

Now, from Fig. 3.6(a), but now taking off the voltage source and by connecting an independent current source in the X-terminal, the following circuit is obtained:

From Fig. 3.10 the system given in Eq. (3.3) (Step 2) is obtained:

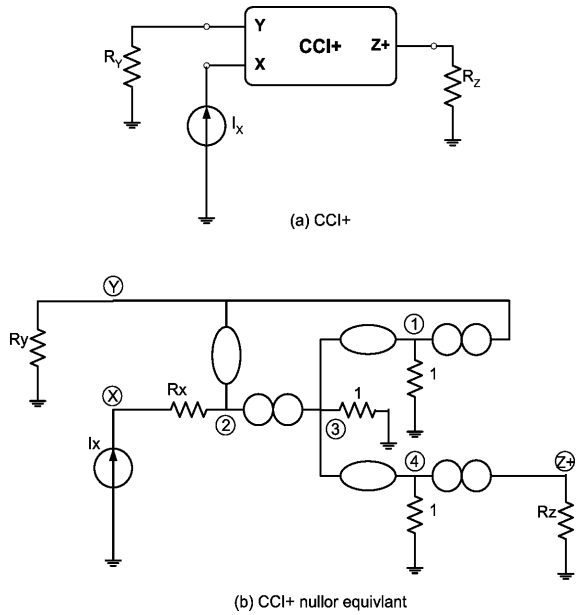


Figure 3.10: (a) CCI+ and (b) Nullor equivalent of (a).

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ Ix \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & gx & 0 & 0 & 0 & -gx & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & g_Y & 0 & 0 \\ 0 & -gx & 0 & 0 & 0 & gx & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & g_Z \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_Y \\ V_X \\ V_Z \end{bmatrix} \tag{3.10}$$

From matrix in Eq. (3.10), adding the columns corresponding to the nodes 1-3-4, 2-Y and adding the rows that correspond to nodes 1-Y, 2-3, 4-Z the following reduced system is obtained:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ Ix \end{bmatrix} = \begin{bmatrix} 1 & g_Y & 0 & 0 \\ 1 & gx & -gx & 0 \\ 1 & 0 & 0 & g_Z \\ 0 & -gx & gx & 0 \end{bmatrix} \begin{bmatrix} V_{1,3,4} \\ V_{2,Y} \\ V_X \\ V_Z \end{bmatrix} \tag{3.11}$$

Solving Eq. (3.11):

$$V_y = -\frac{Ix}{g_Y} \tag{3.12}$$

$$V_z = -\frac{Ix}{g_Z} \tag{3.13}$$

The minus sign indicates that currents are in the opposite direction, so by reordering Eqs. (3.12) and (3.13) one obtains:

$$I_y = I_x \tag{3.14}$$

$$I_z = I_x \tag{3.15}$$

So, Eqs. (3.9), (3.14) and (3.15) describe the behavior of a CCI+, which was described in Chapter 2 by Eq. (2.2).

ICCI+ analysis:

As a second example, lets consider the nullor-based ICCI+ equivalent shown in Fig. 3.6(c), and connecting to the Y-terminal the independent voltage source nullor equivalent shown in Fig. 3.3(d) to follow Step 1, then it results in the circuit equivalent shown in Fig. 3.11(b).

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ V_{IN} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ 0 & gx & 1 & -gx & 0 \\ 0 & 0 & 1 & 0 & g_Z \\ 1 & 0 & 0 & 0 & 0 \\ 0 & -gx & 0 & gx + g_1 & 0 \end{bmatrix} \begin{bmatrix} V_{1,Y,7} \\ V_{2,4} \\ V_{3,5,6} \\ V_X \\ V_Z \end{bmatrix} \tag{3.16}$$

Solving the system:

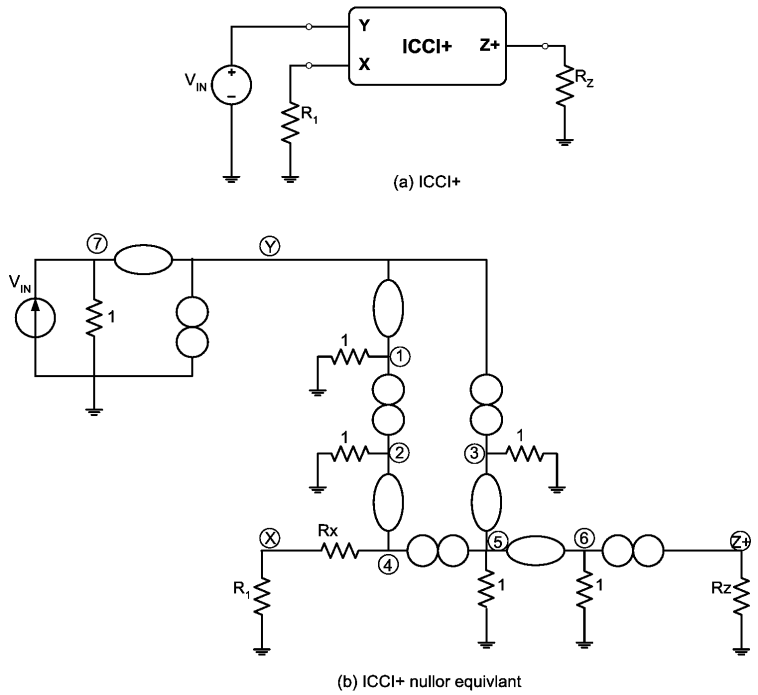


Figure 3.11: (a) ICCI+ and (b) Nullor equivalent of (a).

$$V_y = V_{IN} \tag{3.17}$$

$$V_x = -\frac{gxV_{IN}}{gx + g_1} \tag{3.18}$$

If $g1 = 0S$ and substituting Eq. (3.17) in Eq. (3.18) is obtained:

$$V_x = -V_y \tag{3.19}$$

In order to obtain the other equations that describe the behavior of the ICCI+, take off the independent voltage source from the Y-terminal and connect an independent current source at the X-terminal to obtain the circuit shown in Fig. 3.12, whose reduced system is:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ Ix \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 \\ g_Y & 0 & 1 & 0 & 0 \\ 0 & gx & 1 & -gx & 0 \\ 0 & 0 & 1 & 0 & g_Z \\ 0 & -gx & 0 & gx & 0 \end{bmatrix} \begin{bmatrix} V_{1,Y} \\ V_{2,4} \\ V_{3,5,6} \\ V_X \\ V_Z \end{bmatrix} \tag{3.20}$$

Solving the system in Eq. (3.20) is obtained:

$$V_y = -\frac{Ix}{g_y} \tag{3.21}$$

$$V_z = -\frac{Ix}{g_z} \tag{3.22}$$

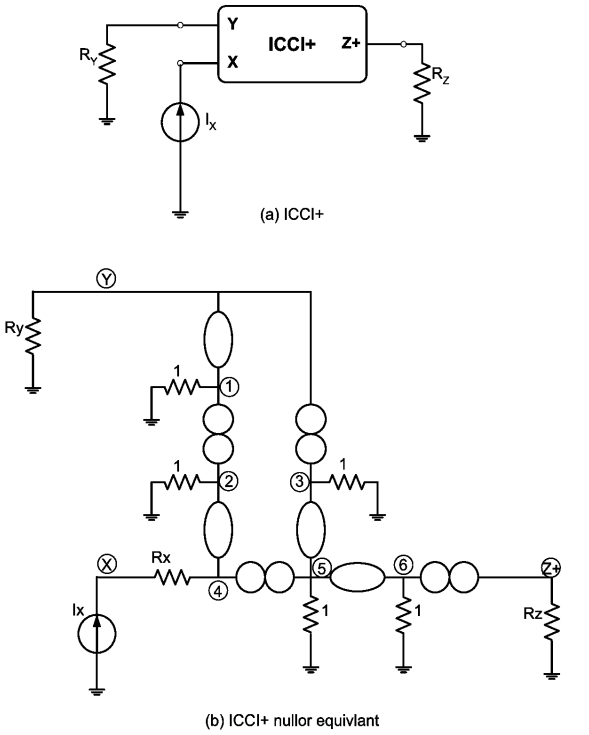


Figure 3.12: (a) ICCI+ and (b) Nullor equivalent of (a).

Again, the minus sign indicates that currents are in the opposite direction, so by reordering Eqs. (3.21) and (3.22) is obtained:

$$I_y = I_x \tag{3.23}$$

$$I_z = I_x \tag{3.24}$$

Therefore, Eqs. (3.19), (3.23) and (3.24) describe the behavior of an ICCI+, which was described in Chapter 2 by Eq. (2.2).

ICCIII- analysis

Following the procedure of the previous sections, let us connect an independent voltage source in the Y-terminal of an ICCIII- in order to obtain the voltage behavior:

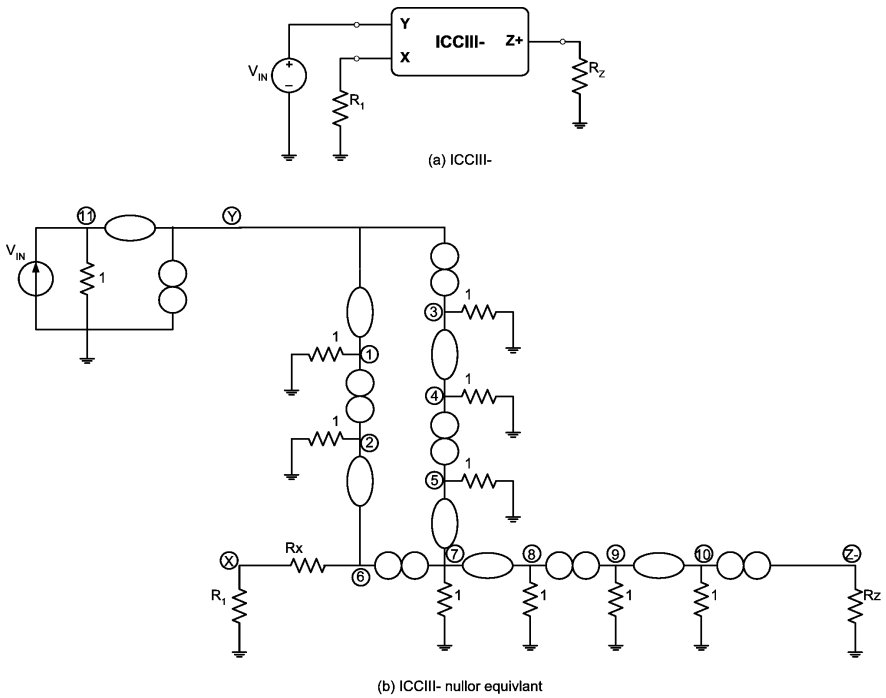


Figure 3.13: (a) ICCIII- and (b) Nullor equivalent of (a).

The reduced matrix obtained from Fig. 3.13 is:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ Iin \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & gx & 0 & 1 & 0 & -gx & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & g_Z \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -gx & 0 & 0 & 0 & gx & 0 \end{bmatrix} \begin{bmatrix} V_{1,Y,11} \\ V_{2,6} \\ V_{3,4} \\ V_{5,7,8} \\ V_{9,10} \\ V_X \\ V_Z \end{bmatrix} \tag{3.25}$$

Solving the system in Eq. (3.25):

$$V_y = V_{IN} \tag{3.26}$$

$$V_x = -\frac{gxV_{IN}}{gx + g_1} \tag{3.27}$$

If $g1 = 0S$ and by substituting Eq. (3.26) in Eq. (3.27):

$$V_x = -V_y \tag{3.28}$$

Afterwards, in order to obtain the equations that describe the current behavior of the ICCIII-, taking off the independent voltage source at the Y-terminal and connecting an independent current source to the X-terminal, the following circuit is obtained:

The matrix system obtained from Fig. 3.14 is:

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ Ix \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ g_Y & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & gx & 0 & 1 & 0 & -gx & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & g_Z \\ 0 & -gx & 0 & 0 & 0 & gx & 0 \end{bmatrix} \begin{bmatrix} V_{1,Y} \\ V_{2,6} \\ V_{3,4} \\ V_{5,7,8} \\ V_{9,10} \\ V_X \\ V_Z \end{bmatrix} \tag{3.29}$$

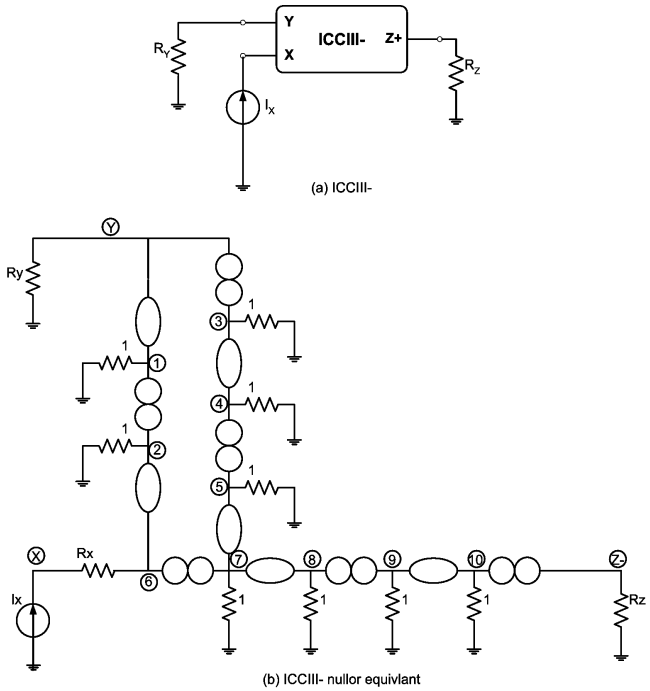


Figure 3.14: (a) ICCIII- and (b) Nullor equivalent of (a).

Solving the system in Eq. (3.29):

$$V_y = \frac{Ix}{g_y} \tag{3.30}$$

$$V_z = \frac{Ix}{g_z} \tag{3.31}$$

As opposite as the previous sections, here Eqs. (3.30) and (3.31) have no negative sign, but due to the direction considered by NA, the currents of the equations mentioned before are negative, following the current direction convention established in Chapter 2, so reordering those equations:

$$I_y = -I_x \tag{3.32}$$

$$I_z = -I_x \tag{3.33}$$

Therefore, Eqs. (3.28), (3.32) and (3.33) describe the behavior of an ICCIII- which was described also in Chapter 2 by Eq. (2.6).

3.4 Nullor-Based Current Mode Universal Filter

In this section the analysis of a Dual-Output CCII-based current-mode universal filter taken from [18] is shown, using the CC nullor equivalent. The filter topology is shown in Fig. 3.15 and its nullor equivalent in Fig. 3.16. The reduced matrix system is given by Eq. (3.34) and the transfer function is given by Eq. (3.35), where I_{out} was obtained by evaluating $I_{out} = g_L V_0$. From Eq. (3.35), the transfer function of each filter is obtained by setting: $I1 = Iin$ and $I2 = I3 = 0$ for low-pass (LP) response, $I2 = Iin$ and $I1 = I3 = 0$, for band-pass, $-I1 = I2 = I3 = Iin$ for high-pass, and $I2 = I3 = Iin$ and $I1 = 0$, for Notch response.

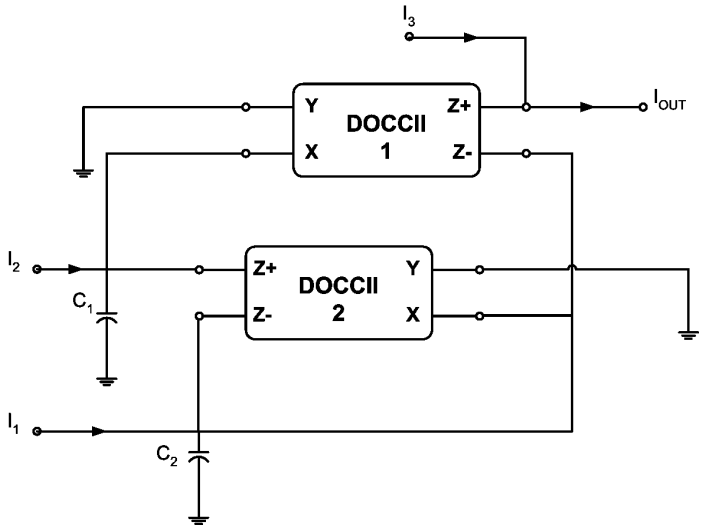


Figure 3.15: Current-mode DOCCII-based universal filter topology.

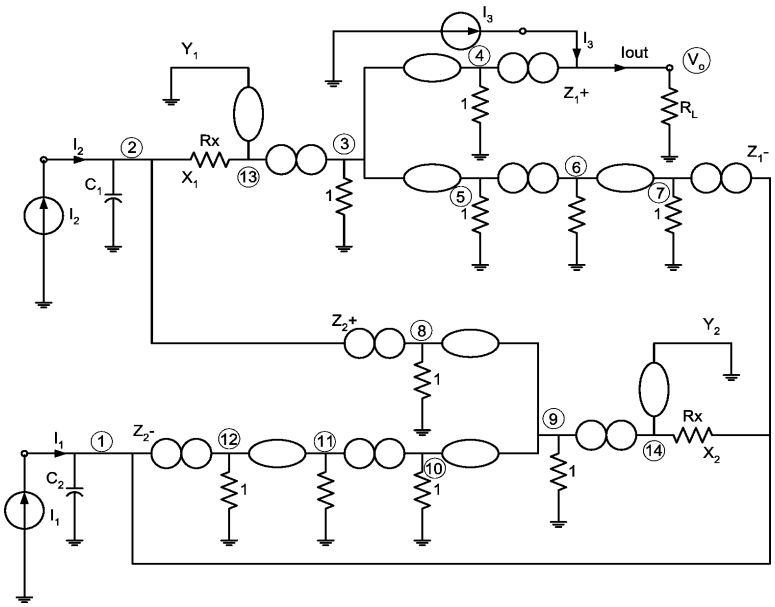


Figure 3.16: Nullor equivalent of current-mode DOCCII-based universal filter.

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} sC_2 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & sC_1 + gx_1 & 0 & 0 & 1 & 0 & 0 \\ 0 & -gx_1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & g_L \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ -gx_2 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_{3,4,5} \\ V_{6,7} \\ V_{8,9,10} \\ V_{11,12} \\ V_{Vo} \end{bmatrix} \tag{3.34}$$

$$I_{out} = \frac{(s^2 Rx_1 Rx_2 C_1 C_2 + sRx_2 C_2 + 1)I_3 - (sRx_2 C_2)I_2 + I_1}{s^2 Rx_1 Rx_2 C_1 C_2 + sRx_2 C_2 + 1} \tag{3.35}$$

From Eq. (3.35) one can obtain the center or cut-off frequency of each type of filter, which is given by Eq. (3.36):

$$\omega_0 = \sqrt{\frac{1}{Rx_1 Rx_2 C_1 C_2}} \tag{3.36}$$

For a frequency response of 3 MHz, the following values result: $C_1 = C_2 = 15pF$ and $Rx_1 = Rx_2 = 3.5K\Omega$. The responses of the filter are derived by setting: $I_1 = Iin$ and $I_2 = I_3 = 0$ for low-pass (LP) response, $I_2 = Iin$ and $I_1 = I_3 = 0$, for band-pass (BP), $-I_1 = I_2 = I_3 = Iin$ for high-pass (HP), and $I_2 = I_3 = Iin$ and $I1 = 0$, for Notch response. The ideal responses are shown in Fig. 3.17. The LP response appears with a dashed line, BP with a dashed-dot line, HP with a dotted line and the Notch response is in a solid line.

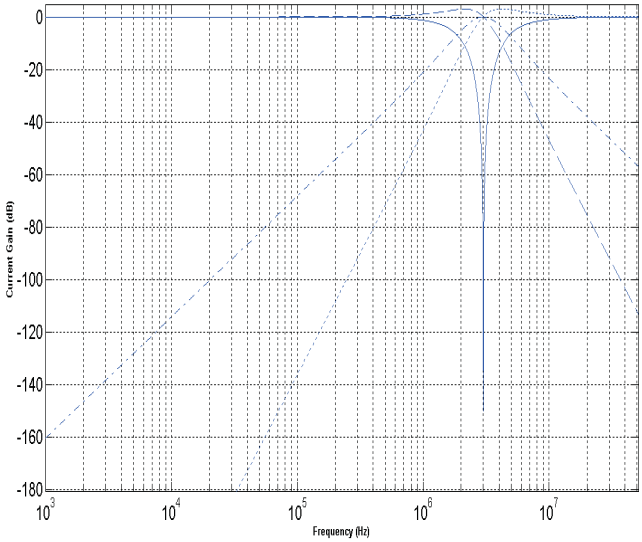


Figure 3.17: Ideal responses of the current-mode universal filter.

Chapter 4

Unity Gain Cells (UGCs)

As it was shown in Chapter 2, the CCs can be designed by superimposing or making cascade connections of Unity Gain Cells (UGC): Voltage Follower (VF), Current Follower (CF), Voltage Mirror (VM) or Current Mirror (CM) [22]. In this section these four UGCs are designed at a transistor level, in order to build each CC.

4.1 Voltage Follower (VF)

The VFs are one of the most indispensable blocks in analog circuits. The ideal VF presents infinite input and zero output impedance, a gain equal to unity and no distortion of the input signal [23, 24]. Its implementation using conventional opamps with unity gain feedback has severe limitations in the input and output voltage swings due to the voltage required for the tail current in the front-end differential amplifier and voltage required for the common drain type at the output stage, respectively [25]. In this work three VFs will be used in order to construct the CCs. These three transistor-based VFs structures are shown in Fig. 4.1.

In order to measure their electrical parameters, the ideal current sources were substituted by simple current mirrors. The VFs presented in this work are class-AB type, which are characterized by a low quiescent power consumption and a high driving capability, taking current from the supply sources only when the load requires it. Therefore class-AB circuits are considered to be good candidates for

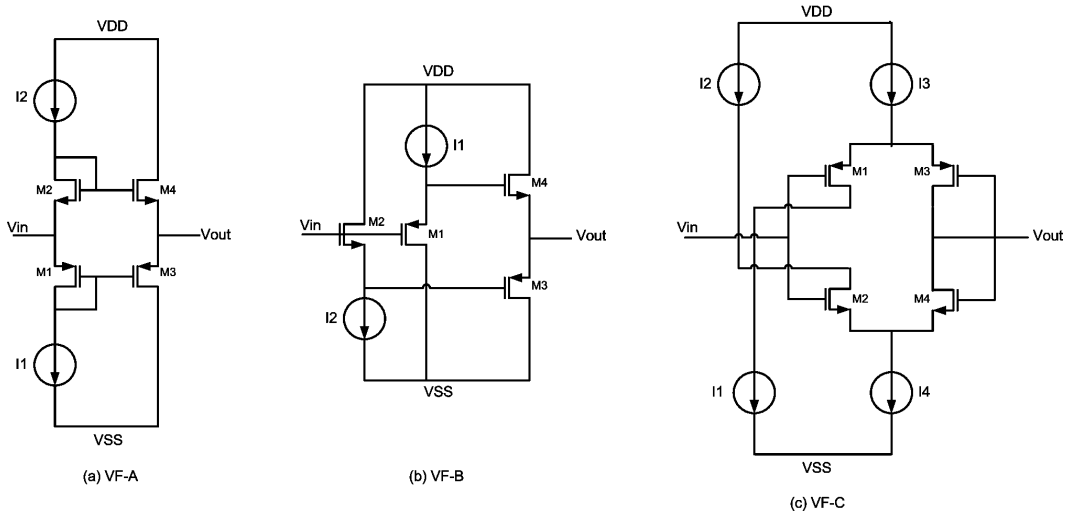


Figure 4.1: Voltage Followers: (a) VF-A, (b) VF-B and (c) VF-C.

low-power analog design [26].

4.1.1 VF-A

This class-AB VF is the most used VF structure in CCs design. It has been reported in [22, 25, 26, 27, 34]. Its implementation with transistor-level bias circuit is shown in Fig. 4.2:

This VF provides good control and high effectiveness in the use of the quiescent current. The circuit has relatively low voltage offset which is determined mainly by transistor mismatch [25].

From Fig. 4.2, M1, M2, M3 and M4 are the core of the VF, while M5-M10 and Mx work as CMs with the only purpose to bias the VF core. The current through M3 and M4 has the same value as the current through M1 and M2, because M5 and M6 are mirroring the $Iref$ current to the branches formed by M7/M8 and M9/M10. When an AC signal is injected to Vin node, it varies the M1 and M2 gate-source voltage (V_{GS1} and V_{GS2}), which produces a variation in the current circulating through these transistors. This current variation is mirrored to the branch formed by M3 and M4, obtaining a voltage variation at Vout node, which is directly proportional to the variation in the Vin node. Because aspect ratios between all NMOS and between all PMOS are equal, the voltage gain in the Vout

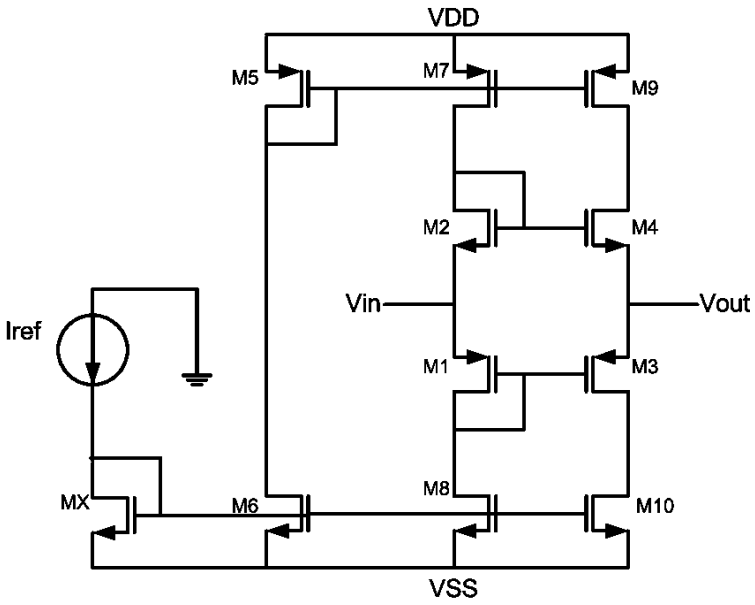


Figure 4.2: VF-A.

node respect to the Vin node is ideally unity. In order to calculate each transistor aspect ratio in the VF-A, one assigns the node voltages in the circuit, which are shown in Fig. 4.3:

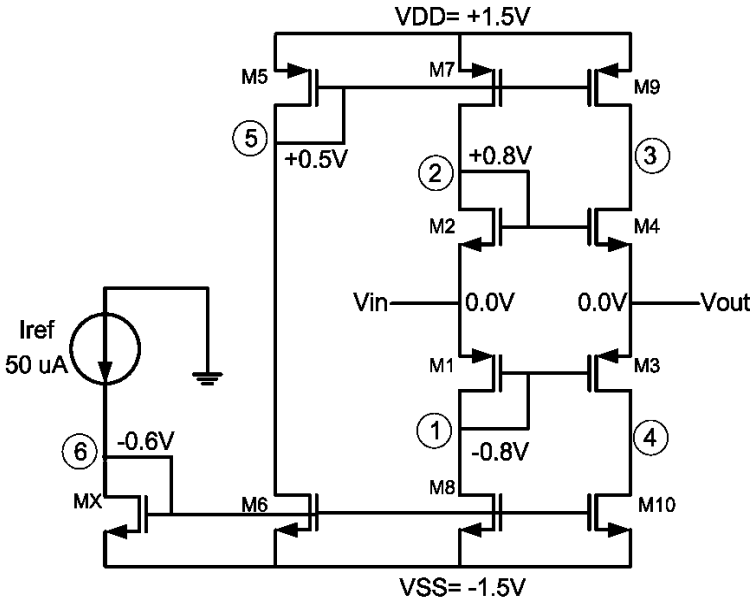


Figure 4.3: VF-A with node voltages.

The bias current or $Iref$ has a value equal to $50\mu A$, the bias voltage $VDD = -VSS = 1.5V$. Using Eqs. (A.12) and (A.18) for NMOS and PMOS, respectively, it's possible to calculate the aspect ratio (W/L) of each transistor. Determining that the channel length of all transistors is equal to $1\mu m$, one obtains the channel width from the following equations:

$$W_n = \frac{2L_n Iref}{K'n\left(V_{GS} - V_{TH}\right)^2} \tag{4.1}$$

$$W_p = \frac{2L_p Iref}{K'p\left(V_{SG} - |V_{TH}|\right)^2} \tag{4.2}$$

Eqs. (4.1) and (4.2) are based on Eqs. (A.11) and (A.18), respectively.
For this work, the technology that is used is $0.35\mu m$, where the Threshold Voltage for NMOS transistors is about $0.6V$ (V_{THn}) and for PMOS is $-0.7V$ (V_{THp}). So, with these parameters it's easy to calculate the W of each transistor. For M2 and M4, $V_{GS2/4}$ must be greater than V_{THn}, so $V_{G2/4} = +0.8V$ and $V_{S2/4} = 0.0V$, so $V_{GS2/4} = 0.8V$ and, due to the fact that this transistor is in a diode connection (M2), one ensures that M2 and M4 will be turned on and in saturation region, where its $V_{DS2/4}(sat) = 0.2V$. The same is for M1 and M3, $V_{SG1/3}$ must be greater than V_{THp}, assigning $V_{G1/3} = -0.8V$ and $V_{S1/3} = 0.0V$, so $V_{SG1/3} = 0.8V$, in order to have $V_{SD1/3}(sat) = 0.1V$. For M6, M8, M10 and Mx, $V_G = -0.6V$ and $V_S = -1.5V$, so $V_{GS} = 0.9V$ that correspond to $V_{DS}(sat) = 0.3V$. For M5, M7 and M9, $V_G = +0.5V$ and $V_S = 1.5V$, so $V_{SG} = 1V$ that correspond to $V_{SD}(sat) = 0.3V$. After this, one ensures that all transistors are in saturation region. All substrate or bulk terminals are connected to VDD or VSS, depending on the transistor type (PMOS or NMOS, respectively). Substituting all of this V_{GS} and V_{SG} in Eq. (4.1) and (4.2), one obtains the channel width of all transistors, which are shown in Table 4.1 with voltage gain, input/output resistance, output voltage offset, bandwidth and DC transfer curve.

4.1.2 VF-B

The second class AB VF used in this work, described in [23, 28, 29, 34], is shown in Fig. 4.4 at transistor level. The VF core is formed by M1-M4, connected in two common drain stages, which are biased by current mirrors implemented by both NMOS and PMOS transistors (M6/M8/Mx and M5/M7, respectively). The positive voltage following is made by transistors M2 and M3, while negative voltage following is made by transistors M1 and M4.

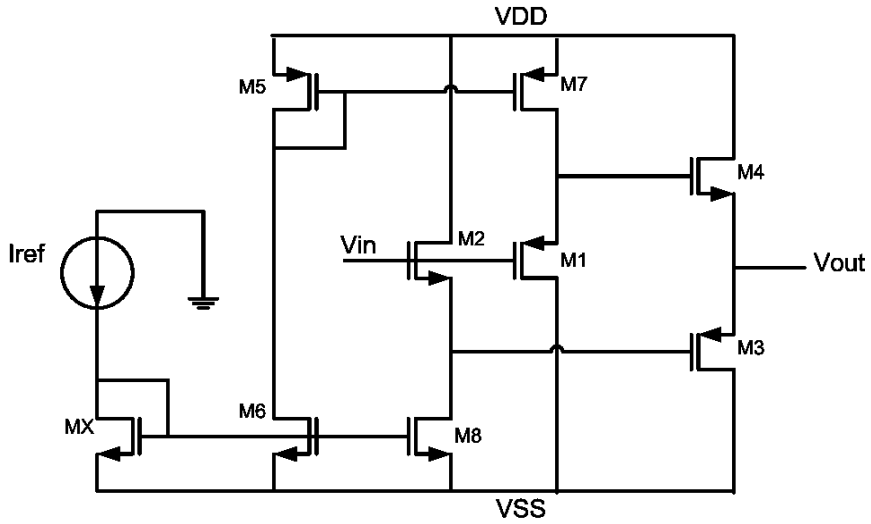


Figure 4.4: VF-B.

This VF needs a good matching between each transistor couple, due to the fact that the Threshold Voltage is the responsible for a low offset voltage and an unity voltage gain. This topology can be only implemented in a double well technology in order to reduce the body effect (refer to Appendix A). In the way to implement this topology in an one well technology, a compensation technique must be considered, because the body effect directly impact in the Threshold voltage increase in the NMOS transistors [30]. As in the VF-A, one assigns the node voltages to the circuit, shown in Fig. 4.5, in order to obtain the channel width (W). The $Iref$ current, VDD and VSS for this VF and for all circuits in this thesis have the same values as in VF-A ($Iref = 50\mu A$, $VDD = -VSS = 1.5V$).

From Fig. 4.5, for M2, $V_{GS2} = 0.8V$ that results in a $V_{DS2}(sat) = 0.2V$; for M1, $V_{SG1} = 0.8V$ that results in a $V_{SD1}(sat) = 0.1V$. For M3, $V_{SG3} = 0.8V$

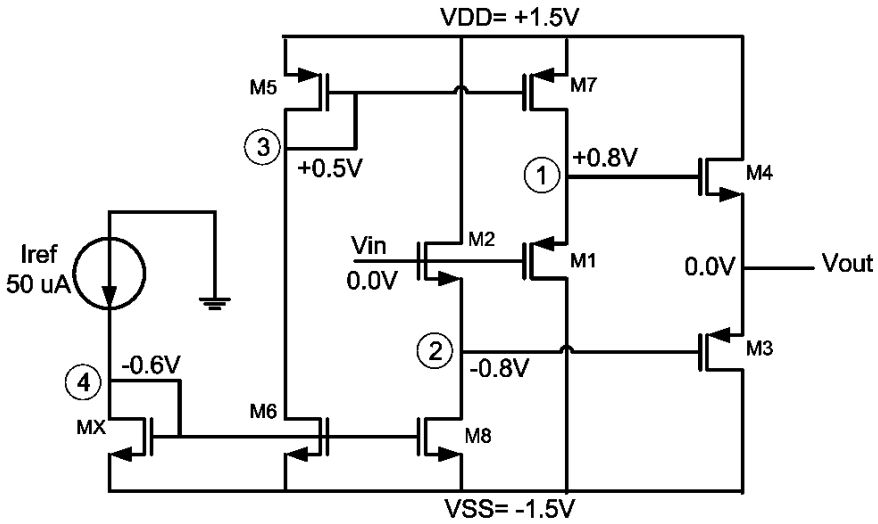


Figure 4.5: VF-B with node voltages.

with $V_{SD3} = 0.1V$ and for M4, $V_{GS4} = 0.8V$ which results in $V_{DS4} = 0.2V$. As it was said before, this four transistors have connected their bulk terminal to the source terminal, in order to avoid the body effect, keeping the Threshold voltage in a low level and as a consequence to maintain them on. For the CMs that bias the VF core, the NMOS transistors (Mx, M6 and M8) have a $V_{GS} = 0.9V$ with a $V_{SD}(sat) = 0.4V$. For the PMOS transistors (M7 and M7) $V_{SG} = 1V$ which results in a $V_{SD}(sat) = 0.3V$. With this results all transistors are in the saturation region. Substituting all of this V_{GS} and V_{SG} in Eq. (4.1) and (4.2), one obtains the channel width of all transistors. The electrical parameters as voltage gain, input/output resistance, output voltage offset, bandwidth and DC transfer curve are shown in Table 4.1.

4.1.3 VF-C

The circuit of Fig. 4.6 is a new class AB voltage buffer that is based on the Differential Flipped VF (DFVF) circuit reported in [27, 31, 32, 33, 34]. The VF core is formed by M1-M4, with a quiescent current of $Iref/2$. The bias CM circuit is formed by the NMOS transistors M6/8 and Mx, and the PMOS transistors M5/7.

The circuit works as follows: From Fig. 4.7, when the input signal in Vin

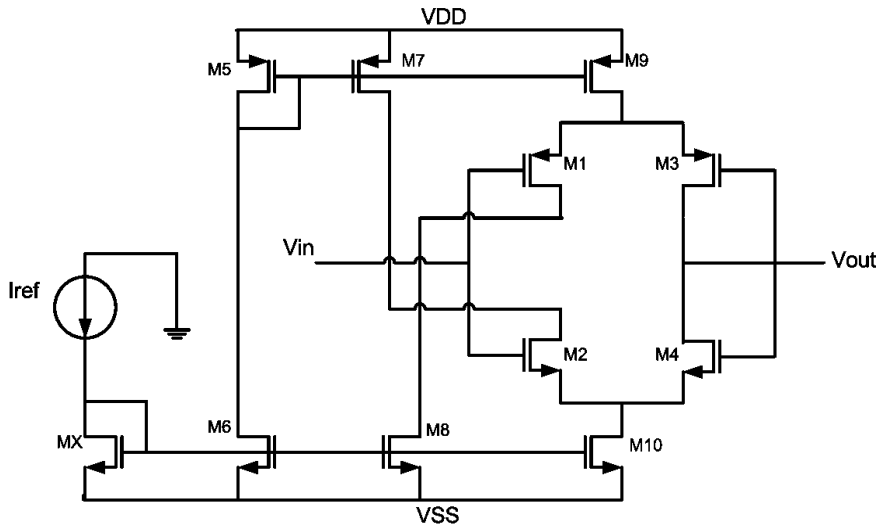


Figure 4.6: VF-C.

node increases with respect to the output voltage in $Vout$ node, nodes 1 and 2 also follow this variation. This way V_{SG3} increases and V_{GS4} decreases. This causes the current through M3 to increase and the current through M4 to decrease. This generates a positive output current that charges the load at $Vout$ node, and increases the output voltage, until it reaches a value of the input voltage. A similar situation arises when the input voltage decreases with respect to the output voltage. The proposed buffer operates in class-AB given that the transient current of the output transistors M3 and M4 can be much larger than their quiescent current $Iref/2$ [31].

From Fig. 4.7 and, as it was done with VF-A and VF-B, one assigns node voltages in order to be able to calculate the channel width of each transistor. Opposite to the VF-B, in this VF all substrate or bulk terminals are connected to VDD or VSS, depending of the transistor type. Substituting all V_{GS} and V_{SG} in Eq. (4.1) and (4.2), one obtains the channel width of all transistors. The electrical parameters as voltage gain, input/output resistance, output voltage offset, bandwidth and DC transfer curve are shown in Table 4.1.

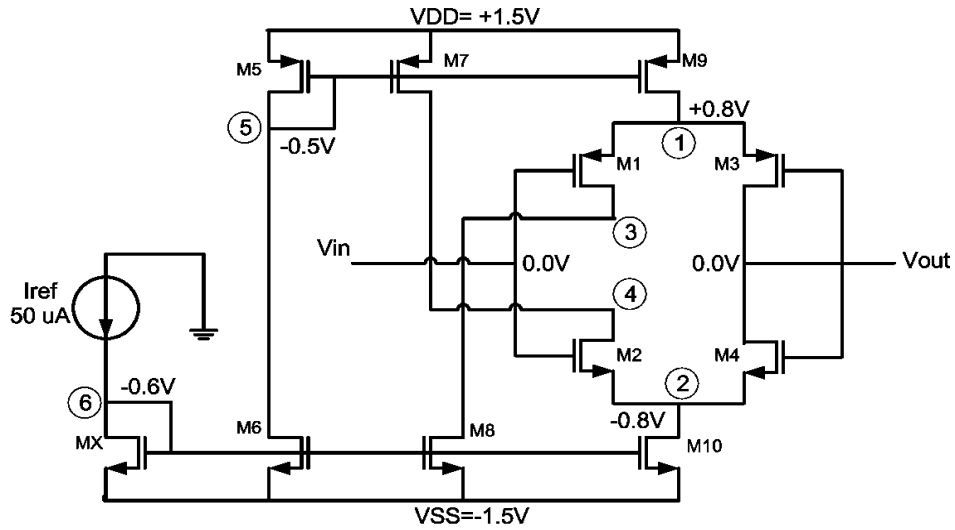


Figure 4.7: VF-C with node voltages.

4.1.4 VFs Measurements

The channel width W, voltage gain Av, input/output resistance $Rin/Rout$, output voltage offset V_{offset}, bandwidth BW_V and DC transfer curve of the three VFs are shown in Table 4.1.

Table 4.1: VFs electrical parameter measurements.

		VF-A	VF-B	VF-C
PMOS W (μm)	**M1, M3**	192	300	96.15
	M5	21.36	21.26	21.36
	M7	21.36	21.26	10.68
	M9	21.36	—	21.36
NMOS W (μm)	**M2, M4**	26	11.75	12.5
	M6, Mx	11.11	11.11	11.11
	M8	11.11	11.11	5.55
	M10	11.11	—	11.11
DC	**Rin** ($K\Omega$)	92.19	∞	∞
	Rout (Ω)	931.47	811.26	5K
	$\mathbf{V_{offset}}$ (μV)	11.11	11.11	5.55
	Trans. Curve. (V)	$\pm$400	$\pm$600	$\pm$400
AC	$\mathbf{A_v}$	0.989	0.990	0.979
	$\mathbf{BW_v}$ (MHz)	99	95	34

4.2 Current Mirror (CM)

Current Mirrors (CM) are the basic building blocks of current-mode circuits, suitable for low-voltage high speed analog signal processing [35]. Recently low power and low voltage analog and mixed mode circuits have gained importance, especially for portable electronics and mobile communication systems. In all analog and mixed mode VLSI circuits, a CM is an integral part of a signal processing elements like opamps, current feedback amplifiers, CCs, etc. [36]. True to its name, a CM performs the similar functions with electrical currents as a plane optical mirror does for optical signals. The CM reverses the direction of current, injected into a low impedance input port and allows its true or scaled version to flow into a high impedance output port [37]. The CM uses the principle that if the V_{GS} of two identical MOS transistors are equal, the channel currents should be equal. Fig. 4.8 shows the implementation of a simple NMOS CM. The i_{in} current is assumed to be defined by a current source and i_{out} is the output "mirrored" current. M1 is in saturation, because it is in a diode connection, that is

$V_{GS1} = V_{DS1}$ [21]. Assuming that $V_{DS2} > (V_{GS2} - V_{TH2})$, is correct to use the saturation region equation (Eq. (A.12)). The ratio of i_{out} to i_{in} is as follows:

$$\frac{i_{out}}{i_{in}} = \left(\frac{L_1 W_2}{W_1 L_2}\right)\left(\frac{V_{GS} - V_{TH2}}{V_{GS} - V_{TH1}}\right)^2 \left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\left(\frac{K'_2}{K'_1}\right)\right] \tag{4.3}$$

All the components of a CM are processed on the same integrated circuit, so all the physical parameters, such as V_{TH} and K' are identical for both type of devices. As a result, and if $V_{DS2} = V_{DS1}$, the ratio of Eq. (4.3) can be simplified by:

$$\frac{i_{out}}{i_{in}} = \frac{L_1 W_2}{W_1 L_2} \tag{4.4}$$

So in Eq. (4.4), i_{out}/i_{in} is a function of the aspect ratios that are under designer control.

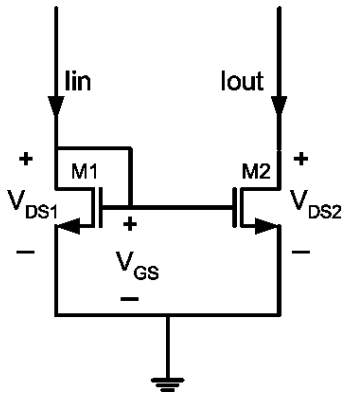


Figure 4.8: NMOS Current Mirror.

4.2.1 Simple CM (SCM)

The simplest symmetrical CM is based on the circuit shown in Fig. 4.8, just adding the same structure by PMOS transistors at the top of that circuit, to have

the Simple symmetrical CM or Simple CM (SCM) shown in Fig. 4.9, which will be used in this work. Substituting all V_{GS} and V_{SG} in Eq. (4.1) and (4.2), one obtains the channel width of all transistors. The electrical parameters as current gain, input/output resistance, output current offset, bandwidth and DC transfer curve are shown in Table 4.2.

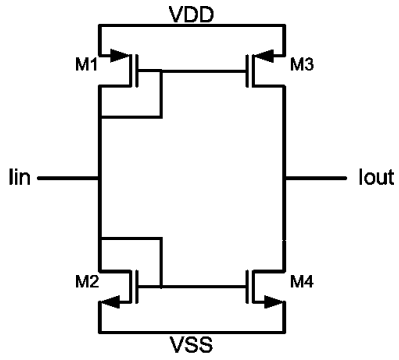


Figure 4.9: Simple Current Mirror.

4.2.2 Low Voltage CM (LVCM)

One of the most important disadvantages of the SCM is its poor output impedance and linearity worsening with smaller channel length designs [38]. Now is presented the commonly named Wide-swing or Low-voltage Cascode CM (LVCM) [38, 39, 40, 41, 42]. Its topology is shown in Fig. 4.10. In this work is not used the very popular Cascode CM, because of the low value of the bias voltages (VDD and VSS). On its place it was chosen the low voltage version of that CM. The V_{DS1} and V_{DS2} are controlled by the gate of transistors M4 and M3, respectively. So, the V_{DS1} and V_{DS2} are not equal to its V_{GS1} or V_{GS2} for each case. The matching between these two elements ensure identical voltage at the drains of these transistors (M1 and M2), leading to a systematic current matching. The gates terminals of M3 and M4 are biased by a control voltage (Vb) that maintain both M1 and M2 in the saturation region. This voltage avoid M4 to move to the triode region [43]. In order to agree with this, the voltages relations given by Eqs. (4.5) and (4.6).

$$Vb - V_{TH4} - V_{DS4}(sat) > V_{DS1}(sat) \tag{4.5}$$

$$Vb - V_{DS1} - V_{TH4} < V_{TH1} + V_{DS1}(sat) - V_{DS1} \tag{4.6}$$

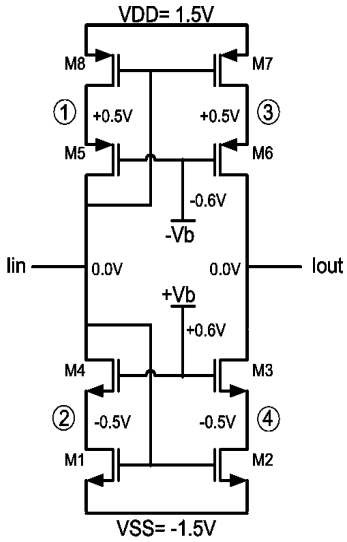


Figure 4.10: Low Voltage Current Mirror.

As it was done with the VFs, once are assigned the nodes voltages in order to keep all transistors in the saturation region, is quite simple to calculate the channel width (W) dimensions for all transistors. The control voltage Vb has a value of $0.6V$. The electrical parameters as current gain, input/output resistance, output current offset, bandwidth and DC transfer curve are shown in Table 4.2.

4.2.3 Cascode and Wilson CM

The output resistance can be increased by using either Cascode or Wilson CM. These CMs have the disadvantage of reduced signal swing [20]. More over, these types of topologies require greater bias voltages than the two CMs seen before, as a consequence these topologies are not suitable for low voltage applications. The Cascode and Wilson CM topologies are shown in Fig. 4.11.

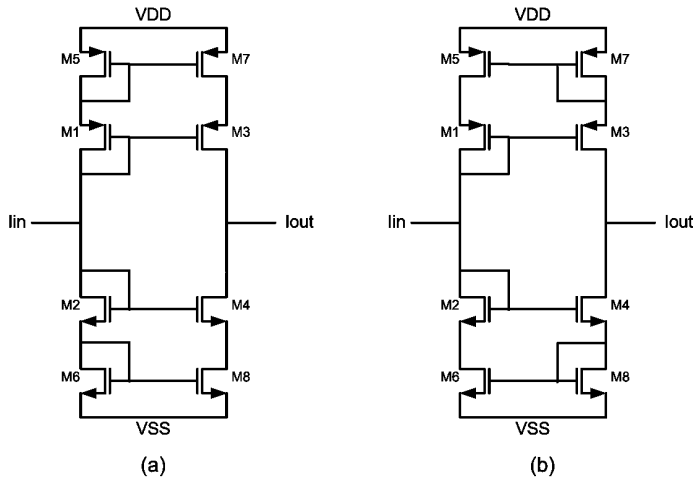


Figure 4.11: (a) Cascode and (b) Wilson Current Mirrors.

4.2.4 CMs Measurements

The channel width W, current gain A_i, input/output resistance $Rin/Rout$, output current offset I_{offset}, bandwidth BW_i and DC transfer curve of the Simple and Low Voltage CMs are shown in Table 4.2.

Table 4.2: CMs electrical parameter measurements.

		SCM	**LVCM**
PMOS W (μm)	**M1**	3	12
	M3	3	3
	M5	—	12
	M7	—	3
NMOS W (μm)	**M2**	1.2	4
	M4	1.2	1.2
	M6	—	4
	M8	—	1.2
DC	**Rin** ($K\Omega$)	5.13	6.15
	Rout ($M\Omega$)	0.346	13.15
	$\mathbf{I_{offset}}$ (nA)	-348	-5.8
	Trans. Curve (μA)	$\pm$200	$\pm$130
AC	$\mathbf{A_i}$	0.983	0.999
	$\mathbf{BW_i}$ (MHz)	855	550

4.3 Voltage Mirror (VM)

A VM is simply a VF with an inverting block at its input terminal. This inverting block can just be a CMOS transistor in a common-source configuration, with its active load. This is shown in the Fig. 4.12. The input stage is formed by MA and MB, in other words gm_A and gm_B which are single input single output transconductances. The next stage is the VF with a negative feedback that minimize the input impedance at the output terminal [44].

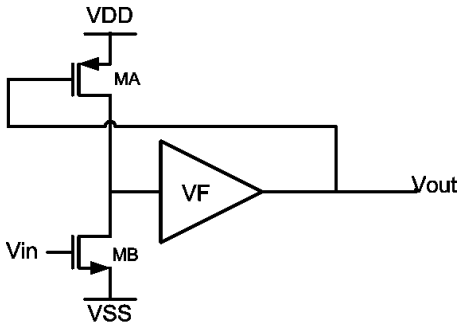
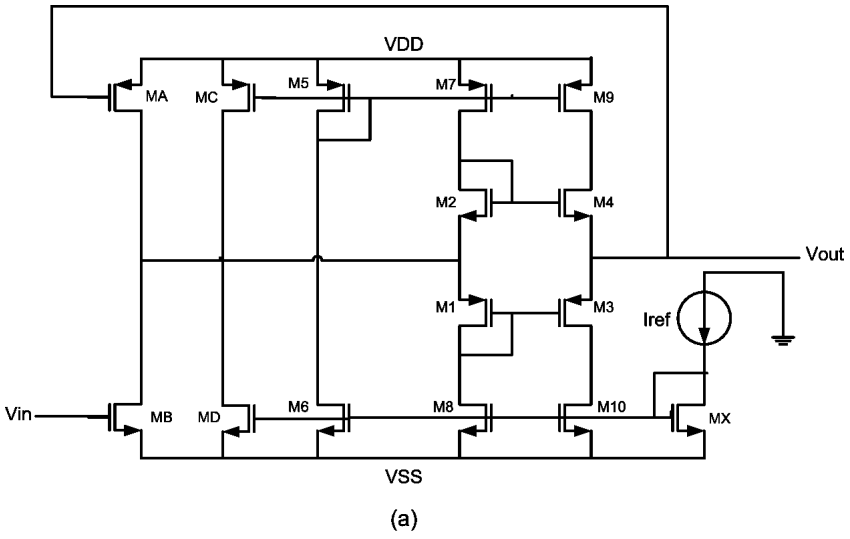


Figure 4.12: Voltage Mirror.

Using the three analyzed VFs, one obtains three different VMs. These VMs are shown at transistor level.

From Fig. 4.13, each VF has connected four transistors at its input terminal, where MA/MB are the inverting stage and MC/MD compensate the offset gen-



(a)

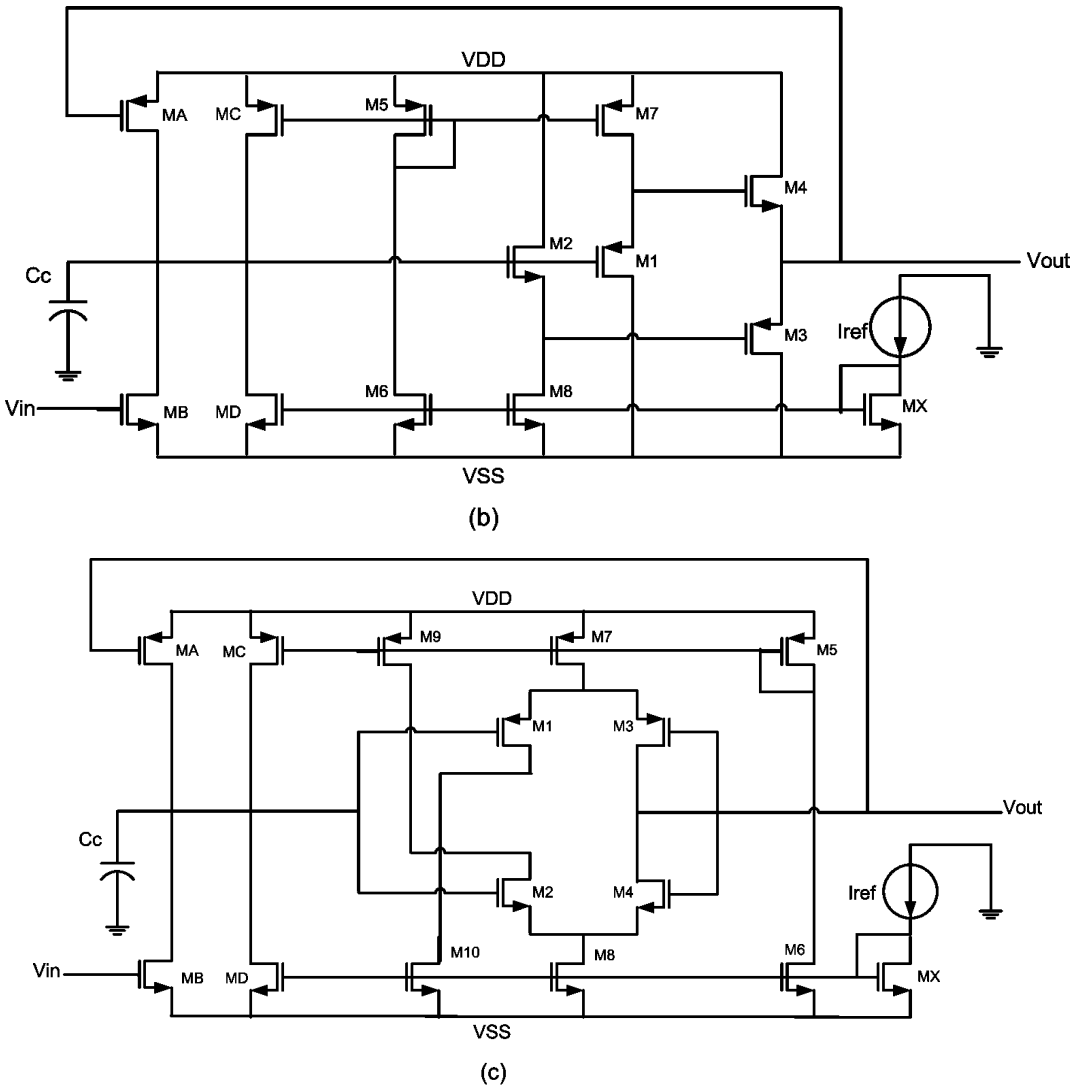


Figure 4.13: Voltage Mirror: (a) VM-A, (b) VM-B and (c) VM-C.

erated by MA and MB. The offset in the gates terminals of M1 and M2 is fixed by the feedback between $Vout$ node and the gate terminal of MA. MC and MD drain a current that generates a voltage in that node that compensates the fixed offset. VM-B and VM-C have a capacitor named Cc in order to smooth the AC response near the cut-off frequency. At this point, without Cc, VM-B and VM-C present a peak of some units of dB, making these circuits unstable. The reason is due to the connection of the inverted stage output with the M1 and M2 gates, which represents a very high impedance at this point.

4.3.1 VMs Measurements

The channel width W, current gain A_i, input/output resistance $Rin/Rout$, output current offset I_{offset}, bandwidth BW_i and DC transfer curve of the CMs are shown in Table 4.3.

Table 4.3: VMs electrical parameter measurements.

		VM-A	**VM-B**	**VM-C**
PMOS W (μm)	**M1, M3**	192.31	300	21.36
	M5	192.31	21.26	21.36
	M7	192.31	21.26	42.7
	M9	192.31	—	21.36
	MA	9	9	9
	MC	192.31	23.75	21.36
NMOS W (μm)	**M2, M4**	100	11.75	6.25
	M6, Mx	100	11.11	25
	M8	100	11.11	50
	M10	100	—	25
	MB	3	3	3
	MD	41.7	5	8.35
DC	**Rin** ($K\Omega$)	∞	∞	∞
	Rout (Ω)	50.82	31	172.5
	$\mathbf{V_{offset}}$ (μV)	-70	-7.11	-450
	Trans. Curve (V)	$\pm$300	$\pm$400	$\pm$350
AC	$\mathbf{A_v}$	-0.957	-0.987	-0.986
	$\mathbf{BW_v}$ (MHz)	18	63	26.6

4.4 Current Follower (CF)

A CF can be made by adding two CMs. By connecting two CMs in serie, the input signal will be mirrored twice, so at the output node the signal will have a phase equal to 0°, as it is shown in Fig. 4.14. In [44, 45, 46, 47, 48] are presented some asymmetrical CFs topologies. The scope of this work is to build CCs based in symmetrical UGCs, so the simplest way to design a CF is to add two CMs.

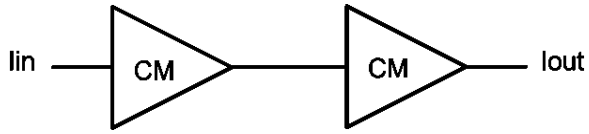
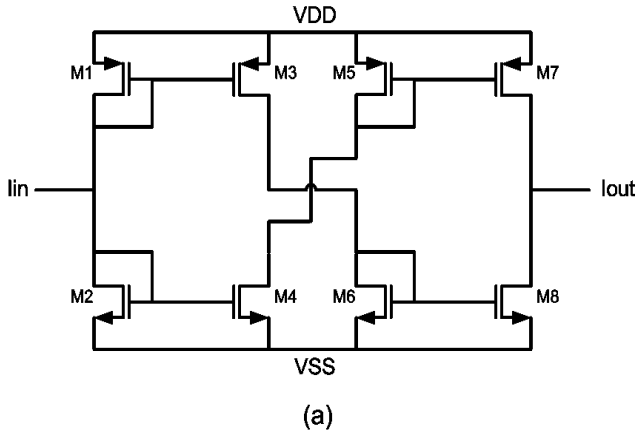


Figure 4.14: Current Mirror based Current Follower.

So, as it is shown in Fig. 4.14, and taking the Simple and Low Voltage CMs, it is possible to obtain two types of CFs, these are shown in Fig. 4.15. Taking the Cascode and Wilson CMs, it is possible too to design a CF, following the same structure shown in Fig. 4.15.

4.4.1 CFs Measurements

The channel width W, current gain A_i, input/output resistance $Rin/Rout$, output current offset I_{offset}, bandwidth BW_i and DC transfer curve of the CMs are shown in Table 4.4.



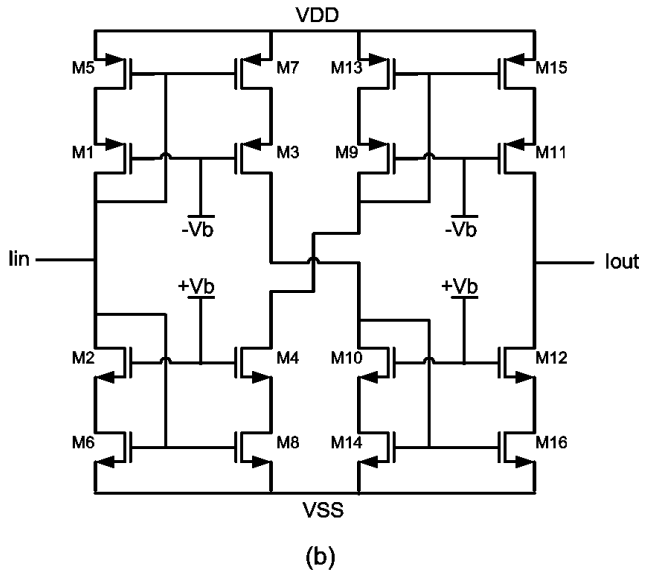


Figure 4.15: (a) Simple and (b) Low Voltage Current Followers.

Table 4.4: CFs electrical parameter measurements.

		SCF	**LVCF**
PMOS W (μm)	**M1, M3**	3	12
	M5, M7	3	3
	M9, M11	—	12
	M13, M15	—	3
NMOS W (μm)	**M2, M4**	1.23	4
	M6, M8	1.23	1.2
	M10, M12	—	4
	M14, M16	—	1.2
DC	**Rin** ($K\Omega$)	5.13	6.15
	Rout ($M\Omega$)	0.346	13.15
	$\mathbf{I_{offset}}$ (nA)	-348	-5.8
	Trans. Curve (μA)	$\pm$120	$\pm$100
AC	$\mathbf{A_i}$	-0.954	-0.998
	$\mathbf{BW_i}$ (MHz)	478	345

Chapter 5

Direct and Inverse Current Conveyors

The CC is a basic building block that can be implemented in analog circuit design. It also represents an effective alternative to the opamps designers, due to the fact that practical CCs are marked by characteristics that are very close to the ideal one. More over, with the growing diffusion of the current-mode approach as a way to design low-voltage low-power circuits, CCs have gained an increased popularity [4].

In orther to classify all CCs, and since all CCs will be Dual-output type, they will be named in the following order:
CC Type - VF or VM type - CM and CF type.

An example of the nomenclature will be:

$$DOCCI - VFA - S$$

It indicates a Dual-output First Generation CC, based in the VFA and Simple CMs and CFs. In order to name a Dual-output Third Generation CC, VFC and Low Voltage CMs and CFs based, the nomenclature will be:

$$DOCCIII - VFC - LV$$

5.1 Direct Current Conveyors

5.1.1 Direct First Generation Current Conveyor (CCI)

The behavior and structure of the CCI was described in Chapter 2 by Eq. (2.1) and Fig. 2.2, respectively. In order to implement a CCI with a CMOS transistor-based circuit, it is necessary to join a VF with two CMs (CCI+) or a VF with a CM and a CF (CCI-). A Double-output CCI (DOCCI) block structure is shown in Fig. 5.1, which is based in the VF-A. Of course, it can be based in the VF-B or VF-C circuits.

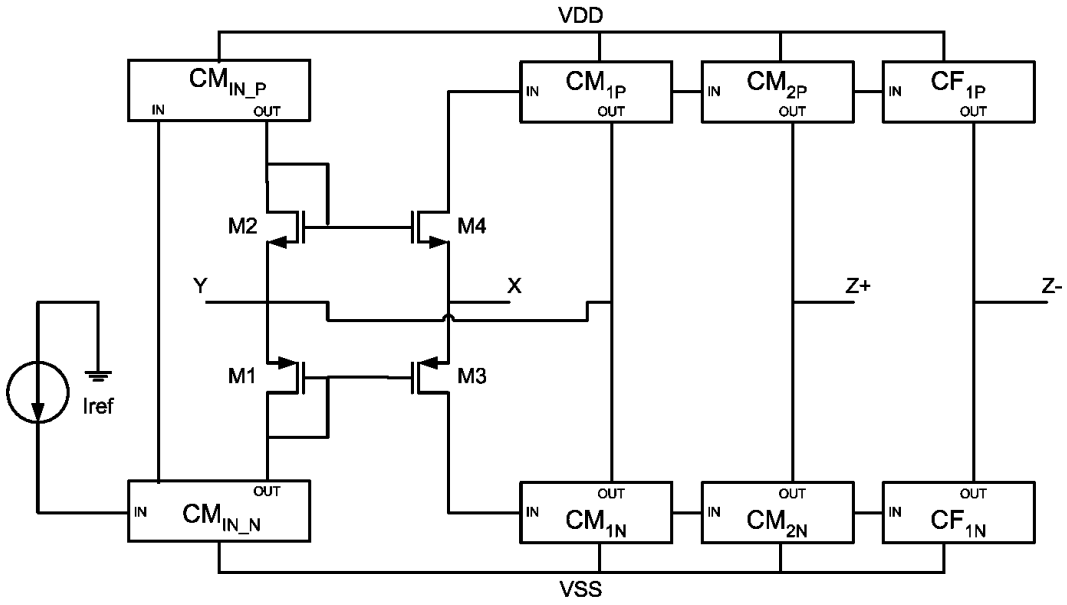


Figure 5.1: DOCCI structure.

Where, in Fig. 5.1, CM_{IN_P} and CM_{IN_N} are formed by M5/M7 and M6/M8 respectively, and its purpose is to bias the VF. CM_{1P} and CM_{1N} are the first Current Mirror for $i_y = ix$. CM_{2P} and CM_{2N} are the second Current Mirror for $i_z = ix$. Finally CF_{1P} and CF_{1N} are the first Current Follower for $i_z = -ix$.
For a complete transistor level, in Fig. 5.2 is shown a DOCCI based in the VFA, SCM and SCF, where CM_{1P} and CM_{1N} is formed by M9/M11 and M10/M12, respectively. CM_{2P} and CM_{2N} is formed by M9/M13 and M10/M14, respectively. Finally CF_{1P} and CF_{1N} is formed by M9/M15/M17/M19 and M10/M16/M18/M20,

respectively.

Then, if is used the same VFA, but now with LVCMs and a LVCFs, the DOCCI-VFA-LV is obtained, which is shown in Fig. 5.3. Now CM_{1P} and CM_{1N} is formed by M13/M15/M17/M19 and M14/M16/M18/M20. CM_{2P} and CM_{2N} is formed by M13/M15/M21/M23 and M14/M16/M22/M24. Finally CF_{1P} and CF_{1N} is formed by M13/M15/M25/M27/M29/M31/M33/M35 and M14/M16/M26/M28/M30/M32/M34/M36, respectively.

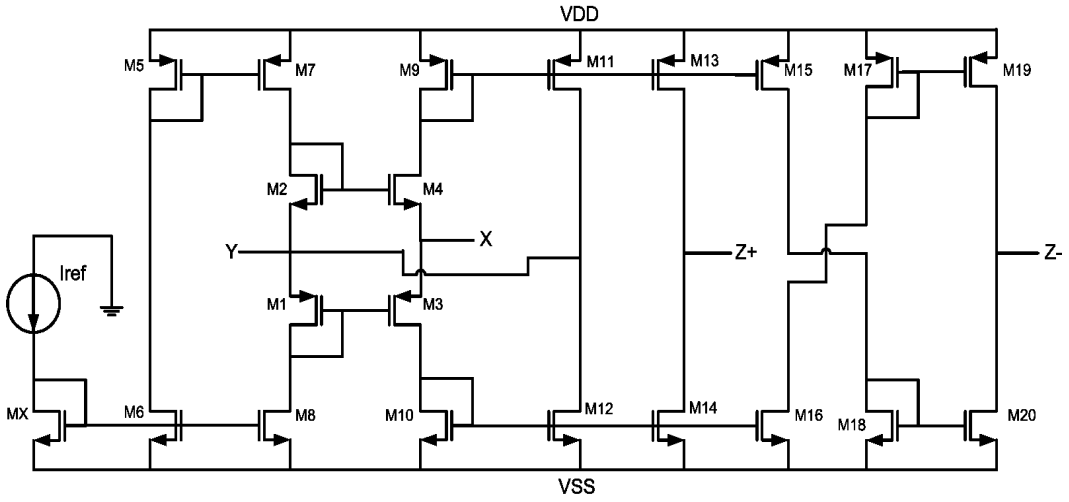


Figure 5.2: DOCCI-VFA-S

Combining the three VFs with the Simple and Low Voltage CMs and CF, six different DOCCIs are obtained. These six CCs are shown in transistor level in Appendix B. The channel Length (L) for all transistors is $1\mu m$. The channel width of all transistors is shown in table 5.1. The electrical measurements made for these six DOCCIs are shown from table 5.2 to 5.7.

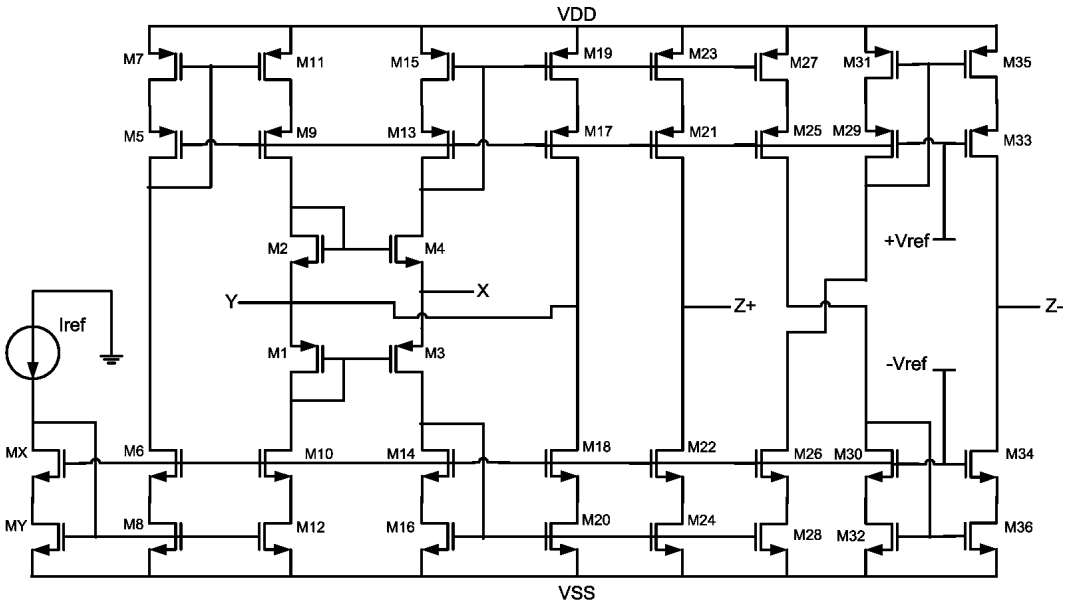


Figure 5.3: DOCCI-VFA-LV

Table 5.1: DOCCI channel width (W) dimensions.

DOCCI							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	150	21.35	50
	M3	192.35	48	50	150	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15,19	192.35	48	7	192.35	192.35	4
	M21,25,29,33	—	—	—	192.35	192.35	6
	M23,27,31,35	—	—	—	192.35	192.35	4
NMOS	M2	100	6.25	30	50	6.25	40
	M4	100	2.25	30	50	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16,20	100	11.11	1.5	100	100	1
	M22,26,30,34	—	—	—	100	100	3
	M24,28,32,36	—	—	—	100	100	1
	My	—	—	—	100	100	10

Table 5.2: DOCCI-VFA-S electrical parameter measurements

DOCCI-VFA-S					
Term. Resistance		$R_y = 81.2K\Omega$	$R_x = 510.44\Omega$	$R_{z+} = 240.13K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.3	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	2.64	0.131	-0.728
	$\mathbf{I_{T.C.}}$ (mA)	—	± 14	± 14	± 6
$\mathbf{AC_v}$	**Gain** (V/V)	0.993	—	—	—
	$\mathbf{BW_v}$ (MHz)	91	—	—	—
	Onoise ($V/(Hz)^{1/2}$)	$4.3p$	—	—	—
	Inoise ($V/(Hz)^{1/2}$)	2.2μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.02	1.02	-1.08
	$\mathbf{BW_i}$ (MHz)	—	59.6	49.2	40.8
	Onoise ($V/(Hz)^{1/2}$)	—	$4.2p$	$4.17p$	$4.32p$
	Inoise ($V/(Hz)^{1/2}$)	—	$4.17n$	$4.06n$	$3.99n$
$\mathbf{Tran_v}$	**SR** ($V/\mu seg$)	50.19	—	—	—
	ST ($nseg$)	17	—	—	—
	THD (%)	1.48	—	—	—
	SNR (dB)	-80.4	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	9730	9030	-8180
	ST ($nseg$)	—	15	15	17.3
	THD (%)	—	0.185	0.06	0.089
	SNR (dB)	—	-28	-40	-40

Table 5.3: DOCCI-VFB-S electrical parameter measurements

DOCCI-VFB-S					
Term. Resistance		$R_y = 467.18K\Omega$	$R_x = 2.13K\Omega$	$R_{z+} = 472.59K\Omega$	$R_{z-} = 457.09K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.72	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	0.393	0.393	-0.576
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.75	± 0.75	± 0.75
$\mathbf{AC_v}$	**Gain** (V/V)	0.978	—	—	—
	$\mathbf{BW_v}$ (MHz)	66.8	—	—	—
	Onoise ($V/(Hz)^{1/2}$)	5.77μ	—	—	—
	Inoise ($V/(Hz)^{1/2}$)	5.9μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.015	1.015	-1.04
	$\mathbf{BW_i}$ (MHz)	—	129	122	88.7
	Onoise ($V/(Hz)^{1/2}$)	—	$7.030n$	$7.030n$	$7.030n$
	Inoise ($V/(Hz)^{1/2}$)	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** ($V/\mu seg$)	37.8	—	—	—
	ST ($nseg$)	18.5	—	—	—
	THD (%)	1.33	—	—	—
	SNR (dB)	-96.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	3250	11325	-11746
	ST ($nseg$)	—	10.8	10	24.3
	THD (%)	—	0.207	0.206	0.475
	SNR (dB)	—	-40	-50.4	-74

Table 5.4: DOCCI-VFC-S electrical parameter measurements

DOCCI-VFC-S					
Term. Resistance		$R_y = 283.79K\Omega$	$R_x = 2.88K\Omega$	$R_{z+} = 704.38K\Omega$	$R_{z-} = 697.95K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	-0.877	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	±500	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	0.613	0.613	-0.658
	$\mathbf{I_{T.C.}}$ (mA)	—	±0.05	±0.05	±0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.990	—	—	—
	$\mathbf{BW_v}$ (MHz)	39.3	—	—	—
	Onoise $(V/(Hz)^{1/2})$	3.02μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	3.05μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	0.997	0.997	-1.0048
	$\mathbf{BW_i}$ (MHz)	—	96.2	79	75.6
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** ($V/\mu seg$)	31.23	—	—	—
	ST ($nseg$)	33.1	—	—	—
	THD (%)	1.24	—	—	—
	SNR (dB)	-91.3	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	6910	9370	-10320
	ST ($nseg$)	—	65	75	72
	THD (%)	—	0.714	0.690	0.773
	SNR (dB)	—	-47.3	-57.5	-56.8

Table 5.5: DOCCI-VFA-LV electrical parameter measurements

DOCCI-VFA-LV					
Term. Resistance		$R_y = 1.11M\Omega$	$R_x = 599.1\Omega$	$R_{z+} = 11.6M\Omega$	$R_{z-} = 11.59M\Omega$
Vref		$\pm 0.5V$			
Analysis ($Vref = \pm 0.5V$)		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	44.7	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	±400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	51.13	56.46	-55.44
	$\mathbf{I_{T.C.}}$ (mA)	—	±0.3	±0.3	±0.3
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—	—
	$\mathbf{BW_v}$ (MHz)	90.3	—	—	—
	Onoise $(V/(Hz)^{1/2})$	1.053μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	1.056μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.00	1.00	-1.00
	$\mathbf{BW_i}$ (MHz)	—	65	53.5	57
	Onoise $(V/(Hz)^{1/2})$	—	$4.27p$	$4.16p$	$4.27p$
	Inoise $(V/(Hz)^{1/2})$	—	$4.26n$	$4.15n$	$4.24n$
$\mathbf{Tran_v}$	**SR** ($V/\mu seg$)	51.3	—	—	—
	ST ($nseg$)	17.4	—	—	—
	THD (%)	2.06	—	—	—
	SNR (dB)	-78.6	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	12800	9900	-8019
	ST ($nseg$)	—	14.3	8.7	12.4
	THD (%)	—	0.145	0.133	0.149
	SNR (dB)	—	-40.6	-75.1	-74.0

Table 5.6: DOCCI-VFB-LV electrical parameter measurements

DOCCI-VFB-LV					
Term. Resistance		$R_y = 11.25M\Omega$	$R_x = 841.02\Omega$	$R_{z+} = 12M\Omega$	$R_{z-} = 11.98M\Omega$
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	771	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	**Ioffset** (nA)	—	43.75	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.5	± 0.5	± 0.5
$\mathbf{AC_v}$	**Gain** (V/V)	0.989	—	—	—
	$\mathbf{BW_v}$ (MHz)	86.7	—	—	—
	Onoise $(V/(Hz)^{1/2})$	4.67μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	4.72μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.00	1.00	-1.00
	$\mathbf{BW_i}$ (MHz)	—	89.6	88.2	86.8
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	56	—	—	—
	ST $(nseg)$	25	—	—	—
	THD (%)	0.89	—	—	—
	SNR (dB)	-78.0	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	8390	11300	-10147
	ST $(nseg)$	—	10	15.4	18.3
	THD (%)	—	0.075	0.077	0.123
	SNR (dB)	—	-72.3	-74.2	-72.4

Table 5.7: DOCCI-VFC-LV electrical parameter measurements

DOCCI-VFC-LV					
Term. Resistance		$R_y = 8.64M\Omega$	$R_x = 2.74K\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-223	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 500	—	—	—
$\mathbf{DC_i}$	**Ioffset** (nA)	—	13.53	10.07	-13.53
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—	—
	$\mathbf{BW_v}$ (MHz)	38.2	—	—	—
	Onoise $(V/(Hz)^{1/2})$	2.51μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	2.53μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0002	1.0002	-1.0012
	$\mathbf{BW_i}$ (MHz)	—	83.1	67.2	66.8
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	26.92	—	—	—
	ST $(nseg)$	38.3	—	—	—
	THD (%)	0.651	—	—	—
	SNR (dB)	-88.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	7630	8096	-8395
	ST $(nseg)$	—	88.4	91.7	85.5
	THD (%)	—	0.938	0.912	1.07
	SNR (dB)	—	-58.4	-56.1	-55.3

5.1.2 Direct Second Generation Current Conveyor (CCII)

The behavior (Eq. (2.3)) and structure (Fig. 2.6) of the CCII was already described in Chapter 2. So remembering from this chapter, in the way to implement a CCII with CMOS transistors, it is necessary to join a VF with a CM (CCI+) or a VF with a CF (CCI-). A DOCCII block structure is shown in Fig. 5.4, which is based in the VF-B.

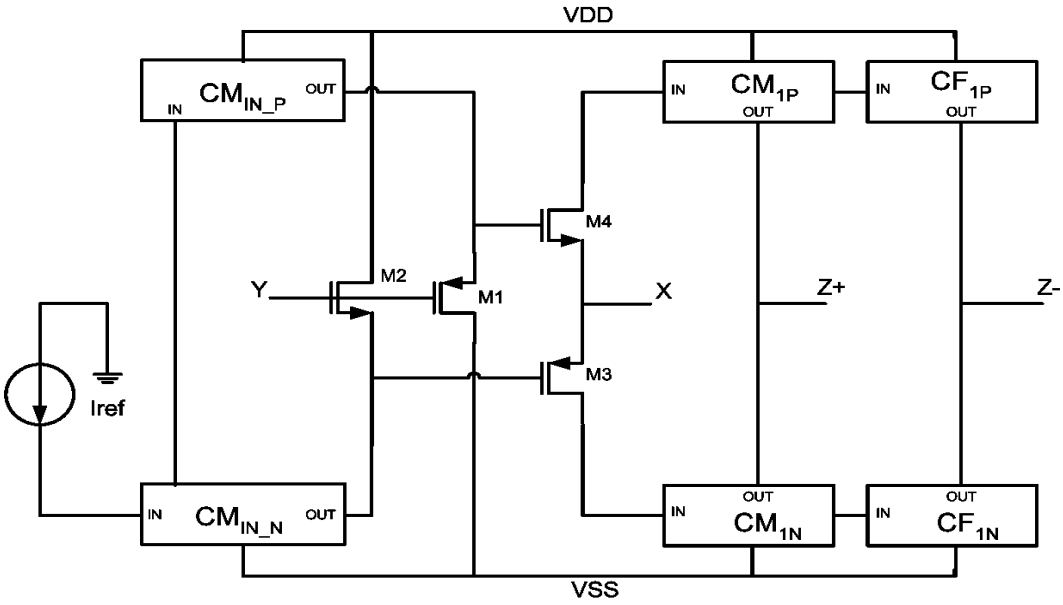


Figure 5.4: DOCCI structure.

Where, in Fig. 5.5 CM_{1P} is formed by M9/M11 and CM_{1N} is formed by M10/M12. CF_{1P} by M9/M13/M15/M17 and CF_{1N} by M10/M14/M16/M18.

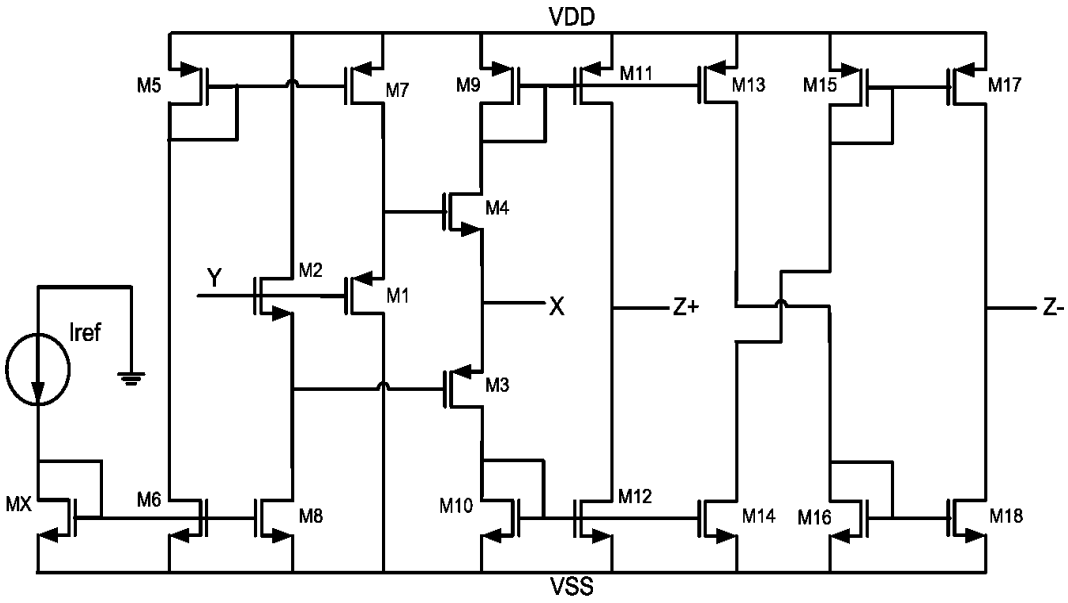


Figure 5.5: DOCCII-VFB-S

Again, combining the three VFs with both CMs and CFs (simple and low voltage), is possible to obtain six DOCCIIs, which are shown in Appendix B in transistor level. As the DOCCIs, the channel length (L) is equal to $1\mu m$. The channel width (W) of all DOCCIIs transistors are shown in table 5.8. The electrical parameter measurements of these CCCs are shown from table 5.9 to 5.14

Table 5.8: DOCCII channel width (W) dimensions.

DOCCII							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	192.35	21.35	50
	M3	192.35	48	50	192.35	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15	192.35	48	7	192.35	192.35	4
	M21,25,29	—	—	—	192.35	192.35	6
	M19,23,27,31	—	—	—	192.35	192.35	4
NMOS	M2	100	6.25	30	100	6.25	40
	M4	100	2.25	30	100	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16	100	11.11	1.5	100	100	1
	M22,26,30	—	—	—	100	100	3
	M20,24,28,32	—	—	—	100	100	1
	My	—	—	—	100	100	10

Table 5.9: DOCCII-VFA-S electrical parameter measurements

DOCCII-VFA-S				
Term. Resistance	$R_y = 122.6K\Omega$	$R_x = 510.44\Omega$	$R_{z+} = 240.13K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.3	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	131.32	-728.57
	$\mathbf{I_{T.C.}}$ (mA)	—	± 12	± 8
$\mathbf{AC_v}$	**Gain** (V/V)	0.993	—	—
	$\mathbf{BW_v}$ (MHz)	90.7	—	—
	Onoise $(V/(Hz)^{1/2})$	$708.92n$	—	—
	Inoise $(V/(Hz)^{1/2})$	$731.76n$	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.028	-1.082
	$\mathbf{BW_i}$ (MHz)	—	59.7	47
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	50.1	—	—
	ST $(nseg)$	18	—	—
	THD (%)	1.48	—	—
	SNR (dB)	-80.3	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	11284	-9515
	ST $(nseg)$	—	15	18.6
	THD $(m\%)$	—	46.24	79.24
	SNR (dB)	—	-50.9	-44.1

Table 5.10: DOCCII-VFB-S electrical parameter measurements

DOCCII-VFB-S				
Term. Resistance	$R_y = \infty$	$R_x = 2.13K\Omega$	$R_{z+} = 472.59K\Omega$	$R_{z-} = 457.06K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.72	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	393.97	-576.61
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.75	± 0.75
$\mathbf{AC_v}$	**Gain** (V/V)	0.978	—	—
	$\mathbf{BW_v}$ (MHz)	67.2	—	—
	Onoise $(V/(Hz)^{1/2})$	5.77μ	—	—
	Inoise $(V/(Hz)^{1/2})$	5.9μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.015	-1.047
	$\mathbf{BW_i}$ (MHz)	—	141	97.4
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	37.98	—	—
	ST $(nseg)$	20	—	—
	THD (%)	1.33	—	—
	SNR (**dB**)	-96.0	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	14277	-12384
	ST $(nseg)$	—	12.2	29
	THD $(m\%)$	—	191.18	430.95
	SNR (dB)	—	-57.4	-60.0

Table 5.11: DOCCII-VFC-S electrical parameter measurements

DOCCII-VFC-S				
Term. Resistance	$R_y = \infty$	$R_x = 2.88K\Omega$	$R_{z+} = 704.38K\Omega$	$R_{z-} = 697.95K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-877	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 500	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	612.13	-658.42
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.990	—	—
	$\mathbf{BW_v}$ (MHz)	39.4	—	—
	Onoise $(V/(Hz)^{1/2})$	3.02μ	—	—
	Inoise $(V/(Hz)^{1/2})$	3.95μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	0.997	-1.004
	$\mathbf{BW_i}$ (MHz)	—	82.9	79
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	31.23	—	—
	ST $(nseg)$	33.4	—	—
	THD (%)	1.24	—	—
	SNR (dB)	-90.7	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	10340	-9196
	ST $(nseg)$	—	82.8	63.5
	THD $(m\%)$	—	679.18	762.72
	SNR (dB)	—	-57.5	-56.7

Table 5.12: DOCCII-VFA-LV electrical parameter measurements

DOCCII-VFA-LV				
Term. Resistance	$R_y = 1.22M\Omega$	$R_x = 599.10\Omega$	$R_{z+} = 11.6M\Omega$	$R_{z-} = 11.59M\Omega$
Vref	± 0.5			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	44.7	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	56.46	-55.4
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.3	± 0.3
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—
	$\mathbf{BW_v}$ (MHz)	90.4	—	—
	Onoise $(V/(Hz)^{1/2})$	1.053μ	—	—
	Inoise $(V/(Hz)^{1/2})$	1.056μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0025	-1.007
	$\mathbf{BW_i}$ (MHz)	—	66.2	67
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	52.77	—	—
	ST $(nseg)$	26.4	—	—
	THD (%)	2.06	—	—
	SNR (dB)	-78.7	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	10064	-9296
	ST $(nseg)$	—	18.4	22
	THD $(m\%)$	—	130.41	151.4
	SNR (dB)	—	-73.5	-73.2

Table 5.13: DOCCII-VFB-LV electrical parameter measurements

DOCCII-VFB-LV				
Term. Resistance	$R_y = \infty$	$R_x = 841.02\Omega$	$R_{z+} = 12M\Omega$	$R_{z-} = 11.98M\Omega$
Vref	± 0.4			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}(\mu V)$	771.43	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.5	± 0.4
$\mathbf{AC_v}$	**Gain** (V/V)	0.989	—	—
	$\mathbf{BW_v}$ (MHz)	87.3	—	—
	Onoise $(V/(Hz)^{1/2})$	4.67μ	—	—
	Inoise $(V/(Hz)^{1/2})$	4.72μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0007	-1.0031
	$\mathbf{BW_i}$ (MHz)	—	105	97.4
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	56.43	—	—
	ST $(nseg)$	29.4	—	—
	THD (%)	0.89	—	—
	SNR (dB)	-78.5	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	14132	-11135
	ST $(nseg)$	—	10.4	17.7
	THD $(m\%)$	—	47.5	105.76
	SNR (dB)	—	-75.0	-72.9

Table 5.14: DOCCII-VFC-LV electrical parameter measurements

DOCCII-VFC-LV				
Term. Resistance	$R_y = \infty$	$R_x = 2.74K\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Vref	± 0.4			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-223.4	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 500	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	13.53	-10.07
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—
	$\mathbf{BW_v}$ (MHz)	38.1	—	—
	Onoise $(V/(Hz)^{1/2})$	2.51μ	—	—
	Inoise $(V/(Hz)^{1/2})$	2.52μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0002	-1.0012
	$\mathbf{BW_i}$ (MHz)	—	69.8	69
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	26.92	—	—
	ST $(nseg)$	39.2	—	—
	THD (%)	0.651	—	—
	SNR (dB)	-87.5	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	6689	-6501
	ST $(nseg)$	—	96.8	92.7
	THD (%)	—	0.902	1.06
	SNR (dB)	—	-56.1	-55.2

5.1.3 Direct Third Generation Current Conveyor (CCIII)

As it was seen in Chapter 2, where the behavior and structure of the CCIII was described by Eq. (2.5) and Fig. 2.10 respectively, in order to implement a CCIII is necessary to join a VF with a CM and a CF (CCIII+) or a VF with two CFs (CCIII-). A DOCCIII block structure is shown in Fig. 5.6, which is based in the VF-C.

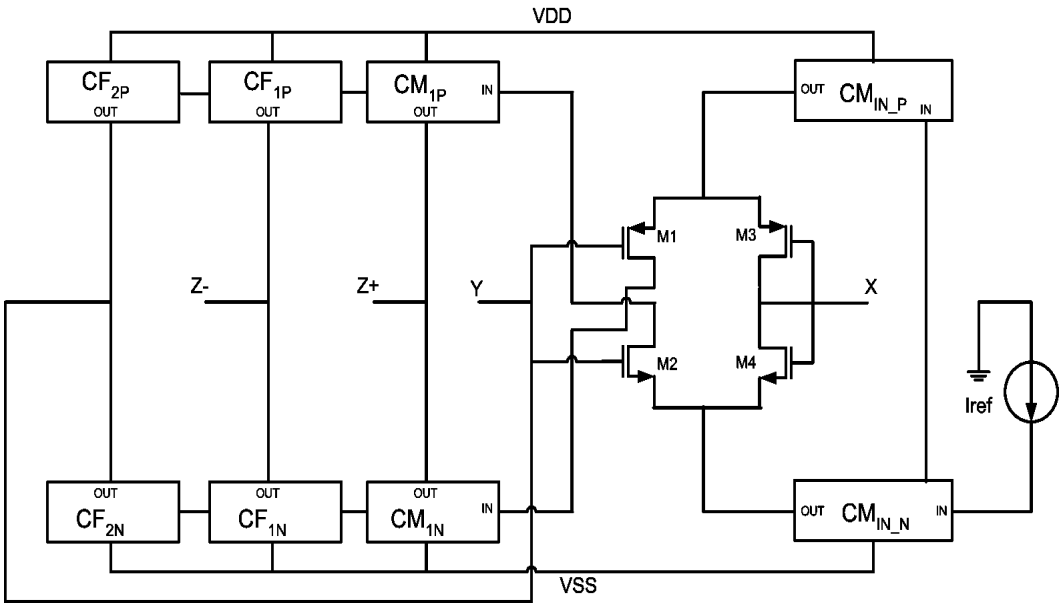


Figure 5.6: DOCCIII structure.

From Fig. 5.6, CM_{1P} and CM_{1N} are the first Current Mirror for $i_{z+} = i_x$. CF_{1P} and CF_{1N} are the first Current Follower for $i_{z-} = -i_x$. Finally CF_{2P} and CF_{2N} are the second Current Follower for $i_y = -ix$.

In Fig. 5.7 is shown a DOCCIII-VFC-SCM, where CM_{1P} and CM_{1N} are formed by M9/M11 and M10/M12. CF_{1P} and CF_{1N} are formed by M9/M13/M15/M17 and M10/M14/M16/M18. Finally CF_{2P} and CF_{2N} are formed by M9/M13M15/M19 and M10/M14/M16/M20.

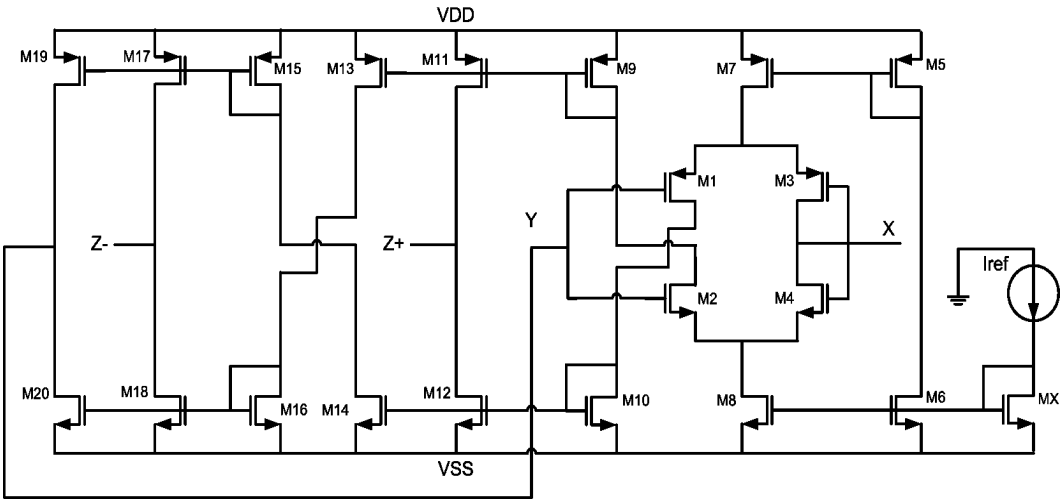


Figure 5.7: DOCCIII-VFC-S

The six DOCCIIIs obtained are shown in transistor level in Appendix B. The channel Length (L) for all transistors is $1\mu m$. The channel width of all transistors is shown in table 5.15. The electrical measurements made for these six DOCCIs are shown from table 5.16 to 5.21.

Table 5.15: DOCCIII channel width (W) dimensions.

DOCCIII							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	192.35	21.35	50
	M3	192.35	48	50	192.35	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15,19	192.35	48	7	192.35	192.35	4
	M21,25,29,33	—	—	—	192.35	192.35	6
	M23,27,31,35	—	—	—	192.35	192.35	4
NMOS	M2	100	6.25	30	100	6.25	40
	M4	100	2.25	30	100	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16,20	100	11.11	1.5	100	100	1
	M22,26,30,34	—	—	—	100	100	3
	M24,28,32,36	—	—	—	100	100	1
	My	—	—	—	100	100	10

Table 5.16: DOCCIII-VFA-S electrical parameter measurements

DOCCIII-VFA-S					
Term. Resistance		$R_y = 79.58K\Omega$	$R_x = 510.44\Omega$	$R_{z+} = 240.13K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.29	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	1.78	0.131	-0.728
	$\mathbf{I_{T.C.}}$ (mA)	—	± 8	± 12	± 8
$\mathbf{AC_v}$	**Gain** (V/V)	0.993	—	—	—
	$\mathbf{BW_v}$ (MHz)	90.8	—	—	—
	Onoise $(V/(Hz)^{1/2})$	$708.92n$	—	—	—
	Inoise $(V/(Hz)^{1/2})$	$713.76n$	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.0821	1.0286	-1.0821
	$\mathbf{BW_i}$ (MHz)	—	36.4	60	42
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	50.14	—	—	—
	ST $(nseg)$	17.3	—	—	—
	THD (%)	1.48	—	—	—
	SNR (dB)	-80.3	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-7245	11290	-8542
	ST $(nseg)$	—	22.7	15.2	19.7
	THD $(m\%)$	—	62.2	82.84	78.09
	SNR (dB)	—	-32.5	-46.2	-51

Table 5.17: DOCCIII-VFB-S electrical parameter measurements

DOCCIII-VFB-S					
Term. Resistance		$R_y = 464K\Omega$	$R_x = 2.13K\Omega$	$R_{z+} = 472.59K\Omega$	$R_{z-} = 457.09K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	1.72	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	0.576	0.393	-0.576
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.75	± 0.75	± 0.75
$\mathbf{AC_v}$	**Gain** (V/V)	0.978	—	—	—
	$\mathbf{BW_v}$ (MHz)	67.2	—	—	—
	Onoise $(V/(Hz)^{1/2})$	5.77μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	5.9μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.048	1.015	-1.047
	$\mathbf{BW_i}$ (MHz)	—	81.5	141	82.6
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	37.98	—	—	—
	ST $(nseg)$	20.3	—	—	—
	THD (%)	1.33	—	—	—
	SNR (dB)	-96.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-16025	14283	-12100
	ST $(nseg)$	—	20.3	11.1	26.3
	THD $(m\%)$	—	439.4	197.3	439.95
	SNR (dB)	—	-55.6	-57.5	-77.6

Table 5.18: DOCCIII-VFC-S electrical parameter measurements

DOCCIII-VFC-S					
Term. Resistance		$R_y = 155.89K\Omega$	$R_x = 2.88K\Omega$	$R_{z+} = 704.38K\Omega$	$R_{z-} = 697.95K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (mV)	-0.877	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 500	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (μA)	—	-0.658	0.612	-0.658
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.990	—	—	—
	$\mathbf{BW_v}$ (MHz)	39.4	—	—	—
	Onoise $(V/(Hz)^{1/2})$	3.02μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	3.05μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.0048	0.997	-1.0048
	$\mathbf{BW_i}$ (MHz)	—	66.4	83	76.7
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	31.23	—	—	—
	ST $(nseg)$	34.6	—	—	—
	THD (%)	1.24	—	—	—
	SNR (dB)	-91.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-11071	10337	-9322
	ST $(nseg)$	—	80	69.5	68.8
	THD $(m\%)$	—	748.2	678.9	779.8
	SNR (dB)	—	-56.8	-57.5	-56.6

Table 5.19: DOCCIII-VFA-LV electrical parameter measurements

DOCCIII-VFA-LV					
Term. Resistance		$R_y = 1.10M\Omega$	$R_x = 599.1\Omega$	$R_{z+} = 11.61M\Omega$	$R_{z-} = 11.6M\Omega$
Vref		$\pm 0.5V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	44.7	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-60.66	56.46	-55.44
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.3	± 0.3	± 0.3
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—	—
	$\mathbf{BW_v}$ (MHz)	90.3	—	—	—
	Onoise $(V/(Hz)^{1/2})$	1.053μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	1.056μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.007	1.002	-1.007
	$\mathbf{BW_i}$ (MHz)	—	48.5	66.1	56.9
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	52.6	—	—	—
	ST $(nseg)$	25.3	—	—	—
	THD (%)	2.06	—	—	—
	SNR (dB)	-78.9	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-8572	9753	-7771
	ST $(nseg)$	—	20	26.8	30
	THD $(m\%)$	—	182.7	132.9	159.9
	SNR (dB)	—	-32.6	-75.5	-72.1

Table 5.20: DOCCIII-VFB-LV electrical parameter measurements

DOCCIII-VFB-LV					
Term. Resistance		$R_y = 12.82M\Omega$	$R_x = 841.02\Omega$	$R_{z+} = 12M\Omega$	$R_{z-} = 11.98M\Omega$
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	771.43	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-47.92	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.45	± 0.5	± 0.45
$\mathbf{AC_v}$	**Gain** (V/V)	0.989	—	—	—
	$\mathbf{BW_v}$ (MHz)	87.3	—	—	—
	Onoise $(V/(Hz)^{1/2})$	4.67μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	4.72μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.003	1.0007	-1.003
	$\mathbf{BW_i}$ (MHz)	—	80.1	105	80.2
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	56.43	—	—	—
	ST $(nseg)$	28.7	—	—	—
	THD $(m\%)$	890.35	—	—	—
	SNR (**dB**)	-78.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-11996	14132	-10300
	ST $(nseg)$	—	20.7	10.9	19.2
	THD $(m\%)$	—	121.68	52.58	121.16
	SNR (dB)	—	-73.2	-74.5	-73.1

Table 5.21: DOCCIII-VFC-LV electrical parameter measurements

DOCCIII-VFC-LV					
Term. Resistance		$R_y = 5.01M\Omega$	$R_x = 2.74K\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-223.4	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 500	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-10.07	13.53	-10.07
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	0.996	—	—	—
	$\mathbf{BW_v}$ (MHz)	38.1	—	—	—
	Onoise $(V/(Hz)^{1/2})$	2.51μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	2.52μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.0012	1.0002	-1.0012
	$\mathbf{BW_i}$ (MHz)	—	57.5	69.8	67.7
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	26.92	—	—	—
	ST $(nseg)$	39.3	—	—	—
	THD $(m\%)$	650.95	—	—	—
	SNR (dB)	-88.3	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-8951	6689	-6679
	ST $(nseg)$	—	61.4	78.4	81.3
	THD $(\%)$	—	1.052	0.903	1.08
	SNR (dB)	—	-55.3	-56.0	-55.1

5.2 Inverse Current Conveyors (ICCs)

The ICCs are not so popular as the direct CCs. The Inverse Second Generation CC (ICCII) has been reported by [49] as a new block to the current conveyor family to obtain and design current-mode circuits from their voltage-mode counterparts [50]. In [51] is shown a universal topology which can form all types of CC, based in differential pairs. At this moment only the ICCII has been used for filtering, oscillators and floated inductance simulator applications in [50, 52, 53, 54]. So, the ICCI and ICCIII topologies, based in UGCs, are contributions of this thesis.

5.2.1 Inverse First Generation Current Conveyor (ICCI)

As it was seen, the behavior and structure of the CCI was described in Chapter 2 by Eq. (2.2) and Fig. 2.3, respectively. A ICCI is formed by a VM connected with two CMs (ICCI+) or with a CM and a CF (ICCI-). As with Direct CCs, we will show Dual-output ICCs, because is include both positive and negative types. In Fig. 5.8 is shown the block structure of the DOICCI, where, CM_{1P} and CM_{1N} are the first Current Mirror for $i_y = ix$. CM_{2P} and CM_{2N} are the second Current Mirror for $i_z = ix$. Finally CF_{1P} and CF_{1N} are the first Current Follower for $i_z = -ix$.

For a complete transistor level, in Fig. 5.9 is shown a DOICCI based in the VMA, SCM and SCF, where CM_{1P} and CM_{1N} is formed by M9/M11 and M10/M12, respectively. CM_{2P} and CM_{2N} is formed by M9/M13 and M10/M14, respectively. Finally CF_{1P} and CF_{1N} is formed by M9/M15/M17/M19 and M10/M16/M18/M20, respectively.

The six different DOICCIs, obtained from the three VMs with the Simple and Low Voltage CMs and CF, are shown in transistor level in Appendix B. The channel Length (L) for all transistors is again $1\mu m$. The channel width of all transistors and the electrical measurements are shown in table 5.22 and from 5.23 to 5.28 respectively.

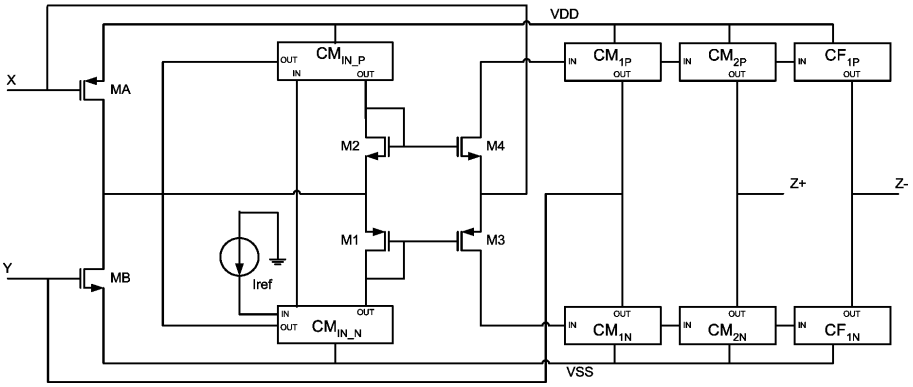


Figure 5.8: DOICCI structure.

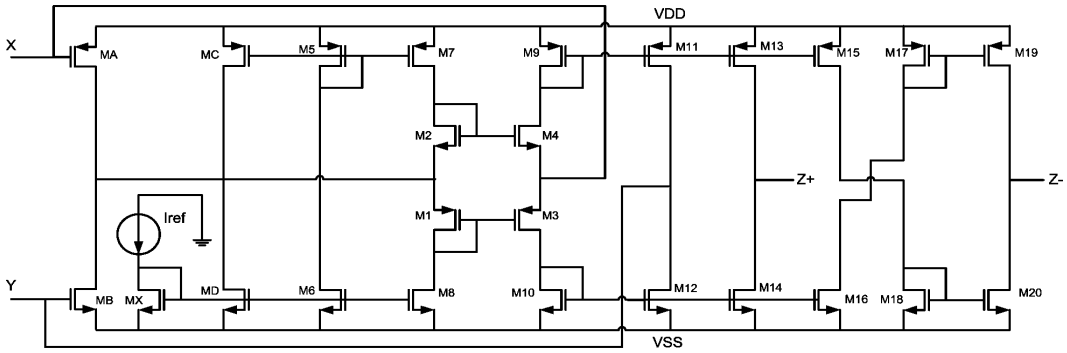


Figure 5.9: DOICCI-VMA-S

Table 5.22: DOICCI channel width (W) dimensions.

DOICCI							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	150	21.35	50
	M3	192.35	48	50	150	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15,19	192.35	48	7	192.35	192.35	4
	M21,25,29,33	—	—	—	192.35	192.35	6
	M23,27,31,35	—	—	—	192.35	192.35	4
	MA	9	9	9	9	9	9
	MC	192.35	23.75	28.75	192.35	192.35	100
	ME	—	—	—	206	206	148.35
NMOS	M2	100	6.25	30	50	6.25	40
	M4	100	2.25	30	50	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16,20	100	11.11	1.5	100	100	1
	M22,26,30,34	—	—	—	100	100	3
	M24,28,32,36	—	—	—	100	100	1
	My	—	—	—	100	100	10
	MB	3	3	3	3	3	3
	MD	41.7	11.35	4.35	100	100	20
	MF	—	—	—	35.35	35.35	2.75

Table 5.23: DOICCI-VMA-S electrical parameter measurements

DOICCI-VMA-S					
Term. Resistance		$R_y = 239.8K\Omega$	$R_x = 34.41\Omega$	$R_{z+} = 240.14K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-75.68	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	131.31	131.31	-728.54
	$\mathbf{I_{T.C.}}$ (mA)	—	± 8	± 8	± 6
$\mathbf{AC_v}$	**Gain** (V/V)	-0.957	—	—	—
	$\mathbf{BW_v}$ (MHz)	17.7	—	—	—
	Onoise $(V/(Hz)^{1/2})$	12.93μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.5μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.028	1.028	-1.082
	$\mathbf{BW_i}$ (MHz)	—	50.4	50.4	41.9
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-22.62	—	—	—
	ST $(nseg)$	30.6	—	—	—
	THD (%)	3.75	—	—	—
	SNR (dB)	-78.0	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	9154.2	9156.9	-8354.1
	ST $(nseg)$	—	15	15	21.1
	THD $(m\%)$	—	84.82	48.19	98.5
	SNR (dB)	—	-35.2	-39.4	-42.3

Table 5.24: DOICCI-VMB-S electrical parameter measurements

DOICCI-VMB-S					
Term. Resistance		$R_y = 478.02K\Omega$	$R_x = 83.25\Omega$	$R_{z+} = 472.53K\Omega$	$R_{z-} = 457.00K\Omega$
Cc		$1pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-752.96	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	394.03	394.03	-576.69
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.90	± 0.90	± 0.90
$\mathbf{AC_v}$	**Gain** (V/V)	-0.986	—	—	—
	$\mathbf{BW_v}$ (MHz)	57.7	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.26μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.45μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.015	1.015	-1.047
	$\mathbf{BW_i}$ (MHz)	—	121	121	90.0
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-74.02	—	—	—
	ST $(nseg)$	32.4	—	—	—
	THD (%)	4.49	—	—	—
	SNR (dB)	-104	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	13569	13590	-11872
	ST $(nseg)$	—	11.7	11.7	25.6
	THD $(m\%)$	—	213.48	213.56	453.1
	SNR (dB)	—	-63.9	-61.1	-60.3

Table 5.25: DOICCI-VMC-S electrical parameter measurements

DOICCI-VMC-S					
Term. Resistance		$R_y = 157.68K\Omega$	$R_x = 116.61\Omega$	$R_{z+} = 704.36K\Omega$	$R_{z-} = 697.97K\Omega$
Cc		$2pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-184.42	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	615.69	615.69	-661.91
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.985	—	—	—
	$\mathbf{BW_v}$ (MHz)	27.1	—	—	—
	Onoise $(V/(Hz)^{1/2})$	14.66μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	14.88μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.011	1.011	-1.018
	$\mathbf{BW_i}$ (MHz)	—	81.5	81.5	87.1
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-30.15	—	—	—
	ST $(nseg)$	52.7	—	—	—
	THD (%)	4.48	—	—	—
	SNR (dB)	-104	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	11710	11724	-10622
	ST $(nseg)$	—	76.5	80.5	76.3
	THD (%)	—	1.19	1.19	1.26
	SNR (dB)	—	-47.8	-47.8	-48.0

Table 5.26: DOICCI-VMA-LV electrical parameter measurements

DOICCI-VMA-LV					
Term. Resistance		$R_y = 11.08M\Omega$	$R_x = 18.61\Omega$	$R_{z+} = 11.60M\Omega$	$R_{z-} = 11.59M\Omega$
Vref		$\pm 0.5V$			
Analysis ($Vref = \pm 0.5V$)		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	442.16	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 300	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	56.46	56.46	-55.40
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.3	± 0.3	± 0.3
$\mathbf{AC_v}$	**Gain** (V/V)	-0.994	—	—	—
	$\mathbf{BW_v}$ (MHz)	19.8	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.37μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.44μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.002	1.002	-1.007
	$\mathbf{BW_i}$ (MHz)	—	54.3	54.3	57.9
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-15.75	—	—	—
	ST $(nseg)$	43	—	—	—
	THD (%)	3.2	—	—	—
	SNR (dB)	-75.2	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	8396.4	8407.2	-7989.7
	ST $(nseg)$	—	12.5	12.5	21.3
	THD $(m\%)$	—	137.86	129.95	153.62
	SNR (dB)	—	-75.0	-76.3	-73.6

Table 5.27: DOICCI-VMB-LV electrical parameter measurements

DOICCI-VMB-LV					
Term. Resistance		$R_y = 12.85M\Omega$	$R_x = 23.57\Omega$	$R_{z+} = 11.99M\Omega$	$R_{z-} = 11.98M\Omega$
Cc		$1pF$			
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-190.75	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	43.75	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.5	± 0.5	± 0.5
$\mathbf{AC_v}$	**Gain** (V/V)	-0.997	—	—	—
	$\mathbf{BW_v}$ (MHz)	45.7	—	—	—
	Onoise $(V/(Hz)^{1/2})$	12.4μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	12.4μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0007	1.0007	-1.003
	$\mathbf{BW_i}$ (MHz)	—	88.4	88.4	85.7
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-40.25	—	—	—
	ST $(nseg)$	54.3	—	—	—
	THD (%)	5.01	—	—	—
	SNR (dB)	-84.3	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	11129	11128	-10021
	ST $(nseg)$	—	22.3	22.5	19.4
	THD $(m\%)$	—	81.69	80.63	128.67
	SNR (dB)	—	-60.5	-73.6	-71.7

Table 5.28: DOICCI-VMC-LV electrical parameter measurements

DOICCI-VMC-LV					
Term. Resistance		$R_y = 5.01M\Omega$	$R_x = 76.6\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Cc		$2pF$			
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-169.68	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	13.53	13.54	-10.06
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.998	—	—	—
	$\mathbf{BW_v}$ (MHz)	25.4	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.22μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.22μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0007	1.0007	-1.0016
	$\mathbf{BW_i}$ (MHz)	—	71.0	71.0	70.6
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-28.73	—	—	—
	ST $(nseg)$	54	—	—	—
	THD (%)	5.03	—	—	—
	SNR (dB)	-82.9	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	7712.7	7701.8	-7458
	ST $(nseg)$	—	128	132.5	127.7
	THD $(m\%)$	—	413.13	410.75	461.43
	SNR (dB)	—	-55.8	-55.5	-55.0

5.2.2 Inverse Second Generation Current Conveyor (ICCII)

This type of ICCs are formed by a VM and a CM or a CF in order to form an ICCII+ or an ICCII-, respectively. Its behavior and structure was already described by Eq. (2.4) and Fig. 2.7. In Fig. 5.10 is shown a DOICCII block diagram, where CM_{1P} is formed by M9/M11 and CM_{1N} is formed by M10/M12; CM_{2P} by M9/M13/M15/M17 and CM_{2N} by M10/M14/M16/M18 in Fig. 5.11.

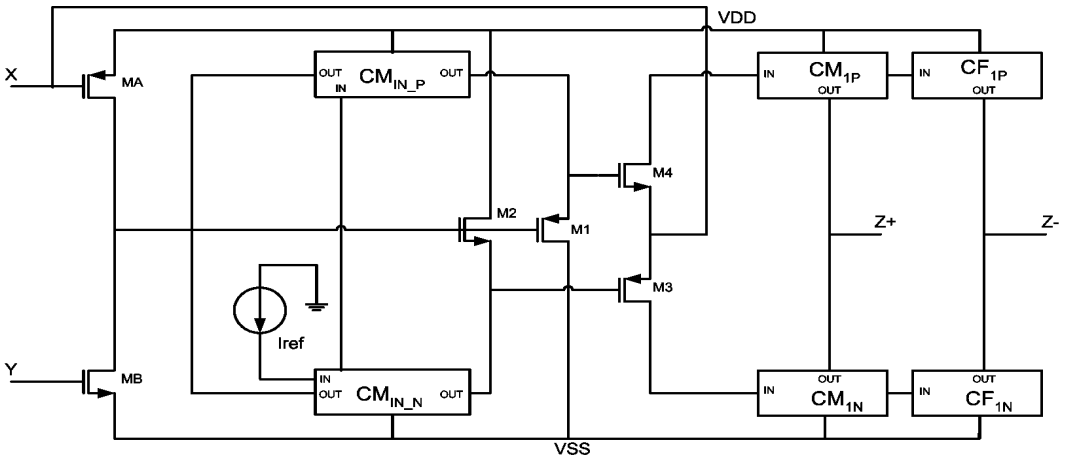


Figure 5.10: DOICCII structure.

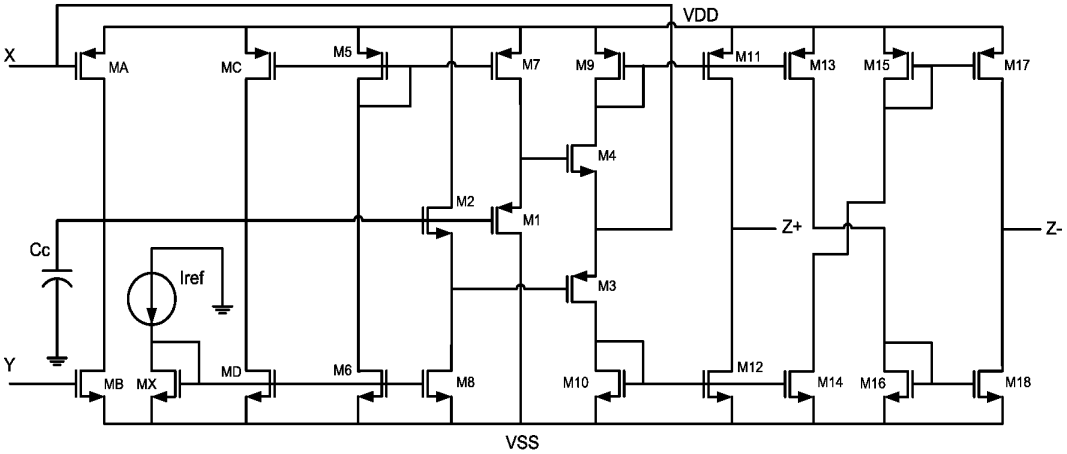


Figure 5.11: DOICCII-VMB-S

The six DOICCIIs are shown in Appendix B in transistor level. The channel width (W) of all DOICCIIs transistors are shown in table 5.29, where again the

channel length (L) for all transistors is equal to $1\mu m$. The electrical parameter measurements of these ICCIIs are shown from table 5.30 to 5.35

Table 5.29: DOICCII channel width (W) dimensions.

DOICCII							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	192.35	21.35	50
	M3	192.35	48	50	192.35	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15	192.35	48	7	192.35	192.35	4
	M21,25,29	—	—	—	192.35	192.35	6
	M19,23,27,31	—	—	—	192.35	192.35	4
	MA	9	9	9	9	9	9
	MC	192.35	23.75	28.75	192.35	192.35	100
	ME	—	—	—	206	206	148.35
NMOS	M2	100	6.25	30	100	6.25	40
	M4	100	2.25	30	100	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16	100	11.11	1.5	100	100	1
	M22,26,30	—	—	—	100	100	3
	M20,24,28,32	—	—	—	100	100	1
	My	—	—	—	100	100	10
	MB	3	3	3	3	3	3
	MD	41.7	11.35	4.35	100	100	20
	MF	—	—	—	35.35	35.35	2.75

Table 5.30: DOICCII-VMA-S electrical parameter measurements

DOICCII-VMA-S				
Term. Resistance	$R_y = \infty$	$R_x = 31.41\Omega$	$R_{z+} = 240.14K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-75.68	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	131.31	-728.57
	$\mathbf{I_{T.C.}}$ (mA)	—	± 8	± 6
$\mathbf{AC_v}$	**Gain** (V/V)	-0.957	—	—
	$\mathbf{BW_v}$ (MHz)	17.7	—	—
	Onoise $(V/(Hz)^{1/2})$	12.93μ	—	—
	Inoise $(V/(Hz)^{1/2})$	13.50μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.028	-1.082
	$\mathbf{BW_i}$ (MHz)	—	60.8	48.1
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-22.63	—	—
	ST $(nseg)$	30.1	—	—
	THD (%)	3.75	—	—
	SNR (dB)	-79.3	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	9986.3	-9472.5
	ST $(nseg)$	—	13.6	23
	THD $(m\%)$	—	81.96	95.03
	SNR (dB)	—	-36.6	-43.0

Table 5.31: DOICCII-VMB-S electrical parameter measurements

DOICCII-VMB-S				
Term. Resistance	$R_y = \infty$	$R_x = 83.25\Omega$	$R_{z+} = 472.53K\Omega$	$R_{z-} = 457.00K\Omega$
Cc	$1pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-752.96	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	394.03	-576.69
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.85	± 0.85
$\mathbf{AC_v}$	**Gain** (V/V)	-0.986	—	—
	$\mathbf{BW_v}$ (MHz)	59.5	—	—
	Onoise $(V/(Hz)^{1/2})$	13.26μ	—	—
	Inoise $(V/(Hz)^{1/2})$	13.45μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.015	-1.047
	$\mathbf{BW_i}$ (MHz)	—	137	98.4
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-74.36	—	—
	ST $(nseg)$	41.6	—	—
	THD (%)	4.49	—	—
	SNR (dB)	-103	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	14276	-12615
	ST $(nseg)$	—	10.4	24.5
	THD $(m\%)$	—	203.79	440.89
	SNR (dB)	—	-57.6	-68.1

Table 5.32: DOICCII-VMC-S electrical parameter measurements

DOICCII-VMC-S				
Term. Resistance	$R_y = \infty$	$R_x = 116.61\Omega$	$R_{z+} = 704.36K\Omega$	$R_{z-} = 697.97K\Omega$
Cc	$2pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-182.42	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	612.59	-661.91
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.985	—	—
	$\mathbf{BW_v}$ (MHz)	27.1	—	—
	Onoise $(V/(Hz)^{1/2})$	14.66μ	—	—
	Inoise $(V/(Hz)^{1/2})$	14.88μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.011	-1.018
	$\mathbf{BW_i}$ (MHz)	—	84.6	81.6
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-30.16	—	—
	ST $(nseg)$	52.8	—	—
	THD (%)	4.48	—	—
	SNR (dB)	-100	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	11747	-10493
	ST $(nseg)$	—	76.5	77.4
	THD (%)	—	1.20	1.27
	SNR (dB)	—	-47.7	-47.9

Table 5.33: DOICCII-VMA-LV electrical parameter measurements

DOICCII-VMA-LV				
Term. Resistance	$R_y = \infty$	$R_x = 18.61\Omega$	$R_{z+} = 11.60M\Omega$	$R_{z-} = 11.59M\Omega$
Vref	± 0.5			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-442.16	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	56.46	-55.40
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.3	± 0.3
$\mathbf{AC_v}$	**Gain** (V/V)	-0.994	—	—
	$\mathbf{BW_v}$ (MHz)	19.8	—	—
	Onoise $(V/(Hz)^{1/2})$	13.37μ	—	—
	Inoise $(V/(Hz)^{1/2})$	13.44μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.002	-1.007
	$\mathbf{BW_i}$ (MHz)	—	66.6	67.0
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-18.54	—	—
	ST $(nseg)$	34.7	—	—
	THD (%)	4.20	—	—
	SNR (dB)	-65.4	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	10594	-9305
	ST $(nseg)$	—	16.4	30.8
	THD $(m\%)$	—	124.63	145.45
	SNR (dB)	—	-76.0	-74.2

Table 5.34: DOICCII-VMB-LV electrical parameter measurements

DOICCII-VMB-LV				
Term. Resistance	$R_y = \infty$	$R_x = 23.57\Omega$	$R_{z+} = 121.99M\Omega$	$R_{z-} = 11.98M\Omega$
Cc	$1pF$			
Vref	± 0.4			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-160.95	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.5	± 0.4
$\mathbf{AC_v}$	**Gain** (V/V)	-0.997	—	—
	$\mathbf{BW_v}$ (MHz)	45.8	—	—
	Onoise $(V/(Hz)^{1/2})$	12.40μ	—	—
	Inoise $(V/(Hz)^{1/2})$	12.43μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0007	-1.0031
	$\mathbf{BW_i}$ (MHz)	—	104	95.6
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-40.39	—	—
	ST $(nseg)$	52.5	—	—
	THD (%)	5.01	—	—
	SNR (dB)	-82.9	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	12159	-11142
	ST $(nseg)$	—	20.6	18.6
	THD $(m\%)$	—	62.14	115.33
	SNR (dB)	—	-74.4	-74.3

Table 5.35: DOICCII-VMC-LV electrical parameter measurements

DOICCII-VMC-LV				
Term. Resistance	$R_y = \infty$	$R_x = 76.60\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Cc	$2pF$			
Vref	± 0.4			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-169.68	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	13.53	-10.07
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.998	—	—
	$\mathbf{BW_v}$ (MHz)	25.4	—	—
	Onoise $(V/(Hz)^{1/2})$	13.22μ	—	—
	Inoise $(V/(Hz)^{1/2})$	13.25μ	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	1.0007	-1.0016
	$\mathbf{BW_i}$ (MHz)	—	72.0	71.3
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-28.73	—	—
	ST $(nseg)$	54.1	—	—
	THD (%)	5.03	—	—
	SNR (dB)	-82.7	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	7697.8	-7426
	ST $(nseg)$	—	142	136
	THD $(m\%)$	—	415.43	455.92
	SNR (dB)	—	-55.7	-55.1

5.2.3 Inverse Third Generation Current Conveyor (ICCIII)

In this section are described the electrical parameters of the less common CC. Again, it was described by Eq. (2.6) and Fig. 2.11, where these kind of CCs are formed by a VM with a CM and a CF (ICCIII+) or with two CFs (ICCIII-). The block structure of a DOICCIII is shown in Fig. 5.12. On Fig. 5.13 CM_{1P} and CM_{1N} are formed by M9/M11 and M10/M12. CF_{1P} and CF_{1N} are formed by M9/M13/M15/M17 and M10/M14/M16/M18. Finally CF_{2P} and CF_{2N} are formed by M9/M13M15/M19 and M10/M14/M16/M20.

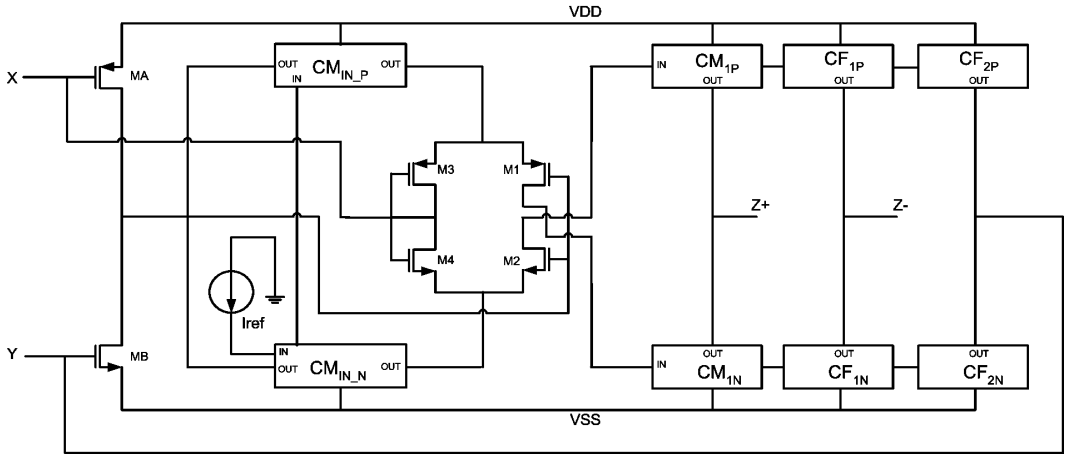


Figure 5.12: DOICCIII structure.

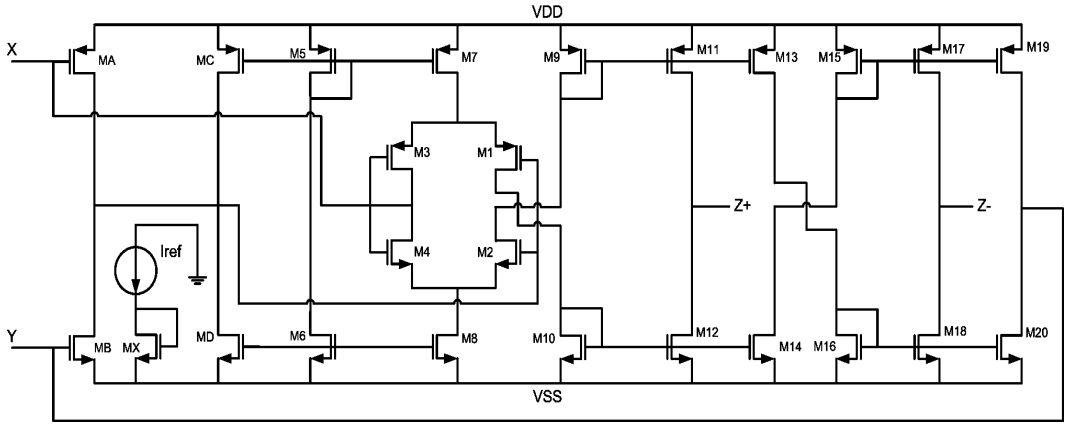


Figure 5.13: DOICCIII-VMC-S

The channel width of the six DOICCIIIs transistors is shown in table 5.36.

The electrical measurements shown from table 5.37 to 5.42. The channel width (W) for all transistors is equal to 1 μm.

Table 5.36: DOICCIII channel width (W) dimensions.

DOICCIII							
W (μm)		**VFA-S**	**VFB-S**	**VFC-S**	**VFA-LV**	**VFB-LV**	**VFC-LV**
PMOS	M1	192.35	21.35	50	192.35	21.35	50
	M3	192.35	48	50	192.35	120	50
	M5	192.35	21.35	21.35	192.35	192.35	100
	M7	192.35	21.35	21.35	192.35	192.35	150
	M9	192.35	48	7	192.35	192.35	100
	M11	192.35	48	7	192.35	192.35	150
	M13,17	192.35	48	7	192.35	192.35	6
	M15,19	192.35	48	7	192.35	192.35	4
	M21,25,29,33	—	—	—	192.35	192.35	6
	M23,27,31,35	—	—	—	192.35	192.35	4
	MA	9	9	9	9	9	9
	MC	192.35	23.75	28.75	192.35	192.35	100
	ME	—	—	—	206	206	148.35
NMOS	M2	100	6.25	30	100	6.25	40
	M4	100	2.25	30	100	5.5	40
	M6,Mx	100	25	6.3	100	100	20
	M8	100	25	6.3	100	100	10
	M10	100	11.11	1.5	100	100	20
	M12	100	11.11	1.5	100	100	10
	M14,18	100	11.11	1.5	100	100	3
	M16,20	100	11.11	1.5	100	100	1
	M22,26,30,34	—	—	—	100	100	3
	M24,28,32,36	—	—	—	100	100	1
	My	—	—	—	100	100	10
	MB	3	3	3	3	3	3
	MD	41.7	11.35	4.35	100	100	20
	MF	—	—	—	35.35	35.35	2.75

Table 5.37: DOICCIII-VMA-S electrical parameter measurements

DOICCIII-VMA-S					
Term. Resistance		$R_y = 228.49K\Omega$	$R_x = 34.41\Omega$	$R_{z+} = 240.14K\Omega$	$R_{z-} = 227.65K\Omega$
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-75.68	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-728.54	131.31	-728.54
	$\mathbf{I_{T.C.}}$ (mA)	—	± 6	± 8	± 6
$\mathbf{AC_v}$	**Gain** (V/V)	-0.957	—	—	—
	$\mathbf{BW_v}$ (MHz)	17.7	—	—	—
	Onoise $(V/(Hz)^{1/2})$	12.93μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.50μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.0821	1.0286	-1.0821
	$\mathbf{BW_i}$ (MHz)	—	43.1	60.9	43.1
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-22.63	—	—	—
	ST $(nseg)$	29.6	—	—	—
	THD (%)	3.75	—	—	—
	SNR (dB)	-78.3	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-8454.2	9991.1	-8458.2
	ST $(nseg)$	—	20	13.2	20.1
	THD $(m\%)$	—	97.45	61.81	97.4
	SNR (dB)	—	-42.2	-35.6	-42.2

Table 5.38: DOICCIII-VMB-S electrical parameter measurements

DOICCIII-VMB-S					
Term. Resistance		$R_y = 450.32K\Omega$	$R_x = 83.25\Omega$	$R_{z+} = 472.53K\Omega$	$R_{z-} = 457.00K\Omega$
Cc		$1pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	$\mathbf{V_{offset}}$ (μV)	-752.96	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-576.69	394.03	-576.69
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.80	± 0.85	± 0.80
$\mathbf{AC_v}$	**Gain** (V/V)	-0.986	—	—	—
	$\mathbf{BW_v}$ (MHz)	57.8	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.26μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.45μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.047	1.015	-1.047
	$\mathbf{BW_i}$ (MHz)	—	84.2	137	84.2
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-74.36	—	—	—
	ST $(nseg)$	39.7	—	—	—
	THD (%)	4.49	—	—	—
	SNR (dB)	-102	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-12272	14282	-12244
	ST $(nseg)$	—	34.9	10.9	35
	THD $(m\%)$	—	456.84	204.59	456.76
	SNR (dB)	—	-70.7	-65.7	-74.1

Table 5.39: DOICCIII-VMC-S electrical parameter measurements

DOICCIII-VMC-S					
Term. Resistance		$R_y = 283.49K\Omega$	$R_x = 116.61\Omega$	$R_{z+} = 704.36K\Omega$	$R_{z-} = 697.97K\Omega$
Cc		$2pF$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-184.42	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 430	—	—	—
$\mathbf{DC_i}$	**Ioffset** (nA)	—	-661.91	615.59	-661.91
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.985	—	—	—
	$\mathbf{BW_v}$ (MHz)	27.2	—	—	—
	Onoise $(V/(Hz)^{1/2})$	14.66μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	14.88μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.018	1.011	-1.018
	$\mathbf{BW_i}$ (MHz)	—	79.7	84.7	79.7
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-30.16	—	—	—
	ST $(nseg)$	52.5	—	—	—
	THD (%)	4.48	—	—	—
	SNR (dB)	-102	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-10557	11744	-10575
	ST $(nseg)$	—	78.9	77.8	78.3
	THD (%)	—	1.27	1.19	1.23
	SNR (dB)	—	-47.9	-47.8	-48.3

Table 5.40: DOICCIII-VMA-LV electrical parameter measurements

DOICCIII-VMA-LV					
Term. Resistance		$R_y = 12.14M\Omega$	$R_x = 18.61\Omega$	$R_{z+} = 11.61M\Omega$	$R_{z-} = 11.60M\Omega$
Vref		$\pm 0.5V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-493.34	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	**Ioffset** (nA)	—	-55.36	56.41	-55.36
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.3	± 0.3	± 0.3
$\mathbf{AC_v}$	**Gain** (V/V)	-0.994	—	—	—
	$\mathbf{BW_v}$ (MHz)	19.9	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.37μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.44μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.007	1.002	-1.007
	$\mathbf{BW_i}$ (MHz)	—	57.7	66.7	57.7
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-19.14	—	—	—
	ST $(nseg)$	35.5	—	—	—
	THD (%)	4.48	—	—	—
	SNR (dB)	-65.7	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-8722.4	10186	-8733.1
	ST $(nseg)$	—	22.5	17.4	22.4
	THD $(m\%)$	—	159.46	135.63	162.02
	SNR (dB)	—	-74.5	-76.4	-73.4

Table 5.41: DOICCIII-VMB-LV electrical parameter measurements

DOICCIII-VMB-LV					
Term. Resistance		$R_y = 11.25M\Omega$	$R_x = 23.57\Omega$	$R_{z+} = 11.99M\Omega$	$R_{z-} = 11.98M\Omega$
Cc		$1pF$			
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-190.65	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-47.92	43.75	-47.92
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.5	± 0.5	± 0.45
$\mathbf{AC_v}$	**Gain** (V/V)	-0.997	—	—	—
	$\mathbf{BW_v}$ (MHz)	45.8	—	—	—
	Onoise $(V/(Hz)^{1/2})$	12.40μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	12.43μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.003	1.0007	-1.003
	$\mathbf{BW_i}$ (MHz)	—	79.8	104	79.8
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-40.39	—	—	—
	ST $(nseg)$	54.4	—	—	—
	THD (%)	5.01	—	—	—
	SNR (dB)	-83.8	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-9528.4	12159	-9523.7
	ST $(nseg)$	—	25.4	18.4	25.3
	THD $(m\%)$	—	119.10	58.94	119.61
	SNR (dB)	—	-69.7	-75.1	-72.9

Table 5.42: DOICCIII-VMC-LV electrical parameter measurements

DOICCIII-VMC-LV					
Term. Resistance		$R_y = 8.63M\Omega$	$R_x = 76.60\Omega$	$R_{z+} = 23.93M\Omega$	$R_{z-} = 23.86M\Omega$
Cc		$2pF$			
Vref		$\pm 0.4V$			
Analysis		$\mathbf{V_{(x/y)}}$	$\mathbf{I_{(y/x)}}$	$\mathbf{I_{(z+/x)}}$	$\mathbf{I_{(z-/x)}}$
$\mathbf{DC_v}$	**Voffset** (μV)	-169.68	—	—	—
	$\mathbf{V_{T.C.}}$ (mV)	± 400	—	—	—
$\mathbf{DC_i}$	$\mathbf{I_{Offset}}$ (nA)	—	-10.07	13.53	-10.07
	$\mathbf{I_{T.C.}}$ (mA)	—	± 0.05	± 0.05	± 0.05
$\mathbf{AC_v}$	**Gain** (V/V)	-0.998	—	—	—
	$\mathbf{BW_v}$ (MHz)	25.4	—	—	—
	Onoise $(V/(Hz)^{1/2})$	13.22μ	—	—	—
	Inoise $(V/(Hz)^{1/2})$	13.25μ	—	—	—
$\mathbf{AC_i}$	**Gain** (A/A)	—	-1.0016	1.0007	-1.0016
	$\mathbf{BW_i}$ (MHz)	—	70.3	72.1	70.3
	Onoise $(V/(Hz)^{1/2})$	—	$7.030n$	$7.030n$	$7.030n$
	Inoise $(V/(Hz)^{1/2})$	—	$7.023n$	$7.037n$	$7.023n$
$\mathbf{Tran_v}$	**SR** $(V/\mu seg)$	-28.73	—	—	—
	ST $(nseg)$	54	—	—	—
	THD (%)	5.03	—	—	—
	SNR (dB)	-83.1	—	—	—
$\mathbf{Tran_i}$	**SR** (A/seg)	—	-7589.2	7697.7	-7580.1
	ST $(nseg)$	—	137.6	133	137.6
	THD $(m\%)$	—	467.26	416.10	465.93
	SNR (dB)	—	-55.0	-55.7	-55.0

5.3 Parasitic Elements

Due to the fact that the CCs are built with CMOS transistors, they present parasitic components inherent to their topology. These elements influence the behavior of the CCs at high frequencies, principally the parasitic capacitances which are responsibles of the limited frequency behavior [30].

In Fig. 5.14 are shown the most important parasitic elements in the CCs, where $(R_Y//C_Y)$ constitutes the input impedance on Y-terminal, when output X-terminal is open. R_Y, R_X and R_Z are the low frequency output resistance on Y, X and Z terminals, respectively, as it was seen before. $(R_Z//C_Z)$ is the output impedance on Z-terminal, where R_Z and C_Z can reproduce the high frequency peak of the output current flowing on Z-terminal when it is grounded [55].

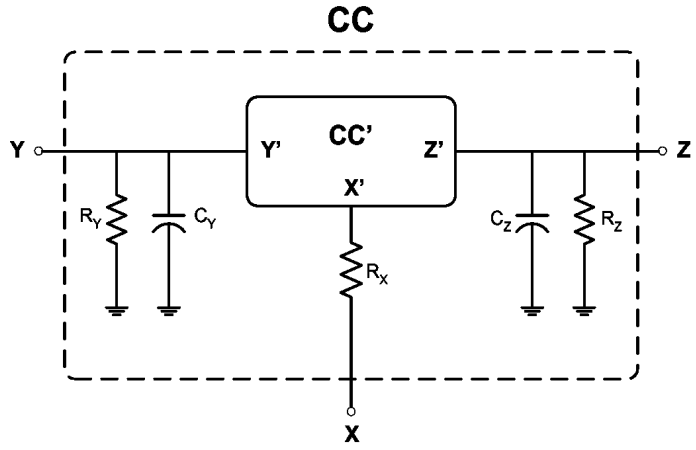


Figure 5.14: CCs parasitics elements.

The parasitic elements can be measured from the impedance curve in each terminal, connecting a voltage source in the interest terminal and dividing its value with the current through that terminal. So the resistive elements are measured at low frequency and the capacitances are deduced from the $-3dB$ cut-off frequency of the magnitude of the input impedance curve [30, 55]. The capacitive parasitic elements are determined with the following equations:

$$C_Y = \frac{1}{2\pi f_Y R_Y} \tag{5.1}$$

$$C_{Z+} = \frac{1}{2\pi f_{Z+} R_{Z+}} \tag{5.2}$$

$$C_{Z-} = \frac{1}{2\pi f_{Z-} R_{Z-}} \tag{5.3}$$

where f_Y, f_{Z+} and f_{Z-} are the $-3dB$ cut-off frequency of the magnitude of the impedance curve, described before.

In Table 5.43 are shown the capacitive parasitic elements of four CCs, which are used then in Chapter 6 in some applications.

Table 5.43: CCs capacitive parasitic elements

ELEMENTS	**DOCCI-VFA-S**	**DOCCII-VFC-S**	**DOCCII-VFB-LV**	**DOICCII-VMC-LV**
C_Y (fF)	2470	59.89	2.76	8.3
C_Z+ (fF)	568.0	18.34	530.86	18.52
C_Z- (fF)	566.2	18.27	530.26	18.53

Chapter 6

Applications

The CCs can be employed in a very large number of different applications. For instance, this chapter shows applications of CCs including universal filters, oscillators and inductance simulation.

6.1 CCI Applications

The tested applications for the CCI are two voltage-mode filters and a sinusoidal oscillator. For these circuits the $DOCCI - VFA - SCM$ was used, because it has the best gain value between the DOCCIs designed with simple CMs and CFs. As it will be seen, this filters and oscillator where designed for a CCI+ topology, so if a Dual-output type will be used, the modification is just to ground the $Z-$ terminal in order to obtain the original CCI needed for each application.

6.1.1 CCI-Based Filters

Band-pass filter (BPF)

A voltage-mode tunable BPF is shown in Fig. 6.1, which is a modified topology of the universal filter topology presented in [56].

The transfer function of the BPF is shown in Eq. (6.1), and the center frequency of the filter ω_0 is shown in Eq. (6.2). As we can see in (6.1), the parasitic

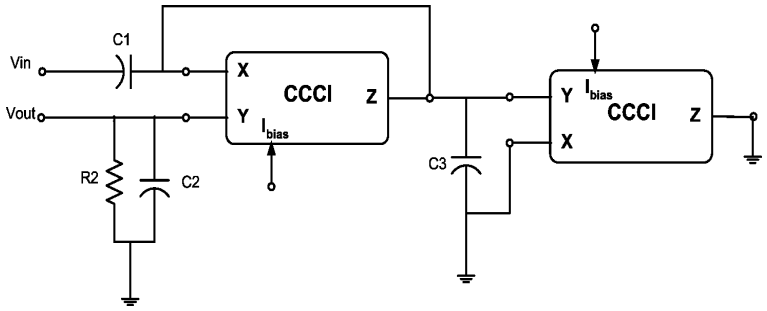


Figure 6.1: CCI-based BPF Filter

resistance Rx is a dominant parameter that strongly modifies the frequency response of the BPF.

$$Vout = \frac{sC_1R_2Rx}{s^2\left[(C_1+C_3)C_2Rx^2R_2\right] + s\left[(C_1+C_3)Rx^2 - (C_1-C_2+C_3)RxR_2\right] + (R_2+Rx)} \tag{6.1}$$

$$\omega_0 = \frac{1}{Rx}\sqrt{\frac{R_2+Rx}{(C_1+C_3)C_2R_2}} \tag{6.2}$$

In order to simulate this filter, the center frequency was chosen to be 3 MHz, so that the passive elements are: $R_2 = 5K\Omega$, $C_1 = C_2 = C_3 = 77.15pF$ and $Rx = 510.44\Omega$. This value of Rx is obtained with $Iref = 50\mu A$. As a result, the ideal and real frequency responses of the BPF are shown in Fig. 6.2. The ideal responses were obtained using MatLab (dashed lines), and the real responses were obtained using HSPICE (solid lines). For instance in the ideal case, to reach a center frequency of 1.57 MHz, the bias current $Iref$ was varied to $20\mu A$, that corresponds to a $Rx = 1.02K\Omega$; as mentioned above, for a center frequency of 3 MHz, $Iref$ was varied to $50\mu A$, that corresponds to a $Rx = 510.44\Omega$; and for a center frequency of 6 MHz, $Iref$ was varied to $160\mu A$, that corresponds to a $Rx = 246.21\Omega$. In HSPICE, for a center frequency of 1.57 MHz, $Iref$ was varied to $22\mu A$; for a center frequency of 3 MHz, $Iref$ was varied to $55\mu A$, and for a center frequency of 6 MHz, $Iref$ was varied to $185\mu A$.

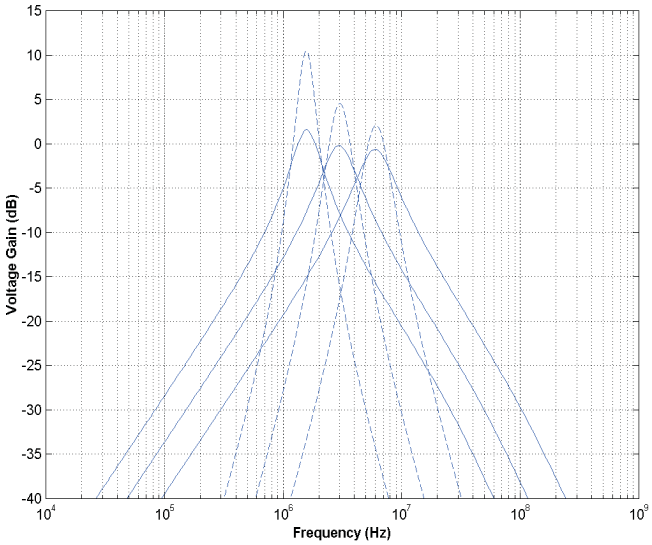


Figure 6.2: BPF filter AC response.

High-pass Filter (HPF)

The HPF circuit is shown in Fig. 6.3. This filter is a modified version of the filter presented in [56], where Y and X terminal were interchanged. The transfer function and the cut-off frequency of this filter are shown in Eqs. (6.3) and (6.4), respectively. As in the filter presented before, it is clear that the parasitic resistance Rx is an important parameter to determine the frequency response.

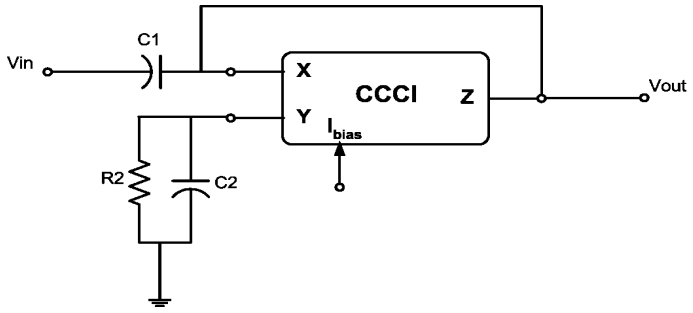


Figure 6.3: CCI-based BPF Filter

$$Vout = \frac{s^2 C_1 C_2 R_2 Rx + sC_1(Rx - R_2)}{s^2 C_1 C_2 R_2 Rx + s(C_1 Rx + 2C_2 R_2 - C_1 R_2) + 2} \tag{6.3}$$

$$\omega_0 = \sqrt{\frac{2}{C_1 C_2 R_2 Rx}} \tag{6.4}$$

As for the BPF, the HPF the center frequency was chosen to be 3 MHz, so that the passive elements are: $R2 = 1K\Omega$, $C_1 = C_2 = 105pF$ and $Rx = 510.44\Omega$, corresponding to an $Iref = 50\mu A$. The ideal and real frequency responses of the HPF are shown in Fig. 6.4, where the ideal responses were obtained using MatLab (dashed lines), and the real responses were obtained using HSPICE (solid lines). As in the past filter, in order to reach an ideal center frequency of 2.12 MHz, the bias current $Iref$ was varied to $20\mu A$ that corresponds to a $Rx = 1.02K\Omega$; for a center frequency of 3 MHz, $Iref$ was varied to $50\mu A$ that corresponds to a $Rx = 510.44\Omega$; and for a center frequency of 5 MHz, $Iref$ was varied to 300μA that corresponds to a $Rx = 180\Omega$. In HSPICE, for a cut-off frequency of 780 KHz, $Iref$ was varied to $22.5\mu A$; for a cut-off frequency of 3 MHz, $Iref$ was varied to 75μA, and for a the cut-off frequency of 5 MHz, $Iref$ was varied to $385\mu A$.

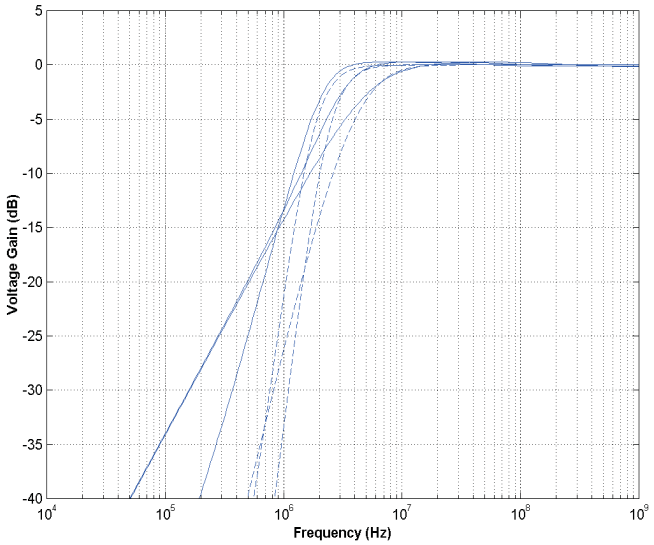


Figure 6.4: HPF filter AC response.

6.1.2 Sinusoidal Oscillator

Not only the CCIs can be applied to filtering applications but also they are quite useful to build an oscillator, as shown in Fig. 6.5 [57]. The characteristic equation and the oscillation frequency are shown in Eqs. (6.5) and (6.6), respectively. The oscillation condition is given by Eq. (6.7).

$$s^2\left[\frac{C_1C_4}{R_3+Rx}\right]+s\left[\frac{C_4R_3R_4+C_2R_3(R_3+Rx)}{R_3R_4Rx(R_3+Rx)}\right]+\frac{1}{R_4Rx(R_3+Rx)} \tag{6.5}$$

$$\omega_0=\sqrt{\frac{R_3+Rx}{C_1C_4R_4Rx(R_3+Rx)}} \tag{6.6}$$

$$\frac{1}{C_4R_3}=\frac{1}{C_2R_4} \tag{6.7}$$

The passive elements values are: $C_1 > C_4$, $C1 = 40pF$, $C2 = C4 = 30pF$, $R1 = R4 = 10K\Omega$. For an ideal case, in order to reach an oscillation frequency of 1.8 MHz, $Iref$ must to be equal to $40\mu A$, and for an oscillation frequency of 3.55 MHz, $Iref$ must to be equal to $350\mu A$. In HSPICE, for an oscillation frequency of 1.8 MHz, $Iref$ was varied to $70\mu A$, which is shown in Fig. 6.6. And for an oscillation frequency of 3.5 MHz, $Iref$ was varied to $155\mu A$, shown in Fig. 6.7.

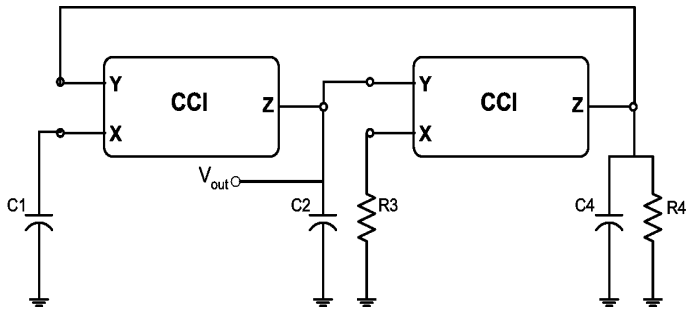


Figure 6.5: CCI-based Sinusoidal Oscillator

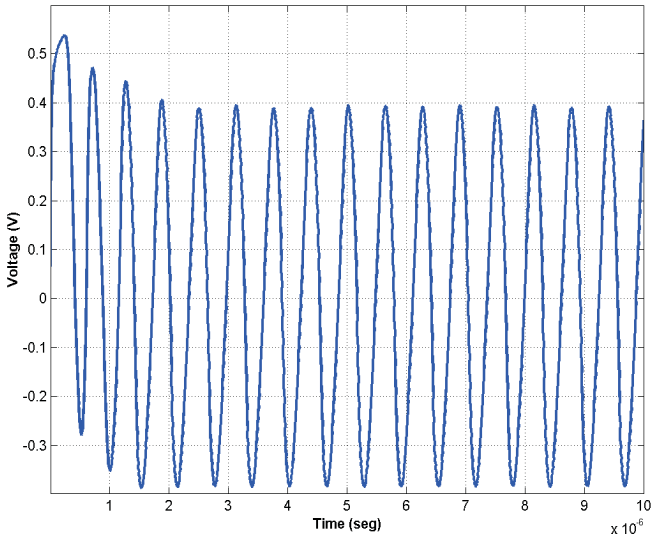


Figure 6.6: Oscillator AC response for 1.8 MHz.

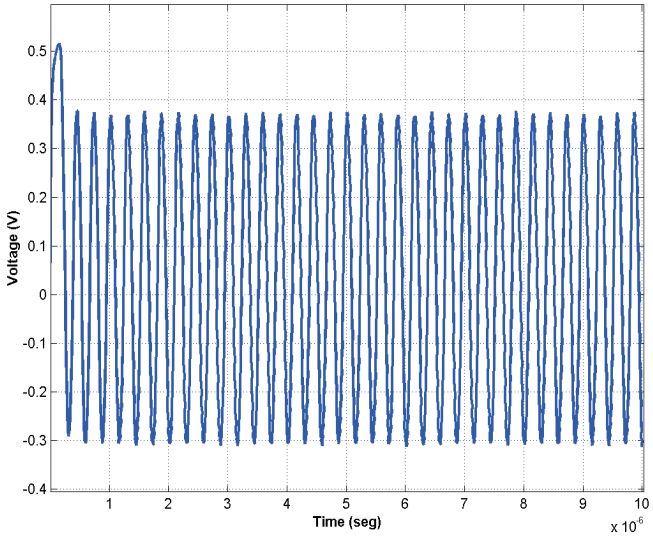


Figure 6.7: Oscillator AC response for 3.5 MHz.

These applications are designed for CCCIs, so the "Rx vs. Iref" curve is shown in Fig. 6.8

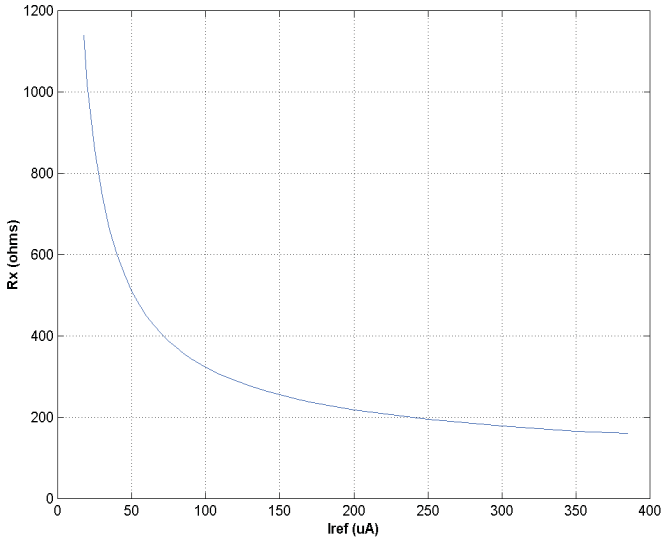


Figure 6.8: DOCCI-VFA-SCM Rx vs. Iref curve.

6.2 CCII Applications

The CCII is the most popular configuration, it has been applied to most of the CC applications. Now it will be shown a universal current-mode filter, two floating inductance simulators and a FTFN applied to another universal current-mode filter and to a sinusoidal oscillator.

6.2.1 Universal Current-Mode Filter

This universal filter was already shown ideally in Chapter 3. Now it will be shown the simulated results. $Iref$ is adjusted to the following values: $27\mu A$ for LP, $40\mu A$ for BP, $60\mu A$ for HP, and $40\mu A$ for Notch. The frequency responses of the CM universal filter using the $DOCCCII-VFC-SCM$, as a current controlled type, are shown in Fig. 6.9.

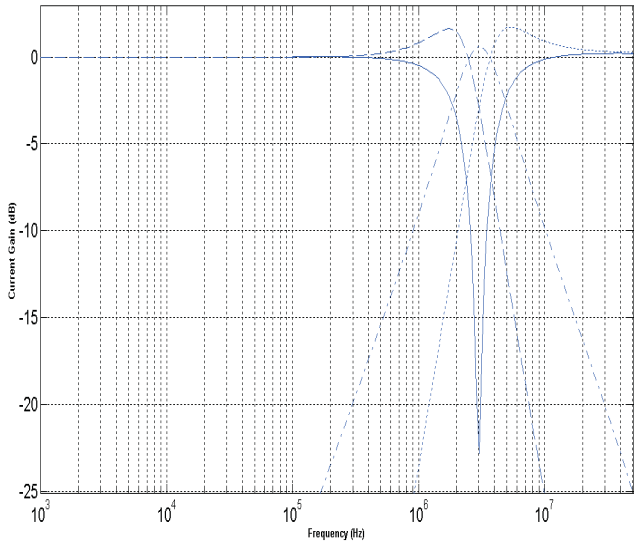


Figure 6.9: Universal current-mode AC response.

6.2.2 Floated Inductance Simulators

Floated Inductance Simulator 1

Lets consider the fifth-order LPF shown in Fig. 6.10. The transfer function of the ideal five order LPF is given by Eq. (6.8). Its realization using floated simulated inductors can be performed by using the DOCCCII-based floated inductance shown in Fig. 6.11, which is taken from [58]. The passive element values of the RLC filter are: $Rs = 17K\Omega$, $R_L = 1\Omega$, $C_1 = C_3 = C_5 = 30pF$, and $L_2 = L_4 = 295.211\mu H$. To simulate the floated inductances, L_2 and L_4 are evaluated using Eq. (6.9), which is derived by calculating the impedance between the nodes labelled by V1 and V2 by the NA method (Chapter 3). In this manner, $R_1 = R_2 = 10K\Omega$, $Rx = 2.88K\Omega$, $C_3 = 30pF$, and $R_4 = 29,267\Omega$. As a result, in Fig. 6.12 is shown the ideal (dashed line) and real (solid line) frequency response of the LPF. In this case, Iref is tuned to $85\mu A$.

$$V_0 = \frac{Iin}{s^5\left[C_1C_3C_5L_2L_4\right] + s^4\left[C_1C_3L_2L_4\right] + s^3\left[C_1C_3L_2 + C_1C_5L_2 + C_3C_5L_4\right] + s^2\left[C_1L_4 + C_1L_2 + C_3L_4\right] + s\left[\frac{L_4+L_2}{R_SR_L}\right] + \frac{1}{R_S}} \tag{6.8}$$

$$Leq = R1R2R_XC3/R4 \tag{6.9}$$

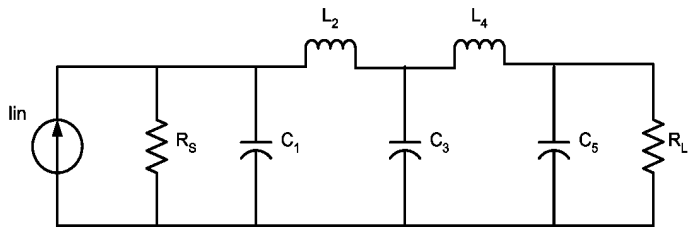


Figure 6.10: fifth-order LPF.

Again as in the universal current-mode filter, the $DOCCCII - VFC - SCM$ was used in order to simulate this floated inductance simulator. The Rx vs. Iref curve of this CC is shown in Fig. 6.13.

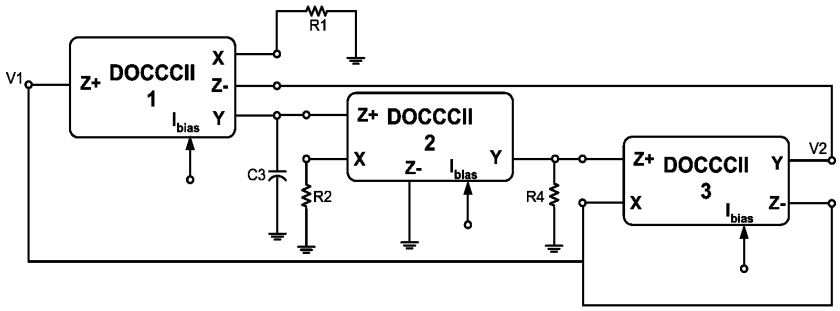


Figure 6.11: DOCCII-based Floated Inductance Simulator.

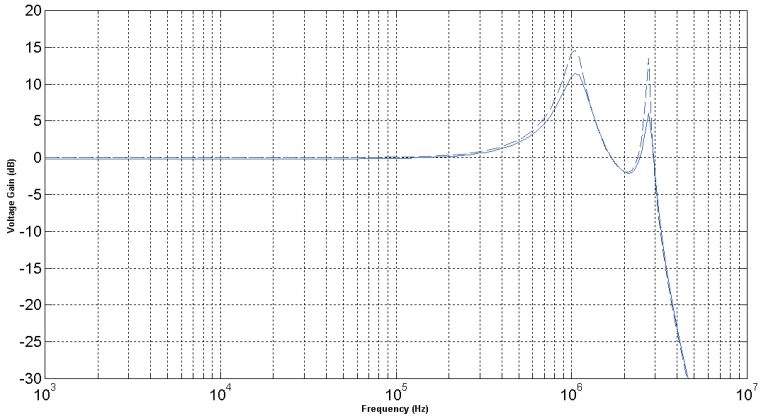


Figure 6.12: Floated Inductance Simulator 1 AC response.

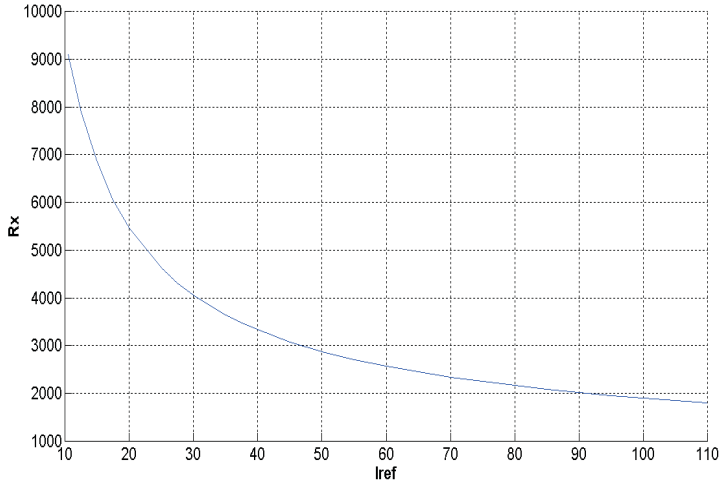


Figure 6.13: DOCCII-VFC-SCM Rx vs. Iref curve.

Floated Inductance Simulator 2

In [59] is shown a DOCCCII-based floated inductor which has the topology shown in Fig. 6.14. Assuming that $Rx_1 = Rx_2 = Rx_3 = Rx$, then the symbolic expression for Leq or the input impedance of the floated inductance simulator is given by Eq. (6.10). The Cint value can be evaluated using Eq. (6.11).

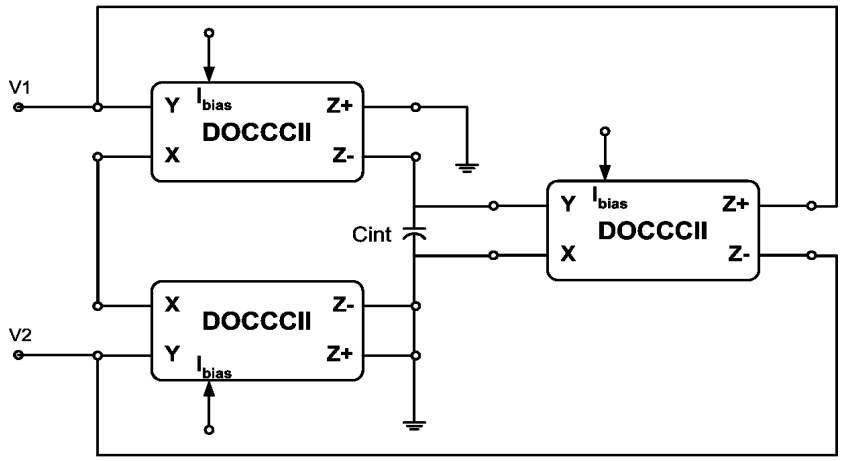


Figure 6.14: DOCCII-based Floated Inductance Simulator 2.

$$Leq = 2sC_{int}Rx^2 \tag{6.10}$$

$$C_{int} = \frac{L}{2Rx^2} \tag{6.11}$$

In Fig. 6.15 is shown the frequency response of the five order LPF. The ideal response is with a dash line and in a solid line is shown the frequency response of the filter with the DOCCCII-based inductor equivalent. The passive element values for the LPF of Fig. 6.10 are: $R_s = 17K\Omega$, $R_L = 1\Omega$, $C_1 = C_5 = 10pF$, $C_3 = 11pF$, $L_2 = L_4 = 295.211\mu H$. Replacing the passive inductors with the DOCCCII-based floated inductor equivalent, $Cint$ of each DOCCCII has a value equal to $208.68pF$, with a $Rx = 841.02\Omega$, that correspond to an $Iref = 50\mu A$.

For this second floated inductance simulator, was used the $DOCCII-VFB-LV$ in order to show that CCs based in low voltage CMs and CFs are suitable too

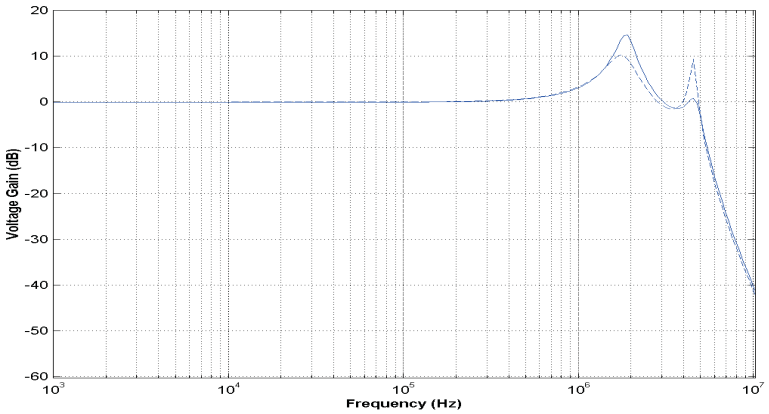


Figure 6.15: Floated Inductance Simulator 2 AC response.

to implement simulated inductances. In Fig. 6.16 is shown the Rx vs. Iref curve for this CC.

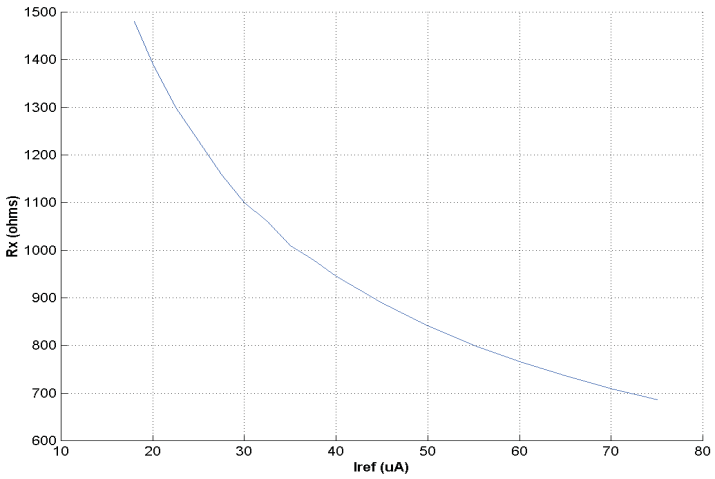


Figure 6.16: DOCCII-VFB-LV Rx vs. Iref curve.

6.2.3 Four Terminal Floating Nullor (FTFN)

When the nullator and norator are floating, one gets the four-terminals floating nullor (FTFN), which is a general building block suitable for linear and nonlinear systems implementations [12], exhibiting an infinite power gain between input and output ports.

In [60] was introduced a novel CMOS implementation of the FTFN using two translinear cells and cascode current mirrors. However, that implementation has two main drawbacks: The input impedances are not high because inputs are provided at the sources of two MOSFETs and it is not suitable for low voltage because it uses cascode current mirrors. In this manner, in this thesis is introduced a FTFN realization by using two CCII+s, where the proposed FTFN has high input impedances since they are provided at the gates of two MOSFETs, it is suitable for low voltage supplies of 1.5V, and the parasitic resistance Rx of the CCII+s is minimized by applying the technique presented in [61].
In Fig. 6.17 is shown the proposed CCII+, which is based in the $DOCCII-VFB-SCM$. Only in this application is used a modified version of the CCs shown in Appendix B and already analyzed in Chapter 5. The VF is formed by M1-M4, the simple CMs are formed by M11-M14, where M11 and M12 are added in order to obtain a low parasitic resistance at the X-terminal. Rx must be very low in order to approximate the ideal behavior of the FTFN. The sizing relationships for this CCII+ are: W for P-channel MOSFETs $M1 = 21.36\mu m$, $M3 = 65\mu m$, $M5 = M7 = M9 = 21.39\mu m$ and $M11 = M13 = 25\mu m$. W for N-channel MOSFETs $M2 = 6.25\mu m$, $M4 = 3.8\mu m$, $M6 = M8 = M10 = MX = 25\mu m$, $M12 = M14 = 6.5\mu m$. For all transistors the channel length (L) was equal to $1\mu m$. $VDD = -VSS = 1.5V$ with a current bias $Iref = 50\mu A$. In this manner, the realization of the FTFN using two CCII+s is shown in Fig. 6.18, where the port relations can be described by $I_X = I_Y = 0$, $I_Z = I_W$ and $V_X = V_Y$. The $I-V$ open-loop characteristic of the FTFN is shown in Fig. 6.19, from which the parasitic resistance of each CCII+ is evaluated to be $Rx = 16.66\Omega$, approximately.

Current-Mode Universal Filter

A current mode single input multiple output universal filter [62] is shown in Fig. 6.20. It employs only three FTFNs, two resistors and three capacitors. In Eqs. (6.12), (6.13) and (6.14) are shown the transfer functions of the low-pass filter (LPF), band-pass filter (BPF) and high-pass filter (HPF), respectively. The cut-off frequency (for the LPF and HPF) or center frequency (for the BPF) is given

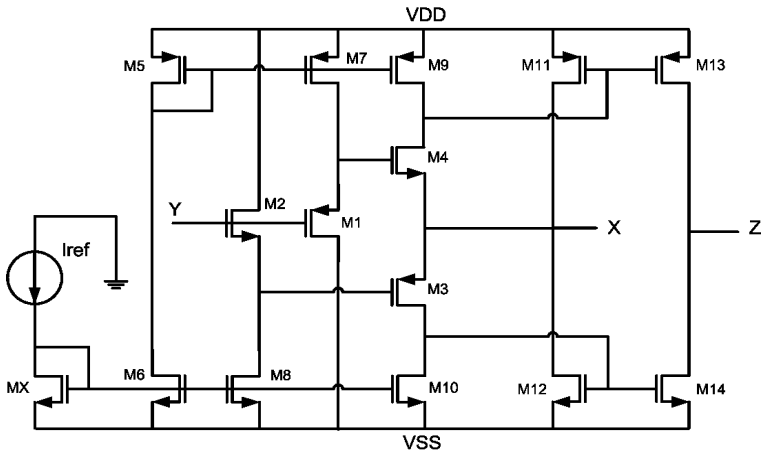


Figure 6.17: CCII with low Rx.

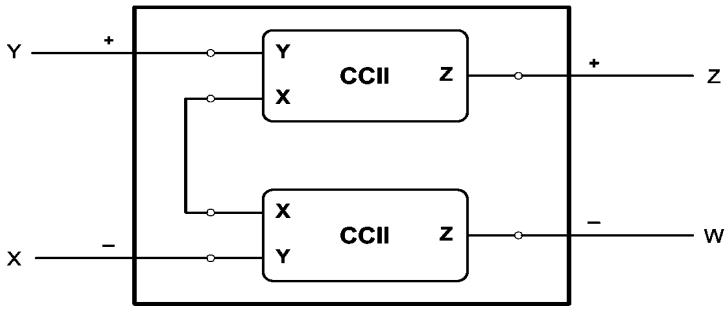


Figure 6.18: FTFN block diagram.

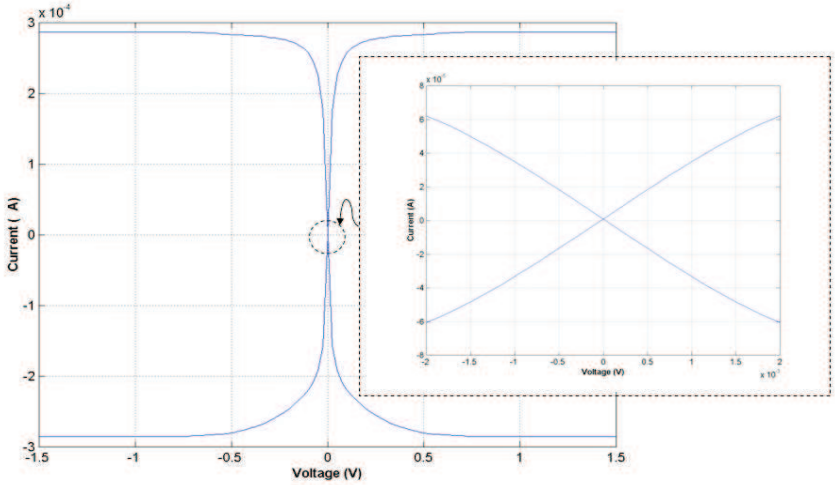


Figure 6.19: FTFN block diagram.

by Eq. (6.15)

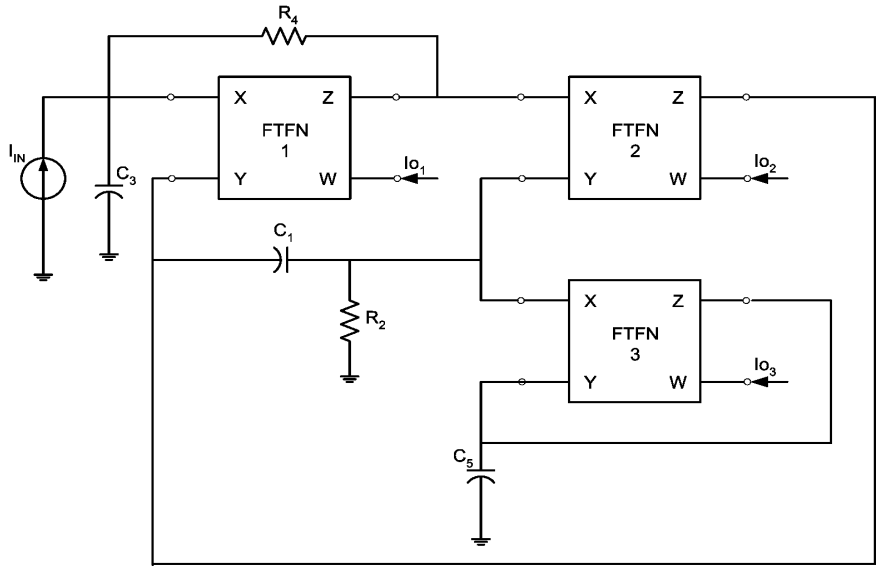


Figure 6.20: FTFN-based Universal Current-Mode Filter.

$$\frac{I_{0_1}}{Iin} = \frac{\frac{1}{C_1C_3R_2R_4}}{s^2 + \frac{s}{C_1R_2} + \frac{1}{C_1C_3R_2R_4}} \tag{6.12}$$

$$\frac{I_{0_2}}{Iin} = \frac{\frac{s}{C_3R_2}}{s^2 + \frac{s}{C_1R_2} + \frac{1}{C_1C_3R_2R_4}} \tag{6.13}$$

$$\frac{I_{0_3}}{Iin} = \frac{\frac{s^2C_5}{C_3}}{s^2 + \frac{s}{C_1R_2} + \frac{1}{C_1C_3R_2R_4}} \tag{6.14}$$

$$\omega_0 = \sqrt{\frac{1}{C_1C_3R_2R_4}} \tag{6.15}$$

This filter was designed for a cut-off frequency (BPF and HPF) or center frequency (BPF) of 2 MHz. The passive elements values were: $C_1 = C_3 = C_5 = 8pF$ and $R_2 = R_4 = 10K\Omega$. The frequency responses of the filter are shown in Fig. 6.21, were the dashed lines are the ideal responses and the solid lines are the HSPICE responses.

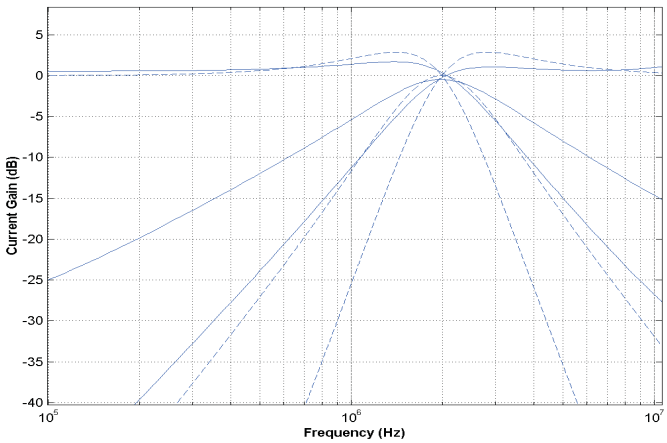


Figure 6.21: FTFN-based Universal Current-Mode Filter AC response.

Sinusoidal Oscillator

In Fig. 6.22 is shown a single FTFN grounded capacitors sinusoidal oscillator [63]. The frequency and condition of oscillation are given by Eqs. (6.16) and (6.17), respectively.

$$\omega_0 = \sqrt{\frac{R_1(R_4 + R_6 + R_7)}{C_3 C_8 (R_2 R_4 R_6 R_7)}} \tag{6.16}$$

$$\frac{C_3}{R_2 R_4} + \frac{C_8}{R_2 R_4} = \frac{C_8}{R_1 R_6} \tag{6.17}$$

The oscillation frequency was chosen to be 2 MHz, so that the passive elements values were: $C_3 = C_8 = 64.5pF$, $R1 = 500\Omega$ and $R_2 = R_4 = R_6 = R_7 = 1K\Omega$. The frequency of oscillation obtained in HSPICE is shown in Fig. 6.23.

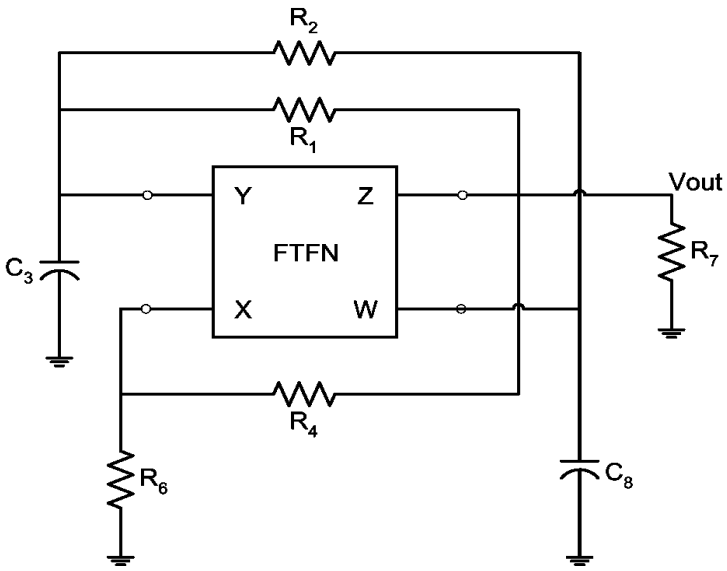


Figure 6.22: FTFN-based Sinusoidal Oscillator.

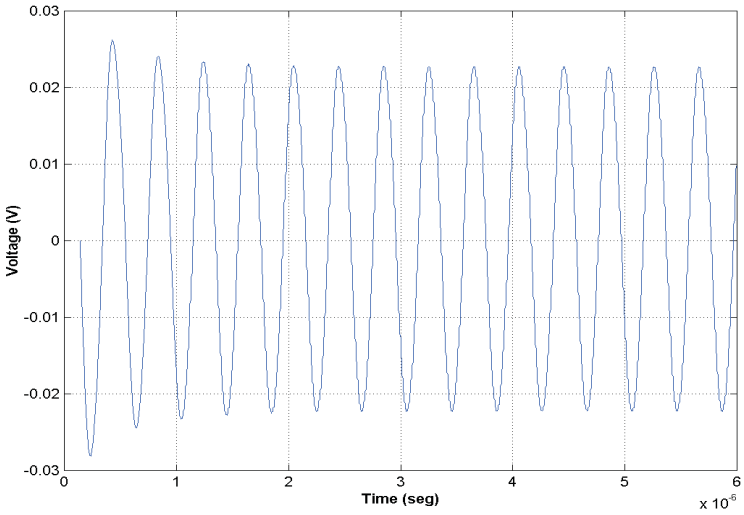


Figure 6.23: FTFN-based Sinusoidal Oscillator AC response.

6.3 ICCII Applications

In this section is shown an Universal Voltage-Mode Filter which has a LPF, BPF and Notch responses using only one ICCII, four resistors and two capacitors.

6.3.1 Universal Voltage-Mode Filter

The filter topology [54] is shown in Fig. 6.24, where $R_1 = (1-a)R_3$, $R_2 = aR_3$, $R_4 = bR_3$ and $a = b/(b+2)$. Substituting the ICCII of this filter for its Nullor equivalent, the transfer function of each response is obtained, which are shown in Eqs. (6.18), (6.19) and (6.20) for the LPF, BPF and Notch respectively.

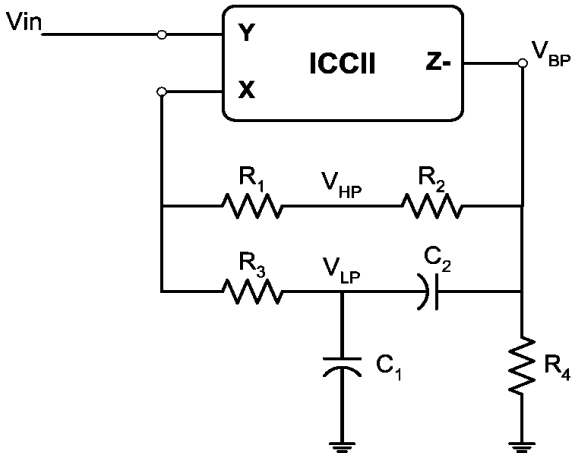


Figure 6.24: Universal Voltage-Mode topology.

$$-\frac{(R_2 + R_1)}{DEN} \tag{6.18}$$

$$\frac{sC\,(R2 + R1)\,R4}{DEN} \tag{6.19}$$

$$\frac{(-C^2 s^2 R4\ R3\ R2 + (-2\,CR2\ R3 + CR1\ R4)\,s - R2)}{DEN} \tag{6.20}$$

Where:

$DEN = C^2(R_4\ R_3\ R_2 + R_4\ R_3\ Rx + R_4\ R_1\ R_3 + R_4\ R_1\ Rx + R_4\ Rx\ R_2)s^2 +$
$C(2\,R_2\ R_3 + 2\,Rx\ R_3 + 2\,Rx\ R_2 + 2\,R_1\ R_3 + 2\,Rx\ R_1 + Rx\ R_4)s +$
$R_1 + R_2 + Rx$

The ideal response is shown in Fig. 6.25 and the response obtained in HSPICE is shown in Fig. 6.26. The LPF, BPF and Notch responses are shown in a dash, dash-dot and a solid line, respectively. For this filter it was not used a current controlled ICC. The passive element values were: $R_1 = 10K\Omega$, $R_2 = 10K\Omega$, $R_3 = 20K\Omega$, $R_4 = 40K\Omega$, $C_1 = C_2 = 56.23pF$. $Iref$ was $50\mu A$ that correspond to a $Rx = 76\Omega$. The ICCII used was the $DOICCII - VFC - LV$ with $Z+$ terminal grounded in order to have a ICCII-.

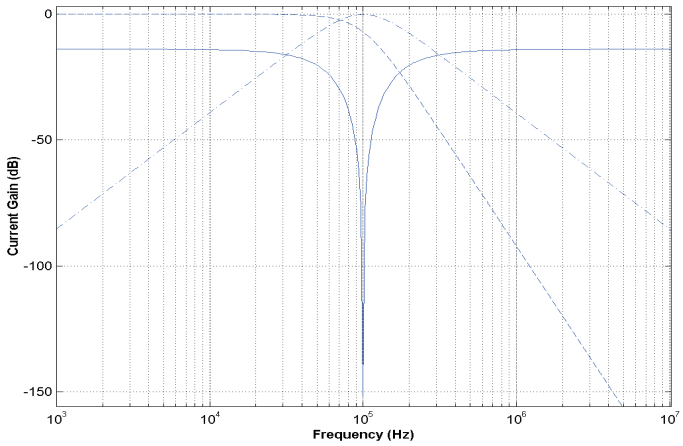


Figure 6.25: Universal Voltage-Mode ideal response.

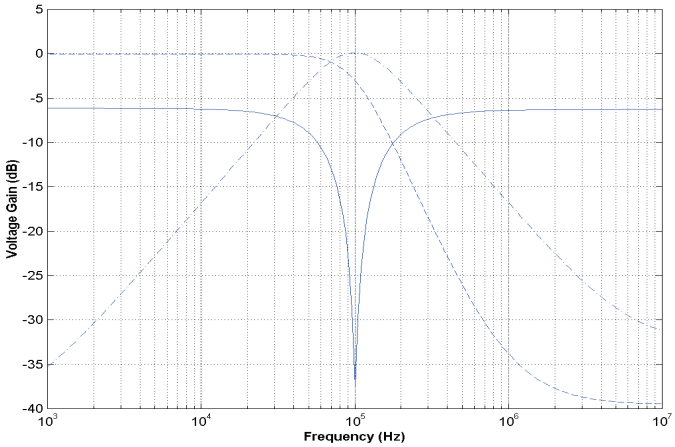


Figure 6.26: Universal Voltage-Mode HSPICE response.

Chapter 7

Conclusions

A CC is a minimum 3-terminals device which can perform many useful analog signal processing functions. The CC is not a new electronic block, since it was first designed in 1969, but it is recently seen as a good alternative for Current-Mode design in order to deal with Voltage-Mode problems.

As a first design step, a CC can be easily designed by combining and by connecting the four UGCs (VF, VM, CF and CM) as basic construction blocks. From the characteristic equation of each CC, they can be constructed just by superimposing or by cascading the different UGCs in order to accomplish it.

The nullor is a very useful concept that helps the designer to easily analyze a given element, circuit or system. The CCII nullor equivalent was taken from literature, but the CCI and CCIII nullor equivalents were contributions of this work. So, using this ideal concept it was easy to analyze a CC-based circuit in order to obtain their characteristics equations. Although the nullor was used to analyze ideally CC-based circuits, the parasitic resistance at the X-terminal of each CC was included as it is a term that strongly modifies the CC behavior, permitting to obtain CCCs.

Once a CC based in the UGCs blocks was designed, and taking the nullor as a powerful analyzing ideal tool, each UGC can be designed in a transistor level. Each UGC was designed as a symmetrical type circuit. Once this was done, each CC can be implemented, just by interconnecting these UGCs. When these blocks are connected between them to form a CC, their dimensions can be modified in

order to have a better performance, but once we have this improved UGCs, they can be taken as a fixed block to change from one type of CC to another one, without any modification, just by interconnecting them as it was done in Chapter 2. These easy way to construct a CC is a contribution of this work. So, based on this, all CCs topologies were designed in a transistor level, including the ICCI and ICCIII which are contributions too.

Finally some implementations were shown where the better performances comes from the CCII types. As it can be seen CCI and ICCII have some behavior problems due to the fact that ideal and HSPICE results doesn't match at all.

7.1 Lines of Future Work

Once it was designed all CCs topologies, a future work proposed is:

- Optimization of all CC topologies in order to have better performances in the CC applications.
- Design very low voltage CC, based in the CMs designed in [64] for very low voltage applications.
- Design filtering, oscillation and inductor simulator applications for ICCI and ICCIII topologies in order to investigate their suitability for a real implementation.
- Improve the Rx value in order to reach lower levels and have CCs closer to the ideal behavior.
- Investigate new VFs topologies due to the fact that most of the electrical parameters depends on this UGC. More over, the VM depends on the VF topology.
- Exploration on the transformation of CCI-based circuits to either or both CCII-based and CCIII-based circuits. Also among ICCI-based, ICCII-basec and ICCIII-based circuits.

Published Papers

1. E. Tlelo-Cuautle, D. Moro-Frías, C. Sánchez-López, M. A. Duarte-Villaseñor, *Synthesis of CCII-s by superimposing VFs and CFs through genetic operations*, IEICE Electronics Express, Vol. 5, No. 11, Pp: 411-417. June 2008.

2. D. Moro-Frías, E. Tlelo-Cuautle, M. Fakhfakh, *Design of CCI-based tuneable active filters and sinusoidal oscillator*, IEEE ICCDCS, ISBN 978-1-4244-1957-9, Cancún, México, April 28-30, 2008.

Appendix A

MOS Transistor Characteristics

In today's IC industry, a solid understanding of semiconductor devices is essential, more so in analog design where transistors are not considered as simple switches and many of their second-order effects impact the circuits performances. This effects become more significant as IC technology scales the devices [19].

A.1 Threshold Voltage

Considering a NMOS transistor connected as it is shown in Fig. A.1, the gate and the substrate form a capacitor, and as the voltage in gate terminal (V_G) becomes more positive, the holes in the p-substrate becomes repelled from the gate area, leaving negative ions behind, generating a depletion region, where no current flows because no charge carriers are available. As V_G increases, the width of the depletion region and the potential at the oxide-silicon interface increase too. When the interface potential reaches a sufficiently positive value, electrons flow from the source terminal to the interface and eventually to the drain terminal. The V_G for which this occurs is called "Threshold Voltage" (V_{TH}), where a channel of charge carriers is formed under the gate oxide, between source and drain terminal and the transistor is turned on. If V_G increases further, the charge in the depletion region remains relatively constant while the channel charge density continues to increase, providing a greater current from source to drain terminals [19].
The gate and body form a parallel-plate capacitor with the oxide layer acting

as dielectric. The positive V_G causes positive charge to accumulate on the top plate of the capacitor or gate electrode. The negative charge is formed on the bottom plate by the electrons in the induced channel. So, an electric field is created in vertical direction, which controls the amount of charge in the channel, channel conductivity and the current that will flow through the channel when V_{DS} is applied [20].

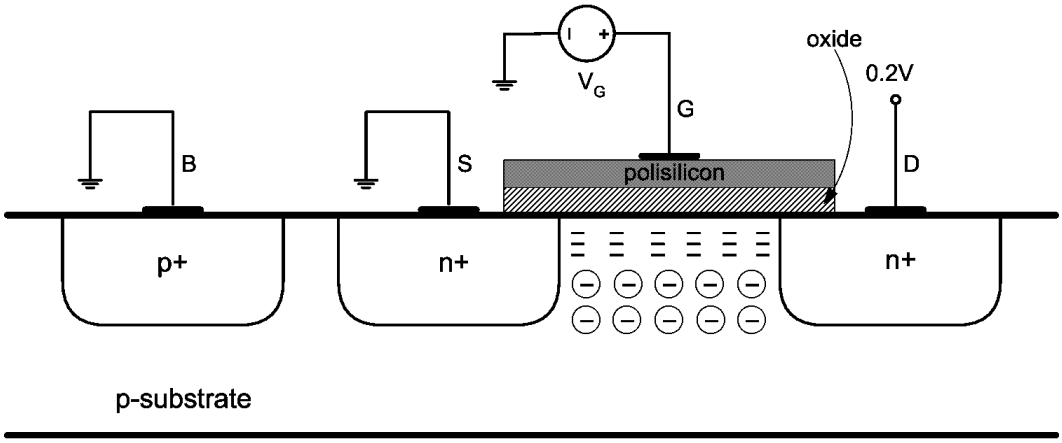


Figure A.1: NMOS Transistor.

The Threshold Voltage is defined by the following equation:

$$V_{TH0} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{Cox} \tag{A.1}$$

Where Φ_{MS} is the difference between the work functions of the polysilicon gate an the silicon substrate. Φ_F is the strong inversion surface potential:

$$\Phi_F = \frac{kT}{q} \ln\left(\frac{N_{sub}}{n_i}\right) \tag{A.2}$$

Q_{dep} is the charge in the depletion region:

$$Q_{dep} = \sqrt{4q\varepsilon_{si}\left|\Phi_F\right| N_{sub}} \tag{A.3}$$

Where Cox is the gate oxide capacitance per unit area, q is the electron charge, ε_{Si} is the silicon permittivity, N_{sub} the doping concentration of the p-type substrate and n_i the intrinsic carrier concentration at $27°C$.

For real situations, the threshold value obtained from the above equation may not be suited to circuit design, for this reason it is typically adjusted by implantation of dopants into the channel area during device fabrication, altering the doping level of the substrate near the oxide interface [19]. Standard practice is to implant the proper type of ions into the substrate in the channel region to adjust the threshold voltage to the desired value. This type of CMOS transistor are also called Enhancement-type MOSFET [20], and are the kind of transistor that will be used in this work. If the opposite impurities are implanted in the channel region of the substrate, the threshold for an n-channel transistor can be made negative. This type of transistor are called Depletion-type MOSFET and can have current flow between drain and source terminals for zero values of the gate-source voltage (V_{GS}) [21].

A.2 CMOS Transistor Regions

There are various regions of operation of the MOS transistor, which depends on the value of $V_{GS} - V_{TH}$. The first region is where $V_{GS} - V_{TH}$ is equal to zero or negative, so the transistor is in the Cutoff region. In Cutoff region the drain current $i_D = 0A$ and $V_{GS} - V_{TH} < 0$.
When the transistor channel is formed between drain and source terminals, the drain current i_D can flow between this two terminals. The dependence of this current can be developed by considering the characteristics of an incremental length of the channel dy. This is illustrated in Fig. A.2:

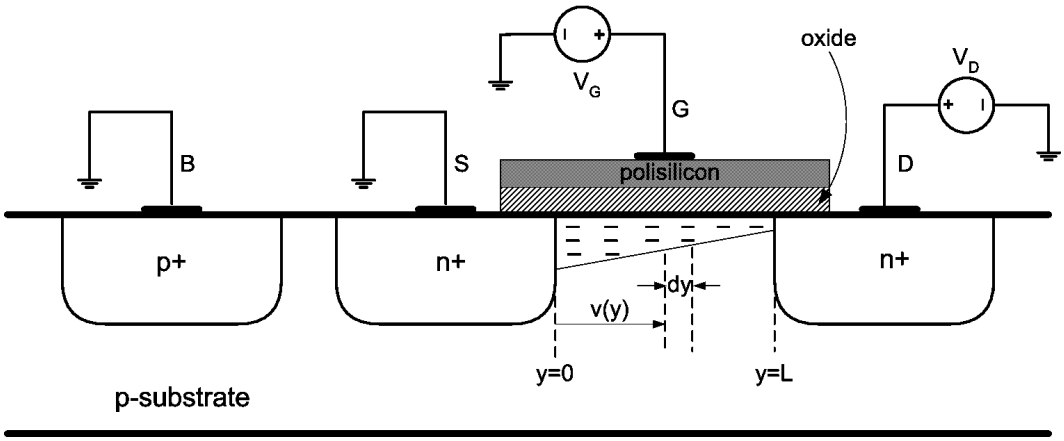


Figure A.2: NMOS Transistor.

Where W is the transistor width (into the page) and the voltage V_{DS} is small. The resistance in the channel per unit of length dy can be written as:

$$dR = \frac{dy}{\mu_n Q_I(y) W} \tag{A.4}$$

Where μ_n is the average mobility of the electrons. The voltage drop, referenced to the source, along the channel in the y direction is:

$$dv(y) = i_D dR = \frac{i_D dy}{\mu_n Q_I(y) W} \tag{A.5}$$

The charge per unit area in the channel $Q_I(y)$ is given by the following Eq. (A.6):

$$Q_I(y) = Cox\left[V_{GS} - V(y) - V_{TH}\right] \tag{A.6}$$

Substituting Eq. (A.6) into Eq. (A.5) and reordering is obtained:

$$i_D dy = W \mu_n Cox\left[V_{GS} - V(y) - V_{TH}\right] dV(y) \tag{A.7}$$

Integrating Eq. (A.7) along the channel:

$$\int_0^L i_D dy = \int_0^{V_{DS}} W \mu_n Cox\left[V_{GS} - V(y) - V_{TH}\right] dV(y) \tag{A.8}$$

Solving Eq. (A.8):

$$i_D = \mu_n Cox \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{A.9}$$

Eq. (A.9) is only valid for $V_{GS} \geq V_{TH}$, $V_{DS} \leq (V_{GS} - V_{TH})$ and L greater than the minimum L allowed for the technology that has been used. The factor $\mu_n Cox$ is defined as the device-transconductance parameter:

$$\mu_n Cox = K'n = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \tag{A.10}$$

Plotting Eq. (A.9), for different values of V_{GS}, we have the parabolas shown in Fig. A.3, where is illustrated that the current capability of the transistor increases with V_{GS}:

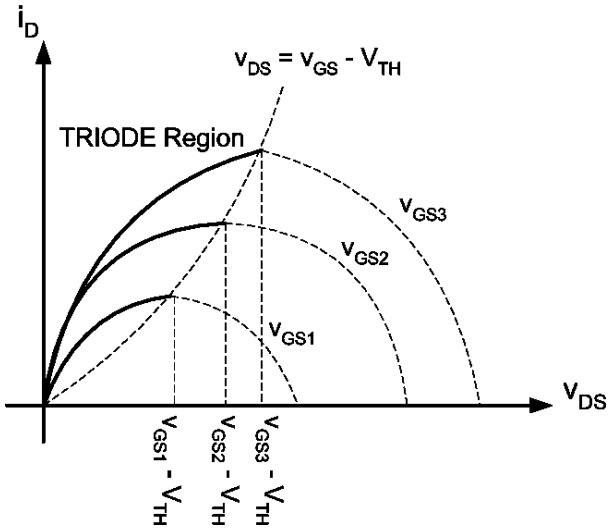


Figure A.3: i_D vs. V_{DS} in the triode region.

After this, we can say the second region known as non-saturated or Triode region is described by Eq. (A.9).

The third region occurs when V_{DS} is greater than $V_{DS}(sat)$ or $V_{GS} - V_{TH}$. At this point the current i_D becomes independent of V_{DS}. So, V_{DS} in Eq. (A.9) is replaced by $V_{DS}(sat)$, obtaining the following equation:

$$i_D = \frac{1}{2} K'n \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{A.11}$$

for: $0 \leq (V_{GS} - V_{TH}) \leq V_{DS}$

The i_D current does not follow the parabolic behavior for the previous relation (Eq. (A.4)), in fact this current becomes relatively constant in the third region, known as Saturation region. That is, from Eq. (A.6) the local density of inversion layer charge is proportional to $V_{GS} - V(y) - V_{TH}$. Thus, if $V(y)$ approaches $V_{GS} - V_{TH}$, then $Q_I(y)$ drops to zero. That is, as shown in Fig. A.4, if V_{DS} is slightly greater than $V_{DS}(sat)$, then the inversion layer stops at $y < L$, and it is said the channel is "pinched off", shown in Fig. A.5. As V_{DS} increases more, the point at which Q_I equals zero gradually moves toward the source. So, taken Eq. (A.8) for a saturated device, and since Q_I is the density of mobile charge, the integral on the left-hand side must be taken from $y = 0$ to $y = L'$, where L' is the point at which Q_I drops to zero, and on the right-hand side from $V(y) = 0$ to $V(y) = V_{GS} - V_{TH}$. As a result:

$$i_D = \frac{1}{2} K'n \frac{W}{L'} \left(V_{GS} - V_{TH}\right)^2 \tag{A.12}$$

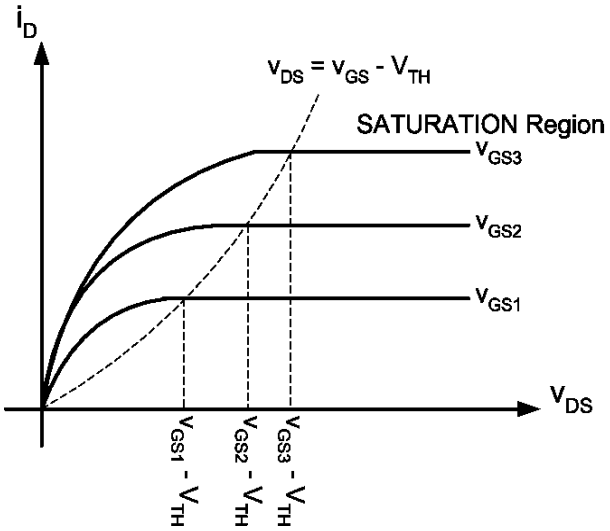


Figure A.4: i_D vs. V_{DS} in the saturation region.

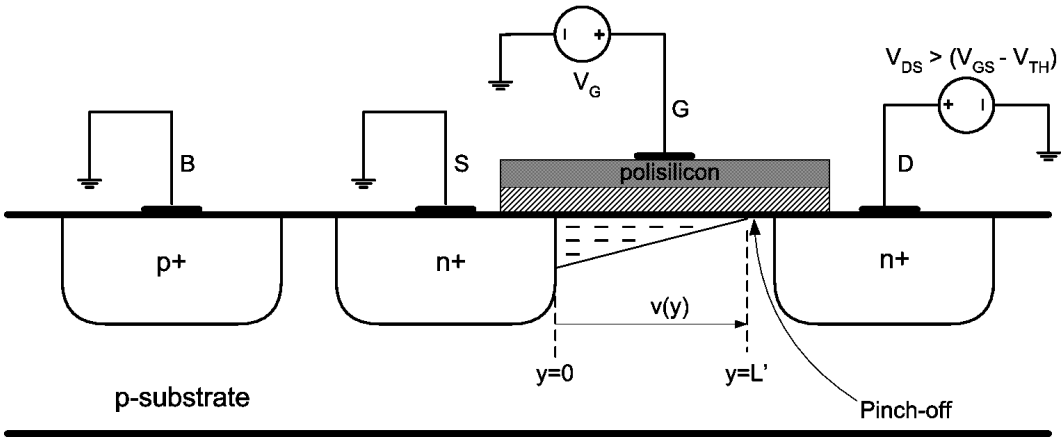


Figure A.5: Pinch-off behavior

With the approximation $L \approx L'$, a saturated MOSFET can be used as a current source connected between drain and source terminals. This current depends on $V_{GS}-V_{TH}$, $V_{DS}(sat)$ or overdrive voltage, describing a figure of merit that indicates how well a device converts a voltage to a current, or more specifically, the change in the drain current divided by the change in the V_{GS}. This quantity is known as Transconductance (gm) and is described by the following equations:

$$gm = \frac{\partial I_D}{\partial V_{GS}}|_{VDS_{const}} \tag{A.13}$$

$$gm = \mu_n Cox \frac{W}{L}\left(V_{GS} - V_{TH}\right) \tag{A.14}$$

$$gm = \frac{2I_D}{V_{GS} - V_{TH}} \tag{A.15}$$

$$gm = \sqrt{2\mu_n Cox \frac{W}{L} I_D} \tag{A.16}$$

All previous equations are for NMOS transistors, but for PMOS type, Eq. (A.9) and (A.11) are as follows:

$$i_D = \mu_p Cox \frac{W}{L}\left[\left(V_{SG} - |V_{TH}|\right) V_{SD} - \frac{V_{SD}^2}{2}\right] \tag{A.17}$$

$$i_D = \frac{1}{2}\mu_p Cox \frac{W}{L}\left(V_{SG} - |V_{TH}|\right)^2 \tag{A.18}$$

Therefore, V_{GS} becomes V_{SG}, V_{DS} becomes V_{SD}, V_{THn} becomes $-V_{THp}$, and so on. In PMOS transistor the Threshold voltage is negative, so the condition to keep this transistor in saturation region is now $V_{SD} > V_{SG} - |V_{THp}|$, and the i_D current now flows from the source to the drain terminals.

A.3 Second-Order Effects

In this section are described two of the most important second-order effects that directly impact in analog design.

A.3.1 Body Effect

The Body Effect directly impact in an increment of the Threshold Voltage level. Is common to see some applications with the substrate terminal connected to the source terminal, where a pn junction is formed between the substrate and the induced channel, generating a constant zero bias or cut-off, and as a consequence, the Threshold Voltage does not change its value. In integrated circuits the substrate, which is common to many MOS transistors, is connected to the most negative (NMOS) or most positive (PMOS) power supply, in order to maintain the cut-off condition for all the substrate-to-channel junctions, but this reverse bias voltage between source and substrate (V_{SB}) will have an effect on the device operation [20]. Lets consider a NMOS transistor with its substrate terminal more negative than its source terminal. As a consequence of the reverse bias voltage, the depletion region becomes wider, reducing the channel depth. So, in order to return the channel to its former state, V_{GS} has to be increased.
From Eq. (A.1) it is clear that the Threshold Voltage is function of the total charge in the depletion region because the gate charge must mirror Q_I before an inversion layer is formed [19]. There for, as V_{SB} increase, V_{TH} will do the same. After this, the Threshold Voltage in a MOSFET is given by:

$$V_{TH} = V_{TH0} + \gamma \left[\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right] \tag{A.19}$$

Where V_{TH0} is the same Threshold Voltage for $V_{SB} = 0$ given in Eq. (A.1),

Φ_F is the strong inversion surface potential described by Eq. (A.2) and γ is a fabrication process parameter known as body-effect parameter, which is given by:

$$\gamma = \frac{\sqrt{2qN_{sub}\varepsilon_{SI}}}{Cox} \tag{A.20}$$

Eq. (A.20) shows that an incremental change in V_{SB} generates an incremental change in V_{TH} which results in an incremental change in i_D. Due to this, substrate terminal acts as another gate for the transistor [20].

A.3.2 Channel Modulation Effect

As it was seen before, the channel length gradually decreases as the potential difference between gate and drain terminals increases (V_{DS}), in other words, as V_{DS} increase beyond $V_{DS}(sat)$, the channel pinch-off point is moved slightly away from the drain toward the source. The voltage across the channel is constant $V_{DS}(sat) = (V_{GS} - V_{TH})$, and the additional voltage applied to the drain terminal appears as a voltage drop across the narrow depletion region between the channel and the drain diffusion, accelerating the electrons that reach the end of the channel, sweeping them across the depletion region into the drain. This is better explained by Fig. A.6:

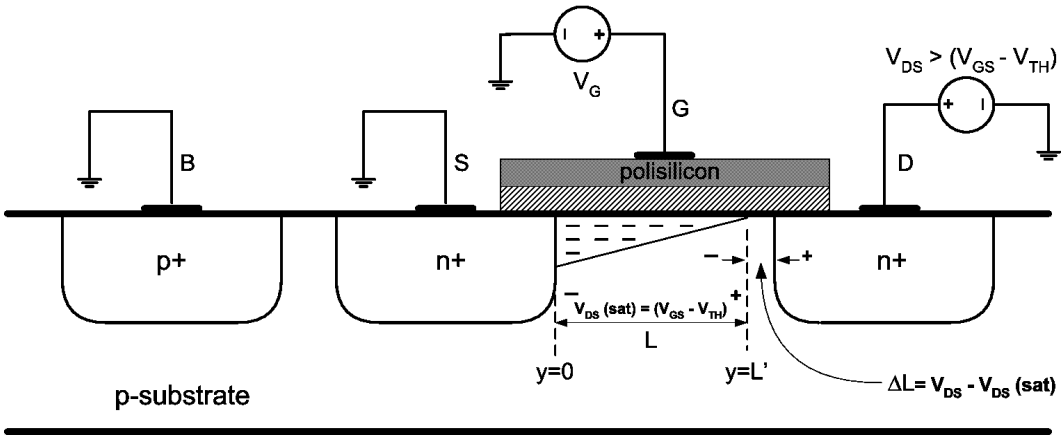


Figure A.6: Channel Modulation behavior.

If $L' = L - \Delta L$, reordering this, is obtained:

$$\frac{1}{L'} \approx \frac{1 + \left(\frac{\Delta L}{L}\right)}{L} \tag{A.21}$$

Assuming a first-order relationship between $\Delta L/L$ and V_{DS}:

$$\frac{\Delta L}{L} = \lambda V_{DS} \tag{A.22}$$

Substituting Eq. (A.22) in Eq. (A.21), and then in Eq. (A.12) we obtain the saturation equation with the channel modulation effect:

$$i_D = \frac{1}{2} K'n \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right) \tag{A.23}$$

Where λ is the channel-length modulation coefficient and is a MOSFET parameter. From Eq. (A.23), it is assumed that L is constant and the real dependence of I_D with V_{DS} is included by the factor $(1+\lambda V_{DS})$. After this, Fig. A.4 is modified by the channel-length modulation, as shown in Fig. A.7:

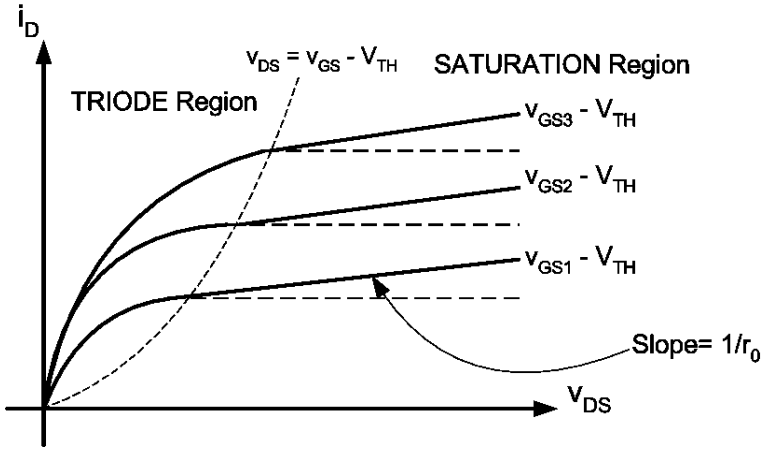


Figure A.7: $i_D vs. V_{DS}$ in the saturation region with channel-length modulation effect.

As a consequence of the channel-length modulation, the output resistance has finite value:

$$r_0 \equiv \left[\frac{\partial i_D}{\partial V_{DS}}\right]^{-1} \tag{A.24}$$

$$r_0 = \left[\lambda \frac{K'n}{2} \frac{W}{L} \left(V_{GS} - V_{TH}\right)^2\right]^{-1} \tag{A.25}$$

Appendix B

CCs transistor level topologies

B.1 CCs

B.1.1 CCIs

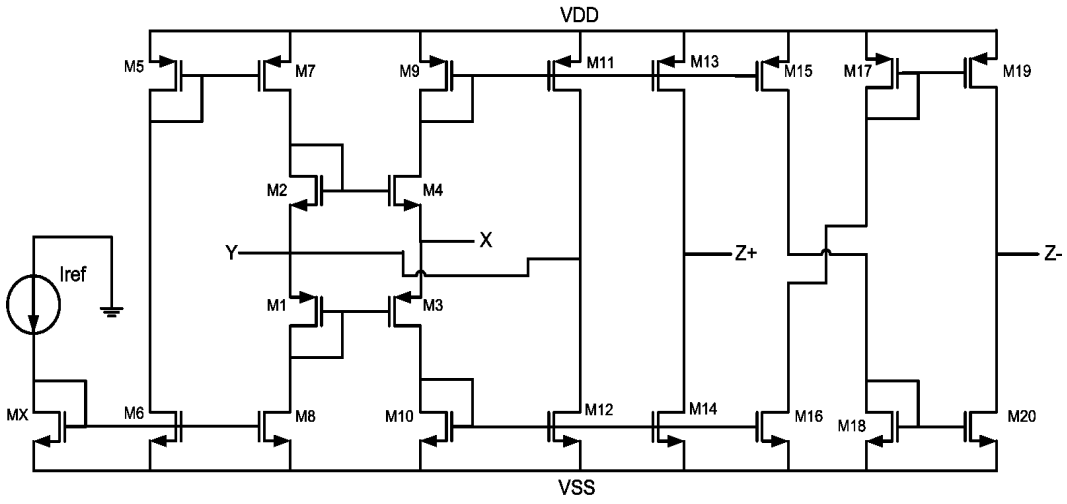


Figure B.1: DOCCI-VFA-S

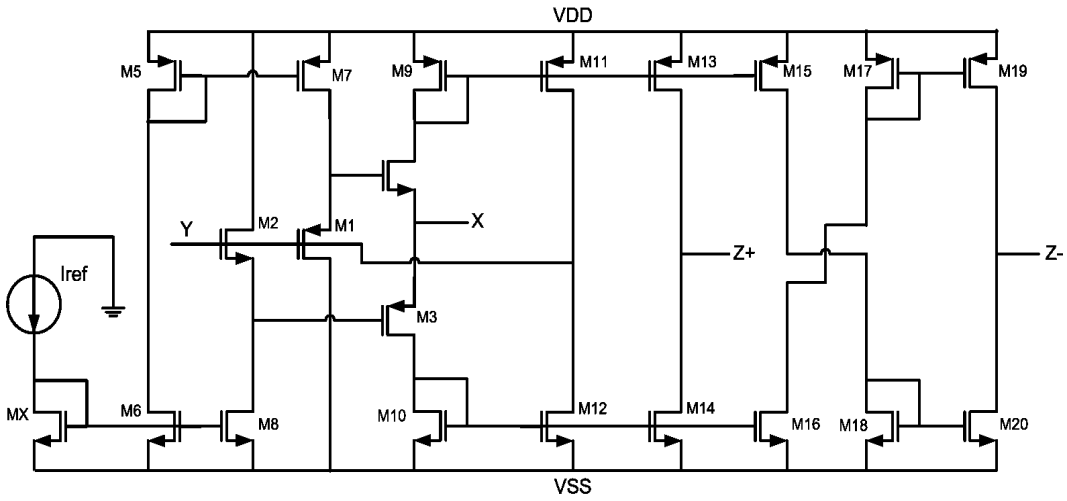


Figure B.2: DOCCI-VFB-S

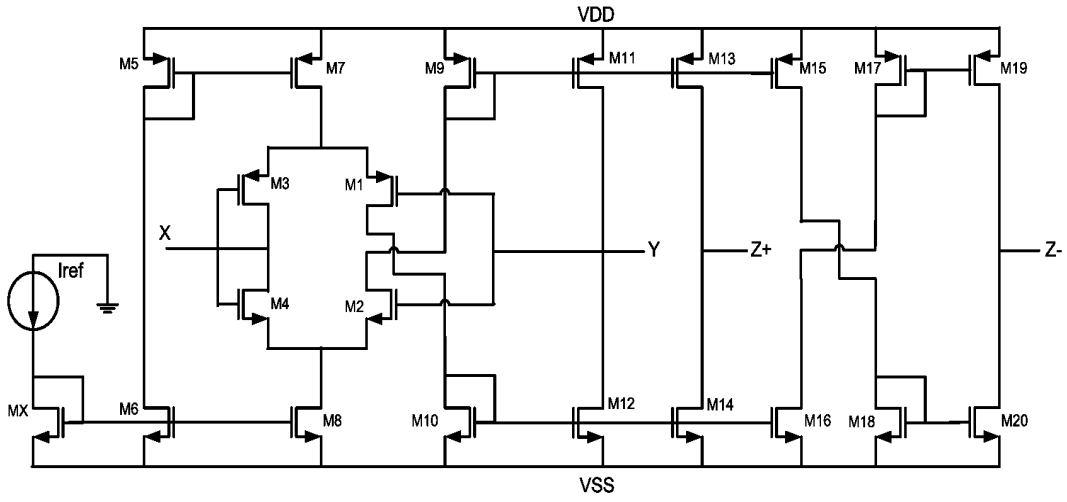


Figure B.3: DOCCI-VFC-S

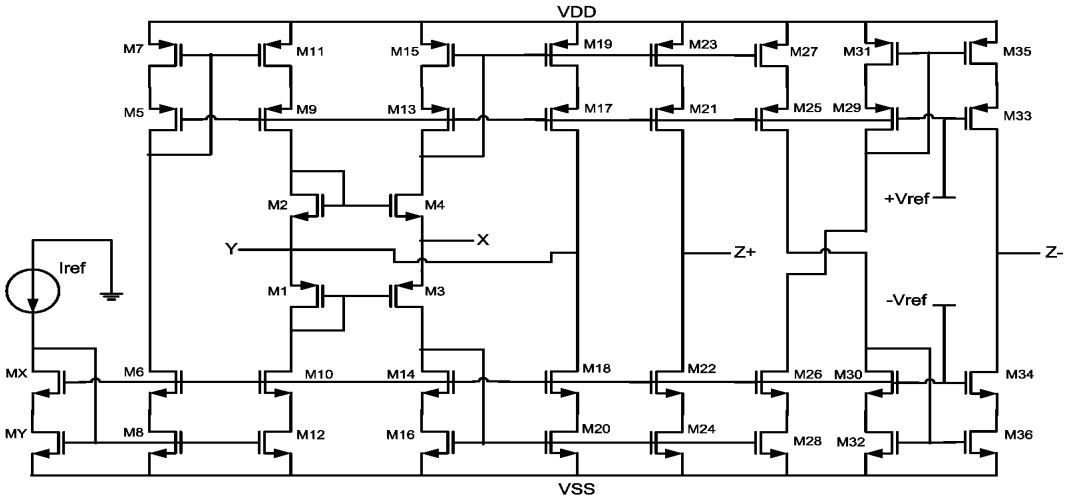


Figure B.4: DOCCI-VFA-LV

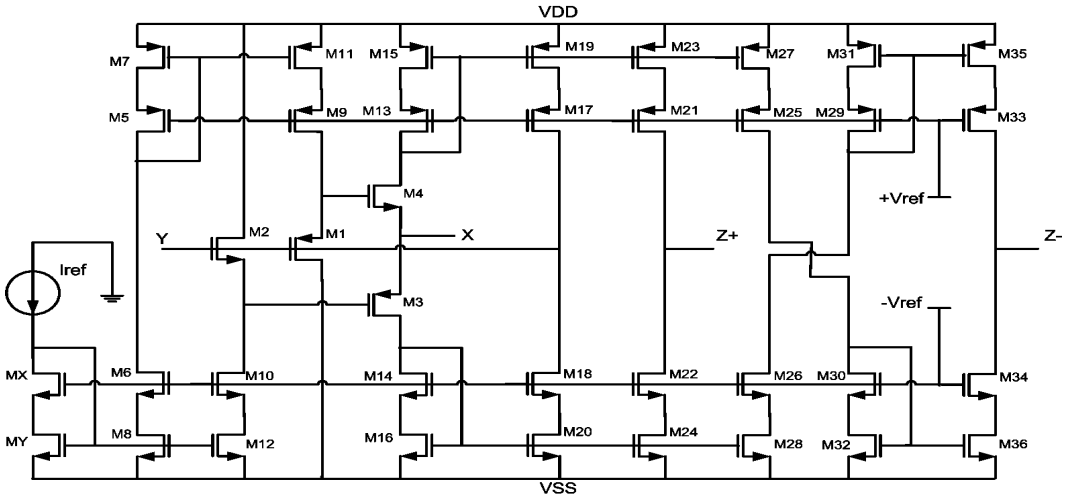


Figure B.5: DOCCI-VFB-LV

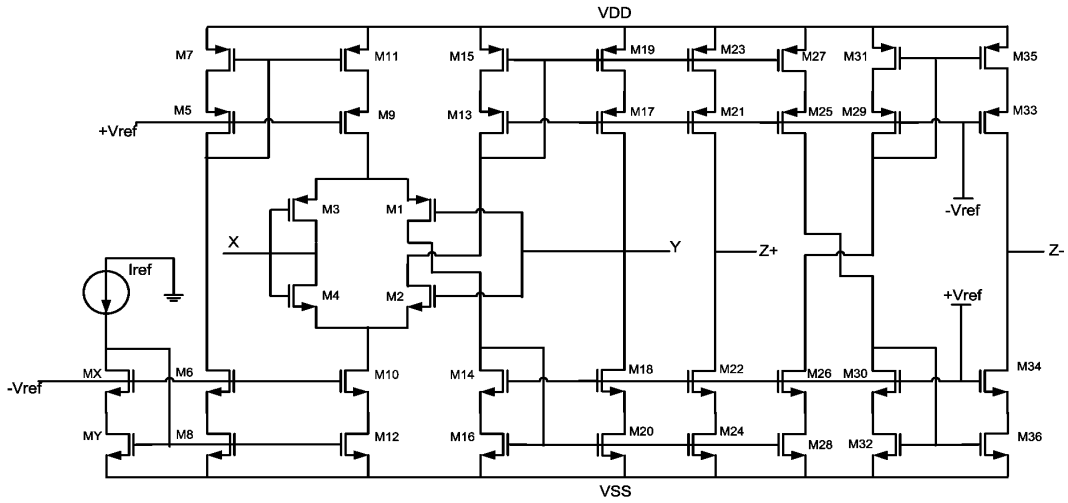


Figure B.6: DOCCI-VFC-LV

B.1.2 CCIIs

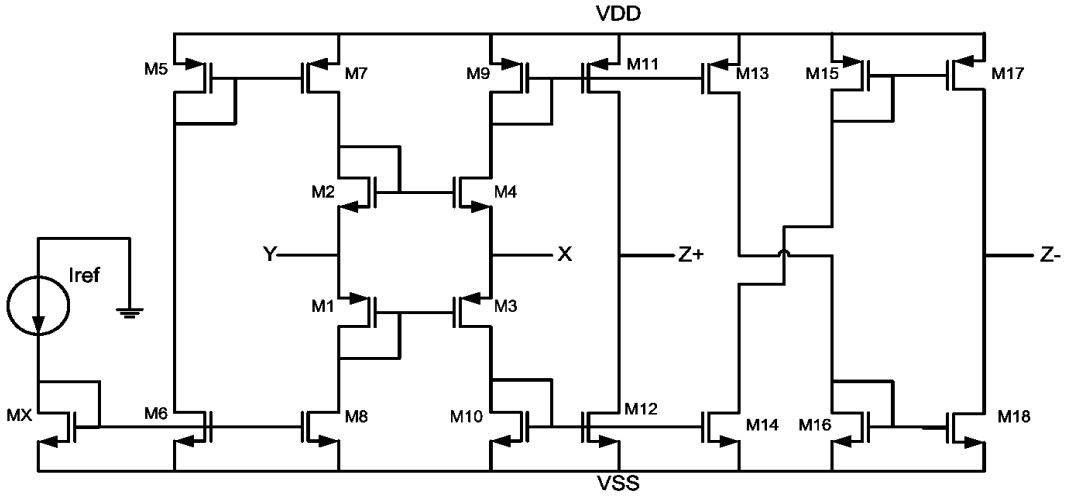


Figure B.7: DOCCII-VFA-S

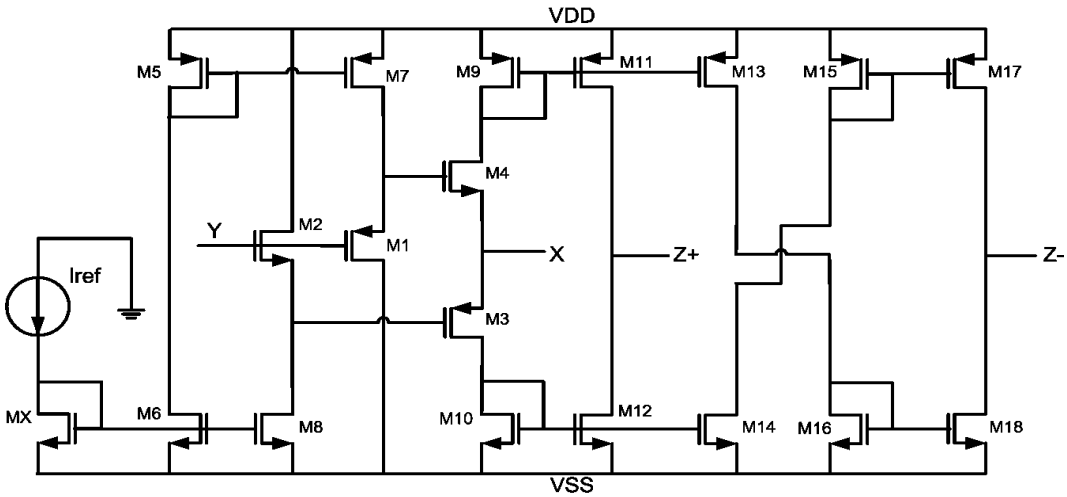


Figure B.8: DOCCII-VFB-S

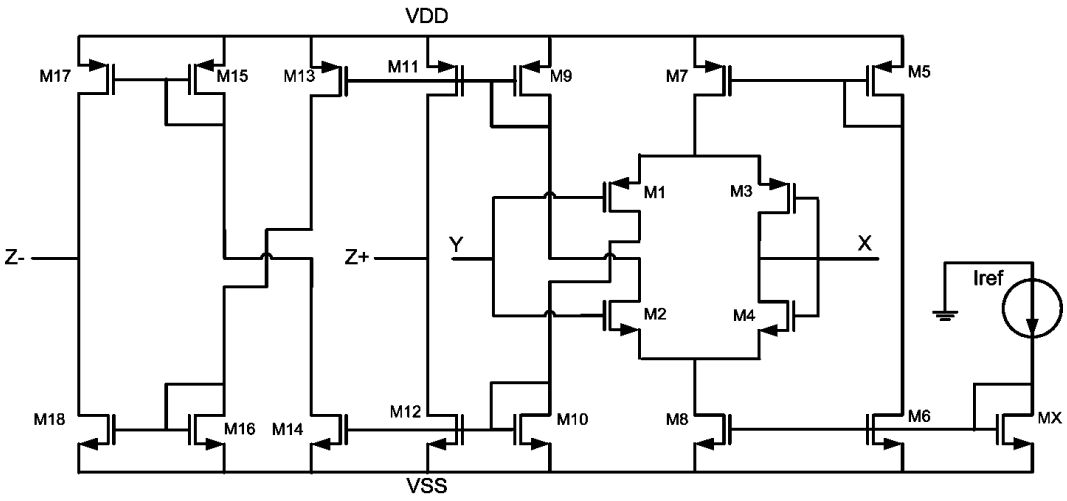


Figure B.9: DOCCII-VFC-S

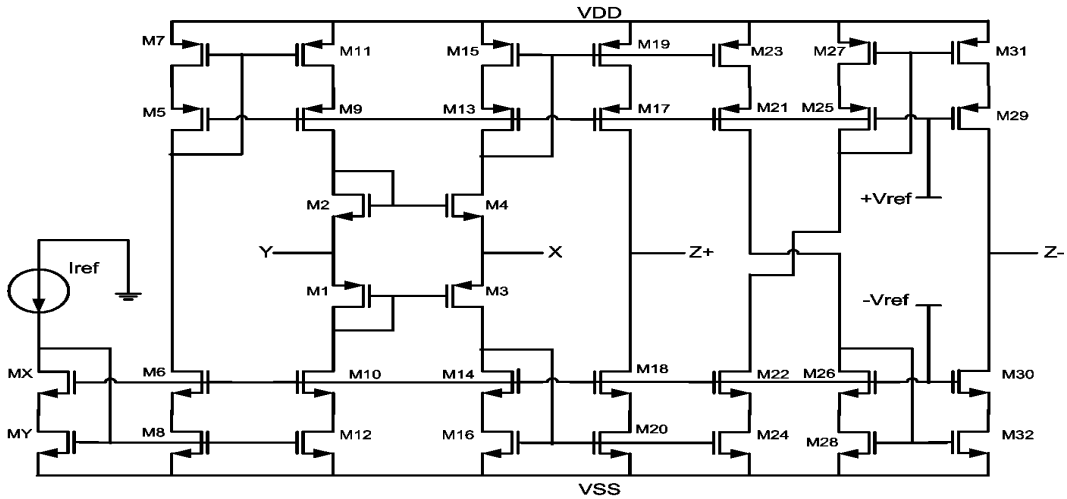


Figure B.10: DOCCII-VFA-LV

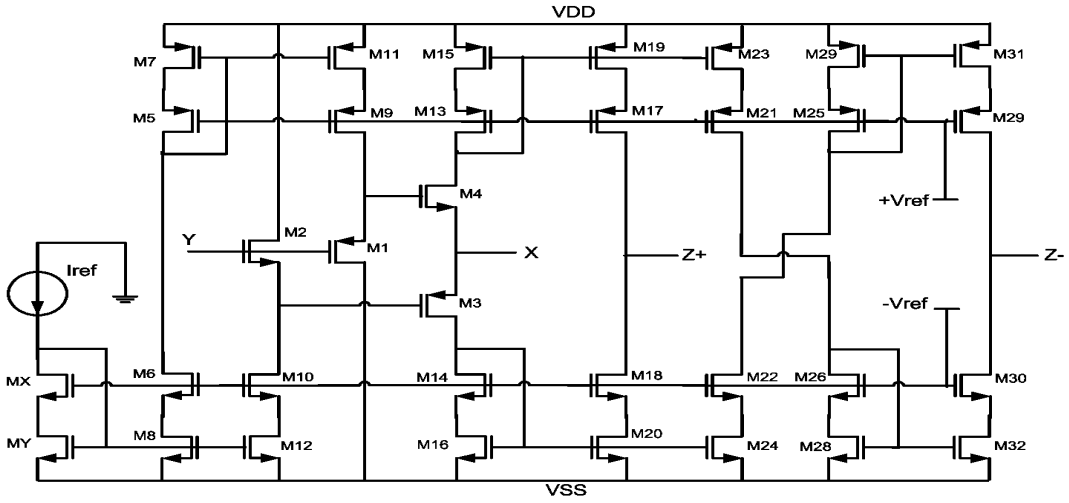


Figure B.11: DOCCII-VFB-LV

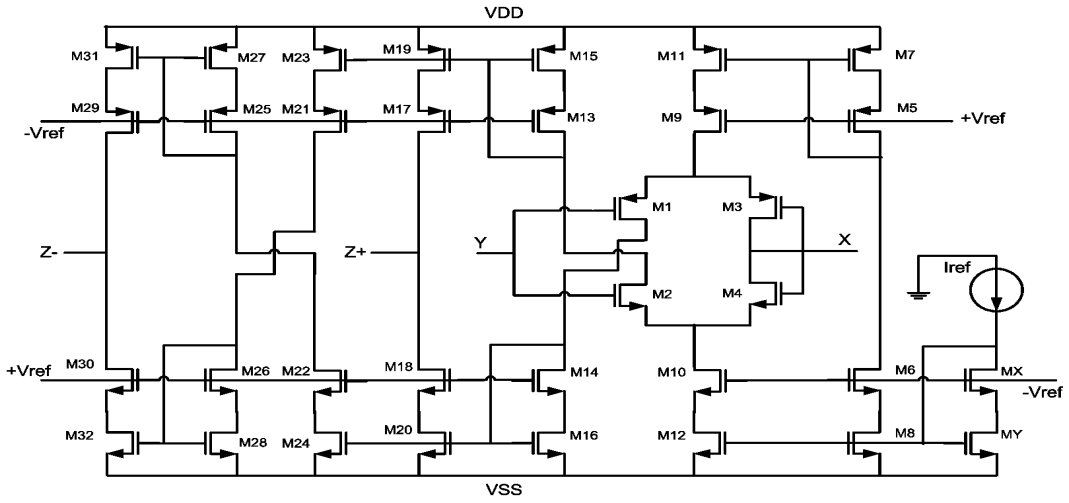


Figure B.12: DOCCII-VFC-LV

B.1.3 CCIIIs

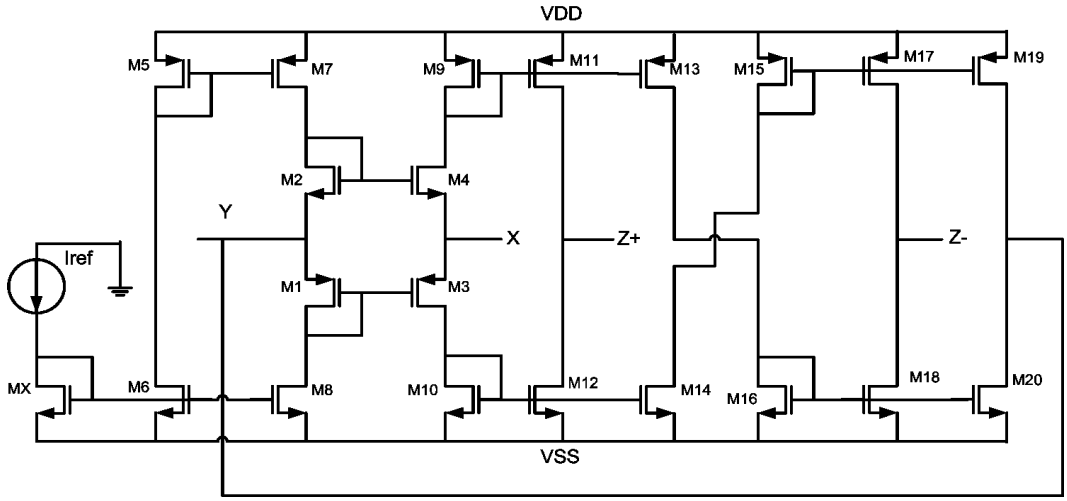


Figure B.13: DOCCIII-VFA-S

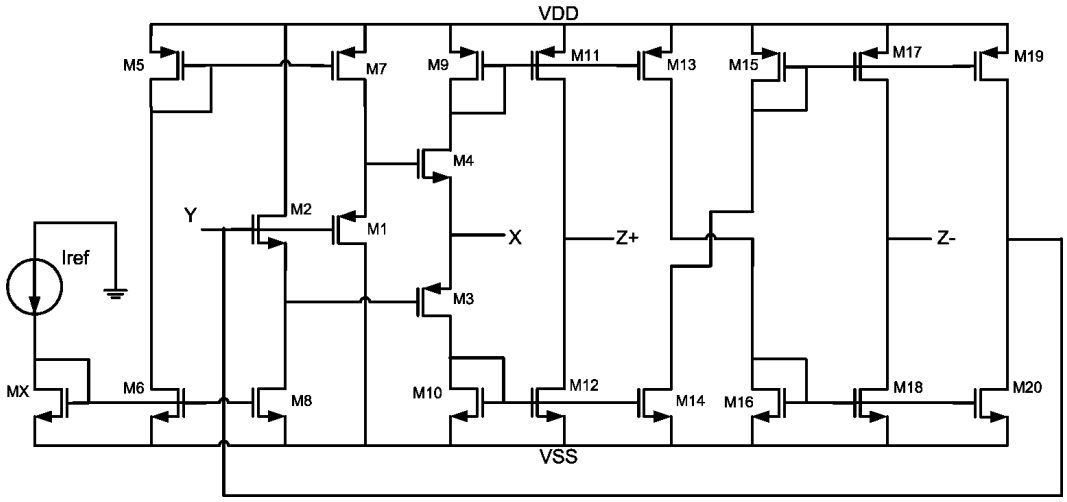


Figure B.14: DOCCIII-VFB-S

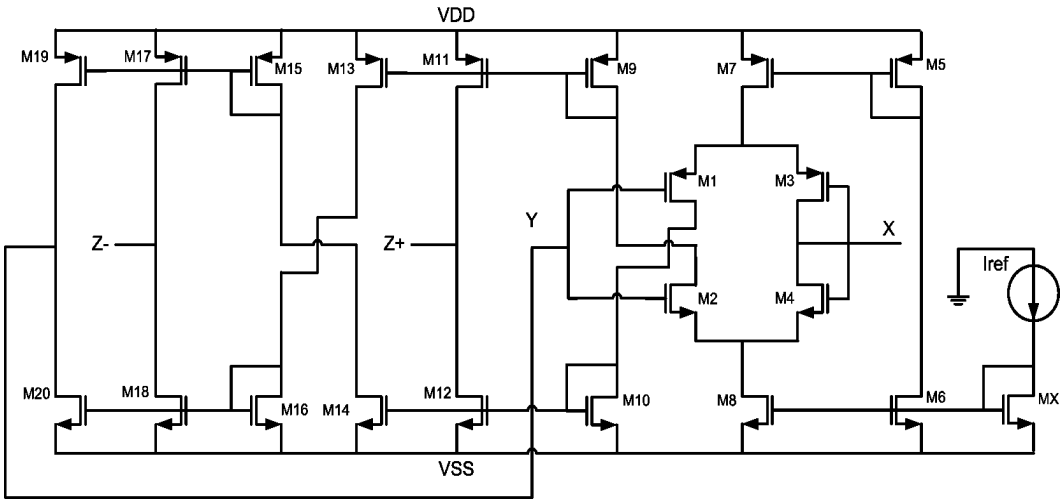


Figure B.15: DOCCIII-VFC-S

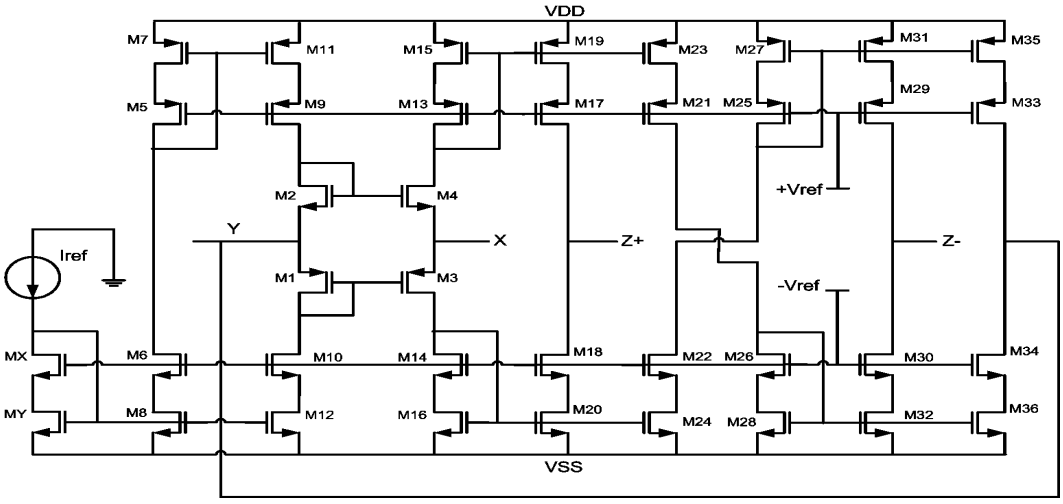


Figure B.16: DOCCIII-VFA-LV

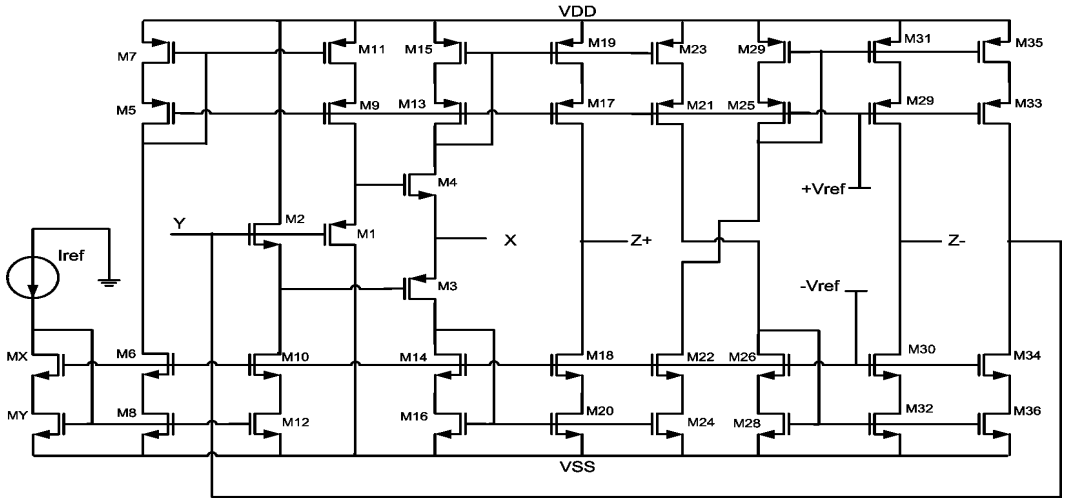


Figure B.17: DOCCIII-VFB-LV

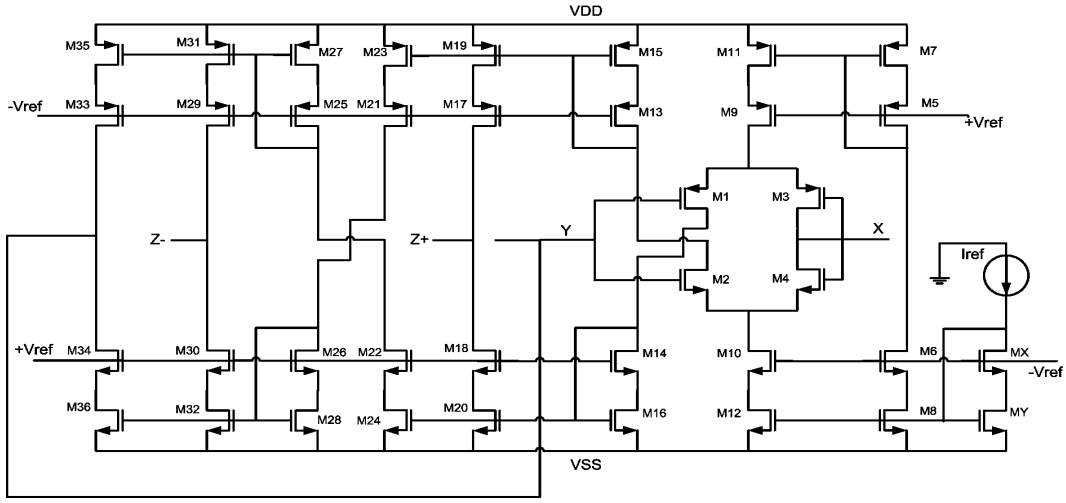


Figure B.18: DOCCIII-VFC-LV

B.2 ICCs

B.2.1 ICCIs

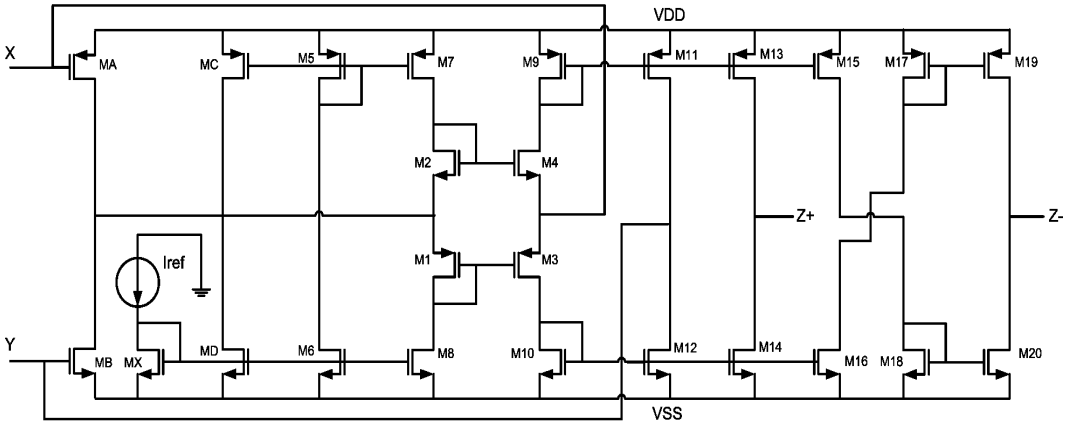


Figure B.19: DOICCI-VMA-S

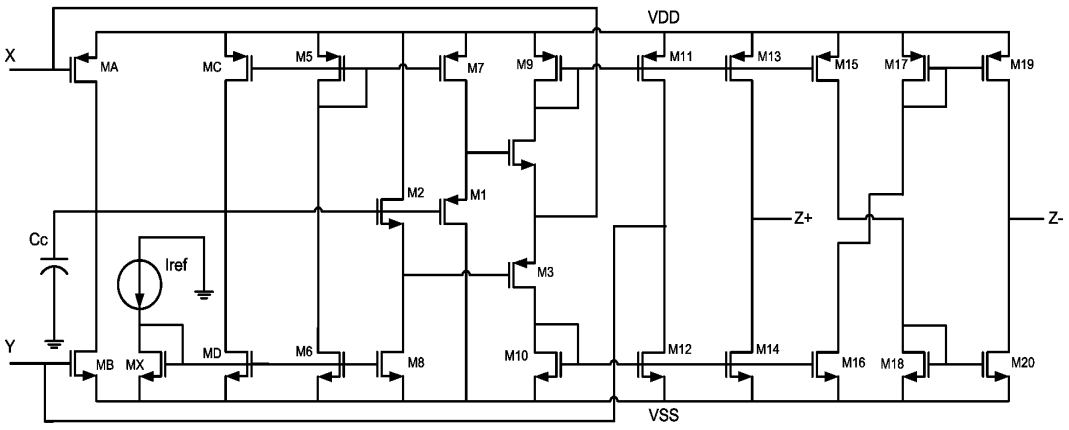


Figure B.20: DOICCI-VMB-S

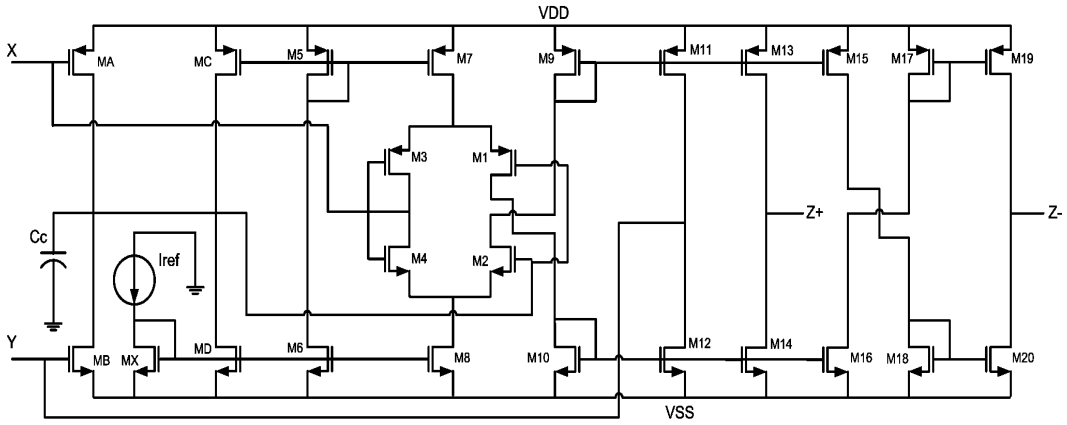


Figure B.21: DOICCI-VMC-S

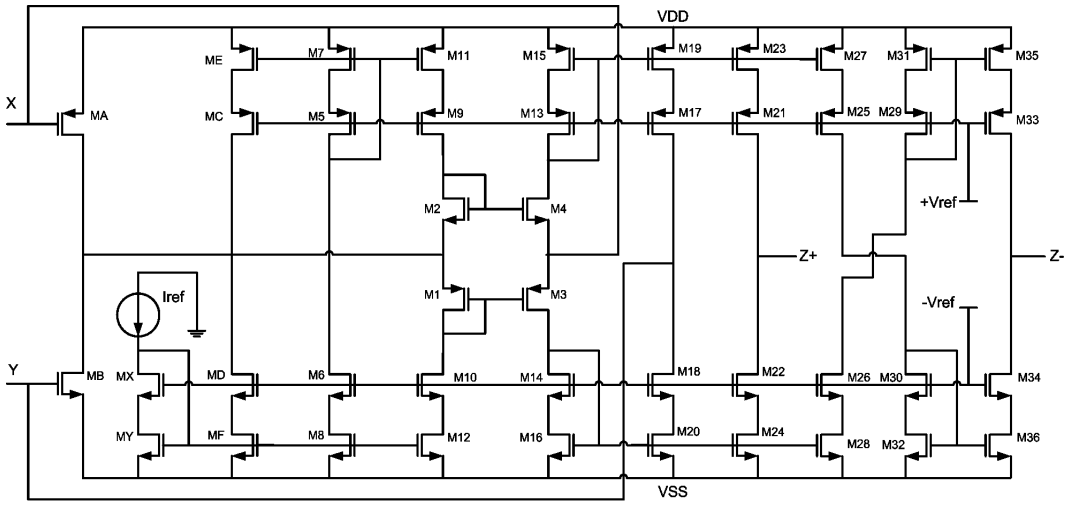


Figure B.22: DOICCI-VMA-LV

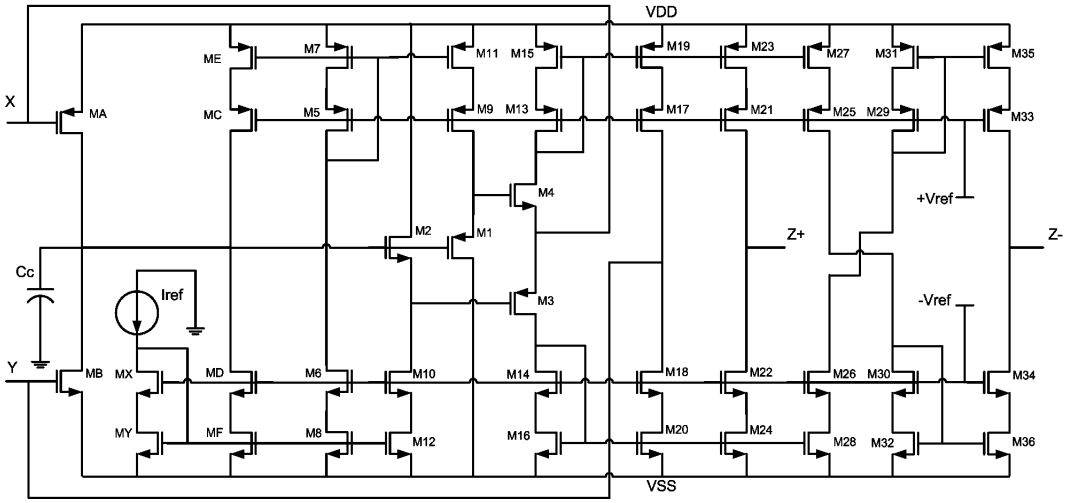


Figure B.23: DOICCI-VMB-LV

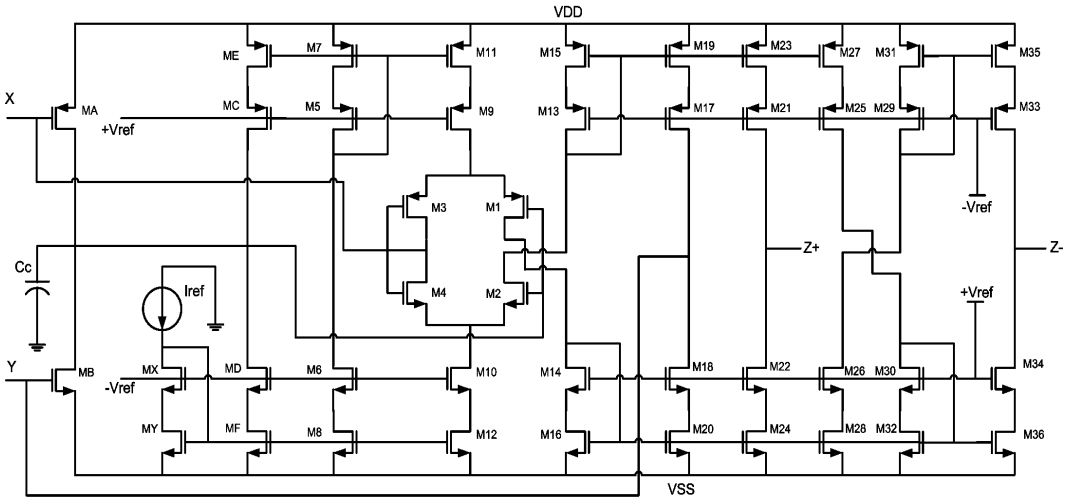


Figure B.24: DOICCI-VMC-LV

B.2.2 ICCIIs

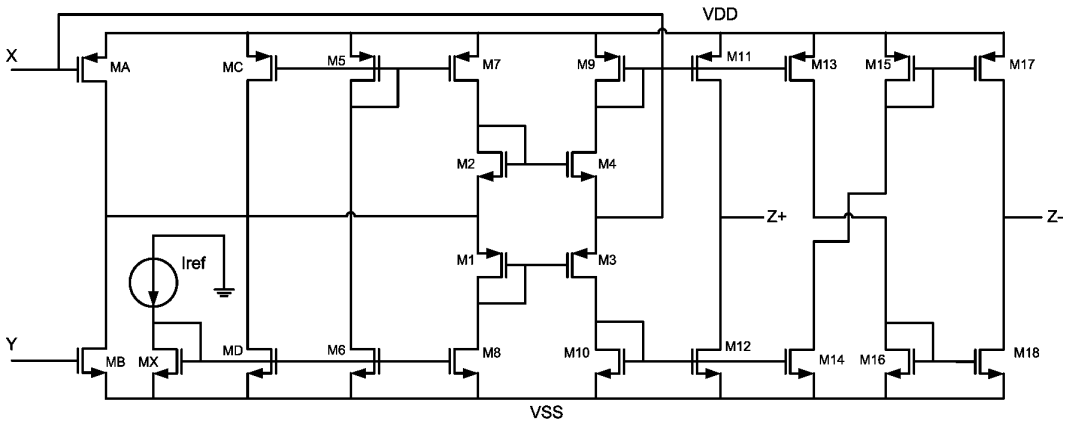


Figure B.25: DOICCII-VMA-S

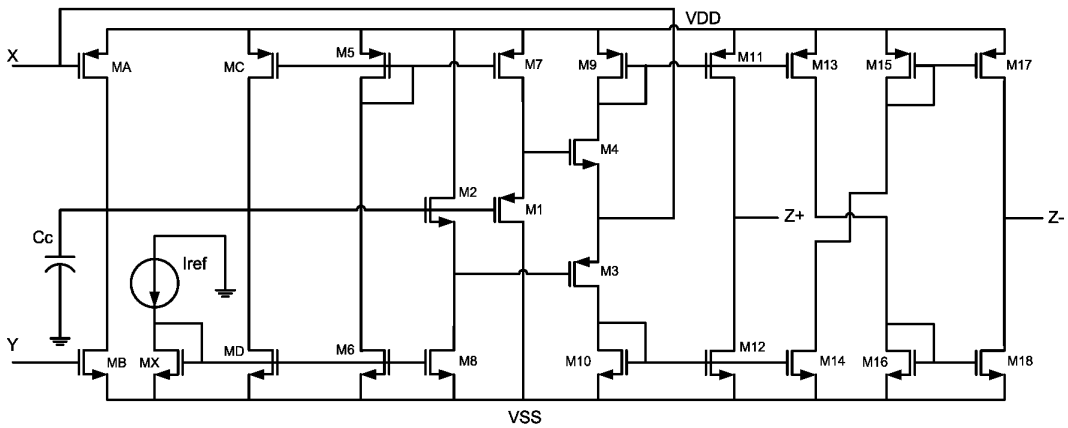
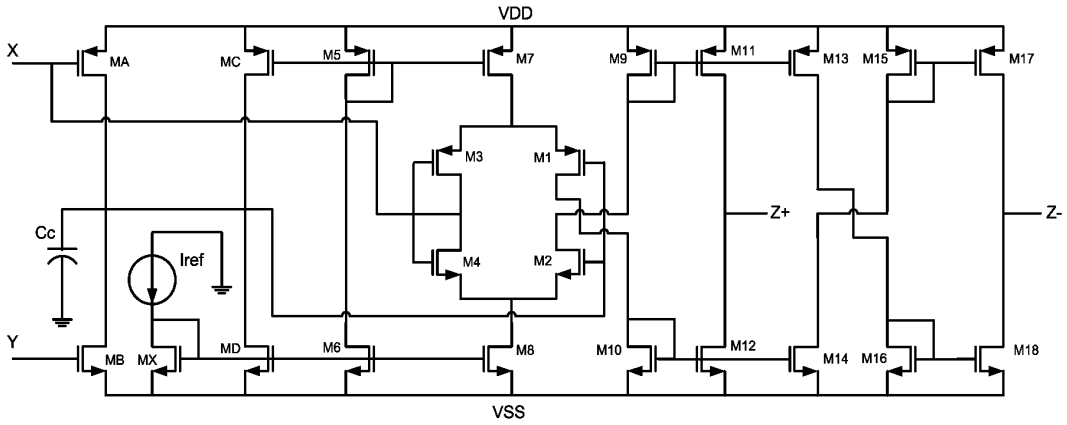


Figure B.26: DOICCII-VMB-S



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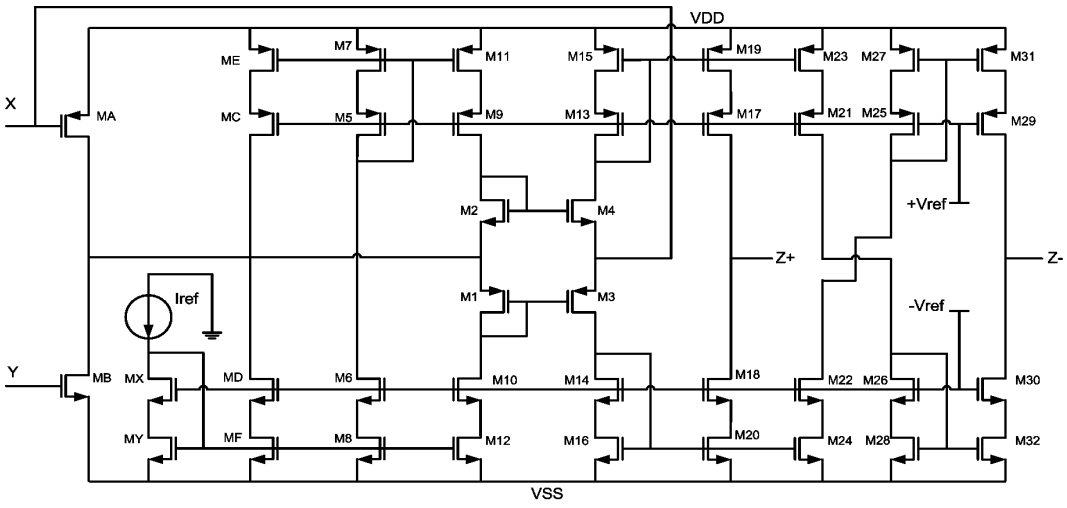


Figure B.28: DOICCII-VMA-LV

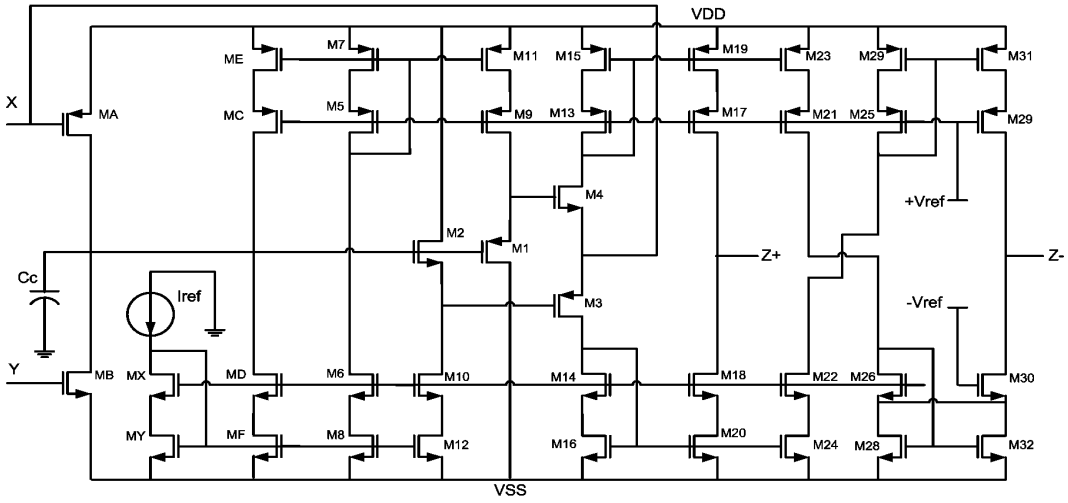


Figure B.29: DOICCII-VMB-LV

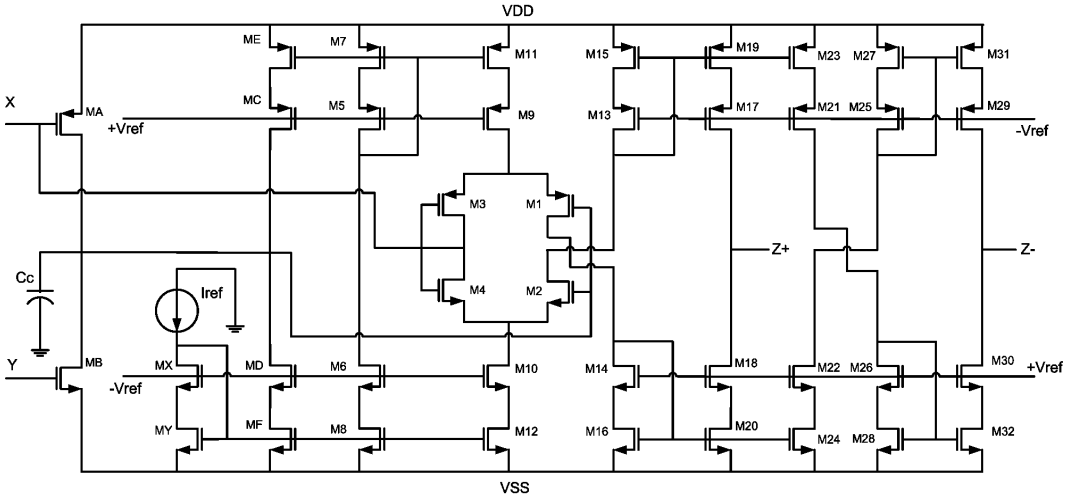
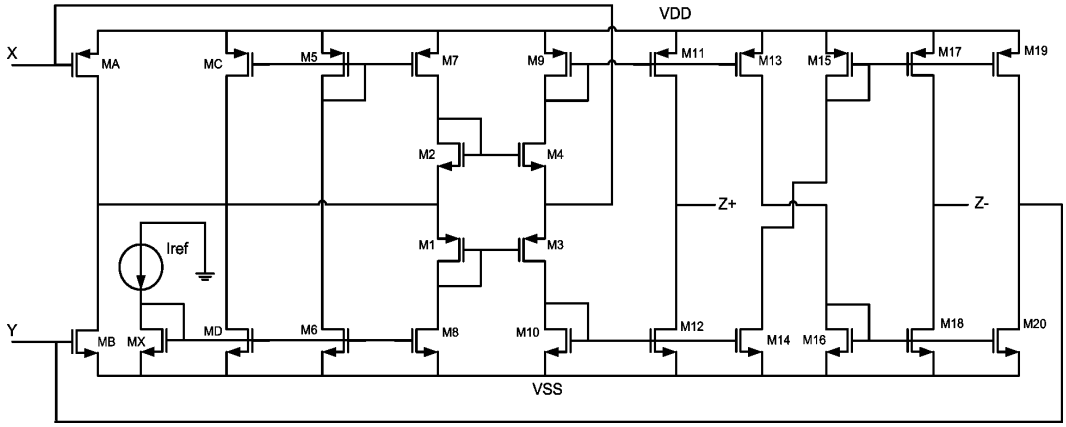


Figure B.30: DOICCII-VMC-LV

B.2.3 ICCIIIs



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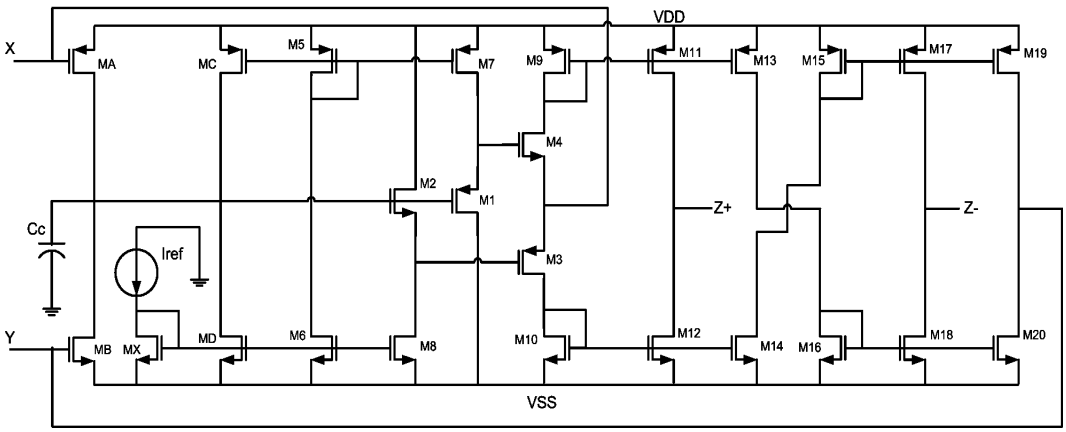

Figure B.32: DOICCIII-VMB-S

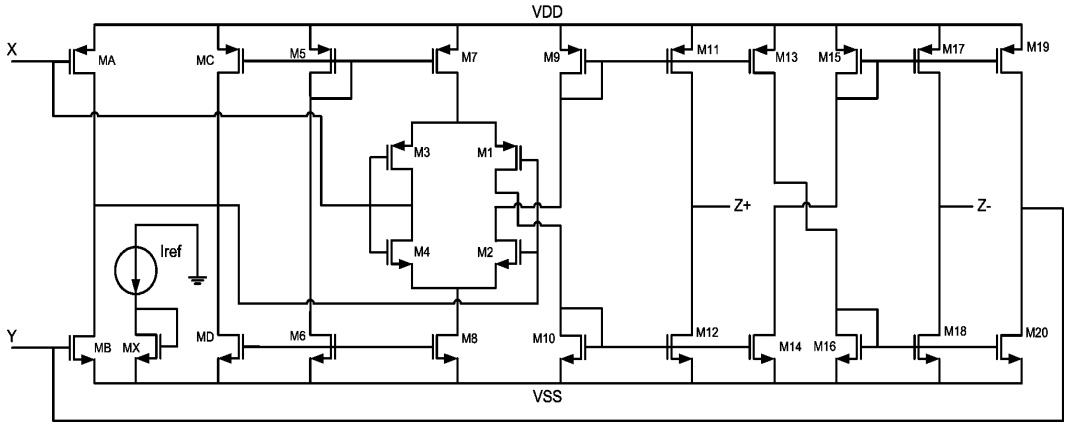

Figure B.33: DOICCIII-VMC-S

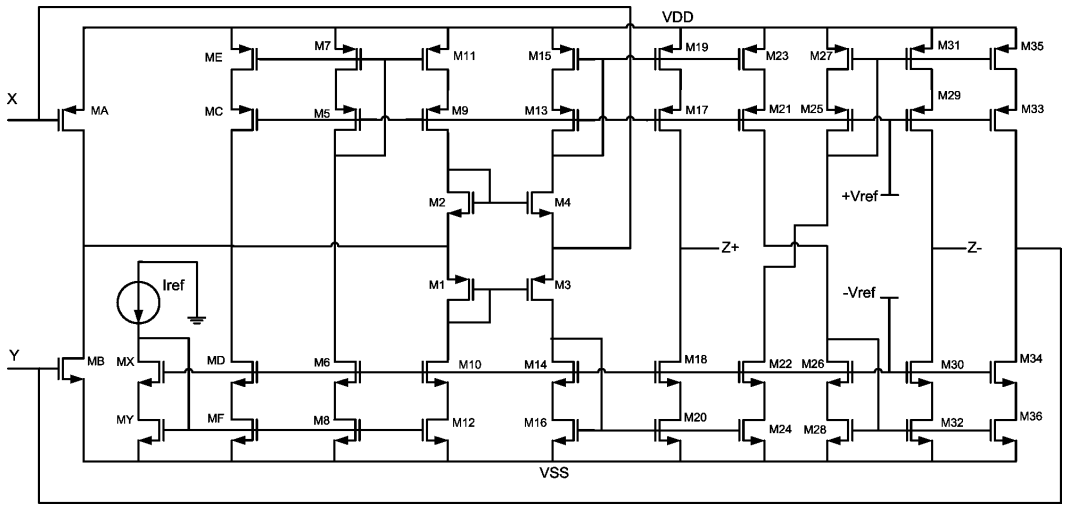

Figure B.34: DOICCIII-VMA-LV

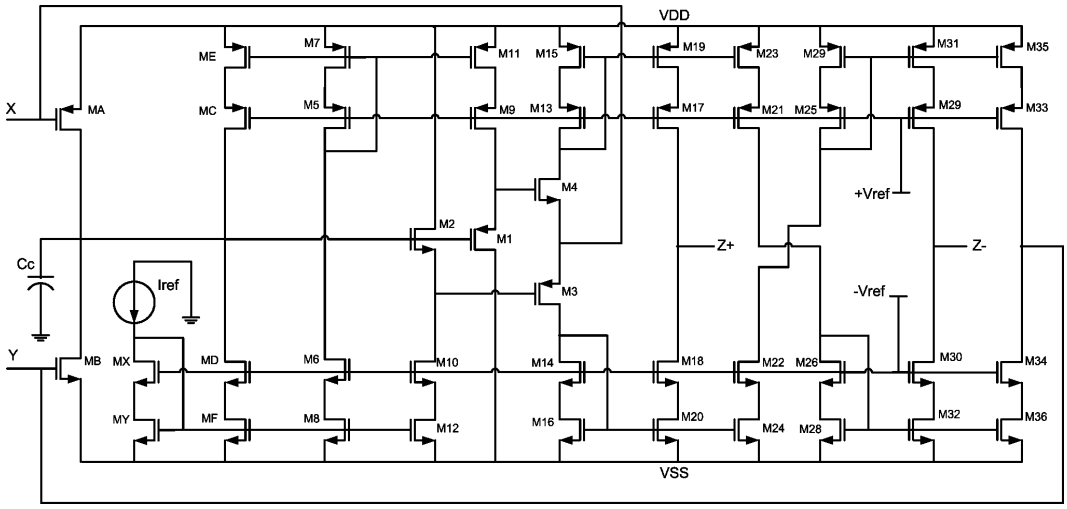

Figure B.35: DOICCIII-VMB-LV

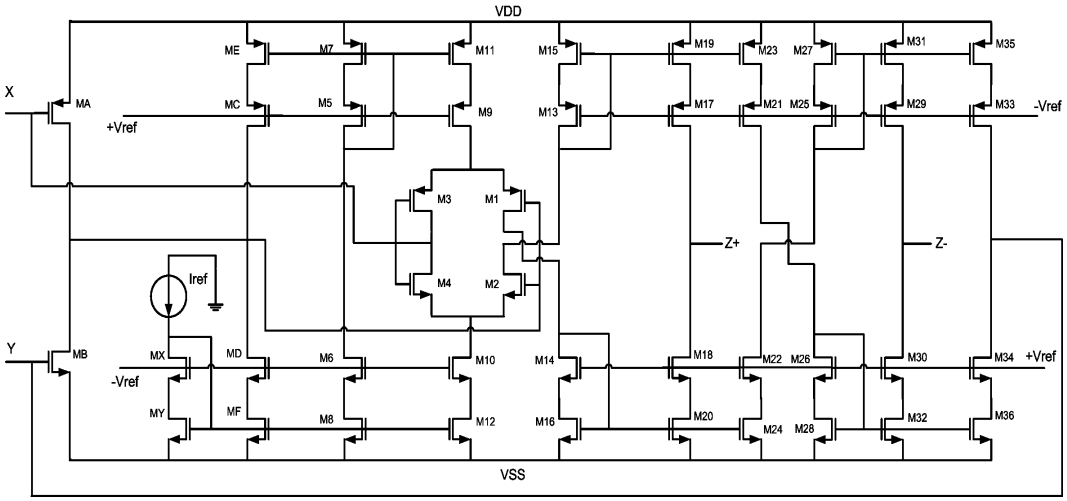

Figure B.36: DOICCIII-VMC-LV

List of Figures

List of Tables

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