Substrate Loss Characterization and Modeling for High Frequency CMOS Applications

by
Emmanuel Torres Rios

M. Sc., INAOE
A Dissertation
Submitted to the Program in Electronics
Electronics Department
in partial fulfillment of the requirements for the degree of

DOCTOR IN ELECTRONICS

at the

National Institute for Astrophysics, Optics and Electronics
November 2008
Tonantzintla, Puebla

Advisors:
Dr. Reydezel Torres Torres
Dr. Edmundo A. Gutiérrez Domínguez
Electronics Department
INAOE

Resumen

Los avances en la tecnología de fabricación de transistores MOS para aplicaciones en sistemas de comunicación en el rango de las micro-ondas, ha sido posible gracias al escalamiento de la longitud de canal. Actualmente, se producen circuitos con transistores de longitud de canal del orden de 45 nm, como es el caso del procesador Core Duo de Intel. El escalamiento de la longitud de canal del transistor MOS a producido una mayor integración de circuitos en un solo encapsulado además de que el dispositivo alcance frecuencias de corte superiores a los 300 GHz. De esta forma, es posible integrar en un mismo encapsulado el sistema de comunicación de radiofrecuencia y el sistema de procesamiento digital de datos. Actualmente, se esta trabajando a nivel investigación en el desarrollo de sistemas de comunicación punto a punto con frecuencias de transmisión de 60 GHz. Para poder desarrollar los circuitos necesarios en el bloque de comunicación es necesario tener modelos precisos y

confiables del transistor MOS que incluyan todos los efectos parásitos asociados al dispositivo cuando trabaja a frecuencias del orden de los 60 GHz.

En esta tesis se describen los principales mecanismos de fuga en el transistor MOS. En específico en este trabajo doctoral se analizan los efectos del tuneleo de banda a banda entre drenaje y substrato, así como la modulación de carga en la región de traslape entre drenaje/fuente y compuerta. Los efectos de tuneleo banda a banda y modulación de la carga en la región de traslape entre drenaje/fuente y compuerta se analizó utilizando mediciones de parámetros S a frecuencias de hasta 50 GHz. Para ello se propusieron metodologías de extracción basadas en los principios físicos de operación de los transistores MOS. Dichas metodologías fueron verificadas en transistores MOS con una longitud de canal de 100 y 65 nm.

Finalmente se presentan los retos para las nuevas generaciones de transistores MOS con una longitud de canal menor a 45 nm. Para transistores con una longitud de canal menor a los 45 nm, los efectos cuánticos son apreciables y determinan la respuesta del dispositivo. Esto implica enormes retos en el diseño, fabricación y modelado del transistor MOS. Es en este punto donde la caracterización y modelado de los transistores MOS usando medición de parámetros S, ha mostrado ser una de las herramientas de medición ideal para el estudio de efectos cuánticos tales como el tuneleo de banda a banda.

Agradecimientos

Durante el desarrollo del trabajo de investigación doctoral, muchas personas me han ayudado de forma directa o indirecta a la conclusión de esta tesis. A ellos les doy mi más sincero agradecimiento y aprovecho estas líneas para expresarles mi gratitud:

- A Dios por brindarme la oportunidad de vivir y darme uno de los regalos más hermosos que hay en el mundo, mi familia.
- A mi esposa "Almendra" y a mis hijos: Alondra, Jonathan y Ana. Sin su amor cariño y comprensión jamás hubiera terminado este trabajo.
- A mi papá Alfonso y a mi mamá Judith por todo su apoyo incondicional a lo largo de mi vida. A las bendiciones de mi mamá Carmelita† que nunca dejo de animarme.
- A mis abuelitos Adelita†, Petrita† y Roberto que siempre me animaron a seguir adelante a pesar de mis tropiezos.

- A mis asesores Dr. Reydezel Torres Torres y Dr. Edmundo Gutiérrez D., por aceptarme como su estudiante doctoral y brindarme su apoyo para la conclusión de este trabajo.
- A el CONACYT por el apoyo económico que me otorgo a través de la beca 166715.
- A Intel por el apoyo económico parcial para la realización del proyecto de investigación.
- A todos los compañeros y amigos del INAOE que me brindaron su amistad durante mi estancia doctoral.

Dedicatoria

"La mujer que amo es un pedazo de cielo en mis manos,

es un rayito caliente de sol que abriga mi alma dormida...

La mujer que amo es un minuto de paz en medio de la más sangrienta guerra,

es la lluvia mojando el suelo reseco de un campo cultivado..."

Anónimo

A mi amada esposa y a mis hijos

Contents

Chapter 1

General Introduction

1.1 The MOSFET as a device for microwave circuit design

In today's world, there is an increasing demand for high-speed electronic systems for applications such as gigabit/s point-to-point links, wireless local area network (WLANs) with extraordinary capacity, and short-range high data capacity wireless personal area networks (WPANs) [1]. This has opened the contiguous bandwidth for unlicensed use in the USA and Japan from 7 GHz to millimeter-wave (mm-wave) frequencies (around 60 GHz) [2]. In consequence, there has been a fast growth in the radio-frequency (RF) wireless communications market [3,4], where high-performance

and low-cost solutions are demanded [5]. One of the most attractive solutions is the integration of a system in a single chip (SOC). In this case, the chip includes the digital data processing circuitries, mixed signal baseband and RF transceiver blocks [6]. Historically, all the circuitry necessary for implementing microwave communication systems have been designed using III-V semiconductor technologies, which is due to the benefits offered by these materials such as high electron mobility and breakdown voltage [7]. Nevertheless, the device fabrication process in III-V semiconductor technology is expensive and is not compatible with complementary metal-oxide-semiconductor (CMOS) processes, where the rest of the circuitry is fabricated. Thus, when RF communication circuitry is designed in III-V semiconductor technology, this block has to be mounted separately over the rest of the circuitry, raising the production and costumer costs [1,2,5].

At the present time, several developments have enabled CMOS circuit blocks to operate at microwave frequencies; then, the RF communication circuitry can be designed in the same die as the rest of the components [8]. The main technological contribution of CMOS device miniaturization is the operation at cut-off frequencies (f_T) up to 150 GHz [7,9]. The miniaturization and the corresponding increase in f_T allow large density integration of RF CMOS communication circuits [9]. Therefore, a complete SOC consisting in communication, data processing and input/output interface blocks can be designed in a single die. This results in a considerable reduction of the production and costumer costs. However, time-to-market and design cycles are also experiencing a reduction [1]. Thus, a design environment to accurately predict the circuit performance using simulations is required [10]. This design

environment consists in part of accurate models for interconnects, active and passive devices (valid under several operation conditions including process, temperature, and stress variations) [11,12]. Hence, for the design of circuits for analog and RF applications, the accuracy of the metal-oxide-semiconductor field effect transistor (MOSFET) models is essential [7]. Thus, device characterization under high-frequency (HF) operation conditions is one of the most important fields of research to improve the MOSFET modeling for this type of applications [13-15].

According to the previous discussion, the study of the MOSFET as a device for microwave applications is mandatory to implement reliable SOC's fabricated in CMOS technology, with the required time-to-market and quality demanded by industry.

1.2 Challenges of MOSFET modeling at microwave frequencies

The continuous downscaling of the MOSFET channel length results in an increase of the operation frequency of the device and in a large integration capacity [7,8]. Nevertheless, as the MOSFET operation frequency increases, some adverse effects that were considered negligible have a negative impact on the device's performance, such as; band-to-band-tunneling, gate-induced-drain-leakage current, drain-induced-barrier-lowering, and others [17-19]. Furthermore, most of the HF effects inherent to the MOSFET behavior are frequency dependent [20-22]. One of these effects is the coupling of the MOSFET terminals through the substrate [23,24]. This undesirable

coupling is due to the low resistivity of the MOSFET substrate. As shown in Fig. 1.1a, the MOSFET substrate can be represented by means of a parasitic impedance located at the bulk terminal. Thus, when the MOSFET operation frequency increases, this impedance represents an alternate conductive path which has associated an uncontrolled parasitic charge flow. Moreover, to improve f_T in a MOSFET, designing the device with specific layout rules is necessary. Unfortunately, most of the advanced layout techniques increase the complexity of an HF MOSFET model that includes the substrate effects [25-28]. This is one of the reasons why, in order to avoid these undesired effects, some variations in the conventional CMOS fabrication process have been proposed. One of the most important proposals is the SOI technology [6,7], where the MOSFET is fabricated over an insulating substrate where the growth of an epitaxial layer to form the active area is required. As can be seen in Fig. 1.1b, an important characteristic of an SOI MOSFET is the lack of the bulk terminal. Notice that this also implies that with this fabrication process, the coupling of terminals through the substrate is reduced and a then high f_T can be achieved. Nonetheless, as a consequence of the lack of a substrate terminal, a floating bulk voltage (V_{bs}) appears originating variations in the threshold voltage (V_{th}). This SOI solution, together with other advances in device engineering such as the elevated source and drain architecture (ES/D) [6] has been widely used in the implementation of RF circuits.

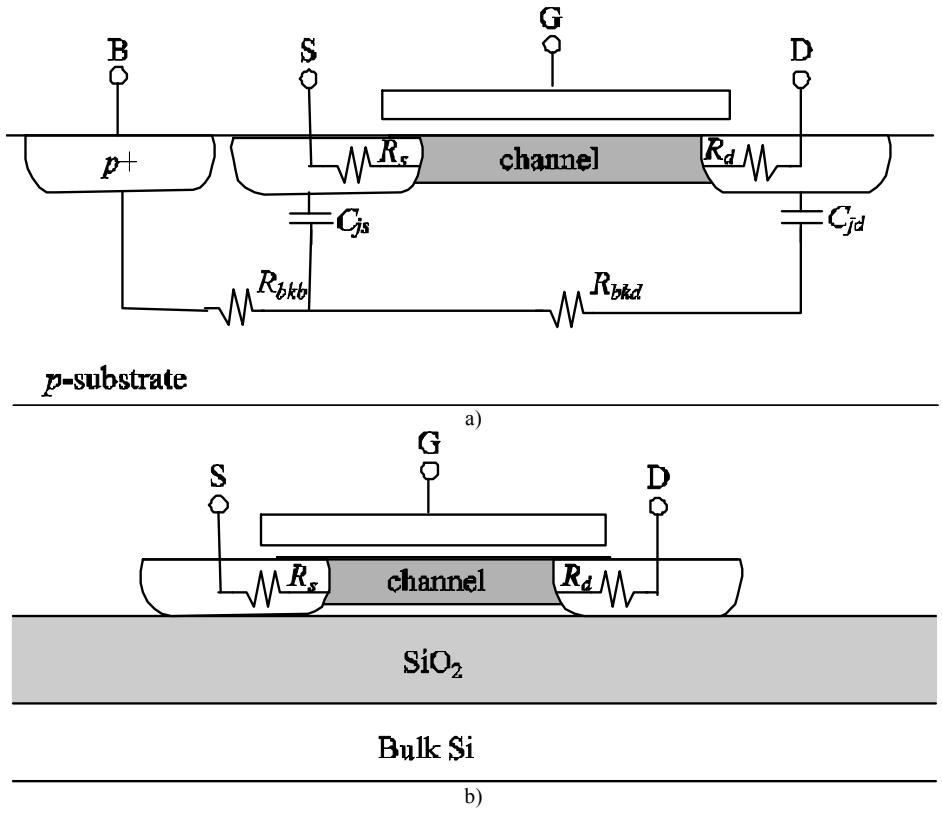
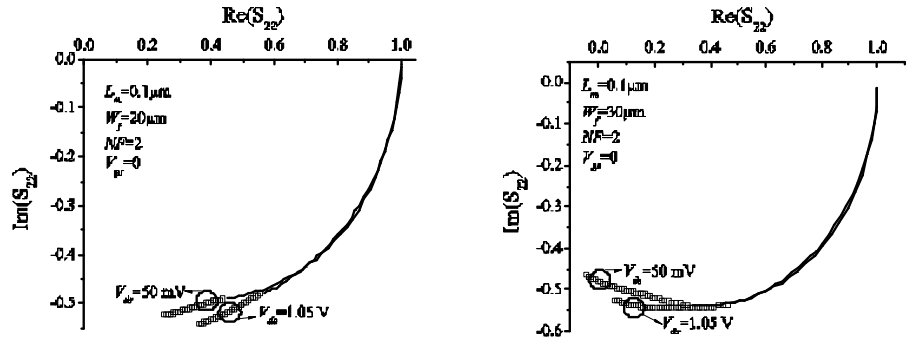


Fig. 1.1: *Cross section view of a) bulk MOSFET, b) SOI MOSFET, showing the principal associated parasitics.*

In recently published literature, the SOI technique is proposed as one of the most accepted solutions to alleviate the problem of substrate coupling. However, the corresponding fluctuation in V_{th} together with the high production cost leads HF circuit designers to prefer conventional CMOS processes. Therefore, some design rules for the MOSFET in CMOS technology are being suggested to obtain the best performance of a CMOS device operating at high frequencies. An example is the multi-fingered gate configuration [25-27], which reduces the effective value of the distributed gate resistance. In this case, however, the fringe capacitance associated with the gate electrode is also increased and new charge leakage paths become apparent. Thus, an exhaustive study of the MOSFET taking into consideration all

these aspects is needed to improve the accurate modeling of the device at high-frequencies for custom applications.



a) b)

Fig. 1.2: *Output bulk MOSFET characteristics of two different transistors of 0.1 μm gate length and a) 20 μm and b) 30 μm channel width from 1 Ghz to 25 GHz. The kink effect is marked in squares*

1.3 Undesirable coupling of the MOSFET terminals

The substrate coupling affects measurable characteristics at each one of the four MOSFET terminals. In the previous section, it was explained that this effect involves non-controlled charge paths from each one of the terminals [29-33]. Nevertheless, not all of the non-controlled charge flows occur at HF. For example, the charge leakage from the gate to the bulk is originated by the very thin thickness of the dielectric material used as gate oxide. Thus, singularities and non-homogeneities occur when the dielectric thickness is reduced, which generates charge leakage [32]. For the case of the coupling between the drain and source terminals, the impedance associated with the substrate determines the non-controlled charge path as the MOSFET when operated at high frequency [34-39]. This is evident in the output characteristics of the

MOSFET at frequencies above 20 GHz, where a kink phenomenon in the measured S_{22} parameter is observed [20] as shown in Fig. 1.2. The kink phenomenon has been analyzed before and it is attributed to the substrate impedance [20,40-42]. In fact, the effect of the frequency dependent substrate impedance and the corresponding correlation with the kink phenomenon has been demonstrated up to 26 GHz in 0.18 μm MOSFETs However, the frequency dependent substrate impedance is not the only mechanism that determines the MOSFET output characteristics. Second order effects that were only considered important at DC, play also an important role as the MOSFET operation frequency goes above 25 GHz in sub-micrometer devices. Among some important second-order effects are the remote surface roughness scattering, mobility degradation, impact ionization, band-to-band tunneling, velocity overshoot, self-heating, channel charge quantization, polysilicon depletion, RF behaviors, NQS effects, and many other. Therefore, since the communication systems working within the microwave band demand that the MOSFET works at HF, a complete study of these second-order effects occurring in the device at any operation frequency and applied bias is necessary.

1.4 Second order effects in a MOSFET at HF

Second order effects are those induced by high vertical and horizontal electric fields [43]. These effects include for example the mobility degradation, bias-dependent series resistance, velocity saturation, effective electrical channel dimensions, etc. The inclusion of second order effects in the MOSFET modeling implies an increment in

the processing time of the device simulation [44]. Therefore, a rigorous analysis to determine the conditions at which the inclusion of certain second order effects is required. Some specific second order effects have a significant impact on the MOSFET characteristics as the technology continues scaling down the channel length, as explained hereafter.

The fabrication of MOSFETs involves the implantation of drain and source

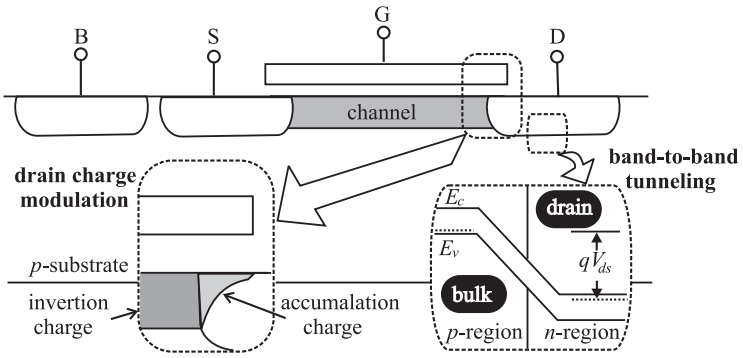


Fig. 1.3: *Sketch illustrating high order effects in a sub-micrometric bulk MOSFET.*

regions. These implantations require an annealing process for the passivation of the substrate, which involves a thermal process that allows the diffusion of dopants under the MOSFET gate. In consequence, as can be seen in Fig. 1.3, the doping under the gate introduces charge that can be modulated by the applied voltage [6,7]. In this case, as the channel length is scaled down, the effect of this modulated charge is more evident. This is because the effective channel length is reduced in comparison to the mask length in sub-micrometric MOSFETs, which introduces a large overlap region under the gate terminal. The main effect associated with this charge modulation is the voltage dependence of the series resistances [45-46]. Several methods to determine the gate-bias-dependent and gate-bias-independent series resistance have been

proposed [47-49]. Nevertheless, these methods do not allow the determination of the drain and source series resistances independently and from measurements performed to a single device. A contribution in this direction was proposed in this thesis.

In addition, in recent years one of the topics of interest in the characterization of second order effects is the direct band-to-band tunneling in the drain-to-bulk junction [50-52]. This is of interest due to the fact that, as the technology continues scaling down, the degradation of the drain and source diffusions present ideal conditions for the tunneling effect to become apparent in the drain-to-bulk junction. This is shown in Fig. 1.3 [43]. Nevertheless, the actual measurement methodologies do not allow quantifying the charge generated by the direct band-to-band tunneling. Therefore, in this work a new measurement technique for evaluating the tunneling current is proposed.

1.5 Purpose of this thesis

The aim of this thesis is to present contributions to the MOSFET modeling at HF including the coupling of MOSFET terminals through the substrate and the band-to-band-tunneling at the drain-bulk junction. As mentioned above, there are several effects associated with the undesired coupling of the MOSFET terminals. These can be classified in two main groups:

1) coupling through substrate, and
2) second order effects.

Hence, in this thesis, a detailed analysis of the second order drain-to-bulk band-to-band tunneling effect is presented. With this purpose, an analytical and methodological extraction procedure for nano-metric MOSFETs under DC and HF operation conditions is presented, as can be seen in Fig. 1.4. To ensure the validity of the measurements under HF conditions, an exhaustive study of parasitics associated to test-fixtures used to probe the devices is presented, which allows assessing the corresponding influence in the parameter extraction methodology. The DC analytical extraction procedure is focused in the measurement of the characteristic curves of the parasitic bipolar transistor associated with the MOSFET intrinsic regions. Thorough a physical-based experimental and theoretical analyses it was observed that a tunneling current originated at the drain junction feeds this parasitic transistor, magnifying the corresponding effect when the MOSFET drives relatively low currents (e.g. when working within the sub-threshold regime). Thus, from the experimental currents of the drain and source terminals obtained in a single MOSFET, it is possible to determine the band-to-band tunneling effect current and the parasitic bipolar gain as well.

For the case of the impact of the parasitic bipolar inherent with the intrinsic MOSFET region, an S-parameter-measurement-based analytical parameter extraction procedure was proposed in this thesis. This allows to obtain the associated conductance of the band-to-band tunneling effect in nano-metric MOSFETs working up to 40 GHz in nanometric MOSFETs. In this case, the extracted conductance shows the intrinsic effect of band-to-band-tunneling at HF. An important point to be remarked is the fact that this HF extraction procedure is based in two-port network S-

parameters measured in a single MOSFET. In contrast, parameter extractions based on regressions of data associated with devices of different lengths lead to a high uncertainty due to the considerable variations of the characteristics of nanometric devices with the geometry. Part of this uncertainty comes from the fact that second-order effects are channel length dependent, which complicates the extraction methodology. Finally, to demonstrate the presence of this phenomenon from DC to high frequencies, a correlation of the extracted band-to-band tunneling effect under DC and HF is presented.

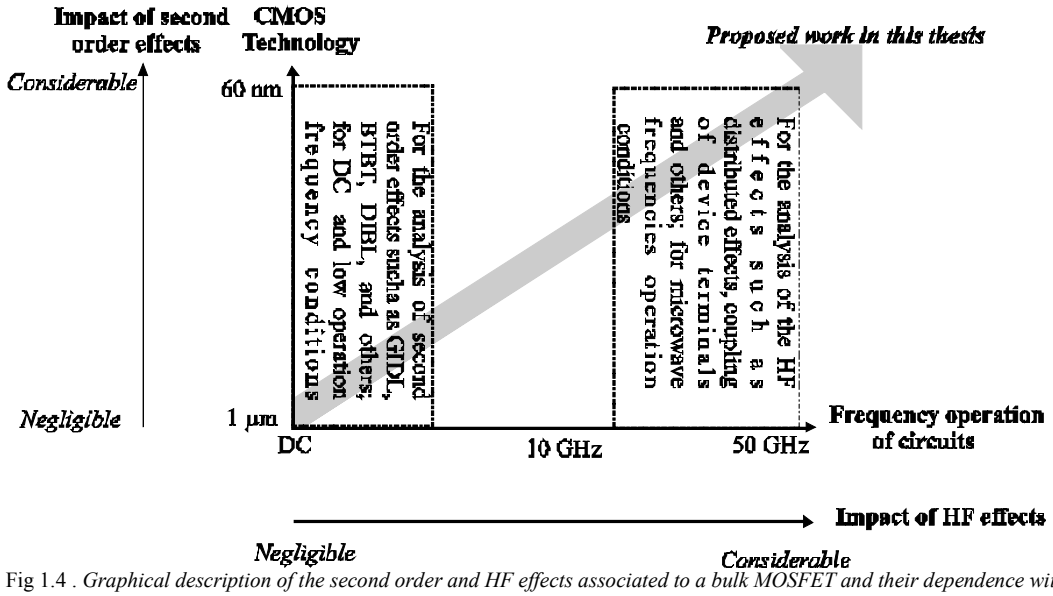


Fig 1.4 . *Graphical description of the second order and HF effects associated to a bulk MOSFET and their dependence with the technology downscaling and frequency operation conditions.*

1.6 Outline

The methodologies used for the analysis of the MOSFET terminals coupling through the substrate under DC and HF conditions, are divided as follows.

In Chapter 2, a complete analytical characterization of HF test fixtures for measuring using coplanar ground-signal-ground probes is presented so that the corresponding impact on the extraction of the model parameters for the device-under-test (DUT) can be assessed. Moreover, the parasitics associated with conventional test fixture of this type are compared with those of a test fixture that includes a shield to avoid the substrate coupling of the pads. The models associated to each one of these popular test fixtures are presented and a discussion about the best option for test structure design is presented.

In Chapter 3 a discussion about the different ways for analyzing the band-to-band tunneling effects using DC measurements in the literature. In addition a proposal to model and characterize the substrate coupling in MOSFETs is presented. In this case, the methodology for the analysis of the band-to-band tunneling effect is based on DC measurements of the current at each of the device terminals under a specific bias condition.

Chapter 4 presents how MOSFET second order effects are analyzed, characterized and modeled using S-parameter measurements. A complete and analytical extraction methodology, which incorporates direct band-to-band tunneling, is presented.

In Chapter 5, a summary and conclusions about the studied topics is presented.

Chapter 2

Characterization of HF Test Structures

2.1 Introduction

The increasing demand for high data transmission rates, bandwidth, data processing and transmission frequency requires the improvement of circuits and systems at the lowest cost [53]. Therefore, many types of high frequency devices have to be modeled and characterized at microwave frequencies [54-56]. This means that accurate measurements are needed to design a high-performance radiofrequency integrated circuit (RFIC) at a reduced cost. This is the reason why on-wafer S-parameter measurements are of great importance in the semiconductor device

industry. In this case, the device under test (DUT) is interconnected to the measurement probes by means of a test fixture. Since this test fixture is intended for measuring purposes (i.e. it will not be included in the actual RFIC), its effect has to be removed from the S-parameter measurement using a de-embedding technique. In this case, the de-embedding technique is considered as a two-tier calibration that moves the measurement reference plane from the probe tips to the DUT to be characterized [57]. In order to remove the effect of the test structure from the experimental S-parameter measurements, several methods have been developed [58-61]. These methods, however, do not allow the identification of the impact of the test fixture parasitic components on the DUT experimental data. This is due to the fact that a de-embedding algorithm is formulated to remove the undesired effects, but the physical origin of these effects is usually ignored, complicating the identification of the dominant parasitics and the possible optimization of the test fixture.

Due to the considerable high parasitic effects introduced by test fixtures at the frequencies at which the characterization of the devices is currently required, the optimization of the test fixtures has recently become an important topic. In fact, alternative test structures have been specifically designed to reduce the parasitic effects associated with the undesired pad coupling through the substrate [57]. These are called “ground-shielded test fixtures” [62,63]. This type of structures, however, introduces a high capacitance that may be comparable to the input impedance of the DUT within the GHz range [61]. In consequence, an optimization process — supported by a physically based modeling and characterization methodology— is also required.

Hereafter, a physical model for the parasitic effects associated with RF test structures fabricated on CMOS technology is presented. The proposed model is applied to an improved shielded test structure, where the pad design for measuring probes is two metal levels above the ground plane. For the parasitic components parameter extraction a de-embedding procedure which uses only two standards to reduce the space needed for this type of structures is used. The results obtained from shielded test structures are compared with the improved layout design. The extracted parameter values are validated with experimental data up to 50 GHz.

2.2 Description of fabricated test structures

On-wafer measurement of S-parameters is the preferred choice to carry out the characterization of semiconductor devices at high-frequencies. In our case, ground-signal-ground (GSG) configured probes were used due to their good confinement of the electric field. In fact, the distribution of the electric field in a GSG-configured test structure is similar to that of a coplanar waveguide. In Fig. 2.1a, the conventional test structure to probe a DUT with a GSG probe configuration is shown. As can be seen in this figure, the pads are formed in the first metal level (the closest to the substrate). In the cross sectional view of the structure shown in Fig. 2.1b, it is observed that there is a coupling between the signal and the ground pads through the substrate. Hence, a parasitic capacitance appears due to the distribution of the electric field lines in the pad corners, and a lossy network is introduced by the low resistivity substrate. The

model for a conventional test structure is presented in Fig. 2.1c, where the shunt admittances (Y_i and Y_o) represent the coupling of the signal and ground pads. In order to overcome the problem associated with this parasitic substrate path, ground shielded structures have been proposed. In this case, as shown in Fig. 2.2a, the first metal layer above the substrate is used as a ground plane to prevent the coupling of the signal and ground pads through the substrate. As can be observed, the ground plane is extended in every direction under the signal pad to prevent the capacitive coupling between the pads and the substrate. Therefore, the electric field is confined between the ground plane and the probe pads, as shown in Fig. 2.2b. A window at the centre of the ground plane is designed (DUT gap) to allow the interconnection of the pads with the DUT [62,63]. A model for a shielded test structure is presented in Fig. 2.2c. Notice that in this model the shunt admittances Y_i and Y_o represent the capacitance between the pads and the ground shield since the pad-to-substrate coupling effect is negligible. This capacitance, however, may present a considerable higher value when compared with that associated with a conventional test structure [61], as shown in Fig. 2.3.

A simple solution to reduce the effect of the pad capacitance in shielded test structures is the design of the probe measurements pads on the second metal level above the ground plane. As shown in Fig. 2.4, the use of an upper metal level increases the distance between the pad and the ground plane, reducing the shunt capacitance. Nevertheless, additional parasitic effects become apparent as the distance between the pad and the DUT increases. For this reason, the impact of the pad layout on two different metal levels by means of a simple but rigorous methodology is explained in the following sections.

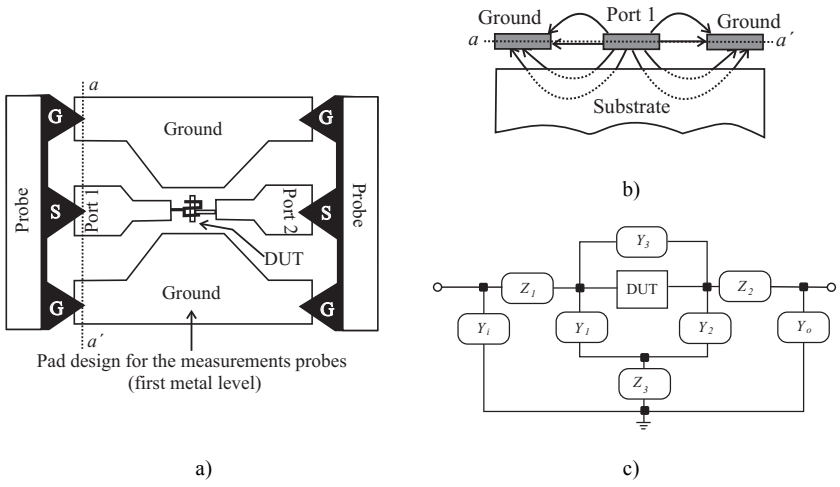


Fig. 2.1: *a) Layout for the pads of a conventional test structure, used to connect the measuring probes with the DUT. b) Cross sectional view (from a to a´) showing the distribution of the electric field. c) Parasitic effects associated with the conventional test structure.*

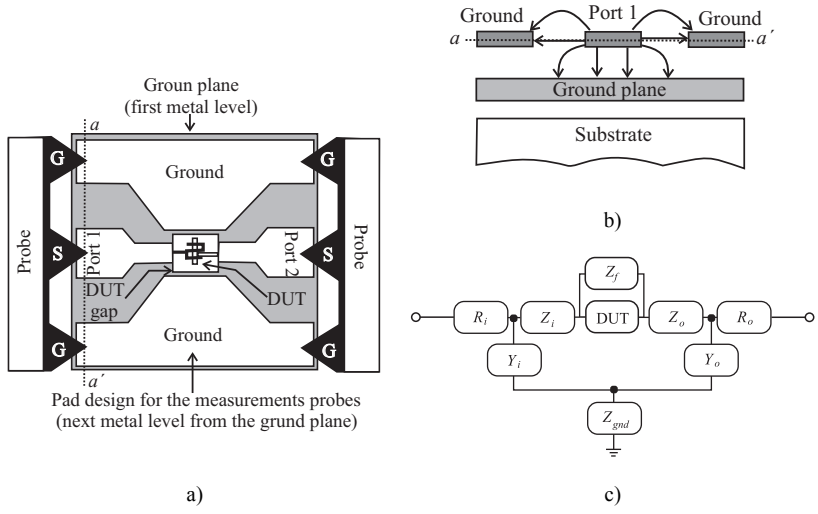


Fig. 2.2: *a) Layout for the pads of a shielded test structure, used to connect the measuring probes with the DUT. b) Cross sectional view (from a to a´) showing the distribution of the electric field. c) Parasitic effects associated with the shielded test structure.*

2.3 General models for RF test structures

Several models have been proposed to determine the effects introduced by the pads and interconnection lines surrounding the DUT in a shielded test structure. All previously proposed models are based on the model of Koolen *et al*. [58], with some simplifications in order to reduce equation complexity, considering the frequency range of interest. In order to apply the model for higher operation frequencies, more elements need to be added. Nevertheless, to make the shielded test structures a standard for on-wafer high frequency measurements, new layout techniques have to be developed to reduce the associated parasitic effects, and better models have to be proposed. A model for shielded test structures in which the pad for probe measuring is located on different metal levels, is presented and compared to that of the conventional structure.

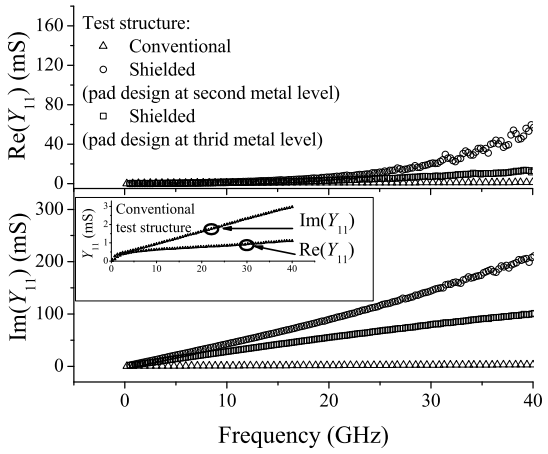


Fig. 2.3: *Y_{11} parameter of conventional, shielded with pad design at second and third metal layer is showed.*

2.3.1 *General model for conventional test structures*

This is the most employed test structure because of its design and fabrication simplicity. The general model for this type of structures is presented in Fig. 2.1c. The eight parasitics elements of the equivalent circuit model have to be extracted by means of an analytical methodology to obtain physical values. Then, each of the eight parasitics is associated with an equivalent circuit model. The equivalent circuit is not simple and the parameter extraction is tedious and complicated by means of the large number of elements to be calculated. The analytical extraction methodology for the conventional test structure associated parasitics is presented in [61]. Nevertheless, the shunt elements associated with coupling of terminals through substrate are smaller compared with MOSFET parasitic capacitance. This is an important aspect when is determined the values of the associated parasitics input/output MOSFET capacitances.

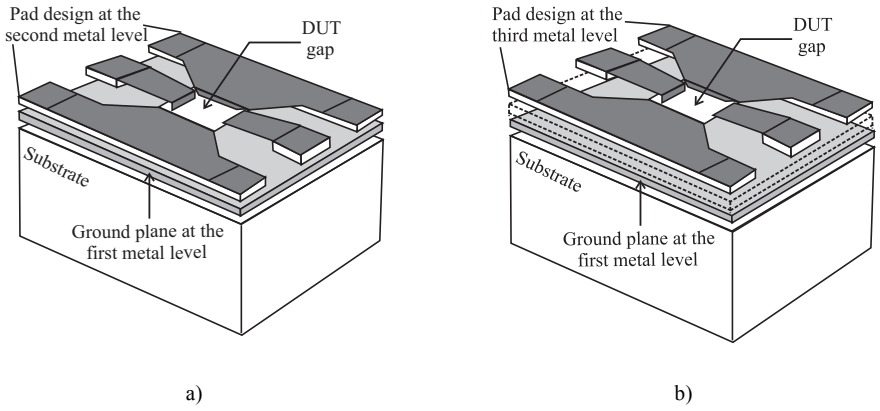


Fig. 2.4*: a) Conventional shielded test structure pad design. b) Improved shielded test structure pad design, where an upper metal level is used.*

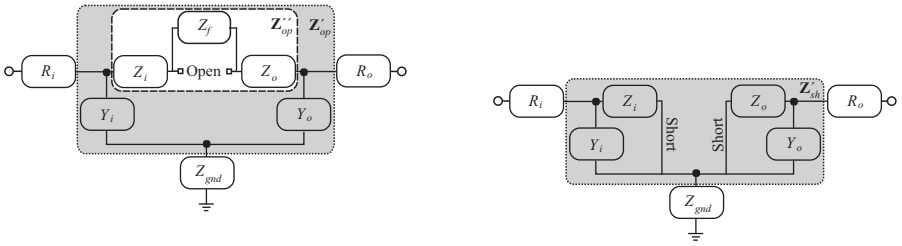
2.3.2 *General model for the shielded test structure with pad probe design at the second metal level*

This is the most employed pad design because of its simplicity, as shown in Fig. 2.4a. The proposed model for this type of shielded test structure is that shown in Fig. 2.2c. As can be seen in this figure, the proposed model takes into account the ground impedance (Z_{gnd}) and the through impedance (Z_f) associated with the pad coupling through air. These parasitic elements had generally been neglected in previous models, since they only become important at frequencies above 20 GHz [63].

This type of shielded test structure pad design presents several advantages, such as simple modeling and parameter extraction, and the elimination of the pad coupling through the substrate. Nevertheless, the high pad capacitance has a considerable value in comparison with the conventional test structure without ground shield.

2.3.3 *General model for the shielded test structure with pad probe design at the third metal level*

In order to optimize a shielded test structure, the reduction of the shunt capacitance is necessary. A simple solution to this problem is the use of a metal layer two levels above the ground plane. As can be seen in Fig. 2.4b, using upper metal levels increases the distance between the pads and the ground shield, which allows reducing the pad capacitance. However, some resistive elements become apparent as a result of the vias needed to connect the higher metal level to the DUT. These elements are considered in the model of Fig. 2.2c by means of the series impedances Z_i and Z_o, which will be explained with more detail in the next section. Once the parasitic elements of the shielded structure have been identified, an equivalent circuit can be



a) b)

Fig. 2.5: *Equivalent circuits associated with the a) open ($\mathbf{Z}_{op}$) and b) short ($\mathbf{Z}_{sh}$) dummy structures.*

associated with each impedance and admittance in the model. Furthermore, we explain in the next section the determination of the model parameters from experimental data.

2.4 Equivalent circuit modeling

2.4.1 *Calculation of the model parameters*

To determine the eight parameters associated to the proposed model in Fig. 2.2c, the S-parameter measurements of the open and short dummy structures are used. The parasitics associated to open and short dummies are shown in Fig. 2.5. Then, from the short dummy, the measured S-parameters are converted in Z-parameters represented by the 2x2 matrix $\mathbf{Z}_{sh}$. Thus, the following parameters can be extracted from operations on the elements of $\mathbf{Z}_{sh}$:

$$R_i \approx \mathrm{Re}\left(Z_{11sh} - Z_{21sh}\right)\Big|_{LF} \tag{2.1}$$

$$R_o \approx \mathrm{Re}\left(Z_{22sh} - Z_{21sh}\right)\Big|_{LF} \tag{2.2}$$

$$Z_{gnd} = Z_{21sh} \tag{2.3}$$

where the subscript *LF* indicates that this approximation is valid at relatively low frequencies at which the reactive components associated with the elements of $\mathbf{Z}_{sh}$ are negligible.

This follows because the structure under analysis is symmetrical and can be transformed in a T-network. Under this condition and in accordance with the model of Fig. 2.5, Z_{gnd}, R_i and R_o can be removed from the measured data using simple algebraic operations; mathematically:

$$\mathbf{Z}'_{sh} = \mathbf{Z}_{sh} - \begin{pmatrix} R_i & Z_{gnd} \\ Z_{gnd} & R_o \end{pmatrix}. \tag{2.4}$$

A similar equation can be written for the model for the open dummy shown in Fig. 2.5a; this is:

$$\mathbf{Z}'_{op} = \mathbf{Z}_{op} - \begin{pmatrix} R_i & Z_{gnd} \\ Z_{gnd} & R_o \end{pmatrix}. \tag{2.5}$$

Upon transforming (2.5) to Y-parameters and inspecting Fig. 2.5a, the input and output port admittances are determined as:

$$Y_i = Y'_{11op} + Y'_{21op}. \tag{2.6}$$

$$Y_o = Y'_{22op} + Y'_{21op}. \tag{2.7}$$

Once Y_i and Y_o are known, their effect is removed from $\mathbf{Y}'_{op}$ using:

$$\mathbf{Y}''_{op} = \begin{pmatrix} Y'_{11op} & Y'_{12op} \\ Y'_{21op} & Y'_{22op} \end{pmatrix} - \begin{pmatrix} Y_i & 0 \\ 0 & Y_o \end{pmatrix}. \tag{2.8}$$

Then, Z_i and Z_o can be extracted from the measurements using:

$$Z_i^{'} = \frac{1}{\frac{1}{Z_{11sh}^{'}} - Y_i} \tag{2.9}$$

$$Z_o^{'} = \frac{1}{\frac{1}{Z_{22sh}^{'}} - Y_o} \tag{2.10}$$

Finally, Z_f is calculated from:

$$Z_f = \frac{1}{Y_{21op}^{''}} - Z_i - Z_o \,. \tag{2.11}$$

2.4.2 *Analytical parameter extraction*

In the model for a shielded test structure R_i and R_o represent purely resistive elements since they are inherent to the sheet resistance of the pad metal layer and contact resistance. This is the reason why these resistances are determined by means of the expressions (2.1) and (2.2). As shown in Fig. 2.6a, there exist considerable differences between the extracted values for R_i and R_o according to which metal layer is used to form the pads. Fig. 2.6a also shows the data corresponding to Z_{21sh}; as can be seen, this parameter is associated with a pure inductance. Thus, Z_{gnd} can be modeled by means of a lumped inductor. Furthermore, this figure shows that Z_{21sh} presents the same trend for the two different shielded structures; this is because the same metal level is used for the ground shield. Therefore, the value of the ground inductance can be determined from:

$$L_{gnd} = \frac{\mathrm{Im}(Z_{21sh})}{\omega} \,. \tag{2.12}$$

Also notice from Fig 2.6b, that the trend of Y_i and Y_o indicates that these parameters are not purely capacitive. An appropriate equivalent circuit for these parasitic elements is a capacitor (C_p) in series with a resistance (R_p). Their values can be extracted from Re($Y_{i,o}$) (which indicates that the procedure is applicable to Y_i and Y_o) by using:

$$\frac{1}{\mathrm{Re}(Y_{i,o})} = \frac{1}{\omega^2 C_p{}^2 R_p} + R_p \,. \tag{2.13}$$

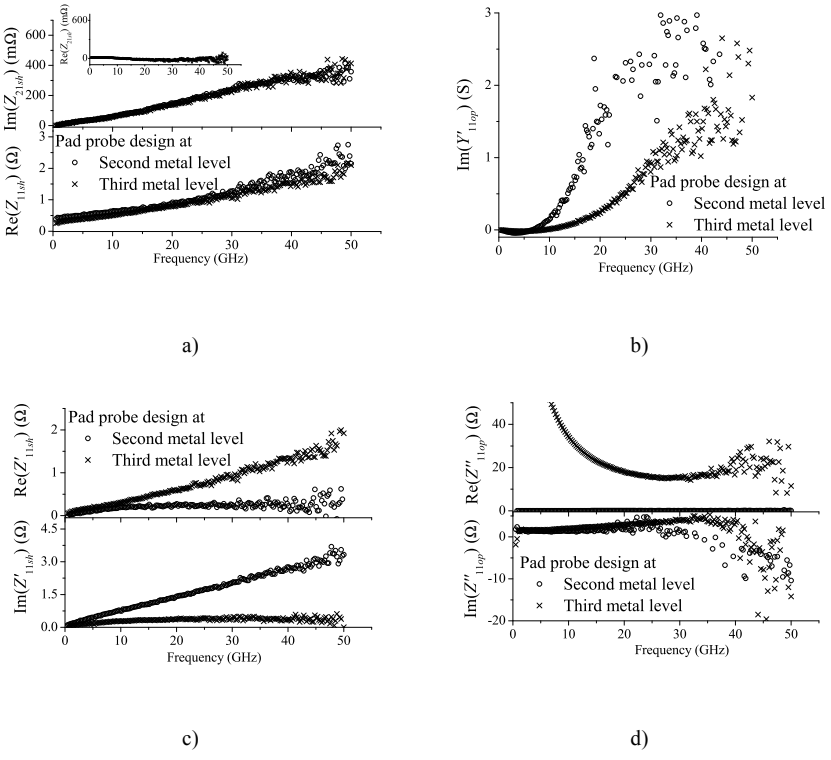


Fig. 2.6: *In these figures the frequency behavior of the parasitic elements of shielded test structure, where the probe pad is designed in the second and third metal layer, are presented.*

Hence, from the linear regression of $1/\mathrm{Re}(Y_{i,o})$ versus $1/\omega^2$, R_p can be determined from the intercept with the abscises (b), and C_p can then be determined from the slope (m):

$$C_p = \sqrt{\frac{1}{mR_p^{\,2}}}\,. \tag{2.14}$$

At this point, it is necessary to point out the fact that C_p and R_p present different values depending on the parameter they are associated with, either Y_i or Y_o.

For Z_i and Z_o two solutions are possible. The first one is when the pad metal layer is located on the metal level immediately above the ground plane. In this case, a pure inductive effect is observed, as is shown in Fig. 2.6c. It then follows that the inductance value can be determined from:

$$L_i = \frac{\mathrm{Im}(Z_{i,o})}{\omega}\,. \tag{2.15}$$

When an upper metal level is used, $Z_{i,o}$ are no longer purely inductive elements, as can be seen in Fig. 2.6c. A better model is that of an inductor (L_i) in parallel with a resistor (R_z). The values for these elements can be calculated from:

$$\frac{\omega}{\mathrm{Im}(Z_{i,o})} = \frac{\omega^2 L_i}{R_z} + \frac{1}{L_i}\,. \tag{2.16}$$

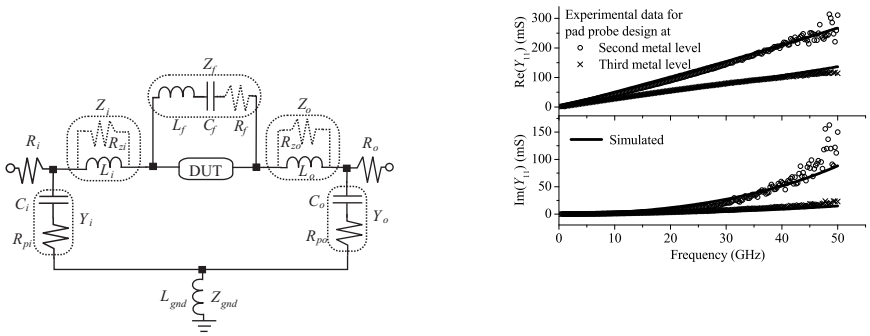
In this case, a linear regression of $\omega/\mathrm{Im}(Z_{i,o})$ versus ω^2 is employed to find the intercept with the abscises (b) and the slope (m). Therefore, $1/L_i$ is determined from b while R_z is determined from m using:

$$R_z = \frac{L_i}{m}. \tag{2.17}$$

Finally, likewise in the case for $Z_{i,o}$, Z_f has a different trend when plotted versus frequency when an upper metal level for the pad design is used, as shown in Fig. 2.6d. As can be seen, when the probe pad is at the metal level next to the ground plane, a pure LC effect is observed. When a higher metal level is used, however, the contribution of a series resistance is needed to model the curves. The values for L_f and C_f in both cases are obtained from the linear regression of:

$$\omega \,\mathrm{Im}(Z_f) = -\frac{1}{C_f} + \omega^2 L_f. \tag{2.18}$$

Then, $-1/C_f$ is obtained from the intercept with abscises, whereas L_f is obtained from the corresponding slope. In the case of R_f for the structure that uses a higher metal level, the extraction is performed from the value of Re(Z_f) at low frequencies,



a) b)

Fig. 2.7: *a) Complete equivalent circuit model for the shielded pad design. The solid lines represent the model for conventional structures, and the dotted lines the elements that have to be added to improve the model for the test structure. b) Comparison between the simulated and experimental data of the real and imaginary parts of parameter Z_{11} for the open dummy, up to 50 GHz.*

where the effect of L_f is negligible.

2.5 Results and discussion

The complete equivalent circuit model for the shielded test structure is presented in Fig. 2.7a. To validate the values obtained using the proposed analytical extraction methodology, in Fig. 2.7b we show a comparison between the simulated and experimental data of the real and imaginary parts of Z_{11} of the open dummy up to 50 GHz. As can be observed in Fig. 2.7b, the proposed model agrees very well with the experimental data. The advantages of using higher metal levels to reduce the input/output shunt capacitance is corroborated, but with the cost of introducing new resistive elements in the equivalent circuit model. The new resistive elements are caused by metal thickness differences in each layer, and the use of deep vias to connect the DUT to the pad. Moreover, even though one would expect Z_f be the same for both cases, experimental data show that this is not the case. As explained above, the metal characteristics of upper levels are not the same (mainly the metal thickness), and thus the pad coupling through air varies according to which layer is used.

The results presented in this experiment show a trade off between the reduction of the input/output shunt capacitance and the parasitic resistive elements. It is clear that more experiments are needed in order to determine the best metal level for pad design, where the optimum shunt capacitance and parasitic resistance values are obtained.

2.6 Conclusions

An accurate model and an analytical parameter extraction methodology for the parasitics associated with a RF shielded test structure fabricated in a CMOS technology have been presented and demonstrated up to 50 GHz. The pad parasitics distribution is proposed, and a simple de-embedding method is based on the use of only two dummy structures is employed. The experimental results show a compromise in the reduction of the shunt input/output capacitance and the appearance of parasitic resistances, when using different metal levels for the pad design.

The proposed equivalent circuit model is shown to be accurate within the measuring range, allowing the proper representation of the parallel and series parasitic components. All of these can be assigned to the physical aspects of the structure, giving the designer insight into the structure, needed to optimize layout techniques in order to reduce undesirable effects on the DUT.

Chapter 3

Modeling of the Band-to-Band Tunneling in Bulk MOSFET's

3.1 Introduction

Minimization of the off-state leakage current is an important issue in high-density, battery powered CMOS technologies [1]-[3]. With the downscaling of MOSFET's channel length and oxide thickness, the effect of the charge leakage mechanism that was neglected for micrometric devices becomes relevant in nanometric technologies. This is the case of the band-to-band tunneling effect (BTBT) in the MOSFET drain-to-bulk junction. The BTBT charge leakage generates a parasitic current in the intrinsic MOSFET bulk. The magnitude of the parasitic current is not noticeable in comparison with drain current at the strong inversion condition. However, the magnitude of this parasitic current is high enough to turn on the parasitic bipolar transistor (pBJT) formed between the intrinsic source, bulk, and drain nodes of the

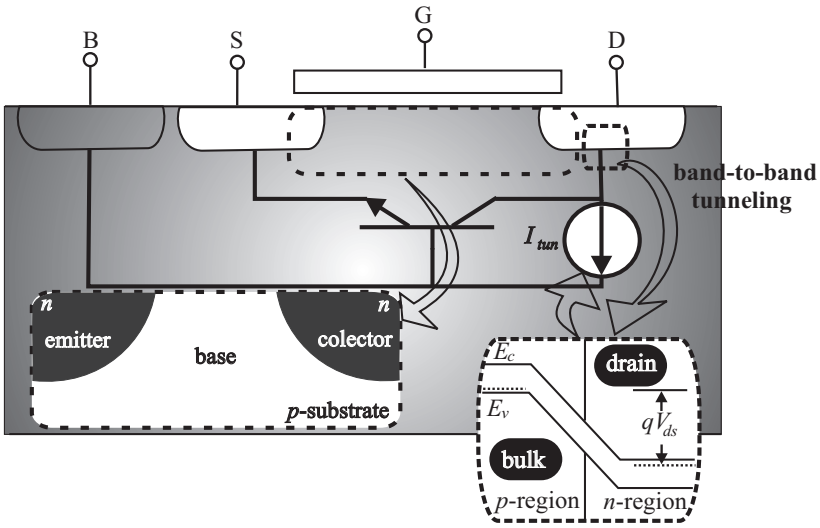


Fig. 3.1. Model for the MOSFET biased at V_{gs}=0 V and V_{ds}>0 V showing the different currents associated with the structure.

MOSFET. This is an undesired effect since the parasitic current associated to the BTBT charge leakage is amplified by the pBJT, which sets a high off-state leakage current flowing from the drain to the source of the MOSFET [43, 44, 50]. Moreover, according to our experimental results [70], this leakage current increases as the channel length decreases. This is because the current gain (β) of the pBJT increases as the base width (given by the channel length) is reduced.

To prove the existence of the BTBT effect, we present measured results of the leakage current generated by the pBJT for bulk MOSFETs with channel lengths (L_m) of 50, 60, and 70 nm, and a channel width (W_T) of 2 μm. These measurements were taken at room temperature at V_{gs}=0 V and V_{bs}=0, 20, 40, 60, 80, 100, 120 mV. Furthermore, an analytical methodology for the extraction of the pBJT gain is presented to carry out a thorough qualitative analysis of the tunneling current effects. Furthermore, the BTBT effect in the drain-to-bulk junction is demonstrated by

comparing the experimental data with a model previously reported by Y. Taur *et al* [43].

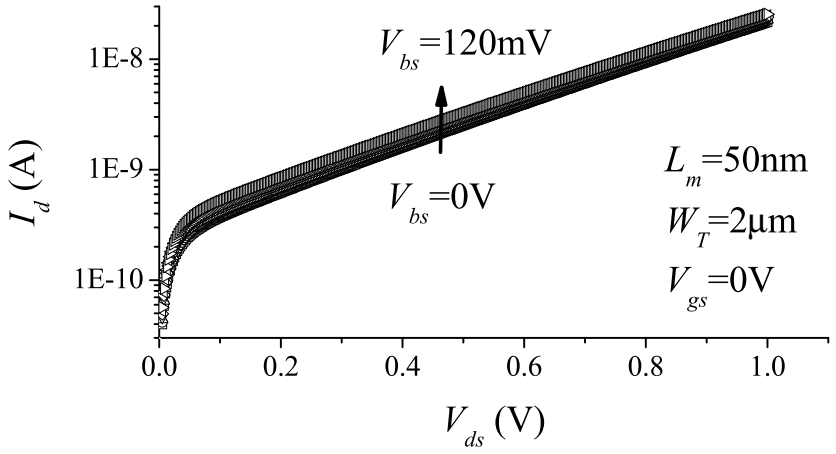


Fig. 3.2. Exponential behavior of the leakage current for a 50nm MOSFET channel length at V_{gs}=0V. Notice the weak dependence of I_d with V_{bs}.

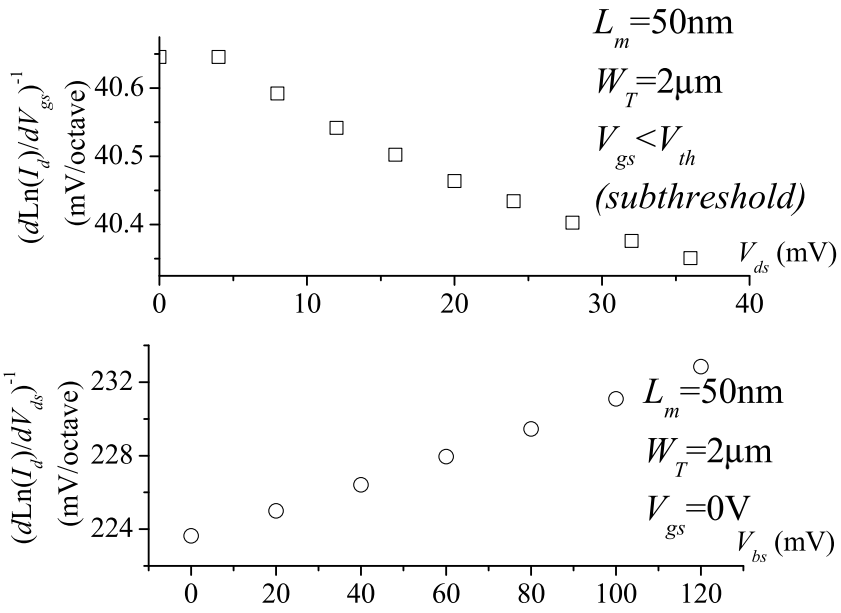


Fig. 3.3. TOP: Inverse of the slope of the ln(I_d)–V_{gs} curves in the subthreshold region plotted versus V_{ds}. BOTTOM: Inverse of the slope of the ln(I_d)–V_{ds} curves at V_{gs}=0 V plotted versus V_{bs}. These results suggest that at V_{gs}=0 V the dominant transport mechanism is diffusion (notice the weak dependence of the plotted data with V_{ds}).

3.2 MOSFET Parasitic Bipolar Transistor Operation at V_{gs}=0 V

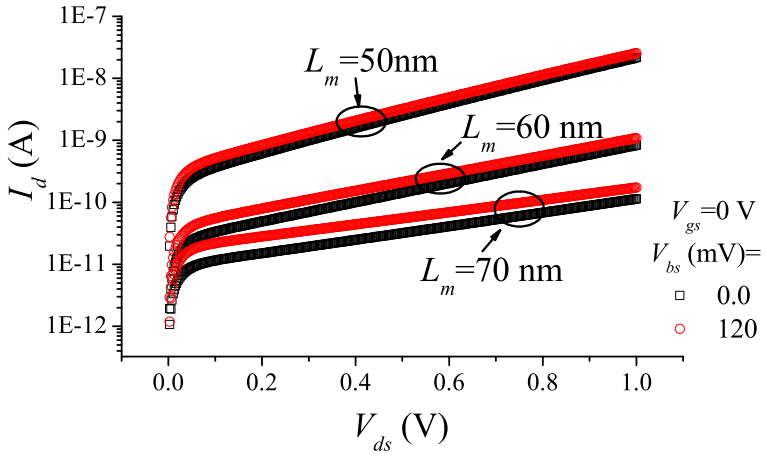


Fig. 3.4. Off-state leakage current measured at V_{gs}=0 V for three MOSFETs with different channel lengths.

The intrinsic parasitic bipolar transistor (pBJT) presented in the MOSFET structure is shown in Fig. 3.1. This pBJT is turned on when a considerable amount of charge flows through the intrinsic bulk terminal of the MOSFET (i.e. the parasitic base terminal). This charge flow may be generated through several mechanisms of charge leakage generation that occur in the bulk MOSFET under different bias conditions, such as tunneling through oxide or impact ionization. One of the most analyzed mechanisms of this type is the gate-induced-drain-leakage (GIDL). GIDL, as its name indicates, is strongly dependent on the applied bias at the gate, which defines a leakage current when the device is operating in the strong inversion region. Thus, in order to observe BTBT, which is the effect we are studying, it is necessary to minimize GIDL, which is achieved when the MOSFET is biased at V_{gs}=0 V. Under this gate-to-source bias condition, the I_d–V_{ds} curves associated with the pBJT were obtained by measuring the drain current when varying the bulk-to-source voltage from 0 to 120 mV in steps of 20 mV. As shown in Fig. 3.2, the drain current presents an exponential behavior inherent to the operation of a bipolar transistor. As it is well

known, the efficiency of a BJT is proportional to the inverse of the slope of the I_d versus V_{ds} curve plotted in a logarithmic scale ($[d\ln(I_d)/dV_{ds}]^{-1}$). In Fig. 3.3, a

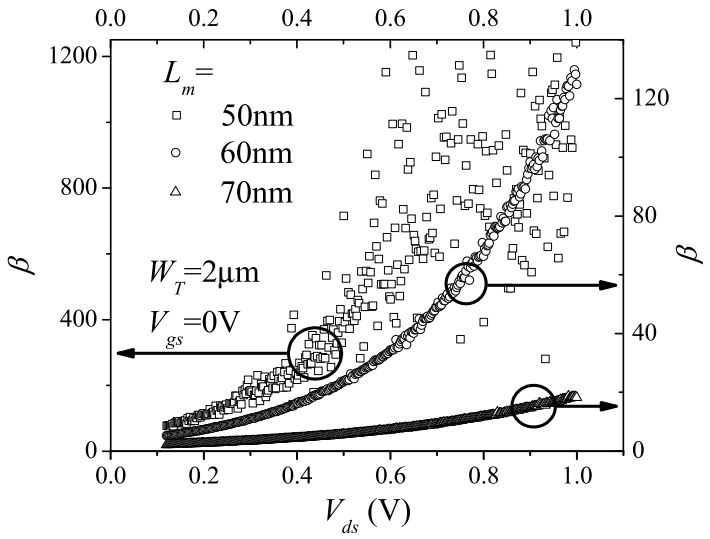


Fig. 3.5. Extracted β versus V_{ds} for transistors with fixed width and different lengths. As expected, β increases as L_m is reduced.

comparison between the inverse of the slope of the I_d–V_{gs} and I_d–V_{ds} curves plotted versus V_{ds} and V_{bs} respectively is shown. Since $[d\ln(I_d)/dV_{gs}]^{-1}$ presents a weak dependence on V_{ds}, the diffusion component of the current flowing between drain and source is negligible when $V_{gs}<V_T$. In contrast, $[d\ln(I_d)/dV_{ds}]^{-1}$ varies in a more accentuated way when plotted versus V_{bs} at V_{gs}=0 V, which means that once the transistor is completely in off-state, the diffusion component becomes important.

Another consideration in the analysis of the pBJT is the dependence of β with the channel length. As it was previously mentioned, the channel of the MOSFET acts as the base of the pBJT. Therefore, the BTBT effect is strongly dependent on the channel length and therefore the measurements corresponding to the leakage current generated by the pBJT considerably vary with L_m as shown in Fig. 3.4. In this figure,

the drain current at V_{gs}=0 and V_{bs}=0 and 120 mV is plotted for MOSFETs with L_m=50, 60, and 70 nm. As can be seen, β of the pBJT increases as the MOSFET channel length is reduced, which is observed as an increase in the BTBT parasitic current due to the reduction of the base region.

3.3 Extraction Methodology of the Parasitic Bipolar Gain (β)

An important parameter for the analysis of the pBJT is the determination of β. In order to extract β from the measured data, the following methodology is proposed. In accordance with Fig. 3.1, the following relations between the pBJT and MOSFET currents can be established:

$$I_d = I_c + I_{tun} \qquad (1) \quad I_s = I_e \; (2)$$

Where I_c and I_e are respectively the collector and emitter currents of the pBJT. Thus, if β>>1, $I_c \approx I_e$ and

$$I_d - I_s = I_{tun} \qquad (3)$$

Hence, assuming that I_{tun} is approximately equal to the base current feeding the pBJT and considering $I_e=(\beta+1)I_{tun}$, the following expression can be obtained by combining (1)-(3):

$$\frac{I_s}{I_d - I_s} = \beta + 1 \qquad (4)$$

In Fig. 3.5, β for the pBJTs associated with MOSFETs with L_m=50, 60, and 70 nm is shown. As previously discussed, β increases as the MOSFET channel length decreases and shows a dependence on V_{ds} since this voltage sets the collector-to-emitter voltage.

3.4 Demonstration of the Parasitic Band-To-Band Tunneling Charge Leakage

Once the presence of the pBJT effect is demonstrated and the corresponding β is extracted, the determination of the charge leakage mechanism that turns on the parasitic current is necessary. Fig. 3.6 shows the experimentally determined base current of the pBJT, which was obtained from (3). Considering that V_{gs}=0, all the associated mechanisms related to the gate are discarded (e.g. tunneling through oxide or impact ionization). Moreover, because of the high drain doping concentration, the avalanche multiplication effect can be neglected at a low V_{ds}. Afterwards, it is demonstrated that the mechanism that is generating the charge leakage in the intrinsic bulk is band-to-band-tunneling. In order to demonstrate the BTBT effect, the experimental I_{tun} data is compared with simulated data using the equation (5) from [43], as shown in Fig. 3.6. Equation (5) defines the density current given for a reverse biased *p-n* junction

$$J_{b-b} = \frac{\sqrt{2m^*}q^3 E V_{ds}}{4\pi^3 \hbar E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3qE\hbar}\right) \quad (5)$$

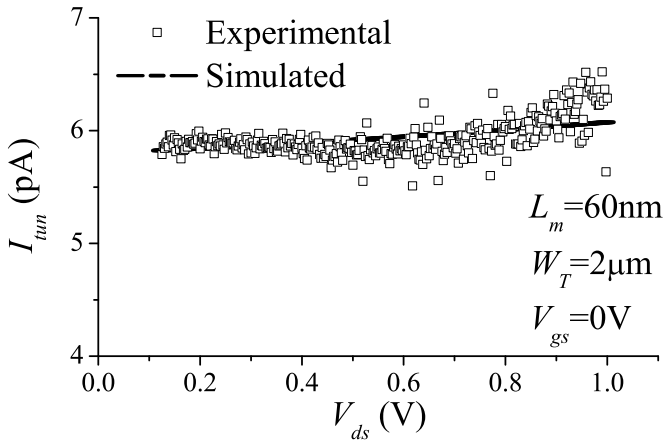


Fig. 3.6. Experimental I_{tun} data compared with simulated data using the equation reported in [7] to demonstrate the BTBT effect.

In equation (6) E_g is the energy bandgap, and

$$E = \sqrt{\frac{2qN_a\left(V_{ds} + \psi_{bi}\right)}{\varepsilon_{Si}}} \qquad (6)$$

Where N_a is the bulk doping concentration and ψ_{bi} is the built-in potential of the drain-bulk junction. The good correlation that is achieved between experimental and simulated data demonstrates the BTBT effect (see Fig. 3.6).

3.5 Conclusions

The analysis and characterization of the off-state leakage current (V_{gs}=0) for a nanometric bulk MOSFET was introduced. The experimental results show that a considerable leakage current is flowing from the drain to the source terminals for V_{gs}=0. The exponential behavior of the drain current proves the presence of a pBJT. To support the analysis, an analytical procedure to extract the gain of the pBJT was presented. Furthermore, the BTBT effect, which is the charge leakage mechanism

that turns the pBJT on was demonstrated and analyzed. The BTBT effect was demonstrated by the good correlation between the experimental and tunneling model. These results show this leakage current needs to be reduced in order to improve the stand by power consumption for high-density, very low-power, battery powered CMOS technologies.

Chapter 4

Analysis of the Impact of the Drain-Junction Tunneling Effect on a Microwave MOSFET from S-parameter Measurements

4.1 Introduction

MOSFET characterization is key among several aspects to improve compact models, to optimize device and circuit design, and to reduce the leakage currents reducing the power efficiency of electronic systems. As pointed out in recently published literature [1], the reduction of the leakage current plays a fundamental role in the transistor and circuit design for low-power CMOS applications. Moreover, due to the increased demand for high-speed electronics products, the accurate modeling of the MOSFET at high frequencies (HF) it becomes necessary to represent the behavior of this device in microwave circuits and systems [2]. However, as the operation frequency continues to increase and the channel length to reduce, higher order effects make

increasingly difficult to represent the electrical behavior of the MOSFET at HF. In this case, one of the characteristics that have to be accurately represented is the output impedance [3]. Several parameters that influence the MOSFET's output characteristics have been previously analyzed in the literature, such as the source/drain parasitic resistances, and the substrate impedance [4]-[6]. In fact, some of the effects that become apparent at HF have been directly associated to these parameters to keep the modeling simple and analytical [65].

As is well known, the MOSFET HF characterization based on the measurement of two-port S-parameters allows the determination of the equivalent circuit model parameters, and several techniques have been reported to obtain MOSFET's intrinsic and extrinsic parameters. Therefore, using an S-parameter measurement-based characterization helps to identify the effects occurring within the device when associating the model parameters with physical phenomena. As the MOSFET dimensions shrink, more of these effects become apparent and have an important influence in device performance. Thus, the proper determination of the associated parameters is necessary to accurately predict the device's behavior under a wide variety of conditions. One of these high-order effects taking importance as the channel length shrinks to nanometric dimensions is the band-to-band tunneling (BTBT) occurring in the drain-bulk junction. Thus, using measured S-parameters to obtain the model parameters associated with this effect is desirable to assess the performance of the device, but also to represent the corresponding behavior under a small-signal regime. The importance of the BTBT effect relies on the fact that the MOSFET's output characteristics are affected with the corresponding tunneling

current at relatively high drain-to-source voltages, which considerably affects the performance of short-channel devices. In fact, previously reported experimental analyses have considered this effect in SOI MOSFETs [53] and in field-induced band-to-band tunneling effect transistors (FIBTET) [51]. These previous analyses of the BTBT effect have been performed using regression methods applied to DC measurements of several devices, assuming that this effect remains constant with the channel length. Until now, however, the potential of S-parameter measurements performed to single devices to carry out an analysis of the BTBT effect has not been explored.

In this chapter, we explore the use of small-signal S-parameter measurements to identify and quantitatively determine the impact of BTBT originated at the drain-bulk junction of a MOSFET. We confirmed the presence of the BTBT effect through an exhaustive analysis of the experimental MOSFET's small-signal parameters up to 40 GHz. For this reason, we also propose a straightforward parameter extraction procedure that allows identifying the dominant effects influencing the device's output impedance. The proposed method is based on S-parameter measurements performed to a device biased at V_{gs}=0 V and V_{ds}>0 V. Using this method, we observe that an additional admittance must be included in the MOSFET HF equivalent-circuit model when considering BTBT. This admittance accounts for the current introduced by the band-to-band carrier tunneling effect occurring at the drain junction in short-channel devices, and allows a considerable improvement of the small-signal modeling of a MOSFET at high frequencies. The proposed methodology is validated through a

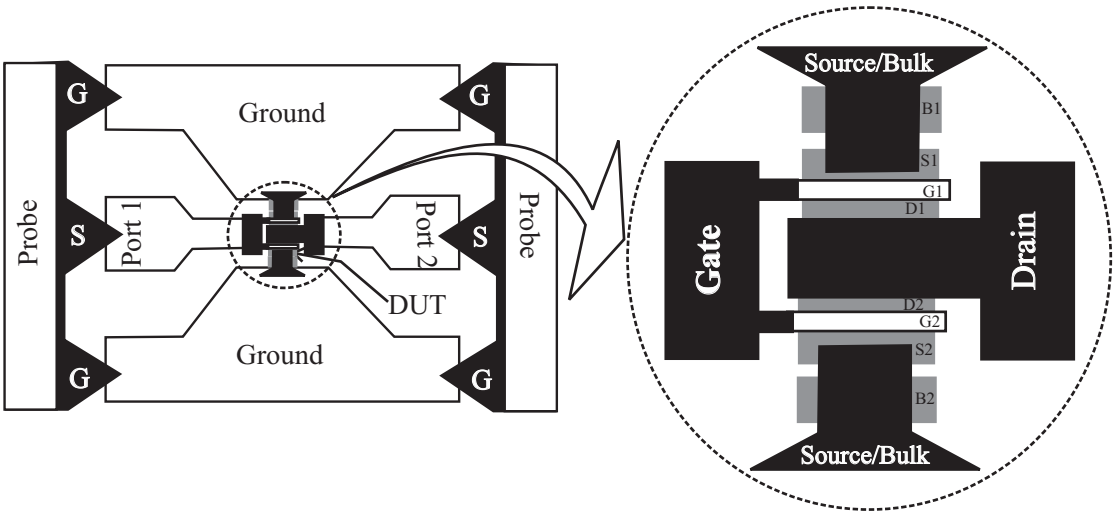


Fig. 4.1. Sketch showing the top view of the MOSFET RF test structure.

correlation between simulated and experimental data for microwave MOSFETs fabricated in a 0.1 μm CMOS technology.

4.2 Experiments

A calibrated vector network analyzer was used to measure S-parameters to four common-source/bulk *n*MOSFETs fabricated on a *p*-type Si substrate. These devices have a channel mask length, L_m=0.1 μm, two gate fingers (NF=2), and finger widths W_f=5, 10, 15 and 20 μm respectively. Additional open and short dummy structures were used to correct the measurements from pad parasitics. The S-parameters were taken at V_{gs}=0 V and V_{ds}=0.3, 0.55, 0.8, and 1.05 V. The top view of the layout of the MOSFET RF test structure is presented in Fig. 4.1. Due to the poor quality channel formation under the V_{gs}=0 V condition, the impact of the parasitic currents flowing between drain and source when there is no channel can be analyzed using an equivalent circuit approach explained hereafter.

4.3 Method Formulation

Fig. 4.2 shows the model of a MOSFET biased at V_{gs}=0 V that includes the intrinsic and extrinsic components. In this model, the source and drain parasitic resistances (R_s and R_d respectively), the drain and source junction capacitances (C_{jd} and C_{js} respectively), the gate resistance (R_g), and the substrate resistance (R_b) are considered as extrinsic elements, whereas the intrinsic part of the MOSFET is represented by means of three capacitances and a complex admittance (g^*_{tun}). The later is associated with the drain to bulk BTBT effect.

In the model presented in Fig. 4.2, all the extrinsic elements are considered as drain-bias independent. This assumption is valid for the source and drain parasitic resistances since the spreading and the accumulation resistances do not present a considerable variation with V_{ds} at V_{gs}=0 [65]. For the case of the drain and source junction capacitances, and for the substrate resistance, this assumption is also reasonable due to the high doping of the *p*-*n* junction associated with the drain and source regions. Besides, accurate results have been obtained when assuming drain-to-source voltage independence of the substrate parameters [73].

In order to determine the substrate parameters, the equivalent circuit of Fig. 4.2 can be used. When V_{ds}=0 V is assumed, the effect of g^*_{tun} can be neglected, and the typical assumptions considered under zero-bias cold-FET conditions allow to arrange the equation associated with the real part of Z_{22} in the form [65]:

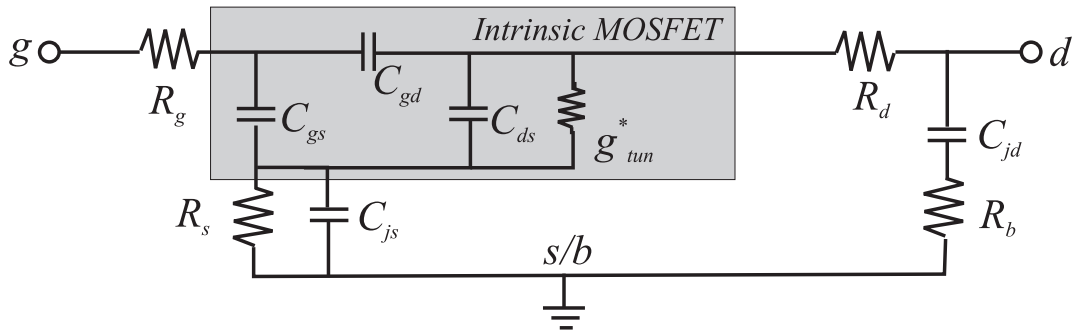


Fig. 4.2. Equivalent circuit model for a MOSFET biased at V_{gs}=0 V and V_{ds}>0 V.

$$\frac{\omega^2}{\mathrm{Re}(1/Z_{22})} \approx R_b\omega^2 + \frac{1}{C_{jd}^2 R_b} \tag{1}$$

Where ω is the angular frequency in radians. Thus, R_b and C_{jd} can be determined respectively from the slope and the intercept with the abscises of a linear regression of the experimental $\omega^2/\mathrm{Re}(1/Z_{22})$ versus ω^2 data.

Once R_b and C_{jd} have been obtained, the corresponding effect is removed from the experimental data by applying the following equation:

$$\mathbf{Y}_A = \mathbf{Y}_{meas} - \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{\omega^2 C_{jd}^2 R_b}{1+\omega^2 C_{jd}^2 R_b^2} + \dfrac{j\omega C_{jd}}{1+\omega^2 C_{jd}^2 R_b^2} \end{bmatrix} \tag{2}$$

where $\mathbf{Y}_{meas}$ represents the Y-parameter matrix obtained from the direct transformation of measured S-parameters into Y-parameter data, whereas $\mathbf{Y}_A$ represents the Y-parameter matrix after the effect of R_b and C_{jd} has been removed from the measurements.

In [73], a procedure to obtain the source and drain resistances was proposed. Using this method, the bias-dependent series resistances were determined allowing good simulation-experiment correlation as presented in the results section. Thus, after R_s

and R_d are extracted, the corresponding effects are de-embedded from the experimental data by applying the following equation:

$$\mathbf{Z}^* = \mathbf{Z}_A - \begin{bmatrix} R_g & X - j\omega C_{js} R_s X \\ X - j\omega C_{js} R_s X & R_d \end{bmatrix} \tag{3}$$

where

$$X = \frac{R_s}{1 + \omega^2 C_{js}^2 R_s^2},$$

$\mathbf{Z}_A$ is the Z-parameter transformation of $\mathbf{Y}_A$, and $\mathbf{Z}^*$ is the corresponding Z-parameter

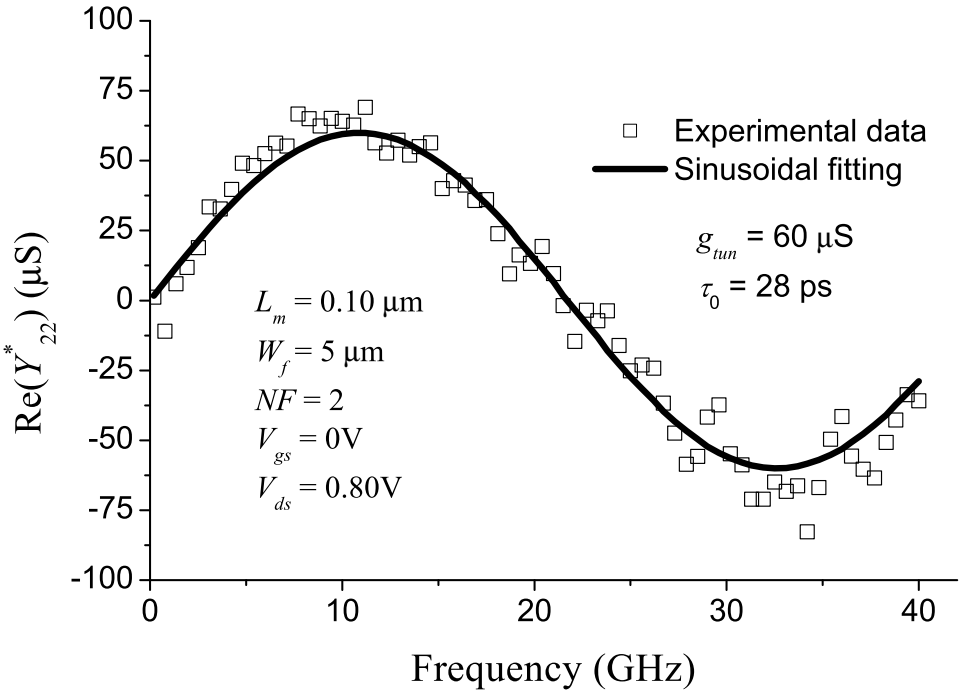


Fig. 4.3. Experimental Re(Y^*_{22}) versus frequency data showing a sinusoidal behavior. The solid line represents the fitting used to determine g_{tun} and τ_0.

matrix after removing the effect of the extrinsic resistances. In the equation (3), $C_{jd} \approx C_{js}$ is considered since, as can be seen in Fig. 4.1, the devices under investigation were designed to be symmetrical (i.e. the total area and perimeter of the drain junctions are the same to those of the source junctions).

After removing the effect of the extrinsic parameters from the measured data, the reference plane of the experimental-data is shifted down to the MOSFET's intrinsic part. In this case, previously reported simplified approaches consider the intrinsic behavior of the device as purely capacitive even for high values of V_{ds}. This means that the real part of the Y-parameters associated with the MOSFET intrinsic part should be approximately equal to zero. However, as shown in Fig. 4.3, a sinusoidal behavior of the experimentally determined real part of the intrinsic Y^*_{22} parameter is observed when plotted versus frequency. This suggests that an additional current flow from the intrinsic drain to source (in parallel with C_{ds}) has to be considered. According to the analysis presented in the results section, this current is associated with the BTBT effect occurring in the depletion region at the drain side [50]. The following theoretical analysis allows verifying the implications of this current when the MOSFET operates at high frequencies.

According to Fig. 4.2, when the admittance g^*_{tun} is connected in parallel with C_{ds}, Y^*_{22} can be expressed by means of:

$$Y^*_{22} = g^*_{tun} + j\omega(C_{ds} + C_{gd}) \tag{4}$$

where g^*_{tun} is associated with the BTBT charge flow and is given by [43]:

$$g_{tun}^{*} = g_{tun} e^{-j(\omega\tau_0 - \pi/2)} \tag{5}$$

In this equation, g_{tun} and τ_0 are respectively the magnitude and the phase delay introduced by the BTBT effect.

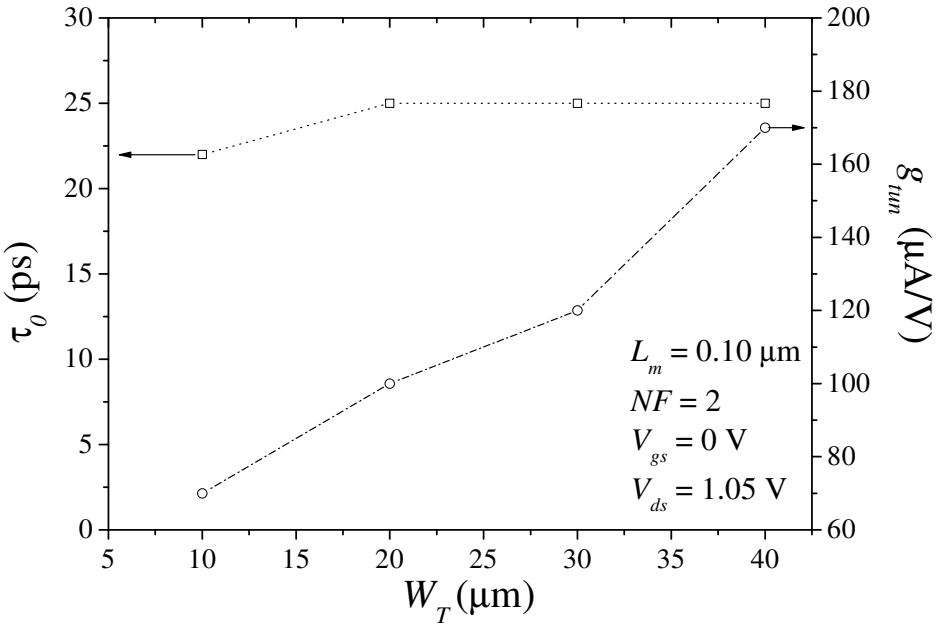


Fig. 4.4. Extracted τ_0 and g_{tun} versus W_T data showing a physically expected trend.

Notice that the equation (5) can be expanded in real and imaginary parts, which yields:

$$g_{tun}^{*} = g_{tun}\left[\cos\left(\omega\tau_0 - \frac{\pi}{2}\right) - j\sin\left(\omega\tau_0 - \frac{\pi}{2}\right)\right]$$
$$= g_{tun}[\sin(\omega\tau_0) + j\cos(\omega\tau_0)] \quad (6)$$

Thus, the combination of (4) and (6) allows confirming that the real part of Y^{*}_{22} presents a sinusoidal form expressed by:

$$\mathrm{Re}(Y_{22}^{*}) = g_{tun}\sin(\omega\tau_0) \quad (7)$$

As can be noticed, g_{tun} and τ_0 can be directly determined from the magnitude and phase velocity of a sinusoidal fitting of the experimental $\mathrm{Re}(Y^{*}_{22})$ versus frequency data. This extraction is illustrated in Fig. 4.3.

Once g_{tun} and τ_0 have been determined, the intrinsic capacitances are directly obtained from the imaginary part of the intrinsic Y-parameters.

4.4 Results and Discussion

In Fig. 4.4, the extracted g_{tun} and τ_0 versus the total gate width (W_T=$NF{\cdot}W_f$) data is plotted. As expected, g_{tun} is proportional to W_T since the current flowing from drain to source will increase as the device's width increases. For the case of τ_0, no dependence with W_T is observed, which is also physically expected since this parameter is associated with a time delay of the carriers flowing between the intrinsic drain and source regions. Thus, τ_0 would be dependent on the separation between drain and source and low sensitive to width variations.

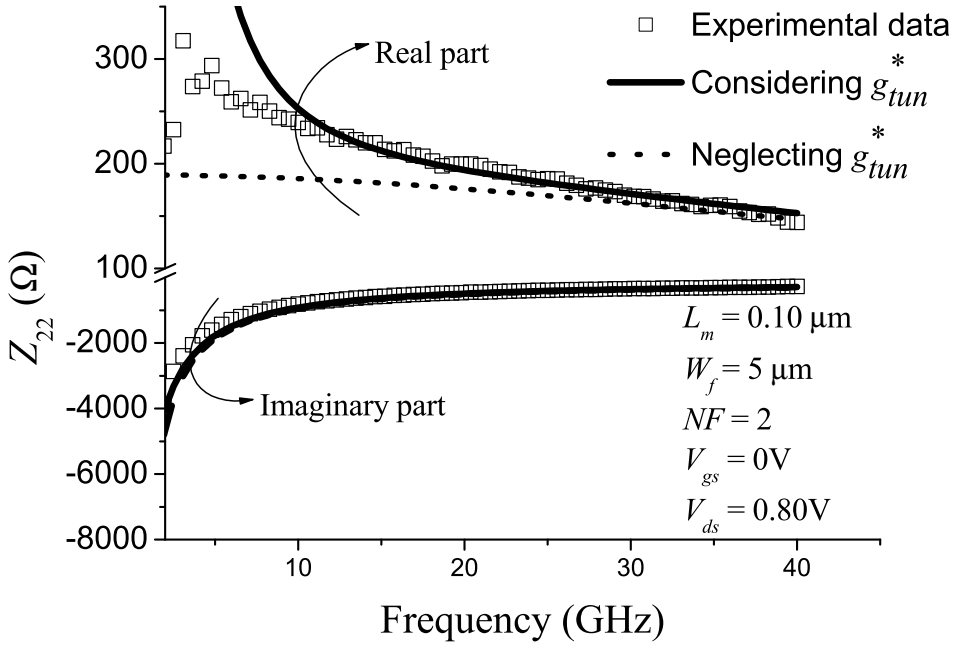


Fig. 4.5. Comparison between the simulated and experimental output impedance showing the improved modeling when considering g^*_{tun}.

Finally, in order to validate the proposed parameter extraction procedure, in Fig. 4.5 the simulated real and imaginary parts of the MOSFET output impedance are compared with experimental data. The simulations were performed with HSPICE after each small signal MOSFET model parameter was obtained following the proposed procedure. As can be seen in Fig. 4.5, the simulation is considerably improved for Re(Z_{22}) above 10 GHz when the current source associated with the current tunneling is considered, whereas an almost frequency independent curve is obtained when ignoring this effect. In contrast, notice that below 10 GHz the MOSFET intrinsic part presents a higher impedance when biased at V_{ds}>0 V, which is not considered in the traditional models and yields an underestimation of this parameter. In the case of the curve obtained when considering the tunneling current

source, the simulation presents the correct trend. Nevertheless, the inclusion of additional elements may be necessary to improve the simulation for this specific low frequency range.

4.5 Conclusions

An analytical method for the extraction of the small-signal MOSFET parameters including BTBT effects was presented and demonstrated. The extracted methodology represents a valuable tool to assess the influence of BTBT effects in nanometric devices from S-parameter measurements. These measurements are performed to a single MOSFET avoiding dependence of the variation of the electrical characteristics with the device geometry. Furthermore, the proposed method allows the determination of the parameters to accurate represent the intrinsic behavior of MOSFETs at high frequencies. Excellent simulation-experiment correlation was achieved up to 40 GHz, and physically expected trend of the extracted parameters was observed when plotted versus channel width. Furthermore, the small-signal model for a MOSFET can be considerably improved when considering this additional effect when operating within the microwave range.

Chapter 5

General Conclusions

5.1 Introduction

A full DC and HF characterization of the drain-to-bulk junction band-to-band tunneling effect has been presented in this thesis. For this reason, the analysis of the charge leakage through the substrate is presented under DC and HF conditions. This analysis was based on an exhaustive study through measurements performed to 0.1 μm and 60 nm CMOS devices. The measured data shows that the input and output features of the HF MOSFET are considerable affected by high order parasitic effects, such as band-to-band tunneling. So far, band-to-band tunneling has been

considered as a pure DC second-order effect. However, in this work it is verified that this particular DC second-order effect has also an impact on the behavior of the MOSFET at HF. This second order effect is associated with current sources (in the case of DC operation conditions) or a conductance (in the case of HF operation conditions) in an equivalent circuit model. In order to obtain accurate values for the parameters associated with these models, a de-embedding involving the parasitic circuit elements was done with great care using a new proposed analytical methodology. Thus, in this thesis two methodologies were proposed, one based on DC measured data and another based on S-parameter measurement.

Additionally, to guarantee the validity of the measured two port network MOSFET parameters, a complete analysis of the impact of the pad parasitics at HF was presented. With this respect, a qualitatively comparison of the conventional test structures and ground-shielded structures, was presented. Even more, an analytical methodology for the extraction of each of the parasitic associated to the shielded test structures was also proposed, which represents a useful tool when performing microwave measurements to semiconductor devices.

With regard to the DC extraction methodology, the gain of the parasitic bipolar transistor presented in 50, 60, and 70 nm channel length MOSFETs was extracted, showing the dependence of the parasitic bipolar gain on the MOSFET channel length. In addition, it was observed that, as the MOSFET channel length is continuing downscaling, the parasitic bipolar gain is increasing, which may result in a larger current leakage. This is due in part to the fact that the miniaturization of the MOS technology implies the use of heavy and very shallow drain/source regions, which

together with the very short channel length, results in a more prominent band-to-band tunneling effect. Therefore, the incorporation of band-to-band tunneling in deep nano-metric MOS technology modeling is a need.

In order to provide information about the impact of the band-to-band tunneling effect under HF conditions, an S-parameter measurement based methodology up to 40 GHz was presented. In this methodology, the importance of single transistor measurements for the determination of the equivalent circuit parameters values is demonstrated. As is well known, many model parameters are channel length dependent. Thus, using a single-device measurement technique eliminates the uncertainty of applying linear regression of data obtained from devices with different channel lengths. An interesting point to be mentioned is that the conductance associated to the band-to-band tunneling effect shows a sinusoidal behavior, which depends on the MOSFET channel length. This sinusoidal trend of the experimental data points out the fact that there are a finite transit time of the carriers associated with the parasitic currents originated by the tunneling effect.

The obtained results indicate that second order effects and in particular the tunneling effect is of great importance. For the tunneling effect, as the channel length shrinks down, the corresponding conductance increases. This may result in a larger degradation of the performance of analog circuits operating in the microwave range.

5.2 New challenges in MOSFET modeling

The continuous scaling of CMOS devices down to the sub-30-nm regime results in higher device density, faster circuit speed, and higher power dissipation. Besides, many new physical phenomena such as 2-D/3-D electrostatics, CLM, DIBL, remote surface roughness scattering, mobility degradation, impact ionization, band-to-band tunneling, velocity overshoot, self-heating, channel charge quantization, polysilicon depletion, NQS effects, gate-induced drain leakage and noise, and discrete dopant become significant since the device dimensions are approaching the technology limits. Meanwhile, accurate MOSFET models that include the observed physical phenomena are crucial to design and optimize advanced VLSI circuits for nanoscale CMOS technology. Moreover, these models are required for both analog and digital circuits. Thus, it is mandatory the development of advanced compact models to face the enormous challenges introduced by the development of sub-30-nm technologies.

The incorporation of all the second-order effects in the development of a HF MOSFET model is beyond a single PhD thesis. Therefore, this work focuses only on contributions regarding some particular aspects including microwave probing, bias-dependent parameter extraction at HF, correlation of DC and RF extracted data, band-to-band tunneling effects, and the corresponding implications at HF. A HF model that incorporates all the effects that become apparent in advanced devices is complex and represents a challenge that is continuously faced through intense research at academy and industry levels. With this respect, future research in this direction will be

continued using different configurations of test structures that are needed to support further analyses. These structures include common gate/bulk MOSFETs and even multiport-configured devices. This is due to the fact that the high-order parasitic effects have different bias and geometry dependence. Even more, the continuous downscaling of the dimensions of the MOSFET makes several effects appear at the same bias conditions. Hence, to analyze a specific effect in the MOSFET, the design of special test structures for a complete characterization is required. In addition, quantum effects [43] that are predominant for deep nano-metric technologies should be also considered for the HF modeling of MOSFETs.

The results that will be obtained in further analyses from DC and HF device characterization will give enough information to determine the geometry dependence of the effects under analysis. This is necessary for the model scalability, where the characterization information has to be implemented in a compact model.

5.3 Model scalability for sub-nanometric devices

As is well known, every compact model needs to accurately represent the DC and HF behavior of a MOSFET of any geometry within an actual design. Then, the scalability of each model for the parasitic effects is important for an accurate simulation of any device, circuit and system. Nevertheless, as the channel length is reduced to nanometric dimensions, a more detailed geometry dependence model is necessary. This is because of the limits imposed by the classical electric characteristics of the

MOSFETs and the quantum electric behavior of the next generation devices. Even when engineering work is being carried out with success to reduce the quantum effects appearing in nanometric devices, eventually these effects will take importance and will determine the conditions at which the classical electric characteristics and quantum behavior assumptions have to be applied. However, the simplicity of the design equations can be carried out with the help of equivalent circuit models. This is because any physical phenomena can be accurately represented by means of an arrangement of the elemental circuits such as resistors, capacitors and inductors. Thus, under certain conditions the equivalent circuit model can be reduced and the equations that determine the behavior of the device in DC and HF conditions can be easily implemented in a compact model.

5.4 Techniques for device characterization

It is obvious that DC and HF nanometric MOSFET modeling requires of special characterization methodologies that incorporates second order effects and substrate current coupling paths. The incorporation of these effects associated to nanometric MOS technologies, will result in reliable de-embedding techniques and electrical models. Nevertheless, the analytical methodologies proposed for the extraction of some kind of parasitic elements associated to a specific parasitic effect are not sufficient to determine the nature of the phenomena. In consequence, a correlation of the behavior of the input and output characteristics of the device operated in DC and

HF behavior is necessary to validate every hypothesis. In this thesis, such kind of analysis has been applied and demonstrated as a good starting point for a full characterization of the MOSFET from DC to HF. It is important to mention that although only the band-to-band tunneling is incorporated, other second-order effects, like for instance GIDL, DIBL, can also be incorporated to develop a scalable HF MOSFET model.

Publications derived from this work

• **Emmanuel Torres-Rios**, Reydezel Torres-Torres and Edmundo A. Gutiérrez-D., ”A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from S-parameters”, *IEEE Trans. Electron Devices*, vol. 53, no. 3, 2006, 571-573.

• **Emmanuel Torres-Rios**, Reydezel Torres-Torres, Roberto Murphy-Arteaga and Edmundo A. Gutiérrez-D., ”Analytical characterization and modeling of shielded test structures for RF-CMOS”, Workshop on Frontiers in Electronics (WOFE) [*Best Student Poster*], Cozumel, Mexico, 2007. *Invited for publication in the International Journal for High Speed Electronics and Systems*.

• **Emmanuel Torres-Rios**, Reydezel Torres-Torres and Edmundo A. Gutiérrez-D,” Analysis of the Impact of the Drain-Junction Tunneling Effect on a Microwave MOSFET from S-parameter Measurements,” *Accepted for publication in Solid State Electronics*.

• **Emmanuel Torres-Rios**, Reydezel Torres-Torres and Edmundo A. Gutiérrez-D “Analysis of the Band-to-Band Tunneling Effect in 65 nm nFETs”, *ESSDERC 2008*, Edinburgh Scotland.

• Edmundo A. Gutiérrez D., **Emmanuel Torres R.** and Reydezel Torres T., ”Magnetic sensing as signal integrity monitoring in integrated circuits”, *ESSDERC 2005*, Grenoble, France, 2005.

Bibliography

[1] R. Bansal, "Microwave surfing, 21st century warfare", *IEEE Microwave Magazine*, vol. 7, no. 1, 2006, pp. 36-38.

[2] B. Razavi, "Gadgets gab at 60 GHz", *IEEE spectrum*, vol. 45, no. 2, 2008, pp. 46-49.

[3] C. Devlin, T. Brazil, and G. Magerl, "Target network: Microwave power amplifiers", *IEEE Microwave Magazine*, vol. 7, no. 2, 2006, pp. 34-48.

[4] N. H. L. Koster, B. J. Koster, D. Erni, and A. Beyer, "Oscillator design for suppressing spurious signals", *IEEE Microwave Magazine*, vol. 8, no. 3, 2007, pp. 67-80.

[5] F. Ivanek, "Microbusiness, business impact of municipal Wi-Fi network", *IEEE Microwave Magazine*, vol. 8, no. 2, 2007, pp. 30-32.

[6] S. Oda, and D. Ferry, "Silicon nanoelectronics", *Taylor & Francis Group*, 2006.

[7] F. Schwierz, and J. J. Liou, "Modern microwave transistors; theory, design and performance", *Wiley Interscience*, 2003.

[8] B. Razavi, "CMOS transceivers for the 60-GHz band", *Proc. Symp. On Computers and Comunications*, 2007.

[9] ITRS roadmap 2006, www.itrs.net.

[10] Y. Tsividis, "Operation and modeling of the MOS transistor", *Oxford*, 1999,2nd edition.

[11] J. Verspecht, and D. E. Root, "Polyharmonic distortion modeling", *IEEE Microwave Magazine*, vol. 7, no. 3, 2006, pp. 44-57.

[12] L. Katehi, W. Chappell, S. Mohammadi, A. Margomenos, and M. Steer, "Heterogeneous wafer-scale circuit architectures", *IEEE Microwave Magazine*, vol. 8, no. 1, 2007, pp. 52-69.

[13] Y. Cheng, "MOSFET modeling for RF IC design", *Int. Jour. High Speed and Sys.*, vol. 11, no. 4, 2001, pp. 1007-1084.

[14] Chih-Hung C, and M. J. Deen, "RF CMOS noise characterization and modeling", *Int. Jour. High Speed and Sys.*, vol. 11, no. 4, 2001, pp. 1085-1157.

[15] A. Goswami, A. Agrawal, C. T. Thuruthiyil, M. Gupta, and R. S. Gupta, "Small-signal analytical MOSFET model for microwave frequency applications", *Microwave and Optical Tech. Letters*, Vol. 25, no. 5, pp. 346-352.

[16] J. Chen, F. Assaderaghi, Ping-Keung K., and C. Hu, "The enhancement of gate-induced-drain-leakage (GIDL) current in short-channel SOI MOSFET and its application in measuring lateral bipolar current gain β", *IEEE Electron Device Letters*, vol. 13, no. 11, 1992, pp. 572-574.

[17] J. S. Kolhatkar, and A. K. Dutta, "A new substrate current model for submicron MOSFET's", *IEEE Trans. Electron Device Letters*, vol. 47, no. 4, 2000, pp. 861-863.

[18] Wen-Chin L., and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence band electron and hole tunneling", *IEEE Trans. Electron Device Letters*, vol. 48, no. 7, 2001, pp. 1366-1373.

[19] A. Mercha, J. M. Rafí, E. Simeón, E. Augendre, and C. Claeys, "Linear kink effect induced by electron balance band tunneling in ultrathin gate oxide bulk and SOI MOSFETs", *IEEE Trans. Electron Device Letters*, vol. 50, no. 7, 2003, pp. 1675-1682.

[20] Shey-Shi L., C. Meng, To-Wei C., and Hsiao-Chin C., "The origin of the kink phenomenon of transistor scattering parameter S_{22}", *IEEE Trans. Microwave Theory and Thec.*, vol. 49,no. 2, 2001, 333-340.

[21] I. Kwon, M. Je, Kwyro Lee, and H. Shin, "A simple and analytical parameter-extraction method of a microwave MOSFET", *IEEE Trans. Microwave Theory and Thec.*, vol. 50,no. 6, 2002, 1503-1509.

[22] Wen-Kuan Y., Chao-Ching K. Shuo-Mao C., Yean-Kuen F., and C. P. Chao, "Effect of extrinsic impedance and parasitic capacitance on figure of merit of RF MOSFET", *IEEE Trans. Electron Devices*, vol. 52, no. 9, 2005, pp. 2054-2060.

[23] Chuang-Hwan K., C. S. Kim, H. K. Yu, and K. S. Nam, "Unique extraction of substrate parameters of common-source MOSFET's", *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 3, 1999, pp. 108-110.

[24] Jyh-Chyurn G., and Yi-Min L., "A new lossy substrate de-embedding method for sub-100 nm RF CMOS noise extraction and modeling", *IEEE Trans. Electron Devices*, vol. 53, no. 2 2006, pp. 339-347.

[25] B. Razavi, Ran-Hong Y., and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices", *IEEE Trans. on Circuits and Syst.-1*, vol. 41, no. 11, 1994, pp. 750-754.

[26] T. E. Kolding, "Consistent layout technique for successful RF CMOS design", *Proc. Workshop on New Tech. for RF Circuits*, 2000.

[27] C. S. Kim, Jung-Woo P., H. K. Yu, and H. Cho, "Gate layout and bonding pad structure of a RF n-MOSFET for low noise performance", *IEEE Electron Device Letters*, vol. 21, no. 12, 2000, pp. 607-609.

[28] Yo-Sheng L., "An analysis of small-signal source-body resistance effect on RF MOSFETs for low-cost system-on-chip (SoC) applications", *IEEE Trans. Electron Devices*, vol. 52, no. 7, pag. 1442-1451, Jul. 2005.

[29] X. Gao, J. J. Liou, J. Bernier, and G. Croft, "An improved model for substrate current of submicron MOSFETs", *Solid State Electronics*, vol. 46, 2002, 1395-1398.

[30] R. Gwoziecki, and T: Skotnicki, "Physics of the subthreshold slope-initial improvement and final degradation in short CMOS devices", *Proc. ESSDERC*, 2002.

[31] H. L. Kao, A. Chin, C. C. Liao, C. C. Chen, S. P. McAlister, and C. C. Chi, "Electrical-stress effects and device modeling of 0.18-μm RF MOSFETs", *IEEE Trans. Electron Devices*, vol. 53, no. 4, 2006, pp. 636-642.

[32] S. Nuttinck, G. Curatola, and F. Widdeshoven, "Gate-stack analysis for 45-nm CMOS devices from an RF perspective", *IEEE Trans. Electron Devices*, vol. 53, no. 4, 2006, pp. 925-929.

[33] J. P. Sun, W. Wang, T. Toyabe, N. Gu, and P. Mazunder, "Modeling of gate current and capacitance in nanoscale-MOS structure", *IEEE Trans. Electron Devices*, vol.53, no. 12, 2006, pp. 2950-2957.

[34] B. Ricco, R. Versari, and D. Esseni, "A novel method to characterize parasitic capacitance in MOSFET's", *IEEE Electron Device Letters*, vol. 16, no. 11, 1995, pp. 485-487.

[35] C. H. Wang, "Identification and measurement of scaling-dependent parasitic capacitances of small-geometry MOSFET's", *IEEE Trans. Electron Devices*, vol. 43, no. 6, 1996, pp. 965-972.

[36] R. Torres-Torres, and R. Murphy-Arteaga, "Straightforward determination of small-signal model parameters for bulk-MOSFETs", *Proc. Fifth ICCDCS*, 2004.

[37] D. Lederer, V. Kilchytska, T. Rudenko, N. Collaert, D. Flandre, A. Dixit, K. De Meyer, and J.-P. Raskin, "FinFET analogue characterization from DC to 100GHz", *Solid State Electronics*, vol. 49, pp. 1488-1496.

[38] R. P. Jindal, "Compact noise models", *IEEE Trans. Electron Devices*, vol. 53, no. 9, 2006, pp. 2051-2061.

[39] E. Bouhana, P. Sceer, S. Boret, D. Gloria, G. Dambrine, M. Minondo, and H. Jaouen, "Analysis and modeling of substrate impedance network in RF CMOS", *IEEE ICMTS*, 2006.

[40] A. Goswami, A. Agrawal, S. Bose, S. Haldar, M. Gupta, and R. S. Gupta, "Substrate-effect-dependent scattering parameter extraction of short-gate-length IGFET for microwave frequency applications", *Microwave and Optical Tech. Letters*, vol. 24, no. 5, 2000, pp. 341-348.

[41] Yo-Sheng L., and Shey-Shi L., "Theoretical analysis of the anomalous dips of scattering parameter S_{22} in deep sub-micrometric MOSFETs", *Microwave and Optical Tech. Letters*, vol. 36, no. 3, 2003, pp. 193-200.

[42] Yo-Sheng L., and Shey-Shi L., "An analysis of the kink phenomenon of scattering parameter S_{22} in RF power MOSFETs for system-on-chip (SOC) applications", *Microwave and Optical Tech. Letters*, vol. 36, no. 5, 2003, pp. 371-376.

[43] Y. Taur, and T. H. Ning, "Fundamentals of modern VLSI devices", *Cambridge*, 1998.

[44] Official web-site of the BSIM3/BSIM4 models:
www-device.eecs.berkeley.edu/~bsim3.

[45] K. K. Ng, and W. T. Lynch, "Analysis of the gate-voltage-dependent series resistance of MOSFET's", *IEEE Trans. Electron Devices*, vol. ED-33, no. 7, 1986, pp. 965-972.

[46] Seong-Dong K., Cheol-Min P., and J.C.S. Woo, "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime-part I: theoretical derivation", *IEEE Trans. Electron Devices*, vol. 49, no. 3, 2002, pp. 457-466.

[47] Seong-Dong K., Cheol-Min P., and J.C.S. Woo, "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime-part II: quantitative analysis", *IEEE Trans. Electron Devices*, vol. 49, no. 3, 2002, pp. 467-472.

[48] K. Y. Lim, and X. Zhou, "A physically-based semi-empirical series resistance model for deep-submicron MOSFET *I-V* modeling", *IEEE Trans. Electron Devices*, vol. 47, no. 6, 2000, pp. 1300-1302.

[49] H. T. Kim, I. C. Nam, K. S. Kim, K. H. Kim, J. B. Choi, J. U. Lee, S. W. Kim, G. C. Kang, D. J. Kim, K. S. Min, D. W. Kang, and D. M. Kim, "Extraction of source and drain resistances in MOSFETs using parasitic bipolar junction transistor", *Electronics Letters*, vol. 41, no. 13, 2005, pp. 772-774.

[50] P. M. Solomon, D. J. Frank, J. Jopling, C. D'Emic, O. Dokumaci, P. Ronsheim, and W. E. Haensch, "Tunnel current measurements on p/n junction diodes and implications for future device design", *Proc. IEDM*, 2003.

[51] K. R. Kim, D. H. Kim, Ki-Whan S., G. Baek, H. H. Kim, J. I. Huh, J. D. Lee, and Byung-Gook P., "Silicon-based field-induced band-to-band tunneling effect transistor", *IEEE Electron Device Letters*, vol. 25, no. 6, 2004, pp. 439-441.

[52] M. Bao, and K. L. Wang, "Accurately measuring current-voltage characteristics of tunnel diodes", *IEEE Trans. Electron Devices*, vol. 53, no. 10, 2006, pp. 2564-2568.

[53] D. Flandre, J.-P. Raskin, and D. Vanhoenacker-Janvier, "SOI CMOS transistors for RF and microwave applications", *Int. J. of High Speed Electronics and Sys.*, vol. 11, no. 4, 2001, pp. 1159-1248.

[54] S. Barker, and T. Weller, "A guest editorial look at RF-MEMS", *IEEE Microwave Magazine*, vol. 8, no. 6, 2007, pp. 6-8.

[55] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design", *IEEE J. of Solid-State Circuits*, vol. 40, no. 1, 2005, pp.144-155.

[56] Han-Yu C., Kun-Ming C., Guo-Wei H., and Chun-Yen C., "Small-signal modeling of SiGe HBTs using direct paramter-extraction method", *IEEE Trans. Electron Devices*, vol. 53, no. 9, 2006, pp. 2287-2295.

[57] A. Aktas, and M. Ismail, "Pad de-embedding in RF CMOS", *IEEE Circuits and Devices*, vol. 17, no. 3, 2001, pp. 8-11.

[58] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization", *Proc. IEEE Bipolar Circuits Technol. Meeting,*1991.

[59] H. Cho, and D. Burk, "A three step method for the de-embedding of high frequency S-parameter measurements", *IEEE Trans. Electron Devices*, vol. 38, no. 6, 1991, pp. 1371-1375.

[60] E. P. Vandamme, D. M. M.-P. Schreurs, and C. V. Dinther, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures", *IEEE Trans. Electron Devices*, vol. 48, no. 4, 2001, pp. 737-742.

[61] R. Torres-Torres, R. Murphy-Arteaga, and J. A. Reynoso-Hernández, "Analytical model and parameter extraction to account for the pad parasitics in RF-CMOS", *IEEE Trans. Electron Devices*, vol. 52, no. 7, 2005, pp. 1335-1342.

[62] T. E. Kolding, "Shield-based microwave on-wafer device measurements", *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 6, 2001, pp. 1039-1044.

[63] T. Kaija, and E. O. Ristolainen, "An improved model for ground-shielded CMOS test fixtures", *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 1, 2006, pp. 82-87.

[64] T. E. Kolding, "Test structure for universal estimation of MOSFET substrate effects at gigahertz frequencies", *Proc. ICMTS*, 2000.

[65] S. Lee., C. S. Kim, and H. K. Yu, "A small signal RF model and its parameter extraction for substrate effects in RF MOSFETs", *IEEE Trans. Electron Devices*, vol. 48, no.7, 2001, pp. 1374-1379.

[66] Yo-Sheng L., and Shey-Shi L., "An analysis of small-signal substrate resistance effect in deep-submicrometer RF MOSFETs", *IEEE Trans. Microwabe and Tech.*, vol. 51, no. 5, 2003, pp. 1534-1539.

[67] U. Mahalingam, S. C. Rustagi, and G. S. Samudra, "Direct extraction of substrate network parameters for RF MOSFET modeling using a simple test structure", *IEEE Electron Device Letter*, vol. 27, no. 2, 2006, pp. 130-132.

[68] S. F. Tin, A. A. Osman, K. Mayaram, and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design", *IEEE Jour. Solid-State Circuits*, vol. 35, no. 4, 2000, pp. 612-624.

[69] R. Torres-Torres, and R. Murphy-Arteaga, "Enabling a compact model to simulate the RF behavior of MOSFETs in SPICE", *Int. Jour. RF and Microwave Computer-Aded Engineering*, vol. 15, no. 3, 2005, pp. 255-263.

[70] Jin-Young C., and J. G. Fossum, "Analysis and control of floating-body effects in fully depleted submicrometer SOI MOSFET's", *IEEE Trans. Electron Devices*, vol. 38, no. 6, 1991, pp. 1348-1391.

[71] K. K. Young, and J. A. Burns, "Avanlanche-induced drain-source breakdown in silicon-on-insulator n-MOSFET's", *IEEE Trans. Electron Devices*, vol. 35, no. 4, 1988. pp. 426-431.

[72] S. M. Sze, "Semiconductor devices; physics and technology", *John Wiley & Sons*, 1985.

[73] E. Torres-Rios, R. Torres-Torres, G. Valdovinos-Fierro, and E. A. Gutiérrez-D., "A method to determine the gate bias-dependent and gate bias-independent components of MOSFET series resistance from *S*-parameter measurements," *IEEE Trans. Electron Devices*, vol. 53, no. 3, 2006, pp. 571-573.