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Electronics Department

A Methodology for Modeling Vias in High-Speed Interconnects Including Electromagnetic Radiation Effects

by

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Abstract

Nowadays, RF electronics systems are demanding high performance operating frequencies and compactness. Integration approaches, as system on package, have emerged as a reliable solution because it is based on multilayer technology using low-cost and high-performance materials. Nevertheless, these systems use vertical interconnects, especially vias, to connect several traces and devices through different layers. For this reason, studying the performance of these interconnects is mandatory these days for optimizing the corresponding structures. However, as the frequency of operation of the electronics systems increases this task has become more complicated due to the high-order effects that occur within vias carrying signals at these frequencies. In this regard, the purpose of this thesis is the study and characterization of the high-order effects occurring in vias. Consequently, a new topology for the characterization of vias embedded in dielectric substrates surrounded by ground vias is presented as a result of this thesis.

Chip design as well as fabrication technologies have experienced a tremendous evolution in recent years, whereas package design at this time barely starts to evolve. In fact the delay associated with vias embedded in packages is reaching unacceptable levels letting current electronic systems unable to handle high-frequencies signals, becoming vias the bottleneck when designing high-speed interconnection channels. For this reason, package performance at high frequencies has to improve by identifying the effects that negatively influence the corresponding electrical performance. In order to do this, equivalent circuit models for packages can be used in the analysis to carry out an optimization of the interconnection channel.

Thus, within this project several prototypes were fabricated to carry out an exhaustive analysis of the origins of high-order effects which degrade the signals in practical interconnection channels implemented in PCB technology. This analysis includes not only experimental studies of these structures, but also full-wave simulations of the 3D-models corresponding to these structures correlating both approaches.

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A mis padres Miguel y Cristina con todo mi amor

y a mi novia Carolina

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Preface

Current requirements for data processing have made the electronic systems to trend toward faster and higher density devices. In this regard, multilayer structures have become a reliable solution to deal with these difficulties. However, interconnection channels embedded in these structures are reaching its limits. In fact, as clock rates present in modern PCs continue to rise into the gigahertz range, data rates requirements are in the tens of gigabits per second. Thus, high-order effects that become apparent at these frequencies need to be considered. For this reason, the fabrication of interconnects and packages capable to guide broadband signals without degrading the signal integrity to unacceptable levels is necessary.

This project started last year; however, it is the result of more than three years of research in the field of package modeling in INAOE. Several techniques to represent and characterize signal vias embedded in dielectric substrates surrounded by ground vias have been studied and analyzed, allowing also proposing a new model and a reliable parameter extraction method for circuit-oriented modeling of vias embedded in dielectrics substrates. In addition, as a result of this project one article has been submitted to an international refereed magazine.

I have written this thesis under the genuine belief that it can serve as a guide for the implementation of reliable high-frequency package models, but also to motivate scientific research in the field of package design in Mexico, which is one of the emerging research areas in the world.

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July 2010

Chapter 1

Introduction

Current requirements for faster data processing have originated that much effort behind the development of new assembling approaches is focused on the reduction of the size and weight, and on improving the performance of the electronics systems. In this regard, reducing the parasitics associated with interconnects as well as using multi-leveled systems for placing different types of circuitry have been proposed for achieving these improvements. For this reason, the correct design of the interconnects between the different system levels results in better matching for avoiding signal leakages.

For implementing high-performance electronics systems at a relatively low cost, printed-circuit-board (PCB) technology has been widely used in the electronics industry for many years. However, the ever increasing speed of the data processing introduces undesirable effects that degrade the integrity of the transmitted signals. Hence, in order to design optimal interconnects, not only the line impedances should be matched, but also the corresponding electrical transitions so that the return loss can be reduced. For this reason, much research has been carried out for the correct design of interconnection channels. This suggests that the improvement of transmission line interconnects is an important field of opportunity for microwave engineers.

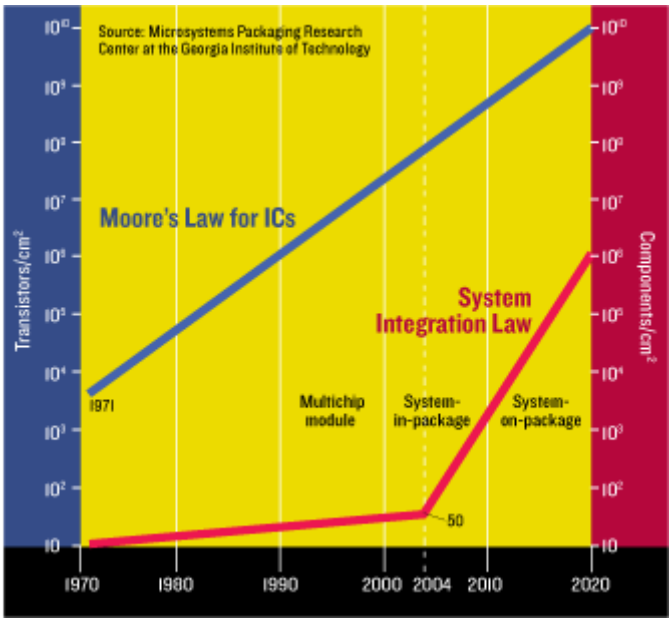


Fig. 1.1 Moore's Law predicting the number of transistors found in an IC [1].

As is well known, the number of transistors within an integrated circuit (IC) increases in accordance to Moore's Law [2], which is depicted in Fig. 1.1. Since this scaling prediction can also be applied to data processing, Moore's law can be used to

predict the bandwidth requirements for interconnects, which has recently reached the range of tens of gigahertz in computing applications.

Until recently, interconnects used in ICs have provided adequate bandwidths preserving the integrity of the signals. However, as clock rates continue to rise within the microwave range, problems associated with the electrical transitions between transmission lines are becoming apparent, such as distortion, resonances, crosstalk, and radiation. Furthermore, the complexity of the advanced structures and the increased density of the devices complicate the corresponding analysis as well as the design tasks. These are some of the reasons why the correct characterization and modeling of the electrical transitions present in current interconnection channels become mandatory from a signal integrity point of view.

1.1 Vertical Interconnects

In multilayer PCB as in any other technology for integrating systems, it is desirable to interconnect transmission lines located at different layer levels. For this reason, vertical interconnects are commonly found on these technologies. These transitions can be used as an interface between chips and boards, and are considered an important part of interconnection channels. This type of interconnects are usually found in ball grid arrays (BGA), pin grid arrays (PGA), land grid arrays (LGA), wire bonds, solder bumps, sockets and vias. These vertical interconnects are depicted in Fig. 1.2.

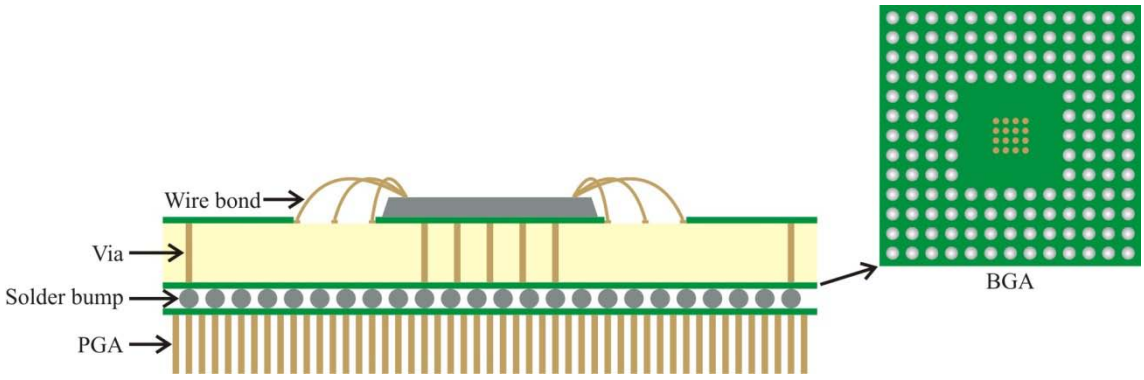


Fig. 1.2 Vertical interconnects.

Vias are vertical interconnects that are present in almost all technologies for fabricating electronics circuits, and their main function is to carry signals from one level or layer to another. Generally, vias are used in multilayered PCBs to reach high-density interconnection [3]. Vias typically consist of a barrel, a pad, and an antipad as can be seen in Fig. 1.3 [4]. The most common type is the through-hole via, which is a hole drilled trough the PCB that is filled with metal in order to achieve connection; other types of vias are the blind via, the step via, the buried via, the stacked via, and the microvia. These vias are depicted in Fig. 1.4. For particular applications, the correct choice for the type of via, which will be employed in a multilayered PCB, determines important properties of the system such as the size of the substrate, the interconnection density and others [3].

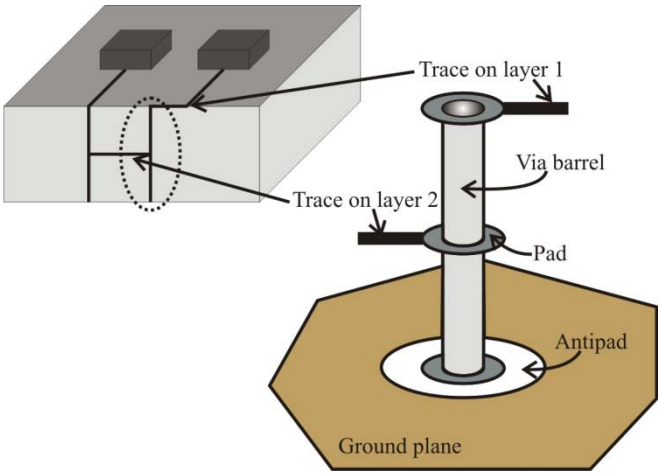


Fig. 1.3 Example of a through-hole via: the antipad avoids the connection between the via and the ground plane.

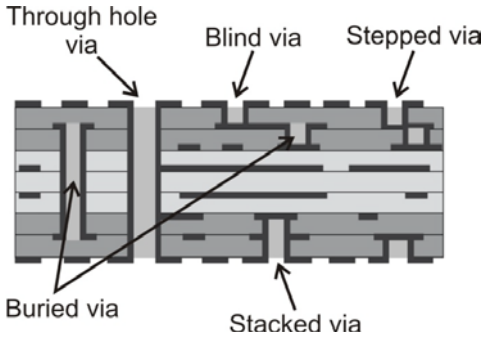


Fig. 1.4 Different types of vias in multilayer technology.

The most common way to fabricate vias is using mechanical drill. However, mechanically-drilled vias are limited to diameters down to approximately 150 microns. Below this diameter, the production cost becomes very expensive due in part to the deterioration of the drill bit. For this reason, alternative methods for fabricating vias have been proposed, and include [3]:

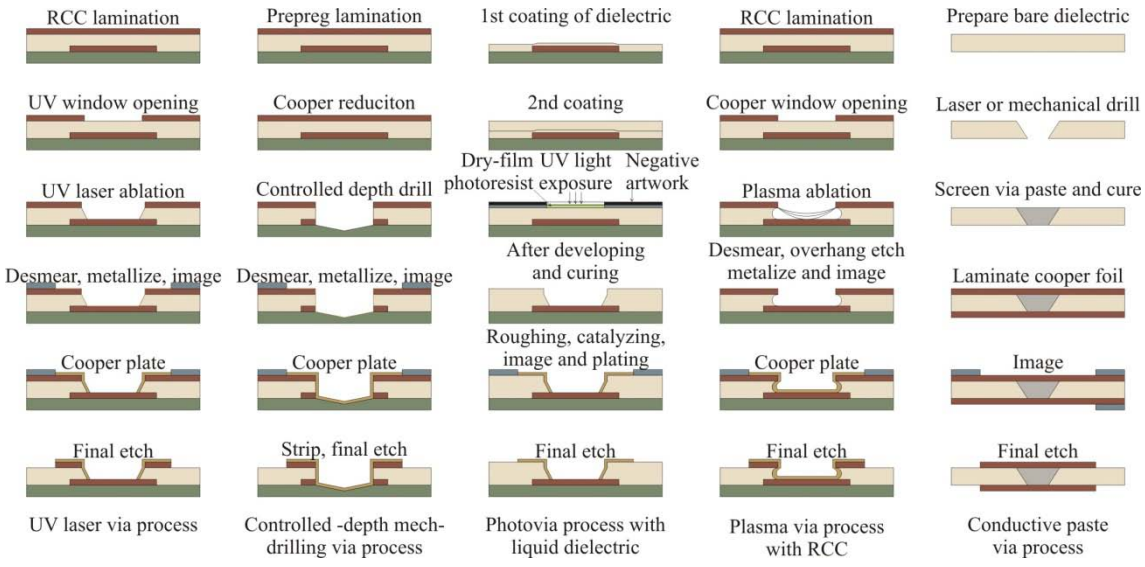


Fig. 1.5 Methods of via generation [3].

- *Laser via technology*. Is the most microvia hole formation. The wavelengths for laser energy are in the infrared and ultraviolet region. Laser drilling requires programming the beam fluence size and energy. High-fluence beams can cut metal and glass, whereas low-fluence beams remove organics without damage metals. The laser is the most common method of production of microvias to be plated or filled with a conductive paste. For UV laser via process, first a laminate of resin-coated cooper (RCC) is deposited over the dielectric. After that, a window opening is made and a UV laser beam removes part of the dielectric in the site where the via is desired. Then, a desmear process is made to remove via formation residues from via interconnects and via capture pads in order to affect a tightly adherent bond of the subsequent metallized coating. Afterward, a cooper plate is adhered to the surface and a final etch is made to have the via process complete.
- *Mechanically drilling blind via technology*. Mechanical drilling has traditionally been the most widely practiced method for hole creation. This process is anisotropic, whereas many of non-drilling processes are not. That is, the vertical walls are straight up and down. In this process, once the board has the proper widths for the materials a controlled depth drill is made by means of bit. After that, a desmear process is made followed by a metallized and image process. Afterward, a cooper plate is adhered to the surface and a final etch is made to have the entire via process.
- *Photo process defined vias*. This is one of the oldest method for performing microvias. The process starts with a bare core which has to be treated with an adhesion promotion process to ensure good adhesion of dielectric material to the cooper surface. After that, dielectric resin is semicured after coating to eliminate tackiness, and then the hole pattern is exposed by photo exposure processing. Afterward, an etching process is made to remove any residual resin at the bottom of the hole and simultaneously create microporus surfaces to ensure desirable peel strength after cooper plating.
- *Plasma via technology*. This process is mainly used to fabricate sophisticated flex and flex-rigid wiring boards in small quantities. First, an opening or window is made through copper foil by a normal etching process. When plasma etching is applied through this window, the shape of the hole tends to be like a bowl. Due to this, the cooper edge of the window hangs out over the hole, which results in poor reliability after panel plating. Therefore, a secondary etching is necessary to remove this cooper overhang. Nevertheless, with this secondary etching is that since surface cooper is thinned, formation of finer conductors is easier. Finally cooper plate and final etch processes are needed to conclude the via formation.
- *Insulation displacement*. Three types of dry metallization are insulation displacement, conductive ink, and conductive paste. In this process the conductive paste forms a spike that penetrates microvias made before in the dielectric formed by photoimaging, laser, or mechanical drill. This conductive

paste acts as the conductive path between layers. Surface metallization may be accomplished either by laminating cooper foil onto the dielectric surface or by chemical deposition.

1.2 Applications of Vias

As mentioned above, the term *via* commonly refers to an opening formed in a dielectric layer or substrate and metallized to create an electrical connection between two or more conductor layers [3]. Due to the enhancement in speed, density, and routing complexity in IC design, vias are extensively used to connect signal traces within different layers. However, this is not the only purpose of vias. These vertical interconnects are also used for short-circuiting metal planes to keep the potential as close as possible between layers [5]. This application is very important since the performance of many integrated circuits is affected by the differences in the incoming voltage levels. For instance, the speed of the core blocks in a PC processor may be function of the applied voltage. Another common application is when vias are used as plug-in receptors for mounting a through-hole component to a board or other modules [4]. In this case, the hole has one leg of a component soldered into it. In other applications vias are used for routing signals within paths that behave electrically in a similar way [4]. One recently explored application is for exciting waveguides [7, 8]. Thus, a metal via embedded between waveguides serve as launcher/receiver of transmitted signals, acting as the terminals of the waveguides [9].

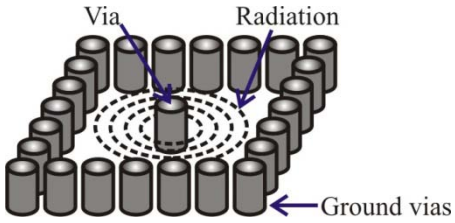


Fig. 1.6 Signal via surrounded by ground vias. Since signal vias do not have a reference plane with which it support well-guided electromagnetic waves, at the moment for routing a signal it will radiate causing undesired high-order effects.

Another important aspect to be mentioned is that vias may also introduce undesired effects when interconnecting transmission lines at different levels, Fig. 1.6. In this case, vias induce propagation in high-order modes when routing signals from one level to another. This effect is seen as a leakage of signal, which is obviously undesired. For understanding this effect, a via may be seen as a discontinuity were mode conversion is likely to occur. Mode conversion is the phenomenon of the reconfiguration of the electromagnetic fields at the discontinuities [13, 14]. This is an adverse effect when a via is used as a vertical interconnection, but can be used on purpose for exciting certain modes in waveguides or to provide smooth transitions between different waveguides. Since vertical plates cannot be made on current PCB technology, rectangular waveguides are not reliable on this technology. In this regard, synthetic rectangular

waveguides known as substrate integrated waveguides (SIW) are used. It basically consists of two parallel conductor planes short-circuited by means of a ground vias array. Fig. 1.7 shows one example of this last application in which one via is carrying a signal and radiation occurs, causing propagation in an SIW whereas another via collects the electromagnetic fields carried in this mode for recovering the information.

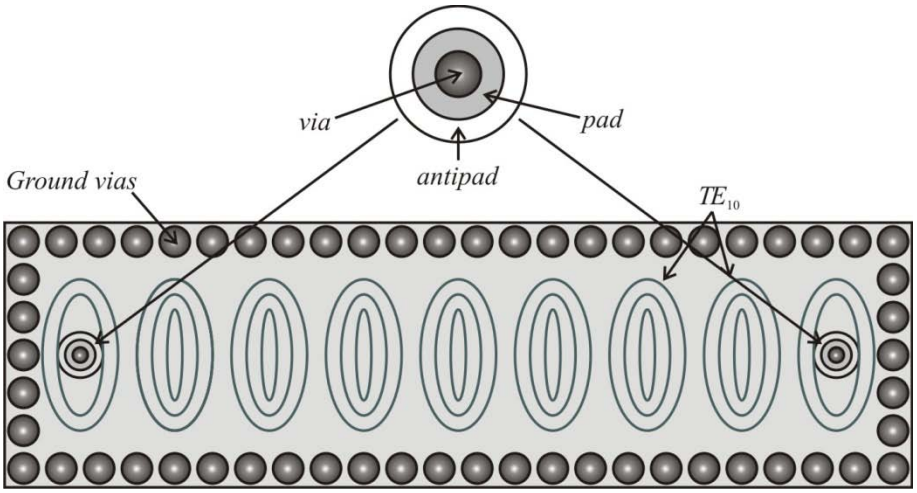


Fig. 1.7 A via carrying a signal through an SIW will present radiation due to the discontinuity, inducing propagation of the signal through the waveguide. The signal is transmitted in the fundamental mode TE_{10} through the SIW, whereas another via located at the left side of the SIW acts as a monopole antenna collecting the electromagnetic fields recovering with that the information.

Notice that for this last application, the propagation of waveguide modes is desirable. However, this effect is present when vias route signals into an interconnection channel, and part of the energy is lost due to radiation. This undesirable radial transmission will be discussed in Chapter 2.

1.3 High-Frequency Effects

An increasing interest in the electromagnetic effects associated with vias in high-speed interconnect designs has been recently observed. Since vias do not have simple and symmetrical reference plane such as that associated transmission lines, these vertical interconnects cannot guide electromagnetic waves in a regular and well defined forms [15], see Fig. 1.6. For this reason, high return-loss occurs and the signal integrity is affected when propagating through vias as well as through the transitions from the vias to signal traces. Moreover, as clock speeds continue to rise into the microwave frequency range, problems such as crosstalk, resonances, and radiation that are intrinsic to vias are becoming increasingly difficult to overcome [10]. These effects are closely related to the physical structure of the vias. For instance, the aperture between the pad and the plane forms a parasitic via-to-ground capacitance, whereas the barrel of the via introduces a parasitic inductance, which greatly affect the coupling of these interconnects within a composite channel. These negative effects can be reduced by changing the via dimensions; for example, a small via pad will represent a relatively

small capacitance, whereas a short-length via will represent a low inductance. It is important to mention that the effects originated by the vias cause unexpected impedance discontinuities that originate transmission issues, whereas the capacitance also slows down the rising time of the propagated digital signals. Although both effects degrade the signal transmission, the inductance effect is more accentuated in the via design and there are some actions that can be taken in order to minimize it; for example [11]:

- Upper layers must be designated for high-priority supplies.
- Avoid the use of long vias which can have a stub behavior.
- Shorten the distance in which the current has to travel through the via.
- Placing ground planes in order to shield the transmission and avoid parasitic propagation at high frequencies.
- Reduce the number of layers in which high-speed signal traces has to be routed, thus limiting the number of vias employed.

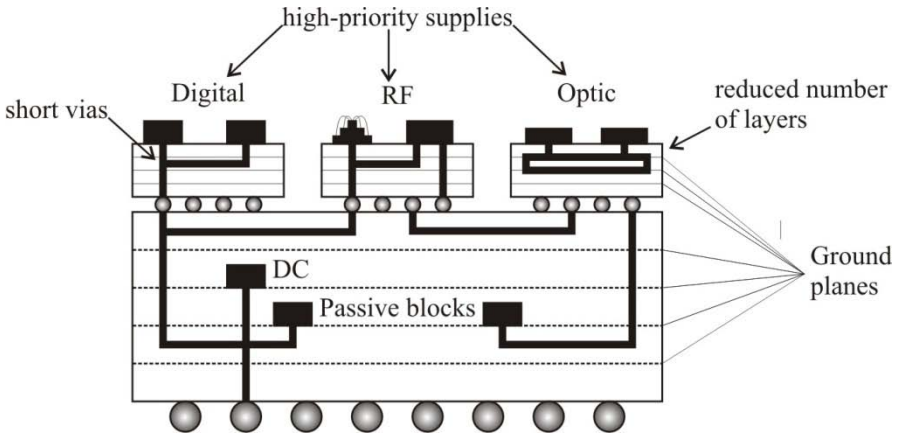


Fig. 1.8 Example of the actions that must be considered when vias are involve in the IC design.

Recently, the study of high-frequency effects associated with vias has received particular attention due to their widely use in the integration of the systems. In fact, the concepts introduced by system-on-package (SoP) demands this study [12], this is because electromagnetic interference (EMI), which is caused by radiating vias, can degrade the signal integrity to the point of letting the interconnection channel useless.

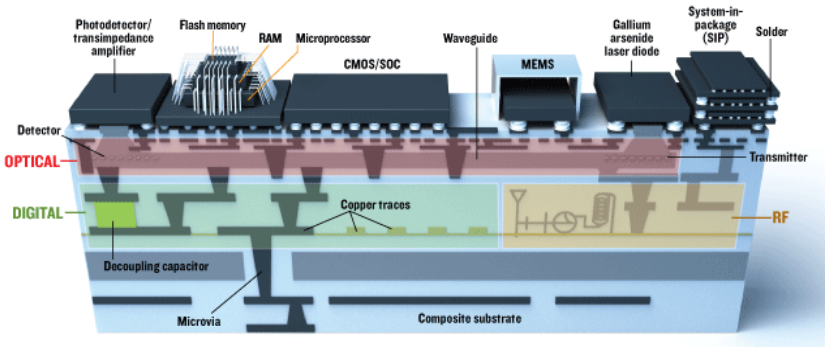


Fig. 1.9 Illustration of a system-on-package test bed that combines three types of circuits in its dielectric layers. Vias are the vertical interconnects between those layers [1].

1.4 Modeling of Vias

In order to estimate the impact on signal and power integrity, as well as the EMI effects caused by vias in printed circuit boards and other electronic components, there is a need for modeling tools. At present, there are three main types of approaches for modeling vias; some of the most representative are [17]:

- *Circuit-oriented*: Modeling the structures with equivalent-circuit networks, which are analyzed using SPICE-like simulators.
- *Analytical* (compact): Solution of Maxwell´s equation for the dominant mode of a radial waveguide and derivation of the pertinent transfer and driving point impedances.
- *Full-wave solvers*: Derivation of Green's function of a resonant cavity to model the finite substrate with the correct boundaries plus the derivation of the port impedances, or direct 3-D numerical solution of Maxwell's equations using frequency or time-domain full-wave techniques such as finite-element-method (FEM) and transmission-line method (TLM).
- *Hybrid* methods: Combination of more than one of the previous methods. Combining full-wave simulations, analytical solution, or measurements results with circuit simulations. Moreover, by processing the data obtained from full-wave analysis, analytical solutions, or measurements to extract circuit models and perform subsequent simulations.

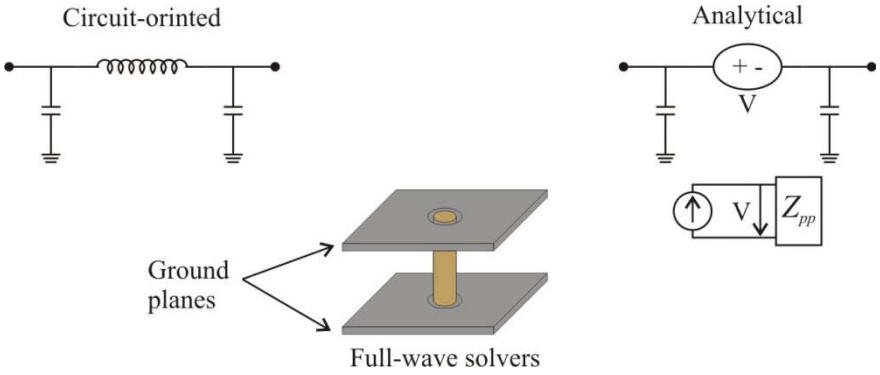


Fig. 1.10 Different models for vias.

When using equivalent circuits, vias are typically modeled with a lumped π-model, including the inductive and capacitive effects. This model (shown in Fig. 1.6) is valid when the time delay associated with the via is considerably larger than the edge rate associated with the signal [6]. In this model, each lumped element represents a parasitic effect physically observed in the structure. An inductance that accounts for the via barrel, and two via-to-ground capacitances consider the displacement currents from the via to the top and bottom planes [13].

For the case of a compact model, the basis is the same as above, but the parasitics of the via are calculated from closed-equations [6] and is extended by a model for the parallel planes. In this model the effect of the parallel planes is achieved by a voltage

noise travelling against the signal path [14], by means of a terminated-waveguide-like impedance Z_{pp}. This impedance is used to describe the return path of the via current, and can be calculated using the cavity model or boundary element method (BEM) [5]. However, the via itself is not accurately modeled since the boundary condition on the via barrels is not rigorously enforced.

Finally full-wave modeling tools, such as High Frequency Structure Simulator (HFSS), CST Microwave Studio, Momentum etc, can be used to simulate vias transitions in typical PCB boards. The main advantage of full wave modeling tools is the high accuracy of the results. Whereas, the two main disadvantages of full-wave modeling tools is the time consumption together with the limitations on the complexity of the model due to the available computer resources. In addition, calibrating a 3D model for performing full-wave simulations is a tough task due to the large amount of material and geometry parameters that have to be considered, which are also in most of the cases frequency dependent. However, full-wave simulations are widely used as a validation standard for the different approaches.

1.5 Purpose of This Work

As mentioned in this chapter, the advances in multilayer technologies for implementing electronic systems are remarkable. For this reason, the aim of this work is contributing to the study of signal integrity issues presented on PCB through the analysis and modeling of high-order effects occurring in via transitions. This is supported with an exhaustive and systematic model-experiment correlation by means of a theoretical understanding of the physical phenomena occurring in these transitions. Once this is achieved, an equivalent circuit model and the corresponding parameter extraction is proposed for via transitions embedded in dielectric substrates and surrounded by electric-wall boundaries. The results of this project can be used for either designing or analyzing the radiation occurring in vias used at microwave frequencies.

1.6 Description of this Document

This thesis is organized as follow. Chapter 2 presents the high-order effects occurring in vias, which includes the study of the horizontal radiation associated with vertical interconnects, as well as the interaction between signal and ground vias (i.e. effects on packages). Chapter 2 also presents a brief overview on substrate integrated waveguides (SIWs), and some theoretical basis useful in the design of the proposed topology. Chapter 3 presents the electromagnetic modeling of via interconnects. In this chapter, the description of the methodologies employed in this work, and the determination of the effective length in SIWs is detailed. Chapter 4 presents the comparison between experimental results and equivalent circuit modeling used in the proposal. Finally, chapter 5 presents the general conclusion of the approach presented in this thesis.

Chapter 2

High-Order Effects in Vias

As the operating frequencies increase and the working voltage decreases in high-speed digital systems, modeling and designing power/ground planes is becoming more and more important. In PCBs, the power and ground planes essentially form parallel plate waveguides that provide a noise coupling path, which can lead to signal integrity problems [23]. In fact, the noise coupled through the parallel planes can also radiate at the edges of the planes due to the fringing fields, and can couple nearby structures, resulting in electromagnetic interference (EMI) problems. Therefore, a good design of the power/grounds planes is essential to preserve the signal integrity and to reduce the risk of EMI problems. Fig. 2.1 shows a basic example of these problems. When a via is routing a signal through a parallel plate environment, radiation in a parasitic mode is likely to occur above certain frequencies; thus, another via carrying the same (or even a different) signal will receive the parasitic propagated energy, resulting in multimode propagation. As is well known, this multimode propagation affects considerably the signal integrity in a high-speed channel due to dispersion.

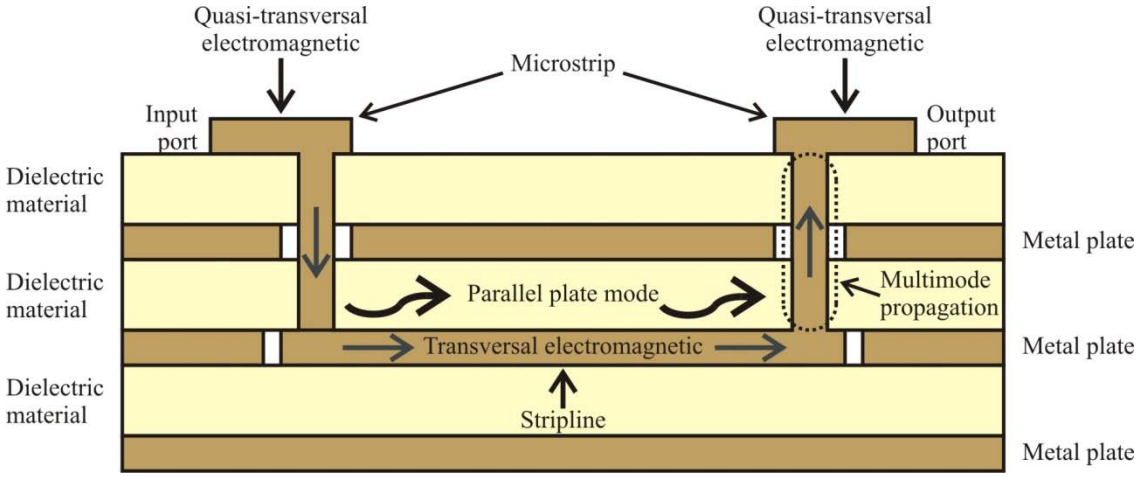


Fig. 2.1 Sketch of the side view of a multi-layer substrate showing the undesired coupling in a simple interconnection channel.

The parasitic mode propagation is one of the main studied effects in high-speed interconnection channels [23–25] and will be discussed in this chapter. With this, a clear idea of the effects that may occur in complex transitions such as packages is provided.

2.1 Vertical Interconnect – Horizontal Radiation

Current PCB and package structures are built in low-loss substrates to reduce the electric losses [23]. However, low-loss dielectrics and parallel metal planes used as

ground-planes in interconnects are the ideal environment to develop second order effects, such as via radiation, which is very common in packages [26]. Via radiation causes that part of the signal leaks away from the desired propagation path originating a partial loss of the signal power. Fig. 2.2 shows this effect. In this case, the parasitic propagation is radial with a magnitude that decreases with the distance from the via. This effect is also common in PCB structures. For this reason, the analysis of this type of parasitic propagation is necessary to improve the performance of interconnects that contain vias and multilayer planes [25].

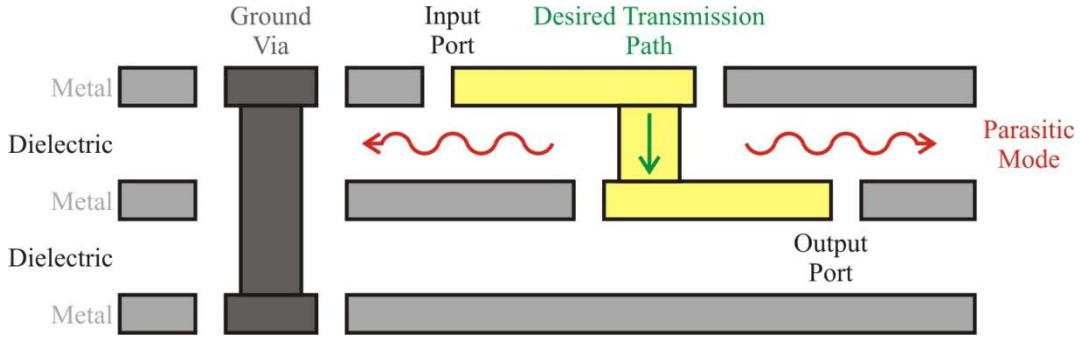


Fig. 2.2 Sketch of the side view of a package that conceptually illustrates the origin of the PPM excitation.

A. Resonances

Second order effects caused by vias, such as the parasitic mode propagation, may originate ground bouncers or simultaneous switching noise (SSN) within packages [27, 28]. For this reason, the proper design of vias and the corresponding environment is very important when optimizing packages. Furthermore, SSN and a high *Q* of the resonator formed between the parallel planes facilities the presence of resonances [28]. In general, these resonances are caused by the fact that the parasitics associated with a transition may behave as a reflective element (i.e. either an open or a short circuit). In this case, the transition can be seen as an energy-storage structure at given frequencies. In practical cases, the performance of packages may be severely degraded as a result of ring and cavity resonances [28]. Ring resonances occur when parallel plate modes are coupled with other structures at the edges of the package [29, 30], whereas cavity resonances occur when the package behaves as a rectangular cavity [31]. These resonances originate large spikes in the insertion-loss versus frequency curves, similar to those observed in the response of a notch filter (see Fig. 2.3). The presence of a second resonance is result of the propagation of higher order modes, which have a higher cutoff frequency than the principal mode of propagation. For this reason, the insertion loss is lower in the second resonance than in the first resonance. In particular, this second order effect causes huge damage to the performance of high-speed interconnection channels, and is considered one of the worst effects introduced by vias [32].

As mentioned above, the edges of the parallel planes are one factor that is involved in the occurrence of resonances. Thus, when an electromagnetic wave traveling in a

parasitic mode reaches the edge of the board, part of the energy is radiated outside the structure whereas the other part is reflected back, which is similar to the effects associated with a monopole antenna mounted in a finite size ground plane. In this regard, there exist three main configurations for representing practical structures including parallel planes:

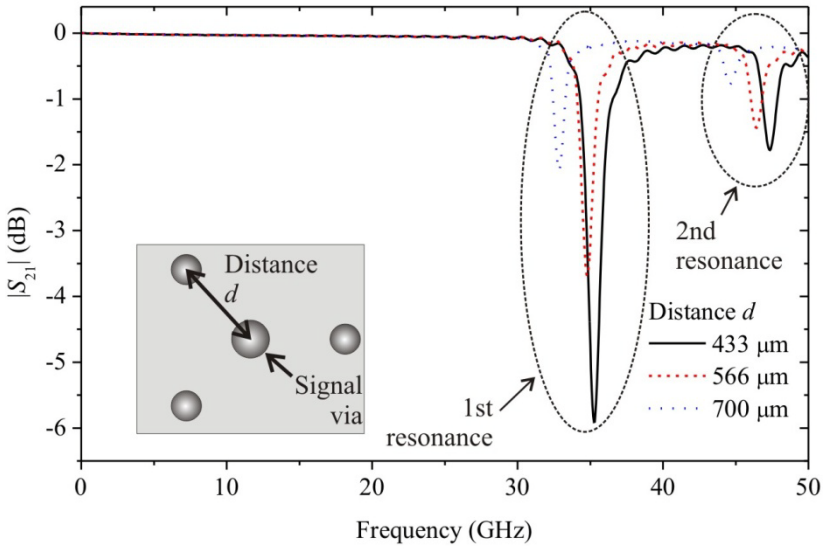


Fig. 2.3 Insertion loss versus frequency curves for a triangle configuration of vias, with a center-to-center distance between the signal and ground vias varying from 433 to 700 microns [32]. As can be seen, resonances occur at certain frequencies causing a loss in the transmission.

- Finite size planes: resonances are likely to occur when the signal propagated in a parasitic plate mode reaches the edge of the board and part of the energy is reflected back. The reflected signal can be added to a new signal if both are in-phase and a resonance occurs, whereas if they are out-phase no resonance is present (see Fig. 2.4).
- Infinite planes: resonances cannot occur since the signal propagated in a parasitic plate mode cannot reach the edges of the board. The same effect is present if the planes are terminated on matched boundaries.
- Electric wall (short circuit boundary): cavity resonances may occur at certain frequencies [28]. Nevertheless, parasitic parallel plate mode is confined and cannot reach the edge of the board avoiding the presence of ringing resonances.

In accordance to the previous discussion, the systematic design of the electrical transitions plays a key role in achieving performance for an interconnection channel. So, different techniques can be used to reduce the impact of the undesired effects introduced by vias; among these are [4, 33]:

- placing a bypass capacitor near the vias (see Fig. 2.5), trying to keep the capacitive coupling between all the reference planes, and maintain the high-frequency traces in the same plane;

- reducing the dielectric thickness so that the parasitic mode propagation occurs at frequencies outside the useful bandwidth, and
- using a proper configuration of the ground via array for maintaining the signal energy confined [32].

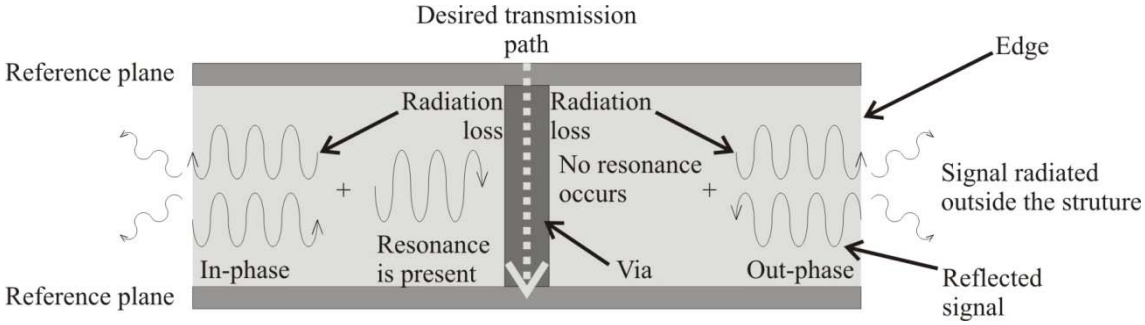


Fig. 2.4 Sketch illustrating the origin of resonances in a via in a multilayer structure. When the traveling signal due to radiation loss reaches the edge of the structure, part is radiated outside the structure and other part is reflected. If traveling and reflected signals are in-phase the resonance is present in the transmission; whereas, if both are out of phase the signals cancel each other and no resonances occur.

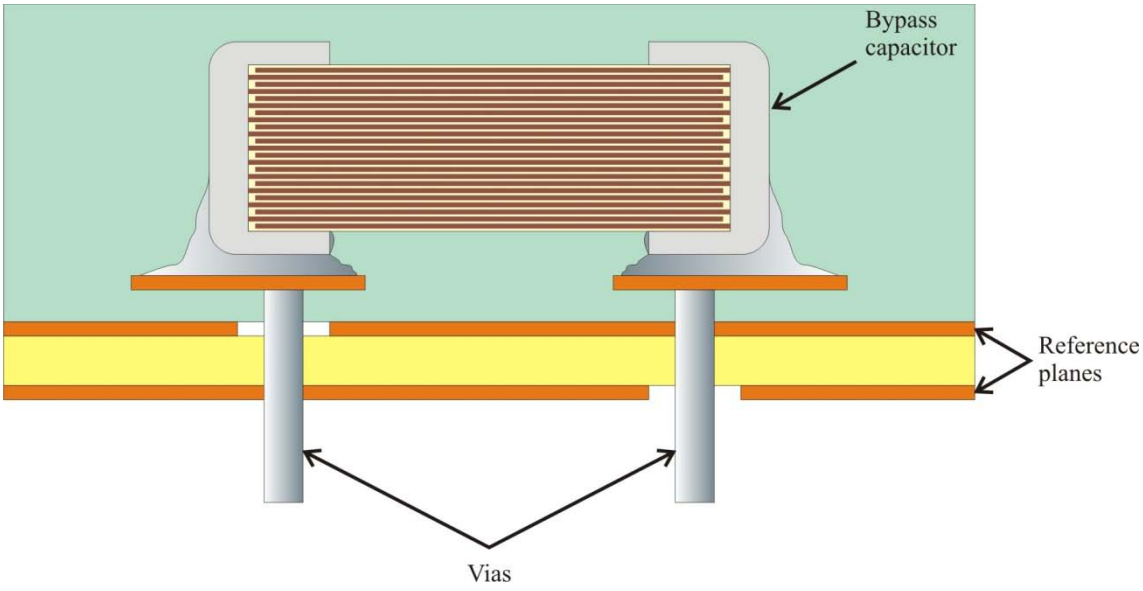


Fig. 2.5 Sketch of a bypass capacitor in the uppermost plane [34].

B. Via as a Monopole Antenna

Since a radiating antenna can be seen as a device that converts electromagnetic waves traveling through a transmission line into waves radiated to free space [20], some similarities between a monopole antenna and a via embedded between multilayered substrates can be noticed. For instance, in an interconnection channel a via may present a similar behavior when routing a signal through multilayer environments and radiation occurs. In fact, in many cases this structure can be modeled as a monopole antenna embedded within a dielectric substrate. Since antennas are inherently bi-directional, they can transmit and receive signals. Thus, at certain frequencies vias embedded in a substrate can be seen as antennas either propagating or coupling parasitic modes,

resulting in EMI problems for the interconnection channel due to the multimode propagation.

In general terms, a monopole antenna is a type of ratio-antenna formed by replacing one half of a dipole antenna with a ground plane (see Fig. 2.6). If the ground plane is large enough, the monopole behaves exactly like a dipole, whereas the missing half of the dipole is formed by the reflection in the ground plane. For the ideal case of a ground plane of infinite extent and infinite conductivity, the monopole antenna can be analyzed using the method of images as a dipole with one half the input impedance and double the peak directivity of the dipole. On the other hand, for an infinite-size ground plane the radiation pattern is exactly the same as in the dipole. Thus, for a monopole element mounted on a ground plane of finite extent, the outer edge of the ground plane diffracts incident radiation in all directions, and consequently modifies the currents on the ground plane. Outer-edge diffraction becomes increasingly significant with decreasing size of the ground plane because of the increasing magnitude of the currents on the ground-plane faces at the outer edge [21].

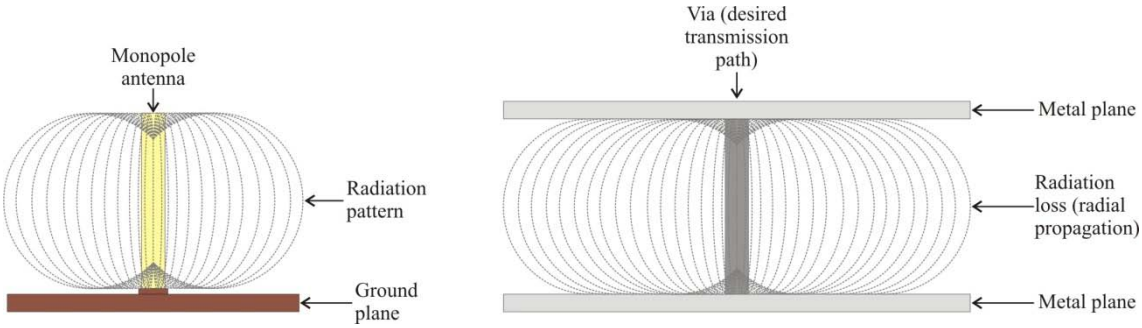


Fig. 2.6 Analogy between a monopole antenna and a via embedded in a substrate.

In accordance to the previous discussion, it can be noticed that similar effects are caused by the edges of the ground plane in a monopole antenna as in the case of via embedded in a substrate. Furthermore, the modeling of a via with a monopole antenna is a reliable solution in the characterization of these vertical interconnects.

2.2 Signal and Ground Vias on Packages

In general terms, a package is a multilayer structure with several vertical transitions that allow the interconnection of bare dies with a PCB [24]. In addition to the signal path, these structures include many ground vias that interconnect different layers for maintaining the same potential. This is achieved by short-circuiting every plane within the package (see Fig. 2.7), which also prevents the propagation of signals in parasitic modes, avoiding energy leakage. Unfortunately, several high-order effects occur in packages due to the complexity of the corresponding design [28]. One of these is the parallel plate mode, which degrades the performance of the interconnection channel in which the package is embedded. In this regard, ground via arrays can also be used to alleviate the resonance problems presented in packages due to the propagation of

parallel plate mode inside it. In fact, in accordance to [32], the presence of resonances varies in a systematic way by changing:

- the distribution of the ground vias around the signal via, and
- the distance between the ground and signal vias.

As the separation between ground vias decreases, resonances occur at higher frequencies and the corresponding penalty in the insertion loss will be smaller. This suggests that as the separation between the ground vias becomes smaller the wavelength of the signals that may leak away the structure will be shorter, which implies that the resonances will occur at higher frequencies. The ideal case to avoid signal leakage is by forming a metallic wall interconnecting the ground planes and surrounding the signal via, which can be implemented in a package by means of closely spaced ground vias (see Fig. 2.8).

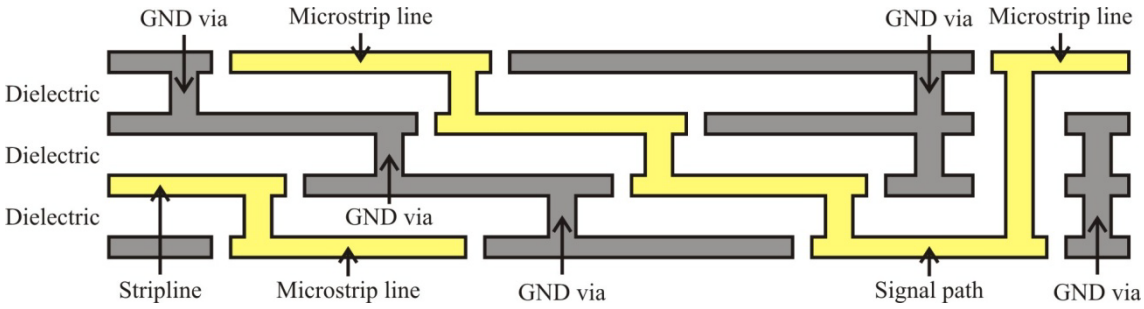


Fig. 2.7 Side view of the basic structure of a generic package.

Bear in mind, however, that placing ground vias inside packages introduces new boundary conditions for the structure, which in some cases originate a waveguide behavior. Fig. 2.8 illustrates a case in which ground vias form waveguide paths around a vertical transition within a vertical transition in a package. For this reason, in order to prevent the propagation of electromagnetic waves in parasitic modes within the packages, ground vias must be placed as close as possible to the signal via in such a way that the cutoff frequency of the fundamental waveguide mode is sent to frequencies that are outside the useful bandwidth.

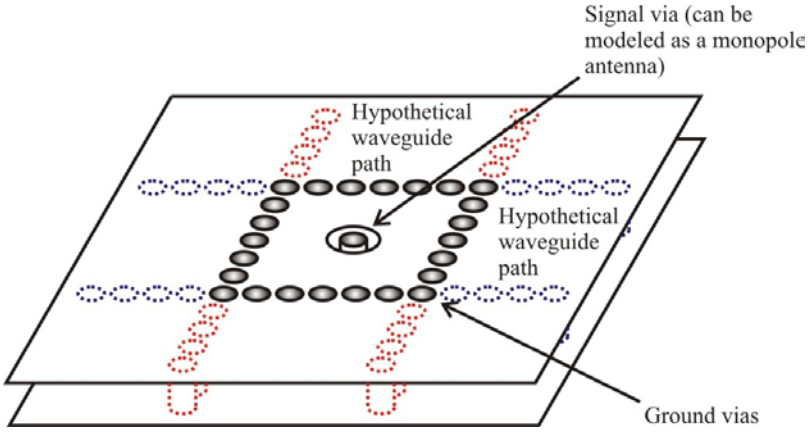


Fig. 2.8 Structure of a vertical interconnect including one signal via and several ground vias. Notice also the hypothetical SIWs that may lead to undesired horizontal propagation.

2.3 Substrate Integrated Waveguides

Fig. 2.8 points out the similarities between packages and rectangular waveguides. In this regard, the electric wall formed by the ground via arrays can be seen as the walls of a rectangular waveguide, whereas the metallic post located at the middle of the package acts as a monopole antenna exciting such a waveguide [8]. For this reason, waveguides can be used to study the propagation of parasitic modes in environments such as those of packages, as well as the impact of high-order effects on it.

The way to form a rectangular waveguide in current PCB technology is by placing parallel metal plates on top and bottom of a dielectric slab and two sidewalls of metallic posts. This structure is the so-called substrate integrated waveguide (SIW) [8]. Thus, the metallic posts at the sidewalls of SIWs present similar characteristics to those of a ground via array within a package. Fig. 2.9 depicts the basic structure of this microwave element. In an SIW, when the posts of the sidewalls are placed close enough to avoid or at least to keep the leakage of the signal to a minimum level, the structure can be viewed, for all practical purposes, as a rectangular waveguide with an effective width dependent on the radii of the ground vias and the frequency of the propagated signals. In fact, there are approaches for calculating the effective distance between sidewall posts in an SIW [35].

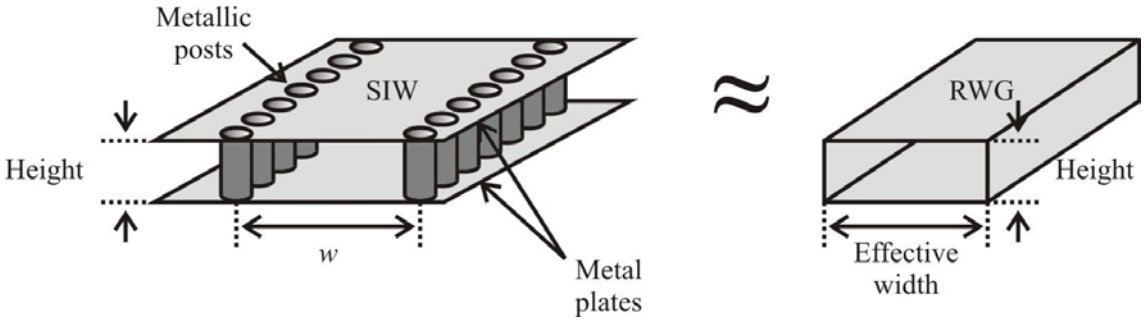


Fig. 2.9 Sketch of a SIW compared with an actual rectangular waveguide (RWG).

For determining the frequency at which an SIW starts propagating electromagnetic signals, the corresponding cutoff frequency of the fundamental mode needs to be calculated. In rectangular waveguides, this is:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{w_{eff}}\right)^2 + \left(\frac{n\pi}{t}\right)^2} \tag{2.1}$$

where m and n are the mode indexes, ε and μ are the material permittivity and permeability respectively, t is the waveguide dielectric thickness, and w_{eff} is the effective width. A good approximation to calculate the latter for an SIW is [36]:

$$w_{eff} = w - \frac{d^2}{0.95b} \tag{2.2}$$

where *d* is the post diameter, *b* is the center-to-center post distance, and *w* is the width defined in Fig. 2.9.

The importance of the calculation of the cutoff frequencies for the SIW resides in the fact that, when the cutoff frequency of the fundamental mode (in this case TE_{10}) is reached, a via perpendicularly embedded into the SIW starts to behave as a radiating monopole antenna. Notice that whereas in the case of an SIW the transmission originated by this radiation is desirable, in the case of a via embedded in a package the transmission in horizontal way is undesirable and via radiation should be avoided. Thus, when the cutoff frequency is reached, parasitic mode propagation will occur in the latter case. Fig 2.10 shows how a package can be seen as an SIW.

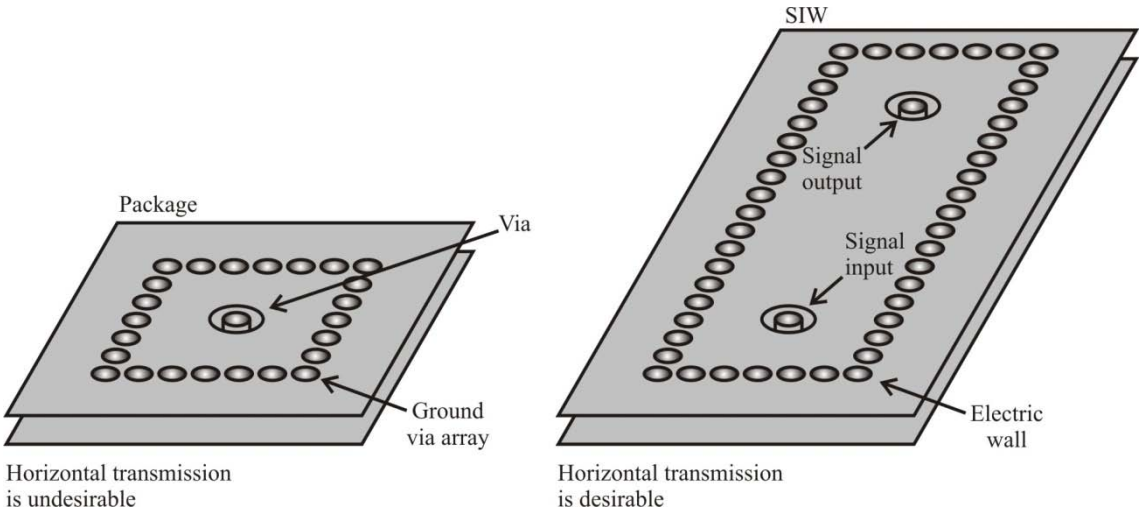


Fig. 2.10 Analogy between a package and a monopole-fed SIW.

As can be seen in Fig. 2.11, a package structure can be separated in three sections, two uniform short-circuited terminated SIWs at the outer sides and a central region in which the evanescent modes surrounding the via exist and the corresponding effects are present. For this reason, the study of uniform transmission lines with short-circuit terminations is discussed in the next section.

Another important parameter associated with an SIW is the characteristic impedance. (Z_0), which is calculated from the formula that relates the wave impedance in a rectangular waveguide with γ, this is [8]:

$$Z_0 = j\frac{\pi^3 t\, f\, \mu}{4 w_{eff}\, \gamma} \tag{2.3}$$

where *f* is the frequency in hertz. This parameter is used to determine the equivalent impedance seen by the exciting element at the extremes of an SIW, and will be used latter in this document to obtain the equivalent circuit model of a radiating via embedded in an SIW-like environment.

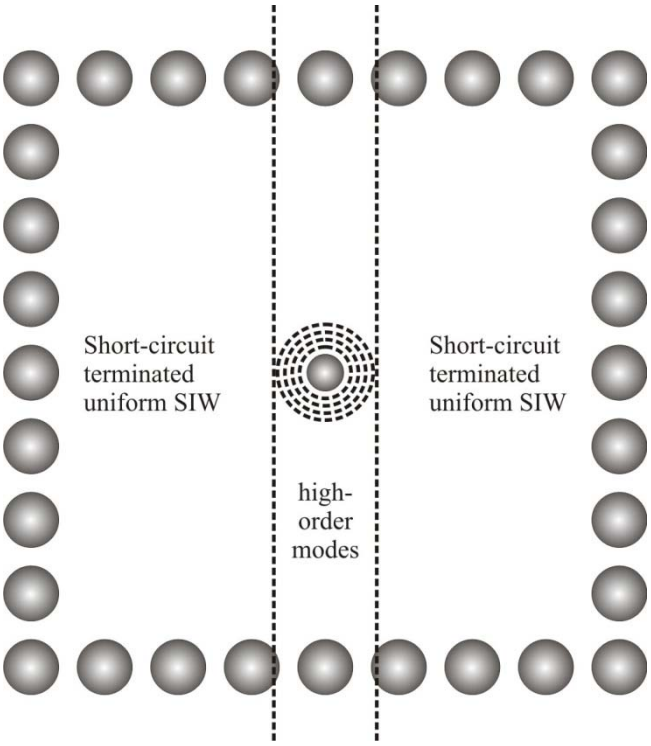


Fig. 2.8 Top view of a package illustrating the three main regions at which different propagation of electromagnetic waves occurs.

2.4 Theoretical Basis

For carrying out a rigorous analysis of the structures and the corresponding electromagnetic interactions mentioned before in this chapter, several Transmission Line Theory concepts have to be discussed. For this reason, some theory that is found useful in the understanding of the research proposed in the next chapter is discussed in this section.

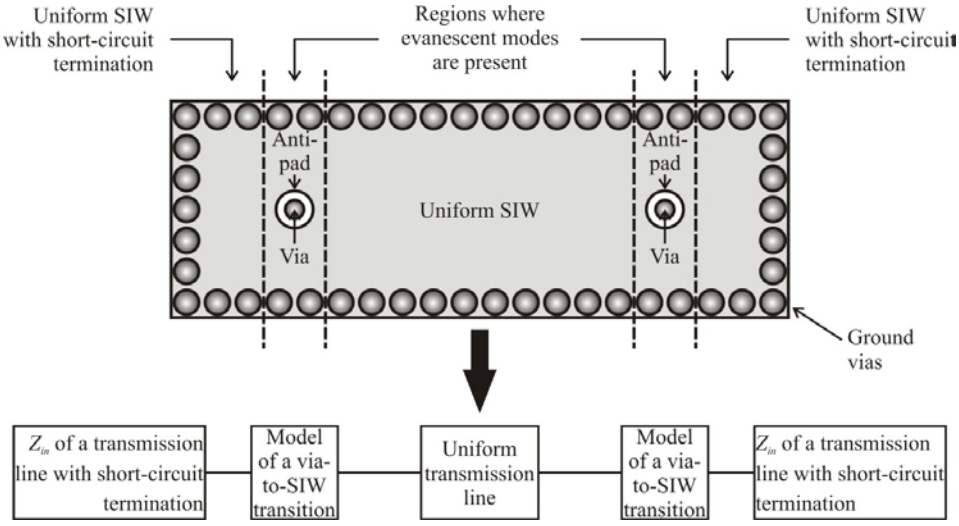


Fig. 2.9 Top view of a SIW illustrating the different region in which it can be divided and the corresponding block model to represent the complete structure.

A via carrying signals from one level to another induce the presence of evanescent modes surrounding it. Nevertheless, these modes only exist within a short region near the via and the rest of the structure can be modeled using closed-form expressions as the input impedance of a uniform transmission line terminated with a short-circuit (see Fig. 2.9). For this reason, the input impedance of a transmission line is discussed hereafter.

A. Input Impedance

If a sinusoidal wave is injected into a transmission line, the resulting voltage is a function of time and the distance from the load. Moreover, this voltage results from the sum of the incident and reflected waves, and can be defined as:

$$V(z,t) = V^{+}e^{-\gamma z}e^{j\omega t} + V^{-}e^{\gamma z}e^{j\omega t} \tag{2.4}$$

where V^{+} and V^{-} are the voltages travelling toward the load and source respectively, and $e^{j\omega t}$ represents the temporal variation of the voltage.

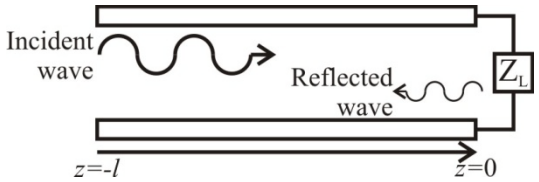


Fig. 2.10 Transmission line terminated with an impedance Z_L.

The reflection coefficient (Γ) describes the amplitude of the reflected wave relative to the incident wave and is dependent on the discontinuity in the load as well as the length of the line. The importance of this parameter within the context of this thesis relies on the interaction between high-order modes and outer edges and how it affects the performance of the transition. Γ can be written as:

$$\begin{aligned}\Gamma(l) &\equiv \frac{V^{-}e^{\gamma l}}{V^{+}e^{-\gamma l}} \\ &= \Gamma_0 e^{-2\gamma l} \\ &= \frac{Z_l - Z_0}{Z_l + Z_0} e^{-2\gamma l}\end{aligned} \tag{2.5}$$

Thus, the expressions for the voltage and current wave on a transmission line can be written as a function of Γ as:

$$V(l) = V^{+}e^{-\gamma l}\left[1 + \Gamma(l)\right] \tag{2.6}$$

$$I(l) = \frac{1}{Z0}\left(V^{+}e^{-\gamma l}\left[1 - \Gamma(l)\right]\right) \tag{2.7}$$

Hence, the ratio of the incident voltage to the incident current at a distance *l* from the load is the input impedance. Thus the input impedance terminated in an arbitrary load can be determined as:

$$\begin{aligned} Z_{in} &= \frac{V(l)}{I(l)} = Z_0 \frac{1+\Gamma(l)}{1-\Gamma(l)} \\ &= Z_0 \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)} \end{aligned} \tag{2.8}$$

whereas for a short-circuit termination, an open-circuit termination and a matched termination the input impedance is modeled respectively as:

$$Z_{in}^{sc} = Z_0 \tanh(\gamma l) \tag{2.9}$$

$$Z_{in}^{oc} = Z_0 \coth(\gamma l) \tag{2.10}$$

$$Z_{in}^{m} = Z_0 \tag{2.11}$$

The input impedance of transmission lines with short-circuit terminations receives a particular attention in this work, since this approach is used to model the small electric-wall-terminated sections of SIW located the outer sides of the structures used for the verification of the proposed model (see Fig. 2,11). Fig. 2.12 shows the magnitude of the input impedance versus frequency curves for two lines with the structure of Fig. 2.11 differing only in length. As can be seen, this parameter presents well-defined peaks that are caused by the interaction between incident and reflected waves. Moreover, the frequency and magnitude of these peaks are closely related to the physical length of the structure [37]. For instance, in a long structure the period of the peaks is smaller than that corresponding to a smaller structure, whereas the corresponding magnitude of these peaks is bigger in the latter. For this reason, as the length of the structure increases, in theory approaching to infinite, the effect of the reflected waves becomes negligible and the input impedance can be approximated by the characteristic impedance of the line. This same effect is observed when a line is terminated with a matched load where no reflections occur.

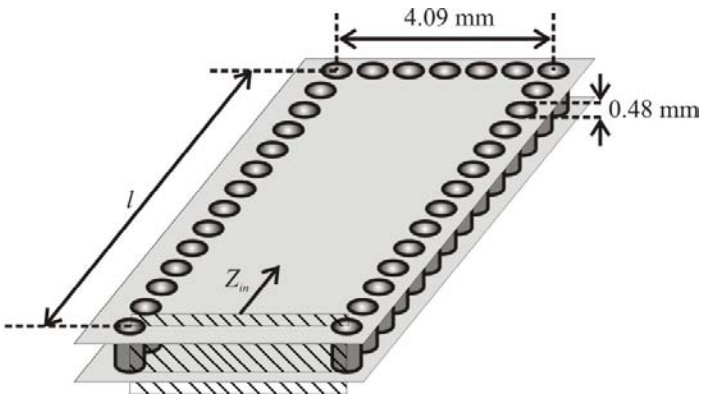


Fig. 2.11 Sketch of a uniform SIW section with short-circuit termination.

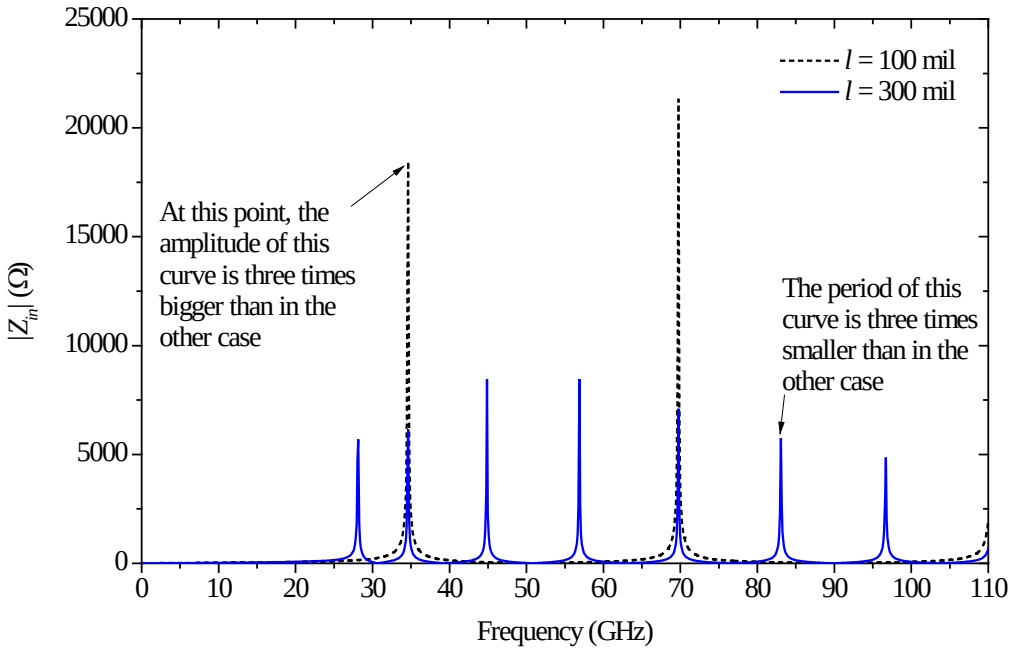


Fig. 2.12 Magnitude of Z_{in}^{sc} versus frequency curves calculated using (2.9) for the SIW depicted in Fig. 2.11 with two different lengths.

As can be seen in Fig. 2.12 the physical structure of the SIW affects in a considerably way the impedance seen by the signal when it propagates through the waveguide. For this reason the study of Z_{in} was proposed, nevertheless, is necessary to study the effect when the SIW acts as a resonator.

As mentioned above, one technique used to minimize the impact of resonances is placing ground vias in an adequate configuration. However, cavity resonances still may occur at certain frequencies. For this reason, a model for resonant cavities is discussed next.

B. Parallel-Plate Impedance – Cavity Model

Another aspect to be studied in this project is the traveling of electromagnetic signals in waveguide environments. Especially, parallel-plate and quasi-rectangular structures. As mentioned above, parallel planes may yield the propagation of the simultaneous switching noise generated between the power and ground planes. This effect is also related to the parallel-plate impedance, Z_{pp}, which can be seen as the combined effect of the impedance of the equivalent waveguide, and the impedance of the exciting element (e.g. a via). In accordance to [13], the magnitude of the switching noise is proportional to Z_{pp}. In this regard, a lower parallel plate impedance means a weaker switching noise resulting in better performance of the system, therefore a better transmission. For this reason, the study of this impedance becomes mandatory in the analysis of high-speed circuits and several approaches can be used for either estimating or obtaining Z_{pp}. Some of these approaches are the cavity model [38-40], the finite

element method [41], the method of moments [42], and the finite difference method [43, 44].

In the cavity model, Z_{pp} is calculated as the ratio of the induced voltage between the planes at the observation port to the impressed current at the source port putting all other ports open. In this model the transfer impedance is defined by the integration of Green's function in a parallel plane cavity as:

$$Z_{ij} = \frac{h}{S_i S_j} \iint_{S_i} \iint_{S_j} G(x, y; x', y')\, dx dy dx' dy' \tag{2.12}$$

where h is the separation between the two parallel planes, S_i and S_j are the areas of the ports i and j respectively, and $G(x,y,x',y')$ is the electric field Green's function due to impressed electric current density inside a parallel-plane cavity. The observation and source points are located at $(x,y) \in S_i$ and $(x',y') \in S_j$ respectively.

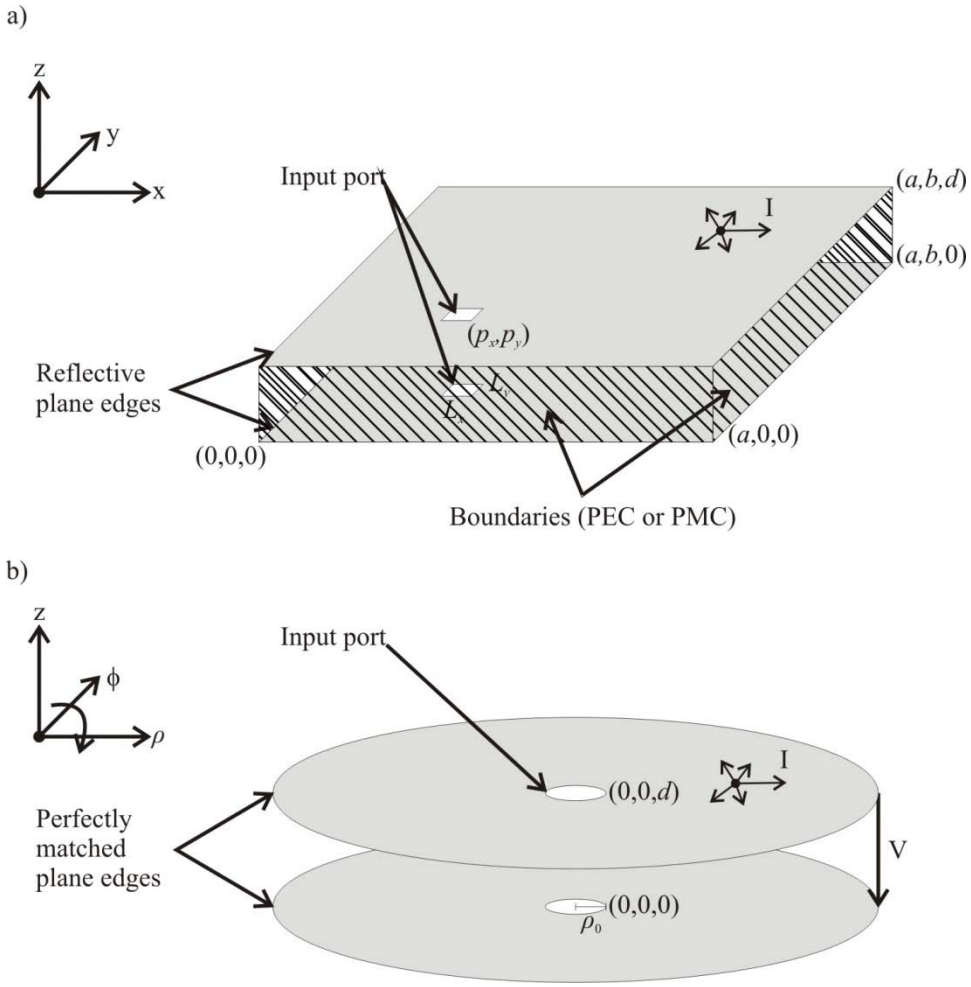


Fig. 2.13 a) Illustration of Z_{pp} with PMC or PEC boundaries at its four sidewalls. b) Illustration of Z_{pp} with PML boundary.

A closed form expression for Z_{pp} depends on the configuration of the structure. The three most common are (see Fig. 2.13):

- parallel planes of finite, rectangular size with open boundaries (i.e. PMC),
- parallel planes of finite, rectangular size with shorted boundaries (i.e. PEC), and
- parallel planes of infinite size (i.e. PML).

For the first two configurations, Z_{pp} can be obtained as:

$$Z_{pp} = \frac{j\omega\mu d}{ab} \cdot \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{C_m^2 \cdot C_n^2 \cdot f_b\left(p_x, p_y\right) \cdot f_p\left(L_x, L_y\right)}{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 - k^2} \tag{2.13}$$

where j is the imaginary unit, ω is the angular frequency, μ is the permeability, d is the plane distance, a and b are the plane dimensions, p_x and p_y are the port locations, L_x and L_y are the port dimensions, m and n are the mode indexes for the number of evanescent modes surrounding the via, and:

$$Cm, Cn = \begin{cases} 1 & m, n = 0 \\ \sqrt{2} & otherwise \end{cases}$$

$$f_b\left(p_x, p_y\right) = \begin{cases} \cos^2\left(\frac{m\pi p_x}{a}\right) \cdot \cos^2\left(\frac{n\pi p_y}{b}\right) & for\ PMC \\ \sin^2\left(\frac{m\pi p_x}{a}\right) \cdot \sin^2\left(\frac{n\pi p_y}{b}\right) & for\ PEC \end{cases}$$

$$f_p\left(L_x, L_y\right) = \mathrm{sinc}^2\left(\frac{m\pi L_x}{2a}\right) \cdot \mathrm{sinc}^2\left(\frac{n\pi L_x}{2b}\right)$$

$$k = \omega\sqrt{\varepsilon\mu}\left(1 - j\frac{\tan\delta + r/d}{2}\right)$$

$$r = \sqrt{\frac{2}{\omega\mu\sigma}}$$

where sinc is the cardinal sine, $\mathrm{sinc}(x) = \sin(x)/x$.

Whereas for the third configuration Z_{pp} is obtained as:

$$Z_{pp} = \frac{j\eta d}{2\pi\rho_0} \cdot \frac{H_0^{(2)}\left(k\rho_0\right)}{H_1^{(2)}\left(k\rho_0\right)} \tag{2.14}$$

where $\eta = \sqrt{(\mu/\varepsilon)}$ is the intrinsic impedance of the medium between the planes, ρ_0 is the radius of the via, $H_0^{(2)}$ and $H_1^{(2)}$ are Hankel functions of the second kind of order 0 and 1 respectively. It should be noticed that (2.14) is formulated in cylindrical coordinates whereas (2.13) is in Cartesian coordinates.

Unfortunately, the use of this approach for obtaining Z_{pp} presents some difficulties from a practical point of view. Since (2.13) presents infinite double summations, it is

necessary to apply truncations or approximations. In addition, the direct implementation on circuit simulators is relatively complicated when compared with circuits using single lumped elements due to this impedance is not represented using a closed-form expression.

Fig. 2.14 shows the dependence on the number of evanescent modes taken for (2.13) demonstrating with that the first issue mentioned above. As can be seen, the number of modes taken for Z_{pp} formulation considerably affects the behavior of the parallel-plate impedance resulting in a problem since the number of modes needed is found once the behavior of Z_{pp} remains constant. Due to this, several calculations have to be made in order to find the correct number of evanescent modes required for the correct characterization of Z_{pp}, resulting in a high-computational cost.

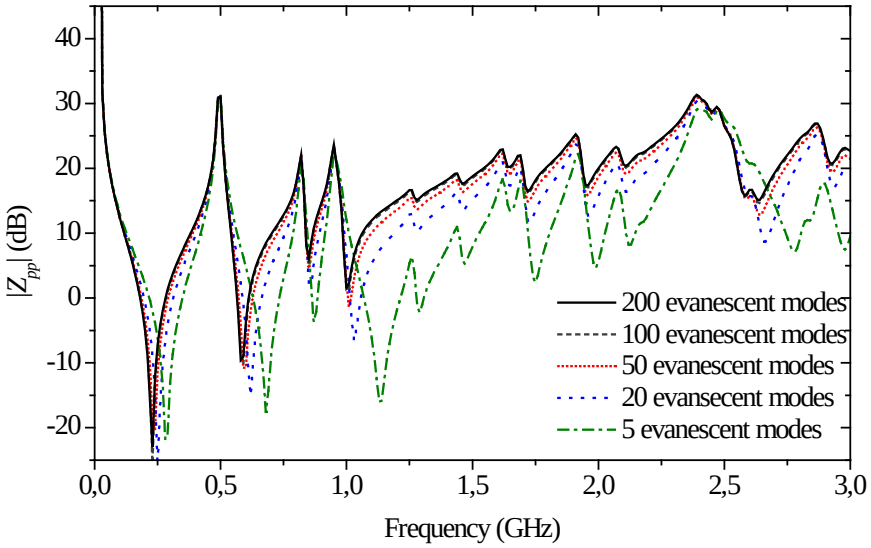


Fig. 2.14 Magnitude of Z_{pp} versus frequency curves for different number of modes for a PMC configuration proposed in [5].

As can be noticed from Fig. 2.14 a high precision is needed for the calculation of this impedance, and this required precision is achieved by adding each time more evanescent modes to (2.13). However, this means a bigger sum which spent more time and computational requirements limiting the calculations of this expression. For this reason, the study of this impedance means actually a huge opportunity for microwave engineers, since with the recent necessity for the integration of systems in smaller spaces the effect of this impedance has become increasingly evident.

2.5 Conclusions

With the sensibility of multilayer-structures to effects that become apparent at high frequencies, the leakage of signal energy is present and cannot be recovered at the end of the desired transmission path. For this reason, some of the most adverse effects occurring in vias when used for used for high-speed signal routing were studied here in

simple structures. Nevertheless, this gives a good insight about the possible issues which may occur in more complex structures.

After the physical origin of some high-order effects was well understood, some techniques to reduce the impact in the transmission were reviewed, such as placing ground vias in the correct places. In addition, some transmission line theory concepts were presented in order to represent the studied effects in a more physical way. Finally, it can be concluded that the study of high-order effects caused by vias in multilayer environments is of great importance in the advance of the design of high-speed electronics systems.

Chapter 3

Electromagnetic Modeling of Vias

Currently, much effort for the advance in computation technologies has been focused in the miniaturization of the components, allowing the integration of more devices in smaller spaces, thus producing more performance per unit volume. This progress is a direct result of the exponential growth of computational systems [45]. In fact, the expected data rate for computer systems by 2012 is about 20 Gbps (see Fig. 3.1), which will require frequency bandwidth of at least 30 GHz [46]. However, signals travelling at these rates present wavelengths that are comparable to the dimensions of IC packages [47]. Due to this, electromagnetic coupling between vias and neighbor devices is likely to occur. Consequently, electromagnetic modeling of vias is necessary in order to determine the impact of the corresponding effect on the signal integrity within actual interconnection channels.

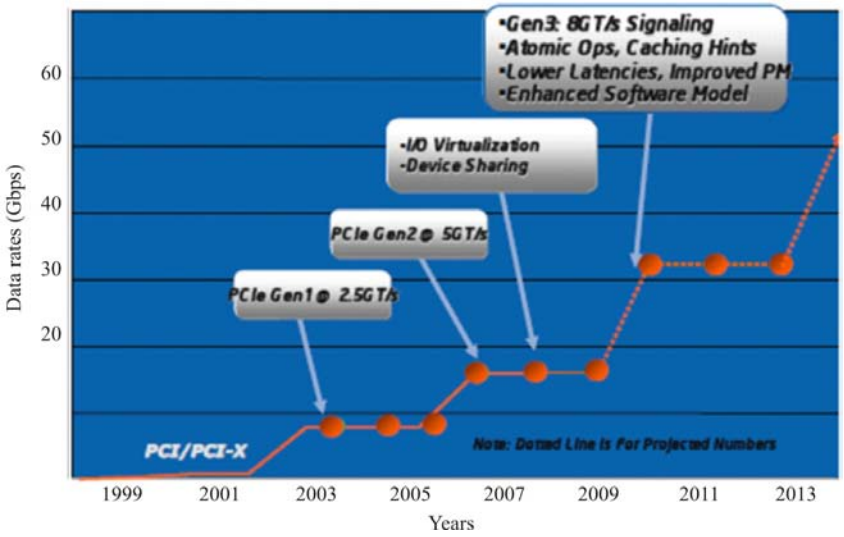


Fig. 3.1 Peripheral component interconnect (PCI) technology roadmap and extrapolation showing the expected data rates in the near future [46]. PCI is a computer bus which is used to interconnect peripheral devices to the motherboard of a personal computer.

Several modeling and characterization methods have been reported to analyze vias embedded in dielectric substrates [10, 12-17]. However, as mentioned in Chapter 1 (Section 1.4), these approaches either require *a priori* knowledge of the material properties and the effective dimensions of the structure or fully rely on the correlation of electromagnetic models with experimental data [48]. The Z_{pp} formulation, for instance (described in Chapter 2, Section 2.4), uses a double infinite summation to represent the impedance of a via embedded in a dielectric substrate and surrounded by electric walls (such as those used in electronic packages) [25]. Unfortunately, since this impedance is not represented using a closed-form expression, the direct implementation on circuit

simulators is relatively complicated when compared with circuits using simple lumped elements.

Thus, in order to provide an alternative easy-to-implement representation for vias embedded in dielectric substrates, methodologies for the characterization and modeling of these transitions are proposed in this chapter. The proposal allows to determine the parasitics associated to the via, and the effects that become apparent once the via starts to radiate. Furthermore, from the analysis of these radiation effects presented at microwave frequencies, the elements that negatively influence the performance of the systems can be determined. Moreover, the corresponding results are useful for optimization purposes.

3.1 Description of the Methodologies

As mentioned in previous chapters, the electrical characterization of vias embedded in dielectric substrates is of great importance when designing electronic systems operating at microwave frequencies. Even though full-wave models can be used to obtain very accurate results for these applications, the corresponding implementation is relatively difficult and requires the previous knowledge of the material and structure characteristics for obtaining realistic results. Besides, these models are computationally expensive and are better suitable for analyzing detailed phenomena occurring in the structures (as will be used here for extracting some electrical parameters). In contrast, equivalent circuit modeling approaches are simple, intuitive and easily implemented. Moreover, when appropriate topologies are selected for representing a given structure, very physical results can be obtained and every electrical component will represent a particular effect associated with the structure. For this reason, one of the contributions of this project is developing physically-based equivalent circuit models and parameter extraction strategies so that vertical transitions can be studied in a direct and simple way.

The aim of this thesis is to model the high-order effects introduced by vias in complex structures like packages. However, since this area is very extensive, the scope of this project only includes the analysis and modeling of vertical transitions considering a signal via surrounded with ground vias (see Fig. 3.2). In this regard, the modeling of this type of structure will be developed through the following subsections. Initially, only the first-order parasitic effects associated with the via are studied, after that, the interaction within the package is considered.

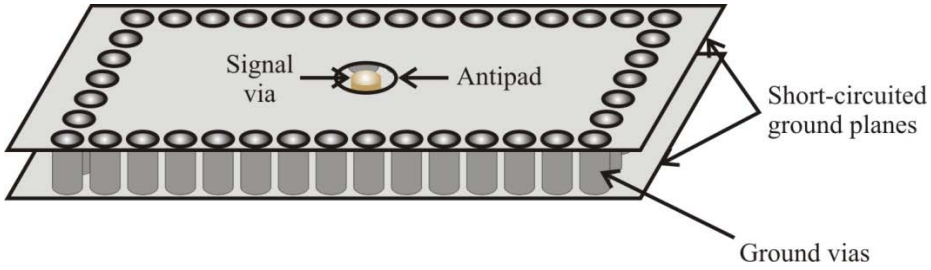


Fig. 3.2 Sketch of the package structure under study.

A. Simple Model of a Via

A via is typically represented with a π-model (see Fig. 3.3). This simple RLC topology is associated with the geometrical features of the via. Specifically, the capacitance is associated with the parallel-plate capacitor formed between the pad and the ground plane, the inductance is associated with the inductive behavior introduced by the barrel of the via, whereas the resistor is related to metal losses. Most of the times, the latter parameter is neglected since the length of the vias are usually small and introduce relatively low insertion losses. In fact, it is important to mention at this point that the main adverse effect introduced by vias is a mismatch between the sections composing an interconnection channel. This effect is accurately represented using only LC equivalent circuits as will be shown later.

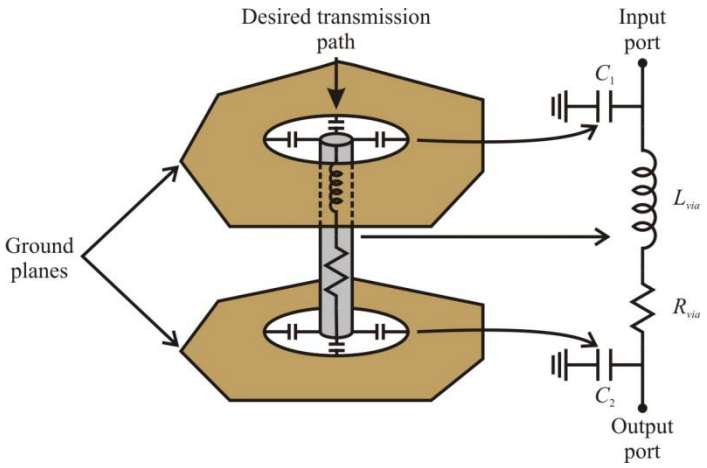


Fig. 3.3 Parasitic elements of a via and the resulting equivalent circuit model.

In accordance to Fig. 3.3, a via can be represented by means of a two-port network, where the port 1 (input port) is located at the top of the via, whereas the port 2 (output port) is located at the bottom end. Using this network representation, the parasitic via-to-ground capacitances and the effective inductance of the via can be obtained from the corresponding two-port *Y*-parameters by using:

$$C_1 = \frac{\mathrm{Im}\left(Y_{11} + Y_{12}\right)}{\omega} \tag{3.1}$$

$$C_2 = \frac{\mathrm{Im}\left(Y_{22} + Y_{12}\right)}{\omega} \tag{3.2}$$

$$L_{via} = \frac{1}{\omega\,\mathrm{Im}\left(Y_{12}\right)} \tag{3.3}$$

where ω is the frequency in radians.

In computing systems, the signals are propagated in digital formats. However, digital signals are not perfectly square-shaped. In fact, these signals require a finite time for

transitioning from a logic state to another. Thus, the higher the speed of these signals, the smaller the transitional time is. The time spent by the signal for transitioning from a low to a high state is known as *rise time* (T_r), see Fig. 3.4. When this parameter is known for the signal travelling along a particular interconnect, it is possible to determine if a via within this interconnect can be modeled using lumped or distributed equivalent circuits. The criterion based on T_r establishes that, when the time that the signal takes to travel through the via (T_{vd}) is bigger than T_r /10, the simple model of a via is not longer useful and distributed effects have to be considered. The parasitic effects of vias considerably influence T_{vd}; for instance, large capacitances increase this parameter, which reduces the capacity of the via to respond to signals with small rising time. In other words, the effects that increase T_{vd} reduce the capability of digital systems to handle high frequency signals.

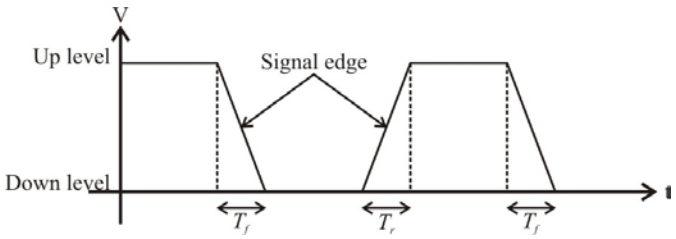


Fig. 3.4 Sketch of a digital signal showing the rise time. Similarly, the fall time (T_f) can be defined as the time spent by a signal for transitioning from a high to a low state.

Many of the undesired effects associated with vias operating at high frequencies are due to the similarity of package-like structures with resonators. For instance, in a package the reference planes are short-circuited by ground vias and only one conductor is present, which makes the structure to behave as a resonant cavity. In fact, this facilitates electromagnetic propagation in transversal magnetic (TM), transversal electric (TE), but not the transversal electromagnetic (TEM) mode [20], being the latter the desired mode in conventional PCB and package structures. Thus, TE modes are parasitic in a package; however, since the width of the package is usually bigger than the dielectric thickness, TE modes are likely to occur at high frequencies. For instance, Fig. 3.5 shows the top view of a package indicating the distribution of the electric field obtained from a full-wave simulation. In this case, the fundamental mode in which the via is undesirably radiating energy is the TE_{10}, with a cutoff frequency (f_c) of 27 GHz.

As mentioned above, it is expected that future electronic systems will handle signals with millimeter wavelengths which are comparable to the current physical dimensions of IC packages. This suggests that parasitic modes will become apparent in these structures, originating signal radiation inside the package and resulting in EMI problems. As can be noticed, this effect is not considered in the typical π-model shown in Fig. 3.3. Therefore, a model for considering the interaction of the via with other structures due to radiation effects is necessary. In order to achieve this, the π-model needs to be appropriately modified.

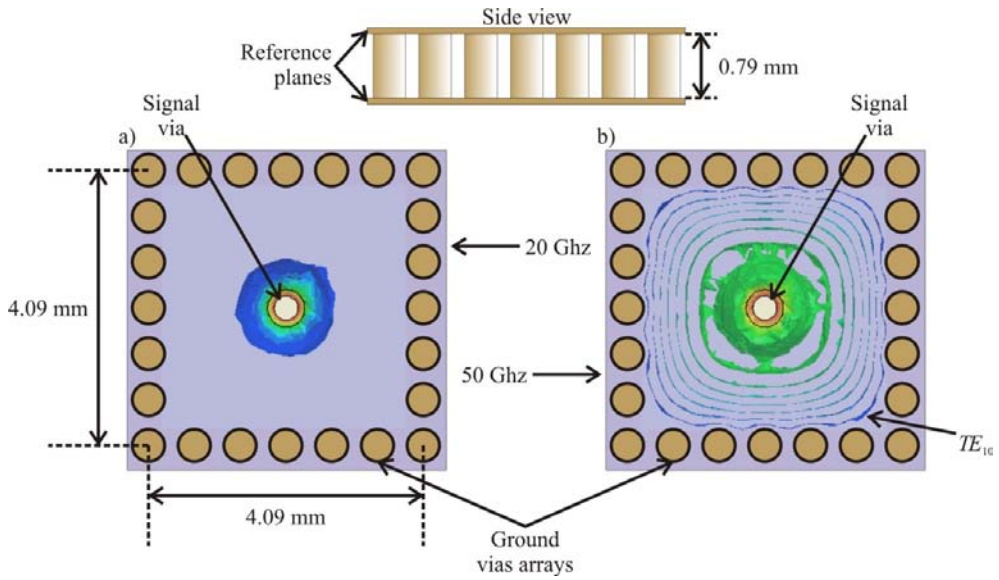


Fig. 3.5 Distribution of the electric field within a package: a) At frequencies below f_c (only evanescent waves take place), and b) beyond f_c. Notice in a) that all fields are concentrated close the via since the signal frequency is smaller than f_c, whereas in b) f_c is already reached; therefore, the via starts to radiate and part of the signal is propagated within the package in undesired directions.

B. Modeling Radiation Effects in Vias

In addition to the inductive and capacitive elements in the typical π–model of a via, the circuit proposed in this thesis for vias embedded in dielectric substrates includes the parameter Z_{eq}. This parameter allows the appropriate modeling of the effects that become apparent once that the via starts radiating and signal leakage occurs. Fig. 3.6 shows the corresponding equivalent circuit.

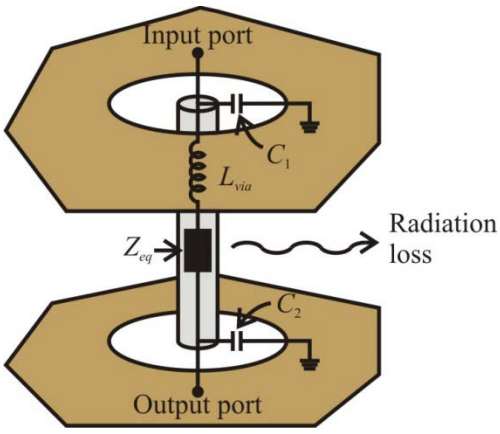


Fig. 3.6 Equivalent circuit for a via embedded in a dielectric substrate including Z_{eq}, which accounts for the radiation effect.

In this project, the electromagnetic radiation caused by the via is restricted to only horizontal propagation taking as reference the structure shown in Fig. 3.2. This allows that the package can be divided in three main regions; a region of transition, which includes the via and the evanescent modes surrounding it, embedded between two

waveguides. Therefore, for the characterization of the effect introduced by the electromagnetic radiation occurring in vias, consider now the structure shown in Fig. 3.7a, where the via is located at the middle along the length of a package-like structure. Assume that the top and bottom ground planes of this structure are grounded only by two rows of ground vias. Moreover, perpendicularly to these rows of vias the structure is assumed to be terminated with perfectly coupled loads (Terminations 1 and 2); i.e. the load is assumed to equal the characteristic impedance of the waveguide formed by the planes and ground vias. In this regard, coupled loads are used as terminations in order to avoid the effects associated with signal reflections caused by the edges of the structures. Fig. 3.7b shows the corresponding equivalent circuit of this structure. Since the via can be seen as a monopole antenna radiating signals inside the structure, an electrical transition between the via and the structure exists and it makes that the electromagnetic waves experience an impedance change when transitioning. For this reason, besides the parasitics of the via, an impedance transformer which maps the characteristic impedance of the via into the characteristic impedance of the package-like structure is used in the equivalent circuit [49]. Furthermore, among the effects that have to be considered at this transition is that associated with the impedance Z_t, which is related to the evanescent modes present at the surrounding of the via. Thus, with these elements, the electrical transition from the via to the package is fully modeled. However, it is necessary to include the hypothetical waveguide path discussed in Chapter 2 (Section 2.2) which accounts for the waveguide formed by the planes and ground vias. For this reason, in addition to the impedance transformer and Z_t, two uniform transmission lines associated with the propagation in the direction that is parallel to the rows of ground vias are considered and characterized by means of the corresponding propagation constant (γ) and the characteristic impedance of the waveguide (Z_0) [8].

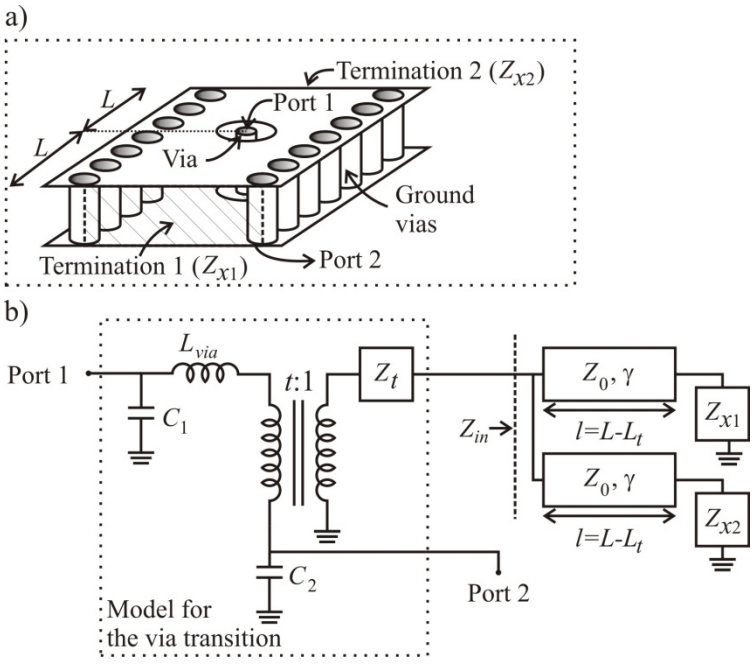


Fig. 3.7 a) Sketch showing the 3D model of a via transition embedded between two perfectly-matched waveguide terminations, and b) the corresponding equivalent circuit for $f > f_c$.

Notice in Fig. 3.7b that the ratio of the impedance transformer is *t*:1. For explaining the determination of *t* see Fig. 3.8. This parameter depends on the position of the via along the *x* axis and can be obtained as [50]:

$$\csc^2\left(\frac{\pi d}{a}\right):1 \tag{3.4}$$

where, *d* and *a* are the distances shown in Fig. 3.8. Notice that, when the via is at the middle between the two rows of ground vias *t*=1.

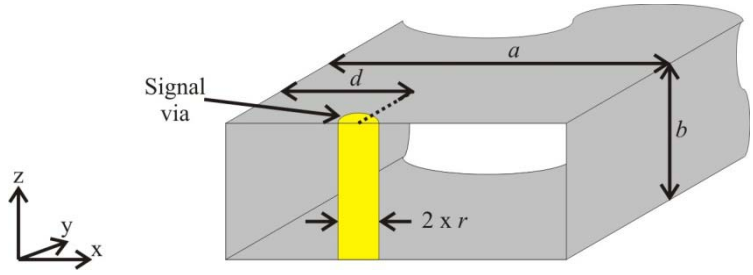


Fig. 3.8 Perspective of a waveguide with a via for illustrating the determination of the transformer ratio. In the case of the structures under study, *a* is the effective width of the package-like structure, *b* is the thickness of the dielectric, *r* is the radii of the via and *d* is the distance from the upper side of the waveguide to the center of the via as can be seen in the figure.

For the characterization of the electromagnetic radiation and the extraction of the equivalent-circuit model parameters, full-wave simulations of the 3D-model structure shown in Fig. 3.7a are carried out. Since the two rows of ground vias placed at each side of the structure resemble the lateral walls of an SIW, it can be said that the transition region is embedded among two SIWs. In other words, the via "sees" two SIWs in the direction in which it radiates. In this regard, the input impedance (Z_{in}) involved in the equivalent-circuit model shown in Fig. 3.7b represents the input impedance of these two SIWs placed in parallel. Moreover, since these SIWs are terminated with coupled loads in order to simplify the analysis, it can be assumed that each SIW section can be approximated by its characteristic impedance (Z_0) regardless of the corresponding length making the via "sees" Z_0 at both sides. This allows reducing Z_{in} to $Z_0/2$. Under all the assumptions previously discussed, the equivalent circuit depicted in Fig. 3.7b can be simplified in this case to the equivalent circuit shown in Fig. 3.9. Notice that the impedance transformer is omitted in this equivalent circuit since the via is located at the middle along the width of the package modeled in this project.

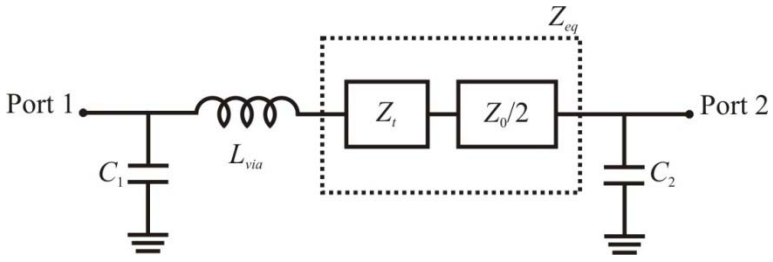


Fig. 3.9 Simplified model for the via transition assuming perfect matched boundaries in the radiation directions.

As can be noticed, Z_0 is involved in the equivalent circuit model shown in Fig. 3.9. In this regard, the calculation of Z_0 can be done using (2.3) exposed in Chapter 2 (Section 2.3). However, this closed-expression uses in its formulation γ. Consequently, γ can be obtained from the surface resistivity of the metal plates of the package and the wavenumber of the SIW sections as follows [5]:

$$r = \sqrt{\frac{2}{\mu\sigma\omega}} \tag{3.5}$$

$$k_c = \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \tag{3.6}$$

$$k = \omega\sqrt{\mu\varepsilon}\left(1 - j\frac{\tan\delta + r/b}{2}\right) \tag{3.7}$$

$$\gamma = \sqrt{k_c^2 - k^2} \tag{3.8}$$

where μ is the permeability of the dielectric, σ is the conductivity of the metal plates, ω is the frequency in radians, m and n are the mode indices (in this case m=1 and n=0 for TE_{10}), a is the effective width of the SIW, b is the height of the SIW and tanδ is the loss tangent of the dielectric.

Thus, since the parasitics of the via are already known, Z_{eq} can be determined from the simulated Y-Parameters of the 3D-model and the equivalent circuit model related to Fig. 3.9 for $f > f_c$ as:

$$Z_{eq} = -\frac{1}{Y_{12}} - j\omega L_{via} \tag{3.9}$$

Hence, since Z_{eq} is the series impedance of Z_t and Z_{in}, Z_t can be obtained from (3.9) as:

$$Z_t = Z_{eq} - \frac{Z_0}{2} \tag{3.10}$$

As could be noticed, the use of perfectly coupled loads in the terminations of the 3D-model shown in Fig. 3.7a allows that the determination of Z_t would be in a direct and simple way. However, bear in mind that packages has ground vias surrounding the signal via as can be seen in Fig. 3.2. For this reason, instead of coupled loads, now electric-walls (i.e. short-circuit) terminations are used in the 3D-model shown in Fig. 3.7a. So that, $Z_{X1} = Z_{X2} = 0$ and Z_{in} represents in this case the input impedance of two identical short-circuit terminated transmission lines in parallel; mathematically:

$$Z_{in} = \frac{Z_0}{2}\tanh\left(\gamma\left(L - L_t\right)\right) \tag{3.11}$$

where L is shown in Fig. 3.7a and L_t is the distance within the evanescent modes are present.

Thus, the equivalent impedance used to characterize the effects that become apparent once the via starts to radiate in packages is given by:

$$Z_{eq} = Z_t + Z_{in} \tag{3.12}$$

where Z_t has been previously determined.

At this point, now that all the parameters of equivalent circuit related to Fig. 3.7b using short-circuit terminations are known, packages as the one shown in Fig. 3.2 can be fully modeled using lumped elements. However, analyzing the results of the full-wave simulations applied to the 3D-model used in the characterization of the electromagnetic radiation, it could be noticed that the distance L_t did not has a constant value as the frequency increases once the via starts radiating. Thus, since this distance plays a key role in the calculation of Z_{eq}, the next section presents an approach of how deal with it.

3.2 Determination of the Effective Length for the Uniform SIW Sections

As mentioned above, during the characterization of the input impedance of a short-circuit terminated waveguide the distance (L_t) at which the evanescent waves occur, measured from an electrical transition, varies with the frequency. In consequence, the effective length of a waveguide (in this case, an SIW) that presents electrical transitions is also frequency dependent. Fig. 3.10 shows the distance (l) versus frequency curve considered for the uniform SIW section for a specific case. As can be seen, as the frequency increases l starts increasing as well. This suggests that the fundamental mode of propagation is well-defined closer to the via as the frequency continues to rise.

Evanescent modes are basically modes with imaginary wavenumbers, and are characterized by an exponential attenuation and lack of a phase shift [20]. In this regard, the electric field in function of the length for any propagation mode can be expressed as:

$$E\left(l\right) = E_0 e^{(\gamma l)} \tag{3.13}$$

where E_0 is any input constant electric field.

Since in evanescent modes the imaginary part of the propagation constant is nearly zero, equation (3.15) for evanescent modes can be rewritten as:

$$\frac{E(l)}{E_0} = e^{(\alpha l)} \tag{3.14}$$

and, isolating l from (3.14):

$$l = \frac{\ln\left(\frac{E(l)}{E_0}\right)}{\alpha} \tag{3.15}$$

Trying to determine the effect of each evanescent mode to L_t would be a hard task and since this is out of the scope of the project, in this thesis, L_t is left as a fitting parameter easily determined by correlating (3.12) with full-wave simulated data.

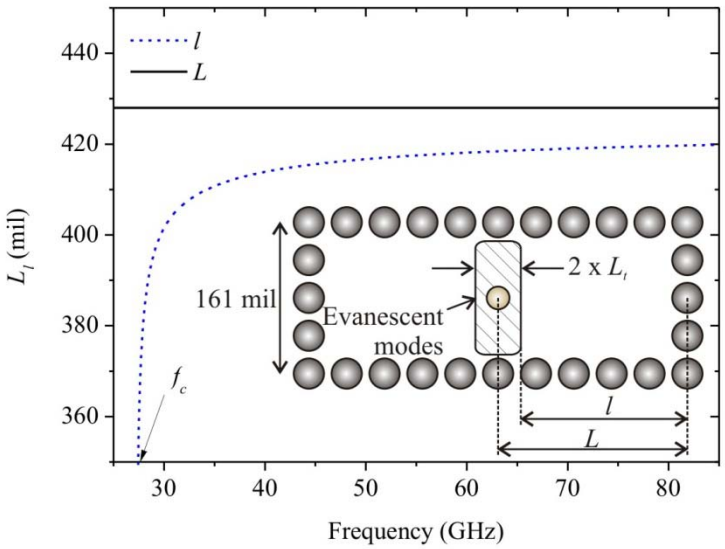


Fig. 3.10 Comparison between the physical length L and the effective length l used in the determination of the input impedance for a short-circuit-terminated transmission line. $l = L - L_t$.

3.3 Conclusions

In this chapter, the equivalent circuit topology proposed for vias embedded in dielectric substrates and surrounded by ground vias was derived. This approach not only considers the parasitics of the via, but also the effects that become apparent once that the via starts radiating electromagnetic waves inside the structure.

The proposal is described based on two of the most representative approaches used to model vias, circuit-oriented and full-wave solvers, considering the main advantages of each one. Full-wave simulations are used, due to its high-accuracy, for the determination of the model parameters whereas an equivalent-circuit model, due to its simplicity and intuitiveness, is used to represent the parasitics of the via besides the effects related to the electromagnetic radiation.

An analysis of the distance (L_t) in which the evanescent modes are present was carried out, determining that the best way to deal with it is correlating closed-expressions with simulated data.

Chapter 4

Experimental Results and Validation

In order to demonstrate the corresponding accuracy of the equivalent circuit topology for vias embedded in dielectric substrates surrounded by ground vias presented in Chapter 3, several SIWs with vias as launch structures were fabricated on PCB technology. In this regard, the validation is performed by reproducing the measurements of the scattering parameters of the SIWs with the equivalent circuits proposed in Chapter 3.

With this purpose, two simulators were used. As the starting point in the characterization of the SIW, a 3D-model was implemented in the HFSS full-wave simulator [51]. This model was calibrated with the experimental data so that the equivalent circuit parameters of the implemented transitions can be obtained in a direct and simple way. Finally, a block model was implemented in the ADS circuit simulator [52], and compared with the experimental data.

4.1 Fabrication and Measurements of the SIWs

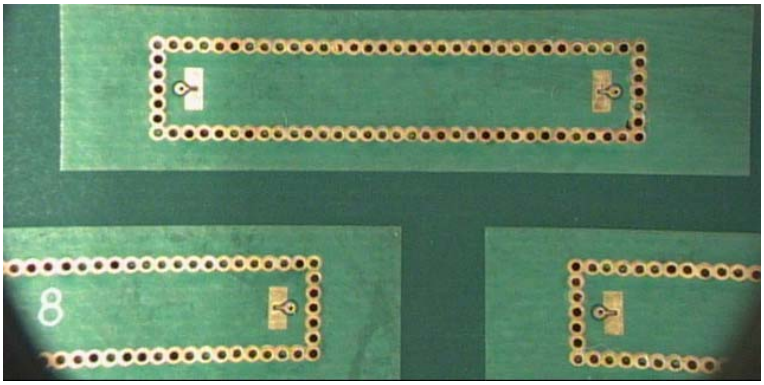


Fig. 4.1 PCB board including the SIWs used for the verification of the proposed method.

SIWs with the same cross-section but different lengths were fabricated on a PCB made of Rogers RT/Duroid 5880 material with a thickness of 0.79 mm (see Fig. 4.1). According to Fig. 4.2, the dimensions for the fabricated structures are: a = 4 mm, Ls = 1.02 mm, a diameter of the ground vias of 0.48 mm, and a center-to-center separation between ground vias of 0.68 mm. The nominal relative permittivity and loss tangent for this material at 50 GHz is ε_r = 2.2 and $\tan\delta$ = 0.0017 respectively. The SIWs were fabricated with a via as a launch structure and terminated with ground-signal-ground configured pad structures so that coplanar RF-probes with a pitch of 150 μm can be used to carry out *S*-parameter measurements (see Fig. 4.3).

Two-port S-parameters were measured to these structures using a previously calibrated Agilent E8361A Precision Network Analyzer and ground-signal-ground coplanar probes. A line-reflect-match (LRM) calibration was performed previous the measurements of the prototypes, which were taken up to 110 GHz. It is important to mention that a deembedding process was not performed in this case because it is no necessary to remove the effect of the vias; thus, the measurement presents the effects of the text fixtures (the pads are placed as close as possible to the exciting post).

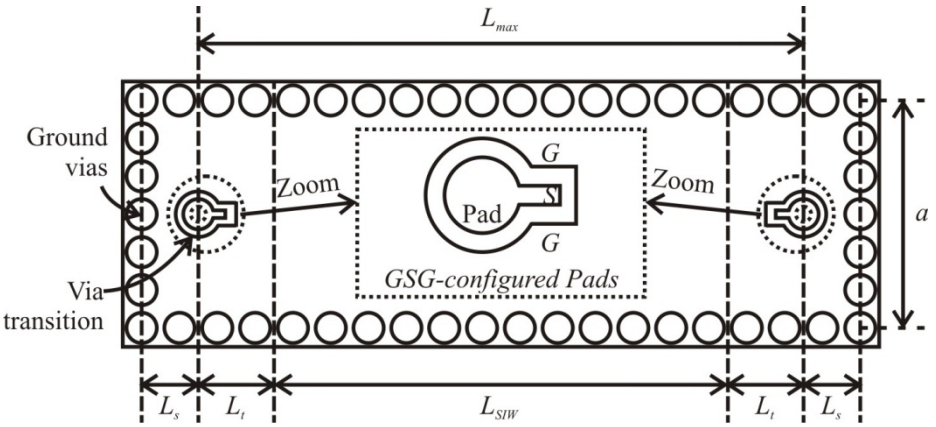


Fig. 4.2 Top view of the SIWs fabricated for illustrating the formulation of the proposed method.

To prevent signal degradation, it is desired that the power of a signal traveling along an SIW is transmitted in a single (i.e. the dominant TE_{10}) mode. Thus, the vias shown in Fig. 4.2 were designed to excite this mode. For that matter, the vias were symmetrically placed in such a way that even modes, such as TE_{20}, cannot be excited. This allows to extend the usable transmission bandwidth from the cutoff frequency of the TE_{10} (i.e. f_c) to the cut-off frequency of the TE_{30}, which is the next higher order odd mode.

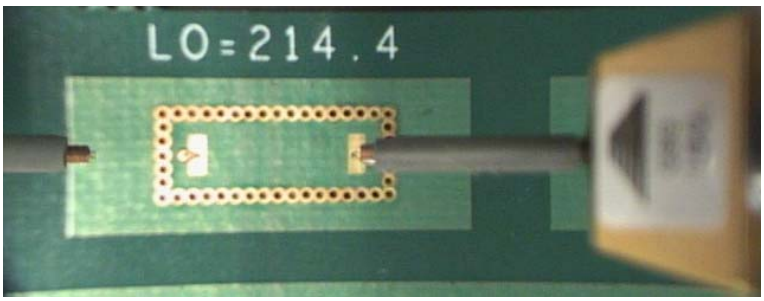


Fig. 4.3 GSG probes used to measure the *S*-parameters of the SIWs under verification.

4.2 Calibration of the 3D-Model

The methodologies for the extraction of the model parameters discussed in Chapter 3 are based in full-wave simulations. For this reason, a calibration of the 3D-model implemented in HFSS with the experimental data obtained from the SIWs is performed previously to the extraction of the parameters. Fig. 4.4 shows the comparison between the measured and simulated *S*-parameters once the calibration is done. As can be seen, a

good correlation between the full-wave simulation and the experimental data is achieved. Therefore, the correct extraction of the model parameters is guaranteed. In addition, the complex propagation constant (γ) as well as the characteristic impedance (Z_0) of the simulated SIWs are compared with experimental data in Fig. 4.5 and 4.6 respectively. As can be seen, excellent correlation is observed up to 83 GHz, which is the cutoff frequency of the TE_{30} mode.

As can be seen in the insertion losses in Fig. 4.4, approximately at 27 GHz the SIW starts to propagate the signals from port one to port two. Thus, the cutoff frequency (f_c) of the fundamental mode, in this case TE_{10}, is ≈ 27 GHz. Moreover, in Fig. 4.5 at this frequency it can be noticed that the phase shift of the SIW starts to increases whereas the attenuation decays to nearly zero.

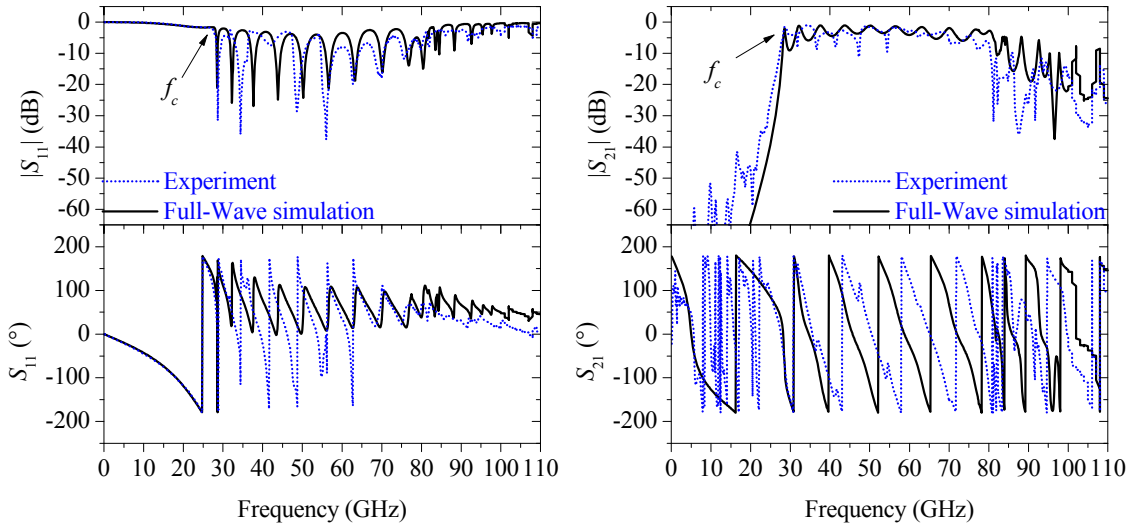


Fig. 4.4 Measured return and insertion losses compared with the 3D-model full-wave simulation for an SIW with L_{max} = 10.9 mm.

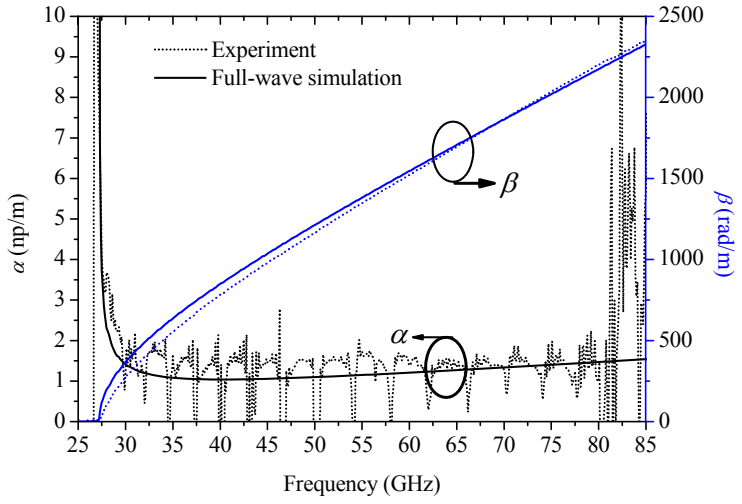


Fig. 4.5 Experimental and simulated attenuation and phase delay versus frequency for the homogeneous part of SIW.

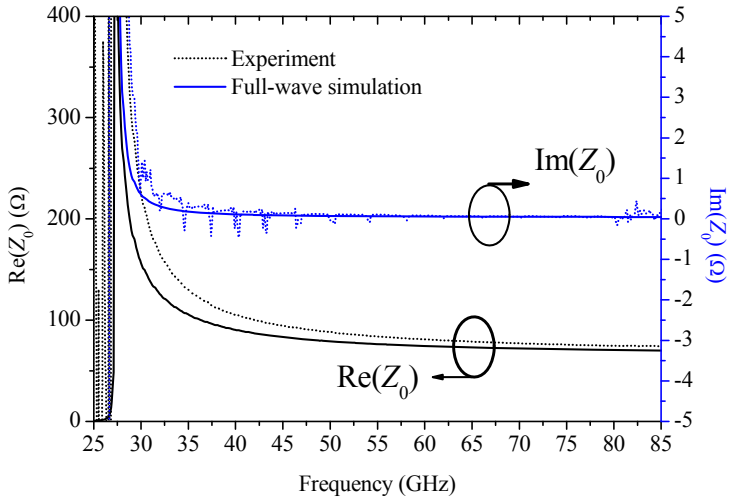


Fig. 4.6 Experimental and simulated characteristic impedance versus frequency for the homogeneous part of SIW.

Once the 3D-model is calibrated with experimental data, the complete structure can be simplified into a simpler one (see Fig. 4.7). This structure only considers one signal via, and the effective width of the SIW is calculated in order to replace the ground vias with solid metallic walls. So that, it allows reducing the computational cost besides the methodologies proposed in Chapter 3 can be directly applied this structure. Consequently, the determination of the equivalent circuit model can be done in a simple and direct way as will be shown in the next section.

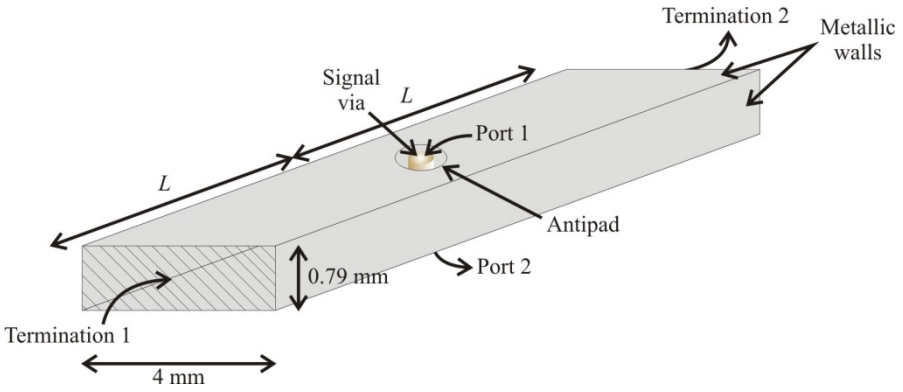


Fig. 4.7 Rectangular waveguide (RWG) used instead of the SIW for the extraction of the model parameters with an arbitrary length L and equivalent dimensions.

4.3 Parameter Determination

Since the 3D-model is calibrated with experimental data, additional losses are included in the via-to-ground capacitances. For this reason, R_1 and R_2 are added in series to C_1 and C_2 respectively in the simple model of the via in order to consider these expected losses (see Fig. 4.8). As is mentioned in Chapter 3, the via starts to radiate the

signal inside the SIW once f_c is reached. Thus, the parasitics of the via can be determined from the *Y*-parameters resulting of the full-wave simulations of the 3D-model for $f < f_c$. Based on the equivalent circuit model depicted in Fig. 4.8 Z_1, Z_2 and Z_3 can be obtained as:

$$Z_1 = \frac{1}{Y_{11} + Y_{12}} \tag{4.1}$$

$$Z_2 = -\frac{1}{Y_{12}} \tag{4.2}$$

$$Z_3 = \frac{1}{Y_{22} + Y_{12}} \tag{4.3}$$

where

$$C_1 = -\frac{1}{\omega \operatorname{Im}(Z_1)} \tag{4.4}$$

$$R_1 = \operatorname{Re}(Z_1) \tag{4.5}$$

$$L_{via} = \frac{\operatorname{Im}(Z_2)}{\omega} \tag{4.6}$$

$$R_{via} = \operatorname{Re}(Z_2) \tag{4.7}$$

$$C_2 = -\frac{1}{\omega \operatorname{Im}(Z_3)} \tag{4.8}$$

$$R_2 = \operatorname{Re}(Z_3) \tag{4.9}$$

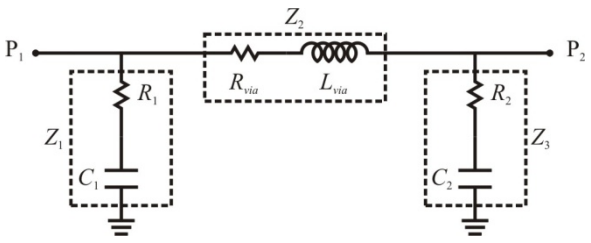


Fig. 4.8 π-network used for the extraction of the via equivalent circuit model.

Fig. 4.9 and Fig. 4.10 show C_1, C_2, and L_{via} versus frequency curves respectively. As can be noticed, the values of these elements are practically constant for frequencies below f_c. However, R_1 and R_2 do not show this behavior (see Fig. 4.11). For this reason, a new equivalent circuit for the via is proposed since in this project the equivalent circuit proposed for vias embedded in dielectric substrates is intended not to be frequency-dependent. In this regard, a capacitor is place in parallel with R_1 and R_2 in

order to model the dependence with frequency of such elements. Fig. 4.12 shows the corresponding equivalent circuit for the parasitics of the via.

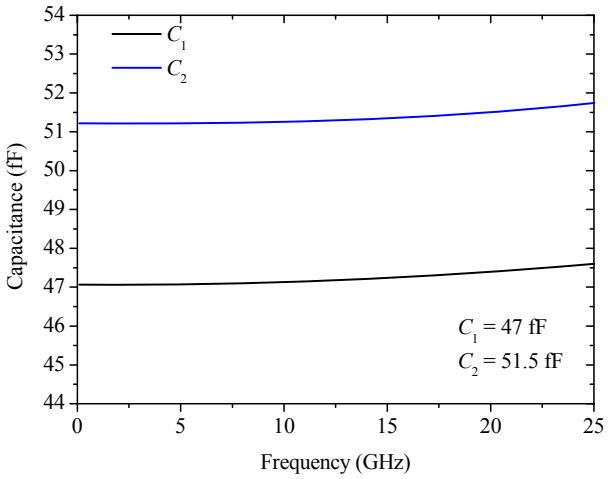


Fig. 4.9 Parasitic via-to-ground capacitances.

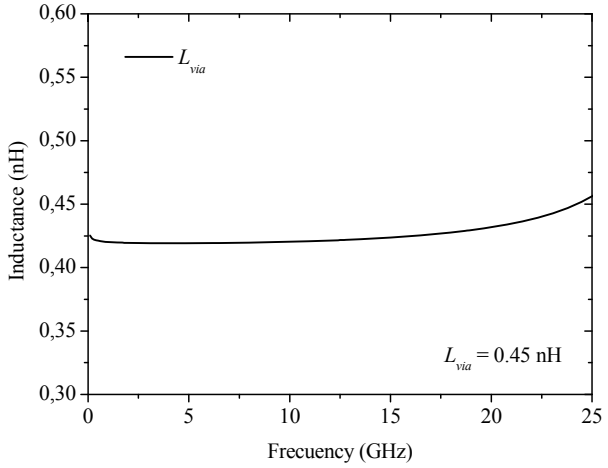


Fig. 4.10 Parasitic inductance of the via.

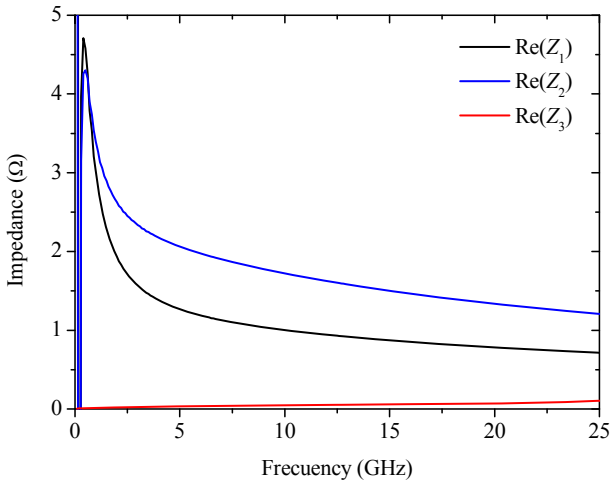


Fig. 4.11 Expected losses for the via-to-ground capacitances and those related to the finite conductivity of the metal.

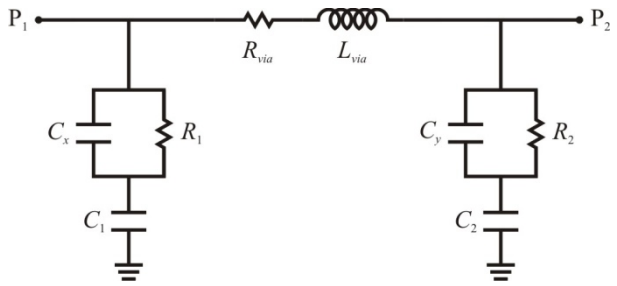


Fig. 4.12 Modified π-model for the via at smaller frequencies than f_c.

In accordance to Fig. 4.12, for the determination of the real part of Z_1 and Z_3 a linear fit can be used, whereas R_{via} is neglected due to its small value (see Fig. 4.11). Thus, according to the previous discussion, the real part of Z_1 can be modeled as:

$$Z_1 = \frac{R_1}{1+j\omega C_x R_1} + \frac{1}{j\omega C_1} = \frac{R_1}{1+j\omega C_x R_1}\left(\frac{1-j\omega C_x R_1}{1-j\omega C_x R_1}\right) + \frac{1}{j\omega C_1}$$
$$= \frac{R_1}{1+\omega^2 C_x{}^2 R_1{}^2} - j\left(\frac{1}{\omega C_1} + \frac{\omega C_x R_1{}^2}{1+\omega^2 C_x{}^2 R_1{}^2}\right) \tag{4.10}$$

$$\mathrm{Re}(Z_1) = \frac{R1}{1+\omega^2 C_x{}^2 R_1{}^2} \tag{4.11}$$

where

$$\frac{1}{\mathrm{Re}(Z_1)} = \omega^2 C_x{}^2 R_1 + \frac{1}{R_1} \tag{4.12}$$

Now, relating (4.12) with the slope and intercept form of the equation of the straight, a linear fit can be assumed by: $y = 1/\mathrm{Re}(Z_1)$, $m = C_x{}^2 R_1$, $x = \omega^2$ and $b = 1/R_1$. In a similar way the real part of Z_3 can be obtained. Fig. 4.13 and Fig. 4.14 show the results of the linear fit applied to each curve including the values of the desired elements.

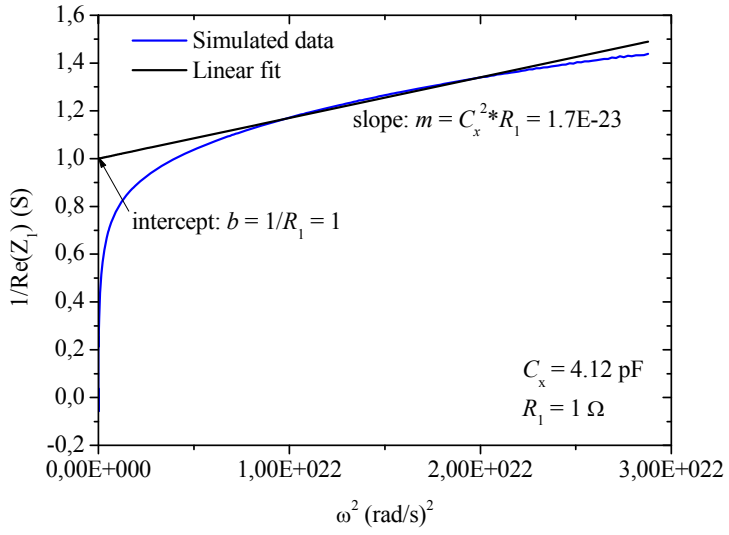


Fig. 4.13 Linear regression applied to simulated data for the determination of C_x and R_1.

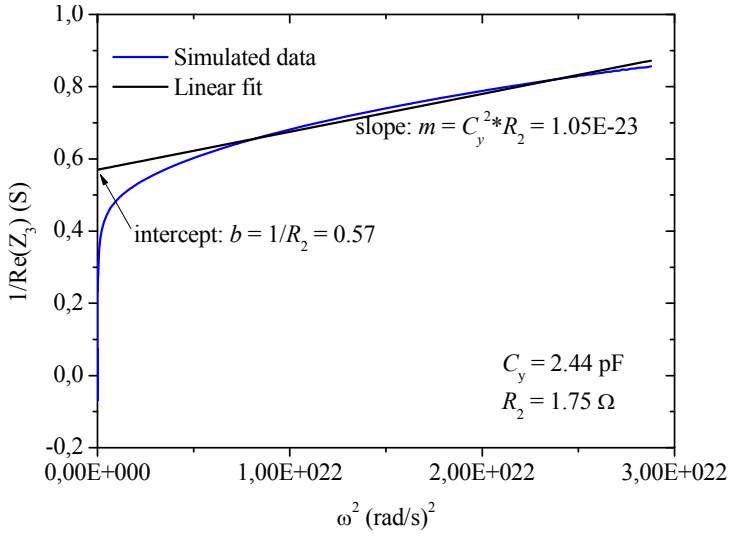
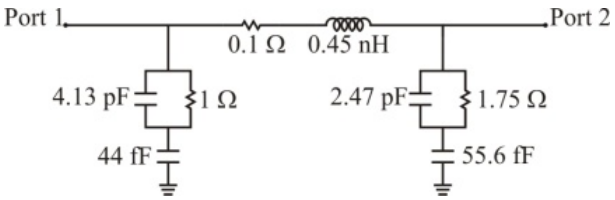


Fig. 4.14 Linear regression applied to simulated data for the determination of C_y and R_2.

Once all the parameters of the circuit related to Fig. 4.12 are known, see Fig. 4.15a, the equivalent circuit must be able to accurately reproduce the measured return losses of the experiment for $f < f_c$. Fig. 4.15b shows this parameter versus frequency curve. An excellent agreement between the measured and the equivalent circuit model return losses can be noticed for frequencies below f_c.

a)



b)

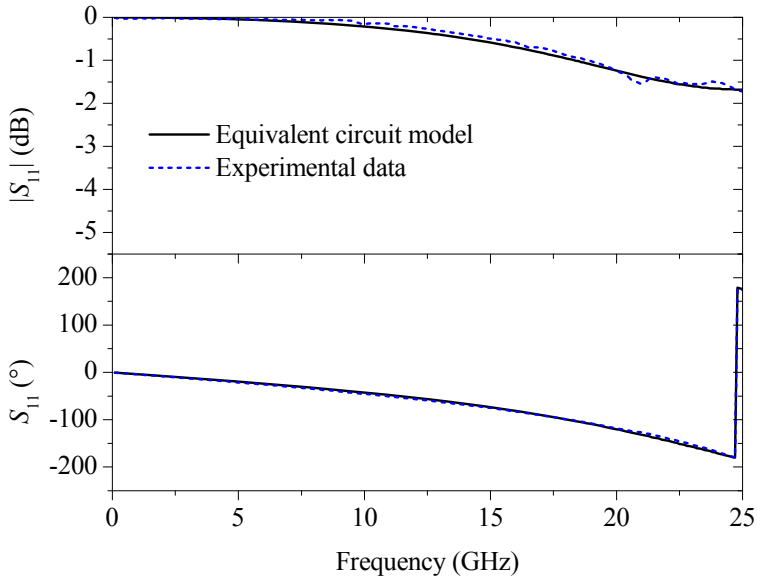


Fig. 4.15 a) Equivalent circuit model implemented in ADS, b) Measured return loss compared with simulation using the equivalent circuit model before f_c.

At this point, seen Fig. 4.15b, the parasitics of the via are correctly determined. Therefore, now is necessary to determine the couple that exists among the via and the waveguide once the via starts to radiate electromagnetic waves. For this reason, consider the terminations of the RWG shown in Fig. 4.7 as perfectly coupled loads. As previously mentioned in Chapter 3 (Section 3.1), using coupled loads allow determining the impedance of the transition (Z_t) in a simple way and the distance l can still be any arbitrary distance. Thus, the 3D-model is simulated to obtain such coupling from the simulated two-port Y-parameters but now for $f > f_c$. In this case since L_{via} is already determined, Z_{eq} can be determined as:

$$Z_{eq} = -\frac{1}{Y_{21}} - j\omega L_{via} \tag{4.13}$$

and the transition impedance can be obtained from (4.13) in the next way:

$$Z_t = Z_{eq} - \frac{Z_0}{2} \tag{4.14}$$

where Z_0 is the characteristic impedance of the waveguide (see Fig. 4.6).

Fig. 4.16 shows Z_t versus frequency curve. At this point is important to said that since Z_t is associated with the evanescent modes at the surroundings of the via, it presents a pure reactive behavior which originates that $\mathrm{Re}(Z_t) \approx 0$.

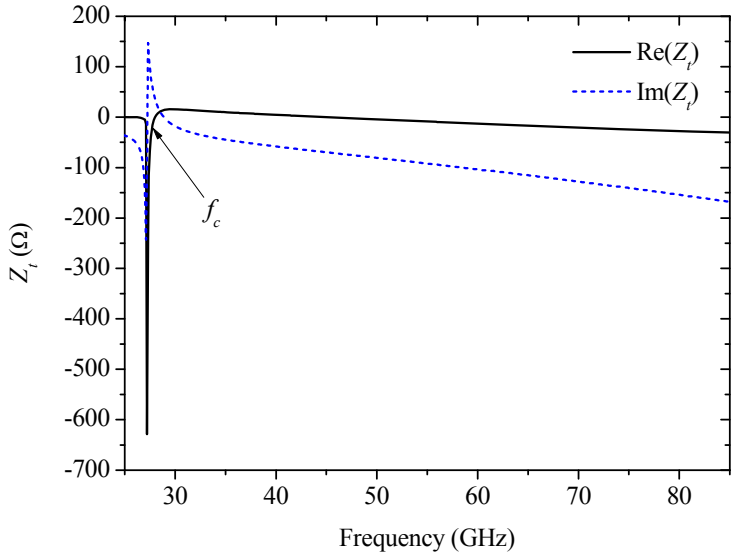


Fig. 4.16 Z_t versus frequency curves, related to the nonlinear effects surrounding the via.

As is above mentioned, perfectly coupled loads are used as terminations to determine Z_t in a simple way and not have to deal with the distance in which evanescent modes are present. However, bear in mind that the fabricated SIWs use electric-wall terminations at the outsides, so that, coupled loads must be changed to short-circuit (SC) terminations. In Chapter 3 (Section 3.1), for the simplicity of the model the via is placed at the middle along the length of the structure (see Fig. 4.7). Nevertheless, since Z_{in} only

represents the parallel impedance of two short-circuit terminated transmission lines, it can be rewritten as:

$$Z_{in} = Z_0 \frac{\tanh\left(\gamma\left(L_l - L_t\right)\right)\tanh\left(\gamma\left(L_r - L_t\right)\right)}{\tanh\left(\gamma\left(L_l - L_t\right)\right) + \tanh\left(\gamma\left(L_r - L_t\right)\right)} \tag{4.15}$$

where L_l and L_r represent the distances from termination 1 and termination 2 to the center of the via respectively whereas L_t represents the distance within the evanescent modes are present.

Hence, Z_{eq} using SC terminations can be determined as:

$$Z_{eq} = Z_t + Z_{in} \tag{4.16}$$

In order to demonstrate the above mentioned, a full-wave simulation of the 3D-model depicted in Fig. 4.7 using SC terminations but now with L_l = 40 mil and L_r = 428 mil is carried out. Fig. 4.17 shows Z_{eq} versus frequency curves using (4.16), and full-wave simulation.

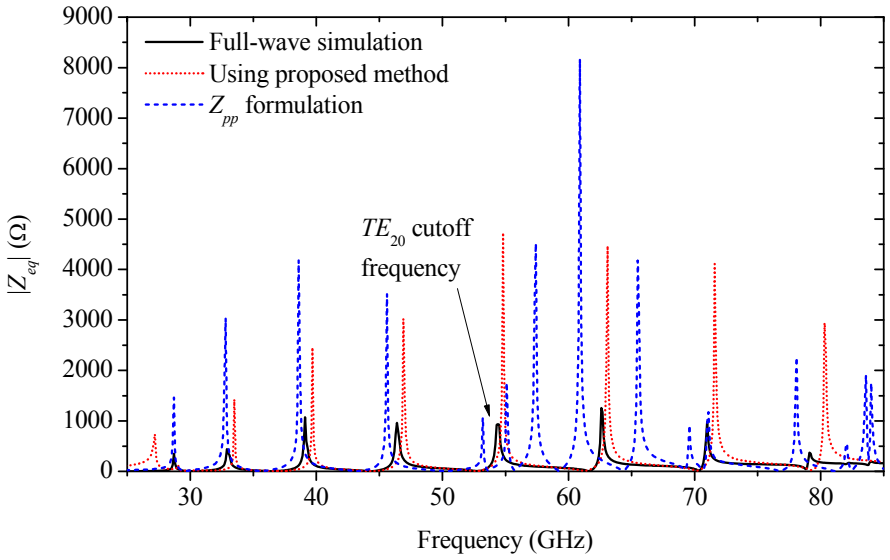


Fig. 4.17 Equivalent impedance for the via transition obtained from full-wave simulations, using the proposed method, and the Z_{pp} formulation.

Since in this case Z_{eq} corresponds to the input impedance of a via surrounded by rectangular-shaped electric walls, this parameter can also be determined using the Z_{pp} formulation [25], which is also shown in Fig. 4.17. As can be seen, there is a good agreement between the extraction using the proposed method and full-wave simulations for the entire useful bandwidth. For the case of the Z_{pp} formulation also good prediction of experimental data can be achieved but requiring previous knowledge of the effective dimensions and material parameters of the structure. Bear in mind, however, that in the studied structures this formulation failed to accurately reproduce Z_{eq} above approximately 54 GHz (see Fig. 4.17). This is due to the fact that Z_{pp} considers all the

propagation modes supported by the structure even though some modes are intentionally omitted, such as the TE_{20} mode in the SIWs studied here.

In Chapter 3 (Section 3.2) is explained how L_t is left as a fitting parameter. In this regard, Z_{eq} obtained from full-wave simulations shown in Fig. 4.17 is used for the determination of L_t by means of correlating it with (4.16). Fig. 4.18 shows the corresponding L_r versus frequency curve once the correlation is made. As can be noticed, an important frequency-dependence of L_t is shown.

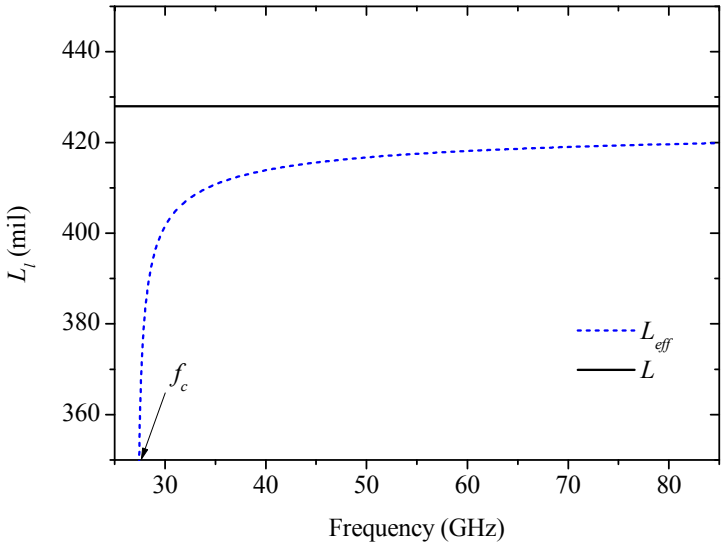


Fig. 4.18 L_{eff} versus frequency curve compared with L_r. In this case L_r = 428 mil.

At this point, all the parameters involved in the characterization of the via embedded in dielectric substrates and its coupling with the waveguide are known. Finally, to complete the verification of the proposed model it is necessary to reproduce the measurements of the fabricated SIWs with a block-cascade model.

4.4 Experimental Validation

Fig. 4.19 shows the equivalent circuit for the SIW depicted on Fig. 4.2. This model includes the equivalent circuit for the parasitics of the via and the via-to-SIW transition at each port of the structure. In addition, the homogeneous section of SIW is represented by means of its *S*-parameters matrix obtained from the well-known ABCD matrix for uniform transmission lines, whereas the small electric wall-terminated sections of SIW with a length L_s located at the outer sides of the structure are represented by means of the input impedance $Z_w = Z_0 \tanh(\gamma (L_s - L_t))$.

Fig. 4.20 shows the comparison between the measured *S*-parameters and the simulations using the proposed equivalent circuit model for one of the fabricated SIWs. As can be seen in this figure, excellent simulation-experiment correlation is achieved from the cutoff frequency of the TE_{10} mode to that corresponding to the TE_{30} mode, which is the useful bandwidth of the SIW.

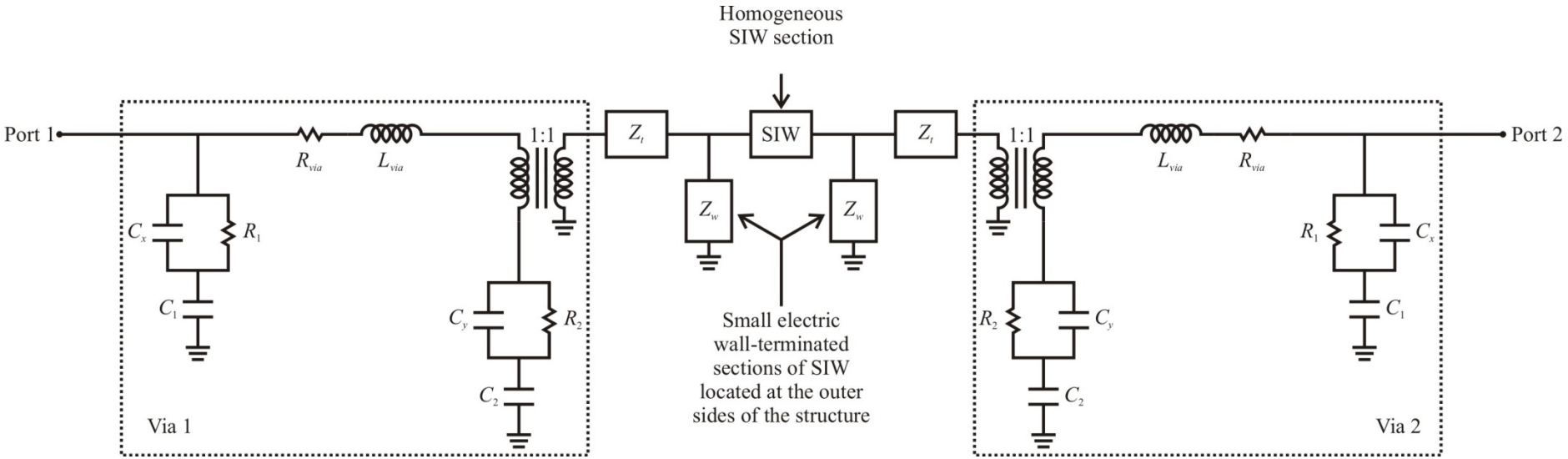


Fig. 4.19 Block-cascade model implemented in ADS for the verification of the proposed method.

Notice that in spite of previous experimentally validated approaches [7], [48], excellent correlation was obtained for S_{11} in a relatively wide frequency range. This is not only due to the use of probes instead of coaxial test fixtures for minimizing the insertion losses, but also due to the reliable extraction of the frequency-dependent Z_t parameter for modeling the via transition.

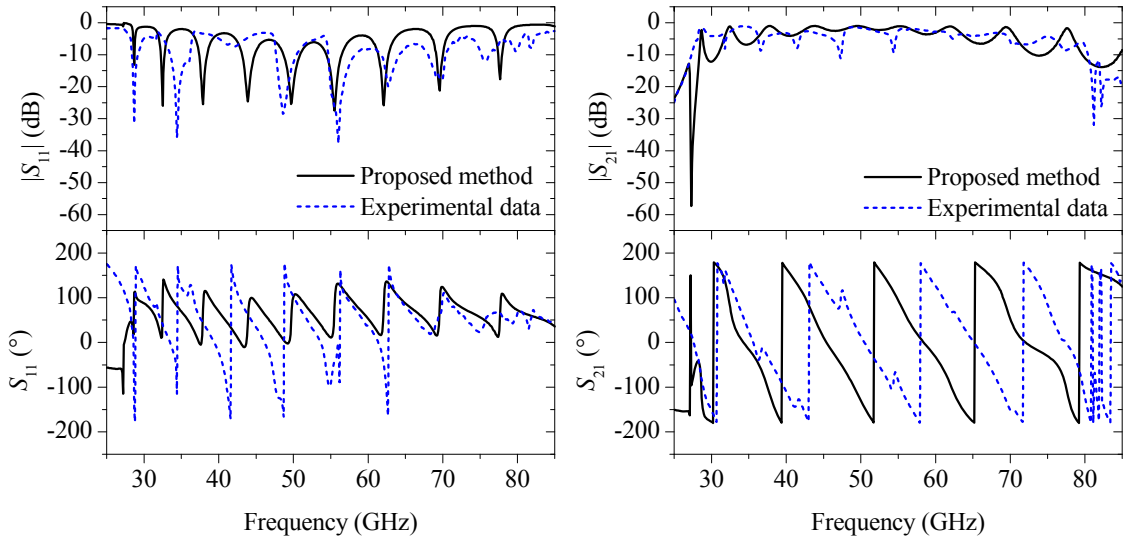


Fig. 4.20 Measured return and insertion losses compared with the simulations using the proposed equivalent circuit for an SIW with L_{max} = 10.9 mm.

4.5 Conclusions

In this Chapter, the topology proposed in Chapter 3 for the characterization of vias embedded in dielectric substrates surrounded by ground vias were verified and validated with a set of SIWs fabricated on PCB.

As can be noticed through the process of validation, the model proposed for the characterization of vias allows changes in its methodologies for the parameter extraction, thus showing the adaptability of the model to new circumstances.

Additionally, after the phenomena occurring in transitions like the one studied here is fully understood complex structures can be simplified in such a way that, simulating and extracting the equivalent circuit parameters from a simpler structure allows modeling more complex structures (like the SIWs studied here or packages). Thus, the proposal also helps in the reduction of the computational costs.

Chapter 5

General Conclusions and Future Work

A detailed analysis for identifying the impact of high-order effects on the propagation of high-frequency signals through vias on PCBs was carried out in this thesis. The modeling of these interconnects is based on the analysis of full-wave simulations, whereas the representation of each physical effect occurring in the transition is achieved with lumped elements in an equivalent-circuit model. As a result of the analysis performed to vias embedded in dielectric substrates, some observations and important conclusions are presented in this final chapter.

A via used to carry a signal in a multilayer structure can be seen as an electrical discontinuity which introduces a mismatch between two transmission lines embedded in an interconnection channel. This mismatch introduced by vias can even let the interconnection channel useless at certain frequencies. Moreover, since the package can behave as a resonant cavity, at the frequencies of resonance the transmission of signals through the via is null. In addition, the losses introduced by the via, in the range of frequencies studied in this thesis, cannot be neglected anymore causing loss of expensive RF power. Thus, the corresponding results obtained from the analysis of the radiation effects are useful for optimization purposes. For instance, in chapter 4 (Fig. 4.17) an example of the equivalent impedance seen by the signal when is passing from the via the packages is exposed. The magnitude of those peaks are closely related with the transmission coefficient of the via, since the higher the magnitude of those peaks are, the more the energy of the signal passing through the via is lost.

One technique used to minimize the effect of resonances in packages is using a proper configuration of the ground vias array surrounding the signal via. Nevertheless, this makes the package to behave as a cavity resonator. Hence, in this project the radiation of the electromagnetic waves inside the package is restricted in only one direction. This allows that the package can be seen as a region of transition embedded among two SIWs. Therefore, in Chapter 3 an approach for the characterization of this transition region is presented.

The modeling technique presented in this thesis allows changes in its methodologies for the parameter extraction, thus showing the adaptability of the proposal to new circumstances. In addition, although the validation is carried out with relatively simple structures, this can gives us important insights into the impact of electromagnetic radiation in more complex structures such as packages. Consequently, the analysis presented in this thesis becomes more important since modeling techniques for packages are one of the most important areas studied for signal integrity engineers these days due to the importance of packages in today’s electronic industry.

In accordance to the previous discussion, the contributions of this thesis can be summarized in the next points:

1. The main contribution derived from the analysis presented throughout this thesis is, the formulation of a novel topology for the modeling of vias embedded in dielectric substrates surrounded by ground vias. This model is described based on full-wave simulations and circuit-oriented approaches, obtaining a very accurate and physical representation of the transition. Moreover, this allows identifying the elements that negatively influence the signal integrity. In this regard, since the main adverse effect caused by vias is a mismatch, the proposal can be used for optimization purposes.

2. Introduce the modeling of vias embedded in dielectric substrates as monopole antennas radiating electromagnetic waves inside the structure.

3. Surrounding signal vias with ground vias allow maintaining the signal energy confined. Unfortunately, this technique makes the package to behave as a resonant cavity. In this regard, several approaches have been presented in order to deal with this effect. However, these approaches consider the package as a unique structure whereas, in this thesis, the transition region where the evanescent modes are present is isolated. This allows that the rest of the package can be modeled with simple SIW sections.

4. Determine that the area where the region of transition is present varies with the frequency. Thus, a reliable way to extract this parameter is discussed in this thesis.

As a result of the mentioned above, future research is proposed to overcome the problems in the packages seen throughout this thesis. Thus, in the near future new guidelines to reduce or suppress the effects of parasitic propagation in packages will be developed. For this reason, in this final part of the chapter, some research lines are discussed.

The materials that have traditionally been used for implementing PCBs for high-speed applications are reaching their corresponding technological and physical limits. For this reason, new materials will have to be developed in order to support the expected speeds of the operation signals without introducing undesirable effects. The model proposed in this thesis only considers one signal via, whereas current packages may have thousands of vertical transitions and devices embedded in it. For this reason, models for additional effects, such as crosstalk, need to be included in the modeling of vias embedded in dielectrics substrates. Moreover, during the analysis of the electromagnetic radiation, it is observed that the distance (L_t) occupied by the region of transition does not present a constant value; instead, it varies with the frequency. In this

thesis, this distance is left as a fitting parameter. For this reason, another research opportunity is the determination of an analytical closed-form expression for the calculation of L_t.

In addition to the previous points, the lack of comprehensive data for the frequency dependence of the Rogers RT/Duroid 5880 in the state of the art, forces that, the 3D-model implemented in the full-wave simulator used for the validation of the model in Chapter 4 uses a frequency-independent model when simulating the dielectric. This necessarily reduces the agreement between the measured and the simulated results. In this regard, models for the electrical properties (i.e. ε_r and $\tan\delta$), such as the Debye-model for the dielectric constant, need to be considered in the characterization of the dielectric.

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