A PVT Compensated Active Inductor Based VCO on SOI CMOS Technology

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INAOE

To my parents Maria Bohórquez, Mario Astro
and to my loved wife Ana Luisa.

To God.

Contents

ACKNOWLEDGMENTS

First of all, I would like to thank God for enabling me to get up every day and give me the needed strength for accomplishing my goals and dreams. But overcoat, I am very grateful to him for having brought to my wife into my life.

Of course, I would like to show my gratitude to the woman who gave me the life, my mom Maria. Without her infinite support, confidence and love, it had been very difficult to be where I am. In addition, my dad Mario and my brothers Alejandro and David, without their happiness, love and support would not be itself.

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SUMMARY

TITLE:

A PVT Compensated Active Inductor Based VCO on SOI CMOS Technology. [1]

AUTHOR:

Ricardo Astro Bohórquez. [2]

KEY WORDS: Active Inductor, VCO, SOI, phase noise, PVT variations.

DESCRIPTION: In this work the design of a PVT compensated active inductor based VCO is presented, with the aim of providing a robust alternative to the problem of limited tuning range of the passive LC VCO.

Initially, the different characteristics of some typical structures of active inductors are analyzed, and some factors that make this sort of circuit sensitive about PVT variations are identified. Subsequently, an active inductor based on gyrator principle, along with a bias scheme based on a PTAT active cell, a threshold shifter and an analog current switch, are proposed in order to reduce the effect of the PVT variations. The inductor is composed by a traditional differential pair with diode-connected load and a cross-coupled pair for increasing the inductive frequency range. In addition, some cross-coupling of signal are added to reduce the inductance value and the effect of the mismatch on the circuit performance. The frequency results show an inductance between 4 and 14 nH, with a maximum deviation of its nominal value (6.860 nH) of 8.81% with regard to fabrication process and temperature; meanwhile, the statistical analysis yields a mean value of 6.952 nH and an standard deviation of 0.249 nH. The power consumption of the whole active inductor is between 1 and 3.1 mW@1 V for the mentioned inductance range.

The proposed inductor is inserted in a variation of the NMOS Cross-Coupled pair with current sinker. The obtained results show a center frequency of 5.36 GHz, with a phase noise of -88 $\frac{dBc}{Hz}$@1 MHz. For its part, the total frequency band covers from 3.192 to 7.501 GHz, yielding a frequency tuning range of 80.39 %. On the other hand, the transient response yields an startup, transition and settling time of 250, 300 and 600 ps respectively. Lastly, the results of the statistical analysis yield a mean value and an standard deviation of 5.381 GHz and 411.03 MHz respectively for the center frequency.

[1] Master project

[2] National Institute for Astrophysics, Optics and Electronics. Advisor Ph.D Guillermo Espinoza Flores-Verdad.

RESUMEN

TÍTULO:

VCO Basado en un Inductor Activo Compensado en PVT en Tecnología SOI CMOS. [3]

AUTOR:

Ricardo Astro Bohórquez. [4]

PALABRAS CLAVE: Inductor Activo, VCO, SOI, ruido de fase, variaciones PVT.

DESCRIPCIÓN: En este trabajo se presenta el diseño de un VCO basado en un inductor activo compensado en PVT, con el objetivo de proporcionar una alternativa robusta al problema de rango de entonado limitado del VCO de tanque pasivo.

Inicialmente, se analizan las diferentes características de algunos inductores activos típicos, y se identifican los factores que hacen sensible a este tipo de circuitos respecto a las variaciones PVT. Posteriormente, se presentan un inductor activo , basado en el principio del girador, y un esquema de polarizacion compuesto por una celda activa PTAT, un desplazador de umbral y un conmutador analógico de corriente, con el propósito de reducir el efecto de las variaciones PVT sobre el valor nominal de la inductancia.

El inductor está formado por un par diferencial, cargas de diodo y un par de acople cruzado para incrementar el rango de frecuencia inductivo. Adicionalmente, algunos acoples cruzados de señal son agregados para reducir la inductancia y el efecto del *mismatch* sobre el deseñpeño del circuito. Los resultados en frecuencia muestran una inductancia entre 4 y 14 nH, con una desviación máxima de 8.81% del valor nominal (6.860 nH) con respecto al proceso y la temperatura; mientras que el análisis estadístico da una media de 6.952 nH y una desviación estándar de 0.249 nH. El comsumo de potencia del inductor completo se encuentra entre 1 y 3.1 mW@1 V para el rango de inductancia mencionado.

El inductor propuesto es insertado en una variante del par de acople cruzado NMOS con sumidero de correinte. Los resultados obtenidos muestran una frecuencia central de 5.36 GHz, con un ruido de fase de -88 $\frac{dBc}{Hz}$@1 MHz. Por su parte, la banda de frecuencia cubre desde 3.192 a 7.501 GHz, generando un FTR de 80.39 %. Por otra parte, la respuesta transitoria muestra un tiempo de arranque, transición y asentamiento de 250, 300 y 600 ps respectivamente. Por último, los resultados del análisis estadístico dan una media y una desviación estándar de 5.381 GHz y 411.03 MHz para la frecunecia central respectivemente.

[3] Proyecto de Maestría

[4] Instituto Nacional de Astrofísica, Óptica y Electronica. Director Dr. Guillermo Espinoza Flores-Verdad.

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Acronyms

AAC Amplitude Automatic Control.

BOX Buried Oxide.

BW Band-Width.

CC Cross-Coupled.

CCII Current Conveyors II.

CMFB Common-Mode FeedBack.

CMRR Common-Mode Rejection Ratio.

CNR Carrier-to-Noise Ratio.

CTAT Complementary-To-Absolute-Temperature.

DIBL Drain-Induced Barrier Lowering.

FB Floating Body.

FOM Figure-Of-Merit.

FTR Frequency Tuning Range.

GIC Generalized Immittance Converter.

ILD Inter-Layer Dielectric.

ITR Inductance Tuning Range.

KCL Kirchoff's Current Law.

LDO Low Drop-Out.

PBT Parasitic Bipolar Transistor.

PCs Process Corners.

PD-SOI Partially-Depleted Silicon-On-Insulator.

PTAT Proportional-To-Absolute-Temperature.

SNR Signal-to-Noise Ratio.

TEOS Tetra-Ethyl-Ortho-Silicate.

UWB Ultra Wide Band.

VCO Voltage Controlled Oscillator.

Chapter 1

Introduction

The notable growth of the wireless communication technology has created the need to design transmission and reception systems for high performance, particularly efficient in the bandwidth distribution in order to provide support to a large quantity of users. The responsible of the Band-Width (BW) distribution in a transceiver is the frequency synthesizer block, which translates the output frequency and selects the transmission channel [1]. The frequency synthesizer efficiency is limited by the specifications of the Voltage Controlled Oscillator (VCO), mainly by its phase noise and tuning range. As core cell, VCO limits the selectivity of the frequency synthesizer when its phase noise degrades the system Signal-to-Noise Ratio (SNR) at once to disturb proper down-conversion process as it is shown in Figure 1.1, and its limited tuning range prevents the system covering completetly the operation band.

LC tank based VCOs take up a large die area in the transceiver front-end because of the inductor. Generally, the inductor has a low quality factor and self-resonant frequency, and a fixed inductance, making it a limiting factor in the VCO operation and performance. Due to these problems of the spiral inductor, it has been unleashed the trend to use active inductors, because of its high and tunable inductance and quality factor, high self-resonant frequency and low area compared to spiral inductors.

Active Inductor and even so VCO performance are directly related to both fabrication process and operation conditions, which are known as PVT (Process, Voltage and Temperature) variations. As the dimensions have been shrunk, the variation of physical and electrical parameters of transistors, whose extreme values are known as worst-case corners, has increased considerably. Different combinations of these process corners cause serious changes on the design variables and therefore in the circuit behavior, entailing a wide intra-

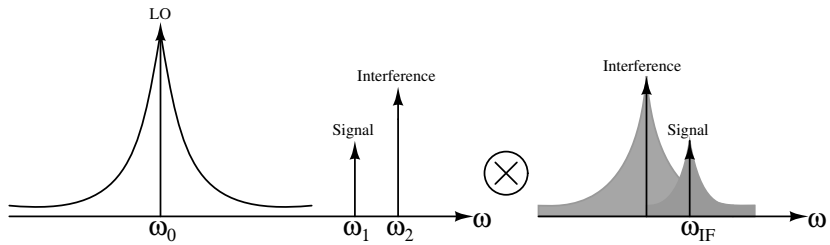


Figure 1.1: Effect of phase noise in a wireless receiver.

die and inter-die performance range [2]. The power supply used in most integrated circuits is a battery with a specific chemical composition. In accordance with its structure and load conditions, batteries present substantial current and voltage variations which modify the operation conditions for the devices, and therefore, the circuit's performance [2, 3]. The temperature is undoubtedly one of the most critical and demanding factors on the operation and design of an integrated circuit. Its changes and gradients inside an integrated circuit cause considerable modifications in some factors such as carrier mobility, threshold voltage and mismatch between devices [4].

Each one of these factors is a serious problem for correct operation of a MOS integrated circuit, but a combination of them can result in a significant loss not only in performance, but also in reliability and a decrease of the yield. This situation is unacceptable for the industrial environment, where reliability represents a larger number of sales and the yield represents bigger profits. Trying to solve these problems, the integrated circuit designers of the industry use centering, calibration and adjustment techniques, increasing area and power consumption, which means higher cost and autonomy loss. Taking into account the previously mentioned, in this master project is proposed the compensation of PVT variations in an intrinsic way on an active inductor used in a VCO. That is, the compensation is generated by the structure itself, and the bias scheme used to make the circuit. With this design methodology, a higher simplicity, robustness and performance are achieved over the ones achieved using external correction structures.

1.1 Voltage Controlled Oscillator, VCO

There are a lot of ways to classify oscillators depending on their basic properties, functionality or pole patterns. Each one of these parameters gives rise to a range of appropriate topologies depending on the specific application. For example, the strong requirements

in wireless communications systems have led to the most widely used VCO topology implementation be LC lumped resonator due to its low phase noise, while to control the operation of digital circuitry, a square wave oscillator is desired due to its lower noise sensitivity at zero-crossings [5].

A large number of works have been published about oscillators, which focus on getting the best performance using the lowest power consumption and area. Each one of these works attacks a performance parameter, or applies either centering or optimization techniques. The most common parameters used to quantify the oscillator performance are center frequency, frequency tuning range, power consumption, area, quality factor and phase noise. These parameters present strong trade-offs among them, making difficult to achieve the required performance. In the following subsections, the previously mentioned, and others, parameters will be described and specifically analyzed.

1.1.1 Tuning Range and Linearity

The center frequency, tuning range and its linearity are specifications set by the application, and have a considerable impact on the oscillator design difficulty level. The center frequency determines key points such as tank quality factor-Q, optimum value for elements and the influence of the parasitic elements associated to devices and interconnections. The value for this frequency is fixed by communication standards which regulate and distribute the electromagnetic spectrum [6].

Together with center frequency, the oscillator tuning range plays a very important role in the system's performance. This parameter is defined as the frequency span achieved by the oscillator, and it is set by factors like fabrication technology, tuning structure and parasitic elements. Generally, this frequency tuning has been implemented in oscillators through PN diodes, MOS transistors operating in either inversion or accumulation mode and, in lesser degree, MEMS capacitors. The tuning bandwidth is expressed as a percentage of the center frequency and is a function of the ratio between maximum and minimum value of varactor capacitance as it is shown in Equation 1.1 [7].

$$TR = \pm \frac{C_{max} - C_{min}}{C_{max} + C_{min}} \tag{1.1}$$

A linear behavior on the tuning range is highly desired to reduce the complexity implementation of the frequency synthesizer [1]. The non-linear nature of the varactor

limits both tuning range and linearity making it difficult to achieve the requirements for a large frequency band like in Ultra Wide Band (UWB) communication standard [6]. To characterize the linearity of tuning range the VCO gain constant is used, which is defined as the derivate of function f_{osc} vs V_{Tune}, as shown in Equation 1.2 [8].

$$K_{VCO} = \frac{\partial f_{osc}}{\partial V_{Tune}} \tag{1.2}$$

1.1.2 Quality Factor

The quality factor-Q is a very important parameter in the oscillator performance, since it influences on the power consumption, phase noise, frequency drift, and area of tank lumped elements. There are plenty of definitions for this parameter; however, the most fundamental one is as follows [9]:

$$Q \equiv \omega \frac{E_{stored}}{P_{Avg-Dis}} \tag{1.3}$$

Where ω is the resonant frequency, E_{stored} and $P_{Avg-dis}$ are the stored energy and average power dissipation per cycle respectively. This basic definition doesn't say anything specific about what stores or dissipates the energy, allowing to compare both resonant and non-resonant circuits. In resonator based oscillators, a high-Q enables oscillator to obtain a low-phase noise due to inverse proportion to the square of the quality factor. Moreover, frequency drift is reduced because the influence of active device reactances on output signal is decreased. It is worth mentioning that isolating the resonator from these reactances, reduces temperature effects [10].

The quality factor of lumped elements like those used in LC-tank oscillators is mainly determined by the fabrication technology and the geometries used to layout the elements. Ten years ago the tank's Q (Q_T) was limited by the inductor's Q (Q_L), due to the low imaginary impedance associated to it at the resonant frequency. However, since the increase of the operation frequency, as a result from the shrinking of the devices dimensions, the Q_L has rapidly increased, being nowadays the varactor's Q (Q_V) the limiting factor to get high quality factors in the resonant tank. It should be mentioned that active inductors were proposed to achieve high-Q, tuning characteristics and low area compared to passive inductors, making them an attractive option to integrate low-cost and low-power systems [11].

1.1.3 Pulling and Pushing

Ideally, the oscillation frequency and amplitude of the output signal must be independent of the power supply. However, as power supply presents drifts with time, temperature, and load variations, the active devices junction capacitances present variations causing changes on the output signal characteristics. In addition, noise in the supply lines causes significant FM and AM modulation modifying the spectral content of the signal. This dependence is known as Pushing. Pushing is measured by obtaining the output frequency versus supply voltage. To solve this problem, a filtering to power supply can be applied, but an optimum solution is to design a tank with high Q to isolate the resonant circuit from active-device reactances.

Changes on the coupled load to the oscillator cause variations on the center frequency of the oscillator. This effect is referred as Pulling, which can be measured by computer simulation or direct measurement by varying the load impedance while are observed the cascade phase response, the reflection coefficient or the actual oscillation frequency. Pulling is typically specified for a load with a given return loss magnitude at any angle. A return loss magnitude of 12 dB (VSWR=1.671) is commonly used to define a pulling specification. To minimize the load effect on the oscillator output signal a buffer is used to isolate the resonant tank from load impedance variations.

1.1.4 Output Power

The output signal power is a very important parameter in the oscillator performance. Generally, this parameter is referred to a load impedance about 50 or 75 Ω. However, due to load variations a buffer is usually used to isolate the resonant tank. With this, the oscillator output power level is influenced by the buffer operation.

If an oscillator provides a high power level to the next stage, for example a doubled-balance mixer, it is beneficial since it reduces the noise figure of this type of mixer. Additionally, a high output power level allows decreasing the phase noise. The output power level is affected by the oscillator operation mode and therefore by its power consumption. That is, if the oscillator operates in current mode the output level is proportional to its tail current, whereas if it operates in voltage mode is independent of power consumption and it is defined by the operation ranges of transistors. Although a high oscillator output level is desired, a large voltage swing can give rise to problems like saturated transistors in the next stage and cause duty-cycle variation or corrupt the oscillator waveform [5].

1.1.5 Phase Noise

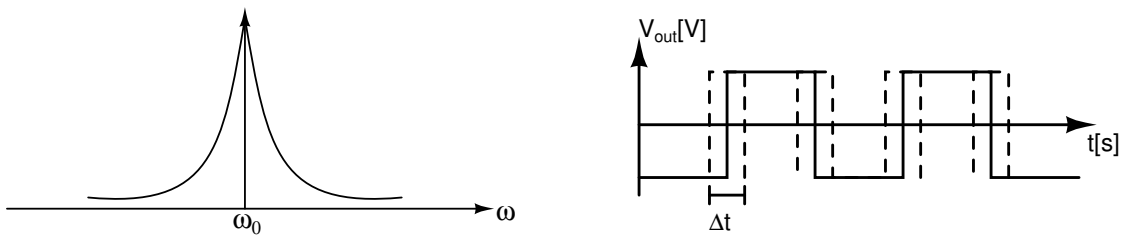
Undoubtedly frequency instability is the main and more complicated specification to accomplish on the design of an oscillator. This factor has been subject of studies and analysis since its identification and it has been modelled in a lot of ways. However, it is very difficult to describe it mathematically in a precise form because of its stochastic behavior and non-linearities associated to the region transitions of transistors, and different noise and interference sources such as thermal, flicker, substrate and supply noise. Because of these noise and interference sources, the oscillator output signal has fluctuations in its amplitude and frequency, described in a general form as shown in the Equation 1.4. These fluctuations cause a corruption of the spectral purity of the output signal which can be characterized in both time and frequency, just as it will be described next [12].

$$V_{out}(t) = V_o[1 + A(t)]f(\omega_o t + \Phi(t)) \tag{1.4}$$

In the frequency domain, these amplitude and phase fluctuations are observed as power sidebands close to the center frequency known as phase noise, whereas in the time domain the fluctuations are observed as variations in zero-crossing and is known as timing jitter. In the Figures 1.2(a) and 1.2(b) phase noise and timing jitter are respectively shown. The measures used to quantify the frequency instabilities have a practical sense according with the application. For example, the oscillator used in a transceiver is harmonic and therefore it is more useful to analyze the performance of the phase noise. Whereas to control digital circuitry the oscillator provides a square wave and so the timing jitter is a more descriptive parameter. Considering that the proposed oscillator in this thesis is harmonic, from this moment the phase noise will be used to quantify the frequency instabilities in the oscillator. For a detailed analysis of phase noise in LC and ring oscillators the reader can refer to [12].

The most common measure used to quantify the phase noise is known as Carrier-to-Noise Ratio (CNR). This factor is calculated by getting the ratio between the carrier power at f_o and the noise power in a bandwidth of 1 Hz to Δf_m away from the carrier, as shown in Equation 1.5. It should be noted that the power noise in Equation 1.5 includes the effect due to both amplitude and phase fluctuations.

$$CNR(\Delta f_m) = -10log(\mathscr{L}(\Delta f_m)) = -10log\left(\frac{P_s(f_o)}{P_n(f_o + \Delta f_m)}\right)\left[\frac{dBc}{Hz}\right] \tag{1.5}$$



(a) Phase noise. (b) Timing jitter.

Figure 1.2: Frequency instabilities measured in the frequency and time domain.

Once some performance specifications of the oscillator were described, a revision of LC oscillator's core, the resonant tank, will be made. In this revision is found a short description of its advantages, disadvantages and some implementation alternatives.

1.2 LC Tank

The resonant tank of oscillators for wireless communication systems is composed by a varactor and an inductor, because of its low phase noise. This property is a result from its capacity to store either electric or magnetic energy in each half-period oscillation [5]. The quantity of stored energy depends on the quality factor of the resonant tank. As it was mentioned, at low frequency the quality factor is limited by the inductor, whereas at high frequency the varactor is the limiting factor. As the quality factor is larger, the spectral purity increases too. However, a very high Q causes an increment in the settling time of the oscillator. In some communication standards as TDMA based, an extremely large settling time is unacceptable, since the channel switching must be fast to transmit the information in an efficient way [5].

As it was previously mentioned, the varactor of the tank has been implemented in some different ways, the PN junction, the MOS transistor operating in both inversion and accumulation mode and, a lesser degree, MEMS capacitor. Each one of these alternatives has specific advantages and disadvantages, and its use is mainly defined by the application restrictions.

On the other side, inductors are traditionally implemented by means of a spiral inductor. This type of inductors fabricated on silicon present some important characteristics such as: a constant inductance value, a high-signal linearity, low noise, besides being

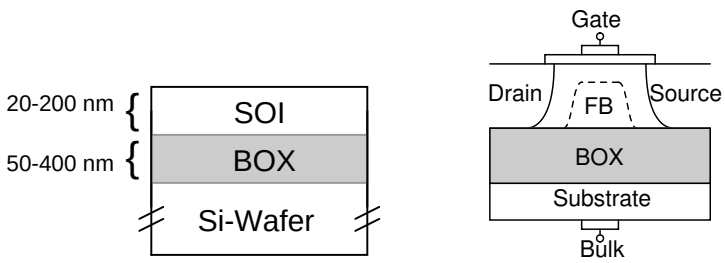
robust to PVT variations. Nevertheless, it should be mentioned that the performance of those inductors is limited by intrinsic characteristics associated to the layout. Among the limitations it can be found: a low quality factor, a low self-resonant frequency, a small and non-tunable inductance and a prohibitively large silicon area. Particularly, due to the need for a large silicon area to fabricate spiral inductors, it has been unleashed a great interest on the synthesis of inductors using active devices, allowing to minimize silicon consumption and subsequently fabrication cost, besides to improve its quality factor even so the selectivity of the oscillator.

Each one of the performance specification of the oscillator mentioned in the previous section is related in a direct way with the LC tank and therefore to PVT variations, particularly the fabrication process variations. In this project a Partially-Depleted Silicon-On-Insulator (PD-SOI) CMOS 45 nm technology is used, whose most important characteristics will be briefly described in the next section.

1.3 SOI CMOS Technology

During last years Bulk-CMOS became the dominant technology due to its attractive characteristics like high integrability, high performance and low power consumption. However, because of the technology scaling a set of effects such as the carrier mobility degradation, the gate tunneling current and the increment of PN junction leakage current have done less feasible the development of high-performance systems in this technology. Due to the aforementioned factors, the industry has been moving toward the SOI CMOS technology, since it has features of low parasitic apacitances which increases the speed operation in almost 30% regarding Bulk, while the power supply decreases. However, the advantages of this technology are not limited to the areas of speed and power, this also include good radiation hardness, the ability to withstand high temperatures and the capacity to handle high voltages [13,14]. In addition, this technology allows the fabrication of MEMS besides to provide flexibility in the devices design.

The SOI technology for LSI integration presents the structure shown in Figure 1.3(a), where three basic layers can be observed: the Si-substrate, the Buried Oxide (BOX) layer and the top Si or SOI layer. The first one is the traditional base wafer or support substrate. The second one, BOX layer, is made by the oxidation of Si or oxygen implantation into Si. This layer is the key for the higher performance of the SOI devices. Finally the SOI layer is a single-crystal Si layer with a certain thickness between 20 and 200 nm.



(a) SOI wafer layers. (b) PD-SOI device.

Figure 1.3: SOI technology layers and device.

According to the SOI and BOX layer thicknesses, devices are classified into several categories: fully-depleted, partially-depleted, power/high-voltages and MEMS sensors. Our interest will be focused into the second category, the partially-depleted because of the advantages in power and speed regarding fully-depleted technology. In the Figure 1.3(b) a PD-SOI transistor is shown. The name partially-depleted comes from the fact that the depletion region does not reach the bottom of the Si film, leaving a free zone known as Floating Body (FB). Due to this depletion condition and the characteristic structure, the device behavior and performance present a high dependence on the voltage of its electrically-isolated body, and the charge it contains. According to this, it is necessary an understanding of the effects that change the FB voltage in order to achieve an adequate modelling and then decrease the complexity of the design process. The FB voltage variations has its origin mainly in five mechanisms: coupling capacitance, junction capacitance leakage, active diode action, impact ionization and gate oxide tunneling. Next, some FB effects and their influence on transistor performance will be briefly described.

1.3.1 The SOI Transistor Junction Capacitances

Similarly to Bulk CMOS transistor, the SOI transistor has two diodes which form the device heart. Because of FB, these capacitances are a function of the charge contained in the FB and therefore of time. SOI transistor's most important effects associated to the junction capacitances are the capacitive coupling, leakage current and active diode action. The first one refers to the junction capacitance ability to couple changes in gate, drain and source potential into the body voltage instantaneously. This causes a change in the transistor threshold voltage and I-V characteristic curves which modifies the circuit behavior and performance.

The second one refers to the junction leakage current generated by electron/hole recombination and defects/impurities in the space charge region and high-energy carriers, which affect body voltage over an extended period [15]. It should be noted that due to FB the body-source diode is often weakly forward biased being the predominant active transport mechanism for moving charge out of the body. This effect is known as active diode action. Considering the body-source diode forward biasing and the body-drain diode reverse biasing, a parasitic bipolar transistor is made which generates a variation in the transistor's I-V curve known as Second Kink.

The PVT variations with the forward and reverse leakage current play a very important role in the dynamic performance of the circuit. The process variations change the ratio between the forward and reverse diode leakages establishing a new balance in the internal voltages of the transistor. The voltage variations affect not only the junction leakage magnitude but moreover the ratio between currents which will modify the transistor's threshold voltage and performance. Finally, the temperature changes junction leakage, threshold voltage and consequently the FB potential and so transistor behavior and performance.

1.3.2 The Impact Ionization

As the technology scaling reaches an atomic level, some effects like impact ionization become more important and influential on the circuit performance. Generally in a IC almost all transistors operate in the saturation region where the channel length presents a reduction due to the increase of the body-drain diode's depletion region. In this channel zone high electrical fields are present which provide high energy to the carriers who collide with lattice atoms and generate hole-electron pairs.

The impact ionization leads to damage in the silicon lattice by the hot carrier effect by three modes: conducting, nonconducting and substrate hot carriers. Due to the BOX layer, the substrate hot carriers are not present in SOI technology. For analog circuits the conducting hot carriers is the most worrying mechanism, since this appears when the transistor operates in saturation region causing injection of carriers into the gate insulator and FB. This causes not only damage in the silicon interface and a wear out mechanism but also generate positive charge which accumulates in the device isolated body causing a reduction of the threshold voltage and so a variation of transistor's I-V curve known as First Kink [15].

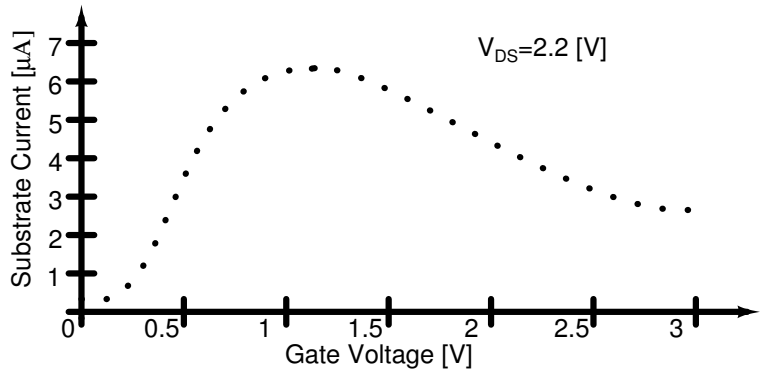


Figure 1.4: Impact ionization as a function of gate voltage.

In Figure 1.4 the impact ionization behavior is shown with regard to gate voltage and a fixed drain voltage. As it can be observed, according to the channel saturation degree, the impact ionization presents a different value. That is, if the transistor operates in the triode-saturation edge, the electrical field in the pinched-off channel is not very high and the hot carriers' energy presents a normal value. As the saturation degree increases, hot carriers' energy is higher and the impact ionization has a great impact on the charge contained in the FB.

1.3.3 Floating Body Effects

1.3.3.1 History Effect and Threshold Voltage Variability

The history effect establishes that the PD-SOI transistor's I-V characteristic curves are no longer constant, but dependent on the amount of charge contained in the device body at any given time. Considering either analog or digital operation, the quantity of charge contained in the device body is mainly dependent on factors like: previous state and schematic position of the transistor, slew rate of input and load capacitance, channel length and process corners, power supply, temperature, operating frequency and specific switching factor [15]. All the mentioned factors generate a body potential range which determines the transistor performance. When a combination of voltages is applied to the transistor, the body potential changes in search of a value that achieves an equilibrium condition. These changes in the body potential generate variations in the threshold voltage in a certain range, which is known as Body Effect in Bulk CMOS technology, and as First Kink in SOI technology where it is mainly caused by the impact ionization [15].

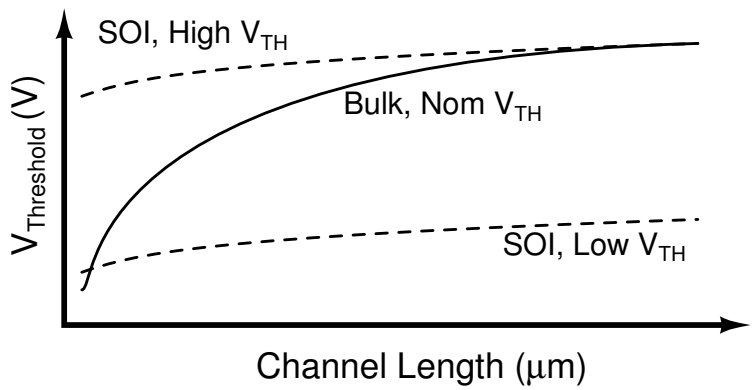


Figure 1.5: Short channel effect for Bulk and SOI CMOS technology.

1.3.3.2 DIBL and Reduced Short Channel Effects

In Bulk-CMOS short-channel transistors, the Drain-Induced Barrier Lowering (DIBL) effect is one of the most influential on the threshold voltage value. This effect can be seen either as a reduction in the height of the potential barrier near to the source, or a shrinking of the channel length which looks as a fall in the threshold voltage. In SOI transistors the DIBL effect has little meaning because of the floating body. As it was earlier mentioned, the body potential is a "free" variable who searches the balance between the different potentials and currents inside the transistor. When the V_{DS} voltage increases, charge from drain is injected toward the body through body-drain diode and due to impact ionization, generating an increase of the body potential. This fact causes a reduction of the transistor threshold voltage, giving the feeling of a increased DIBL effect without being real.

The threshold voltage reduction with channel length for short channel devices, known as short channel effect, is lower in SOI than Bulk-CMOS technology due to the floating body. This is due to the fact that floating body has the ability to adjust its potential, so that the threshold voltage roll-off will be lower than in a bulk device. In Figure 1.5 the variability of the threshold voltage is shown regarding to channel length for Bulk and high-low threshold voltage SOI devices [15]. As it can be observed, a reduced variability in both high and low threshold voltage SOI device regarding to Bulk devices is obtained. It should be noted that this behavior is very beneficial in order to tight the range of possible delays in the digital circuits.

1.3.3.3 Parasitic Bipolar Transistor

As it was earlier described, as the floating body burden, the body-drain and body-source junction diodes form a Parasitic Bipolar Transistor (PBT). This device is an intrinsic and big concern for Bulk-CMOS designers due to latch-up and snap-back effects. However in SOI CMOS, thanks to BOX layer, the latch-up is not longer concerned, because the substrate prevents the connection between the different devices and prevents the formation of a thyristor. However, this PBT has a large influence in the operation, lifetime and reliability of circuits made in SOI technology. In a digital circuit, for example, depending on last state the bipolar action can run down the logical level of an internal node, generating fails in the logic. Furthermore, the peak and duration of the bipolar current are function of factors like the channel length, operating frequency, switch factor and power supply. All these factors affect the SOI circuit's lifetime and reliability through effects such as the wear-out of the materials, the bipolar breakdown and the increase of the current levels in the interconnections [15].

1.3.4 Insulator-related Effects

The BOX layer has a big impact on the device performance due to its isothermal and amorphous nature. Some advantages and disadvantages of the SOI transistor are product of this layer. Among the most important is found the self-heating, the reduction in the diffusion capacitances, the latch-up elimination and the radiation hardness. Next, these effects will be briefly described. Nonetheless some of them have been mentioned along this document and therefore will not be mentioned again.

In Bulk CMOS, the heat generated by charge transfer is dissipated through the substrate, achieving that local device transconductance does not suffer changes. Nevertheless in SOI technology, the device is completely isolated. Underneath, the BOX layer isolates it. Up, the heat path is blocked by the SiO_2 Inter-Layer Dielectric (ILD), and laterally Tetra-Ethyl-Ortho-Silicate (TEOS) covers it. This shield prevents heat dissipation, causing an increase in the operation temperature around 20 $°C$ regarding to Bulk-CMOS. The temperature drift modifies the expected behavior and performance of the transistor, decreasing the reliability and robustness. In SOI technology the self-heating is inevitable, and the only option to decrease its effect is to reduce the current levels inside the device.

SOI devices have a bigger hardness to alpha and cosmic radiation with regard to Bulk devices thanks to BOX layer. In these devices the radiation events cause less charge

generation and collection than in Bulk transistors, since the active region through which the alpha particle passes is limited to SOI layer. Along its trajectory, the alpha particle creates ionized charge which is swept up by the reverse biased junctions, avoiding its influence on device performance.

1.4 State of the Art

A large number of works about VCOs using spiral and active inductors have been reported. However, active inductors based VCO in SOI CMOS technology were not found in the made search. Some of the most outstanding previous works are summarized in Table 1.1, where it can be observed an strong trend to increase both the frequency tuning band and the center frequency of the oscillator. To achieve it, they are using active inductors which are adjustable and show pretty interesting characteristics. Among them, the occupied area is much smaller than the spiral inductors, enabling to reduce the fabrication cost.

The works presented by Miyashita and Lin deal with and try to compensate PVT variations in order to keep low the phase noise [16, 17]. Each one of them attacks the problem in very different ways. For his part, Miyashita uses a structure consisting of two peak-detectors, a level shifter and error amplifier to adjust the tail current according to PVT variation of the core and so to obtain the lowest value for the phase noise [16]; whereas, Lin uses a Low Drop-Out (LDO) regulator and an amplitude control loop [17]. As it can be observed, to compensate PVT variations a strong increment in the complexity, area and power consumption of the circuit is required.

In [18] an active inductor based VCO is reported made in a Bulk CMOS technology. The most important about that work is the large increase in the frequency range, passing from 0.3 GHz achieved with tuning traditional mechanism to 6.3 GHz with a tunable active inductor. Besides this, the VCO occupies a very small area as a result of using the active inductor. On the other hand, the reported VCO in SOI CMOS technology uses an inductor made in high resistivity substrate achieving higher quality factors than those obtained in Bulk CMOS inductors [19]. This and other characteristics enable it to work in bands of very high frequencies like millimeter-wave. Observing the current scene, it is possible to infer that this work will cause a certain impact on the IC design, since this is the first work to report an active inductor based VCO on SOI technology, besides compensating the PVT variations in the active inductor in an intrinsic way.

Author	D. Miyashita	T. Lin	D. DiClemente	F. Ellinger
Reference	[16]	[17]	[18]	[19]
Year	2005	2007	2009	2004
Topology	*Double Cross-Coupled*	*PMOS Cross-Coupled*	*NMOS Cross-Coupled*	*NMOS Cross-Coupled*
V_{DD}[V]	1.8-3.3	1.8	1.8	1.2-1.5
Power [mW]	3.9-23.1	7.5	45	9.6-21
Center Freq. [GHz]	2.5	5.1	1.6	57-60
FR[GHz]	2.2-2.8	5.1-5.44	0.2-6.5	52.4-61.56 ; 65.8-64.2
Phase Noise [$\frac{dBc}{Hz}$]	-90@100k	-104.8@100k	-118.5@1M	-90 and -94@1M
Area [mm^2]	–	0.49	4.22e-3	0.1
Act. Inductor	No	No	Yes	No
CMOS Tech. [nm]	Bulk 180	Bulk 180	Bulk 180	SOI-CMOS 90

Table 1.1: Previous works on VCOs.

1.5 Organization of the Thesis

After making a brief introduction about the problem to solve, and the technology used for developing the project; the core of the solution is introduced: the active inductor. In the second chapter, the operation principle, specifications, advantages, disadvantages and different implementations of active inductors reported in the state of the art will be described. Subsequently, the proposed circuit for implementing the active inductor, its bias scheme and the design process for these circuits are described. After, the verification process under nominal conditions, PVT variations and lastly an statistical analysis to determine both the robustness and reliability of the circuit is shown.

In the third chapter, the active inductor is inserted in a variation of the NMOS Cross-Coupled pair with the purpose to verify its performance inside a more complex structure. A performance characterization similar to the active inductor is made, and finally a robustness and reliability analysis are carried out.

The fourth and last chapter contains a summary of the main contributions, observations and conclusions obtained along the development of this master work. To finish, we propose some future works that allow us to obtain a greater understanding and grasp on the active inductor's design.

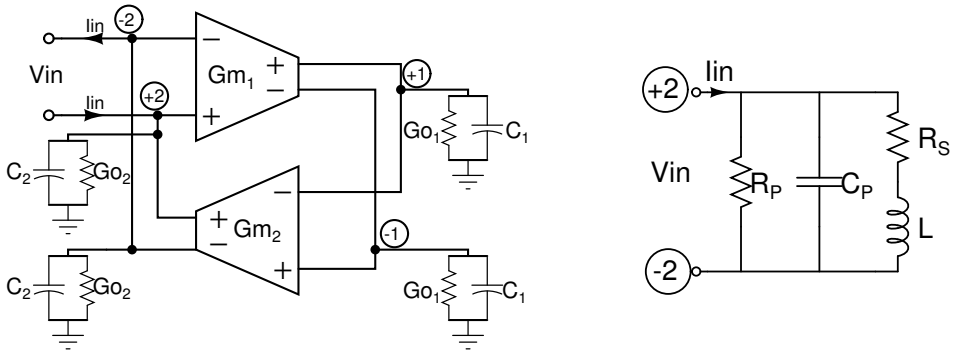
Chapter 2

Active Inductors

As it was mentioned in the previous chapter, active inductors offer some outstanding advantages over their spiral counterparts including large and tunable inductance value and quality factor, high self-resonant frequency, low area and high compatibility with digital CMOS technology. However, they present a high sensitivity to PVT variations which change drastically their characteristics and performance [20]. In order to compensate PVT variations, it is essential to understand the operation principle and various specifications used to characterize the active inductor performance, and how these are affected by those variations. Next, it will be briefly described the gyrator-C operation principle and the most important specifications used to quantify the active inductors performance such as frequency range, quality factor, noise, power consumption and linearity.

2.1 Gyrator-C Operation Principle

There exist some different ways to implement an active inductor, among them are the Generalized Immittance Converter (GIC), OpAmp, Current Conveyors II (CCII) based topologies and OTA-C techniques. Each one of these techniques has advantages and disadvantages according with their application field. Considering operation at high frequency, a higher simplicity represents a better performance and a possible reduction on area and power consumption. Because of the previously mentioned, the OTA-C based techniques have had a great reception and have become the most used techniques for implementing active inductors. The most common OTA-C based principle is gyrator-C, which will be briefly discussed below.



(a) Gyrator-C Structure. (b) Equivalent circuit.

Figure 2.1: Lossy floating active inductor.

A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor the obtained network is called gyrator-C. A real gyrator-C, that is, a lossy gyrator-C, has finite impedances and capacitances associated to transconductors, which cause a limited quality factor, frequency range and self-resonant frequency of the inductor. In Figure 2.1(a) a lossy differential gyrator-C network is shown. This differential structure allows making floating inductors, suitable for the kind of oscillator used in this work, besides to take advantage of intrinsic characteristics of this sort of differential structures.

To obtain the characteristic admittance of the gyrator-C network, the Kirchoff's Current Law (KCL) equation at nodes +1, -1, +2 and -2 is written:

$$-Gm_1(V_2^+ - V_2^-) + \left(\frac{sC_1 + Go_1}{2}\right)(V_1^- - V_1^+) = 0 \tag{2.1}$$

$$Iin + \left(\frac{sC_2 + Go_2}{2}\right)(V_2^- - V_2^+) + Gm_2(V_1^+ - V_1^-) = 0 \tag{2.2}$$

Solving Equations 2.1 and 2.2 we obtain:

$$Y = \frac{Iin}{V_2^+ - V_2^-}$$

$$Y = s\frac{C_2}{2} + \frac{Go_2}{2} + \frac{1}{s\left(\frac{C_1}{2Gm_1Gm_2}\right) + \frac{Go_1}{2Gm_1Gm_2}} \tag{2.3}$$

where Gm_1, Gm_2, Go_1 and Go_2 are the transconductance and output conductance of the transconductors, whereas C_1 and C_2 are the integration and input capacitance of the gyrator structure.

This admittance expression can be represented by the passive equivalent circuit shown in Figure 2.1(b), whose parameters are given by:

$$R_P = \frac{2}{Go_2} \; ; \; C_P = \frac{C_2}{2} \; ; \; R_S = \frac{Go_1/2}{Gm_1 Gm_2} \; ; \; L = \frac{C_1/2}{Gm_1 Gm_2} \tag{2.4}$$

As it can be observed at Equation 2.3, gyrator-C network behaves as a lossy inductor in a certain frequency range, whose small-signal behavior is fully characterized by the RLC equivalent circuit. It is important to mention that resistances R_P and R_S have not effect on the inductance value; however, these should be respectively maximized and minimized in order to reduce the power consumption and the ohmic loss [20].

On the other hand, the self-resonant frequency of the inductor, that is the resonant frequency of the RLC equivalent circuit, depends on the cut-off frequency of the transconductors constituting the active inductor, and is given by:

$$\omega_o = \sqrt{\frac{1}{LC_P}} = \sqrt{\frac{Gm_1}{C_1}\frac{Gm_2}{C_2}} = \sqrt{\omega_{t1}\omega_{t2}} \tag{2.5}$$

2.2 Characterization of Active Inductors

To characterize the behavior and performance of active inductors it is common to use characteristics like frequency range, inductance tunability, quality factor, noise, linearity and stability. In this section we are going to look through some of these, giving important details about its behavior, dependences and design considerations.

2.2.1 Inductive Frequency Range

A lossy active inductor only exhibits an inductive behavior over a specific frequency range of the spectrum. To quantify this range, the admittance expression obtained in the previous section is transformed into the impedance expression of the Equation 2.6.

$$Z = \left(\frac{R_S}{C_P L}\right)\frac{s\frac{L}{R_S} + 1}{s^2 + s\left(\frac{1}{R_P C_P} + \frac{R_S}{L}\right) + \frac{R_P + R_S}{R_P C_P L}} \tag{2.6}$$

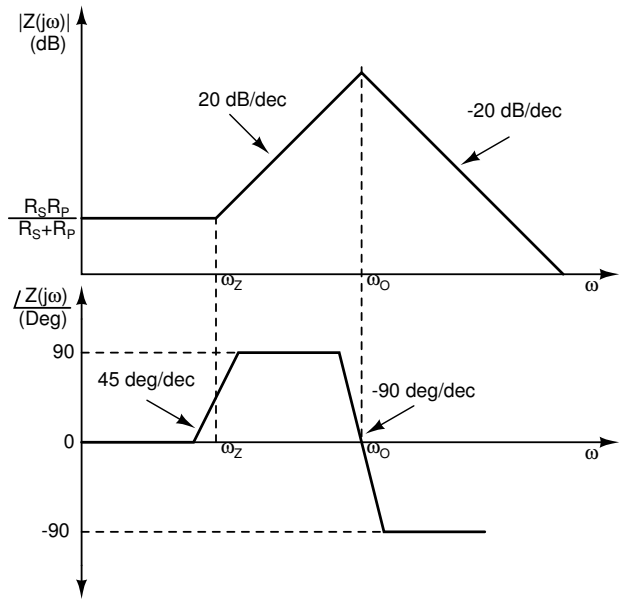


Figure 2.2: Bode plots of Z.

When complex conjugate poles are present in this expression, the pole resonant frequency of Z is given by:

$$\omega_P = \sqrt{\frac{R_P + R_S}{R_P C_P L}} \; ; \; R_P \gg R_S \;\rightarrow\; \omega_P \approx \sqrt{\frac{1}{LC_P}} = \omega_o \tag{2.7}$$

Bode plots of Z, Figure 2.2, shows that it has a resistive behavior when $\omega < \omega_Z$, inductive when $\omega_Z < \omega < \omega_o$ and capacitive when $\omega > \omega_o$, where ω_Z is the frequency at which is located the zero of Z.

$$\omega_Z = \frac{R_S}{L} = \frac{Go_1}{C_1} \tag{2.8}$$

From Equation 2.6 two important design considerations to increase the frequency range in which the gyrator-C behaves like an inductor are inferred. First one, because R_S imposes the lower bound of the inductor frequency range, it should be minimized which is achieved increasing the output impedance of the direct transconductor. And second one, C_p should be reduced to increase ω_o, even so the upper bound of the frequency range.

2.2.2 Inductance Tunability

In contrast to spiral inductors, active inductors can modify its inductance value through two different ways: changing the integration capacitance and transconductance value. To change the integration capacitance value, a fixed capacitor is used in parallel with a varactor. The p+/n-well and n+/p-well varactors in a SOI fabrication process can operate like floating varactors with a similar performance among them. However, they preserve disadvantages of Bulk varactors like a limited quality factor, small capacitance tuning range and an stringent voltage swing requirement [7]. On the other hand, MOS varactors have a similar ratio $\frac{C_{Max}}{C_{Min}}$ and a larger voltage swing across the varactor terminal than p-n varactor, making them the most used in voltage and current controlled oscillators, VCOs and CCOs respectively [7, 20].

Tranconductance tuning can be done by varying the bias current of transconductors, enabling a large inductance tuning range. This tuning mechanism is mainly limited by two restrictions. The transconductor transistors must remain in the saturation region in order to carry out a good current injection. And second one, the changes in the bias current modify the input dynamic range of the transconductors, and therefore the minimum phase noise value of the inductor.

It is worth mentioning that the tuning of the conductance modifies not only L but also R_S, which changes the inductor quality factor. This fact indicates that the tuning mechanism for L and Q must be done by independent ways.

2.2.3 Quality Factor

The quality factor Q of an inductor allows quantifying the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle, which is dependent on the applied voltage and flowing current across the active inductor. A general definition of Q comes from complex power of the inductor, Equation 2.5.1, where the imaginary term quantifies the magnetic energy stored and the real term accounts for the net energy loss in the parasitic resistances of the inductor. Evaluating the Z expression of the Equation 2.6 and obtaining the ratio between imaginary and real part yields the Q expression of the Equation 2.10.

$$P(j\omega) = I(j\omega)V^*(j\omega) = \mathfrak{Re}[Z]|I(j\omega)|^2 + j\mathfrak{Im}[Z]|I(j\omega)|^2 \tag{2.9}$$

$$Q = \frac{\mathfrak{Im}[Z]}{\mathfrak{Re}[Z]} = \left(\frac{\omega L}{R_S}\right)\frac{R_P}{R_P + R_S\left[1 + \left(\frac{\omega L}{R_S}\right)^2\right]}\left[1 - \frac{R_S^2 C_P}{L} - \omega^2 L C_P\right] \tag{2.10}$$

Each one of the terms that form the Equation 2.10 represents certain dependence on Q with regard to frequency. The first one quantifies the inductor Q at low frequencies. The second one takes into account the changes of the finite output impedance of the transconductors, whereas the third term shows that the quality factor vanishes when frequency approaches to ω_o.

Taking into account some particular conditions in the characteristics of the transconductors constituting the gyrator-C network it is possible to extract some important design considerations. To obtain a high Q, R_S should be minimized. This reduction is achieved using cascode, regulated cascode, multi-regulated cascode techniques or a shunt negative resistor at the output of the positive transconductor. However, this causes a reduction in the dynamic ranges of the inductor, and even so a higher signal sensibility on the inductance value [20]. Due to their length the rest of considerations will not be described in this text. To review these and other design considerations in depth about Q, the reader can turn to [20].

2.2.4 Noise

To analyze the noise of the inductor, the transfer functions of the circuits shown in Figure 2.3 are obtained, and subsequently compared to determine the contribution of each noise source of the transconductors on the equivalent noise sources of the inductor.

To determine the input equivalent noise, the input nodes are put in short-circuit and the noise voltage at node 1 is found (v_{1-SC}). By means of a small signal analysis the implication expression of the Equation 2.11 for the two circuits is obtained. Comparing these expressions it can be deduced that the input equivalent noise voltage is given by the expression on the right side of the Equation 2.11.

$$v_{1-SC} = \frac{Gm_1}{Y_1}\left[vn_1 + \frac{in_2}{Y1}\right] \iff v_{1-SC} = \frac{Gm_1}{Y_1}vn \rightarrow vn = vn_1 + \frac{in_2}{Y_1} \tag{2.11}$$

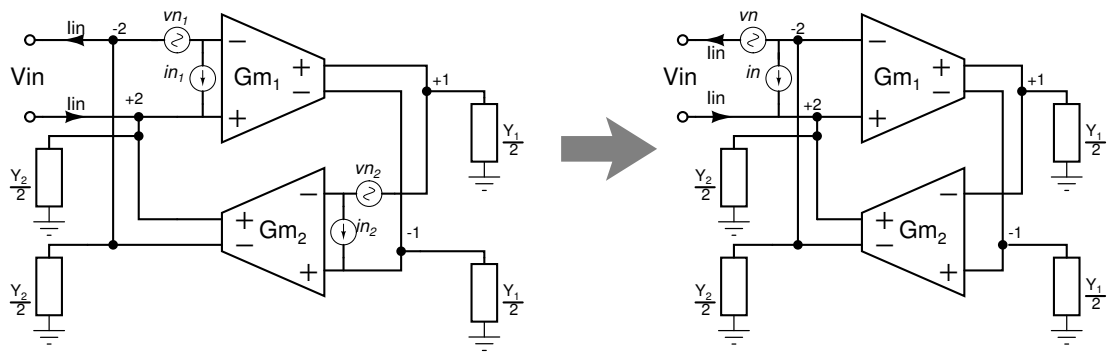


Figure 2.3: Noise of differential gyrator-C active circuit under analysis.

To determine the equivalent noise current, the input terminals are put in open circuit and the noise voltage at node 1 is determined (v_{1-OC}) , similar as it was done in the previous analysis. The obtained result is shown in the Equation 2.12.

$$v_{1-OC} = \frac{Gm_1}{Y_1} \frac{Y_1}{Y_1Y_2 + Gm_1Gm_2} \left[in_1 + \frac{Y_2 in_2}{Gm_1} + Y_2 vn_1 + m_2 vn_2 \right] \leftrightarrow v_{1-OC} = A_V Z_{in} in \tag{2.12}$$

Taking into account the constraints at the input impedance of the gyrator-C network and voltage gain, Equation 2.13, the input equivalent current noise is given by the Equation 2.14.

$$Z_{in} = \frac{Y_1}{Y_1Y_2 + Gm_1Gm_2} \; ; \; A_V = \frac{Gm_1}{Y_1} \tag{2.13}$$

$$in = in_1 + \frac{Y_2 in_2}{Gm_1} + Y_2 vn_1 + Gm_2 vn_2 \tag{2.14}$$

From the previous Equations some important design considerations can be drawn to reduce the noise of the active inductor. Y_1 and Y_2 should be respectively increased and reduced. The first one entails a reduction at the output-input impedances of the direct and feedback transconductors respectively, while the second one entails an increment at the input-output impedances of the direct and feedback transconductors. It is worth mentioning that to make this impedances arrangement reduces the inductor quality factor because of the reduction of R_P. Besides, the Gm_1 value should be increased, while Gm_2 value reduced, enabling to reduce the noise associated to in_2 and vn_2 respectively.

2.2.5 Linearity and Power Consumption

The linearity of the active inductors is limited by the range in which the transconductance of the transconductors constituting gyrator-C network remains constant and linear. This range is limited by the transitions of operation mode, that is from saturation to cutoff region and saturation to triode region. In these transitions, inductance is no longer linear nor constant; however, the inductive characteristic remains valid. When these transitions happen the expression which depicts the inductance value changes from $L = \frac{C}{Gm_1 Gm_2}$ to $L = \frac{C}{Gds_1 Gds_2}$.

Due to the quadratic behavior of the current of MOS transistors, the transconductance is a linear function of the overdrive voltage, and therefore depends on the dynamic range even if the transconductors do not have transitions of operation mode. This dependence is called signal sensitivity, and is a big problem in systems where the active inductor experiences a large signal swing.

The linearity of active inductors is directly related with the DC power consumption. While a high overdrive voltage allows reducing the non-linear factors of higher order in the transistor current, which improves the linearity, the power consumption is increased [21]. On the other hand, a high overdrive voltage allows achieving a high input dynamic range at the transconductors. Nonetheless, this increment in the input dynamic range reduces the saturation region of the device because of the limited power supply, which degrades the circuit's linearity.

The power consumption is one of the most important differences between spiral and active inductors. As it is known the spiral inductors do not consume static power. Meanwhile, active inductors consume DC power due to the biasing currents of their transconductors, biasing schemes and negative resistor networks used to compensate the ohmic loss.

Each one of the specifications mentioned in this section is very useful to describe and estimate the behavior and performance of the active inductor. However, its utility loses importance when is applied over a limited equivalent model as a gyrator-C network instead of a real topology. Because of this, in the next section some floating active inductor topologies will be briefly described, and their most important advantages, disadvantages and limiting factors will be highlighted.

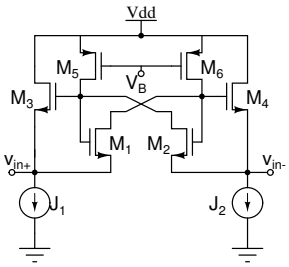
2.3 Active Inductors Topologies

As it was previously mentioned, the active inductor can be implemented by means of a grounded or floating structure. Given that the VCOs used in wireless communications systems generally have differential structures, the floating structures are the most proper option to implement this sort of circuit since it reduces the effects of the mismatch on the VCO performance. Considering this, we will look through some topologies of floating active inductor, trying to show in a simple way their most important characteristics.

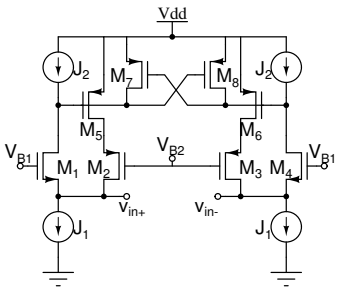
In Figure 2.4 Lu-Hsieh's, A. Thanachayanont's, Mahmoudi-Salama's, Akbari-Dilmag's, Abdalla-Eleftheriades's and Thanachayanont-Ngow's active inductor topologies are shown [22–27]. Each of these topologies is based on the gyrator-C principle with little differences among them. The Lu-Hsieh's active inductor, Figure 2.4(a), is based on a cross-coupled differential pair loaded with transistors operating in the triode region, and a common drain stage as feedback transconductor. This structure provides a C_P equal to 0, optimum value to increase the self-resonant frequency of the inductor. However, the resistance R_P associated to its equivalent circuit is low, limiting the maximum quality factor of the inductor. On the other hand, the value of R_S is dependent on the difference $(gds_5 - gm_1)$, which implies a high power consumption and a limited dynamic range [22]. In addition, the fact that the load transistor operates in the triode region increases the sensitivity of its specifications with regard to PVT variations.

In Figures 2.4(b) and 2.4(f) the Thanachayanont's class A inductor and its class AB version are shown [23, 27]. These topologies consist of a common gate stage as direct and a cascode stage as feedback transconductor. To compensate their ohmic loss, they use negative resistance networks implemented by cross-coupled pairs, which enables it to reach high Qs. Its R and C parameters are given by: $R_P \simeq 1/gm_1$ and $C_P \simeq C_{gs1}$, that means a limited quality factor and frequency range. The most notable advantages of these topologies are the low noise level and large dynamic ranges, as a result of the low input and high output impedance, and the low overdrive voltage of the output transistors.

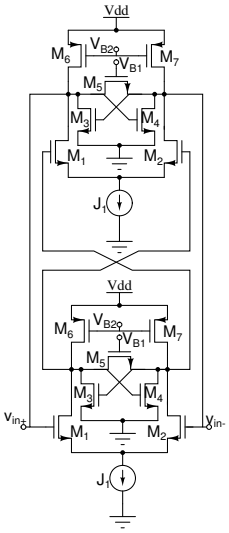
These structures have some weak points regarding PVT variations. First one, given the grounded nature of feedback transconductor, any process, temperature or voltage variation will modify its transconductance value, and therefore the value of the emulated inductance. And second one, the different process corners along with the use of bias voltage can cause changes on the operation conditions of the transconductors, and as a result generate large offset currents.



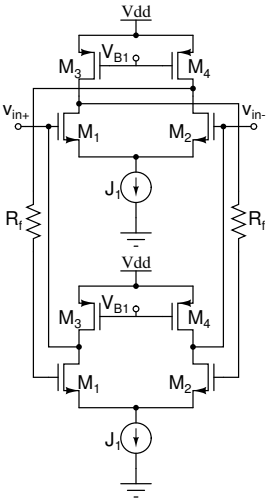
(a) Hung Lu - Hung Hsieh's active inductor [22].



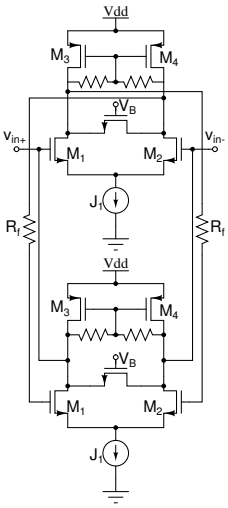
(b) Apinunt Thanachayanont's active inductor [23].



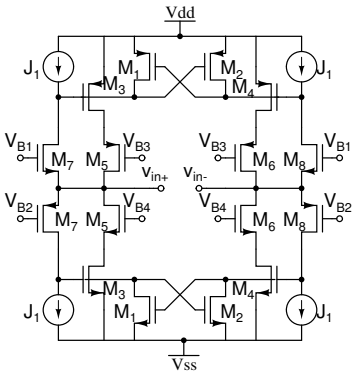
(c) Mahmoudi-Salama's active inductor [24].



(d) Akbari-Dilmaghani's active inductor [25].



(e) Abdalla-Eleftheriades's active inductor [26].



(f) A. Thanachayanont - Ngow's active inductor [27].

Figure 2.4: Floating active inductor topologies.

Mahmoudi-Salama's, Akbari-Dilmaghani's and Abdalla-Eleftheriades's active inductors are pair differential based topologies [24–26]. The first one has a cross-coupled differential pair to control the common mode voltage and to compensate the ohmic loss, and an additional transverse transistor operating in the triode region to adjust the resistance value without a tail current [24]. To control the output common mode voltage by means of this transistor becomes a disadvantage, since its dependence regarding the fabrication process causes changes on the operation region of the input transistors, and therefore modifies the input dynamic ranges of the inductor. In addition, it is worth mentioning that the negative resistance network is dependent on PVT variations.

On the other hand, Akbari-Dilmaghani's active inductor uses a common mode feedback circuit and a feedback resistor to control the output common mode voltage, achieving to tune the quality factor and inductance value through independent mechanisms. The feedback resistor is implemented by a transistor operating in the triode region, making it sensible to PVT variations and the bias voltage used for controlling it.

The Abdalla-Eleftheriades's active inductor is quite similar to Akbari-Dilmaghani's, but it has some little modifications. Besides the feedback resistor, this topology uses a pair of resistors as load with a transverse transistor operating in the triode region to adjust the output impedance and output common mode voltage. Just like the other topologies that use this control mechanism, this structure requires a control system to reduce its sensitivity to PVT variations. In addition, the use of load resistors is not a good choice to obtain a high output impedance because of the large occupied area and the large deviations of this nominal value.

Each one of the topologies described in this section has the outstanding advantages like high Q, large and tunable inductance value, etc, that characterize to active inductors, but also the strong disadvantages related to PVT variations. Despite using additional circuitry to achieve a good performance, the weak points regarding PVT variations are neither treated nor attacked in most of cases. In the next section the active inductor proposed in this master project will be introduced, and its most important characteristics related to the compensation of the PVT variations will be analyzed.

2.4 Proposed Inductor

Just like most of the topologies described in the previous section, the proposed inductor is based on the differential pair because it allows to compensate PVT variations in a simple

way. The inductor consists of two main sub-circuits: the core cell and the bias scheme. Some particular signal connections have been applied on the core cell in order to reduce the effect of the mismatch between paired devices. Each one of these sub-circuits and signal connections will be described in detail in the next subsections.

2.4.1 Core Cell

The inductor topologies with one or both transconductors grounded, the case of Lu-Hsieh's, Thanachayanont's and Thanachayanont-Ngow's topologies, show a high sensitivity on their performance with regard to PVT variations. This is due to the fact that any change of process, voltage or temperature is reflected on its bias conditions, and therefore on its transconductance value. Meanwhile, the adaptable and floating nature of transconductors based on differential pairs make them more robust but not insensitive against PVT changes.

The proposed core cell, Figure 2.5, consists of one differential pair with diode-connected load and a cross-coupled pair. The two load sort in the differential pair are used for obtaining a high impedance without excessively limiting the dynamic range. This enables the inductor to increase its quality factor and frequency through a reduction of the ohmic loss and the frequency value for the zero. In addition, the diode-connected load allows adapting the DC output level to the process changes of the PMOS transistors.

Transistors M_7 and M_8 inject current signal toward input nodes with low losses, because of the relative high output impedance provided by the drain of the output transistors. An important data is that the proposed core cell has the positive transconductor

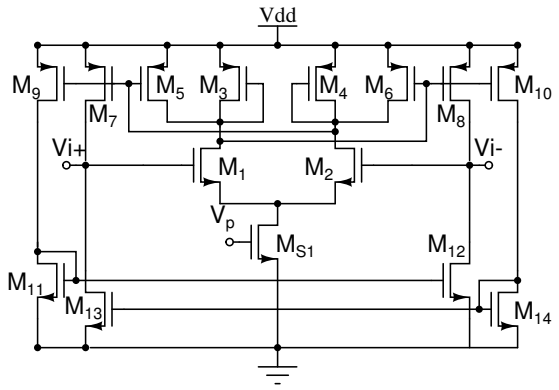


Figure 2.5: Proposed core cell for the active inductor.

tied to input nodes. This fact allows using the VCO cross-coupled pairs to compensate the ohmic losses, different to topologies described in the previous section.

At this moment, the proposed topology has two transistors injecting current, which indicates the necessity for two bias current source. To provide these currents from the opposite branch, allow not only using them as bias but also as signal sources. This injection mechanism has some important advantages. First one, it is not necessary to use additional devices to provide the bias current only. Second one, the cross current injection causes the reduction of the inductance value, allowing to achieve a higher operation frequency than using one current injection. And lastly, the cross signal injection reduces the effect of the mismatch between paired devices and therefore a more robust circuit is obtained. Just like the others topologies, the proposed cell shows a limited dynamic range because of its active nature. Moreover, offset currents appear between the current mirrors because of the difference between their bias conditions.

The proposed core cell shows a gyrator-C structure a little different than the traditional one, Figure 2.6. Despite looking as a complex structure, it is not. Each one of the transconductors is implemented by one pair of transistors, and the associated impedance is given by a current mirror, which also operates as a transconductor. A simple analysis of the structure shows that the input admittance is given by the Equation 2.15.

$$Y = s\frac{C_3}{2} + \frac{Go_3}{2} + f_L(s) \tag{2.15}$$

where f_L is given as follows:

$$f_L(s) = \frac{2\beta C_2 Gm_1 Gm_2 s + 4Gm_1 Gm_2 Gm_3 + 2\beta Gm_1 Gm_2 Go_2}{C_1 C_2 s^2 + (C_1 Go_2 + C_2 Go_1)s + Go_1 Go_2} \tag{2.16}$$

The f_L function can be represented by an inductor in series with a frequency dependent resistance. This dependence with regard to the frequency generates an exponential behavior of the quality factor due to the function "$tan(\phi)$" that relates them.

Unlike what a lot of people think, to bias a differential pair with a constant current source or sinker is not enough to compensate the effect of the process, voltage and temperature variations. Because of that, it is necessary to know and to understand the behavior of the main design variables regarding those variations, and so to generate adequate compensation mechanisms that allow obtaining the desired performance. After making several behavioral simulations on a differential pair, some important design

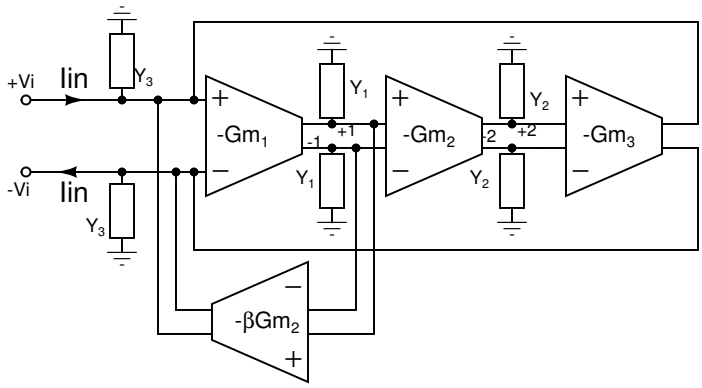


Figure 2.6: Gyrator-C structure of the core cell.

considerations have been drawn to obtain a robust inductance. To achieve a constant transconductance, principal variable of the inductance, with regard to temperature, a Proportional-To-Absolute-Temperature (PTAT) behavior on the bias current source is needed. On the other hand, if we consider the process variations, an increment of the bias current is needed when the slow corner is present, while a reduction must be carried out for the fast corner. These observations have been used to develop a Gm-constant scheme, key point in the compensation process of the PVT variations. Next, the Gm-constant scheme will be described.

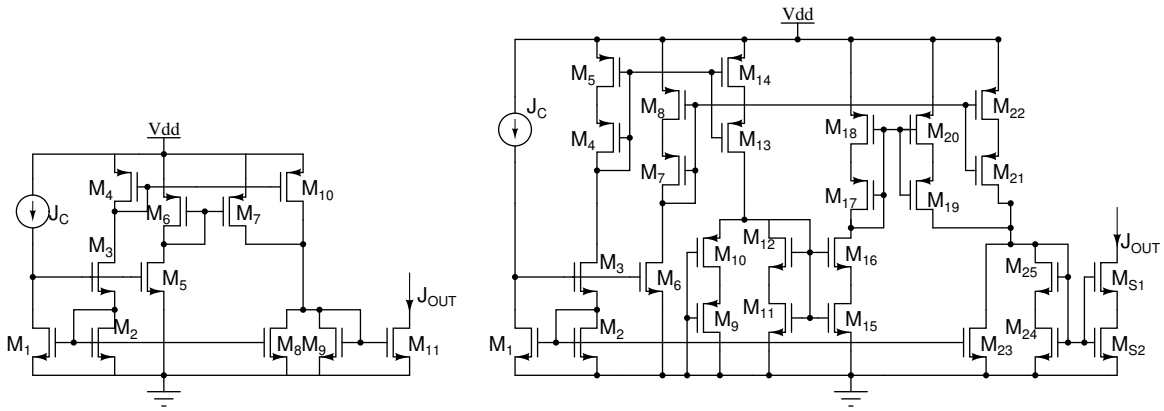
2.4.2 Proposed Gm-Constant Circuit

Some different schemes have been proposed to compensate the effect of PVT variations, specially on designing variable Gm. Most of these circuits are based on external structures that sense the deviation of the performance due to the process, voltage or temperature variations, and apply a corrective action. Some of these circuits are not focused in compensating PVT variations, but they attack one or several specifications and as a consequence reduce their impact. In [28,29] for example, Miyashita et. al. and Lin et. al. have as goal to reduce the oscillator phase noise. In the first work an Amplitude Automatic Control (AAC) consisting of two peak detectors, one level shifter and an error amplifier which drives the tail current source of the circuit. The second work uses a switched-transistor triode array based AAC, and an LDO regulator, getting the optimum oscillation level to reduce phase noise. The achieved performances are very good, but in both works the cost is an strong increment of the area and power consumption.

In [30] Sroka tackles the problem applying an optimization process, in a limited design space, over a Gm-constant cell proposed by Thomas Lee. Although the obtained results are good, the design methodology has neither support nor theoretical fundamentals. On the other hand, a novel bias circuit is proposed in [31] by Mukadam. This circuit operates in open loop and is limited by a large number of design constraints in order to achieve insensitivity regarding to power supply. Moreover, it uses a resistive divider that takes up a large die area reduce the power consumption.

Initially, a general bias scheme for modifying the tail current and to compensate the PVT variations was proposed by us, Figure 2.7(a). This scheme allows obtaining the desired compensation in most of the topologies described in the previous section. However, the proposed core cell has a behavior a little different because the PMOS and NMOS transconductance that define the inductance value depend on the same bias current. Because of this, one branch is added to compensate the combined process corners, N_F-P_S and N_S-P_F, giving rise to the particular bias scheme shown in the Figure 2.7(b). This proposed Gm-constant circuit has a simple structure consisting of a current source, a modified Complementary-To-Absolute-Temperature (CTAT) cell, two branch used to compensate the process corners, and a current sinker. The current source, J_C, is used not only for biasing the structure but also as a control mechanism for the inductance value, since it allows adjustment of the transconductance values.

The traditional CTAT cell consists of the M_1 and M_3 transistors and a passive resistance instead of the M_2 transistor [32]. By replacing the resistance for the M_2 transistor is possible to modify the behavior from CTAT to PTAT under certain conditions that will be described in the design section. Transistor M_6 is located in parallel to the PTAT cell for reducing or increasing the current of M_{24} when a positive or negative deviation of the fabrication process arises. On the other hand, $M_{9,10}$ and $M_{11,12}$ transistors carry out a comparison for the combined process corners, and inject or not inject a current toward M_{24} in accordance with the corner. The transistor M_{23} sinks the spare current of the circuit. The rest of the transistors are for driving the current toward the core cell. With this brief introduction of the proposed core cell and bias scheme, we are going on with the detailed description of the design process for each of these sub-circuits.



(a) General proposed bias scheme. (b) Particular proposed bias scheme.

Figure 2.7: Proposed bias schemes.

2.5 Design of the Active Inductor

Each sub-circuit of the active inductor shows different trade-offs between its specifications; however, the methodology used to tackle them is similar for both core cell and bias scheme. First, the most important constraints are examined and evaluated looking for the strongest dependences among the variables. Subsequently, an equilibrium point is fixed to make the sizing process using models PD-SOI CMOS 45 nm provided by IBM. Lastly, a verification and adjustment process is made.

2.5.1 Core Cell

To design the core cell, we shall analyze some restrictions about bias conditions, input and output impedance, gate oxide capacitances, power consumption, noise and dynamic ranges to consider its most relevant trade-offs. It is worth mentioning that most of the expressions obtained in the sections 2.1 and 2.2 do not describe directly neither the behavior nor the performance of the active inductor, but some of them afford important design considerations since the operation principle is the same like the traditional gyrator-C structure. The most important expressions of these sections (input impedance of the active inductor, quality factor, self-resonant frequency, zero frequency, noise current and voltage, from Equation 2.17 to 2.24), along with the obtained for the input impedance and quality factor of the core cell, Figure 2.8, are rewritten next to provide a higher clarity about the design process.

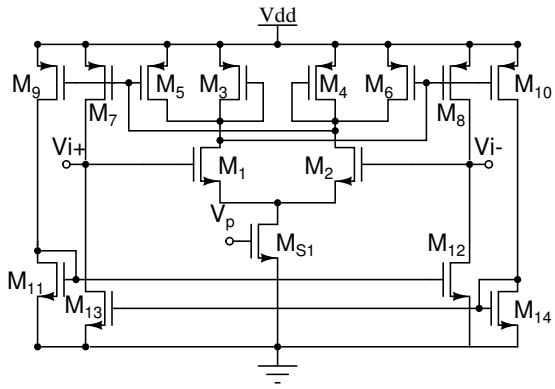


Figure 2.8: Proposed core cell.

$$Z_P = 2C_1C_2s^2 + (2C_1Go_2 + 2C_2Go_1)s + 2Go_1Go_2/$$
$$C_1C_2C_3s^3 + (C_1C_2Go_3 + C_1C_3Go_2 + C_2C_3Go_1)s^2 + (4C_2Gm_1Gm_2 + C_1Go_2Go_3 +$$
$$C_2Go_1Go_3 + C_3Go_1Go_2)s + 8Gm_1Gm_2Gm_3 + 4Gm_1Gm_2Go_2 + Go_1Go_2Go_3 \tag{2.17}$$

$$P(j\omega) = I(j\omega)V^*(j\omega) = \mathfrak{Re}[Z_P]|I(j\omega)|^2 + j\mathfrak{Im}[Z_P]|I(j\omega)|^2$$
$$Q = \frac{\mathfrak{Im}[Z_P]}{\mathfrak{Re}[Z_P]} = \left(\frac{\omega L}{R_S}\right)\frac{R_P}{R_P + R_S\left[1 + \left(\frac{\omega L}{R_S}\right)^2\right]}\left[1 - \frac{R_S^2C_P}{L} - \omega^2LC_P\right] \tag{2.18}$$

$$\omega_P = \sqrt{\frac{R_P + R_S}{R_PC_PL}}\ ;\ R_P \gg R_S\ \rightarrow\ \omega_P \approx \sqrt{\frac{1}{LC_P}} = \omega_o \tag{2.19}$$
$$\omega_o = \sqrt{\frac{1}{LC_P}} = \sqrt{\frac{Gm_1}{C_1}\frac{Gm_2}{C_2}} = \sqrt{\omega_{t1}\omega_{t2}} \tag{2.20}$$
$$\omega_Z = \frac{R_S}{L} = \frac{Go_1}{C_1} \tag{2.21}$$
$$Z_{in} = \frac{Y_1}{Y_1Y_2 + Gm_1Gm_2}\ ;\ A_V = \frac{Gm_1}{Y_1} \tag{2.22}$$
$$vn = vn_1 + \frac{in_2}{Y_1} \tag{2.23}$$
$$in = in_1 + \frac{Y_2in_2}{Gm_1} + Y_2vn_1 + Gm_2vn_2 \tag{2.24}$$

The main goal in the design of an oscillator used in a wireless communication system is to reach the highest oscillation frequency with a wide tuning range, keeping a low phase noise level. To achieve it, the active inductor parameter L, just the same as C_P and R_S, must be reduced since it increases the self-resonant frequency and reduces the zero frequency, Equations 2.19 and 2.21. It is worth mentioning that in active inductors based oscillators the tuning range must coincide with the range where gyrator-C network behaves like an inductor.

The increase of ω_o is directly related to the power consumption because of the transconductance value, and to the area due to the gate oxide capacitances used for the integration, Equation 2.20. To reduce C_1 and C_2, the ideal channel length for $M_{1,2}$ and $M_{3,4,5,6,7,8,9,10}$ would be the minimum allowed by the fabrication process. However, it should be noted that if $M_{1,2}$ has that channel length, its output impedance is reduced and the ohmic loss, represented by R_S, increases causing a reduction of the inductor quality factor. Even more important, if R_S reduces and C_1 increases, the zero frequency increases, causing a reduction of the frequency range of the inductor and a late beginning of the inductive behavior. To keep constant the frequency range or even expand it, the channel length and transconductance value must be relatively large, which represents a higher power consumption and die area.

Considering the noise expressions of Equations 2.23 and 2.24, to reduce $rds_{1,2}$ is a good option, since it allows decreasing the equivalent input noise voltage of the inductor. On the other hand, increasing the inductor input impedance is a good point, not only reduces the inductor loss but also the input noise current. Taking into account the different observations previously described, the channel length is not fixed in the minimum allowed value. The channel lenght is selected based on its influence on the compensation process of the transconductance of the devices regarding to fabrication process and temperature.

Through a simple test made on the basic differential pair, we could determine the changes required for the tail current to keep constant the transconductance value over various Process Corners (PCs), and several channel lengths. After analyzing the results, we set the channel length and overdrive voltage of the input transconductors at 200 nm and 100 mV respectively. The selected parameters allow obtaining a more robust circuit against process and temperature variations than at 80 and 160 nm, and a higher operation frequency than at 240 nm. However, the overdrive voltage selected for the design limits the input dynamic range, and therefore affects the signal sensitivity of the inductor. The results obtained in the test are reported in Table 2.1.

L 80 nm	100 [mV]	125 [mV]	150 [mV]
Typ	150 μA	150 μA	150 μA
N_F	132 μA	128 μA	123 μA
N_S	178 μA	186 μA	198 μA

L 160 nm	100 [mV]	125 [mV]	150 [mV]
Typ	150 μA	150 μA	150 μA
N_F	137 μA	134 μA	131 μA
N_S	168 μA	173 μA	178 μA

L 240 nm	100 [mV]	125 [mV]	150 [mV]
Typ	150 μA	150 μA	150 μA
N_F	141 μA	139 μA	138 μA
N_S	163 μA	168 μA	162 μA

Table 2.1: Gm-constant test for a differential pair at T=60°C.

The power consumption of the core cell in typical conditions is set at 1.3 mW@1V, which is distributed as follows: 400 μA for the NMOS transconductor, 112.50 and 87.50 μA for the diode-connected load and cross-coupled pair respectively, and 900 μA for P mirrors. This value was fixed from a valuation of the possible inductance range (5-10 nH). Considering that the classic quadratic model is very imprecise, the sizing process is made using a higher order model that considers velocity saturation and mobility degradation, Equation 2.25 and 2.27. The transistor parameters used in the sizing process of the circuit are reported in Table 2.2. Subsequently, we make an adjustment process by means of the simulator. The channel width for M_1 and M_2 is reported in Table 2.3. Once the first transconductor was sized, the next step is to fix the trade-off between the two loads, and to define the value of the second transconductance.

Parameter	**NMOS**	**PMOS**	**Unity**
$\mathbf{K_m}$	0.4125	1.2	–
$\boldsymbol{\mu_o}$	670	250	$\frac{cm^2}{Vs}$
$\mathbf{C_{ox}}$	$19.07e-3$	$17.09e-3$	$\frac{F}{m^2}$
$\mathbf{V_{th}}$	0.185	-0.285	V
$\boldsymbol{\theta}$	0.8957	0.3342	V^{-1}
$\boldsymbol{v_{sat}}$	$8.5e4$	$6e4$	$\frac{m}{s}$
$\boldsymbol{\lambda}$	0.35	0.45	V^{-1}

Parameter	**NMOS**	**Unity**
$\mathbf{K_m}$	0.4125	–
$\boldsymbol{\mu_o}$	670	$\frac{cm^2}{Vs}$
$\mathbf{C_{ox}}$	$19.07e-3$	$\frac{F}{m^2}$
$\mathbf{V_{th}}$	0.375	V
$\boldsymbol{\theta}$	0.8957	V^{-1}
$\boldsymbol{v_{sat}}$	$8.5e4$	$\frac{m}{s}$
$\boldsymbol{\lambda}$	0.35	V^{-1}

Table 2.2: Electrical parameters of the $lvtnfet$ and $svtnfet$ transistors, L=200 and 80 nm.

Tran	Type	Var	Val[μm]	Var	Val[nm]	m	Var	Val[$\frac{mA}{V}$]	Var	Val[fF]
M_1	lvtnfet	W	2.80	L	200	4	Gm	2.364	C_G	30.00
$M_{3,9}$	lvtpfet	W	2.00	L	200	2	Gm	1.285	C_G	7.32
M_5	lvtpfet	W	1.60	L	200	2	Gm	1.049	C_G	5.94
M_7	lvtpfet	W	2.00	L	200	6	Gm	3.752	C_G	21.99
M_{11}	svtnfet	W	1.20	L	80	1	Gm	0.793	C_G	5.18
M_{13}	svtnfet	W	1.20	L	80	3	Gm	2.286	C_G	17.43

Table 2.3: Core cell's adjusted sizing.

$$I_D = K_m \mu_o C_{ox} \frac{W}{L} \frac{(|V_{GS}| - |V_{TH}|)^2}{1 + \left(\theta + \frac{\mu_o}{v_{sat} L}\right)(|V_{GS}| - |V_{TH}|)} (1 + \lambda V_{DS}) \tag{2.25}$$

$$Gm = K_m \mu_o C_{ox} \frac{W}{L} (1 + \lambda V_{DS}) \frac{2(|V_{GS}| - |V_{TH}|)F_1 - \left(\theta + \frac{\mu_o}{v_{sat} L}\right)(|V_{GS}| - |V_{TH}|)^2}{F_1^2} \tag{2.26}$$

$$F1 = 1 + \left(\theta + \frac{\mu_o}{v_{sat} L}\right)(|V_{GS}| - |V_{TH}|) \tag{2.27}$$

The channel length of the load transistor is fixed at 200 nm. Just like in the NMOS transistors, the channel length selected reduces the effect of the process and temperature variations over the circuit performance. Moreover, the channel modulation is lower than for 160 nm, while the transconductor keeps a high cutoff frequency . It is worth mentioning that the ratio between the channel length of the PMOS and NMOS transistors is not the best in order to reduce noise generated by the circuit [33].

To avoid instability and phase inversion at the load of the differential pair, the transistor M_3 is made 25% bigger than M_5. The M_3 and M_5 channel width are set looking to achieve a high ratio $\frac{Gm3}{C_3+C_5}$, without restricting the output dynamic range. The values set for the transistors are reported in the Table 2.3.

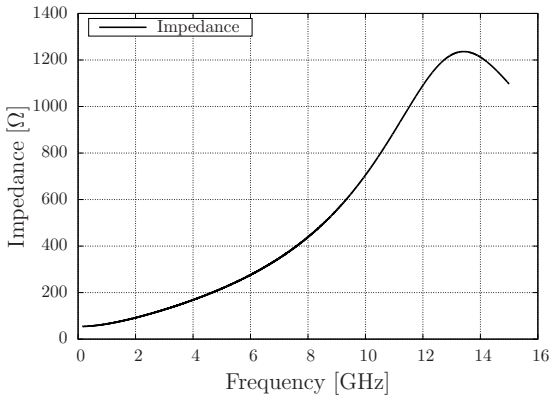
The diode-connected load is the key point in the proposed core cell, since it allows injecting current toward the input nodes in a direct and cross way, this latter by means of an NMOS current mirror. However, owing to its presence, the PMOS process variations have a direct influence on the transconductance of the differential pair and the compensation process is not direct. In addition to inject in a cross-way, the NMOS current mirror generates a second integration that causes an additional phase shifting. Thus, the phase crosses for the ideal value, (90°), and therefore the inductor reachs infinity quality factors without the need for any compensation network.

The proximity between the integrations determines largely the inductive frequency range, since the closer them are, the more quickly the phase shifting happens, and the narrower the inductive frequency range is. Because of this, the current ratio for the PMOS current mirrors is set M_3-M_9 1:1 and M_3-M_7 1:3, since it allows reducing the capacitance of the first integration, while the second integration is kept far away and the transconductance is slightly affected. The channel length for the NMOS transistors of the current mirror is fixed at 80 nm, since at this value the output impedance of the $svtnfet$ (Super-High V_{TH}) transistor is greater than $lvtpfet$ (Low V_{TH}), which allows increasing the inductive frequency range. The channel width for the N mirrors is set at 1.2 μm. With this sizing the N mirror keeps a high f_T, and the current mismatch between M_7 and M_{13} is reduced.

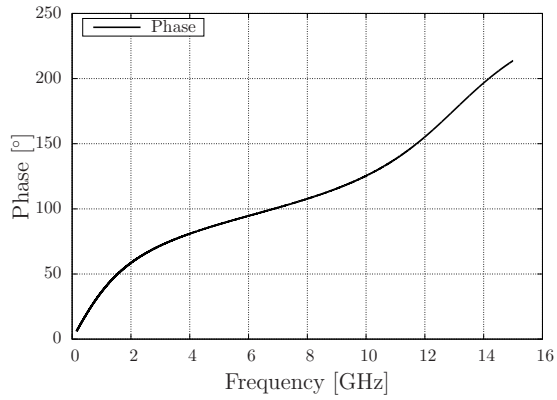
Once the core cell is properly sized, the circuit performance is evaluated by means of an AC small signal and transitory analysis using HSPICE RF and models for a 45 nm PD-SOI CMOS technology provided by IBM. The circuit is simulated using typical models for the devices, a power supply to the value 1 V and temperature at 60°C. It is worth mentioning that the current sinker M_{S1} is implemented by an ideal element of the simulator. The results obtained in the simulation are shown in the Figures 2.9(a), 2.9(b) and 2.9(c), where it is possible to observe the increase of the impedance magnitude with regard to the frequency, and the phase shifting until reaching 90° at 5.277 GHz.

For measuring the inductance value emulated by the circuit, we take the impedance value at 5.277 GHz, and assume that all the equivalent circuit behaves like an inductor with a resistance in series of 0 Ω. The value obtained is 7.016 nH. This measurement methodology is applied because it is very difficult to estimate separately the contribution of the capacitive and inductive elements when the process variations influence the circuit performance. It is worth mentioning that if a passive inductor shows a phase behavior like in Figure 2.9(b), it implies a change in its nature; that is, it would be an active instead of a passive element. The transient response of the inductor current shows two important aspects related with the damping factor. First one, it is observed a considerable jump at the beginning of the response that can be confused with an offset current. And second one, the settling time, around 500 ps, is too long to fulfill with the channel selection process of the VCO.

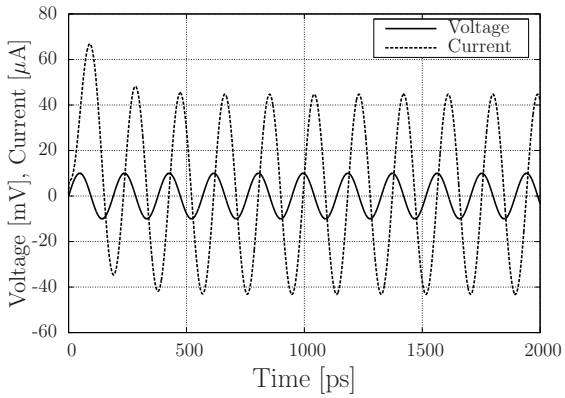
Trying to keep the same performance of the inductor despite the PVT variations, the changes required in the current of the tail sinker are determined. The results obtained are reported in Figure 2.10. From the data obtained, the requirement of a PTAT behavior



(a) Impedance magnitude of the active inductor.

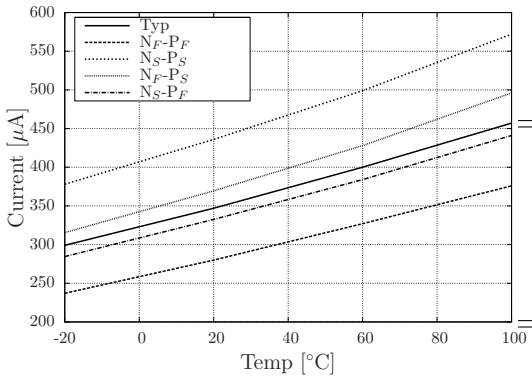


(b) Impedance phase of the active inductor.



(c) Voltage and current of the active inductor.

Figure 2.9: Frequency and transient response of the active inductor.



	Temp			
PC	-20°C	20°	60°C	100°C
Typ	299 μA	347 μA	400 μA	457 μA
N_F-P_F	237 μA	280 μA	327 μA	376 μA
N_S-P_S	378 μA	436 μA	499 μA	572 μA
N_F-P_S	315.5μA	369.5μA	428 μA	496 μA
N_S-P_F	284.5μA	332.5μA	384 μA	441 μA

Figure 2.10: Tail current changes for compensating PT variations.

with slight changes of the slope when the temperature is greater than 60°C is observed. In addition, the tail current shows some particular decreases and increases according to the process corners, as it was described in the design of the core cell. Once the changes

required for the tail current were found, we go on to continue with the most important part of the inductor, the bias scheme. In the next section a brief description of the circuit, along with the main constraints and design considerations will be described.

2.5.2 Gm-constant Bias Scheme

The bias scheme proposed to sense and compensate mainly the changes of the fabrication process and temperature is shown again in the Figure 2.11. As it was previously described, the circuit consists of a PTAT cell, and two branches used for compensating the process corners. The PTAT behavior comes from the current mirror constituted by one transistor saturated (M_1), and one transistor (M_2) operating on the edge of sub-threshold region. From a simple analysis considering the traditional quadratic behavior for the drain current in the saturation region regarding overdrive voltage, it is possible to infer the relation at the Equation 2.28.

$$V_{GS1}(T) = K_H T^{\frac{K_1}{2}} + V_{THo} + K_T(T - T_o)$$
$$K_H = \sqrt{\frac{2I_D L}{WC_{ox}\mu(T_o)T_o^{K_1}}} \; ; \; K_1 \approx \frac{3}{2} \; ; \; K_T \approx -4.38\frac{mV}{^\circ K} \tag{2.28}$$

From this equation we can conclude that the V_{GS1} voltage shows a CTAT behavior dominated by the V_{TH} voltage, because of the low current levels used in the biasing [34]. However, the overdrive voltage shows a PTAT behavior owing to the presence of the K_H

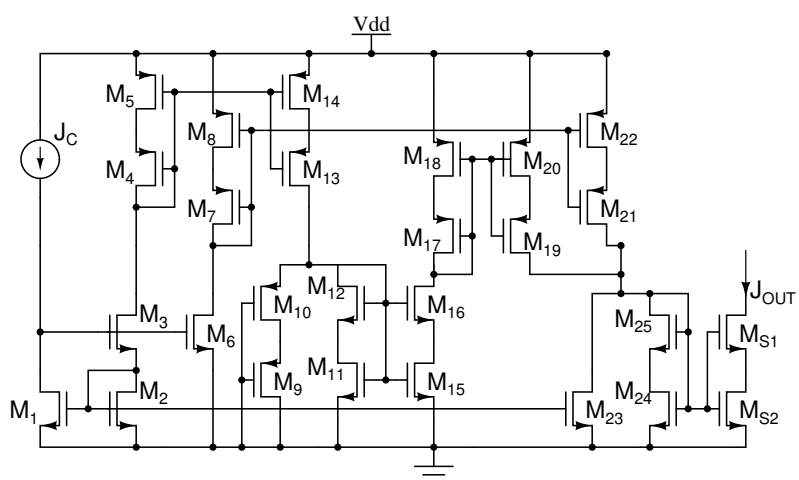


Figure 2.11: Proposed bias schemes.

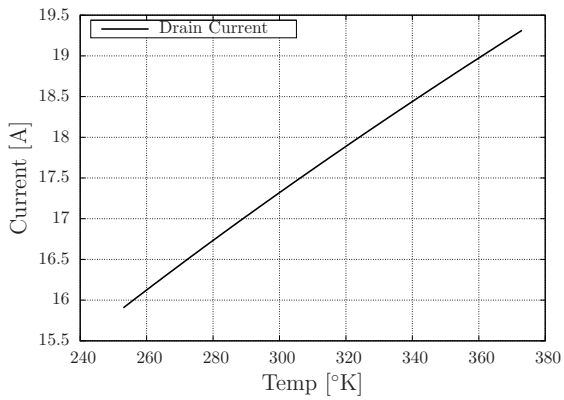


Figure 2.12: Drain current for transistor in sub-threshold region.

factor. When this voltage is applied to a transistor operating in sub-threshold region, the signal mirrored by the circuit has a behavior Quasi-PTAT, as it is shown in the Equation 2.29 and the Figure 2.12, where T is given in Kelvin degrees.

$$I_D = \mu V_T^2 \frac{W}{L} e^{\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)} \; ; \; e^{\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)} = C$$
$$I_D = \mu(T_o)\left(\frac{T_o}{T}\right)^{\frac{3}{2}}\left(\frac{K_B T}{q}\right)^2 \frac{W}{L} C \rightarrow I_D = \frac{C K_B^2 \mu(T_o) T_o^{\frac{3}{2}}}{q^2} \frac{W}{L} T^{\frac{1}{2}} \tag{2.29}$$

The current source J_C, to the value 50 μA, is used as a reference signal. The channel length for $M_{1,2,3}$ is selected at 200 nm to obtain similarity between the core cell's and bias scheme's variations. However, these transistors are different, M_1 is a $lvtnfet$ transistor whereas $M_{2,3}$ are $nfet$ transistors. This particular difference is used to reduce the branch current and the width of $M_{2,3}$. It should be noted that these transistors show very similar characteristics regarding mobility and threshold voltage, as shown in Table 2.4.

The width of M_1 is adjusted in order to obtain a V_{GS1} equal to V_{TH2}. This condition guarantees that the overdrive voltage and current of M_2 are robust to the process variations, relevant fact to achieve an adequate compensation of the PVT variations. Using the higher order model previously described for the drain current, the W_1 is fixed at 3.2 μm, and adjusted through the simulator at 2.6 μm.

The temperature slope of I_{M2} is fixed by means of its width. Its value is set at 7.8 μm to achieve a slope of 250 $\frac{nA}{^{\circ}K}$. Lastly, the PMOS current mirrors are implemented with composed transistors based on $svtpfet$ transistors, since these provide a much higher output impedance that the simple mirrors, and require less voltage than implemented with other sort of transistors such as $hvtpfet$ or $pfet$. Additionally, these characteristics

	$\mathbf{V_{TH}(mV)}$			
Type	$\sigma = 3$	Typ	$\sigma = -3$	Abs. Var.
lvtnfet	101.20	176.99	251.05	-75.79,+74.06
lvtpfet	207.82	298.42	387.12	-90.06,+88.70
nfet	186.17	261.31	336.77	-75.14,+75.46
pfet	272.37	361.94	449.97	-89.57,+88.03
hvtnfet	252.60	329.24	404.21	-76.64,+74.97
hvtpfet	313.85	408.12	500.57	-94.27,+92.15
svtnfet	254.38	340.94	425.81	-86.56,+84.87
svtpfet	244.32	342.74	437.04	-98.42,+94.30
uvtnfet	356.18	441.28	524.57	-85.10,+83.29
uvtpfet	436.65	533.21	620.58	-96.56,+87.37

Table 2.4: Threshold voltage variations for NMOS transistors with L=200 nm.

are achieved at the expense of a low increment of area regarding to the simple mirror.

The channel length for these transistor is fixed at 500 nm, and stacked transistors are made 3 times greater than the grounded. This factor is used because it provides an excellent ratio between die area and output impedance. The value for W_4 and W_5 is set at 7 μm with multiplicity factors of 6 and 2 respectively.

The second section of the bias scheme is composed by the transistors M_6, M_7, M_8, M_{21} and M_{22}. This branch is in charge to compensate process corners with a same deviation, that is N_F-P_F and N_S-P_S. The key in this compensation branch is the similarity of the absolute variations of the threshold voltage for some transistors of the technology, and a level shift given by the process. To achieve a higher clarity about it, the variations of the threshold voltage for most SOI NMOS and PMOS transistors is given in Table 2.4. As it can be observed, the absolute variation among the different transistors is very similar, which allows generating a voltage shift equal to one Δ of the threshold voltage.

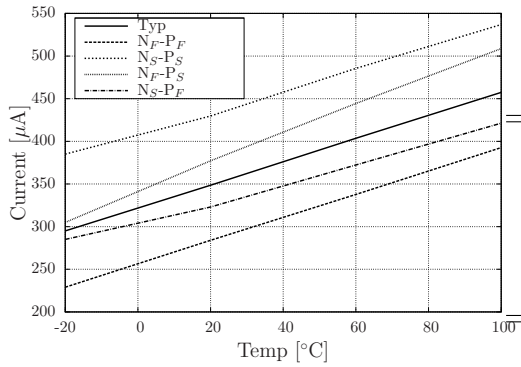
Now, we will describe how the circuit senses process variations at corners with a same deviation. When process has a positive deviation, the gate voltage of the transistor M_3 has a reduction of two ΔV_{TH} approximately, because of M_2 and M_3. Nevertheless, its current keeps constant because of the feedback loop, important and useful fact for the compensation. On the other hand, the gate of the grounded transistor, M_6, perceives a reduction of two ΔV_{TH}, and therefore its overdrive voltage is reduced by one ΔV_{TH} regarding the typical case. This condition entails a decrease of the current injected toward M_{24}, just like the core cell requires it at this process corner. The situation is similar for

the negative deviation, but instead of a reduction, a bigger current injection toward M_{24} is generated.

The transistor M_6 used for injecting the output current is an $uvtnfet$ transistor. Its choice is based on its high V_{TH}, which allows reducing the power consumption associated to this branch. In addition, it shows a higher output impedance than $svtnfet$, $hvtnfet$ and $nfet$ transistors for the same level current. It should be noted that this transistor has a PTAT behavior in its drain current, favorable fact to achieve the PTAT behavior desired at the output current. Just like the other NMOS transistors, the channel length of M_6 is set at 200 nm, and its width its fixed at 4 μm to obtain the current unbalance required for the core cell. Just the same as the first PMOS current mirror, the channel length and width of M_7 ans M_8 are 500 nm and 7 μm, but the multiplicity factors are 3 and 1 respectively, instead of 6 and 2.

When the circuit falls into these process corners, the transistors M_{11} and M_{12} ideally do not have changes on their drain currents because of process variations. However, it is dependent on the temperature because of the PTAT current injected by transistors M_{13} and M_{14}. For the combined corners, N_F-P_S and N_S-P_F, transistor M_6 operates similarly than at corners with the same deviation, while transistors $M_{9,10}$-$M_{11,12}$ begin operating. If the N_F-P_S corner arises, a strong increment of M_{11} drain current, and therefore of the current injected by M_{19} toward the transistor M_{24}, is generated. This injection is made bigger than the non-injected current by M_{21}, and the output current is a little greater than its typical value. The opposite situation happens when process corner is N_S-P_F. At that moment, the unbalance decreases the current of M_{11}, and transistor M_{19} injects less current than for the typical case toward M_{25}. With these unbalances it is possible to achieve the current requirement for the core cell. Trying to reduce the power consumption of the circuit, the ratio of all current mirrors is increased up to the output composed transistor.

To size this stage of the bias scheme the influence of the multiplicity factor between the transistors M_{11} and M_{12} was analyzed, and was fixed a ratio 1:1, since this provides the lowest temperature slope, and allows reducing the power consumption of the branch. Additionally, the channel length and width are fixed at 0.2 μm and 6 μm respectively, in order to keep the similarity with the core cell and the rest of the bias circuit. On the other hand, the ratio 3:1 previously used for the PMOS mirrors is applied over its current mirror too. The sizing of the rest of the transistors used for delivering the current is made by means of the simulator. An important fact is the presence of the transistor M_{23}



PC	Temp -20°C	20°	60°C	100°C
Typ	295 μA	348.6 μA	403.6 μA	457.4 μA
N_F-P_F	229 μA	284.0 μA	337.7 μA	392.7 μA
N_S-P_S	385 μA	429.7 μA	485.5 μA	536.9 μA
N_F-P_S	305 μA	377.2 μA	444.3 μA	508.7 μA
N_S-P_F	285 μA	323.0 μA	372.3 μA	421.3 μA

Figure 2.13: Output current of the bias scheme.

located in parallel to the output transistor, which allows sinking the remaining current of the design process. Lastly, the final dimensions and the behavior of the circuit for the different process corners, power supply at 1 V, and the temperature range from -20 to 100 °C are shown in the Table 2.5 and the Figure 2.13. The power consumption of the bias scheme for the typical, worst and best case of operation are 607, 757 and 398 μW respectively.

Tran.	Type	Var.	Val. [μm]	Var.	Val. [μm]	m
M_1	lvtnfet	W	2.60	L	0.20	1
$M_{2,3}$	nfet	W	7.80	L	0.20	2
$M_{4,17,21}$	svtpfet	W	7.00	L	0.50	6
$M_{5,18,22}$	svtpfet	W	7.00	L	0.50	2
M_6	uvtnfet	W	4.00	L	0.20	1
M_7	svtpfet	W	7.00	L	0.50	3
M_8	svtpfet	W	7.00	L	0.50	1
$M_{9,10}$	svtpfet	W	2.00	L	0.50	1
$M_{11,12,15,16}$	svtnfet	W	6.00	L	0.20	1
$M_{13,19}$	svtpfet	W	7.00	L	0.50	12
$M_{14,20}$	svtpfet	W	7.00	L	0.50	4
M_{23}	lvtnfet	W	4.40	L	0.20	1
M_{24}	lvtnfet	W	7.00	L	0.50	3
M_{25}	lvtnfet	W	7.00	L	0.50	9
M_{S1}	lvtnfet	W	7.00	L	0.50	18
M_{S2}	lvtnfet	W	7.00	L	0.50	6

Table 2.5: Final dimensions of the proposed bias scheme.

2.6 Simulation Results

Once the core cell and bias circuit were designed, it is time to join them to check the right behavior of the whole active inductor, and getting a description both quantitative and qualitative of its performance, specifically regarding the PVT variations. Initially, we make a characterization of the inductor performance for nominal conditions: typ-typ process corner, power supply at 1 V, and temperature at 60 °C. According to the literature, the most common specifications used for characterizing the active inductor performance are the area, power consumption, maximum quality factor and noise. The results obtained for each one of these and others additional specifications are summarized in Table 2.6, where the obtained results in this work and other similar works are compared. As it can be observed, the obtained results show a quite good performance for the circuit, where the most remarkable points are the low power consumption and the infinity quality factor.

The core cell proposed in this work can be tuned by changing the tail current of the differential pair, and so their transconductances. Applying this method, the inductance range is between 4.77 and 14.84 nH, at 6.649 and 3.72 GHz respectively. This inductance range is achieved by altering the control current, J_C, between 30 and 70 μA. However, there exists an strong limitation in this tuning method. Once the control current is changed, the operation conditions of the bias scheme are disturbed and the compensation process works differently. That is, the temperature slope and the current unbalances change and give as a result new current values for the core cell at the different process

Reference	[26]	[35]	[36]	[37]	[38]	**This work**
Year	2006	2008	2002	2005	2008	2011
$\mathbf{V_{DD}}$ **[V]**	1.5	1.8	±1.5	1.5	3.0	1
Power [mW]	68-18	2.55	2.7	3.9	5.52	3.06-0.93
$\mathbf{Q_{Max}}$	100	1000	126	35	160	∞
Application	Ph. Shifter	RF Filter	RF Filter	VCO	AI	VCO
Area [$\mu\mathbf{m^2}$]	22000	12.96[1]	NR	NR	2500	105.44
$\mathbf{L_{Range}}$ **[nH]**	2.5-13.6	15-50	51.6	1.7-6.3	0.21-0.36	4.77-14.84
$\mathbf{F_{Work}}$ **[GHz]**	5.00	4.95	1.00	4.00	28.50	5.29
FOM [$\frac{\mathbf{Hz}}{\mathbf{W}}$]	112.07	123.20	NC	120.71	124.34	124.16
Technology [nm]	CMOS 130	CMOS 180	CMOS 350	CMOS 180	BiCMOS $SG25H3$	SOI-CMOS 45

! [1] It does not include the current sinkers area.

Table 2.6: Comparison of the obtained results for the active inductor.

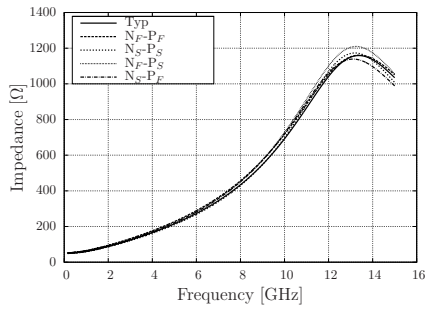
and temperature combinations. On the other hand, it is worth noting that this is a coarse tuning method, and it would be useful an additional fine method that allows adjusting precisely the inductance value. The Maneatis's principle or the tuning of a varactor can be used to achieve it, allowing to change the PMOS transconductance of the transistor connected as a diode, or the integration capacitance without modifying excessively the effect of the compensation process.

After searching Figure-Of-Merits (FOMs) used to compare the AI performance, we realized that there is none for this sort of circuit. Because of this, we decide to propose one based on their most relevant specifications. However, in accordance with our criterion, it is unfair to include the most important specification of the active inductors, quality factor, because our topology achieves an infinity value. Moreover, the noise and the inductive frequency range are not reported in most of the works; meanwhile, the area is referred to the layout or simply is not reported , which makes difficult its inclusion in the FOM. Taking into account the previously mentioned, the FOM proposed only considers the average power consumption, the inductance range and the work frequency, just like is shown in the Equation 2.30. Based on the scores at the Table 2.6, we conclude that the results obtained in this master project are competitive, achieving the second best FOM, even against circuits implemented in a technology with better characteristics like BiCMOS. It is worth mentioning that this work is the second reported active inductor in SOI CMOS technology, and the first that tries to compensate the PVT variations over this useful and versatile circuit.

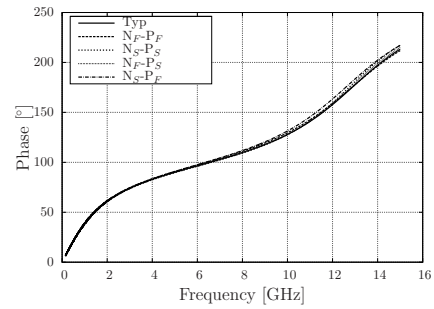
$$\mathbf{FOM} = 10\log\left(\frac{(L_{max} - L_{min}) * F_{Work}}{L_{Aver} * P_{Aver}}\right) \tag{2.30}$$

2.6.1 PVT Variations Results

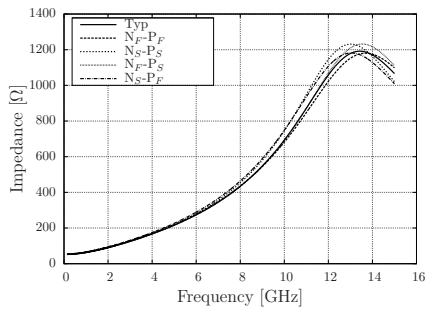
The ultimate objective of this project is to obtain an active inductor with a relative variation between ±10% for its most important specifications regarding the PVT changes, specifically its inductance value. To determine how effective the compensation process is, the power supply is fixed at 1 V, and the process corners with the temperature points handled along the design are altered. The frequency and transitory response of the active inductor for the different corners and temperatures are shown in Figures 2.14(a)-2.14(h) and 2.15(a)-2.15(h). As it can be observed, the inductive behavior is kept similar to the typical case, although them are specific variations caused by the deviations of the tail



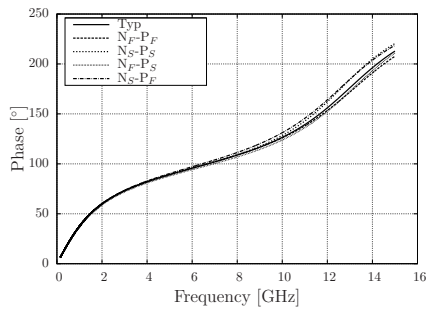
(a) Impedance magnitude at -20 °C.



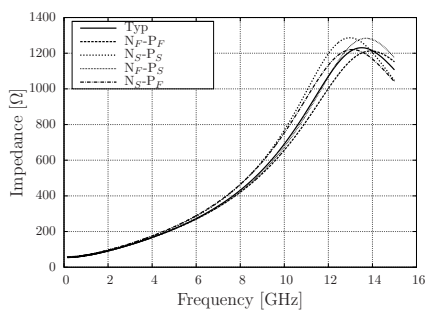
(b) Impedance phase at -20 °C.



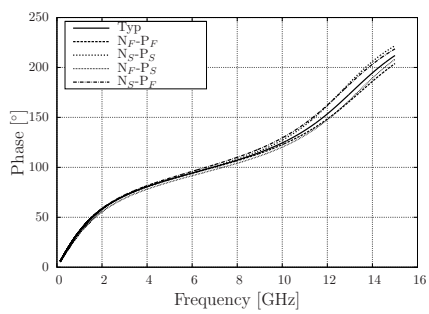
(c) Impedance magnitude at 20 °C.



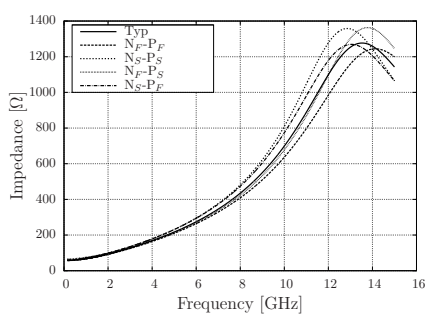
(d) Impedance phase at 20 °C.



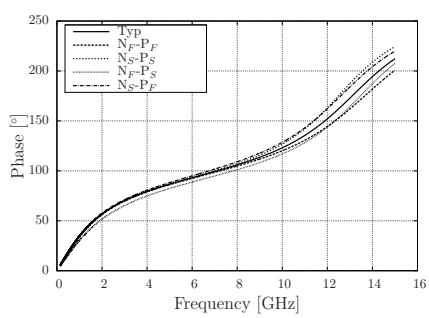
(e) Impedance magnitude at 60 °C.



(f) Impedance phase at 60 °C.

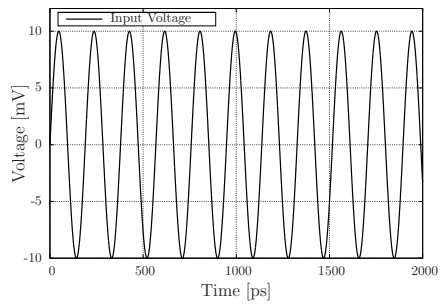


(g) Impedance magnitude at 100 °C.

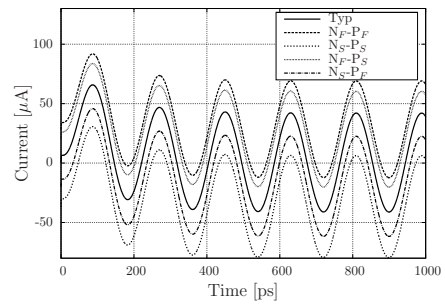


(h) Impedance phase at 100 °C.

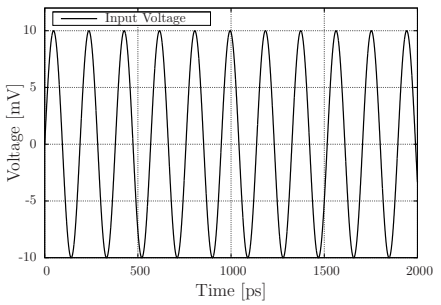
Figure 2.14: Frequency response of the active inductor for the different process corners and temperatures, and V_{DD}=1 V.



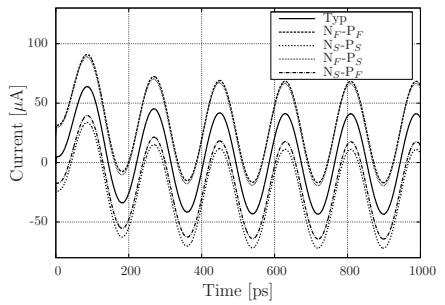
(a) Input voltage at -20 °C.



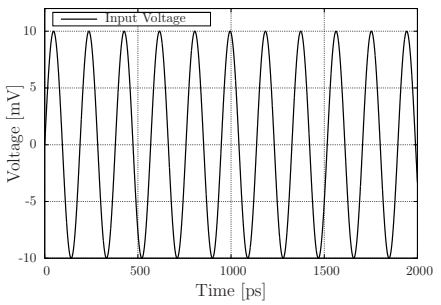
(b) Output current at -20 °C.



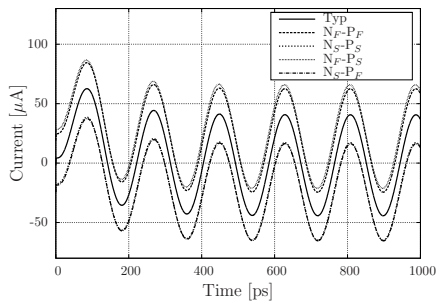
(c) Input voltage at 20 °C.



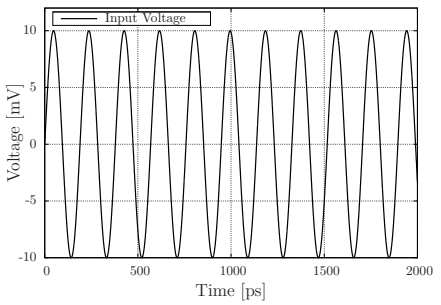
(d) Output current at 20 °C.



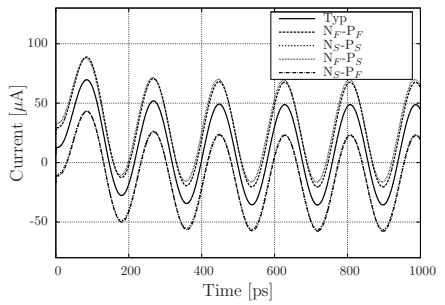
(e) Input voltage at 60 °C.



(f) Output current at 60 °C.



(g) Input voltage at 100 °C.



(h) Output current at 100 °C.

Figure 2.15: Transitory response of the active inductor for the different process corners and temperatures, and V_{DD}=1 V.

current regarding its ideal value. In spite of having a different location for the impedance peaks, it is little important because the operation band is located around 4.8 and 5.8 GHz. In this band, the variations of both impedance and phase are in a narrow margin about of ±3%, giving as a result a reduction of the effect of the process and temperature variations on the frequency behavior of the active inductor. Just like in the design section of the core cell, the inductance value is calculated at the frequency where the impedance phase is equal than 90° for the typical case. It is worth mentioning that this frequency value changes because of the process and temperature variations, and it must be considered to quantify precisely the inductance value. On the other hand, the transitory response has similar behaviors for the different combinations of process and temperature, showing a different amplitude and settling time. The most notable difference among transient responses is the DC shifts come from of the offset between the output transistors. However, this DC offset is not so important for the proper operation of the oscillator, since this has a common mode feedback circuit that compensates this problem. As reference point to calculate the relative variations of the inductance we use the operation nominal conditions. At this specific point, the results obtained are an inductance to the value 7.008 nH and an infinity quality factor at 5.3035 GHz. The rest of results are reported in Table 2.7. Each combination of PT in the Table has three items: the inductance value, the relative error of the inductance value with regard to the nominal value, and the quality factor of the inductor at 5.3035 GHz. The results show that compensation process is effective, since the

			PC		
Temp	N_S-P_S	N_S-P_F	***Typ***	N_F-P_S	N_F-P_F
	7.014 nH	7.171 nH	7.192 nH	7.376 nH	7.350 nH
-20°C	0.09%	2.32%	2.63%	5.25%	4.89%
	26.43	19.30	21.82	25.86	19.95
	7.217 nH	7.332 nH	7.054 nH	6.918 nH	6.921 nH
20°C	2.99%	4.62%	0.65%	-1.27%	-1.23%
	40.27	23.61	41.81	184.27	55.90
	7.297 nH	7.290 nH	7.008 nH	6.807 nH	6.699 nH
60°C	4.13%	4.02%	0%	-2.86%	-4.39%
	541.40	49.13	∞	19.72	73.85
	7.501 nH	7.369 nH	7.058 nH	6.849 nH	6.588 nH
100°C	7.03%	5.16%	0.71%	-2.26%	-5.98%
	56.90	466.74	49.59	10.16	25.20

Table 2.7: Variation of the inductance regarding PT changes, V_{DD}=1 V.

Temp	N_S-P_S	N_S-P_F	PC *Typ*	N_F-P_S	N_F-P_F
-20°C	6.258 nH	6.608 nH	6.572 nH	6.375 nH	6.585 nH
	1.21%	6.88%	6.29%	3.11%	6.50%
	-10.69%	-5.69%	-6.21%	-9.02%	-6.03%
	49.41	19.16	22.12	66.08	24.31
20°C	6.402 nH	6.552 nH	6.163 nH	5.900 nH	5.937 nH
	3.55%	5.97%	-0.31%	-4.57%	-3.97%
	-8.63%	-6.50%	-12.04%	-15.80%	-15.27%
	158.59	41.74	4010.34	35.53	92.51
60°C	6.469 nH	6.521 nH	6.183 nH	5.868 nH	5.813 nH
	4.63%	5.47%	0%	-5.08%	-5.97%
	-7.68%	-6.94%	-11.76%	-16.25%	-17.04%
	68.67	382.51	47.80	16.05	25.43
100°C	6.626 nH	6.587 nH	6.254 nH	5.914 nH	5.763 nH
	7.17%	6.53%	1.15%	-4.33%	-6.78%
	-5.44%	-6.00%	-10.74%	-15.59%	-17.75%
	32.32	66.68	25.94	10.45	15.87

Table 2.8: Variation of the inductance regarding PT changes, V_{DD}=1.1 V.

maximum variation of the inductance value is a little larger than 7 %, in the N_S-P_S process corners at 100 °C, similar variation to that of an spiral inductor [39]. In addition, it is worth mentioning that the minimum quality factor achieved by the inductor is 10.16, in the N_F-P_S process corner at 100 °C, which represents a good performance for the proposed circuit. As it can be observed in the obtained results, 100°C is a critical temperature for the active inductor performance. This is mainly due to the large deviations of the tail current regarding the ideal value.

To complete the characterization of the active inductor, we vary the power supply from 0.9 to 1.1 V, and PT corners are evaluated again. The results for 1.1 V are reported in Table 2.8, while for 0.9 V are reported in the Table 2.9. Besides the inductance value, relative error and quality factor, these tables have a new data in the second row for each PT combination: the relative error to the local nominal inductance. As it can be observed, the internal variation of the inductance is relatively small, 7.17 % for 1.1 V and -10.73 % for 0.9 V, but regarding nominal inductance value is extremely large reaching a maximum value of 28.58% at N_S-P_S corner, temperature at 100°C and 0.9 V.

The variation of the inductance for 0.9 V is a result not only of the variations in the current of the core cell's sinker, but also of the low saturation degree of the input

Temp	N_S-P_S	N_S-P_F	PC *Typ*	N_F-P_S	N_F-P_F
-20°C	7.948 nH	8.059 nH	8.472 nH	8.881 nH	8.886 nH
	-2.43%	-10.73%	3.99%	9.00%	9.07%
	13.42%	15.00%	20.89%	26.79%	26.80%
	19.38	14.99	13.69	14.68	11.87
20°C	8.388 nH	8.340 nH	8.267 nH	8.413 nH	8.274 nH
	2.95%	2.38%	1.47%	3.27%	1.56%
	19.69%	19.02%	17.96%	20.06%	18.06%
	22.78	16.45	20.02	76.50	20.14
60°C	8.620 nH	8.357 nH	8.147 nH	8.223 nH	7.915 nH
	5.81%	2.58%	0%	0.93%	-2.84%
	23.01%	19.25%	16.26%	17.34%	12.94%
	49.36	25.60	45.33	18.84	68.39
100°C	9.010 nH	8.537 nH	8.195 nH	8.347 nH	7.716 nH
	10.60%	4.79%	0.60%	2.46%	-5.28%
	28.58%	21.82%	16.95%	19.11%	10.11%
	283.66	48.35	513.68	7.15	66.09

Table 2.9: Variation of the inductance regarding PT changes, V_{DD}=0.9 V.

transistors for this power supply value. Because of this, it is necessary to limit its minimum value to 1 V in order to guarantee acceptable saturation conditions, or to use a voltage regulator to eliminate or reduce the power supply variations.

To reduce the effect of the power supply on the active inductor performance, some changes to the bias scheme are made. Considering that the problem is associated to the behavior of the core cell sinker's current when the power supply changes, an NMOS sinker with a directly proportional behavior regarding it is added to the circuit. The sinker consists of the transistors M_{23} and M_{A-F}. On the other hand, the transistor M_{2a} is added in order to control the proportion between the temperature slope and the DC current generated by the PTAT cell. The modified bias scheme is shown in the Figure 2.16. With this new bias circuit, an increment of the current of the core cell's sinker is achieved when the power supply drops and vice versa, allowing us to reduce the relative error of the inductance value regarding the power supply variations. It is worth mentioning that the current sinker shows a marked dependence with regard to the process and temperature variations, which must be considered in order to obtain the desired results.

The dimensions fixed for the circuit are reported in Table 2.10. The power consumption of the circuit for typical conditions is 665.96 μW, while the value for the worst and

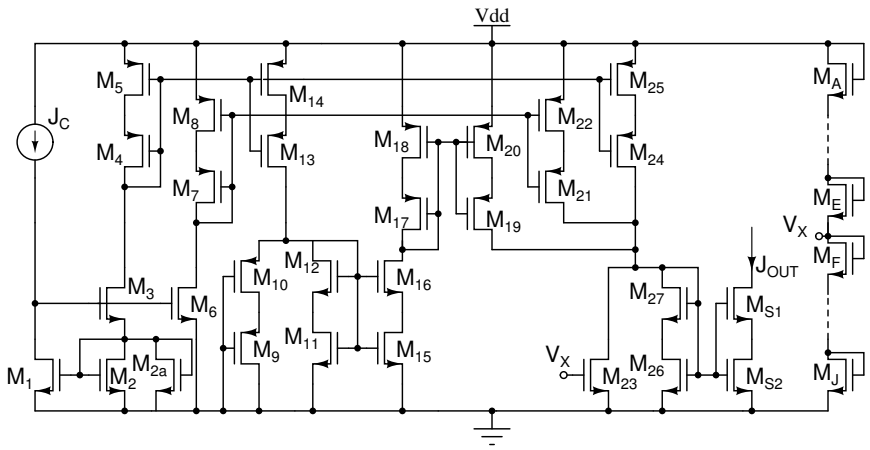


Figure 2.16: Modified bias scheme for compensating power supply variations.

Tran.	**Type**	**Var.**	**Val.** [μm]	**Var.**	**Val.** [μm]	**m**
$M_{1,2a}$	lvtnfet	W	2.60	L	0.20	1
$M_{2,3}$	nfet	W	7.80	L	0.20	2
$M_{4,19,21}$	svtpfet	W	5.00	L	0.50	6
$M_{5,20,22}$	svtpfet	W	5.00	L	0.50	2
M_6	uvtnfet	W	2.00	L	0.20	1
$M_{7,17,24}$	svtpfet	W	5.00	L	0.50	3
$M_{8,18,25}$	svtpfet	W	5.00	L	0.50	1
$M_{9,10}$	svtpfet	W	3.00	L	0.20	1
$M_{11,12,15,16}$	svtnfet	W	5.00	L	0.20	1
M_{13}	svtpfet	W	5.00	L	0.50	9
M_{14}	svtpfet	W	5.00	L	0.50	3
M_{23}	lvtnfet	W	1.60	L	0.50	1
$M_{26,S2}$	lvtnfet	W	5.00	L	0.50	4,8
$M_{27,S1}$	lvtnfet	W	5.00	L	0.50	12,24
$M_{A,B,C,D,E}$	lvtnfet	W	2.00	L	0.20	1
$M_{F,G,H,I,J}$	lvtnfet	W	2.00	L	0.20	1

Table 2.10: Final dimensions for the proposed bias scheme.

best operation case is 873.55 and 433.57 μW at N_S-P_S, 100 °C, 1.1 V and N_F-P_F, -20 °C and 0.9 V respectively. Lastly, it is worth mentioning that the area of the PMOS current mirrors was reduced almost 30% thanks to the compensation process made for the power supply variations.

The operation and performance of the active inductor are evaluated again through the PVT variations. The specifications obtained by means of the simulations, Table 2.11,

show an inductance value of 6.860 nH and an infinity quality factor at 5.3636 GHz, with a higher robustness regarding voltage variations than the previous active inductor . On the other hand, the maximum inductance deviation with regard to process and temperature increased 1.8% with regard to the results previously obtained.

Quantitatively, the changes to the bias scheme had a great impact over the circuit performance. The inductance variation for 1.1 V was reduced almost 50% regarding the previous results, and for 0.9 V the reduction achieved a higher percentage. In spite of the improvements, the maximum deviations reach values equals 16.83 and 24.61 % for 0.9 V, temperature at 100 °C, and process corners N_S-P_F, N_S-P_S respectively. This is due to the fact that, for these operation conditions, the input transistors are pushed by the load transistors to the linear region, where they lose its capacity for delivering current in an efficient way.

After describing in detail the proposed circuit, its operation principle, design flow, and finally the results obtained regarding PVT variations, it is time to compare how good our proposal is against others. To do so, we take the structure reported by Akbari-Dilmaghani in [25], Figure 2.4(d) but without feedback resistors. The circuit is designed under the same considerations than the active inductor proposed in this work. That is, channel length equal to 200 nm for the transconductors, overdrive voltage of 100 mV and a nominal inductance of 6.940 nH at 3.6132 GHz. The power consumption used for obtaining the required inductance value is 3.20 mW, which is distributed in three equal parts among the transconductors and the Common-Mode FeedBack (CMFB) circuit. It is worth mentioning that the tail sinkers are implemented by means of ideal elements of the simulator, with the purpose to clearly observe the effect of the process and temperature variations over the circuit performance.

Once the circuit is sized, we apply only the PT variations and record the changes of its inductance value. The Akbari-Dilmaghani's topology shows a maximum deviation for the inductance of 35.34 % at the N_F-P_F and -20 °C combination, a value 4 times larger than our maximum deviation. The rest of results obtained in the simulations are reported in Table 2.12. This simple comparison shows how our bias scheme compensates the effect of the PVT variations over the performance of an active inductor. Besides, the interesting characteristics of the proposed core cell such as simplicity and efficiency make it an attractive option for its inclusion in high performance systems.

V_{DD}	Temp	PC N_S-P_S	N_S-P_F	Typ	N_F-P_S	N_F-P_F
0.9	-20°C	6.726 nH	7.201 nH	7.129 nH	7.576 nH	7.301 nH
		-1.94%	4.98%	3.93%	10.44%	6.42%
		145.94	23.85	30.50	48.79	25.50
	20°C	7.516 nH	7.541 nH	7.241 nH	7.463 nH	7.169 nH
		9.57%	9.93%	5.56%	8.79%	4.50%
		68.72	25.94	51.61	47.46	53.55
	60°C	7.996 nH	7.711 nH	7.276 nH	7.489 nH	7.056 nH
		16.56%	12.41%	6.97%	9.17%	2.86%
		2311.48	45.72	236.93	11.71	111.12
	100°C	8.548 nH	8.015 nH	7.407 nH	7.702 nH	6.949 nH
		24.61%	16.83%	7.97%	12.27%	1.30%
		51.00	133.46	37.55	5.84	27.28
1.0	-20°C	6.753 nH	7.072 nH	6.953 nH	7.100 nH	7.226 nH
		-1.54%	3.09%	-0.08%	3.50%	5.34%
		30.52	18.42	25.72	29.56	19.29
	20°C	7.069 nH	7.258 nH	6.880 nH	6.863 nH	6.967 nH
		3.05%	5.81%	0.29%	0.45%	1.56%
		40.85	21.82	43.40	463.86	38.98
	60°C	7.215 nH	7.275 nH	6.860 nH	6.771 nH	6.790 nH
		5.18%	6.05%	0%	-1.29%	-1.02%
		244.76	38.42	∞	21.35	242.88
	100°C	7.464 nH	7.396 nH	6.897 nH	6.764 nH	6.617 nH
		8.81%	7.82%	0.53%	-1.39%	-3.53%
		73.90	106.24	47.88	10.34	30.68
1.1	-20°C	6.559 nH	7.128 nH	6.767 nH	6.853 nH	7.319 nH
		-4.37%	3.90%	-1.34%	-0.10%	6.69%
		25.23	14.15	20.56	23.33	14.54
	20°C	6.749 nH	7.201 nH	6.663 nH	6.521 nH	6.888 nH
		-1.61%	4.97%	-2.86%	-4.93%	0.41%
		36.15	17.57	38.40	157.81	29.07
	60°C	6.796 nH	7.117 nH	6.646 nH	6.373 nH	6.630 nH
		-0.92%	3.75%	-3.10%	-7.09%	-3.34%
		160.14	29.76	199.79	31.84	945.20
	100°C	6.944 nH	7.138 nH	6.625 nH	6.284 nH	6.395 nH
		1.23%	4.06%	-3.41%	-8.39%	-6.76%
		97.93	69.98	61.23	14.43	33.85

Table 2.11: Variation of the active inductor specifications regarding PVT changes.

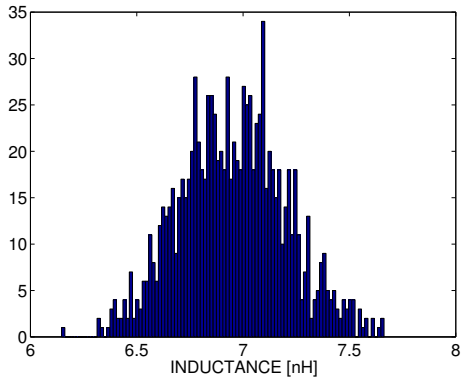
Temp	N_S-P_S	N_S-P_F	PC Typ	N_F-P_S	N_F-P_F
	5.820 nH	5.693 nH	5.078 nH	4.599 nH	4.486 nH
-20°C	-16.13%	-17.96%	-26.82%	-33.72%	-35.34%
	606.04	99.78	40.56	26.79	20.52
	6.844 nH	6.692 nH	5.961 nH	5.391 nH	5.255 nH
20°C	-1.37%	-3.56%	-14.10%	-22.30%	-24.27%
	57.81	93.85	121.29	35.06	29.03
	7.988 nH	7.801 nH	6.940 nH	6.285 nH	6.114 nH
60°C	15.10%	12.41%	0%	-9.43%	-11.89%
	39.11	42.27	∞	35.02	33.46
	9.282 nH	9.054 nH	8.028 nH	7.278 nH	7.058 nH
100°C	33.75%	30.46%	15.68%	4.87%	1.70%
	29.98	30.77	263.94	31.00	32.23

Table 2.12: Variations of the Akbari-Dilmaghani's active inductor regarding PT changes, V_{DD}=1 V.

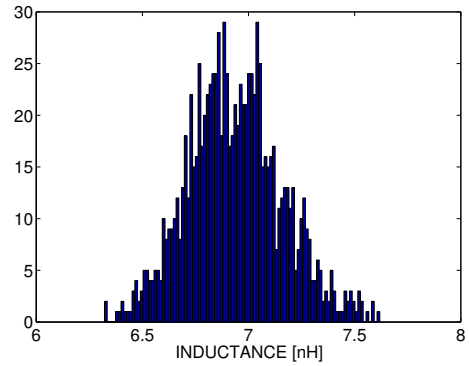
2.7 Statistical Analysis

Previously in this chapter, PVT analysis was used as a tool to determine the robustness of the active inductor under the worst operation conditions, and to know if the circuit is able to work in the limits of the technology. However, although those operation conditions change, it is the same variation of one or several characteristic parameters for all devices of the circuit. Actually, the parameters of every device change randomly around its typical value subject to correlation factors defined by the anisotropic properties of the fabrication process and the layout techniques used in the circuit. The statistical analysis, better known as Monte Carlo Analysis, enable us to study the circuit performance taking into account these random variations in order to determine its reliability. This analysis vary randomly the model parameters for every device around its typical value considering a Gaussian probability distribution, a certain number of samples fixed by the designer. In our case the number of samples set is 1000. With the purpose to compare in a fair way the advantages of our core cell, against the Akbari-Dilmaghani's circuit, we use ideal current sinkers to bias the circuit under nominal operation conditions; that is, typical process, power supply at 1 V and temperature at 60 °C.

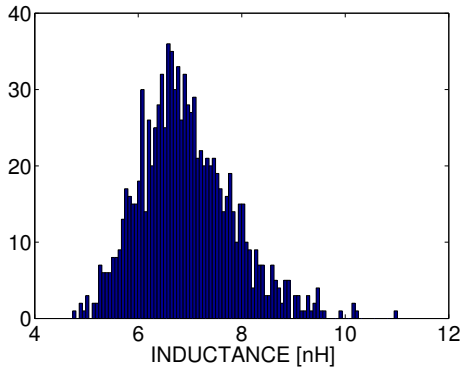
Monte Carlo analysis is used to determine the variability of the core cell's inductance at 5.3244 GHz, and Akbari's circuit at 3.6132 GHz. The results obtained for the core cell, Figure 2.17(a), show a mean value of 6.952 nH and a standard deviation of 0.2499 nH;



(a) Histogram of the Core Cell.



(b) Histogram of Akbiri-Dilmaghani's circuit.



(c) Results of the Monte Carlo Analysis.

Figure 2.17: Histogram of the complete active inductor.

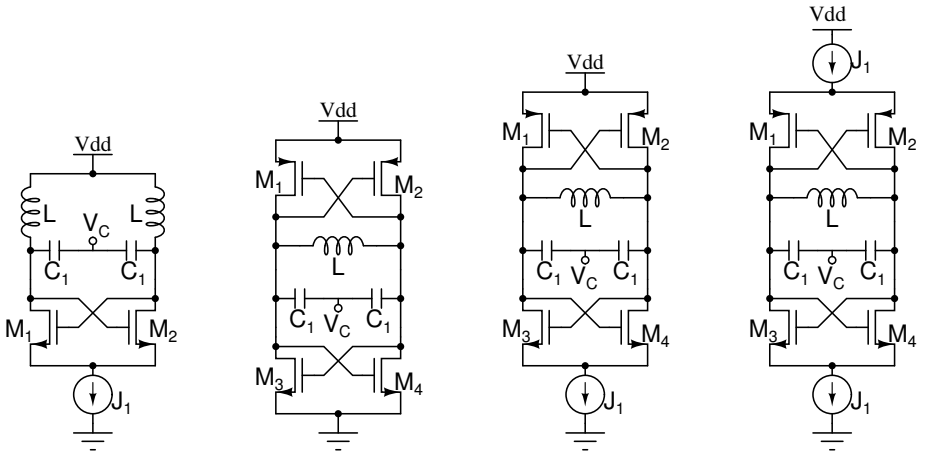
meanwhile, the Akbaris's circuit, Figure 2.17(b), has a mean value of 6.936 nH and a standard deviation 0.222 nH. As it can be observed, the core cell proposed in this work shows an standard deviation equal to the 3.59% of the mean value, similar to the Akbari's circuit. This value entails a high reliability and therefore a high yield. Even more important, this reliability is accomplished with a much lower die area and power consumption than other topologies like the Akbari's.

To finish, a Monte Carlo analysis on the core cell including the bias scheme is made. The obtained results show a mean value of 6.929 nH and a standard deviation of 0.905 nH, a value 4 times larger than using the ideal current sinkers. This indicates that the bias scheme shows a high sensitivity with regard to mismatch. Particularly, it is believed that the error comes from the mirroring made by the composed transistors, and the analog current switch used to identify the cross process corners. Lastly, the histogram of the inductance for the whole active inductor is shown in Figure 2.17(c).

Chapter 3

Active Inductor Based VCO

Once the active inductor is completely designed, the next step is including it into a VCO structure. The most common structures for LC-VCOs are shown in the Figure 3.1. These circuits show structures very similar, but those little changes exert a big difference between their performance, application fields and ability to adapt. The NMOS Cross-Coupled (CC) pair with current sinker, for example, Figure 3.1(a), does not allow using floating inductors, and the mismatch between the inductors could become a big problem. Its advantages stem in the few noise sources, and the possibility to compensate PVT variations changing its tail current. On the other hand, the double CC pair, Figure 3.1(b),



(a) NMOS CC pair with current sinker.

(b) Double CC pair.

(c) Double CC pair with tail sinker.

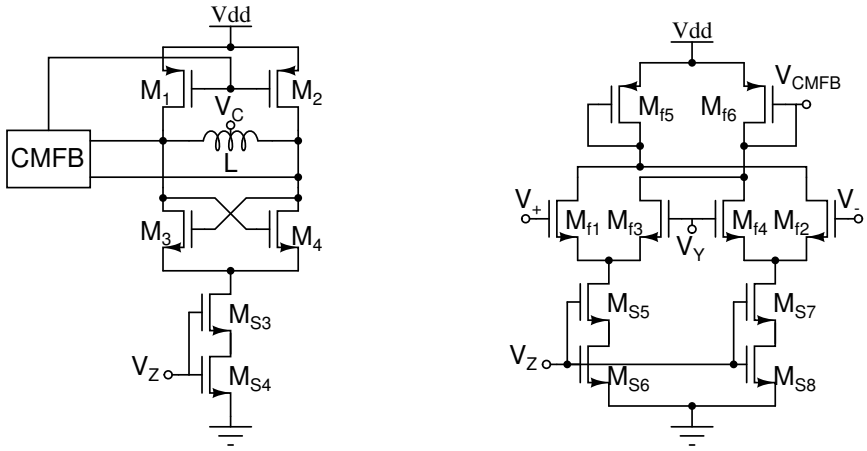
(d) Double CC pair with current source and sinker.

Figure 3.1: Oscilator topologies.

enables the circuit to use differential inductors because of its floating nature inside the circuit. According to the state-of-art, this VCO structure defines better the output waveform than the NMOS cross-coupled, and it is possible to reduce the phase noise in most of cases despite the increase in the number of noise sources. However, this circuit does not have any possibility to compensate PVT variations when it is implemented with passive elements, different to the double cross-coupled pair with one or two current sources, Figures 3.1(c) and 3.1(d) respectively.

The double CC pair with tail current sinker allows using floating inductors apart from having the possibility of compensating the PVT variations by adjusting the tank current. However, its PMOS grounded transconductor entails a direct and strong dependence on the input DC level of the active inductor regarding PVT variations. This is a huge problem for the proper biasing of the active inductor, which is avoided using the double CC pair with two current sources. This last VCO structure has the advantages of the rest: allows using floating inductors, compensating the effect of the PVT variations by adjusting the current tank, and controlling the input DC level of the active inductor. In addition, its structural similarity with the active inductor makes the bias scheme a key point to keep stable the negative resistance value of the CC pairs. An extremely exclusive characteristic of this structure is the presence of two current sources, since it prevents us biasing adequately to the active inductor, at least the PMOS CC pair and its current source operate in the sub-threshold region, which inserts high noise levels and deteriorates the phase noise of the oscillator. It should be noted that this structure would be proper if we had the complementary active inductor, and the bias conditions would meet the inductor.

Taking into account the arguments previously described, and after observing the performance obtained with the structures previously described, we decided to propose a variation of the NMOS CC pair with current sinker, looking for reduce the center frequency variations of the oscillator. With this new structure, the fine tuning mechanism is made by changing the inductance value through a varactor located inside of the inductor, while the coarse tuning is made by modifying the J_C current. It is worth mentioning that the structure is not complete yet, since it is necessary to add a CMFB circuit in order to fix an stable DC level that enables the inductor to work properly. The complete structure of the VCO is shown in Figure 3.2(a), where $M_{1,2}$ are current-source load and $M_{3,4}$ work as a negative resistance network.



(a) Proposed structure.

(b) Common-Mode Feedback Circuit.

Figure 3.2: Complete structure of the VCO.

The CMFB circuit used in this work, Figure 3.2(b), is a continuous-time circuit proposed by Martin in 1985, and subsequently modified by Duque-Carrillo in 1993 to increase its Common-Mode Rejection Ratio (CMRR) characteristic [33]. The CMFB circuit uses a reference voltage coming from the stacked NMOS transistors of the bias scheme, drain of the transistor M_D, Figure 2.16. This is done in order to adapt the dynamic range of the core cell in accordance with the power supply variations. After selecting the VCO structure and making a brief description of it, we shall begin the oscillator design with one key point of the structure, the cross-coupled pair.

3.1 Cross-Coupled Pair

As it was previously mentioned, the cross-coupled pair is a key point in the selected structure. First, it compensates the losses associated to the resonant tank through a continuous and periodic injection of current that allows the structure to keep stable the output oscillation. Second, and more important for the proper operation of our active inductor, it is a natural limiter of the output oscillation ranges, and therefore make easy the function of the CMFB circuit.

First of all, we select the sort of transistor to implement the CC pair in accordance with the operation conditions and restrictions. As it was previously mentioned, the proposed VCO structure consists of one NMOS CC pair with current-source load, and a CMFB

circuit. Because of the power supply limitation and the need of adequately biasing the transistors, they are leaded close to the edge between saturation and sub-threshold region, where they are more susceptible to the PVT variations. However, and despite its bankruptcies, the Low-Voltage (lvt) transistors operate far from this edge, which makes them the most suitable option for implementing the CC pair, the diode-connected load of the CMFB and therefore the current-source load of the VCO structure. In addition, we can not forget that its influence over the current sinker is lower than any other sort of transistor.

Once the sort of transistor has been chosen, the CC pair is sized considering a rough estimation of the losses of the tank associated to the output impedances of the active inductor, the current-source load and to the CC pair, Equation 3.1, where $I_{Tail-Ind}$ is the inductor tail current, I_{CC} is the CC pair tail current, and the subscripts I and V of the channel-length modulation factor denote the belongings to the inductor and the VCO structure, respectively.

$$G_{Loss} \approx 0.825 * I_{Tail-Ind}(\lambda_{nI} + \lambda_{pI}) + 0.5 * I_{CC}(\lambda_{nV} + \lambda_{pV})$$
$$G_{Loss} \approx 330e-6 * (0.35 + 0.45) + 150e-6 * (1.35 + 0.53) = 546.0\ \mu S \tag{3.1}$$

The values used in the previous equation for the channel-length modulation factor belong to channel lengths of 200, 150 and 50 nm used in the active inductor, the current-source load and the CC pair respectively. It is worth mentioning that although the gate leakage of the transistors of the input transconductor and the CC pair represent a loss resistance, this was estimated for low- frequency and disregarded due to its low value.

Generally, the negative resistance generated by the CC pair is made a couple of times larger than the equivalent loss resistance to guarantee the beginning of the oscillation in spite of the PVT variations. In this design, we chose a factor 3 times, which guarantees the oscillation and allows reducing the power consumption of the VCO, while it is achieved an acceptable performance in the phase noise.

After estimating the losses, we made a sweep to set the width of the CC pair transistors. The channel width for the transistors is fixed at 2 μm. With these dimensions, we obtain a compensation transconductance equal to 1.516 $\frac{mA}{V}$.

On the other hand, the CMFB circuit is sized using the design considerations described along the second chapter. The tail currents are fixed at 150 μA, the NMOS channel length

Tran.	Type	Var.	Val. [μm]	Var.	Val. [μm]	m
$M_{1,2}$	lvtpfet	W	1.50	L	0.15	3
$M_{3,4}$	lvtnfet	W	2.00	L	0.05	1
M_{f_1,f_2,f_3,f_4}	lvtnfet	W	1.50	L	0.05	1
M_{S_3}	lvtnfet	W	5.00	L	0.50	18
M_{S_4}	lvtnfet	W	5.00	L	0.50	6
M_{S_5,S_7}	lvtnfet	W	5.00	L	0.50	9
M_{S_6,S_8}	lvtnfet	W	5.00	L	0.50	3

Table 3.1: Final dimensions of the VCO structure and CMFB circuit.

is 50 nm and the PMOS channel length is 100 nm. The final dimensions for the VCO structure and the CMFB circuit are reported in Table 3.1.

With the VCO structure and the active inductor designed, the last step to complete a functional VCO is to select the varactors that allow tuning the output frequency of the oscillator. In the next section, the most important characteristics and constraints of the varactor, with some details about its electric model will be mentioned.

3.2 Varactor

A varactor is an adjustable capacitor that behaves linearly for a certain range of the control signal. The electrical model used for describing its behavior consists of an adjustable ideal capacitor in series with a resistance dependent on the operation frequency, as shown in Figure 3.3. The varactor can operate mainly in two modes: inversion and accumulation. The first one shows a lower parasitic resistance, so a higher operation frequency and quality factor. However, the noise injected through the substrate is higher, and the tuning range is narrower than in accumulation mode.

In a 45 nm PD-SOI CMOS technology, this element is implemented by an NMOS accumulation varactor; that is, an NMOS transistor except for the fact that it is made over an N-Well instead of a P-Well. This fact increases the varactor tuning range, since allows eliminating the parasitic capacitances associated from drain-source to body [7].

The variables which define its range of values are the channel length (L), either 0.232 μm or 0.472 μm, the channel width (W), and the number of fingers (nf). The mathematical model for this device has been fitted for the range -0.5 V $< V_{G,SD} <$ 1 V. Below -0.5 V, the model is no longer valid due to the hole generation.

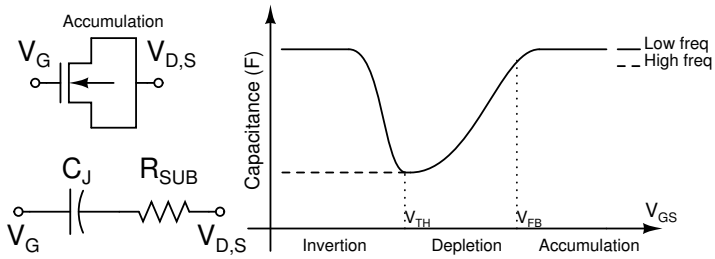


Figure 3.3: Scheme, passive equivalent and transfer function of a varactor.

As it was previously mentioned, the voltage range of V_{G-SD} to change the capacitance value of the varactor is around -0.5 to 1 V. However, after observing the operation conditions of the varactor, we decided to reduce it between -0.5 V $<$ V$_{G,SD}$ $<$ 0.5 V, because of the quasi-linear relationship between those two variables for this voltage range. Considering that the differential oscillation range expected inside the active inductor is close to 200 mV$_{PP}$ over a DC level of 600 mV, the control voltage is restricted to the range 0.2-1.0 V, as shown in Equation 3.2, where V_{out1} is one output terminal of the oscillator.

$$\begin{gathered} -0.5\ V \leq V_{out1} - V_{ctrl} \leq 0.5\ V \\ 0.5\ V \leq V_{out1} \leq 0.7\ V \\ 0\ V \leq V_{ctrl} \leq 1.0\ V\ \cap\ 0.2\ V \leq V_{ctrl} \leq 1.2\ V \\ 0.2\ V \leq V_{ctrl} \leq 1.0\ V \end{gathered} \tag{3.2}$$

To select the dimensions of the varactor, we analyze the oscillation conditions of the circuit. As it can previously mentioned, the varactor is located inside the active inductor for changing the inductance value. Thus, the capacitance of the resonant tank consists of the capacitance of the input transconductor, the CC pair and the drain-gate capacitance of the various transistors connected to the output node. A crude approximation of this capacitance is 94.79 fF. Considering this, the required inductance value to obtain an oscillation frequency of 5.363 GHz is 9.3 nH.

To reach this inductance value, we introduce the varactor in the integration nodes of the active inductor. For convenience, we fix the channel length at 0.232 μm, the channel width at 4.64 μm and the control voltage at 0.7 V. Subsequently, we sweep the number of fingers of the varactor and set it at 4. With the selected dimensions, the capacitance range of the varactor is between 10.88 fF and 39.42 fF. Meanwhile, the center frequency

and phase noise of the oscillator are 5.293 GHz and -81.52 $\frac{dBc}{Hz}$@1 MHz, respectively. Due to the low value of the phase noise, we adjust some dimensions of the active inductor and we evaluate again the results obtaining a center frequency and phase noise of 5.360 GHz and -88.04 $\frac{dBc}{Hz}$@1 MHz.

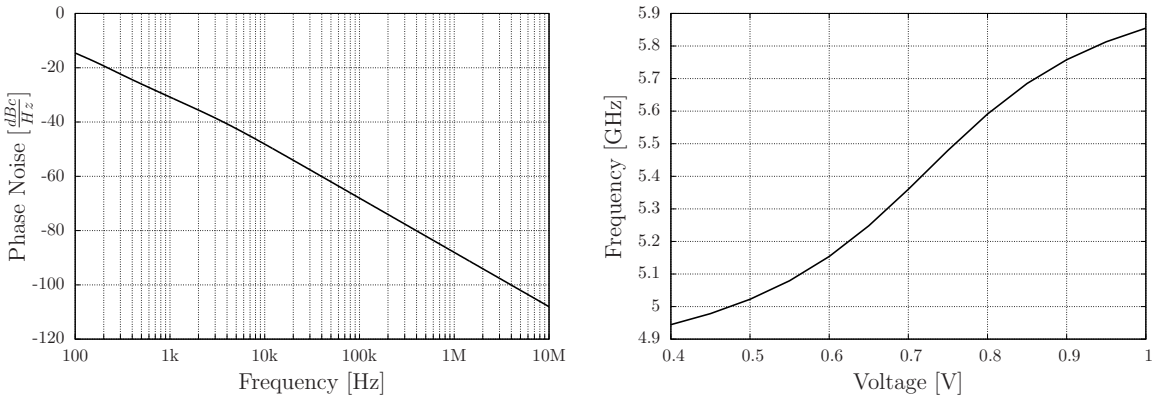
Once the oscillator is designed, we shall carry out a characterization stage of the oscillator to evaluate and to quantify its most important specifications, among them its center frequency, phase noise, tuning range and power consumption.

3.3 Simulation Results

Once the VCO structure was designed, we will perform a characterization stage of the oscillator under nominal conditions, as it was done with the active inductor. In this initial stage, we will evaluate the most important specifications of the inductor, such as the center frequency, the phase noise, the power consumption and the tuning range. Subsequently, we will do a comparison with others works using a traditional FOM reported in the literature.

As it was previously mentioned, the oscillator has a center frequency of 5.360 GHz, with a phase noise of -88.04 $\frac{dBc}{Hz}$@1 MHz. The behavior of the latter is shown in Figure 3.4(a). Despite not being an outstanding result, the phase noise shows an acceptable value considering that the SOI transistors are more noisy than Bulk transistors [40], like the composed transistor with regard to the simple.

As it was previously mentioned, the frequency tuning of the oscillator is made by means of two mechanisms. The fine method, by changing the capacitance value of the varactor, and the coarse method, by modifying the J_C current. Initially, we evaluate the results of the fine method sweeping the control voltage from 0.4 to 1 V. The obtained tuning range is 910 MHz, covering the frequency band from 4.944 GHz to 5.854 GHz as shown in Figure 3.4(b). From the previous result, we obtain the Frequency Tuning Range (FTR) of the oscillator for nominal conditions using the Equation 3.3, which yields a value of 16.97% and a tuning constant ($\mathbf{K_{VCO}}$) of 1.516 $\frac{GHz}{V}$. On the other hand, the power consumption of the VCO for nominal conditions has a value of 2.629 mW@1 V, relatively low value compared with other VCOs reported in the state of the art, like will be shown in a next section.



(a) Phase noise of the VCO.

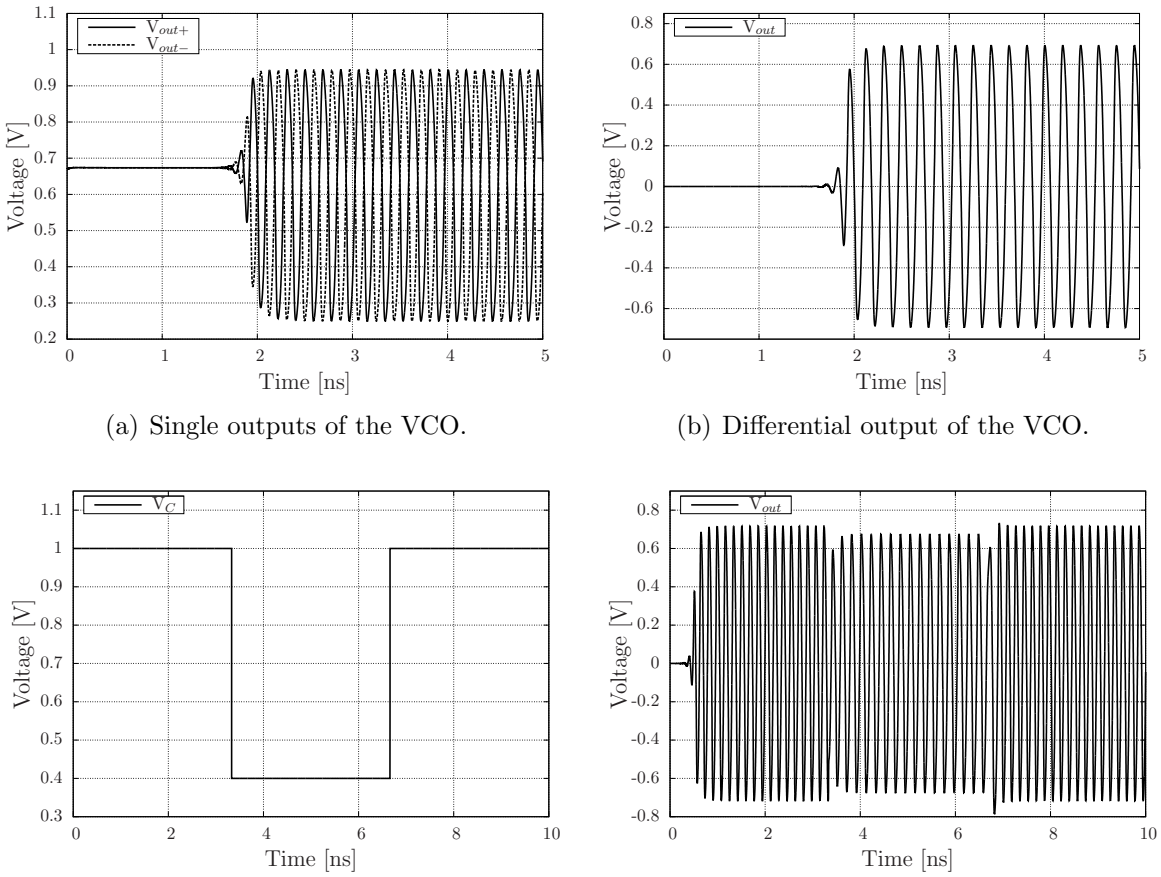
(b) Tuning range of the VCO.

Figure 3.4: Frequency characterization of the VCO.

$$\mathbf{FTR} = \frac{f_{max} - f_{min}}{f_{center}} * 100\ \%\ ;\ \mathbf{K_{VCO}} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \tag{3.3}$$

Lastly, we perform a transient analysis to observe the most important characteristics of the output oscillation. In Figure 3.5, we can visualize the outputs both single as differential of the oscillator, where it is observed a notable shift of the DC level from 670 to 600 mV, that can be confused with an asymmetry between the maximum and minimum peaks of these signals. Although it is believed that this shift is the main reason to have obtained a phase noise so high, this operation point yielded the best result for this specification. To finish the transient analysis, it is worth remarking the most important characteristics of the transient response of an oscillator: the startup and settling time.

The obtained results in this design show an startup time around 1.6 ns and a settling time close to 600 ps for a control voltage of 0.7 V, this latter measurement very similar to the active inductor's. It should be mentioned that the startup time has a dependent behavior with regard to the control voltage, since for V_C equal to 1 V, 0.7 V and 0.4 V is 250 ps, 1.6 ns and 1.88 ns respectively. This dependence suggests that to reduce the startup time the circuit must be initialized with a control voltage of 1 V. Additional to these temporal measurements, we determine the settling time for a change in the control voltage. The circuit is initialized with a control signal of 1 V, later changed at 0.4 V and lastly returned to 1 V, giving as a result the square signal of Figure 3.5(c). The transient response of the VCO for this entrance is shown in Figure 3.5(d). As it can be observed, the settling time is relatively short with a value of 300 ps for both the up-down and down-up transition of the control signal.



(a) Single outputs of the VCO.

(b) Differential output of the VCO.

(c) Control signal of the oscillator.

(d) Transient response for the control signal.

Figure 3.5: Transient characterization of the VCO.

The obtained result is quite good because it enables the oscillator to fulfill with the requirements of any system working in this frequency band.

To finish the verification stage, we obtain the total tuning range of the oscillator including the coarse tuning method. To do so, we alter the current J_C from 30 μA to 70 μA in steps of 10 μA, and sweep the control voltage from 0.4 V to 1 V. The obtained tuning ranges cover a frequency band of 4.309 GHz, from 3.192 GHz to 7.501 GHz, as it is shown in the Figure 3.6. Considering the previous result, the total FTR of the oscillator has a value of 80.39%, which is relatively large compared with the 15 % achieved by a passive LC VCO. Additionally, it is worth mentioning that the power consumption of the whole oscillator changes in accordance with the current J_C, from 1.201 mW@1 V for 30 μA to 4.157 mW@1 V for 70 μA of the control current respectively.

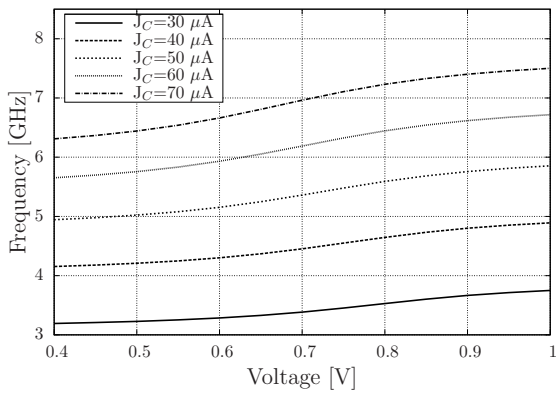


Figure 3.6: VCO's frequency band including the coarse and fine tuning methods.

To conclude this section, we perform a comparison of the obtained results in this work with regard to some reported in the state of the art. To do it, we use a traditional FOM reported in [41], Equation 3.4, which enables us to compare in a fair way all characteristics of our proposal, and not only its weak points. As it can be observed, the results obtained in this work are good, accomplishing the third best FOM despite limitations in the power supply. Although we achieved the lowest power consumption, the second higher center frequency and the second wider frequency band, it was not enough because of the unbalanced weighting for the different specifications of the oscillator. On the other hand, it is worth mentioning that this is the first work reported about active inductor based VCO on a SOI-CMOS technology. Once the VCO has been characterized under nominal conditions, it is time to analyze the VCO behavior regarding the PVT variations, particularly of its center frequency and phase noise measured at an offset frequency of 1 MHz.

$$\mathbf{FOM} = -\mathscr{L}(\Delta_f) + 10\log\left(\left(\frac{f_{osc}}{\Delta_f}\right)^2\left(\frac{FTR}{10}\right)^2\left(\frac{1mW}{P_{DC}}\right)\right) \tag{3.4}$$

3.4 PVT Variations Results

Throughout this work, we have guided the design looking to reduce the impact of the PVT variations over the circuit performance, and it is time to know how successful our considerations were. First of all, we will show the effect of the power supply, the temperature and the fabrication process, the latter in a detailed way, over the center frequency

Reference	[22]	[42]	[43]	[44]	[18]	This work
Year	2006	2007	2008	2008	2009	2011
V_{DD} [V]	1.8	1.8	1.5	3.3	1.8	1
Power [mW]	6-28	28	12-31	10	45	1.20-4.15
F_{Center} [GHz]	1.75	1.73	8.50	0.77	3.35	5.36
PhaseNoise [$\frac{dBc}{Hz}$]	-109.5	-86	-95	-105	-118	-88
BW [GHz]	0.5-3.0	1.32-2.15	6-11	0.68-1.45	0.2-6.5	3.1-7.5
FTR [%]	142.85	47.48	58.82	72.30	188.05	80.39
FOM [$\frac{Hz}{W}$]	185.15	149.81	175.65	169.91	197.95	176.44
Technology [nm]	CMOS 180	CMOS 180	CMOS 130	CMOS 350	CMOS 180	SOI-CMOS 45

Table 3.2: Comparison of the results obtained for the VCO.

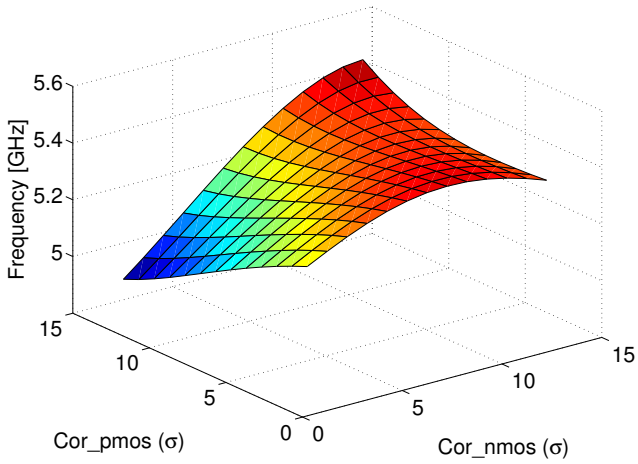
of the oscillator (f_o). To do so, we fix two parameters and sweep the other one so that we can discern only its effect over the circuit performance. The factors are combined as follows: first one, temperature at 60 °C and power supply to the value 1 V, sweeping process deviation for the PMOS and NMOS transistors; second one, typical process and temperature at 60 °C, sweeping the power supply value; and lastly, typical process and power supply at 1 V, sweeping the temperature. The obtained results for these tests are shown in the Figures 3.7(a)-3.7(c).

In the obtained results, we can observe a certain stability degree of the center frequency of the oscillator regarding the PVT variations. The first plot shows the response surface of the center frequency center according to a detailed variation of the deviation in the fabrication process. In this Figure, the axes shows a value from 1 to 13, which is transformed to a real deviation by means of the Equation 3.5. It should be mentioned that the points (0,0),(0,13),(13,0) and (13,13) of the Figure 3.7(a) are the corners N_S-P_S, N_S-P_F, N_F-P_S and N_F-P_F of the fabrication process.

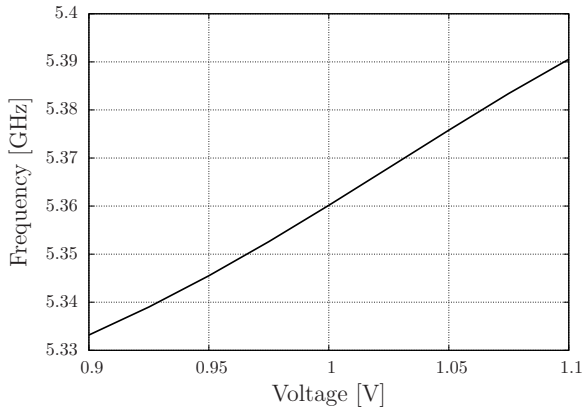
$$\sigma_n = \frac{Cor\_nmos}{2} - 3.5 \quad \& \quad \sigma_p = \frac{Cor\_pmos}{2} - 3.5 \tag{3.5}$$

From the recorded results, we obtain the minimum and maximum center frequency with values 4.949 GHz and 5.499 GHz respectively, which yields an error of -7.66 % and 2.59 % with regard to the nominal value, quite good results considering its active nature.

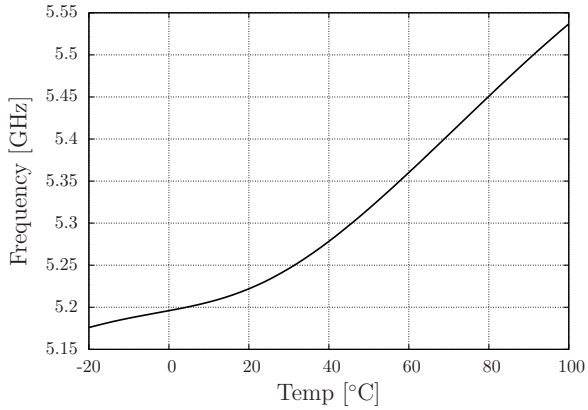
The influence of the power supply is relatively low reaching a variation of 57.46 MHz from 0.9 V to 1.1 V. This variation is equivalent to 1.07 % of f_o, and yields a variation



(a) Influence of the fabrication process over f_o.



(b) Influence of the power supply over f_o.



(c) Influence of the temperature over f_o.

Figure 3.7: Independent effects of the process, voltage and temperature over f_o.

constant of 286.60 $\frac{MHz}{V}$. On the other hand, temperature has been the most influential factor among the three when checking the behavior and performance of the circuit with regard to the PVT variations. In the last test made to the circuit, we found that the variation of the center frequency regarding the temperature reaches 360.84 MHz along the temperature range, and yields a variation constant around 3 $\frac{MHz}{°C}$.

To finish this chapter, we will generate a table with the behavior of the center frequency regarding a total variation of the process, voltage and temperature just like was made for the active inductor. Additionally, we shall make an statistical analysis in order to determine the reliability of the center frequency of the oscillator.

The results of the PVT analysis are reported in Table 3.3. As it can be observed, the minimum and maximum center frequency is 4.612 and 5.825 GHz, which represents a variation of -13.95 and 8.67 % respectively. It should be noted that these variations are relatively small considering the active nature of the whole circuit. The most critical operation corner is the N_F-P_S and temperature at -20 $°C$, because the input transconductor is pushed into the triode region causing a large increase of the inductance value and therefore a reduction in the oscillation frequency. However, we believe that the stability of the center frequency is good enough, which with the wide tuning range provide a large robustness against PVT variations, enabling the system to provide multi-standard support.

Similar to the center frequency, phase noise shows an stable behavior regarding PVT variations despite to fall down in some specific corners, particularly for N_F-P_F. These results allow us to think that the work made in this master project will have a good impact, showing that the active inductors are a good option to reach the multi-standard support without resort to strong increments for the area and power consumption. Lastly, it should be mentioned that as a result of the statistical analysis for the center frequency we got a mean value and standard deviation of 5.381 GHz and 411.03 MHz, respectively. The histogram for the center frequency of the whole oscillator is shown in Figure 3.8.

V_{DD}	Temp	N_S-P_S	N_S-P_F	PC Typ	N_F-P_S	N_F-P_F
0.9	-20°C	5.427 GHz 1.25% -106.46	5.275 GHz -1.58% -86.69	5.138 GHz -4.14% -100.43	4.612 GHz -13.95% -96.97	5.070 GHz -5.41% -76.13
	20°C	5.254 GHz -1.97% -98.79	5.296 GHz -1.19% -83.80	5.188 GHz -3.20% -92.50	4.660 GHz -13.05% -81.45	5.276 GHz -1.56% -81.57
	60°C	5.350 GHz -0.18% -98.79	5.443 GHz 1.54% -83.80	5.333 GHz -0.50% -82.54	5.013 GHz -6.47% -81.45	5.462 GHz 1.90% -80.93
	100°C	5.521 GHz 3.00% -85.30	5.569 GHz 3.89% -63.72	5.514 GHz 2.87% -82.64	5.471 GHz 2.07% -77.01	5.707 GHz 6.47% -80.93
1.0	-20°C	5.185 GHz -3.26% -107.17	5.055 GHz -5.69% -69.71	5.175 GHz -3.45% -91.71	4.570 GHz -14.73% -99.39	4.989 GHz -6.92% -66.69
	20°C	5.152 GHz -3.88% -92.59	5.160 GHz -3.73% -71.82	5.221 GHz -2.59% -92.55	4.693 GHz -12.44% -89.95	5.271 GHz -1.66% -69.91
	60°C	5.287 GHz -1.36% -82.73	5.367 GHz 0.13% -73.51	5.360 GHz 0% -88.04	4.949 GHz -7.66% -83.85	5.499 GHz 2.59% -72.60
	100°C	5.426 GHz 1.23% -82.39	5.534 GHz 3.24% -67.36	5.536 GHz 3.28% -77.79	5.292 GHz -1.26% -66.67	5.768 GHz 7.61% -71.84
1.1	-20°C	5.194 GHz -3.09% -105.16	4.792 GHz -10.59% -67.91	5.148 GHz -3.95% -77.95	4.827GHz -9.94% -91.68	4.834 GHz -9.81% -60.28
	20°C	5.175 GHz -3.45% -98.85	4.972 GHz -7.23% -70.27	5.237 GHz -2.29% -74.46	4.897 GHz -8.63% -88.28	5.227 GHz -2.48% -65.07
	60°C	5.308 GHz -0.97% -89.84	5.232 GHz -2.38% -60.46	5.390 GHz 0.55% -80.79	5.043 GHz -5.91% -86.70	5.524 GHz 3.05% -63.85
	100°C	5.430 GHz 1.30% -75.97	5.432 GHz 1.34% -69.15	5.567 GHz 3.86% -77.08	5.320 GHz -0.74% -82.61	5.825 GHz 8.67% -69.06

Table 3.3: Behavior of the phase noise and f_o of the VCO regarding PVT variations.

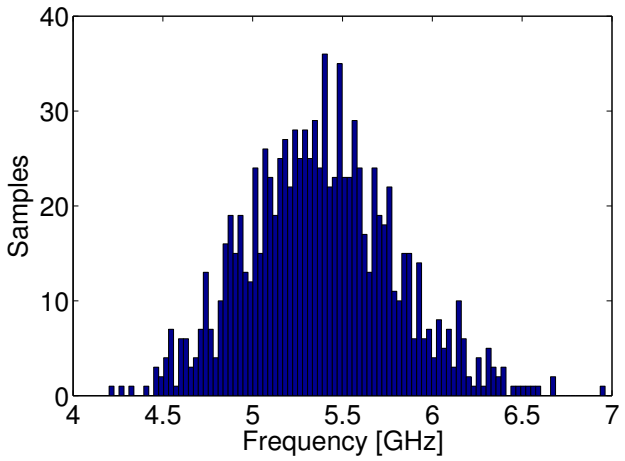


Figure 3.8: Histogram of the VCO center frequency.

Chapter 4

Conclusions

This work focused on trying to solve the tuning limitations of the passive LC-VCO without resorting to a large increment of area and power consumption like happens either by employing digitally switched capacitor and inductor arrays to achieve a programmable wideband local oscillator, or using several receivers on the chip sharing common blocks but with different signal path. The alternative used in this work to solve this problem is to use active inductors which provide high and tunable inductance and quality factors, large self-resonant frequency, low area and a high compatibility with digital CMOS technology. However, due to its high noise and sensitivity to the mismatch and PVT variations this sort of circuit is an untapped option in the industrial environment. The last of the previously mentioned points was our main motivation to develop this master project: to take advantage of the active inductor, but at the same time to obtain a circuit able to operate in the real world in a robust and reliable way.

Throughout this work, various analysis and proposals were made with the purpose to achieve the proposed aims. From the obtained results, some important conclusion were drawn and will be described next:

- It is not recommended to use grounded transconductors nor biasing them by means of reference voltages, since it causes a high sensitivity of the circuit performance with respect to PVT variations.

- A new topology of active inductor which takes efficiently advantage of the power used in its operation was proposed. This is mainly due to a couple of cross current mirrors, which reduce the inductance value at expense of a low increase in area and power consumption of the circuit. Besides, the current mirrors enable the circuit to

compensate partially the effect of the mismatch between the load transistors, and to reach an infinity quality factor at high frequency because of a double integration.

- A Gm-constant scheme based on a reference current, an active PTAT cell robust to process and voltage variations, and two circuits used to detect and compensate the process variations, the threshold sensor and the analog current switch, was proposed. This circuit along with the proposed active inductor allow implementing a robust inductance to PVT variations used to increase the limited dynamic range of the passive LC oscillator.

- An inductance range from 4.77 to 14.84 nH was achieved, yielding an Inductance Tuning Range (ITR) of 102.70 %.

- A variation of the traditional NMOS Cross-Coupled pair with current sinker was proposed. To change the grounded inductors by current sources and relocate the varactors inside the proposed floating inductor, provided better bias conditions to the active inductor than other typical structures. Besides, the new location of the varactors reduced the requirements of the PMOS transonductors, while the linearity of the VCO's tuning range was improved because of the smaller dynamic ranges inside the active inductos.

- A frequency band of 4.30 GHz was covered, from 3.2 to 7.50 GHz, allowing to use the designed VCO in a high performance system to provide multi-standard support.

The achieved goals with the development of this master project have a great merit, not only a novel active inductor was proposed, but also its functionality on a SOI CMOS technology was verified, while the effects of the PVT variations over its performance were compensated in order to obtain a robust and reliable circuit. Additionally, the active inductor was inserted in a proposed variation of the NMOS cross-couple pair with current sinker, looking for obtain a functional VCO to solve the problem of the limited tuning range of the passive LC VCO, which was achieved with great results.

4.1 Future Work

During the development of this project were made a large quantity of analysis and tests in order to achieve a successful design. However, some tasks still pending which should be made to complete the design flow. Among them, the most important in accordance with our consideration will be described next:

- To determine and tackle the sensitive points of the bias scheme regarding the mismatch, with the purpose to achieve a more reliable active inductor and therefore a VCO.
- To increase the dynamic ranges of the inductor using rail-to-rail techniques to improve its performance.
- To analyze the various noise sources of the circuit, and to include this specification in the design flow to improve the circuit performance.
- To study precise mirroring techniques that show low levels of noise.
- To drawn the layout of the circuit with the purpose to verify the validity of the results considering the parasitic elements associated to the fabrication process, and so to obtain a circuit ready for manufacturing.

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