Detection of Small-Delay Defects in Nanometer Technologies Using Inter-Path Correlation

By

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Summary

The aggressive scaling on integrated circuits technology, enable a dramatic increase on circuits performance by allowing higher clock frequencies, devices with larger memory capacity, lower power consumption and lower operation voltage. Nevertheless, the increase in circuits performance also creates complex circuits with higher density, which are liable to process variations and defects. As technology scales down, the number of transistors and interconnections grows at a very fast rate. For nano-scale technologies the growth rate of interconnections have overcome the one of transistors, generating circuits that are highly susceptible to opens and shorts defects. Most of the defects on a circuit creates small increases on delay performance, which may not create a functional failure, which makes them harder to be detected. However, even when this small deviations in delay does not create a failure, they represent a reliability and quality risk.

In this work a new approach to detect small-delay defects (SDD) under the presence of process variations will be presented. This methodology use the correlation information of the circuit outputs delay to establish a statistical reference frame that can be used to screen SDDs. A path-based statistical timing analysis will be implemented to obtain the correlation information between outputs delay of the circuit. This correlation between outputs delay, is analyzed to establish a reference frame of the relationship between circuit output’s delay. The outputs delay of the circuit under test are then compared with the reference frame. For a defect free circuit the relationship between outputs delay must agree with the reference frame, otherwise a defect is present in the circuit. The feasibility of this methodology is validated on benchmark circuits, where the promising results obtained shows that this methodology is
capable of improving the SDD detectability of a circuit.

The first chapter of this thesis presents a description of the fluctuations that affect nanometric technologies. The sources and behavior of process variations are described, making emphasis on their influence on delay performance. The state-of-the-art on delay testing is discussed, considering the main issues of process variations. At the end of first chapter, the concept of small-delay defects will be described, addressing topics like sources and their effects on delay performance, testability and reliability.

The second chapter of this thesis introduces the methodology to establish the statistical reference frame that can be used to screen small-delay defects. The process of detecting delay deviations is described in two stages. First, the analysis is made considering full correlation between outputs delay, then this approach is extended to consider lower correlation degrees and its effects on SDD detection resolution. A multiple correlation approach is proposed as an optimization showing its advantages and limitations.

In the third chapter the statistical-timing framework that estimate inter-path correlation is described. The beginning of this chapter describe the models used to characterize the behavior of parameter fluctuations in nano-meter technologies. This framework considers random and systematic variations; therefore, the state-of-the-art models that describe the spatial behavior of process variations will be analyzed. Also, the considerations of phenomenons like structural correlation will be described. At the end of the chapter, the procedure to estimate inter-path correlation will be presented in detail.

Chapter four presents simulation results of the inter-path correlation behavior and its effects on small-delay defect detection. The analysis is divided in two sections: first, the inter-path correlation is analyzed for different circuit and parameter’s conditions; then an analysis of the small-delay detection is implemented on benchmark circuits. Using the results of the analysis, a group of heuristic objectives and restrictions will be presented. These heuristics are implemented on the detection of paths suitable to be included in the analysis. The results are discussed at the end of this chapter, outlining the main considerations to implement this methodology.

Finally, chapter five presents the general conclusions and main contributions.
Resumen

El escalamiento agresivo de las tecnologías de fabricación de circuitos integrados, incrementa el desempeño de los circuitos al permitir el uso de frecuencias de reloj más altas, dispositivos con mayor capacidad de memoria y menor consumo de potencia. Conforme la tecnología se reduce el numero de interconexiones y transistores incrementa a un ritmo acelerado; para tecnologías nano-métricas el crecimiento de interconexiones ha sobrepasado al de los transistores, generando circuitos más susceptibles a defectos y variaciones. La mayoría de los defectos en un circuito, generan incrementos de retardo que son muy pequeños lo cual hace más difícil su detección. Sin embargo, aun cuando estos retardos pequeños no generan una falla funcional, si comprometen la confiabilidad y calidad del circuito.

En el presente trabajo se propone un nuevo enfoque para detectar defectos de retardo pequeño (SDD) bajo la presencia de variaciones de proceso. Esta metodología hace uso de la información de correlación que existe entre los retardos a las salidas de un circuito. Dicha información es utilizada para generar un marco de referencia que permita detectar SDDs. En este trabajo se ha implementado un análisis estadístico de tiempo basado en trayectorias, que permite obtener la información de correlación a las salidas del circuito. Dicha información es analizada para predecir el comportamiento de retardo en ciertas salidas del circuito. Los retardos en las salidas del circuito bajo prueba son comparadas con el marco de referencia establecido con anterioridad para detectar desviaciones en el desempeño de retardo. En un circuito sin defectos, la relación entre los retardos de la salidas debe concordar con con el marco de referencia; de no ser así, el circuito bajo prueba presenta un defecto. La validez de esta metodología fue comprobada en circuitos estándar, donde se obtuvieron resultados
promisorios en la detección de SDDs.

El primer capítulo de esta tesis describe las fluctuaciones de parámetros en tecnologías nano-métricas. Las fuentes y el comportamiento de las variaciones de proceso son descritas haciendo énfasis en su influencia sobre el desempeño de retardo. El estado del arte en lo referente a pruebas de retardo será descrito considerando el efecto de variaciones de proceso. Al final del capítulo, el concepto de SDD se describe analizando sus fuentes principales, la influencia en el retardo y los riesgos de confiabilidad que generan.

EL segundo capítulo presenta la metodología para establecer el marco de referencia usado en la detección de SDDs. El capítulo comienza describiendo los fundamentos estadísticos usados para detectar desviaciones en la correlación de retardo. El proceso de detección de desviaciones en el retardo se describe en dos etapas: Primero, se realiza un análisis considerando retardos de salida completamente correlacionados, después esta aproximación es extendida al considerar diferentes grados de correlación. También se propone el uso de un análisis de correlación múltiple como optimización, mostrando sus principales ventajas y limitaciones.

El tercer capítulo describe la herramienta de análisis estadístico de tiempo desarrollada para estimar la correlación entre trayectorias. Al inicio del capítulo se describen los modelos usados para caracterizar el comportamiento de las variaciones de proceso en tecnologías nano-métricas. La herramienta considera variaciones tanto sistemáticas como aleatorias en los principales parámetros del circuito. Se analiza el estado del arte en los modelos que describen el comportamiento espacial de las variaciones de proceso, así como los efectos de la correlación estructural en la estimación de correlación entre trayectorias.

El cuarto capítulo presenta resultados de simulación al implementar la metodología propuesta. Este capítulo está dividido dos partes: Primero, se presenta un análisis del comportamiento de la correlación entre trayectorias para un circuito bajo diferentes condiciones. Posteriormente la metodología se implementa en circuitos estándar, cuyos resultados son utilizados para proponer un grupo de objetivos y restricciones heurísticas que permiten seleccionar las trayectorias más útiles para la metodología. Los resultados se analizan en la parte final del capítulo.

Por último, el capítulo quinto presenta las conclusiones generales y contribuciones.
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List of Acronyms

AIGD ........ Average inter-gate distance
ASIC ........ Application-specific integrated circuit
ATPG .......... Automatic test pattern generator
BIDM ........ Built-in delay measurement
CD ............ Correlation distance
CMP ........... Chemical Mechanical planarization
CUT ........... Circuit under test
D2D ............ Die-to-die or inter-die variations
EM ............ Electromigration
FNT ............ Fan-in table
IC ............ Integrated circuit
LCRV ........ Linear combination of random variables
LER ............ Line-edge roughness
MMMC ........ Multi-mode and multi-corner analysis
MPU ........... Micro-processor unit
PCB ........ Printed circuit board
PGC ........ Path global correlation matrix
PUT ........ Paths under test
RDF ........ Random-dopant fluctuation
RDF-LT ...... Random-dopant fluctuation look-up table
RV .......... Random variable
SDD ........ Small-delay defect
SEM .......... Scanning electron microscope
SSTA ........ Statistical-static timing analysis
STA .......... Static timing analysis
VHDL ........ Verilog hardware description language
WID ........ Within-die or intra-die variations
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Chapter 1

Introduction

In the resent years, the specifications of components used in cutting-edge electronic systems has been continuously tightened to keep up with the demand of systems with higher performance. Integrated circuits (IC) are not excluded from this tendency, increasing their performance and reducing their cost of manufacturing. In order to keep up with the evolution of electronics systems, ICs have been subject to a continue and aggressive scaling on devices dimensions. This reduction allows manufacturing of cheaper circuits with higher performance. However, scaling also generates circuits with higher density and complexity that are highly susceptible to defects and thus to failures. Figure 1.1 shows the progressive increase in the number of transistors in micro-processors units (MPU) for the coming years.

Due to the increase in the number of transistors, the number of interconnections increase with the same or even higher rate. With higher interconnections density the risk of interconnection-related defects increase, due to the reduction of interconnections size and the distance between them. Moreover, the increase in circuits integration has surpassed the efficiency of IC manufacturing process control. This phenomenon has increased the variability of circuits performance due to random fluctuations on devices (transistors, interconnections, capacitors, inductors, etc.) operation parameters. The variability of devices parameters due to either defects or process fluctuations impacts the performance of the circuit in power consumption, signal integrity and delay.
The maximum operation frequency is one of the most important characteristics in the performance of a circuit, specially for digital circuits. The frequency of operation is closely related to the circuit maximum delay, which is one of the characteristics that are more sensitive to defects and process variations. In fact, delay defects at nano-scale technologies represents one of the biggest reasons of Yield\(^1\) loss. In particular a phenomenon known as small-delay defect (SDD) represents a reliability risk in nano-scale technologies.

This chapter will give a brief overview of the main phenomenons that affects the performance of nano-scale CMOS digital circuits, and the state-of-the-art in digital IC testing for delay defects. Section 1.1 presents an overview of the defects and failures that impact the performance of nano-scale designs. Section 1.2 presents the main sources and behavior of process variations in nano-metric technologies. Section 1.3 presents some of the most important delay testing techniques, showing the concepts of both the traditional and statistical approaches. Section 1.4 presents the description of the SDDs sources and the recent testing techniques used to address this phenomenon. Section 1.5 presents the justification of this work. And finally section 1.6 presents the organization of this thesis.

\(^1\)Yield represents the efficiency of an IC manufacturing process, considering the relationship between manufactured chips and functional chips [2]
1.1 Defects and Failures in Nano-Scale Technologies

For digital circuits, designed in technologies over the quarter of micron, the “side-effects” of scaling were negligible compared to the improvements in area consumption, power consumption and maximum operation frequency. Nevertheless, in nano-scale designs the effects of scaling creates severe variations of the manufactured devices [3, 4, 5, 6]. These fluctuations generates different kinds of deviations from the expected performance depending on their location, type and magnitude.

The deviations that occur in a circuit can be classified as defects, errors or failures. In order to state the differences between deviations the following definitions are given [7]:

- **Defect**: is any non-intentional random fluctuation in the circuit’s devices, which creates deviations between designed and implemented circuit specifications. These fluctuations may appear during the manufacturing process or in the life time of the circuit.

- **Error**: is a deviation on any of the devices parameters (current, threshold voltage, resistance, etc.), that may occur because of defects or environmental fluctuations. The most common environmental fluctuations are temperature variations, supply voltage variations, noise and interaction with other devices.

- **Failures**: is the abstract representation of the effects that an error or defect has over the circuit’s power consumption, operation frequency, signal integrity, etc.

The previous definitions imply that a failure is produced by the effects that an error or defect has over the behavior of a circuit. An error or a defect can produce two different kind of failures, depending on the effects that they have on the circuit behavior. If a failure force the circuit to become non-operational, it is known as a *catastrophic* failure. On the other hand, those failures that allows the circuit to be operational, but cause a deviation on the circuit’s performance regarding to the design specifications are known as *parametric* failures. Even when a parametric failure allows operational circuits, these are in fact defective circuits, and they should be discarded reducing the yield of the manufacturing process. In order to reduce the cost of integrated circuits, the industry has applied techniques to classify the performance
of a circuit and increase the yield by establishing tolerance gaps for each parameter (delay, power, gain, bandwidth, etc.) [8, 9].

The devices of any electrical circuit are connected to each other through metallic structures known as interconnection lines. Some of these interconnections are used to carry signal information and others have the task of distributing the power supply. As the density of ICs increase, the number of interconnections and vias become the predominant structures on the circuit. Therefore, the phenomenons that affect these structures had become an important source of defects. The failure mechanisms that affect these structures have always being present on CMOS technologies, but for nano-scale circuits and nowadays operational frequencies, these mechanisms had become more recurrent and severe. There are two main classes of failure mechanisms, short and open circuit defects, which will be briefly described next.

### 1.1.1 Open-Circuit Defects

An open-circuit defect (or just open-defect), can be described as any non-intentional broken interconnection line, contact or via. If the affected interconnection is completely broken and no signal can flow through the interconnection, like shown in Figure 1.2a, the defect is classified as a *full-open*. On the other hand, if the affected interconnection is not completely broken and signal still able to flow through the interconnection, like in Figure 1.2b, then the defect is classified as *resistive-open*.

![Figure 1.2: Two different kinds of open defects.](image-url)
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Most of the sources of open-defects appear during the manufacturing process, mainly due to [10, 11]:

- The presence of undesirable particles on the surface of wafer during the lithographic process.
- Deficient metal deposition.
- Erosion and dishing due to chemical mechanical planarization (CMP).
- Silicide agglomeration.
- Antenna effects, and others.

As technology is scaled, the probability of a circuit to be affected by an open has increased, specially for resistive opens. This increase is due to phenomenons like etching or slurry, which are very common in manufacturing process like damascene.

When an interconnection is affected by a full open defect, it result in a floating node at the input of a gate, as shown in Figure 1.3. As this node is not isolated from the rest of the circuit, this node will be driven by electric couplings with other interconnections or power supply lines [12, 13, 14]. As a result, the gate with floating input will present an erratic behavior at the output, depending on the fluctuations and the adjacent line’s switching activity [15, 16].

Figure 1.3: Floating node resulting from a full open and the electric coupling that may take control of that node.
As a result of a resistive-open, the resistance of an interconnection increases. Due to the increase in resistance, the characteristic impedance and propagation delay of the interconnection increases [17, 18, 19]. Hence, the increase in delay will be propagated through the gates to reach the primary outputs increasing the delay of the circuit. Depending on the magnitude of the open defect, the delay generated may create a logical failure or just reduce its maximum operation frequency. The value of defect resistance that will make the defect detectable is known as critical open resistance ($R_{CO}$), and depends on the defect location and affected line characteristics.

### 1.1.2 Short-Circuit Defects

A short circuit defect (usually known as short defect or bridge defect) is any non-intentional connection between two signal lines or between a signal line and a power supply line. In Figure 1.4 a short defect between two lines is shown. The interconnection line A is the line carrying the signal of the circuit under analysis, and the interconnection B is a line that may be either a signal line of another section of the circuit or a power supply line.

![Figure 1.4: Two interconnection lines connected by short defect.](image)

Similarly to open defects, short defects are generated mainly during the manufacturing process. The main causes for the appearance of short defects are [11]:

- Fluctuations in the lithographic process (lens aberration, optical proximity effects, etc.).
- Fluctuations during the metal deposition processes.
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- Contamination by conductive particles.
- Electromigration.
- Oxide and dielectric ruptures, and others.

The resistance of a defect depends on its shape and material properties. The effect of a short defect on the performance of a circuit depends on the resistive properties of the defect, its location and the driver of the affected line. Figure 1.5 show the electrical representation of a short defect. The current that flows through the driver is equal to the current that discharge the load ($I_{C_L}$) plus the current that flows trough the defect ($I_{R_{sh}}$). If the value of $R_{sh}$ is high enough, the current flowing trough the defect will be negligible and the driver will discharge its load. On the other hand, if the resistance of the defect is low enough, a non-negligible current will flow through the defect and the driver will not be able to discharge the load properly generating a failure on the circuit performance.

![Figure 1.5: Electric influence of a short defect in a circuit.](image)

When the resistance of a defect is high enough to not create a logical failure, the sort-defect is known as resistive-short. The value of resistance above which the circuit will not fail, is known as critical resistance ($R_{CS}$). The value of $R_{CS}$ for a certain location depends on each line driver’s resistance and load.
1.1.3 Susceptibility of Open and Short Defects to Degradation

As mentioned earlier, the critical resistance for opens and shorts-defects, represents a threshold where the effects of the defect can be neglected or not. The critical resistance of a certain defect depends on the location and characteristics of a line, but not on the characteristics of the defect. If the resistance of a resistive-short (resistive-open) is higher (lower) than the critical resistance for that location, then the defect will not be detected at the testing stages. On the other hand, if the resistance is lower (higher) than the critical resistance the defect will create a failure that can be detected during the testing.

For the case of metal structures on interconnections, opens and short-defects represent the main failure mechanism. The main sources of shorts and opens-defects are associated to process variations and contaminant particles. Nevertheless, another important source of defects is the movement of metal molecules due to the flow of electrons and high temperature. If the sufficient current and temperature is applied, the movement of molecules will change the metal structure, as a result of a phenomenon known as electromigration (EM) [11, 20, 21]. The movement of molecules due to electromigration creates voids and extrusions projected from one of the faces of an interconnection, increasing its resistance and the possibility of bridge with another structure [22].

Nowadays circuits operate at high frequencies and temperatures, which increase the effects of electromigration. The effect of electromigration on interconnections have a progressive nature and modifies its resistance. Therefore, defects like resistive-opens and resistive-shorts can be aggravated during the life time of a circuit [23, 24, 25]. This implies that a resistive defect (open or short) can present certain resistive characteristics that do not produce a failure during the testing stages. However, due to electromigration the resistive characteristic of a defect will change and may produce an early on field failure that reduce the circuit quality and reliability [26, 27]. The reliability risk that electromigration and resistive defects represents is one of the main motivation for this work as will be described in section 1.4.
1.2 Process Variations in Nano-Scale Technologies

As a result of the aggressive scaling on devices and interconnection dimensions, the IC manufacturing processes are working on the physical limits of materials and equipments. Therefore, the manufacturing process is far from being accurate and reliable. The fluctuations in the manufacturing process, represent variations on the parameters that define the behavior of a circuit, such as gate length (L), gate width (W), oxide thickness ($T_{ox}$), threshold voltage ($V_{th}$), interconnections geometry (thickness, width and roughness), isolator properties, etc.

The term process variations represents any fluctuation on the parameters of devices and interconnections in a manufactured circuit. These fluctuations are a result of many different factors during the manufacturing process. Large variations in process parameters will lead to large deviations from the designed specifications. The resulting distribution for performance across a large set of manufactured circuits is the reason for the definition of a new class of yield, known as the parametric yield. Parametric yield is the fraction of manufactured samples whose performance do not exactly match the specifications, but that meet the performance tolerance. The concept of parametric yield leads to the definition of timing yield [28], which represent the fraction of manufactured circuits that met the timing performance constrains.

The impact of process variations on performance has been increasing with each semiconductor technology generation. The magnitude of variations in gate length has increased from 35% in a 130nm technology to almost 60% in a 70nm technology [29]. This represent that, for a 70nm technology with variation in gate length of 60%, certain devices will have a gate length fluctuation of $\pm 42$nm. With variations like these, it becomes extremely important for design and testing of ICs to approach these variations in a statistical manner rather than using worst-case scenarios in deterministic analysis.

1.2.1 Sources of Process variations

Nowadays IC’s density has overcome the control systems of the manufacturing processes. The fluctuations in the manufacturing of ICs occur at practically every step of the process
and have many different causes. Nevertheless, the fluctuations that affect the performance of a circuit can be classified depending on their origin as environmental, electrical or physical variations.

1.2.1.1 Environmental Variations

These variations represent the fluctuations in the surrounding environment in which a circuit is operating. This includes temperature variations, and variations in power supply [17]. A reduced power supply lowers the drive strengths of the devices and degrades their performance. Similarly, an increased temperature results in a lower performance for devices and interconnections. Those variations are time-related as they depend on the operation of the circuit and the conditions of the environment. This kind of variations may occur during certain operation conditions that can be anticipated at the circuit design stage. Nevertheless, these variations are not treated statistically, since a circuit is not allowed to fail over its entire operational life-time. Therefore, current circuit designs implement techniques and constrains that focus on minimize the effects of environmental fluctuations.

1.2.1.2 Electrical Variations

Electrical variations, just like environmental, are time related-variations that depends on the circuit operation and the influence of surrounding devices. Due to the extremely high density of circuits and their high operation frequencies, the possibility of coupling between devices (crosstalk) has grown. In addition, the probability of simultaneous switching in current devices is high increasing the appearance of phenomenons like power-supply fluctuations (\(I - R\) drop and \(L\frac{di}{dt}\)).

1.2.1.3 Physical Variations

Contrary to electrical and environmental variations, physical variations have permanent effects on circuit’s performance. This kind of variations appears as differences between the physical parameters of a manufactured circuit and the parameters of design. Most of these
variations appear as result of deviations in the manufacturing processes of lithography, deposition, planarization (CMP) and doping implantation. These variations represents physical changes in the structure of a circuit, that will have a large influence on the electrical behavior of a circuit and are capable of producing errors and failures. The main sources of physical variations are:

1. **Lithography:**

   Variations in the lithographic process produce the majority of physical parameters fluctuations, specially on the geometrical parameters of devices and interconnections. The main reason for these fluctuations is the low values of lithographic aggressiveness ($k_1$), which is a metric of how “sharply” a pattern can be printed over a silicon wafer. The parameter $k_1$ can be computed as follows [30, 31]:

   $$k_1 = \frac{NA}{\lambda} CD$$  \hspace{1cm} (1.1)

   where $NA$ is the optical aperture of the lens in use, $\lambda$ is wavelength of the incident light and $CD$ is the critical dimension of the pattern to print (smallest pattern). Equation (1.1) implies that as technology shrinks, $CD$ will decrease and consequently $K_1$. This means that for smaller technologies the precision at which a pattern can be printed will be very low. This imprecisions results in several types of distortions due to proximity effects [32] such as line width variation, corner rounding, line-end shortening [31] and line-edge roughness [33]. Figure 1.6 shows the main variations due to lithographic effects.

   The variations in the geometric structure of devices and interconnections are capable of producing large deviations in the circuit’s performance. Unfortunately, the continuous scaling of technology only leads to larger variations due to lithographic deviations, which represents a challenge for designers in deep nano-scale technologies.

2. **Material Deposition and Planarization:**

   The damascene and dual-damascene process are two of most used IC manufacturing
1.2 Process Variations in Nano-Scale Technologies

Figure 1.6: Different defects due to proximity effects in the lithographic process.

techniques, due to its properties that allows the manufacturing of circuits with higher density. Nevertheless, these techniques require the use of metal deposition and pla-
narization procedures that are susceptible to deviations. During deposition, most of the variations are due to vias partial voiding [34]. During the planarization procedure, which is made usually with (CMP), phenomenons like dishing and erosion [35] are generated. These phenomenons are forms of local planarization where areas of the wafer polish faster than others. In dishing the metal is displaced out of the line; meanwhile in erosion, sections of oxide and lines are polished faster than others. The dishing and erosion phenomenons are shown in Figure 1.7.

![Figure 1.7: Side effects of using CMP as a planarization technique.](image)

The loss of material in metal structures due to CMP produces fluctuations on interconnections resistance and consequently on their delay performance. If the effects of erosion and dishing affects the oxide thickness of a device, this will produce variations on its threshold voltage.

3. **Dopants Implantation:**

The dopants implantation process is one of the most important steps in the manufacturing of ICs, but also due to the implantation technology the number of atoms implanted have a random behavior. As technology scales down the number of dopant atoms on devices structure is decreasing. For a 70nm (40nm of effective length) technology with a dopant density of $10^{18} \text{cm}^{-3}$, the number of dopants will be an average of 100 atoms. For such a small number of dopants, the fluctuations in the dopant implantation will produce large variations in $V_{\text{th}}$ of the transistors. This variability is known as *random*
1.2 Process Variations in Nano-Scale Technologies

dopant fluctuations (RDF) (or pure random variations). This phenomenon will be approached in detail on section 3.2.4.1.

The previous sources of variations may produce fluctuations on the electrical behavior of devices and interconnections. Most of these variations have a random behavior that can no longer be described with a deterministic value; rather, they have to be described with a probability distribution function. These variations can also be classified according with their behavior and the influence that they have on the circuit performance.

1.2.2 Influence Range of the Process Variations

In order to make a more accurate analysis, process variations are divided in two classes: inter-die variations (D2D) and intra-die variations (WID). The classification of the effects that a variation has on a circuit is made according to their influence range on a design.

1.2.2.1 Inter-Die Variations (D2D)

These variations have an almost constant effect for devices inside a die. This implies that the variation of certain parameter is constant across a die, and has a different value at others dies. Therefore, these variations have a range that includes variations from die-to-die, wafer-to-wafer, lot-to-lot and factory-to-factory. These variations on a die are represented by a single value and represents a shift on the mean of certain parameter. Henceforth, D2D variations on a certain parameter $P$ can be accounted as follows [29, 36, 37, 38]:

$$P = P_{nom} + \Delta P_{D2D}$$  \hspace{1cm} (1.2)

where $P_{nom}$ represents the nominal value of the parameter and $\Delta P_{D2D}$ is a zero mean random variable (RV) that represents the fluctuations of the parameter due to D2D variations. The variable $P_{D2D}$ has a single value for all the devices inside a die. This kind of variations can be easily captured by a simple corner analysis, as this analysis assumes a shift on the parameters of all the devices for each corner. However, when multiple parameters are con-
sidered simultaneously during the analysis, the *correlation* between those parameters must be considered.

### 1.2.2.2 Intra-Die Variations (WID)

These variations represent the differences in certain parameter value for each device across a die. This implies that each device in the die must have a different RV to represent its parameters deviation. Depending on the nature of the variations, WID variations can have an spatial behavior (i.e. variations due to the lithographic process, CMP, deposition, etc.) or they can have a random pattern across a die (i.e. ion implantation, line edge roughness LER, etc.). These differences between spatially correlated and spatially uncorrelated variables, leads to two classes of WID variations. Those variations that show a spatially correlated behavior are known as *systematic variations* and those that are spatially uncorrelated are known as *random variations* (pure random variations).

1. **Systematic Variations:**

   This kind of WID variations show a behavior that can be systematically modeled at any location of a die. These variations can be addressed by implementing a model that captures their behavior at any given location of die, assuming that the variations have a monotonic behavior that is a function of the distance between locations. This models will be described on section 3.2.3.

2. **Random Variations:**

   Although all variations are considered as random variables, the term random variation is conventionally used to addressed those variations that do not show any spatially correlated behavior. These variations are modeled as individual and independent RVs for each device on a circuit.
1.3 IC Testing Overview

The effects of WID in a parameter $P$ can be considered by modifying equation (1.2) as follows:

$$P = P_{nom} + \Delta P_{D2D} + \Delta P_{WID}(X_i, Y_i) + \Delta P_{rand,i}$$

(1.3)

where $P_{WID}$ represents the component of WID variations, $x_i$ and $y_i$ represents the location of the $i$-th device and $\Delta P_{rand,i}$ represents the component of variation due to the $i$-th random variation. The previous process variations classes can be summarized in Figure 1.8. With regard to the scope of this work, the process variations that will be considered are the physical variations.

![Figure 1.8: General classification of main sources of defects and errors.](image)

1.3 IC Testing Overview

The process variability and the existence of defects reduces the yield and reliability of a manufacturing process. In order to reduce the cost of manufacturing, the IC industry has invested a large amount of resources to minimize the yield loss and increase the reliability and quality of the circuits. The cost of testing stages is justified by being lower than the cost
due to a defective circuit that later will have to be replaced from a PCB. All the manufactured circuits are tested for failures in functionality, power and delay performance.

One of the main challenges at the testing stages is that once a circuit is fabricated, the only available points of testing are the input, output and power pins of the circuit. Therefore, most of the testing techniques focus on analyze and interpret the information at the pins of a circuit.

One of the first testing techniques that still in use for present circuits is the logic fault testing. This technique focus on finding the logical functionality of the circuit, if the circuit present a logical failure it means the existence of a defect. The most common technique is the stuck-at testing, where using a specific test vector at the primary inputs of a circuit, the logic state of an specific node can be propagated up to the primary outputs of the circuit. If the logic state propagated to the outputs agrees with the state expected for that specific testing vector, then that node is defect free. Otherwise, if the logical state at the outputs is incorrect, then a defect is present on that node. Since the beginning of the logic testing, great advances have been made on testing vector generation and on the systematical selection of the test nodes to maximize the fault coverage\footnote{The fault coverage is a metric that represents the percentage of defects that a testing technique can detect on a certain circuit.}.

Another testing approach is the measuring and analysis of quiescent-state (static state) current consumption of the circuit. The first technique with this approach is the IDDQ testing, which relies in the fact that defect free circuits will have no quiescent current consumption, contrary to those that are defective. Other techniques are modifications of this principle, like IDDQ signature which is based on generating a current consumption signature for a group of circuits with a set of input testing vectors, and look for differences between the current signatures. $\Delta_{\text{IDDQ}}$ is based on finding the differences in current consumption of a circuit when the defect is activated or not. IDDQ based techniques had a great boom on the 80’s and 90’s due to its fault coverage and simplicity, even when it had always been an expensive technique. However, for nano-metric circuits, the efficiency of IDDQ has been dramatically reduced by the increase in MOSFET leakage currents.
A novel approach of testing is detecting timing failures associated to defects at the outputs of a circuit. These techniques are known as delay testing techniques, and they rely on the fact that defects like opens and shorts increase the delay of a path in a circuit. These techniques use a timing reference to detect deviations in the delay performance that are associated to defects in certain nodes of the circuit. One of the main advantages of delay testing, is its capability of detecting defects that do not produce logical failures, which increase the fault coverage. Nevertheless, the efficiency of delay testing has being affected by process variations. For highly fluctuating processes the delay behavior of a path is no longer deterministic, rather it has random behavior that complicates the implementation of delay testing as will be shown later on this chapter. Due to the scope of this work the delay testing will be treated with more detail.

1.3.1 Delay Testing

This approach has shown advantages over other techniques like logical testing or IDDQ testing. Nevertheless, as technology scales down and process variations become more significant, the implementation of delay testing has been modified to account for the effects of process variations. Therefore, delay testing is currently implemented following two approaches, one deterministic where the effects of process variations are minimized or neglected and a novel approach where process variations are considered and modeled statistically. The two main approaches of delay testing will be described next.

1.3.1.1 Traditional Delay Testing

In the early years of delay testing, the effects of process variations were not as critical as they are in nano-scale technologies. Therefore, most of the current delay testing techniques are based on a deterministic approach, also known as static-timing-analysis (STA). There are three main models to implement delay testing that can be considered: transition delay model, gate delay model and path delay model. These models and their characteristics will be discussed next.
1. **Transition Fault Model:**

This model assumes that defects affect the delay of only one gate in the circuit. There are two transition faults associated with each gate: a rise edge and fall edge. In a defect-free circuit, each gate has some nominal delay; nevertheless the existence of a defect produce an increase of the gate delay. Under the transition fault model, the extra delay caused by the defect is assumed to be large enough to prevent the transition from reaching any primary output at the time of observation. This model is also referred to as the gross-delay model.

The transition fault model is implemented with a set of two test vectors \( \{V_s, V_t\} \). The first vector, set-up vector \( V_s \), is a vector that sensitizes the circuit so the logical value of the node under test can be propagated to any of the primary outputs. Once the circuit is sensitized, the second vector, testing vector \( V_t \), activates the node under test and propagate its logic value to a primary output. If the logical value of the node under test is not propagated on the observation time, then a defect is affecting that particular node. The sets of testing vectors can be vectors generated by a stuck-at testing vector generator. Figure 1.9b shows the waveform for the circuit under analysis of Figure 1.9a.

For the circuit in Figure 1.9a, the logical values in blue color represent the logical values at each node after \( V_s \) and the red values represents the propagated values after \( V_t \). The waveforms in Figure 1.9b shows the propagated transition at the primary output. If the node under test is defect free, the propagated signal on \( O_2 \) will be the one in green color. On the other hand, if the node is defective the propagated transition will be the one in red color.

The main advantage of transition fault model is that the number of possible defects is linear with the number of gates. Also, the test vectors generation tools that are used for logic testing can be used to generate the test vectors in transition fault model. On the other hand, the assumption that the defect affects only one gate is too optimistic. Another disadvantage is the assumption that the defect will produce a large delay that
1.3 IC Testing Overview

Figure 1.9: Example of transitional model delay testing.

The gate-delay fault model assumes that the delay fault is lumped at one gate in the circuit. However, unlike the transitional model, the gate-delay model does not assume that the increased delay will affect the performance of the circuit independently of the
defect propagation path. It is assumed that only long paths through the fault site might cause performance degradation, and that defects in shorter paths must be propagated through longest paths. To determine the ability of a test to detect a gate-delay defect, it is necessary to specify the delay size of the fault. The limitations of the gate-delay fault model are similar to those for the transition fault model. Because of the single gate-delay fault assumption, a test may fail to detect delay faults that are a result of the sum of several small delay defects. The main advantage of this model is that the number of faults is linear in the number of gates in the circuit.

3. **Path-Delay Fault Model:**

This model compares the delay of a path with a certain timing reference, if the path delay exceeds a certain limit the circuit is considered as defective. Each path is defined as a pair of primary input and output that are linked by a chain of gates. The delay of the path can be observed by propagating a transition from the input of the path and observing the total propagation delay at the output. Figure 1.10 shows the concept of path-delay testing on a circuit under test (CUT).

![Figure 1.10](image-url)  
*Figure 1.10: CUT that will be used to show the implementation of a path-delay test.*

As can be observed in Figure 1.10, the transitional signal applied to the input of the path under test is propagated across each of the gates that are involved in the path. Each gate propagates the signal according to its logical function and its propagation delay. The sum of each gate’s propagation delay will be used as timing reference to compare it with the actual behavior of the path. Figure 1.11 shows the two possible
results of implementing a path delay test.

If the propagated delay of the path is smaller than the timing reference of the path (green waveform in Figure 1.11), then the circuit is considered as a defect free. On the other hand, if the actual propagation delay of the path is larger than the timing reference (red wave in Figure 1.11), then a defect is present somewhere in the path.

![Figure 1.11: Possible waveforms that can occur during the implementation of a path-delay test.](image)

The main advantage of path-delay model is the ability to detect distributed small delays along the path. On the other hand, the main disadvantage is the complexity of testing the appropriate number of paths without increasing the cost of the testing.

### 1.3.1.2 The Statistical Approach

With the progressive scaling, the IC process variability and susceptibility to defects has an increasing tendency. This variability produce circuits with a fluctuating delay performance. Therefore, the use of a deterministic approach is not suitable for state-of-the-art technologies due to the variability of gates and paths delays. In order to address this issue, the STA is extended to statistically account for random variations, this analysis is known as statistical-static-timing-analysis (SSTA). This kind of analysis is used in this work and will be treated in more detail in chapter 3, but for now the basic characteristics will be explained.

The delay performance of each gate is represented as a function of random variables and described with a probability distribution function (PDF). The delay performance as well as the random variables involved are represented as a Gaussian distribution $N(\mu, \sigma)$. In order
to maintain an acceptable yield, the circuits whose maximum delay do not exceed a certain timing reference, usually $\mu + 3\sigma$, are considered as functional circuits. Figure 1.12 represents a delay distribution for a given circuit, and the reference that is used to classify a circuit as defective or non-defective.

![Graph showing delay distribution and timing reference](image)

Figure 1.12: Typical delay distribution and the timing reference considered as threshold for defective and non-defective circuits.

In an statistical analysis the delay of each path and gate are represented with a delay probability distribution. The delay distribution of a circuit depends of the maximum path delay distribution. Similarly, the delay distribution of each path depends on the delay distribution of the gates associated to each path. The gate delay distributions can be represented as pin-to-pin delay like shown in Figure 1.13. where each $i$-th pin-to-pin delay is represented as a probability distribution $N_i(\mu_{Di}, \sigma_{Di})$ that represents the propagation delay from the $i$-th input pin to the gate output pin. Once each gate delay distri-
1.3 IC Testing Overview

bution is determined, the signals at the primary inputs of the circuit can be propagated to the primary outputs using two methods:

1. **Path-based**: in this method a group of paths are selected to perform the analysis. This paths are selected according with their probability of being critical [45]. For the selected paths, the total delay distribution is computed by adding the delay distribution of each gate of the path. The circuit total delay distribution is then computed as the maximum distribution using the statistical operator MAX. The SUM statistical operator will be described in detail in chapter 3, meanwhile the operator MAX is described [46]. One of the advantages of the path-based approach is the minimal use of the statistical operator MAX, which is a much more complex operation than the operator SUM. On the other hand, the main disadvantage is that the efficiency of this approach is highly dependent on the critical path selection.

2. **Block-based**: this propagation method is based on the sectioning of the circuit by logic levels, from the primary inputs to the primary outputs. Each of these levels is considered as a sub-circuit with primary inputs and primary outputs. The propagation of delay distributions, just as in the path-base approach, is made using the statistical operators MAX and SUM. The path-based and block-based approaches differ in the manner that the operators are used. In a block-based approach, the arriving time at the input pin of a sub-circuit’s gate is added to the respective pin-to-pin delay and propagated to the output, this is made using the SUM operator. Once each the arrival time had been propagated to the output of the gate, the operator MAX between all propagated arrival times is used to obtain the total delay distribution at the output of the gate. The previous procedure is implemented for each of the gates in the current sub-circuit. The delay distributions at the outputs of each gate is considered as arrival time at the connected primary input of the next sub-circuit (logic level), all the arrival times are propagated to the primary outputs with the procedure mentioned earlier. The previous process continues until the arrival times of the complete circuit are propagated from the primary inputs until the primary outputs. Finally all the delay distributions at
the primary outputs of a circuit are analyzed with the operator MAX to calculate the maximal total delay distribution of the circuit.

The main advantage of the block based approach is that all the nodes in the circuit are analyzed, which increase the fault coverage of the technique. The computational complexity of this approach is lower than the one of the path-based approach, as the circuit under test is always a small segment of the total circuit. Moreover, the computational complexity of a block-based approach increase linearly with the number of logic levels in a circuit. Another advantage is that all paths in the circuit are propagated at the same time.

The main disadvantages of the block-based approach are related with the use of the operator MAX. The operator MAX introduces second order phenomenons on the maximum distribution like skewness and kurtosis [47], which affect the accuracy of the distribution propagation and calculation. The MAX operator is highly dependent of correlation between the distributions under analysis. This means that phenomenons like spatial correlation must be precisely modeled.

As can be observed, statistical delay testing is a great alternative to deal with the continuous increase in variability for recent and future technologies. Nevertheless, this approach is relatively new and a lot of work must be made before SSTA techniques can replace the STA approaches.

1.4 Small-Delay Defects

One of the main challenges of the nano-scale technologies testing is the growing number of defects that create an small deviation in delay performance. Most of the defects produce small delays [48], that are hard to detect as they are masked by critical path delay and process variations. This kind of defects are known as small-delay defects (SDDs) [49, 50, 51, 52, 53]. Although, SDDs may not create functional failures, their presence on circuits represents a reliability risk, as they point out the existence of defects that can be subject to degradation by
1.4 Small-Delay Defects

electromigration and aging [11, 20, 21, 54].

From an static point of view, an SDD is described as a defect that creates a delay increase short enough do not overpassing a certain timing reference. This timing reference, usually referred as timing slack, is used to guarantee the correct logic behavior of the circuit. The timing slack is established considering the setup-time and hold-time for each path. The SDD phenomenon becomes critical for shorter paths because they have larger slacks that may mask the effect of an SDD. On the other hand, in long paths with shorter timing slack the effect of an SDD is easier to detect as they will produce a logical failure. Figure 1.14 shows the static concept of an SDD and the impact in short and long paths.

In Figure 1.14 three paths of a hypothetical circuit are shown. Path 1 is a long path with a very small timing slack ($T_{slk}$), path 2 is a median path that has a medium timing slack ($T_{slk,2}$) and path 3 is a short path with large timing slack ($T_{slk,3}$). Assuming that path 1 is the longest path of the circuit, the total timing slack of the circuit is equal to the timing slack of path 1. In the circuit of Figure 1.14a, three signals are propagated trough paths 1 to 3. The waveforms shown in Figure 1.14b represent each signal at the end of each path for a certain CLK cycle. As can be observed, any increase in propagation delay of path 1 will violate the circuit timing slack. On the other hand, if a delay defect is present in path 3, the propagated signal through path 3 will have an additional delay; if the delay increase due to the defect is large enough the path 3 will violate the timing slack of the circuit; on the contrary, if the delay produced by the defect is small enough, path 3 will keep the timing slack becoming undetectable for common delay testing techniques. This is the condition known as small-delay defect.

When process variations are considered, the point of view of SDDs change. The consideration of process variations implies that the propagated delay is no longer deterministic; therefore, the delay of each path and the circuit’s timing slack will have a random behavior. Under the presence of process variations, a defect on a path will shift the delay distribution of the affected path. The shifting amount depends on the effects that the defect has on the path performance. If the delay introduced by the defect is large, the delay distribution will be shifted by a large amount; on the other hand, if the effects on delay performance are week, the delay distribution will be lightly shifted. Figure 1.15 represents the delay distribution of a
Chapter 1: Introduction

(a) Hypothetical CUT use to show the concept of small-delay defect.

Figure 1.14: Representation of the deterministic concept of an SDD.

(certain path when it is defect-free, when it is affected by a defect that produce an small delay and when it is affected by a defect that produce a large delay.

1.4.1 State of the Art in SDD Testing

Since SSTA testing is a relatively novel approach, most of the works that address the problematic of SDD testing, implement a deterministic approach. Common STA delay testing techniques like transitional [53, 55] and functional [56] tests, have a great performance at detecting large delays. Nevertheless, using these techniques SDDs may only be detected when
they are present on paths with small timing slack, that is why most of the efforts with this kind of techniques focus on generate test patterns that screen SDDs through critical paths [49, 52]. Several proposals have been presented to optimize the test pattern generation techniques [57, 58]. For instance in [59] the authors propose the use of output deviation probability as a criteria to select the optimal paths for SDD screening. The main disadvantage of these test-pattern based methodologies, is that they require the use of advance and complex pattern generation tools. Furthermore, most of these techniques neglects the effects of process variations.

Other approaches focus on stimulate the effects of SDDs to make them more notorious. In [60, 61], the authors propose the use of faster-than-at-speed clock frequencies to increase the effects of SDDs on path delay to the point where they can be detected. Similarly, Qian et al [62] propose a technique similar to very-low-voltage testing (VLV testing) to increase the delay of the paths affected by SDDs, according to the principle that resistive opens/shorts increases its effects on path delay for lower $V_{DD}/V_{th}$ ratios [63]. Nevertheless, the implementation of these techniques increases the complexity of testing and neglects the effects of process variations.

In [64] the authors propose the use of pulse propagation characteristics and on-line test structures to screen SDDs on non-critical paths, but this methodology require the implemen-
tation of pulse detection devices and the propagated signal characteristics are highly sensitive to process variations. In summary, most of the recent SDDs testing techniques focus on optimal test pattern generation, despite the increase in testing complexity. Moreover, the majority of these methodologies minimize the effects of process variations reducing their effectiveness.

Recent works like the one by Tayade et al [50] includes the effects of process variations during test pattern generation of a transitional test, targeting those paths with the smallest variance. This approach focus on generating testing vectors that screen SDDs under the effects of process variations. The main problem with this approach and with all of those that are based on generating testing vectors to screen SDDs, is the fact that SDDs on short paths will be very hard to test as they usually have large timing slacks.

A different approach that consider process variations and test paths independently of their timing slack is the one proposed in [65]. In this work and in the following improvements [66, 67], the authors propose the comparison between delays of two dies that were fabricated next to each other. This approach relies in the fact that these two dies will be affected almost by the same process variations. Therefore, if two non-defective dies are compared, their delay performance will be similar; but if one of them is defective they will have different delay performance. This approach allows the detection of delay defects independently of the circuit’s timing slack and also allows to distinguish between delay fluctuations due to process variations and those fluctuations generated by the presence of a defect. Nevertheless, this approach relies in the fact that two adjacent dies will have a very similar behavior, which implies that the majority of the process variations are D2D variations minimizing the effects of WID variations. The minimization of WID variations, will reduce the efficiency of this approach for future technologies, where the WID variations will conform the majority of process variations.

1.5 Justification of the Present Work

The aggressive and constant scaling of IC manufacturing technology will lead to extremely variable circuits, which will be highly susceptible to small-delay defects that reduces the
quality and reliability of circuits. The increase in process variability and appearance of small-delay defects will demand the implementation of testing techniques that allows the detection of small-delay defects under the effects of process variations, without increasing the circuit’s overhead and power consumption.

This work introduce a new approach to detect small-delay defects under process variations for critical and non-critical paths independently of the path timing slack, using a barely explored phenomenon known as *inter-path correlation* [68]. This methodology only requires the output delay information for at least two paths, and the delay inter-path correlation between them. Once the output delay information of each path is known, the relationship between them must agree with the inter-path correlation. Otherwise a defect is present in one of the paths. This testing methodology screens SDDs under process variations without increasing test pattern complexity, overhead or power consumption.

### 1.6 Organization of this Thesis

The rest of this thesis is organized as follows: chapter 2 presents the methodology for detection of small delay defects using only the outputs relationship information. Chapter 3 introduces the SSTA framework developed to estimate the inter-path correlation needed to implement the methodology proposed. In chapter 4, the SSTA framework is used to show the behavior of inter-path correlation and validate the models used on this work using a group of benchmark circuits. Finally chapter 5 presents the final conclusions of this thesis.
Chapter 2

Methodology to detect Small-Delay Defects Using Inter-Path Correlation

This chapter describes a novel methodology to detect small-delay defects using the delay correlation information between the outputs of a certain circuit. This methodology is based on an statistical approximation of the delay distribution in two or more outputs of a circuit. Once the delay correlation between the outputs of a circuit is known, this methodology allows the establishment of a reference framework to differentiate SDDs fluctuations due to process variations. This chapter is structured as follows: section 2.1 presents an overview of the delay correlation between paths and the use of this information to detect defects in a circuit. Section 2.2 presents a brief overview of the proposed methodology. Section 2.3 presents the statistical concept of correlation used in this methodology. Section 2.4 shows how the correlation information is used to analyze unexpected deviations between two variables. Section 2.5 presents a methodology to detect SDDs using delay correlation information. Section 2.6 presents the use of multiple correlation to further improves SDD detection. Section 2.7 presents different alternatives to acquire the delay measurements needed to implement this methodology. Finally a brief summary of the chapter is given in section 2.8.
2.1 Introduction

The fact that nano-scale technologies are highly susceptible to process variations, motivates the increasing interest in the use of SSTA analysis to describe the performance of a circuit. This tendency has produced great improvements on SSTA tools like the ones proposed by Kang et al [69, 70] or the one by Agrawal et al [71]. Most of the SSTA tools consider correlation between devices as a phenomenon that must be accounted in order to have an accurate delay estimation. Nevertheless, very few literature can be found about the use of correlation to improve the circuit’s design and/or testing. Huisman [68] has made a brief analysis of the use of correlation between paths in the prediction of delay performance. On the other hand, most of the literature on SDDs detection use a deterministic approach, or use a statistical analysis to generate optimized test vectors [45, 50] considering process variations. Therefore, the use of correlation information for circuit testing is a barely explored field that has the potential to increase the reliability of circuits as will be shown in this chapter.

2.2 Methodology Overview

This work proposes the use of the delay correlation information between paths associated to the outputs of a circuit, to detect deviations between the behavior of the circuit’s outputs delay performance. This is based in the fact that, if the delay correlation between the two paths is known, it must remain for a defect free-die. If one of the paths is affected by a delay defect, the correlation between paths will change and the delay defect could be detected. To compute the correlation between paths of a circuit, each path is associated with a primary output, and their delay distribution will be analyzed.

The delay correlation between two paths in a circuit, is known as *inter-path correlation*. The term inter-path correlation represents the degree of relationship that exist between delay variances of two paths. The relationship between two delay measurements, each from different path, must agree with the relationship indicated by the inter-path correlation. In other words, all samples at the output of two paths must agree with the inter-path correlation coef-
Chapter 2: Methodology to detect Small-Delay Defects Using Inter-Path Correlation

ficient; otherwise, a defect is present in one or both of the paths. This correlation deviation principle, represents a simple delay detection technique capable of screening very small delays defects in any path of the circuit. The flowchart of Figure 2.1, represents the process of this methodology to detect SDDs using inter-path correlation deviation.

From the netlist of the paths under test, capacitive loads and interconnection information is extracted. Using paths information and pre-characterized technology information (parameters variations, gates delay sensitivities and nominal delays), each path delay distribution and inter-path correlation can be estimated. Once inter-path correlation is known, the delay samples of the paths are analyzed to check for correlation deviations. Two paths will be considered as defect free if the samples value agree with the relationship predicted by inter-path correlation, otherwise one or both paths are affected by a defect.

Figure 2.1: Small-delay defect detection methodology using inter-path correlation.
2.3 Correlation Background

Random variables are usually described with a probability distribution. The relationship between probability distributions, is described as the degree of how pairs of variables samples deviate together from the nominal value, this characteristic is known as covariance. The covariance between two sets of data can be computed with equation (2.1).

\[
COV(X, Y) = \sigma_{XY} = \sum_{i=1}^{n} \frac{(\mu_X - X_i)(\mu_Y - Y_i)}{n-1}
\] (2.1)

where \( \mu_X \) and \( \mu_Y \) are the mean of data sets \( X \) and \( Y \), respectively. The values \( X_i \) and \( Y_i \) are the \( i \)-th data of sets \( X \) and \( Y \), respectively. As can be observed, equation (2.1) requires a high number of samples of both data sets \( X_i \) and \( Y_i \), which is not always available. In order to simplify the analysis of covariance, it is represented as a dimensionless coefficient known as correlation coefficient \( (\rho) \) which is a numeric value between \(-1\) and \(1\). The correlation coefficient between two variables \( X \) and \( Y \), can be computed as follows

\[
\rho_{XY} = \frac{COV(X, Y)}{\sigma_X\sigma_Y}
\] (2.2)

The easiest way to visualize the correlation between two data sets is the use of an scatter-plot. In Figure 2.2, the scatterplot of two zero mean random variables with unity variance is shown for different degrees of correlation. As can be observed, when two normal variables are highly correlated, the relationship between the two variables achieves a linear behavior. On the contrary, for lower degrees of correlation, no clear behavior of the pattern can be identified.

2.3.1 Third and Forth central moments Phenomenons

The variables used in Figure 2.2 are normally distributed and only first and second central moments [47] are considered. Even when the assumption of normality is a common and valid approximation [47, 72, 73], such assumption is not always truth and the effects of violating...
this considerations has to be accounted. When a correlation study is performed, three basic assumptions have to be fulfilled, normality, linearity and homoscedascity. These three
assumptions are closely related but distinguishing between them is very useful for a correct analysis.

1. **Normality**

   A correlation is said to be *normal* when both variables in the bivariate distribution are normally distributed. For this assumption to be fulfilled, both normally distributed variables must not be skewed in either positive or negative way, and also, no kurtosis must be present [73].

   If any of the variables presents any degree of skewness, the approximation of correlation by a straight line will no longer be valid. The main reason why skewness reduce the accuracy of a straight line approximation, is because the bivariate distribution will not have a linear relationship as can be observed in Figure 2.3.

   ![Figure 2.3: Deviation from linear approximation due to skewness.](image)

   Kurtosis which is a measure of how “flatten” is a distribution (mainly on the tails), can also create a non-linear correlation and therefore reduce the accuracy of the approximation. The effects of kurtosis can be represented as in figure 2.4.

2. **Linearity**

   Approximating correlation by a straight line, is based on the assumption of full correlation. Conditions like full correlation only happen when the relationship between
two random variables is linear. The main reasons for non-linearity, is the lack of normality in the bivariate distribution or the presence of a non-linear relationship between variables.

So far, the technique presented in this work, does not account for non-linear relationships due to non-normality or non-linear relationships. Nevertheless, some techniques like weighted least square regression [73] and quadratic regressions [74, 75], allow the possibility to estimate non-linear relationships.

3. **Homoscedascity**

Homoscedascity is a property of correlation that accounts for the uniformity of the relationship between variables [73]. Homoscedascity can be explained as the degree of homogeneity in the bivariate distribution. Low homoscedascity occurs when a correlation between variables is non uniform over the bivariate distribution. This can be observed in Figure 2.5 as a dispersion with a fan shape, which indicates a progressive reduction in correlation.

Regarding to this work, all random variables in process variations and delay performance are considered normally distributed. Nevertheless, this methodology can be extended to consider non-linear phenomenons with the inclusion of a higher order model. However, the use
of these models will increase radically the complexity of the analysis, creating a compromise between accuracy and complexity of the methodology.

2.4 Correlation Deviations Between Variables

The proposed methodology is based in identifying when the delay of a path suffers a change, due to the presence of a defect, regarding to the performance of another path. To implement this concept, the correlation information between paths will be used as a reference to identify these changes. Therefore, it is necessary to create a reference frame that detect deviations in the correlation between paths.

2.4.1 Full Correlation Approach

When two variables have a medium to high correlation ($\rho > \pm 0.5$), the relationship between both paths distribution acquire a “semi-linear” behavior [72]. Based on the assumption of normality, an straight line can approximate the covariance between two fully correlated distribution. This approximation can be made by a linear regression analysis; nevertheless, a linear regression analysis is not suitable for delay testing as it requires the use of a large amount of delay samples. Nevertheless, a similar approximation can be achieved using the statistical information of each delay distribution ($\mu_D$ and $\sigma_D$). In order to make this approxi-
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...mation, at least two points on the approximation line are needed. Using the characteristics of each random variable, three characteristic points can be found. Figure 2.6 shows the graphical representation of each characteristic point and the relationship with the approximation line for the covariance between two random variables $S_1$ and $S_2$.

![Figure 2.6: Graphical representation of the linear approximation that can represent the covariance behavior of two normal distributions.](image)

In Figure 2.6 the point $\textcircled{1}$ is determined by the intersection between the means of both random variables. The point $\textcircled{2}$ is the intersection of values $\mu_{S_1} + 3\sigma_{S_1}$ and $\mu_{S_2} + 3\sigma_{S_2}$, and the point $\textcircled{3}$ is the intersection of $\mu_{S_1} - 3\sigma_{S_1}$ and $\mu_{S_2} - 3\sigma_{S_2}$. The approximation line formed by $\textcircled{1}$, $\textcircled{2}$ and $\textcircled{3}$ is described by a common line equation as follows

$$S_1 = m \ast S_2 + b$$  \hspace{1cm} (2.3)

where $m$ is the slope of the line, and $b$ is the abscissa intersection. The equation (2.4) calculates $m$ using two points on the line $\textcircled{2}$ and $\textcircled{3}$ substituting the values of these two points as follows

$$m = \frac{(\mu_{S_2} + 3\sigma_{S_2}) - (\mu_{S_2} - 3\sigma_{S_2})}{(\mu_{S_1} + 3\sigma_{S_1}) - (\mu_{S_1} - 3\sigma_{S_1})} = \frac{\sigma_{S_2}}{\sigma_{S_1}}$$  \hspace{1cm} (2.4)
where $\mu_{S_j}$ and $\sigma_{S_j}$ are the mean and variance of the $j$-th variable. In order to simplify the analysis of equation (2.3), both variables can be standardized (zero mean and unity variance) by with the following equation

$$S'_{ji} = \frac{S_{ji} - \mu_{S_j}}{\sigma_{S_j}}$$  \hspace{1cm} (2.5)

where $S'_{ji}$ represents the standardized $i$-th sample of variable $S_j$. The use of standardized variables, implies that they have a unity standard deviation ($\sigma'$). Under this consideration, the equation (2.4) is simplified to the unit. Using standardized variables, the approximation line will be shifted to the origin and can be represented with the following approximation equation

$$\frac{(S_{2,i} - \mu_{S_2})}{\sigma_{S_2}} = \frac{(S_{1,i} - \mu_{S_1})}{\sigma_{S_1}} \times m$$  \hspace{1cm} (2.6)

$$\therefore m = \frac{(S_{2,i} - \mu_{S_2})}{(S_{1,i} - \mu_{S_1})} \times \frac{\sigma_{S_1}}{\sigma_{S_2}}$$  \hspace{1cm} (2.7)

where $S_{ji}$ represents the $i$-th sample of the $j$-th variable and $\mu_{S_j}$ is the mean of the $j$-th variable. Using (2.4) with standardized variance, equation (2.7) can be re-written as in (2.8) to represent the relationship between $S_1$ and $S_2$ with full correlation and standardized properties.

Under the assumption of full correlation, any two standardized delay samples of $S_1$ and $S_2$ must fulfill equation (2.8). Otherwise, one of the samples does not agree with the correlation between variables.

$$\frac{S_{2,i} - \mu_{S_2}}{S_{1,i} - \mu_{S_1}} = \frac{\sigma'_{S_2}}{\sigma'_{S_1}}$$

$$\frac{S_{2,i} - \mu_{S_2}}{S_{1,i} - \mu_{S_1}} = 1$$  \hspace{1cm} (2.8)

### 2.4.2 Non-Full Correlation Approach

The existence of fully correlated variables is an extremely rare condition; therefore a full correlation based methodology is impractical and must be modified to consider non-fully correlated variables. When two RVs are non-fully correlated, the approximation line that describe the behavior of covariance will not be accurate any more, due to the variability of
the bivariate distribution. This can be observed in a scatterplot as a dispersion of the values around the approximation line. Figure 2.7 shows scatter plots for two highly correlated and two poorly correlated variables.

![Scatter plots for correlated variables](image)

Figure 2.7: (a) two correlated variables with high correlation coefficient and (b) with low correlation coefficient, using 1000 samples

A very important difference between a fully correlated relationship and a non-fully correlated one is the *predictivity* of the relationship on each case. Predictivity means how accurately the value of one variable can be estimated based on the value of the other. When a full correlation is present, the prediction is exact, but with a lower correlation the accuracy of the estimation decreases.

Predictivity between two variables can be explained by considering one of the most basic...
interpretations of correlation, the squared correlation coefficient ($\rho^2$). This form of correlation coefficient represents part of variance in one variable that can be described by the variance of the other, and vice versa [72, 76]. For instance, consider that for two variables $A$ and $B$ with $\rho = 0.8$, coefficient $\rho^2 = 0.64$ means that 64$\%$ of the variance in one variable is associated with the variance in the other. In other words, 64$\%$ of the variance of one variable can be attributed to the variance in the other, but there stills 36$\%$ that can not be described. The total variance of one variable can be represented as the sum of the variation associated to the other variable and the variation that can not be described, this can be considered as predictivity error. Figure 2.8 shows a Venn diagram that can graphically represent $\rho^2$. In Figure 2.8, the variance of variable $A$ can be described in terms of the predictable variance ($\sigma^2_{P_{AB}}$) between $A$ and $B$ as follows:

$$\sigma^2_A = \sigma^2_{P_{AB}} + \sigma^2_{e_{AB}}$$  \hspace{1cm} (2.9)$$

where $\sigma^2_{e_{AB}}$ represents the variance of $A$ that is not associated with the variance of $B$ and that represents the error of describing the variance of $A$ with the variance of $B$. The term $\sigma^2_{P_{AB}}$ can be represented in Figure 2.8 as $\{B \in A\}$; meanwhile, $\sigma^2_{e_{AB}}$ can be represented as $\{B \notin A\}$. The squared correlation coefficient ($\rho^2_{AB}$) can be computed as the ratio between the total variance of $A$ and the portion of variance in that is $A$ associated with the variance in $B$, as follows

$$\rho^2_{AB} = \frac{\sigma^2_{P_{AB}}}{\sigma^2_A}$$  \hspace{1cm} (2.10)$$

Figure 2.8: Venn diagram of two variables for different degrees of correlation, and the meaning of the squared correlation coefficient.
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Considering that the predictable portion of variance in $A$ is $\{B \in A\}$, then $\sigma^2_{P_{AB}} = \{A - B \notin A\}$. Replacing $\{A\} = \sigma^2_A$ and $\{B \notin A\} = \sigma^2_{eAB}$, equation (2.10) can be modified as follows:

$$\rho^2_{AB} = \frac{\sigma^2_A - \sigma^2_{eAB}}{\sigma^2_A} \quad (2.11)$$

Reducing (2.11), the squared correlation coefficient can be computed as

$$\rho^2_{AB} = 1 - \frac{\sigma^2_{eAB}}{\sigma^2_A} \quad (2.12)$$

Using equation 2.12, the error of predicting the variance of $A$ with the variance information of $B$ can be quantified with the following equation:

$$\sigma_{eAB} = \sqrt{\sigma^2_A(1 - \rho^2_{AB})} \quad (2.13)$$

Equation (2.13) can be implemented to quantify the error of predicting the delay performance relationship between circuit’s outputs. This implementation is shown in (2.14).

$$\sigma_{eS_1,S_2} = \sqrt{\sigma^2_{S_2}(1 - \rho^2_{S_1,S_2})} \quad (2.14)$$

where $\sigma_{eS_1,S_2}$ represents the **standard error of estimation** when the variable $S_1$ is estimated from variable $S_2$. As can be observed in (2.14), the error of estimation depends on the variance of the variable that is going to be predicted and the correlation between variables. A similar equation is presented in 2.15 where $\sigma_{eS_2,S_1}$ accounts for the error of estimating $S_2$ from the value of $S_1$.

$$\sigma_{eS_2,S_1} = \sqrt{\sigma^2_{S_1}(1 - \rho^2_{S_1,S_2})} \quad (2.15)$$

Both (2.14) and (2.15) are equally valid equations that describe the relationship between two variables (paths delays). Nevertheless, the error of estimation that can be computed with equations (2.14) and (2.15) may be different, depending on the variance properties of each variable. As can be observed in both equations, the error of estimation is proportional to
the square root of the variance in the variable to be predicted. Therefore, in order to reduce the error of estimation between a couple of variables, is recommended to select the variable with the smaller variance. Latter on this section, a methodology to standardize the error of estimation will presented.

Once the standard error of estimation between two variables is known, this correlation can be tested using a sample of each variable. Consider Figure 2.9 where the sample $S_{1,i}$ and the $\sigma_{e_{S_{1},S_{2}}}$ can be used to establish a detection region of $\pm 6\sigma_{e_{S_{1},S_{2}}}$ width, where the value of a sample $S_{2,i}$ agree with the relationship between variables. This region of detection will be addressed as threshold gap and if the value of the any sample $S_{2,i}$ exceeds this threshold gap, then that sample does not agree with the correlation information.

![Figure 2.9: Threshold gap defined by the value of a sample $S_{1,i}$ and the $\sigma_{e_{S_{1},S_{2}}}$](image)

Points $\text{①}$ and $\text{②}$ in Figure 2.9 represent the upper and lower limit of the threshold gap, respectively. This limits are established for the value that a sample of $S_{2}$ must have according to certain sample of $S_{1}$ in order to keep the relationship expected. In other words, for each sample value of variable $S_{1}$ the value of a $S_{2}$ sample can be predicted with an accuracy of $\pm 3\sigma_{e_{S_{1},S_{2}}}$. Limits $\text{①}$ and $\text{②}$, are determined by equations (2.16) and (2.17), respectively.

\[
S_{2,\text{upper}} = S_{2,i_{FC}} + 3\sigma_{e_{S_{1},S_{2}}} \tag{2.16}
\]
\[
S_{2,\text{lower}} = S_{2,i_{FC}} - 3\sigma_{e_{S_{1},S_{2}}} \tag{2.17}
\]
where $S_{2,i_{FC}}$ stands for the value of $S_2$ assuming full correlation. The value of $S_{2,i_{FC}}$ can be determined as a function of $S_1$ using equation (2.7), as given by equation (2.18). Conversely, $S_{1,i_{FC}}$ can be obtained as a function of $S_2$ in the same manner.

\[
(S_{2,i_{FC}} - \mu_{S_2}) = m \times (S_{1,i} - \mu_{S_1}) = \left(\frac{\sigma_{S_2}}{\sigma_{S_1}}\right) (S_{1,i} - \mu_{S_1}) \tag{2.18}
\]

where $S_{2,i_{FC}}$ and $S_{1,i}$ are the $i$-th sample of the respective variable. By normalizing each sample, $\frac{\sigma_{S_2}}{\sigma_{S_1}}$ can be used as $m$. Using (2.16), (2.17) and (2.18) the upper and lower limits of $S_2$ can be represented as in equations (2.19) and (2.20), respectively.

\[
(S_{2,\text{upper}} - \mu_{S_2}) = \left(\frac{\sigma_{S_2}}{\sigma_{S_1}}\right) (S_{1,i} - \mu_{S_1}) + 3\sigma_{e_{S_1},S_2} \tag{2.19}
\]

\[
(S_{2,\text{lower}} - \mu_{S_2}) = \left(\frac{\sigma_{S_2}}{\sigma_{S_1}}\right) (S_{1,i} - \mu_{S_1}) - 3\sigma_{e_{S_1},S_2} \tag{2.20}
\]

Using equations (2.19) and (2.20) the range where the value of $S_{2,i}$ and $S_{1,i}$ agrees with the relationship predicted, can be expressed as follows

\[
\left(\frac{\sigma_{S_2}}{\sigma_{S_1}}\right) (S_{1,i} - \mu_{S_1}) - 3\sigma_{e_{S_1},S_2} \leq S_{2,i} - \mu_{S_2} \leq \left(\frac{\sigma_{S_2}}{\sigma_{S_1}}\right) (S_{1,i} - \mu_{S_1}) + 3\sigma_{e_{S_1},S_2} \tag{2.21}
\]

If two delay samples of two non-fully correlated paths, one of each path, does not fulfill equation (2.21) that means that one (or both) of the samples do not agree with the relationship predicted. In other words a correlation deviation between variables is present.

Expression (2.21) represents the threshold gap when the $S_2$ is approximated by $S_1$. The threshold gap when $S_1$ is estimated from $S_2$, can be expressed in a similar way using the following expression.

\[
\left(\frac{\sigma_{S_1}}{\sigma_{S_2}}\right) (S_{2,i} - \mu_{S_2}) - 3\sigma_{e_{S_2},S_1} \leq S_{1,i} - \mu_{S_1} \leq \left(\frac{\sigma_{S_1}}{\sigma_{S_2}}\right) (S_{2,i} - \mu_{S_2}) + 3\sigma_{e_{S_2},S_1} \tag{2.22}
\]

In both equations (2.21) and (2.22), $\sigma_e$ represents the minimum deviation that can be detected. Even when equations (2.21) and (2.22) are based on the same conditions of variables’ variance and correlation, the width of the detection threshold may be different depending on the variance of the variable that is going to be estimated. In order to unify the detection threshold, both variables $S_1$ and $S_2$ can be standardized. If the variables $S_1$ and $S_2$ are
standardized, then the standard error of estimation given in (2.14) can be rewritten as:

\[ \sigma_{e'} = \sigma_{e_{S'}}, = \sigma_{e_{S'1}} + \sigma_{e_{S'2}} = \sqrt{1 - \rho^2_{S1,S2}} \]  

(2.23)

Using equations (2.5) and (2.23), the equations (2.21) and (2.22) can be simplified as in equations (2.24) and (2.25).

\[ S'_{1,i} - 3\sigma_{e'} \leq S'_{2,i} \leq S_{1,i} + 3\sigma_{e'} \]  

(2.24)

\[ S'_{2,i} - 3\sigma_{e'} \leq S'_{1,i} \leq S_{2,i} + 3\sigma_{e'} \]  

(2.25)

### 2.5 SDD Detection Using Correlation

The basis of correlation deviation detection presented previously will be used to detect delay defects on paths of a circuit. Assuming two paths \( P_1 \) and \( P_2 \) with a delay distribution \( D_{P1} \) and \( D_{P2} \) respectively, equation (2.21) (or its standardized version (2.24)) can be expressed as a function of each path delay distribution as follows

\[
\left( \frac{\sigma_{D_{P1}}}{\sigma_{D_{P2}}} \right) (D_{P2,i} - \mu_{D_{P2}}) - 3\sigma_{e_{P2,i}} \leq D_{P1,i} - \mu_{D_{P1}} \leq \left( \frac{\sigma_{D_{P1}}}{\sigma_{D_{P2}}} \right) (D_{P2,i} - \mu_{D_{P2}}) + 3\sigma_{e_{P2,i}}
\]

(2.26)

where \( D_{j,i} \) is a delay measurement of the \( j \)-th path and \( \sigma_{e_{P2,i}} \) is the standard error of estimation of \( D_{P2,j} \) from the value of \( D_{P1,i} \). The detection principle of this methodology is based on the detecting deviations from the relationship between paths delay. Figure 2.10 shows possible delay distributions of paths \( P_1 \) and \( P_2 \) with a hypothetical correlation coefficient of 0.8. If for a given die, both paths \( P_1 \) and \( P_2 \) are defect-free, the samples \( D_{P1,i} \) and \( D_{P2,i} \) will agree with the relationship expected for \( \rho = 0.8 \). On the other hand, if \( P_2 \) is defective, its delay distribution will change as well as the relationship between paths delay. In other words, if the relationship between samples of two path delays do not agree with the relationship predicted by inter-path correlation, a defect is present in one or both of the paths.

As can be observed in (2.14), the size of the variation that can be detected is dependent
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Figure 2.10: Inter-path correlation between paths $P_1$ and $P_2$ when they are defect free, and its deviation when path 2 presents a defect.

of the correlation coefficient. This means that for outputs with low correlation, the threshold gap is wider, increasing the minimum delay deviation that can be detected. Figure 2.11 shows graphically the concept of delay deviation detection. The waveform of the propagated signal through paths $P_1$ and $P_2$ are shown. Assuming full-correlation between both paths, if for a
certain die \( i \) the time delay of path \( P_1 \) is \( D_{1,i} \), then the time delay of path \( P_2 \) must have a certain value \( D_{2,i-FC} \) (where FC stands for full correlation). The time delay of path \( P_2 \) can be computed from (2.7) as follows

\[
D_{2,i-FC} = \frac{\sigma_{D_2}}{\sigma_{D_1}} (D_{1,i} - \mu_{D_1}) + \mu_{D_2}
\]  
(2.27)

If the inter-path correlation between \( P_1 \) and \( P_2 \) is lower than 1, then equation (2.27) will be no longer valid. This is because the estimated value of \( D_{2,i} \) will have a random value contained inside the detection threshold PDF, which have a mean \( \mu_{FC} = D_{2,i-FC} \) and a standard deviation \( \sigma_{e_{D_1,D_2}} \). If for a certain \( D_{1,i} \) the value of \( D_{2,i} \) is out of the distribution, that means that a correlation deviation is present. The deviation in correlation between \( D_1 \) and \( D_2 \) can be due to an abnormal increase (or reduction) in the delay of \( P_1 \) or \( P_2 \).

Using this principle, SDDs that increase the delay of a path long enough to overpass the detection threshold PDF can be identified from process variations. The minimum detectable delay in \( P_2 \), can be represented as the smallest delay increase that can be detected with certain conditions of path’s variance and inter-path correlation. This minimum increase is considered tacking \( D_{2,i-FC} \) as reference. This minimum delay detectable is represented as \( \Delta D_{\text{min}} \) in Figure 2.11, and can be computed as follows:

\[
\Delta D_{\text{min}} = 3\sigma_{e_{D_1,D_2}}
\]  
(2.28)

The behavior of \( \Delta D_{\text{min}} \) as a function of inter-path correlation can be observed in Figure 2.12, where the value of \( \Delta D_{\text{min}} \) is normalized by the variance of the variable to predict (\( \sigma_{D_2} \)). Figure 2.12 shows that as the inter-path correlation decreases the error of estimation increases. The relationship between error of estimation and inter-path covariance has a negative quadratic behavior; which means that an small increase on inter-path correlation produces a reduction on the error of estimation.

One of the main advantages of the proposed methodology is the ability to detect SDDs on short and long paths, independently of their timing slack. Moreover, this methodology allows
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Figure 2.12: Minimum delay detectable behavior as a function of inter-path correlation.

the detection of defects under the presence of process variations, allowing to distinguish between delay fluctuations due to process variations and delay fluctuations due to the presence of a defect. This last condition can be clarified considering Figure 2.13.

Figure 2.13: Representation of the different cases of SDD detectability increase that can be achieved with the proposed methodology.

In Figure 2.13, the delay of each path under test from three sample dies are analyzed. As can be observed, path 2 is the objective path and path 1 is the path used as reference. On the delay distribution of each path the terms $S_{i,j}$ represents the delay of the $j$-th sample die for the $i$-th path. For each sample of path 1, a correspondent threshold gap is presented on the delay distribution of path 2; the width of these threshold gaps is established using the
2.5 SDD Detection Using Correlation

error of estimation ($\sigma_e$) described by the proposed methodology, assuming a certain positive degree of inter-path correlation. The terms $\Delta_1 \cdots \Delta_3$ represents three possible scenarios for the proposed methodology.

For the case $\Delta_1$, the sample $S_{1,1}$ indicates that the expected value of $S_{2,1}$ must be within the respective detection gap shown on the delay distribution of path 2. The value of $S_{1,1}$ indicates that the process variations that affect die #1, make it a slower than typical; for the case of $\Delta_2$, die #2 has a delay behavior very close to typical, and assuming a positive high correlation, the delay behavior must be within the detection gap for $S_{2,2}$. Finally $\Delta_3$ represents the case of a faster than typical die.

For the matters of establishing a figure of merit that accounts for the SDD detectability achieved by the proposed methodology is necessary to account for the portion of path’s process variance that can be distinguished from fluctuations due to defects. In order to graphically represent this portion of variance consider Figure 2.14, where for simplicity, $S_i$ is a certain delay sample equal to the mean of the delay distribution. Both $\sigma_D$ and $\sigma_e$ represent the standard deviation of the delay distribution and the error of estimation, respectively.

As can be observed in Figure 2.14, the portion of variance due to process variations that can be distinguished from those fluctuations generated by a defect is the sum of the variance exceeding $+3\sigma_e$ (“faster” variance) and below $-3\sigma_e$ (“slower” variance) value. This SDD screenable variance (SSV) can be established as a figure of merit that represents the percentage of variance where the effects of an SDD can be detected. SSV can be computed
as follows:

\[ SSV = \left(1 - \frac{\sigma_e}{\sigma_D}\right) \times 100 \quad (2.29) \]

As can be observed in Figure 2.14, for higher values of SSV, SDDs can be identified in a larger portion of path’s variance. In Figure 2.15, the normalized delay standard deviation \((\sigma_D/\sigma_D)\) is compared with the normalized SSV \((SSV/\sigma_D)\) for different values of correlation. As can be observed, as the correlation grows SSV also grows, which means that a larger part of variance can be screened.

![Figure 2.15: SDD screenable variance behavior as a function of correlation.](image)

A very interesting point to notice is the fact that even with the worst case of correlation \((\rho \approx 0)\), the methodology is able to detect delay defects that are larger than \(\pm 3\sigma_D\) as in others methodologies [50]. A very important characteristic of SSV can be inferred by looking at equation (2.29), where neither mean of \(S_1\) nor the mean of \(S_2\) play a role on SSV computing. This points out that the efficiency of this methodology is related to the paths variance but not to the path’s nominal delay. This characteristic implies that this methodology can be implemented independently of the path’s logic depth and timing slack. However, long paths will tend to have a larger variability which may decrease the correlation between paths depending on the characteristics of the circuit.

To show an example of the application of the proposed methodology consider paths \(P_1\) and \(P_2\) for the circuit shown in Figure 2.16a. The circuit is analyzed for a variation of \(\pm 15\%\)
on L, W, $T_{ox}$ and $V_{th}$. The circuit was implemented on a TSMC 0.18$\mu$m technology and a Monte-Carlo simulation with 1000 iterations was made. The delay distribution of each path is shown in the table of Figure 2.16b.

<table>
<thead>
<tr>
<th>Path</th>
<th>$\mu_D$(ps)</th>
<th>$\sigma_D$(ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_1$</td>
<td>196.6</td>
<td>12.75</td>
</tr>
<tr>
<td>$P_2$</td>
<td>106.02</td>
<td>6.38</td>
</tr>
</tbody>
</table>

Figure 2.16: ISCAS 85 c17 circuit used to show the methodology implementation.

Using the information in Table 2.16b and assuming different degrees of correlation (the procedure for estimating the actual inter-path correlation will be described in chapter 3), the minimum detectable delay in path $P_2$ is represented in Figure 2.17.

Figure 2.17: Minimum delay detectable on circuit of Figure 2.16a as a function of inter-path correlation
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2.6 Improving the Proposed Methodology Using Multiple Correlation

As can be observed in the previous section, the minimum detectable delay depends on the degree of correlation between variables. Therefore, the increasing of inter-path correlation must be considered as a priority goal. This can be achieved by considering multiple paths at the detection reference frame.

As mentioned in the beginning of section 2.4, the variance of a variable that can not be described by the variance of the other, reduces the ability to predict the behavior of that variable. This can be represented in circuits as those variations that have an effect in a path under test but that do not have the same effect in another path; Nevertheless, if there is a third path that is affected by those variations, then its information will be useful to describe the behavior of the path under test. This concept can be represented by the Venn diagram of Figure 2.18.

![Venn diagram](image)

Figure 2.18: Venn diagram that represent the associated portion variance between one variable and another two correlated variables.

2.6.1 Detection of Correlation Deviations Using Multiple Variables

When more than two random variables are considered, the correlation information between all variables together is known as *multiple correlation* and is represented with the multiple correlation coefficient (*R*). The meaning of *R* can be described as a degree of how multiple variables change together. When multiple variables are considered, the correlations between
any pair of variables is known as partial correlation and denoted by \( r_{ij} \), where \( i \) and \( j \) are the correlated variables. The multiple correlation between a certain variable and \( n \) variables is represented by \( R_{i,j_1j_2\ldots j_n} \). The concept of multiple and partial correlation can be represented graphically with a Venn diagram in Figure 2.19.

\[
R_{A,BC} = B \in A \cap C \in A
\]

\[
r_{AB} = B \in A \]

\[
r_{AC} = C \in A
\]

\[
r_{BC} = C \in B = 0
\]

Figure 2.19: Graphical representation of multiple and partial correlation.

If the distributions of a group of variables and the correlation between them is known, multiple correlation can be used to detect deviations in a variable distribution. Nevertheless, in a multiple variable approach, the behavior of one variable is described by the information in more than one variable, this demands the use of a multi-variable approximation. In order to address this issue, a multi-linear regression [72, 76] analysis can be used. This multi-linear analysis is based on establishing an approximation equation as

\[
Y_i = \beta_1 X_{1,i} + \beta_2 X_{2,i} + \cdots + \beta_k X_{k,i}
\]  

(2.30)

where \( Y_i \) is the standardized \((Y_i - \mu_Y)/\sigma_Y \) variable to be approximated, which is referred as criterion variable; the \( X_{j,i} \) terms are the \( i \)-th standardized value of the \( j \)-th variable used to predict \( Y_i \), also referred as predictor variables. The coefficients \( \beta_1 \) to \( \beta_n \) are known as \( \beta \)-weights. Using a similar analysis to the one in section 2.4, the standard error of estimating a variable based on a multi-linear regression can be expressed as follows:

\[
\sigma_{\hat{Y}_{X_1\ldots X_n}} = \sqrt{\sigma_Y^2(1 - R_{YX_1\ldots X_n}^2)}
\]  

(2.31)
If the predictor and criterion variables are standardized, equations (2.30) and (2.39) can be simplified to equations (2.32) and (2.33) respectively.

\[ Y_i' = \beta_1 X_{1,i} + \beta_2 X_{2,i} + \ldots + \beta_k X_{k,i} \]  
(2.32)

\[ \sigma'_{\epsilon Y_{X_1 \ldots X_k}} = \sqrt{1 - R^2_{Y_{X_1 \ldots X_k}}} \]  
(2.33)

The multiple correlation coefficient and the \( \beta \)-weights can be computed from the correlation information between variables. This correlation can be represented in a matrix form as in Figure 2.20. This matrix is divided into three sub-matrix arrays, \( R_{XX} \) also known as *cross-correlation* matrix, which contain the correlation coefficients between predictor variables, and the sub-matrices \( R_{XY} \) and \( R_{TX}^T \) that contains the correlation information of the criterion variable with each of the predictor variables.

\[ \beta = \begin{bmatrix} \beta_1 & \beta_2 & \cdots & \beta_n \end{bmatrix} \]  
(2.34)

\[ \beta = R_{XY} R_{XX}^{-1} \]  
(2.35)
The multiple correlation coefficient can be computed using the following equation

\[
R_{Y,X_1\cdots X_k} = R_{XY}R_{XX}^{-1}R_{XY}^T = \beta R_{XY}^T
\]  

(2.36) \hspace{1cm} (2.37)

Equations (2.32) and (2.33) can be implemented to approximate the delay behavior of a path using multiple inter-path correlation information. Consider \( n \) paths \( \{P_1, P_2, \cdots, P_n\} \) and their delay associated \( \{D_1, D_2, \cdots, D_n\} \). The delay of path \( P_1 \) can be approximated as follows

\[
D_1 = \beta_0 + \beta_1 D_2 + \beta_2 D_3 + \cdots + \beta_{n+1} D_n
\]  

(2.38)

and the error of estimating \( D_1 \) from the delays of the others paths, can be computed as

\[
\sigma_{e_{1,2-n}} = \sqrt{(1 - R_{1,2-n}^2)}
\]  

(2.39)

where \( \sigma_{e_{1,2-n}} \) represents the error of estimating delay of path \( P_1 \) from delays of paths \( P_2 \) to \( P_n \).

### 2.6.2 Multicollinearity Considerations

As can be observed when multiple variables are considered, the multiple correlation coefficient increase reducing the error of estimation. Nevertheless, increasing the number of variables under analysis not always increase the multiple correlation coefficient. When the predictor paths are highly correlated between them, they basically are related to the same variations, this implies the predictor paths will describe the same portion of variance in the criterion variable. In other words, the portion of criterion path variance that is described by a single predictor path is the same that the one considering both predictors. This phenomenon can be observed in Figure 2.21.

As can be observed in Figure 2.21, \( B \in A \) and \( C \in A \) are almost the same, this implies that \( R_{A,BC} \approx r_{A,B} \approx r_{A,C} \). To show the effects of multicollinearity on the multiple correlation coefficient and on the error of estimation, consider the multiple correlation matrix of Figure
2.22a. This matrix is analyzed for different degrees of predictor variables correlation, and the resulting $R$ and $\sigma_e$ of estimating $A$ are shown in Figure 2.22b.

\[
\begin{bmatrix}
B & C & A \\
1 & \rho_{BC} & 0.7 \\
\rho_{BC} & 1 & 0.6 \\
0.7 & 0.6 & 1 \\
\end{bmatrix}
\]

(a) Multiple correlation matrix under analysis.

Figure 2.22: Example of the multicollinearity effects on the multiple correlation and on the estimation error.
2.7 Delay Sampling

The behavior of $\sigma_e$ in Figure 2.22b shows that, as the correlation between predictor variables ($\rho_{BC}$) increase, the value of $R_{A,BC}$ tends to the maximum value of partial correlation between $A$ and any of the predictor variables. This can be understood by considering that the variance of highly correlated predictor variables will be associated to the same portion of variance in the criterion variable; on the other hand, if the predictor variables are poorly correlated the variance of each predictor will be associated to different portion of variance in the criterion variable and in consequence a larger portion of the criterion variance can be described. Therefore, in order to maximize the effectiveness of a multi-variable approach is necessary to reduce the effects of multicollinearity, which can be achieved by selecting predictor paths that are poorly correlated between them.

2.7 Delay Sampling

The methodology described earlier in this chapter is based on the comparison of delay measurements of fabricated circuits and a previously established reference framework. Therefore, the procedure of getting delay samples post-fabrication is a topic that should be considered.

Measuring the propagation delay of a circuit is a very expensive procedure. This is because in order to measure a delay, a certain input and output signal of a circuit must be compared; unfortunately observing a signal on real time consumes a large amount of time and the cost of the equipment capable of measuring those signals will be infeasible. Therefore, diverse techniques that allows delay measurements have been developed. These techniques can be classified in two main categories, direct and indirect measurements.

Indirect Measurements:

Indirect measurements are based on the correlation between the performance of certain built-in structures in a circuit. One of the most common technique is the insertion of ring-oscillators at specific locations of a die. The oscillation frequency of the inserted structures will be correlated with the delay performance of a circuit, specifically to those devices near the oscilla-
The correlation between oscillator’s frequency and delay performance, can be used to approximate the delay of a circuit based on the operation frequencies of the inserted oscillators. Works like [77] found a high correlation between ring-oscillator frequencies and IDDQ. Other approaches use non-nominal voltage supply like in [78], where the authors propose a relationship model between propagation delay and supply voltage reduction.

**Direct Measurements:**

Direct delay measurement had become the industry standard. Some of the methodologies use clock multiplexed pins or multiple signals to enhance the capabilities of ATE equipment. Other approaches like [79] propose the implementation of low frequency testing modes on the circuits structure, in order to allow high speed devices to be tested with relatively slow tester. Nevertheless, these approaches continue to relay on ATE equipment characteristics.

As can be observed from the previous characteristics, indirect measurements are not suitable for implementing the methodology proposed in the present work as they relay on the relationship between devices to produce a delay measurement. Therefore, *multiple-clock schemes*, which is one of the main direct methodologies will be discussed.

### 2.7.1 Multiple-Clock Schemes

In order to reduce the cost of delay measurements and improve its precision, the delay of a circuit is approximated based on the behavior of the circuit for different observation intervals. The *multiple-clock schemes* have proved to be a cheap and efficient methodology to estimate the delay of a circuit [65, 80]. Works like the one by Singh *et al* [65, 67], propose the use this methodology as a delay testing technique. This methodology is based on implementing a transitional test, like the one described in section 1.3.1.1, for multiple observation intervals, each one progressively shorter than the previous. Each observation interval is separated by a certain $\Delta t$. When a testing vector $V_i$ (the same testing vector described in section 1.3.1.1) is applied, the transition is generated and propagated to a primary output where the logic level will be observed at each interval. This process is shown in Figure 2.23.
In Figure 2.23, each interval \( t_i \) represents the \( i \)-th observation interval at which the signal will be analyzed. If at certain interval \( t_i \) the signal crosses the logic threshold, then the delay will be within \( t_{i-1} \) and \( t_i \).

In order to increase the accuracy of the measurement, \( \Delta t \) must be small. The use of closer intervals will increase the resolution of the measurements. Nevertheless, increasing the resolution will rise the number of times that the circuit must be tested which increase the cost of the measurement.

This delay measurement technique can be easily implemented with the proposed methodology. Nevertheless, the resolution of this technique is a critical characteristic that must be considered. Due to the fact that delay measurement will be “quantized”, if the resolution of the measurement is not enough, the closest next time interval may exceed the minimum delay detectable (\( \Delta_{min} \)) as presented in Figure 2.24. This conditions will reduce the efficiency of the methodology because those SDDs that exceed \( \Delta_{min} \) but not the closest next interval will be ignored.

In order to minimize the error of sampling, the observation intervals intervals must be shorter than \( \Delta_{min} \). The worst case of maximum error due to sampling quantization, occurs when the middle of delay variation is aligned with the center of certain observation interval like shown in Figure 2.40. This maximum error can be represented as a maximum increase
Chapter 2: Methodology to detect Small-Delay Defects Using Inter-Path Correlation

Figure 2.24: Minimum delay detectable increase due to low sampling resolution.

of the effective value of $\Delta D'_{\text{min}}$, which can be computed as follows

$$
\Delta D'_{\text{min}} = \Delta D_{\text{min}} \times \left(1 + \frac{\Delta t}{\Delta D_{\text{min}}} \right)
$$

(2.40)

where $\Delta D'_{\text{min}}$ represents the minimum delay detectable on the worst scenario according to Figure 2.24, $\Delta t$ is the observation interval’s length and $\Delta_{\text{min}}$ is the minimum detectable delay established by the reference frame. As can be observed, as the sampling resolution increase, $\Delta D'_{\text{min}}$ tends to the original value of $\Delta D_{\text{min}}$. Therefore, the trade-off created between the sampling resolution and the cost of implementation must be considered during the testing setup.

2.7.2 Other Alternatives

As operation frequencies increase, the use of ATE increase the testing cost. Therefore, in order to reduce the costs, the tendency is to include on-chip testing devices that reduce the use of equipment, these techniques are known as built-in Delay Measurement (BIDM). Some of the first BIDM techniques were gross-delay measurement techniques like AC scan [81] which were used as a qualitative timing characterization. However, as technology scales down and delay defects become smaller, and higher resolution and adaptable methodologies
are required [82]. Other approaches make use of the stability checking scheme, where the values of signals are compared with another reference signal (usually CLK). However, this testing structures are highly sensitive to noise.

No matter which delay sampling technique is used to implement the proposed methodology, the precision of these techniques must be analyzed in order to quantify the error that they induce on the efficiency of the proposed methodology.

2.8 Conclusions

In this chapter the methodology of SDDs detection using inter-path correlation was described. This methodology identify deviations in delay by comparing the actual delay performance of a path with the performance of the other paths. The main contribution of this methodology is that SDDs can be identified from delay fluctuations due to process variations, without increasing the circuits overhead or test pattern generation complexity.

It was shown that the detection capability of the methodology can be enhanced by using a multi-variable approach. However, this enhancement depends on the number of paths considered and the correlation between them. The cost of this methodology rises as the number of paths included in the analysis increase. Moreover, the implementation of a delay measurement technique also increase the cost of this methodology, creating a trade-off between the methodology’s precision and the implementation cost. Therefore this methodology is recommended more as a reliability improvement technique than as an exhaustive testing technique.
Chapter 3

Computing the Degree of Inter-Path Correlation

An statistical-static timing analysis (SSTA) tool has been developed to compute the degree of correlation between paths. The developed SSTA tool accounts for the main physical variations and their spatial behavior; also, the influence of the topology of the circuit is considered. This chapter is constituted as follows: Section 3.1 gives an overview on SSTA. In section 3.2, the models used to describe process variations are presented. The methodology to compute inter-path correlation of the SSTA tool is presented in section 3.3. The implementation algorithm of the SSTA framework is presented in section 3.4. Finally, section 3.5 gives the conclusions of the chapter.

3.1 Introduction

Since process variability has become a critical part of circuit design, the simulation of circuit’s behavior under the effects of process variations has become a mandatory step during the design phase. For many years methods known as corner analysis have been the standard for the industry, even when they overestimate the variance of devices. Nevertheless, in recent years, approaches like SSTA have been used to simulate the variability of a circuit, as these
3.1 Introduction

approaches are faster and more accurate. In this section both approaches will be briefly described.

3.1.1 Corner Analysis

The traditional approach to address process variation is the implementation of a worst case analysis and design. This method is highly accepted because it increases the reliability of a circuit, as it considers the worst cases of process variations. This worst case analysis is implemented in many different scenarios, each of which is determined by three different variables [83].

1. **Parasitics corner (interconnect RC conditions):** it refers to variations in the geometrical parameters of an interconnection.
   - Typical: the parameter of interconnections have the nominal values.
   - Maximum C: represents the maximum interconnection capacitance, with nominal resistance.
   - Minimum C: this refers to the minimum value of capacitance, with nominal resistance.
   - Maximum RC: this refers to the corner with the maximum RC product.
   - Minimum RC: represents a corner with the minimum RC product.

2. **Operating mode:** it stands for the operation mode of the circuit.
   - Normal operation mode.
   - Test mode.
   - Sleep mode.
   - Low Power operation mode.
   - Etc.
3. **Process, voltage and temperature (PVT) corners:**

- Typical: typical process speed, nominal power supply, nominal temperature.
- Fast: fast process, nominal power, nominal temperature.
- Slow-cold: slow process, nominal power supply, low temperature.
- Fast-low-VDD: fast-process, low power supply, nominal temperature.
- Or any other combination of PVT variations.

The corner analysis can be made under any combination of the previous conditions. Implementing an analysis that cover all the possible conditions is not feasible, as it will dramatically increase the testing cost. Therefore, designers selects a group of few corners that allows the best possible characterization of the circuit. Many of these corners can be considered simultaneously by implementing a *multi-mode multi-corner* analysis (MMMC). This kind of analysis is usually addressed by statistical methods like Monte-Carlo analysis [84], which allows the estimation of a probability distribution that represents the performance of the circuit. Nevertheless, this kind of analysis are hard and expensive to implement, and its complexity grows with the number of parameters and the size of the CUT.

### 3.1.2 Statistical-Static Timing Analysis (SSTA)

The use of corner based methodologies is inherently deterministic, as a circuit is tested at multiple times for specific process and operation mode conditions. Even if all the possible corners were considered, this will produce an overestimation of circuits variability [85]. The SSTA on the other hand, is based on representing each parameter of a circuit as a probability distribution (usually gaussian). This implies that the performance of a given gate, path or circuit is described as a probability distribution. Thus every delay on any part of the circuit is described statistically.

The SSTA maps the variation of all parameters regarding to their nominal values into an overall gate, path or circuit delay variation. Thus after an SSTA, the delay performance is the accumulation of all parameters variance. The overall delay distribution mean is considered
Considerations for Inter-Path Correlation Estimation

as the accumulation of all parameter’s distribution mean. The resultant standard deviation 
\( \sigma_T \) will be the sum of the standard deviation of two variables \( \sigma_A + \sigma_B \); if the two variables 
are fully correlated, or \( \sqrt{\sigma_A^2 + \sigma_B^2} \) if the two variables are fully uncorrelated [72]. The case 
of \( \sigma_A + \sigma_B \) is larger than \( \sqrt{\sigma_A^2 + \sigma_B^2} \). As the case of full and non-full correlation are very 
uncommon, the accurate modeling of correlation between parameters is critical in SSTA.

Once the performance of a circuit has been characterized, maximum and minimum values 
of circuit’s parameter performance can be established. The maximum and minimum parameter 
values are described at \( \mu + 3\sigma \) and \( \mu - 3\sigma \) respectively. These \( \pm 3\sigma \) values describe the 
0.135% and 99.865% quantile of the normal distribution. This means that only 0.135% of the 
distribution values are lower than \( \mu - 3\sigma \) or higher than \( \mu + 3\sigma \). The quantile values can be 
adjusted by the designer depending on the precision and complexity required for the analysis. 
For a circuit under test, a timing reference is set according to the maximum delay time of the 
circuit. Using the timing reference of the circuit and the performance distribution, is possible 
to establish the yield of the circuit.

Even when SSTA is a relatively new technique, the trend in process variability is leading 
to an increase in the use of SSTA tools for design and testing of ICs. The main limitation for 
the full migration from STA to SSTA is the complexity of generating statistical models. A 
significant amount of efforts are focused on developing more efficient SSTA tools. SSTA tools 
like the one by Kang et al [69] and the one by Agarwal [71] are very efficient on estimating 
the delay performance of a circuit. The main aspects that an SSTA tool should consider 
are: D2D and WID variations, the spatial correlation between systematic WID variations, the 
structural correlation between devices and the effects of random variations.

3.2 Considerations for Inter-Path Correlation Estimation

Although SSTA is a fast growing alternative to delay performance estimation under process 
variation [69, 85, 86, 87], the inter-path correlation has only been used as a requirement to an 
accurate delay estimation. This section describe the models implemented to estimate inter-
path correlation considering process variations and their spatial and topological behavior.
3.2.1 Process Variability

As mentioned in chapter 1, process variations are the fluctuations from designed parameter values in a structure or device. These variations can be separated into two main classes, die-to-die variations (D2D) and within-die variations (WID). WID variations can be classified as spatially correlated or spatially uncorrelated; those variations that are spatially correlated are also known as systematic variations and the ones that are spatially uncorrelated are conventionally addressed as random variations. Two variables are spatially correlated when the fluctuations of devices that are closely located are very similar, contrary to those that are far from each other. Therefore, spatial correlation between devices is a function of the distance between them [36, 88].

Besides the spatial correlation between devices, two paths can be correlated by their topology. When a gate is present in two or more paths, the process variations of that gate will have the exact same influence on the delay performance of all the paths related to that gate, this kind of correlation is known as structural correlation [86].

In order to estimate inter-path correlation, this work consider process variations in the parameters gate length (L), gate width (W), oxide thickness ($T_{ox}$) and threshold voltage ($V_{th}$), modeling each one of them with a normal distribution $N(\mu, \sigma^2)$. Moreover, the spatial and structural correlation between paths must be modeled according to the spatial location of each device and the circuit topology. The models used in this work to describe random variations and correlation between paths will be described.

3.2.2 Random Variations

One of the random variations that significantly influences the delay performance, specially for nanometer technologies, is known as random dopant fluctuations (RDF) [89, 90, 91, 92]. This phenomenon arise since the scaling has reduced the number of dopants in transistor’s structure, as shown in Figure 3.1. As the number of dopant atoms is reduced its variability increases. This tendency is shown in Figure 3.2.

In order to estimate the effects of RDF, equation (3.1) [89] can be used to calculate the
3.2 Considerations for Inter-Path Correlation Estimation

Figure 3.1: Reduction of dopants in transistor’s structure as technology scales down [93].

\[
\sigma_{VT_H} = \sigma_{VT_H0} \times \sqrt{\frac{L_{min}W_{min}}{L_{eff}W_{eff}}}
\]  

(3.1)

where \( L_{eff} \) and \( W_{eff} \) are the effective gate dimensions of the transistor, \( \sigma_{VT_H0} \) is the threshold voltage variation for a transistor with minimum dimensions and \( L_{min} \) and \( W_{min} \) represents the technology minimum gate dimensions. It can be observed that the effect of RDF is stronger on devices which dimensions closer to the minimum of the technology.
3.2.3 Spatial Correlation

When a process variation is spatially correlated, it means that its behavior on a device in a certain location will have a specific degree of correlation with the variance of the same parameter in a device located in a different position. The amount of spatial correlation between two devices, is a function of the distance between them and the process spatial correlation properties. Hence two devices closely located will be highly correlated and two devices that are faraway from each other will be poorly correlated. This phenomenon is illustrated in Figure 3.3, where the number on the upper right corner indicates the correlation coefficient between that grid and the reference grid (labeled as Ref.).

<table>
<thead>
<tr>
<th></th>
<th>Ref.</th>
<th>0.9</th>
<th>0.75</th>
<th>0.6</th>
<th>0.45</th>
<th>0.30</th>
<th>0.15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref.</td>
<td>0.9</td>
<td>0.9</td>
<td>0.7</td>
<td>0.57</td>
<td>0.42</td>
<td>0.27</td>
<td>0.11</td>
</tr>
<tr>
<td>0.75</td>
<td>0.9</td>
<td>0.7</td>
<td>0.66</td>
<td>0.52</td>
<td>0.39</td>
<td>0.23</td>
<td>0.08</td>
</tr>
<tr>
<td>0.6</td>
<td>0.7</td>
<td>0.66</td>
<td>0.52</td>
<td>0.41</td>
<td>0.32</td>
<td>0.15</td>
<td>0.06</td>
</tr>
<tr>
<td>0.45</td>
<td>0.57</td>
<td>0.52</td>
<td>0.41</td>
<td>0.32</td>
<td>0.26</td>
<td>0.10</td>
<td>0.01</td>
</tr>
</tbody>
</table>

Figure 3.3: Example of the spatial behavior for an X-parameter effects as a function of the distance. [94]

To include spatial correlation in a statistical analysis is necessary to implement a model that allow the spatial correlation to be considered between any two locations on a chip. There are few spatial correlation models in literature [86, 95, 96, 97]. All of them are based in partitioning the circuit in a finite number of grids, which are used to calculate the distance between devices. The main models are the Quad-tree [95] and the analytical model [86].
3.2 Considerations for Inter-Path Correlation Estimation

3.2.3.1 Quad-tree Model

A model to estimate spatial correlation is the quad-tree model which divide the circuit as a group of levelized partitions. This model represents the circuit under test as a single grid, then this grid is divided in four grids, and each one of those grids is also divided into four grids and so on, as can be seen in Figure 3.4. The number of levels in the model depends on the precision needed, as more levels are considered the number of grids increase with a function of $4^{N-1}$, where N is the number of levels.

A large number of grids allows a high resolution and therefore a more accurate representation of spatial correlation; nevertheless, a large number of grids increase dramatically the complexity of the analysis [69, 86]. No matter the number of levels included, the bottom level of the model represents the surface of the circuit and each grid represents a certain location. Ideally, the resolution of the model should be enough so each gate can have an exclusive
Chapter 3: Computing the Degree of Inter-Path Correlation

grid. The random variables that represents a parameter \( X \) at a grid \([2, 1]\) can be expressed as follows:

\[
X_{2,1} = X_0 + \Delta X_{2,1} + \Delta X_{1,1} + \Delta X_{0,1}
\]  

(3.2)

where \( X_0 \) represents the nominal value of parameter \( X \), and \( \Delta X_{i,j} \) represents the fluctuations in parameter \( X \) on the devices located at in the grid \([i, j]\) of the quad-tree model [95]. To estimate the correlation between a pair of points in the circuit, the first step is to choose the two sets of grids that will be associated with the variance on each point. The grids that will be considered are those that includes the location of each point at each level of the model. As an example consider the points located at \([2, 1]\) and \([2, 6]\), equations (3.3) and (3.4) represents the random variables at each grid. The covariance between these two grids is computed based on the common elements of both equations, as can be observed in (3.5).

\[
X_{2,1} = X_0 + \Delta X_{2,1} + \Delta X_{1,1} + \Delta X_{0,1}
\]  

(3.3)

\[
X_{2,6} = X_0 + \Delta X_{2,6} + \Delta X_{1,1} + \Delta X_{0,1}
\]  

(3.4)

\[
COV(X_{2,1}, X_{2,6}) = var(\Delta X_{1,1}) + var(\Delta X_{0,1}) = \sigma^2_{X_{1,1}} + \sigma^2_{X_{0,1}} = 2\sigma^2_X
\]  

(3.5)

where \( var(\Delta X_{i,j}) \) is the variance of the parameter \( X \) in the grid \([i,j]\). If each level of the quad-tree model has associated a variance of \( \sigma^2_X \) then for the case of the example the total variance will be \( 2\sigma^2_X \).

One of the main advantages of quad-tree model is the possibility to account for WID and D2D process variations. In equation (3.3) to (3.4), it is assumed that at each level corresponds the same percentage of the total variance, nevertheless this can be modified to account for WID and D2D variations. Consider the quad-tree model of Figure 3.4, where level 0 represents D2D variations, meanwhile WID variations are considered in levels 1 to N. If from the total variance, a higher percentage is assigned to level 0, this means that D2D variations are the main source of variations and the rest is due to WID variations. Therefore, with quad-tree model both D2D and WID variations can be considered.

Even when quad-tree model is the most used model, it has serious accuracy disadvantages,
3.2 Considerations for Inter-Path Correlation Estimation

like shown in Figure 3.5 [86]. It can be observed that grids [2,6] and [2,10] are clearly next to each other and consequently highly correlated. However, due to the partition sequence of quad-tree model, the correlation between them is underestimated because they only share grid [0,1].

Figure 3.5: Example of the susceptibility of the quad-tree model to underestimate correlation.

3.2.3.2 Analytical Model

Spatial correlation can be described with an analytical function that fits the physical measurement of correlation on a wafer. The complete analysis for the criteria to select a function that accurately model spatial correlation is given in [88]. In this work, the model used to consider spatial correlation is the one proposed by Zhang et al [86], that use an exponential function to describe the spatial correlation behavior. This model makes use of multiple grids to represent the die area, considering that all devices located in a certain grid have the same parameters variations. The correlation between any two grids as shown in Figure 3.6 can be estimated as follows

$$\rho(P_A, P_B) = \exp\left(-\frac{R_{AB}}{CD}\right)$$  \hspace{1cm} (3.6)

where $P_A$ and $P_B$ represent the variation of parameter $P$ at locations $A$ and $B$, respectively. The term $R_{AB}$ is the distance between $A$ and $B$; meanwhile, $CD$ is the correlation distance, which is an experimentally established constant that describes the spatial correlation behavior.

The correlation distance can be considered as the separation between devices at which the correlation between them is nearly zero [88]. This concept can be observed in Figure 3.7 where spatial correlation is plotted as a function of distance for different values of $CD$. As can
be inferred from Figure 3.7, for a short CD the spatial correlation coefficient decreases faster, going from $\rho = 1$ to almost 0 in less than $100\mu l$ ($\mu l$=generic units of length); on the other hand for a large CD the spatial correlation coefficient decrease at a very slow rate, giving a behavior of almost a constant $\rho$ for every distance within a die.

In order to accurately estimate the spatial correlation between devices, grid size must be set according to the correlation distance considered. The model implement a user defined parameter known as resolution which establish the granularity of the spatial model and consequently its accuracy. This parameter is used to set the appropriate number of grids and consequently the size of this grids according to the value of CD that is going to be considered. For short CD the size of the grids must be small in order to accurately capture the behavior of the spatial correlation; meanwhile for large CD the size of the grids may be larger which
reduce the number of grids in the model and its complexity.

\[
\text{gridsize} = \frac{CD}{\text{Resolution}} \quad (3.7)
\]

The analytical model can be extended to include WID and D2D variations by partitioning the total correlation of a parameter according to the relationship between WID and D2D [29]. For large technologies, D2D variations represent the majority of total process variations. Nevertheless, for nanometer technologies, WID variations have a similar or even bigger contribution to the total variance of a circuit [88]. Spatial correlation due to both D2D and WID can be included by assigning a large \( CD \) for D2D and a smaller one for WID [88]. Spatial correlation due to different WID-D2D relationships can be estimated with equations (3.8) to (3.10).

\[
\rho_{\text{WID}}(P_A, P_B) = k_{\text{WID}} \exp \left( -\frac{R_{AB}}{CD_{\text{WID}}} \right) \quad (3.8)
\]

\[
\rho_{\text{D2D}}(P_A, P_B) = k_{\text{D2D}} \exp \left( -\frac{R_{AB}}{CD_{\text{D2D}}} \right) \quad (3.9)
\]

\[
\rho(P_A, P_B) = \rho_{\text{WID}}(P_A, P_B) + \rho_{\text{D2D}}(P_A, P_B) \quad (3.10)
\]

where \( \rho(P_A, P_B) \) represents the total correlation between grids \( A \) and \( B \), \( \rho_{\text{WID}} \) and \( \rho_{\text{D2D}} \) represents the correlation due to WID and D2D variations, respectively. The terms \( K_{\text{WID}} \) and \( K_{\text{D2D}} \) are factors that establish the percentage of total variation assigned to WID and D2D variations respectively; meanwhile, \( CD_{\text{WID}} \) and \( CD_{\text{D2D}} \) represents the considered correlation distance for each class of variation.

### 3.2.4 Structural Correlation

Another class of correlation is generated by the topology of the circuit, and is known as structural correlation. For instance, in the circuit of Figure 3.8, there are three paths presenting structural correlation \( A = \{1, 2, 4\} \), \( B = \{1, 3, 4\} \) and \( C = \{3, 4\} \). Paths \( A \) and \( B \) share gates 1 and 4, due to this, all deviations at those gates will affect both paths with the exact same
magnitude. On the other hand, path C only shares gate 4 with path A, thus the correlation between C and A, is expected to be lower than between paths A and B.

![Figure 3.8](image)

Figure 3.8: Multiple correlated paths due to structural correlation.

When two paths are structurally correlated, its relationship can have two forms. First consider paths A and B, the inputs of paths A and B are the same (inputs of gate 1) and they are propagated up to gate 4, this means that inputs of gate 4 are highly correlated. In this case, the structural correlation is due to the shared gates 1 and 4. This specific case of structural correlation is known as re-convergent fanout. On the other hand, paths A and C shares only gate 4 but not their primary inputs, which means that the only contribution of structural correlation to inter-path correlation is due to shared gate 4.

Re-convergent fan-out is a very important phenomenon that must be considered in order to have an accurate estimation of circuit delay performance. However, the effect of re-convergent fan-out, is only visible when the output delay is estimated using statistical operator MAX, as in the MAX computation the correlation between input signals is critical. In contrast, when inter-path correlation is the main concern, re-convergent fan-out plays no role in the analysis as both paths are considered sensitized and isolated. Nevertheless, the existence of re-convergent fan-out implies the existence of strong structural correlation and should be considered in the analysis.

### 3.2.4.1 Random Variations in the Presence of Structural Correlation

As mentioned in section 3.2.2, random variations (such as RDF) are those that do not present spatial correlation, and they are different and independent for each device. This kind of
variation reduces dramatically the correlation between two gates, because even if both gates are very close, the variability of dopants in one gate is completely uncorrelated with the variability in the other. Nevertheless, in the presence of structural correlation certain gates are common to both paths, this implies that their random variations contribute by equal with the variance in each path. In other words, when random variations occur in uncorrelated paths, they decrease the inter-path correlation; but when they appear in structurally correlated paths, their random behavior have the exact same effect on the variance of both paths.

As a result, the appearance of structural correlation can be considered as an indicative of high inter-path correlation, and the effects of random variations in the inter-path correlation are alleviated.

### 3.3 Computing Inter-Path Correlation

Inter-path correlation is computed using a path-based statistical timing analysis [29]. Therefore, the analysis must be implemented on sensitized and isolated paths which were previously selected. Recalling equation (2.2), in order to estimate inter-path delay correlation each path delay distribution and the covariance between them must be estimated, including random and systematic variations as well as spatial and structural correlation between variables. However, before estimating the inter-path covariance and each path variance, the delay of each gate in the paths must be estimated in order to compute the propagation delay of each path. This section shows each one of the steps that must be followed to estimate inter-path correlation.

#### 3.3.1 Gate Delay Model

Generating the gate delay models is considered the first step of the analysis as it generates the statistical gate delay cells that will be used in the SSTA. In a common STA analysis, each gate delay cell is generated by characterizing the delay of each gate as function of input transition time and gate fan-out. In SSTA analysis, the delay variability of a gate must also
be characterized. The output transition time $t_r$ is characterized as a function of output load $C_L$ using SPICE simulations. The fan-in characteristics of each gate is stored in the \textit{fan-in table} (FNT).

The delay of a gate is a function of random variables, whose behavior has to be described with a probability distribution. A random function $Y(X_1 \cdots X_n)$ can be represented as a \textit{linear combination of random variables} (LCRV) [72], as follows

\begin{equation}
D = D_0 + s_1X_1 + s_2X_2 + \cdots + s_nX_n \tag{3.11}
\end{equation}

\begin{equation}
D = D_0 + \sum_{i=1}^{k} s_iX_i \tag{3.12}
\end{equation}

where $D_0$ represents the nominal delay value, $s_i$ is the delay sensitivity coefficient to variations in the $i$-th process parameter of $X_i$. Each variable $X$ represents the variations of the parameters that affect delay performance in a circuit ($L$, $W$, $T_{ox}$ and $V_{th}$). Such variations can be systematic or random (for the case of random dopant fluctuation). The mean and variance of (3.12) can be expressed as follows

\begin{equation}
\mu_D = D_0 \tag{3.13}
\end{equation}

\begin{equation}
\sigma^2_D = s_1^2\sigma^2_{X_1} + s_2^2\sigma^2_{X_2} + \cdots + s_n^2\sigma^2_{X_n} = \sum_{i=1}^{k} s_i^2\sigma^2_{X_i} \tag{3.14}
\end{equation}

In consequence it is necessary to estimate the corresponding gate’s sensitivity to each process parameter and its nominal delay. In this work, each gate sensitivity and nominal delay is pre-characterized with SPICE simulations. The sensitivity of each gate to each of the parameters under consideration is computed from simulation data using the topology set-up shown in Figure 3.9. The box in the middle of the topology will be substituted by each of the gates that will be characterized. The delay performance of each gate will be simulated for a rising and falling transition on each of its input pins at a time, where the rest of the pins will be connected to the rail that sensitizes the gate (i.e. GND for OR-gates, VDD for AND-Gates, etc.). This will generate two delay measurements, rising and falling, for each of the gate’s \textit{pin-to-pin} delay.
3.3 Computing Inter-Path Correlation

Each of the gate pin-to-pin delay will be measured for different input transition time (both rising and falling) and for different values of output load. The nominal pin-to-pin delay of each gate will be approximated by a polynomial that fits the delay behavior as a function of the input transition time and output load. For the case of parameter sensitivities, the pin-to-pin delay of the gates is measured for different values of the parameters under consideration (L, W, T_{ox}, V_{th}, etc). The sensitivity of each parameter will be computed using simulation data from Monte-Carlo simulations on each parameter separately; at the end the sensitivity of each parameter is approximated by the derivative of the polynomial that fits the delay behavior as a function of the parameter variation, input transition time and output load [98]. For simplicity, all the transistors in a gate will be considered to be placed very close to each other, which made them fully correlated for systematic variations. Therefore, each circuit is analyzed at a gate level and each gate is described by its pin-to-pin delay, as shown in Figure 3.10.

For the case of RDF fluctuations they are represented as a fluctuation in the threshold voltage of the gate [89]. Therefore, the sensitivity of each gate to RDF is equal to the sensitivity to V_{th} whose computation was previously addressed in Figure 3.9. However, RDF fluctuations contribute to pin-to-pin delay distribution differently depending on the transistor size. To address this problem, the contribution of RDF on each active transistor to the overall pin-to-pin delay is computed using equation (3.1) and the contribution of each transistor is accumulated [89] and then considered as a total gate RDF fluctuation. The RDF contribution is characterized for every pin-to-pin delay on each gate and is stored in a look-up table (RDF-LT).
3.3.2 Paths Delay Distributions

Once each gate delay is modeled, the next step is to propagate that delay from the primary inputs to the primary outputs. As mentioned earlier, the present work uses a path-based approach to compute inter-path covariance. Therefore, the delay propagation is made, as in any path-based analysis, using the statistical operator SUM that can be described as follows [47]

\[ Z = X + Y = \text{SUM}(X, Y) \]
\[ \mu_Z = \mu_X + \mu_Y \]
\[ \sigma^2_Z = \sigma^2_X + \sigma^2_Y + 2\text{COV}(X, Y) \]  

(3.15)

Using each gate function and the statistical operator SUM described is possible to estimate each path delay distribution. As an example, consider path \( P \), that is conformed by two gates \((G_1, G_2)\) as shown in Figure 3.11.

Every gate delay can be expressed as a linear function like shown in equations (3.16) to
3.3 Computing Inter-Path Correlation

Figure 3.11: Path under test to show the propagation of delay distribution.

(3.17), where $D_i$ represents the delay distribution of the $i$-th gate $G_i$.

$$D_1 = D_{1,0} + \sum_{i=1}^{k} s_{1,i} X_{1,i}$$  \hspace{1cm} (3.16)

$$D_2 = D_{2,0} + \sum_{i=1}^{k} s_{2,i} X_{2,i}$$  \hspace{1cm} (3.17)

where $k$ represents the number of gates in the path, $D_{j,0}$ represents the nominal gate delay of the $j$-th gate, $s_{j,i}$ represents the sensitivity of the $j$-th gate to the variations in the $i$-th parameter $X$. The parameter $X_{j,i}$ represents the variation of the $i$-th parameter on the $j$-th gate.

The first step for delay propagation is to establish the arrival time ($A_n$) at the input node of the path. The output delay of gate $G_1$ is computed adding the arrival time at the input node of $G_1$ ($A_{n,in}$) and the pin-to-pin delay distribution of $G_1$ ($D_1$). Usually the delay of the input signal is assumed as a constant signal (zero mean and variance), which implies that $A_{n,1} = D_1$. The arrival time at the output node ($A_{n,out}$) can be estimated in a similar way, adding the arrival time $A_{n,1}$ and the pin-to-pin delay of gate $G_2$ ($D_2$). This can be made using equations (3.13) and (3.14) on the gate delay functions (3.16) and (3.17). The mean and variance of the output delay of the path can be obtained as follows.

$$D_p = SUM(A_{n,1}, D_2) = SUM(D_1, D_2)$$

$$\mu_{D_p} = \mu_{D_1} + \mu_{D_2} = D_{1,0} + D_{2,0}$$  \hspace{1cm} (3.18)

$$\sigma_{D_p}^2 = \sigma_{D_1}^2 + \sigma_{D_2}^2 + 2 \sum_{i=1}^{k} s_{1,i} s_{2,i} COV(X_{1,i}, X_{2,i})$$  \hspace{1cm} (3.19)

As can observed in equation (3.18), the mean path delay is computed as the accumulation
Chapter 3: Computing the Degree of Inter-Path Correlation

of all the nominal gate delays in the path. On the other hand, variance is a quite more complex expression that involves the variance of each gate and the covariance between them. The variance of each gate is data known from the gate model characterized previously, but the covariance term refers to the spatial relationship that exist between the parameter variation of each gate. In order to consider the covariance between gates, the spatial correlation model described in section 3.2.3.2 is used. In Figure 3.12 the circuit of Figure 3.11 have been divided in 2 numbered grids (I ··· II), one for each gate. Equation (3.19) can be re-written to consider the spatial location of each gate as follows

\[
\sigma^2_{D_P} = \sigma^2_{D_1} + \sigma^2_{D_2} + 2 \sum_{i=1}^{k} s_{1,i}s_{2,i} \text{COV}(X_{I,i}, X_{II,i}) 
\]

(3.20)

where \(X_{j,i}\) represents the \(i\)-th parameter at the \(j\)-th location (Note: subindex \(j\) will be used to refer to grid location of a gate). The covariance between two gates, can be computed as the covariance between two LCRV as shown in theorem 2.

\textbf{Theorem 2.} Considering two linear combinations of random variables of the form:

\[
A = a_0 + a_1X_1 + a_2X_2 + \cdots + a_kX_k 
\]

(3.21)

\[
B = b_0 + b_1X_1 + b_2X_2 + \cdots + b_kX_k 
\]

(3.22)

where \(a_i\) represents the sensitivity of the function to the \(i\)-th variable \(X\). The covariance
3.3 Computing Inter-Path Correlation

**COV(A, B) can be calculates as**

\[
\text{COV}(A, B) = a_1 b_1 \text{COV}(X_1, X_1) + a_2 b_2 \text{COV}(X_2, X_2) + \cdots + a_k b_k \text{COV}(X_k, X_k)
\]

\[
\text{COV}(A, B) = a_1 b_1 \sigma^2_{X_1} + a_2 b_2 \sigma^2_{X_2} + \cdots + a_k b_k \sigma^2_{X_k}
\]

\[
\text{COV}(A, B) = \sum_{j=1}^{k} \sum_{i=1}^{k} a_i b_j \text{COV}(X_i, X_j) \tag{3.23}
\]

Using theorem 2 and the spatial model of Figure 3.12, the covariance of delay between gates \(G_1\) and \(G_2\) can be computed as follows

\[
\text{COV}(D_1, D_2) = \sum_{i=1}^{k} s_{1,i} s_{2,i} \text{COV}(X_{I,i}, X_{II,i}) \tag{3.24}
\]

where \(\text{COV}(X_{I,i}, X_{II,i})\) represents the spatial correlation between devices in locations \(I\) and \(II\), and which can be computed using the spatial correlation model described in section 3.2.3.2. Equation (3.24) is a reduced version of equation (3.23) as it only includes the covariance between the same parameters but in different locations; in other words, the correlation between different parameters in different locations is neglected. When a path longer than two gates is analyzed, the propagation process must consider the spatial correlation of all the gates in the path. In other words, for the last gates the correlation of the previous gates is needed.

**Example:**

Consider the path shown in Figure 3.13, in which the output delay distribution can be computed as in equation (3.25) which involves the arrival time \(A_{n,k-1}\) and the pin-to-pin delay \(D_k\).

\[
\sigma^2_{D_k} = \sigma^2_{D_j} + \sigma^2_{A_{n,i-1}} + 2 \sum_{j=i+1}^{k} \sum_{i=1}^{k} s_{k,i} s_{k-1,j} \text{COV}(D_k, A_{n,k-1}) \tag{3.25}
\]

The problem of propagating delay through multiple gates (more than two) is to compute \(\text{COV}(D_k, A_{n,k-1})\), which is not straightforward because the arrival time \(A_n\) is not a LCRV
anymore. Nevertheless, $A_{n,k-1}$ can be represented as $A_{n,k-2} + D_{k-1}$ which represents a similar problem as $A_{n,k-2}$ is not a LCRV either. This problem is presented in equations (3.26) to (3.28).

$$A_{n,j-1} = A_{n,j-2} + D_{j-1} \quad (3.26)$$
$$A_{n,j-2} = A_{n,j-3} + D_{j-2} \quad (3.27)$$
$$\vdots$$
$$A_{n,1} = A_{n,n} + D_1 = D_1 \quad \text{if } \sigma_{A_{n,n}} = 0$$
$$\therefore A_{n,j-1} = D_k + D_{k-1} + \cdots + D_1 \quad (3.28)$$

Using equations (3.26) to (3.28), the covariance between $D_j$ (or the delay of any gate in the middle of the path) and $A_{n,j-1}$ (the delay distribution of the previous gates in the path) can be computed using the additivity property of covariance ($COV(A, B + C) = COV(A, B) + COV(A, C)$) [72] as in equation (3.29)

$$COV(D_k, A_{n,k-1}) = COV(D_k, D_{k-1} + D_{k-2} + \cdots + D_1)$$
$$COV(D_k, A_{n,k-1}) = COV(D_k, D_{k-1}) + COV(D_k, D_{k-2}) + \cdots + COV(D_k, D_1) \quad (3.29)$$

Equation (3.29) implies that in order to account the spatial correlation between gates in a path, it is necessary to know the correlation between the current gate and all the previous gates. Therefore, the correlation information between each gate in the path must be accumu-
lated. This problem is addressed using a path-global correlation matrix (PGC), that stores the correlation information between each gate as shown in equation (3.30). Each of the coefficients in equation 3.30 can be computed using matrix (3.24)

\[
PGC = \begin{bmatrix}
\sigma^2_{D_1} & COV(D_1, D_2) & COV(D_1, D_3) & \cdots & COV(D_1, D_k) \\
COV(D_2, D_1) & \sigma^2_{D_2} & COV(D_2, D_3) & \cdots & COV(D_2, D_k) \\
COV(D_3, D_1) & COV(D_3, D_2) & \sigma^2_{D_3} & \cdots & COV(D_3, D_k) \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
COV(D_k, D_1) & COV(D_k, D_2) & COV(D_k, D_3) & \cdots & \sigma^2_{D_k}
\end{bmatrix}
\] (3.30)

### 3.3.3 Inter-Path Covariance

The relationship that exist between two paths variations is commonly expressed as correlation in order to simplify its analysis. To estimate inter-path correlation, inter-path covariance must be estimated first. Similarly to each path delay distribution, the inter-path covariance is computed using the standard cells previously characterized. The inter-path covariance is computed adding the covariance of each combination of gates between paths. As an example, consider the two paths \(PA\) and \(PB\) shown in Figure 3.14. Every gate delay can be expressed as a linear function like shown in equations (3.31) to (3.34), where \(D_i\) represents the delay distribution of the \(i\)-th gate.

![Figure 3.14: Paths under test to show the inter-path estimation methodology.](image)
Chapter 3: Computing the Degree of Inter-Path Correlation

\[ D_1 = D_{1,0} + \sum_{i=1}^{n} s_{1,i} X_{I,i} \quad (3.31) \]

\[ D_2 = D_{2,0} + \sum_{i=1}^{n} s_{2,i} X_{II,i} \quad (3.32) \]

\[ D_3 = D_{3,0} + \sum_{i=1}^{n} s_{3,i} X_{III,i} \quad (3.33) \]

\[ D_4 = D_{4,0} + \sum_{i=1}^{n} s_{4,i} X_{IV,i} \quad (3.34) \]

where \( D_{j,0} \) represents the nominal gate delay of the \( j \)-th gate, \( s_{j,i} \) represents the sensitivity of the \( j \)-th gate to the \( i \)-th parameter and \( X_{j,i} \) represents the \( i \)-th parameter variation in the \( j \)-th grid. The parameter \( X \) may represent fluctuations in either systematical (\( L,W, T_{ox}, V_{th} \)) or random variables (RDF); the only difference in how to treat random or systematical variables is the fact that the correlation between random variables and any other variable will be zero.

The inter-path covariance between paths \( PA \) and \( PB \) can be estimated as follows:

\[
COV(D_{PA}, D_{PB}) = COV(D_1 + D_2, D_3 + D_4) \\
= COV(D_1, D_3) + COV(D_1, D_4) \\
+ COV(D_2, D_3) + COV(D_2, D_4) 
\quad (3.35)
\]

where \( D_i \) represents the linearized delay function of the \( i \)-th gate, similar to (3.31)-(3.34).

Equation 3.35 can be extended to paths with \( k \) gates like the shown in Figure 3.15 using equation (3.36).

![Figure 3.15: Two paths (PA and PB) conformed by k gates.](image)
3.3 Computing Inter-Path Correlation

\[ COV(D_{PA}, D_{PB}) = COV(D_{A,1} + D_{A,2} + \cdots + D_{A,k}, D_{B,1} + D_{B,2} + \cdots + D_{B,k}) \]
\[ = \sum_{j=1}^{k} \sum_{i=1}^{k} COV(D_{A,i}, D_{B,j}) \]  
\[ (3.36) \]

where \( D_{ji} \) represents the delay distribution of the \( i \)-th gate of the \( j \)-th path. The covariance between each pair of gates can be estimated using equation (3.23). Once the covariance between two paths is known, the inter-path correlation can be computed as

\[ \rho_{(D_{PA}, D_{PB})} = \frac{COV(D_{PA}, D_{PB})}{\sigma_{D_{PA}}\sigma_{D_{PB}}} \]  
\[ (3.37) \]

**Structurally correlated Case**

For the case when two paths are structurally correlated, the inter-path covariance estimation is very similar. For instance, consider Figure 3.16 as an example of structural correlation where gate \( G_1 \) is common for both paths. Hence, all the process variations (systematic and random) that affect gate \( G_1 \) will contribute to both path A and B delay distributions, and also to inter-path covariance.

![Figure 3.16: Example of structurally correlated paths.](image)

For this particular topology, the inter-path covariance is given by

\[ COV(D_{PA}, D_{PB}) = COV(D_1 + D_2, D_1 + D_3) \]
\[ = COV(D_1, D_1) + COV(D_1, D_3) + COV(D_2, D_1) + COV(D_2, D_3) \]  
\[ (3.38) \]
where the term $\text{COV}(D_1, D_1)$ can be simplified considering that $\text{COV}(D_1, D_1) = \sigma^2_{D_1}$, modifying equation (3.38) as follows.

$$\begin{align*}
\text{COV}(D_{PA}, D_{PB}) &= \text{COV}(D_1 + D_2, D_1 + D_3) \\
&= \sigma^2_{D_1} + \text{COV}(D_1, D_3) + \text{COV}(D_2, D_1) + \text{COV}(D_2, D_3) \\
&= \sigma^2_{D_1} + \text{COV}(D_1, D_3) + \text{COV}(D_2, D_1) + \text{COV}(D_2, D_3)
\end{align*}$$

(3.39)

### 3.4 Inter-Path Correlation Implementation

The standard-cell statistical characterization was made using HSPICE Monte-Carlo simulation at 200 iterations. There were considered 11 gates for a total of 27 pin-to-pin delays, automatically generated by Mentor Graphic’s IC-Studio in a TSMC 0.18\(\mu\)m technology. On the characterization, variability of $\pm 15\%$ was considered on $L$, $W$, $T_{ox}$, $V_{thn}$ and $V_{thp}$.

The inter-path correlation estimation framework was implemented in MATLAB. The paths under analysis are parsed from an input net-list that contains the gates’ interconnection and location information. Using the standard cells pre-characterized, each path delay distribution and inter-path covariance are computed. Finally, using the inter-path covariance and paths’ delay distributions the inter-path correlation is computed. The MATLAB program is described on Algorithm 1.
Algorithm 1 Inter-path correlation estimation

1: Read: Path_1.Netlist. \{G_{1,1}, \ldots, G_{2,n}\}
2: Read: Path_2.Netlist. \{G_{1,1}, \ldots, G_{2,m}\}
3: Read: Inputs transition times \(t_r(1,0)\) and \(t_r(2,0)\)
4: Load: technology’s parameter sensitivities \(S(t_r, C_L)\), gates output transition time \(t_r(C_L)\)
5: Load: gates output transition time characteristics \(t_r(C_i)\)
6: Load: gates fan-in table (FIT)
7: Load: technology RDF gate characteristics (RDF-LT).
8: for \(i \leftarrow 1, 2\) do \(\triangleright\) Estimates capacitive load and transition time at each node
9: \hspace{1em} for \(j \leftarrow 1, \text{Number gates path}_i\) do
10: \hspace{2em} \text{CL}_\text{node}_i(i,j)=\sum \text{of fan-ins connected to node (i,j)}
11: \hspace{2em} \text{t}_\text{node}_i(i,j)=t_r(\text{CL}_\text{node}_i(i,j))
12: \hspace{1em} end for
13: end for
14: for \(i \leftarrow 1, 2\) do \(\triangleright\) Estimates PCG matrix
15: \hspace{1em} for \(j \leftarrow 2, \text{Number gates path}_i\) do
16: \hspace{2em} \text{PCG}_i(j-1,j)=\text{COV}(G_{i,j}, G_{i,j})
17: \hspace{1em} end for
18: end for
19: for \(i \leftarrow 1, 2\) do \(\triangleright\) Estimates paths delay distribution
20: \hspace{1em} for \(j \leftarrow 0, \text{Number gates path}_i\) do
21: \hspace{2em} \mu_i\text{+delay of } D_{i,j}(t_{r_{i,j}}, C_{L_{i,j}})
22: \hspace{2em} if \(j > 1\) then
23: \hspace{3em} \sigma_i^2\text{+variance of } D_{i,j}(t_{r_{i,j}}, C_{L_{i,j}})+\text{PCG}_i(j-1,j)
24: \hspace{2em} else
25: \hspace{3em} \sigma_i^2\text{+variance of } D_{i,j}(t_{r_{i,j}}, C_{L_{i,j}})
26: \hspace{2em} end if
27: \hspace{2em} end for
28: end for
29: for \(i \leftarrow 1, n\) do \(\triangleright\) Inter-path covariance estimation
30: \hspace{1em} for \(j \leftarrow 1, m\) do
31: \hspace{2em} ip.cov+\text{COV}(D_{1,j}, D_{2,j})
32: \hspace{2em} end for
33: end for
34: \text{Inter-path correlation}=\frac{ip.cov}{\sigma_1 \sigma_2}
3.5 Conclusions

An SSTA tool capable of calculating the correlation information between two paths was implemented in MATLAB. The SSTA framework generated, considers statistical standard cells that includes variations in systematic variables $L$, $W$, $T_{ox}$, $V_{tn}$ and $V_{thp}$ and accounts for the effects of random dopant fluctuations modeled as a random variable for each standard cell. Spatial correlation was considered by implementing an analytical spatial model suitable for scaling, which accounts for the effects of WID and D2D variations independently. The effects of structural correlation were analyzed and included in the analysis considerations.
3.5 Conclusions
Chapter 4

Simulation Results

As shown in chapter 2, the proposed methodology relies on the degree of inter-path correlation of the CUT’s selected paths. In this chapter an analysis of the behavior of inter-path correlation is presented and results for typical logic circuits and benchmark ISCAS circuit are presented. This chapter is structured as follows: Section 4.1 analysis the behavior of inter-path correlation for different circuit conditions. Section 4.2 shows the results of implementing the proposed methodology on selected paths from benchmark circuits. Section 4.3 propose a group of heuristic objectives and restrictions to select paths with the highest correlation available. Section 4.4 shows the conclusions of this chapter.

4.1 Inter-Path Correlation Behavioral Analysis

As shown in chapter 3, the behavior of inter-path correlation depends on the structure and conditions of the circuit. An accurate characterization of the standard cells used to build the benchmark circuits is made to allow proper inter-path correlation estimation.

4.1.1 SSTA Framework Gate Cells Validation

Each gate was modeled using standard cells generated by Mentor Graphics in TSMC 0.18µm technology. Sensitivities and nominal delays were characterized using SPICE simulations.
These are used to obtain the mean and standard deviation of the gate delays. The characteristics of each gate cell used by the SSTA framework (SSTAF), which estimates the inter-path correlation degree, were validated using Monte-Carlo analysis considering ±15% of variation in L, W, $T_{ox}$ and $V_{th}$ at 10,000 iterations. The error on delay mean and standard deviation of each gate are shown in Table 4.1 when a rising transition is present at the input pin of the gate, and in Table 4.2 for a falling transition at the input of the gate.

<table>
<thead>
<tr>
<th>Gate Cell</th>
<th>Input pin</th>
<th>SPICE $\mu_D$ (ps)</th>
<th>SSTAF $\mu_D$ (ps)</th>
<th>Error (%)</th>
<th>SPICE $\sigma_D$ (ps)</th>
<th>SSTAF $\sigma_D$ (ps)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td>1</td>
<td>7.575</td>
<td>7.566</td>
<td>0.119</td>
<td>4.3</td>
<td>4.301</td>
<td>0.023</td>
</tr>
<tr>
<td>AND02</td>
<td>1</td>
<td>94.205</td>
<td>94.189</td>
<td>0.017</td>
<td>5.44</td>
<td>5.417</td>
<td>0.423</td>
</tr>
<tr>
<td>AND02</td>
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<td>102.11</td>
<td>102</td>
<td>0.108</td>
<td>6.057</td>
<td>6.044</td>
<td>0.215</td>
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<tr>
<td>AND03</td>
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<td>101.14</td>
<td>101.02</td>
<td>0.119</td>
<td>5.843</td>
<td>5.851</td>
<td>0.137</td>
</tr>
<tr>
<td>AND03</td>
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<td>109.98</td>
<td>109.82</td>
<td>0.145</td>
<td>6.507</td>
<td>6.484</td>
<td>0.353</td>
</tr>
<tr>
<td>AND03</td>
<td>3</td>
<td>116.21</td>
<td>116.02</td>
<td>0.163</td>
<td>7.021</td>
<td>7.007</td>
<td>0.199</td>
</tr>
<tr>
<td>NAND02</td>
<td>1</td>
<td>70.755</td>
<td>70.673</td>
<td>0.116</td>
<td>4.0478</td>
<td>4.0403</td>
<td>0.185</td>
</tr>
<tr>
<td>NAND02</td>
<td>2</td>
<td>77.994</td>
<td>77.905</td>
<td>0.114</td>
<td>4.566</td>
<td>4.55</td>
<td>0.350</td>
</tr>
<tr>
<td>NAND03</td>
<td>1</td>
<td>71.746</td>
<td>71.663</td>
<td>0.116</td>
<td>4.12</td>
<td>4.112</td>
<td>0.194</td>
</tr>
<tr>
<td>NAND03</td>
<td>2</td>
<td>82.657</td>
<td>82.553</td>
<td>0.126</td>
<td>4.945</td>
<td>4.928</td>
<td>0.344</td>
</tr>
<tr>
<td>NAND03</td>
<td>3</td>
<td>90.852</td>
<td>90.735</td>
<td>0.129</td>
<td>5.547</td>
<td>5.521</td>
<td>0.469</td>
</tr>
<tr>
<td>NAND04</td>
<td>1</td>
<td>68.497</td>
<td>68.425</td>
<td>0.105</td>
<td>3.585</td>
<td>3.602</td>
<td>0.474</td>
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<tr>
<td>NAND04</td>
<td>2</td>
<td>80.338</td>
<td>80.235</td>
<td>0.128</td>
<td>4.812</td>
<td>4.791</td>
<td>0.436</td>
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<tr>
<td>NAND04</td>
<td>3</td>
<td>89.697</td>
<td>89.575</td>
<td>0.136</td>
<td>5.537</td>
<td>5.509</td>
<td>0.506</td>
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<tr>
<td>NAND04</td>
<td>4</td>
<td>96.192</td>
<td>96.075</td>
<td>0.122</td>
<td>6.017</td>
<td>5.987</td>
<td>0.499</td>
</tr>
<tr>
<td>NOR02</td>
<td>1</td>
<td>101.8</td>
<td>101.7</td>
<td>0.098</td>
<td>6.077</td>
<td>6.047</td>
<td>0.494</td>
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<tr>
<td>NOR02</td>
<td>2</td>
<td>108.62</td>
<td>109.03</td>
<td>0.377</td>
<td>6.58</td>
<td>6.52</td>
<td>0.912</td>
</tr>
<tr>
<td>NOR03</td>
<td>1</td>
<td>115.02</td>
<td>114.9</td>
<td>0.104</td>
<td>6.951</td>
<td>6.899</td>
<td>0.748</td>
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<tr>
<td>NOR03</td>
<td>2</td>
<td>139.38</td>
<td>139.82</td>
<td>0.316</td>
<td>8.641</td>
<td>8.595</td>
<td>0.532</td>
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<tr>
<td>NOR03</td>
<td>3</td>
<td>146.72</td>
<td>145.823</td>
<td>0.611</td>
<td>9.149</td>
<td>9.072</td>
<td>0.842</td>
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<tr>
<td>OR02</td>
<td>1</td>
<td>153.17</td>
<td>152.9</td>
<td>0.176</td>
<td>10.091</td>
<td>10.006</td>
<td>0.842</td>
</tr>
<tr>
<td>OR02</td>
<td>2</td>
<td>166.43</td>
<td>165.12</td>
<td>0.787</td>
<td>10.749</td>
<td>10.647</td>
<td>0.949</td>
</tr>
<tr>
<td>XNORF02</td>
<td>1</td>
<td>88.998</td>
<td>88.195</td>
<td>0.902</td>
<td>5.356</td>
<td>5.329</td>
<td>0.504</td>
</tr>
<tr>
<td>XNORF02</td>
<td>2</td>
<td>79.549</td>
<td>78.876</td>
<td>0.846</td>
<td>4.7932</td>
<td>4.755</td>
<td>0.797</td>
</tr>
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<td>XNORR02</td>
<td>1</td>
<td>125.8</td>
<td>124.82</td>
<td>0.779</td>
<td>7.04</td>
<td>6.987</td>
<td>0.753</td>
</tr>
<tr>
<td>XNORR02</td>
<td>2</td>
<td>138.56</td>
<td>137.82</td>
<td>0.534</td>
<td>7.99</td>
<td>7.92</td>
<td>0.876</td>
</tr>
<tr>
<td>BUFF</td>
<td>1</td>
<td>103.35</td>
<td>103.22</td>
<td>0.126</td>
<td>6.254</td>
<td>6.27</td>
<td>0.256</td>
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</table>

Table 4.1: Average mean and standard deviation error for the pre-characterized gate cells used by SSTA framework considering an input rising transition.
As can be observed in tables 4.1 and 4.2, the cells pre-characterized have a mean’s average error of 0.275% for rising transition and 0.308% for falling transition, and an STD average error of 0.493% on rising transition and 0.467% for falling transition. Therefore, the standard cells can be used to observe the behavior of inter-path correlation for different circuit’s conditions. The analysis considers spatial distribution of components, structural correlation of paths under analysis and the effects of paths’ length. Each of the previous conditions is analyzed for different WID-D2D relationships and RDF effects.

<table>
<thead>
<tr>
<th>Gate Cell</th>
<th>Input pin</th>
<th>SPICE $\mu_D$ (ps)</th>
<th>SSTAF $\mu_D$ (ps)</th>
<th>Error (%)</th>
<th>SPICE $\sigma_D$ (ps)</th>
<th>SSTAF $\sigma_D$ (ps)</th>
<th>Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV</td>
<td>1</td>
<td>66.455</td>
<td>66.401</td>
<td>0.081</td>
<td>3.638</td>
<td>3.629</td>
<td>0.247</td>
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<td>AND02</td>
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<td>112.48</td>
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<td>116.2</td>
<td>116.62</td>
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<td>6.768</td>
<td>0.280</td>
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<tr>
<td>AND03</td>
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<td>140.77</td>
<td>140.52</td>
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<td>8.415</td>
<td>8.389</td>
<td>0.309</td>
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<tr>
<td>AND03</td>
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<td>148.31</td>
<td>149.32</td>
<td>0.681</td>
<td>8.888</td>
<td>8.859</td>
<td>0.326</td>
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<td>AND03</td>
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<td>151.28</td>
<td>0.126</td>
<td>9.056</td>
<td>9.1</td>
<td>0.486</td>
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<td>NAND02</td>
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<td>62.213</td>
<td>62.141</td>
<td>0.116</td>
<td>2.992</td>
<td>2.977</td>
<td>0.501</td>
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<tr>
<td>NAND02</td>
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<td>65.178</td>
<td>65.801</td>
<td>0.956</td>
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<td>3.207</td>
<td>0.250</td>
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<td>NAND03</td>
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<td>65.481</td>
<td>65.381</td>
<td>0.153</td>
<td>3.13</td>
<td>3.107</td>
<td>0.735</td>
</tr>
<tr>
<td>NAND03</td>
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<td>72.751</td>
<td>72.97</td>
<td>0.301</td>
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<td>3.576</td>
<td>0.732</td>
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<tr>
<td>NAND03</td>
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<td>NAND04</td>
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<td>74.6</td>
<td>0.150</td>
<td>3.585</td>
<td>3.557</td>
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<tr>
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<td>86.867</td>
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<td>4.312</td>
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<td>92.011</td>
<td>0.545</td>
<td>4.671</td>
<td>4.702</td>
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<tr>
<td>NAND04</td>
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<td>95.074</td>
<td>95.998</td>
<td>0.972</td>
<td>4.854</td>
<td>4.881</td>
<td>0.556</td>
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<tr>
<td>NOR02</td>
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<td>75.865</td>
<td>75.803</td>
<td>0.082</td>
<td>4.219</td>
<td>4.206</td>
<td>0.308</td>
</tr>
<tr>
<td>NOR02</td>
<td>2</td>
<td>86.681</td>
<td>86.601</td>
<td>0.092</td>
<td>4.964</td>
<td>4.949</td>
<td>0.302</td>
</tr>
<tr>
<td>NOR03</td>
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<td>3.965</td>
<td>3.961</td>
<td>0.101</td>
</tr>
<tr>
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<td>91.44</td>
<td>91.381</td>
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<td>5.028</td>
<td>5.017</td>
<td>0.219</td>
</tr>
<tr>
<td>NOR03</td>
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<td>99.937</td>
<td>99.86</td>
<td>0.077</td>
<td>5.542</td>
<td>5.547</td>
<td>0.090</td>
</tr>
<tr>
<td>OR02</td>
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<td>88.267</td>
<td>88.191</td>
<td>0.086</td>
<td>4.883</td>
<td>4.92</td>
<td>0.758</td>
</tr>
<tr>
<td>OR02</td>
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<td>95.519</td>
<td>95.403</td>
<td>0.121</td>
<td>5.31</td>
<td>5.36</td>
<td>0.942</td>
</tr>
<tr>
<td>XNORF02</td>
<td>1</td>
<td>96.569</td>
<td>96.601</td>
<td>0.033</td>
<td>5.052</td>
<td>5.063</td>
<td>0.218</td>
</tr>
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<td>XNORF02</td>
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<td>80.476</td>
<td>79.87</td>
<td>0.753</td>
<td>4.022</td>
<td>4.019</td>
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<td>XNORR02</td>
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<td>138.53</td>
<td>138.32</td>
<td>0.152</td>
<td>8.223</td>
<td>8.278</td>
<td>0.669</td>
</tr>
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<td>XNORR02</td>
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<td>141.05</td>
<td>141.9</td>
<td>0.603</td>
<td>8.528</td>
<td>8.584</td>
<td>0.657</td>
</tr>
<tr>
<td>BUFF</td>
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<td>99.378</td>
<td>99.249</td>
<td>0.130</td>
<td>6.133</td>
<td>6.196</td>
<td>1.027</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$\mu_D$ Average Error</th>
<th>$\sigma_D$ Average Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.308</td>
<td>0.467</td>
</tr>
</tbody>
</table>

Table 4.2: Average mean and standard deviation error for the pre-characterized gate cells used by SSTA framework considering an input falling transition.
4.1.2 Spatial Correlation

The experiment shown in this subsection is intended to show the behavior of the inter-path correlation as a function of the paths’ spatial location. In order to emphasize the effects of the spatial location of the paths, variations due to RDF are neglected and the analysis is made considering different WID-D2D relationships. This experiment will consider a ±15% variation on $L$, $W$, $T_{ox}$ and $V_{th}$. The paths under test (PUT) shown in Figure 4.1; the starting location of each gate, expressed in generic units of length (ul), is given in the $X$-$Y$ coordinate below.

![PUT diagram](image)

Figure 4.1: PUT used to analyze inter-path correlation behavior as a function of spatial correlation.

In this analysis, the behavior of inter-path correlation ($\rho_{AB}$) as a function of inter-path distance ($R_{AB}$) is analyzed. To show the effects of inter-path distance, the position of the path B is progressively shifted away from path A. The effects of increasing inter-path distance are summarized in Figure 4.2, and the same analysis is repeated for different WID-D2D relationships.

As can be observed in Figure 4.2, inter-path correlation is a function of the length of separation between paths and the WID-D2D relationships. From Figure 4.2, it can be observed that D2D variations creates an “off-set” on the inter-path correlation, this mean that even devices located far from each other will show a minimum degree of inter-path correlation [88].
Figure 4.2: Inter-path correlation behavior as a function of distance for different WID-D2D relationships.

In Figure 4.3, the same analysis is made including the effects of random dopant fluctuations. Figure 4.3 shows that inter-path correlation decreases when random variables (e.g. RDF) are considered. This behavior can be explained by looking at equation (3.37), where inter-path correlation is presented as a relationship between paths’ standard deviation and inter-path covariance. Considering that random variations increase paths delay variance but does not contribute to inter-path covariance, the overall effect is a reduction of inter-path correlation.

A similar analysis can explain the reduction of inter-path correlation as WID variations become the dominant kind of variations; the main effect of WID variations is the increase of each path variance without increasing the inter-path covariance.

Figure 4.3: Inter-path correlation behavior as a function of distance for different WID-D2D relationships, including RDF.
4.1.3 Structural Correlation

One of the most important aspects that contribute to inter-path correlation is the structural correlation. To analyze the behavior of inter-path correlation due to different degrees of structural correlation, the paths shown in Figure 4.4 will be considered. Paths in Figure 4.4 are two paths that for matter of analysis are constituted of the same number and kind of cells.

![PUT used to observe structural correlation effects on inter-path correlation behavior](image)

To show the effects of structural correlation on inter-path correlation, this analysis considers four different configurations:

- **Case 1**: Both paths are independent from each other, this means that the path do not share any gate.

- **Case 2**: The first gate of each path is shared between the them.

- **Case 3**: The first and second gates of each path are shared.

- **Case 4**: The first three gates are common to both paths.

In this experiment a WID-D2D relationship of 75-25 will be considered. Paths A and B in Figure 4.4 are placed as indicated in the X-Y coordinates below each gate. The inter-path
correlation for each of the previous cases are shown in Table 4.3. This is shown when RDF is considered and also when RDF is not considered.

<table>
<thead>
<tr>
<th>Case</th>
<th>$\rho$ (No-RDF)</th>
<th>$\rho$ (RDF)</th>
<th>Reduction (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.73815</td>
<td>0.68014</td>
<td>7.85</td>
</tr>
<tr>
<td>2</td>
<td>0.74332</td>
<td>0.6848</td>
<td>7.87</td>
</tr>
<tr>
<td>3</td>
<td>0.75143</td>
<td>0.69217</td>
<td>7.88</td>
</tr>
<tr>
<td>4</td>
<td>0.75719</td>
<td>0.6987</td>
<td>7.89</td>
</tr>
</tbody>
</table>

Table 4.3: Inter-path correlation for each case of structural correlation.

The structural correlation increases the inter-path correlation between the shared gates, which can be seen as a full correlation between paths. This can be easily understood by considering cases 1 and 2. In case 1, random variations between $G_1$ and $G_5$ are completely uncorrelated; meanwhile, systematic variations in $G_1$ are correlated with the variations in $G_5$ because of the spatial correlation between them. Systematic variations of $G_1$ and $G_5$ will never be fully correlated, as there will always be a distance between gates. On the other hand for case 2, systematic variations in $G_1$ and $G_5$ will be fully correlated as they are in fact the same gate; moreover, the random variations in $G_1$ will be the same for gate $G_5$ and will be fully correlated. A similar analysis can be made for cases 3 and 4, where the variations that appear on each pair of shared gates will be fully correlated. This means that effects of systematic and random variations on the shared gates are identical for both paths.

4.1.4 Path Length

To analyze the effects of path’s length on the inter-path correlation, paths shown in Figure 4.5 are considered. For simplicity, paths A and B will be constituted by the same type and number of gates, with a constant inter-path distance ($20\mu l$). The effects of RDF will be neglected for this experiment.

Figure 4.6 summarizes the effect of path length on inter-path correlation. To understand better this phenomenon, Figure 4.6 shows inter-path covariance ($\sigma_{AB}$), inter-path correlation ($\rho_{AB}$) and the product of $\sigma_A \times \sigma_B$ for different logical depths.
Figure 4.5: PUT used to observe the effects of path length on the inter-path correlation behavior.

Figure 4.6: Inter-path covariance ($\sigma_{AB}$), $\sigma_A \times \sigma_B$ and inter-path correlation ($\rho_{AB}$) behavior for different path lengths.

The inter-path correlation has an increasing behavior for very short paths, and then it starts decreasing as paths depth increases. This behavior can be explained by looking at the basic correlation equation shown in (2.2) which can be rewritten as in equation (4.1).

$$\rho_{AB} = \frac{COV(A, B)}{\sigma_A \times \sigma_B} = \frac{\sigma_{AB}}{\sigma_A \times \sigma_B}$$

The total variance of each path is the accumulation of the variance on each path’s gates; therefore, as more gates are considered the variance of the path grows, which consequently increase the $\sigma_A \times \sigma_B$ term in equation (4.1). For short paths, the term $\sigma_{AB}$ of (4.1) grows faster.
than $\sigma_A \times \sigma_B$ which increases inter-path correlation. Nevertheless, as path length grows, the covariance between paths increase but also the variances of both paths as can be observed in Figure 4.6. At certain point the variances on each path increase faster than the covariance between them, reducing the inter-path correlation. Therefore, the efficiency of this methodology will be reduced as the paths under test become longer.

### 4.1.5 Random Dopant Fluctuation

The following experiments are intended to observe the behavior of random process variations like RDF as the logical depth of a path is increased. The analysis is made on three chains of logic gates. In the analysis, each chain is analyzed for a progressively increasing number of gates, from 1 to 10, considering a rising and a falling input transitions. The first chain is constituted of inverters with the characteristics shown in Table 4.4a, second chain is constituted by NAND gates with the dimensions shown in Table 4.4b and finally the third chain is constituted of NOR gates with the dimensions shown in Table 4.4c.

Considering the inverters chain, the behavior of delay standard deviation ($\sigma_D$) is shown in Figure 4.7. This experiment is repeated under the same conditions for a chain of two inputs NAND gate, and two inputs NOR gate. The $\sigma_D$ behavior of NAND and NOR chains is shown in Figure 4.8 and 4.9, respectively.

As can be observed in Figures 4.7, 4.8 and 4.9, the behavior of $\sigma_D$ has an increasing tendency. Nevertheless, in all cases (specially on the inverters chain) the behavior is not monotonic. The reason for this non-monotonic behavior is that the effects of RDF are not

<table>
<thead>
<tr>
<th>Device</th>
<th>L (nm)</th>
<th>W (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS-1</td>
<td>180</td>
<td>450</td>
</tr>
<tr>
<td>PMOS-1</td>
<td>180</td>
<td>990</td>
</tr>
</tbody>
</table>

(a) Inverter device sizes

<table>
<thead>
<tr>
<th>Device</th>
<th>L (nm)</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS-2</td>
<td>180</td>
<td>990</td>
</tr>
<tr>
<td>PMOS-1</td>
<td>180</td>
<td>1.35</td>
</tr>
<tr>
<td>PMOS-2</td>
<td>180</td>
<td>1.35</td>
</tr>
</tbody>
</table>

(b) NAND device sizes

<table>
<thead>
<tr>
<th>Device</th>
<th>L (nm)</th>
<th>W (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS-2</td>
<td>180</td>
<td>450</td>
</tr>
<tr>
<td>PMOS-1</td>
<td>180</td>
<td>1.53</td>
</tr>
<tr>
<td>PMOS-2</td>
<td>180</td>
<td>1.53</td>
</tr>
</tbody>
</table>

(c) NOR device sizes

Table 4.4: Device dimensions of the gates used for the analysis of RDF effects on the delay standard deviation of paths.
the same for the low-to-high than for the high-to-low transition. This inequality in the effects of RDF is due to the difference in sizing between PMOS and NMOS devices. The effects of RDF are stronger for smaller devices [89].

One of the biggest concern for the implementation of this methodology on future technologies is the reduction of inter-path correlation due to the effects of RDF. As technology scales, the reduction of transistors’ dimensions aggravate the effects of RDF, increasing the delay variance of the paths and reducing the inter-path correlation. However, the tendency to design circuits that have shorter and faster paths will alleviate the reduction of inter-path correlation.
correlation for future technologies as shown on section 4.1.4.

The scaling of technology not only increase the effects of RDF, but also the effects of all process variations in general. Therefore, the increase of WID variations will affect inter-path correlation that can be present in a circuit. In order to increase the scalability of the proposed methodology, the spatial correlation model described in section 3.2.3 allows the adjustment of the SSTAF for different WID-D2D variations relationships.

### 4.2 SDD Detection Experimental Analysis

In this section the proposed methodology is evaluated using the benchmark circuits described in appendix A. The analysis has been made using two approaches, the first one restrict the analysis to a simple correlation approach between a pair of paths; meanwhile, the second approach use a multiple correlation analysis. Both approaches are compared.

In order to test the proposed methodology, a group of three circuits with particular characteristics were implemented. The circuits are a BCD to seven segment code converter, the 74LS85 4-bit magnitude comparator and the ISCAS-85 C499 single-bit error detector. These circuits were implemented in a Verilog or VHDL script and synthesized on Mentor Graphics Leonardo for a TSMC 0.18µm technology. The floorplan, cell’s placement and routing were made automatically using the optimization tools of Mentor Graphics IC-Studio.
4.2 SDD Detection Experimental Analysis

4.2.1 Simple Correlation Approach

To show the implementation of inter-path correlation on the detection of delay defects, consider the 4-bit magnitude comparator circuit (74LS85). For this circuit, two pairs of paths have been selected to show different cases of correlation and the effects on delay detection. The circuit generated is located in a total area of $390\mu m \times 620\mu m$. This analysis is made considering a CD of $500\mu m$ with a 65-35 WID-D2D relationship.

4.2.1.1 Non-Structurally correlated paths

First consider the paths in Figure 4.10, where 4.10a is the critical path of the circuit and 4.10b is a path that has no structural correlation with path 4.10a. The correlation between paths in Figure 4.10 is shown in Table 4.5, for the case without RDF and when their effects are considered. In Table 4.5, $\sigma_e$ represents the standard error of estimation at each gate, which can be achieved according to the correlations between paths under test (PUT).

<table>
<thead>
<tr>
<th>Paths</th>
<th>$G_1$</th>
<th>$G_2$</th>
<th>$G_3$</th>
<th>$G_4$</th>
<th>$G_5$</th>
<th>ALB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>(153,36)</td>
<td>(247,36)</td>
<td>(332,36)</td>
<td>(260,36)</td>
<td>(246,36)</td>
<td></td>
</tr>
</tbody>
</table>

(a) Path 1.

<table>
<thead>
<tr>
<th>Paths</th>
<th>$G_6$</th>
<th>$G_7$</th>
<th>$G_8$</th>
<th>$G_9$</th>
<th>ALB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>(153,448)</td>
<td>(423,246)</td>
<td>(334,640)</td>
<td>(219,246)</td>
<td></td>
</tr>
</tbody>
</table>

(b) Path 2.

Figure 4.10: Two non-structurally correlated paths chosen from 74LS85 circuit.

paths in Figure 4.10 is shown in Table 4.5, for the case without RDF and when their effects are considered. In Table 4.5, $\sigma_e$ represents the standard error of estimation at each gate, which can be achieved according to the correlations between paths under test (PUT).

The results of Table 4.5, shows that this methodology allows an SDD screenable variance (SSV) of 17.6% (or 20.5% if the effects of RDF are neglected), increasing the detectability of SDDs on the PUTs. The increase in detectability represents that in 17.6% of the PUT’s variance, the delay fluctuations due to the presence of defects can be identified from within
### Chapter 4: Simulation Results

<table>
<thead>
<tr>
<th>Without RDF</th>
<th>Path 1</th>
<th>$\sigma$</th>
<th>$\rho$</th>
<th>$\sigma_s$</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path 1</td>
<td>29.34ps</td>
<td>0.6060</td>
<td></td>
<td>23.34ps</td>
<td>20.5%</td>
</tr>
<tr>
<td>Path 2</td>
<td>21.44ps</td>
<td></td>
<td></td>
<td>17.05ps</td>
<td></td>
</tr>
<tr>
<td>With RDF</td>
<td>Path 1</td>
<td>30.27ps</td>
<td>0.5668</td>
<td>24.93ps</td>
<td>17.6%</td>
</tr>
<tr>
<td>Path 2</td>
<td>22.21ps</td>
<td></td>
<td></td>
<td>18.28ps</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.5: Inter-path correlation between the two non-structurally correlated paths shown in Figure 4.10.


<table>
<thead>
<tr>
<th>Path 3</th>
<th>$\sigma$</th>
<th>$\rho$</th>
<th>$\sigma_s$</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path 4</td>
<td>$\sigma$</td>
<td>$\rho$</td>
<td>$\sigma_s$</td>
<td>SSV</td>
</tr>
</tbody>
</table>

those variations due to process variations. As can be observed in Table 4.5, the increase of SDD detectability generated by the achieved SSV is equal for both paths, which means that SSV is independent of the path length or timing slack.

### 4.2.1.2 Structurally Correlated Paths

Now consider the paths shown in Figure 4.11 with the gates’ X-Y coordinate location shown below each gate. These paths are structurally correlated sharing gates $G_1$ and $G_2$. The correlation information between these two paths is given in Table 4.6.

![Figure 4.11](image)

When two paths are structurally correlated, a defect on the shared part (gates $G_1$ and $G_2$) will not create a deviation on the inter-path correlation, as it affects both path’s delay with the
Table 4.6: Inter-path correlation between the non-structurally correlated paths 3 and 5.

<table>
<thead>
<tr>
<th></th>
<th>Path</th>
<th>$\sigma$</th>
<th>$\rho$</th>
<th>$\sigma_e$</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Without RDF</strong></td>
<td>Path 3</td>
<td>21.44ps</td>
<td>0.75</td>
<td>14.18ps</td>
<td>33.8%</td>
</tr>
<tr>
<td></td>
<td>Path 4</td>
<td>22.12ps</td>
<td></td>
<td>14.63ps</td>
<td></td>
</tr>
<tr>
<td><strong>With RDF</strong></td>
<td>Path 3</td>
<td>22.22ps</td>
<td>0.6997</td>
<td>15.87ps</td>
<td>28.55</td>
</tr>
<tr>
<td></td>
<td>Path 4</td>
<td>22.87ps</td>
<td></td>
<td>16.33ps</td>
<td></td>
</tr>
</tbody>
</table>

same magnitude. This phenomenon represents that even with a high inter-path correlation, the fault coverage for these shared structures will be reduced. In order to address this problematic, multiple pairs of paths can be considered. For instance, additionally to paths in Figure 4.11, consider the path of Figure 4.12, which is not structurally correlated to any of the paths in Figure 4.11. The inter-path correlation between path 3 and 5 is shown in Table 4.7.

![Path Diagram](image)

Figure 4.12: Path non-structurally correlated with paths 4.11a and 4.11b, which will be used to screen defects on their shared section.

Table 4.7: Inter-path correlation between paths in Figure 4.11a and 4.12.

<table>
<thead>
<tr>
<th></th>
<th>Path</th>
<th>$\sigma$</th>
<th>$\rho$</th>
<th>$\sigma_e$</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Without RDF</strong></td>
<td>Path 3</td>
<td>21.44ps</td>
<td>0.6566</td>
<td>16.17ps</td>
<td>24.6%</td>
</tr>
<tr>
<td></td>
<td>Path 5</td>
<td>20.79ps</td>
<td></td>
<td>15.68ps</td>
<td></td>
</tr>
<tr>
<td><strong>With RDF</strong></td>
<td>Path 3</td>
<td>22.22ps</td>
<td>0.6078</td>
<td>17.54ps</td>
<td>20.6%</td>
</tr>
<tr>
<td></td>
<td>Path 5</td>
<td>21.67ps</td>
<td></td>
<td>17.21ps</td>
<td></td>
</tr>
</tbody>
</table>

When path 4.11a and 4.11b were analyzed, a defect present in the section of path 4.11a between gates $G_1$ and $G_2$ was undetectable. Nevertheless, the rest of the path can be detected according to Table 4.6. When a third path is also considered, defects in the section between gates $G_1$ and $G_2$ can be detected according to Table 4.7. This means that certain sections of paths will have different detection resolution, depending on the paths selected as reference.

By implementing the analysis of multiple pairs of paths, the fault coverage using this methodology can be increased. Nevertheless, the consideration of multiple pairs of paths
involve the estimation of multiple paths delay distribution and the inter-path correlation between them. This generates a compromise between fault coverage and the complexity of establishing the inter-path correlation reference frame.

### 4.2.2 Multi-Variable Approach

As shown in section 2.6, the use of a multiple correlation approach increases the effectiveness of the proposed methodology. In order to further show the advantages of a multiple correlation approach the BCD to seven segment code converter (BCD7S) is analyzed. First consider the paths shown in Figure 4.13 whose gates position are shown at the bottom.

![Diagram of BCD7S circuit](image)

Figure 4.13: PUT from the BCD7S circuit which were selected to implement the proposed methodology with the multiple correlation approach.

Using the SSTA framework described in chapter 3 the correlation between paths under analysis can be computed. The obtained correlations are shown in Table 4.8. For this experiment, path labeled as OP is considered as the objective path of the analysis and paths P1 and P2 will be used as predictor paths. As can be observed in Table 4.8, the path that is the most...
highly correlated with the objective path is $P_1 (\rho_{P_1,OP} = 0.5487)$. Moreover, the correlation between paths $P_1$ and $P_2$ (0.4615) is lower than the correlation between $P_1$ and $OP$, which guarantee an analysis with low multicollinearity between predictor paths.

Table 4.8: Correlation information between the paths of Figure 4.13.

<table>
<thead>
<tr>
<th></th>
<th>Path 1</th>
<th>Path 2</th>
<th>OP</th>
<th>$\sigma(ps)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path 1</td>
<td>1</td>
<td>0.46156</td>
<td>0.5487</td>
<td>16.095</td>
</tr>
<tr>
<td>Path 2</td>
<td>0.46156</td>
<td>1</td>
<td>0.4498</td>
<td>22.397</td>
</tr>
<tr>
<td>OP</td>
<td>0.5487</td>
<td>0.4498</td>
<td>1</td>
<td>18.44</td>
</tr>
</tbody>
</table>

The results of implementing the proposed methodology are shown in Table 4.9, which also show the improvement from using a simple correlation approach under the best conditions and the multiple correlation approach. The comparison is made using the best partial correlation (simple correlation between a predictor path and the objective path) case, which for this case, is the correlation between $P_1$ and $OP$ and the result of implementing a multiple correlation approach.

Table 4.9: Improvement on SDD detection using a multiple correlation approach.

<table>
<thead>
<tr>
<th>Case</th>
<th>$R_{OP,12}$</th>
<th>$\sigma_{OP}(ps)$</th>
<th>$\sigma_e$</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Partial correlation ($\rho_{OP,P_1}$)</td>
<td>0.5487</td>
<td>18.44</td>
<td>15.38</td>
<td>16.4%</td>
</tr>
<tr>
<td>Multiple correlation between 3 paths</td>
<td>0.5917</td>
<td>11.98</td>
<td>19.38%</td>
<td></td>
</tr>
</tbody>
</table>

As shown in section 2.6, the predictability of one criterion variable increase when more predictor variables are considered. Therefore, for the previous exercise a fourth path can be included in the analysis. Consider the path $P_3$ shown in Figure 4.14.

Figure 4.14: Additional path from BCD7S circuit, which will be considered on the multiple correlation analysis of paths in Figure 4.13.
Including a third predictor path in the analysis, the predictability of \( OP \) is increased as \( P3 \) has low multicollinearity with paths \( P1 \) and \( P2 \), like shown on Table 4.10.

<table>
<thead>
<tr>
<th>Path 1</th>
<th>Path 2</th>
<th>Path 3</th>
<th>Objective Path</th>
<th>( \sigma(ps) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path 1</td>
<td>1</td>
<td>0.4615</td>
<td>0.4150</td>
<td>0.5487</td>
</tr>
<tr>
<td>Path 2</td>
<td>0.4615</td>
<td>1</td>
<td>0.3733</td>
<td>0.4498</td>
</tr>
<tr>
<td>Path 3</td>
<td>0.4150</td>
<td>0.3733</td>
<td>1</td>
<td>0.6237</td>
</tr>
<tr>
<td>Objective Path</td>
<td>0.5487</td>
<td>0.4498</td>
<td>0.6237</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.10: Correlation information between the paths of Figure 4.13, including path \( P3 \).

The improvement of considering a third predictor path is shown in Table 4.11, where the improvement against considering only two paths is presented. Similarly, the difference between the case of a simple approach and a multiple approach with four paths is presented. This comparison is made considering path \( P3 \) as it has the higher partial correlation with the objective path.

<table>
<thead>
<tr>
<th>Case</th>
<th>( R )</th>
<th>( \sigma_{P4}(ps) )</th>
<th>( \sigma_{s}(ps) )</th>
<th>SSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Partial correlation (( \rho_{OP,P3} ))</td>
<td>0.6237</td>
<td>18.44</td>
<td>14.4</td>
<td>21.83%</td>
</tr>
<tr>
<td>Multiple correlation between 4 paths</td>
<td>0.7166</td>
<td>12.86</td>
<td>30.25%</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.11: Improvement on SDD detection for a multiple correlation approach using a fourth path.

As can be observed in Table 4.11 the SDD detectability increase from 21.83% on a simple approach to 30.25% in a multiple approach with four paths. The increase of detectability achieved with the inclusion of a predictor path, depends on the correlation degree between the new predictor path and the previously considered paths (both predictors and objective). Nevertheless, if a low degree of multicollinearity is guaranteed, the multiple correlation coefficient will always be higher than any of the partial correlation coefficients between the objective path and any of the predictor paths.

The inclusion of a third predictor path increases the SDDs detectability, as the multiple correlation between \( PO \) and the predictor paths increase. This implies that as more paths are considered in the analysis, the efficiency of the methodology increase. As can be observed, by
considering the correlation between more than two paths, the error of estimation is reduced and the detectability of SDDs on a path is increased. Nevertheless, the increase of SDDs detectability not only depends of the number of predictor paths, but also depends on the multicollinearity between them. Therefore, the selection of the paths under analysis is a critical part of a multiple correlation analysis implementation.

The results of this section shows the main differences between a simple and a multiple correlation approach. Nevertheless, it has to be considered that the implementation of a multiple correlation approach demands the use of more computational resources. The main advantages and disadvantages of a multiple approach regarding a simple approach can be summarized as follows:

**Advantages:**

- Under the same conditions and with low level of multicollinearity a multiple approach will always allows a higher detection resolution.
- With a multiple approach the problem of fault coverage reduction in a path due to structural correlation will be automatically addressed.

**Disadvantages:**

- A multiple approach implies that multiple paths must be analyzed, which increase the computational complexity.
- Implementing a multiple approach demands the measurement of multiple output’s delay.

It can be concluded that a multiple approach allows a higher increase of detectability but requires more resources to establish the reference frame. Nevertheless, during the testing stage of a process, each sample will be compared with the reference frame previously established. Therefore, the increase of computational complexity does not affect directly the testing stage. In consequence, the advantages of a multiple approach overpass its drawbacks. Considering the characteristics of both simple and multiple approaches, the multiple approach is recommend as the best option as the cost of this approach will be justified by the increase of detectability. In the extreme case where the computational and testing resources are limited, the simple approach will be the most feasible option as it will be more cost efficient.
4.3 Highly Correlated Paths Selection

As mentioned throughout this thesis, the proposed methodology is based on the degree of correlation between the output’s delay of a circuit. Therefore, it is necessary to maximize the inter-path correlation between PUT. The use of a multiple correlation approach increase the efficiency of this methodology; nevertheless, it requires the selection of paths that minimize the effects of multicollinearity in order to maximize the multiple correlation coefficient. Therefore, the selection of paths is a task that must be systematized and automated.

4.3.1 Heuristic Selection of Highly Correlated Paths

The best manner to maximize the inter-path correlation and optimize the methodology is the accurate selection of PUT that will be included in the analysis. From the whole universe of paths available on a circuit, some of them are more important than others either because they are the slowest path or because they are indispensable for its functionality. Those paths that are considered as the most important on a circuit are known as critical paths. The selection of PUT starts by stating which are the objective paths that must be tested, these can be the critical paths or any other non-false path of a circuit. Nevertheless, this methodology is designed to be implemented on any of the critical or non-critical paths of a circuit.

The selection of the critical paths has been a hot-topic for many years on STA and SSTA, as it represents the efficiency of the testing procedures. Many works have focused on the selection of those paths that have the longest propagation delay. On STA, paths selection procedures identify the non-false paths with the longest propagation delay [101, 102, 103]. Nevertheless, when process variations are considered the concept of selecting a single critical path, even if is the slowest one, is not valid anymore because of the delay variability. Delay performance variability implies that for a certain die a certain path will be the slowest path, but for another die a different path may become the slowest one. Therefore, instead of selecting a single critical path, a group of paths with the highest probability of being the critical path [45, 50, 104] is selected. Other approaches focus on selecting those paths that maximize the fault coverage of the circuit like in [45].
Once the objective paths are selected, the next step is to choose, from the rest of paths, those whose variations are highly correlated with the variations of the objective path. As shown in section 4.1, the inter-path correlation depends on different conditions of spatial correlation, structural correlation and path length; therefore, these conditions have to be taken into consideration for an accurate selection of paths. Moreover, the paths selection criteria has to consider if the analysis will be made using a simple correlation approach or a multiple correlation approach. Using the previous behavioral analysis, two heuristic algorithms can be design to select the most suitable paths for the analysis of a certain objective path. One of the algorithms will be focused on selecting the most suitable paths to implement a simple correlation approach and the other will be design to select the most suitable paths for a multiple correlation approach. These algorithms will be described next.

4.3.1.1 Simple Correlation Approach

From the behavior analysis presented earlier, it can be observed that those paths that are close to each other will be highly correlated, as well as those that are structurally correlated. However, when two paths are structurally correlated, parts of a circuit can not be tested, as defects in that section will have the same effect on both path. Another aspect that must be considered is the reduction of inter-path correlation as path’s length increase. Therefore, the candidate paths, which may be any non-false path, must maximize the inter-path correlation considering these aspects. The aspects of inter-path correlation mentioned above allows the formulation of three heuristic objectives to select the candidate paths that will be included in the analysis. These heuristics will be described in order of priority:

- **H-spatial**: the distance between the objective path and the selected candidate path must be the smallest possible. In order to quantify the distance between paths, the average inter gate distance (AIGD) must be computed. The AIGD can be computed as follows:

\[
AIGD = \frac{\sum_{j=1}^{N_O} \sum_{i=1}^{N_C} R_{G_{i,j}}}{N_O N_C}
\]  

(4.2)
where $R_{G_{ij}}$ represents the distance between the $i$-th gate of the candidate path and the $j$-th gate of the objective path, $N_C$ represents the number of gates in the candidate path and $N_O$ is the number of gates in the objective path. The candidate path with the lowest AIGD will fulfil H-spatial.

- **H-length**: the candidate path must be the shortest path possible.

- **H-structural**: the candidate path must maximize the number of shared gates between the objective path and itself. The gates that can be considered as shared are those that share the exact same pin-to-pin delay.

The fulfilment of **H-structural** implies that a certain section of the objective path will not be able to be tested, reducing the fault coverage on the objective path. As shown in section 4.2.1, this problem can be solved with the inclusion of a third path that test the shared section of the objective path. Therefore, a heuristic restriction must be formulated:

- **H-maxcoverage**: if the first selected path has structural correlation with the objective path, then the objective path will be divided in two sub-paths as follows:

  1. The common gates between the previously selected path and the objective path, will be sub-path $OP_1$.

  2. Those gates that are not common between objective path and the selected path will be sub-path $OP_2$.

Using the sections previously described, a candidate path that best fulfil **H-length** and **H-spatial** and that is non-structurally correlated with $OP_1$ must be included in the analysis.

The selection of highly correlated paths can be summarized in algorithm 2 presented in appendix B.1, which includes the heuristics previously described.
4.3.1.2 Multiple Correlation Approach

The selection of paths in a multiple correlation approach is very similar to the selection in a simple correlation approach. Both heuristic objectives \textbf{H-spatial} and \textbf{H-length} still valid for a multiple correlation approach. Heuristic \textbf{H-structural} on the other hand, is not suitable for a multiple correlation approach as the structural correlation between paths implies the existence of multicollinearity. For example, consider the paths shown in Figure 4.15, path \textit{OP} is the objective path and \textit{PA} and \textit{PB} are the paths that will be included in the analysis.

As can be observed in Figure 4.15, paths \textit{OP} and \textit{PA} are structurally correlated sharing gates \textit{G}_1 and \textit{G}_2. If path \textit{PB} is highly correlated with \textit{OP}, the structural correlation between \textit{PA} and \textit{OP} implies that \textit{PA} and \textit{PB} will also be highly correlated. This high correlation between \textit{PA} and \textit{PB} increase the effects of multicollinearity, which will reduce the effectiveness of a multiple correlation approach. Therefore, on a multiple correlation approach the presence of structural correlation must be avoided.

The minimization of structural correlation between paths will minimize the multicollinearity effects between paths. However, avoiding structural correlation may limit the number of candidate paths that can be suitable for the analysis. In order to reduce the effects of multicollinearity without restricting the number of candidate paths, the objective path can be divided in two sub-paths \textit{OP}_1 and \textit{OP}_2. Consider that sub-path \textit{OP}_1 is constituted by those gates that are common between \textit{PO} and certain path \textit{PA}, which was previously selected using the \textbf{H-spatial}, \textbf{H-length} and \textbf{H-structural}. Then path \textit{PB} must be such that it is highly cor-
related with sub-path $OP_2$, and must not be structurally correlated with sub-path $OP_1$. This conditions are shown in Figure 4.16.

![Figure 4.16: Objective path segmentation to minimize the effects of multicollinearity in a multiple correlation approach](image)

The structure described in Figure 4.16 reduce the effects of multicollinearity on structurally correlated paths, as $PA$ and $PB$ are highly correlated with path $OP$ but poorly correlated between them. This is because the variations of path $OP$ that occur in sub-path $OP_1$ will be highly correlated with the variations on path $PA$ and poorly correlated with the variations on path $PB$; meanwhile, the variations in $PB$ are highly correlated with the variations that occur in sub-path $OP_2$ and less correlated with the variations in $OP_1$. Additionally, the inter-path correlation between paths $PA$ and $PB$ must be the lowest possible. This analysis allows the statement of another heuristic restriction, described as follows:

- **H-multiple**: if a path $PA$ previously selected is structurally correlated with $OP$, then $OP$ must be divided in two sub-paths such that:
  
  - Sub-path $OP_1$ will include all the gates common between $PA$ and $OP$.
  - Sub-path $OP_2$ will include all of the objective path’s gates that are not structurally correlated between $PA$ and $OP$. 
Using the sub-paths $OP_1$ and $OP_2$, another path $PB$ that maximize the following aspects must be selected:

- The correlation between paths $PB$ and $PA$ must be the lowest possible.
- The correlation between paths $PB$ and $OP_2$ must be the highest possible.

In order to select the candidate path that has the lowest correlation with $PA$, the heuristic $H$-spatial can be implemented in a negative version. This can be made by selecting the candidate path $PB$ that maximize the AIGD between $PA$ and $PB$.

The selection of paths for a multiple correlation approach can be summarized in algorithm 3 shown in appendix B.2. The previous heuristics objectives and restrictions can be used to select the paths that will maximize the effectiveness of the proposed methodology.

### 4.3.2 Analysis of circuit ISCAS-85 C499

To show the implementation of the proposed methodology in a more common environment, the benchmark circuit c499 was selected and few sets of paths were chosen to implement the analysis. The circuit ISCAS-85 C499 was selected as CUT, because of the uniformity of its paths. The selection of the paths under analysis, was carried out using the heuristic selection algorithm described in section 4.3.

On this experiment three paths were chosen as objective paths. The first objective path (PO#1) is the slowest path of the circuit; the second path (OP#2) is a medium size path and finally third path (PO#3) is one of the short path’s of the CUT. This selection was made intending to show that this methodology can be implemented on any path of the circuit, independently of its size and slack-time. Nevertheless, the selection of objective paths could had being made using any other selection criteria like susceptibility to defects, critical probability, maximum variance, etc. For each path a set of predictors were selected using algorithm 3, which selects the most suitable paths for implementing a four paths multiple correlation analysis.
Objective Path #1:

For the case of objective path #1 the path shown in Figure 4.17a was selected and the paths shown in Tables 4.17b to 4.17d were selected as its predictor paths. The spatial location of each gate is presented at the bottom of each gate, where their X-Y coordinates in the die are shown.

![Diagram](image)

Figure 4.17: Objective path #1 and its heuristically selected set of predictor paths.

OP#1 is one of the largest of the circuit, which turns the selection of its predictor paths in a more critical task. This is because, as shown in section 4.1.4, the inter-path correlation decrease as the length of the paths increase. Therefore, the predictor paths are short paths that are spatially distributed along the location of OP#1. The resultant correlation matrix between OP#1 and its predictor paths is shown in Table 4.12.
### 4.3 Highly Correlated Paths Selection

Using the inter-path correlation information of Table 4.12, the standard error of estimation and the total SSV are shown in Table 4.13. The SDD detection increase is directly related with the SSV that can be achieved with the cross-correlation matrix in Table 4.12. The minimum delay detectable on OP#1 and its delay distribution, as well as the delay distribution of the predictor paths are included in Table 4.13.

<table>
<thead>
<tr>
<th>Path</th>
<th>$\sigma_D$</th>
<th>$R_{OP,ABC}$</th>
<th>$\sigma_{e_{OP,ABC}}$</th>
<th>SSV on OP#1 variance</th>
<th>$\Delta D_{\text{min}}$ (4 paths)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path A</td>
<td>20.20ps</td>
<td>0.8383</td>
<td>28.71ps</td>
<td>28.03%</td>
<td>86.149ps</td>
</tr>
<tr>
<td>Path B</td>
<td>22.35ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Path C</td>
<td>22.77ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OP #1</td>
<td>52.75ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.13: Paths delay Distribution and minimum delay detectable in OP #1.

Table 4.13 shows SSV on OP#1 under three conditions. The first analysis is limited to a simple correlation approach using only one predictor path (path C); second one implements a multiple approach using two predictor paths (path B and C) and the last case use a multiple approach using three predictor paths (path A, B and C). As can be observed SSV increase 7.3% from 28.03% using one predictor path, up to a 35.33% using two predictor paths. This increase can be achieved considering that the correlation between the second path included (path B) and the first predictor (path C) is 0.4445 and the correlation with the objective path is 0.6861. This degrees of partial correlation guarantee a low level of multicollinearity.

On the last case, a third predictor path is included increasing SSV 10.22%, from 35.33% up to 45.55%. The larger increase regarding the previous case, can be explained by looking at the partial correlation degrees between the third predictor (path A) and the other paths. The correlation between path A and B is 0.4581 and between A and C is 0.4070, meanwhile...
the partial correlation between OP#1 and path A is 0.6943. The correlation between path A and the predictor paths guarantees a low level of multicollinearity; meanwhile the correlation between path A and OP#1 increase the variance of OP#1 that can be described.

**Objective Path #2:**

The path shown in Figure 4.18a was selected as the objective path #2. It is a medium-sized path conformed by slow and heavy variant gates. Meanwhile, its set of predictor paths shown in Figures 4.18b to 4.18d where selected as its set of predictor paths.

![Figure 4.18: Objective path #2 and its heuristically selected set of predictor paths.](image)

Using the SSTAF proposed in chapter 3, the inter-path correlation matrix between the set of paths for OP#2 can be computed. The resultant correlation matrix is shown in Table 4.14. As can be observed in Table 4.14, the inter-path correlation between the predictor paths A,
### 4.3 Highly Correlated Paths Selection

<table>
<thead>
<tr>
<th></th>
<th>Path A</th>
<th>Path B</th>
<th>Path C</th>
<th>OP #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path A</td>
<td>1</td>
<td>0.5020</td>
<td>0.4673</td>
<td>0.6243</td>
</tr>
<tr>
<td>Path B</td>
<td>0.5020</td>
<td>1</td>
<td>0.4023</td>
<td>0.6461</td>
</tr>
<tr>
<td>Path C</td>
<td>0.4673</td>
<td>0.4023</td>
<td>1</td>
<td>0.5898</td>
</tr>
<tr>
<td>OP #2</td>
<td>0.6243</td>
<td>0.6461</td>
<td>0.5898</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.14: Cross-correlation matrix for the selected set of paths used to implement a multiple correlation approach on path OP#2.

B and C is relatively low regarding the maximum inter-path correlation between OP#2 and any of the predictor paths. This can be understood by looking at the paths location, where the predictor paths are close to the objective path but far from each other. This low correlation between predictor paths, guarantee a low level of multicollinearity on the analysis.

Similarly to the analysis of OP#1, the analysis of OP#2 will be made for one, two and three predictor paths. The results of the analysis on the selected paths is shown in Table 4.15, which also summarizes each path delay distribution. The standard error of estimation ($\sigma_e$) and the minimum delay increase detectable ($\Delta D_{\text{min}}$) shown in Table 4.15 are computed using the correlation achieved with the use of three predictor paths.

<table>
<thead>
<tr>
<th>Path</th>
<th>$\sigma_D$</th>
<th>$R_{OP,ABC}$</th>
<th>$\sigma_{e,OP,ABC}$</th>
<th>SSV on OP#2</th>
<th>$\Delta D_{\text{min}}$ (4 paths)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2 Paths</td>
<td>3 Paths</td>
</tr>
<tr>
<td>Path A</td>
<td>17.14ps</td>
<td>0.7777</td>
<td>29.87ps</td>
<td>23.67%</td>
<td>32.7%</td>
</tr>
<tr>
<td>Path B</td>
<td>20.51ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Path C</td>
<td>27.71ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OP #2</td>
<td>47.53ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.15: Paths delay variance, standard error of estimation, SSV and minimum delay detectable in OP #2.

The value of SSV using only predictor C is 23.67%. With the inclusion of path B, the SSV increase 9.03% to achieve a total of 32.7%. If path A is included as a third predictor, the SSV increase up to 37.13%. The improvement of including extra predictor paths on this analysis is smaller than for OP#1. This is because the correlation between predictor paths are higher, increasing the effects of multicollinearity.
Objective Path #3:

Finally objective path #3 and its set of predictor paths are shown in Figure 4.19. Objective path OP#3 was selected to show that this methodology can be implemented on short paths, which has been one of the main limitations of the state-of-the-art techniques.

![Diagram of Objective Path #3](image)

![Diagram of Predictor Path A](image)

![Diagram of Predictor Path B](image)

![Diagram of Predictor Path C](image)

Figure 4.19: Objective path #3 and its heuristically selected set of predictor paths.

The Table 4.16, shows the cross-correlation matrix computed with the SSTAF proposed. As can be observed, for this set of paths the correlation between predictor paths A, B and C is slightly higher than for the previous analysis. Nevertheless, the level of multicollinearity still low enough to allows an appropriate implementation of the proposed methodology.

<table>
<thead>
<tr>
<th></th>
<th>Path A</th>
<th>Path B</th>
<th>Path C</th>
<th>OP #3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path A</td>
<td>1</td>
<td>0.5060</td>
<td>0.4876</td>
<td>0.6306</td>
</tr>
<tr>
<td>Path B</td>
<td>0.5060</td>
<td>1</td>
<td>0.5128</td>
<td>0.5943</td>
</tr>
<tr>
<td>Path C</td>
<td>0.4876</td>
<td>0.5128</td>
<td>1</td>
<td>0.5861</td>
</tr>
<tr>
<td>OP #3</td>
<td>0.6306</td>
<td>0.5943</td>
<td>0.5861</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.16: Cross-correlation matrix between OP#3 and its predictor paths.
Just like in the previous objective paths, the analysis is presented for three conditions of predictor paths. One using only one predictor path, then this analysis is extended to include a second predictor and finally the last analysis includes three predictor paths. The delay performance of each path and the minimum delay detectable on the objective path #3 is shown in Table 4.17. The minimum delay detectable is computed using the standard error of estimation generated by the analysis that use three predictor paths.

<table>
<thead>
<tr>
<th>Path</th>
<th>$\sigma_D$</th>
<th>$R_{OPABC}$</th>
<th>$\sigma_{eOPA}$</th>
<th>SSV on OP#3</th>
<th>$\Delta D_{min}$ (4 paths)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path A</td>
<td>24.80ps</td>
<td></td>
<td>0.74106</td>
<td>18ps</td>
<td>22.38% 26.54% 32.86% 54ps</td>
</tr>
<tr>
<td>Path B</td>
<td>25.42ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Path C</td>
<td>20.11ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OP #3</td>
<td>26.8123ps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.17: SDD detectability on objective path #3 using the proposed methodology.

On this analysis, SSV using one predictor path has a value of 22.38%; including a second predictor path, increase up to 26.54% and if a third predictor paths is included the total SSV increase up to 32.8%. As can be observed, for this particular case, the degree of correlation between predictor paths is higher than in the analysis of OP#1 and OP#2. The fact that the correlation degree between predictor paths is higher for this objective path, reduce the improvement achieved with the inclusion of predictor paths.

From the analysis of the three objective paths is clear that a multiple correlation approach can considerably increase the SDD detectability. The total increase that can be achieved depends not only of the correlation with the objective paths, but also depends on the correlation degree between predictor paths. This fact increase the importance of the accurate selection of predictor paths.

### 4.4 Conclusion

At the beginning of this chapter, the statistical cells developed on the SSTA framework were validated with an average error lower than 1%. The validated cells were use to analyze the behavior of inter-path correlation for different circuit conditions. The results obtained in the
behavioral analysis shows that inter-path correlation is strongly dependent of the distance between the analyzed paths. Moreover, the presence of structural correlation increase the degree of inter-path. Also the effects of the number of gates in a path were analyzed, showing that as the path’s length grows the inter-path correlation decrease.

The feasibility of the proposed methodology was validated on C499 benchmark circuit. The results of the analysis, shows that the SDDs detectability is increased by this methodology, as the portion of variance where delays can be screened (SSV) is increased. This increase on detectability is because of the possibility of detecting SDDs from within process variations. The part of delay variability due to process variations that can be distinguished from deviations due to defects, is dependent of the correlation degree between PUT; for high correlation degrees, the part of variance that can not be distinguished is a minimal part of the total delay variance. However, even for low correlation degrees the SDDs detectability is increased regarding to the state-of-the-art testing techniques.

As more paths are included in the analysis SSV increase. Therefore, from the two proposed approaches, the multiple correlation represents the most effective alternative. Nevertheless, the implementation of a simple correlation approach is a much cheaper alternative, as it only requires the inter-path correlation between a pair of paths. However, with a simple correlation approach, the effects of structural correlation must be considered. Therefore, for the case of structural correlation, a cost comparative analysis has to be made between a simple correlation approach with three paths and a multiple correlation approach.

Using the behavior analysis previously made, two algorithms to select paths with high inter-path correlation were proposed. This algorithms are base on a group of heuristic objectives and restrictions that accounts for the effects of spatial correlation, structural correlation and paths length. One of the proposed algorithms is focused on selecting the optimal paths for a simple correlation approach, accounting for the effects of structural correlation on the fault coverage of the objective path; meanwhile, the other algorithm optimize the paths selection in a multiple correlation approach considering the effects of multicollinearity. The ISCAS c499 circuit was tested implementing a multiple correlation approach, where the selection of paths were made using the heuristic algorithms.
Chapter 5

Conclusions

The constant and aggressive scaling on transistors dimensions, has increase the variability of circuit’s performance. This variability has encouraged the appearance of delay defects that reduce the performance of circuits, decreasing the yield of manufacturing processes. Moreover, as ICs shrinks, the probability of small-delay defects presence on a circuit has dramatically increase. The existence of small delay defects compromises the reliability of the circuit, as they increase the probability of an early life-time failure. On this work, the background of small-delay defects effects on circuit reliability, which justify the present work, has been presented.

The proposed methodology represents an unexplored alternative to the state-of-the-art approaches for small delay defect detection. This methodology do not increase the circuits overhead, as it do not require the implementation of on-chip testing structures. Moreover, this methodology do not require the implementation of complex testing vector algorithms; in fact, testing vectors from custom logic testing can be used. This methodology is suitable for testing small and large paths independently of their timing slack, this allows the increase of small-delay defects detection coverage, increasing the reliability of the circuit. The main advantage of this methodology is that it allows to distinguish between delay deviations due to process variation from delay deviations due to the presence of a defect.

This methodology is based on the use of correlation information between circuit’s out-
puts delay. Two approaches has been proposed to implement this methodology, a simple and a multiple correlation analysis. The simple correlation approach is the cheaper alternative, meanwhile the multiple correlation approach allows a higher detection resolution. To quantify the small-delay defects detection, $\Delta D_{\text{min}}$ has been proposed as a metric that represents the delay deviation that can be detected. Also SSV has been proposed as a figure of merit that represents the portion of variance in a path where the delay fluctuations due to delay defects can be identified from within delay fluctuations due to process variations.

In order to calculate the inter-path correlation an SSTA framework as been implemented and validated. This framework models the effects of systematic and random variations for the main circuits parameters. A model suitable for scaling, has been implemented to account for the effects of spatial correlation for WID and D2D variations. The effects of random dopants fluctuations has been considered and modeled for each standard cell used in the SSTA framework. Also, the effects of structural correlation has been considered, as well as its effects on the simple and multiple correlation approach of the methodology.

The proposed SSTA framework, has been implemented in MATLAB. The accuracy of the framework has been validated against SPICE Monte-Carlo simulations at 10,000 iterations with an error on mean and variance lower than 1%.

Using this framework, the behavior of inter-path correlation has been analyzed. The results of this behavioral analysis shows that inter-path correlation is dependent of the paths spatial location, paths structural correlation and length. In order to select those paths that maximize the inter-path correlation, a group of heuristic objectives and restrictions has been proposed. These heuristics are focused on selecting the paths most suitable for testing an objective path, considering the aspects that contribute to inter-path correlation. The heuristics generated have been implemented in two algorithms, one that select the paths for a simple correlation approach and a second one that selects paths for a multiple correlation approach.

Results from simulation of benchmark circuits validates the feasibility of the proposed methodology as a technique to enhance the reliability of circuits. Nevertheless, it has been shown that the proposed methodology requires of the accurate estimation of inter-path correlation, and its effectiveness depend on the degree of inter-path correlation. Therefore, future
efforts must be focused on the development of an efficient path selection framework that allows the identification of highly correlated paths. For such a purpose the information contained on this work sets the aspects that must be considered for an optimal path selection.

The main contributions of this work can be listed as follows:

- An SDD testing methodology capable of detecting SDDs on both long and short paths independently of their timing slacks has been proposed, and its feasibility has been validated.

- The proposed methodology is capable of detecting delay fluctuations generated by an SDD from within those fluctuations that are generated by process variations.

- An efficient SSTA framework suitable for scaling and capable of computing the correlation degree between paths have been proposed and validated including the effects of systematic and random variations.

- During this work the aspects that must be considered during the selection of predictor paths has been presented and analyzed; using this information a group of heuristic objectives and restrictions have been formulated.
Appendix A

Benchmark Circuits

Each of the benchmark circuits analyzed in chapter 4 were implemented on a VERILOG or VHDL script, which were latter synthesized with Mentor Graphic’s Leonardo in a TSMC018μm technology without time or area optimization. The layout of each circuit were implemented in Mentor graphics IC-Studio with automatic and optimal placement and routing. The resultant layout and source code of each circuit are presented next.

A.1 BCD7S: BCD to Seven Segments Code Converter:

This circuit is a common ASIC that converts a decimal number coded in BCD into data suitable to be displayed in a seven segment LED display, as shown in Figure A.1.

Figure A.1: Schematic representation of a BCD to seven segment converter.

This circuit has a topology with many structurally correlated paths that have a medium logical depth. The characteristics of this circuit allow the use of simple correlation analysis
on medium-sized paths, where the effects of structural correlation on the defects coverage of the PUT. The BCD to seven code converter was synthesized from the following VHDL script.

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity seg7 is
  Port ( a : in STD_LOGIC_VECTOR (3 downto 0);
        d : out STD_LOGIC_VECTOR (6 downto 0) );
end seg7;

architecture Behavioral of seg7 is
begin
process (a)
begin
  case a is
  when "0000" => d <= "1000000";
  when "0001" => d <= "1111001";
  when "0010" => d <= "0010010";
  when "0011" => d <= "0000110";
  when "0100" => d <= "1001100";
  when "0101" => d <= "0100100";
  when "0110" => d <= "0100000";
  when "0111" => d <= "0001110";
  when "1000" => d <= "0001110";
  when "1001" => d <= "0000100";
  when others => d <= "0000000";
  end case;
end process;
end Behavioral;
```
end process;
end Behavioral;

The final implementation of the BCD7S uses a total of $640 \times 660 \mu m$. The resultant layout is shown in Figure A.4.

![Figure A.2: Layout of the BCD7S circuit, generated on Mentor Graphics IC-Studio.](image)

A.2 74LS85: 4-bit Magnitude Comparator:

Circuit 74LS85 is another common ASIC which is used to detect the qualitative relationship between the magnitude of two 4-bit words, like shown in Figure A.3. The useful characteristics of this circuit are its medium path depth with very few structurally correlated paths. These properties make it very useful for implementing a multiple correlation analysis.

small

module Circuit74LS85 (ALBi, AGBi, AEBi, A, B, ALBo, AGBo, AEBo);
A.2 74LS85: 4-bit Magnitude Comparator:

![Schematic representation of the 74LS85 4-bit magnitude comparator.](image)

Figure A.3: Schematic representation of the 74LS85 4-bit magnitude comparator.

```verilog
input [3:0] A, B;
input ALBi, AGBi, AEBi;
output ALBo, AGBo, AEBo;

TopLevel74L85 Ckt74L85 (ALBi, AGBi, AEBi, A, B, ALBo, AGBo, AEBo);
endmodule

`*`endmodule`

module TopLevel74L85 (ALBi, AGBi, AEBi, A, B, ALBo, AGBo, AEBo);

input [3:0] A, B;
input ALBi, AGBi, AEBi;
output ALBo, AGBo, AEBo;
wire [3:0] G1, G2, P;

GPmodule GPmod0(A,B,G1,G2,P);
CLAmodule ALBmod1(G1,P,ALBi,ALBo);
```
CLAmodule AGBmod2(G2, P, AGBi, AGBo);
EQmodule EQmod3(AEBi, P, AEBo);
endmodule

/*********************************************************************************/
module GPmodule(A, B, G1, G2, P);
  input [3:0] A, B;
  output [3:0] G1, G2, P;
  wire [3:0] Ab, Bb, AbB, ABb;
  not A0bgate(Ab[0], A[0]);
  not A1bgate(Ab[1], A[1]);
  not A2bgate(Ab[2], A[2]);
  not A3bgate(Ab[3], A[3]);
  not B0bgate(Bb[0], B[0]);
  not B1bgate(Bb[1], B[1]);
  not B2bgate(Bb[2], B[2]);
  not B3bgate(Bb[3], B[3]);
  and G10gate(G1[0], Ab[0], B[0]);
  and G11gate(G1[1], Ab[1], B[1]);
  and G12gate(G1[2], Ab[2], B[2]);
  and G13gate(G1[3], Ab[3], B[3]);
  and G20gate(G2[0], A[0], Bb[0]);
  and G21gate(G2[1], A[1], Bb[1]);
  and G22gate(G2[2], A[2], Bb[2]);
  and G23gate(G2[3], A[3], Bb[3]);
and AbB0gate(AbB[0], Ab[0], B[0]);
and AbB1gate(AbB[1], Ab[1], B[1]);
and AbB2gate(AbB[2], Ab[2], B[2]);
and AbB3gate(AbB[3], Ab[3], B[3]);

and ABb0gate(ABb[0], A[0], Bb[0]);
and ABb1gate(ABb[1], A[1], Bb[1]);
and ABb2gate(ABb[2], A[2], Bb[2]);
and ABb3gate(ABb[3], A[3], Bb[3]);

nor P0gate(P[0], AbB[0], ABb[0]);
nor P1gate(P[1], AbB[1], ABb[1]);
nor P2gate(P[2], AbB[2], ABb[2]);
nor P3gate(P[3], AbB[3], ABb[3]);

endmodule

/***************************************************************************/
module CLAmodule (G, P, AxBi, AxBo);
input [3:0] G, P;
input AxBi;
output AxBo;

buf G3gate (G3, G[3]);
and G2P3gate (G2P3, G[2], P[3]);
and G1P2P3gate(G1P2P3, G[1], P[2], P[3]);
and G0P1P2P3gate(G0P1P2P3, G[0], P[1], P[2], P[3]);
and AxBiP0P1P2P3gate(AxBiP0P1P2P3, AxBi, P[0], P[1], P[2], P[3]);
or AxBogate (AxBo, G3, G2P3, G1P2P3, G0P1P2P3, AxBiP0P1P2P3);
endmodule

module EQmodule (AEBi, P, AEBo);
  input AEBi;
  input [3:0] P;
  output AEBo;
  and AEBogate (AEBo, AEBi, P[0], P[1], P[2], P[3]);
endmodule

The implementation of the 74LS85 circuit use a total 740 × 560µm. Figure A.4 shows the final layout of the 74LS85 circuit.

Figure A.4: Layout of the 74LS85 circuit, generated on Mentor Graphics IC-Studio.
A.3 ISCAS 85 C499: 32-Bit Single-Error-Correcting Circuit:

Circuit C499 is used as a single-bit error detection system for 32-bits data transmitted in (40,32) Hamming code. The schematic of the C499 is shown in Figure A.5.

Figure A.5: Schematic representation of the ISCAS-85 c499.

This circuit is one of the medium size ISCAS 85 benchmark circuits, with a medium average logical depth. Therefore, this circuit is very useful to evaluate the methodology in a more typical industrial case. This circuit has a large number of possible paths, some structurally correlated and others non-structurally correlated. Due to the uniformity of the circuit and its recursive structure, paths with a similar structure can be found on different locations of the circuit.

small
**input**  
N1, N5, N9, N13, N17, N21, N25, N29, N33, N37,  
N41, N45, N49, N53, N57, N61, N65, N69, N73, N77,  
N81, N85, N89, N93, N97, N101, N105, N109, N113, N117,  
N121, N125, N129, N130, N131, N132, N133, N134, N135, N136,  
N137;

**output**  
N724, N725, N726, N727, N728, N729, N730, N731, N732, N733,  
N734, N735, N736, N737, N738, N739, N740, N741, N742, N743,  
N744, N745, N746, N747, N748, N749, N750, N751, N752, N753,  
N754, N755;

**wire**  
N250, N251, N252, N253, N254, N255, N256, N257, N258, N259,  
N260, N261, N262, N263, N264, N265, N266, N267, N268, N269,  
N270, N271, N272, N273, N274, N275, N276, N277, N278, N279,  
N280, N281, N282, N283, N284, N285, N286, N287, N288, N289,  
N290, N293, N296, N299, N302, N305, N308, N311, N314, N315,  
N316, N317, N318, N319, N320, N321, N338, N339, N340, N341,  
N342, N343, N344, N345, N346, N347, N348, N349, N350, N351,  
N352, N353, N354, N367, N380, N393, N406, N419, N432, N445,  
N554, N555, N556, N557, N558, N559, N560, N561, N562, N563,  
N564, N565, N566, N567, N568, N569, N570, N571, N572, N573,  
N574, N575, N576, N577, N578, N579, N580, N581, N582, N583,  
N584, N585, N586, N587, N588, N589, N590, N591, N592, N593,  
N594, N595, N596, N597, N598, N599, N600, N601, N602, N607,  
N620, N625, N630, N635, N640, N645, N650, N655, N692, N693,  
N694, N695, N696, N697, N698, N699, N700, N701, N702, N703,  
N704, N705, N706, N707, N708, N709, N710, N711, N712, N713,
N714, N715, N716, N717, N718, N719, N720, N721, N722, N723;

xor XOR2_1 (N250, N1, N5);
xor XOR2_2 (N251, N9, N13);
xor XOR2_3 (N252, N17, N21);
xor XOR2_4 (N253, N25, N29);
xor XOR2_5 (N254, N33, N37);
xor XOR2_6 (N255, N41, N45);
xor XOR2_7 (N256, N49, N53);
xor XOR2_8 (N257, N57, N61);
xor XOR2_9 (N258, N65, N69);
xor XOR2_10 (N259, N73, N77);
xor XOR2_11 (N260, N81, N85);
xor XOR2_12 (N261, N89, N93);
xor XOR2_13 (N262, N97, N101);
xor XOR2_14 (N263, N105, N109);
xor XOR2_15 (N264, N113, N117);
xor XOR2_16 (N265, N121, N125);
and AND2_17 (N266, N129, N137);
and AND2_18 (N267, N130, N137);
and AND2_19 (N268, N131, N137);
and AND2_20 (N269, N132, N137);
and AND2_21 (N270, N133, N137);
and AND2_22 (N271, N134, N137);
and AND2_23 (N272, N135, N137);
and AND2_24 (N273, N136, N137);
xor XOR2_25 (N274, N1, N17);
xor XOR2_26 (N275, N33, N49);
xor XOR2_27 (N276, N5, N21);
xor XOR2_28 (N277, N37, N53);
xor XOR2_29 (N278, N9, N25);
xor XOR2_30 (N279, N41, N57);
xor XOR2_31 (N280, N13, N29);
xor XOR2_32 (N281, N45, N61);
xor XOR2_33 (N282, N65, N81);
xor XOR2_34 (N283, N97, N113);
xor XOR2_35 (N284, N69, N85);
xor XOR2_36 (N285, N101, N117);
xor XOR2_37 (N286, N73, N89);
xor XOR2_38 (N287, N105, N121);
xor XOR2_39 (N288, N77, N93);
xor XOR2_40 (N289, N109, N125);
xor XOR2_41 (N290, N250, N251);
xor XOR2_42 (N293, N252, N253);
xor XOR2_43 (N296, N254, N255);
xor XOR2_44 (N299, N256, N257);
xor XOR2_45 (N302, N258, N259);
xor XOR2_46 (N305, N260, N261);
xor XOR2_47 (N308, N262, N263);
xor XOR2_48 (N311, N264, N265);
xor XOR2_49 (N314, N274, N275);
xor XOR2_50 (N315, N276, N277);
xor XOR2_51 (N316, N278, N279);
xor XOR2_52 (N317, N280, N281);
xor XOR2_53 (N318, N282, N283);
xor XOR2_54 (N319, N284, N285);
xor XOR2.55 (N320, N286, N287);
xor XOR2.56 (N321, N288, N289);
xor XOR2.57 (N338, N290, N293);
xor XOR2.58 (N339, N296, N299);
xor XOR2.59 (N340, N290, N296);
xor XOR2.60 (N341, N293, N299);
xor XOR2.61 (N342, N302, N305);
xor XOR2.62 (N343, N308, N311);
xor XOR2.63 (N344, N302, N308);
xor XOR2.64 (N345, N305, N311);
xor XOR2.65 (N346, N266, N342);
xor XOR2.66 (N347, N267, N343);
xor XOR2.67 (N348, N268, N344);
xor XOR2.68 (N349, N269, N345);
xor XOR2.69 (N350, N270, N338);
xor XOR2.70 (N351, N271, N339);
xor XOR2.71 (N352, N272, N340);
xor XOR2.72 (N353, N273, N341);
xor XOR2.73 (N354, N314, N346);
xor XOR2.74 (N367, N315, N347);
xor XOR2.75 (N380, N316, N348);
xor XOR2.76 (N393, N317, N349);
xor XOR2.77 (N406, N318, N350);
xor XOR2.78 (N419, N319, N351);
xor XOR2.79 (N432, N320, N352);
xor XOR2.80 (N445, N321, N353);
not NOT1.81 (N554, N354);
not NOT1.82 (N555, N367);
not NOT1_83 (N556, N380);
not NOT1_84 (N557, N354);
not NOT1_85 (N558, N367);
not NOT1_86 (N559, N393);
not NOT1_87 (N560, N354);
not NOT1_88 (N561, N380);
not NOT1_89 (N562, N393);
not NOT1_90 (N563, N367);
not NOT1_91 (N564, N380);
not NOT1_92 (N565, N393);
not NOT1_93 (N566, N419);
not NOT1_94 (N567, N445);
not NOT1_95 (N568, N419);
not NOT1_96 (N569, N432);
not NOT1_97 (N570, N406);
not NOT1_98 (N571, N445);
not NOT1_99 (N572, N406);
not NOT1_100 (N573, N432);
not NOT1_101 (N574, N406);
not NOT1_102 (N575, N419);
not NOT1_103 (N576, N432);
not NOT1_104 (N577, N406);
not NOT1_105 (N578, N419);
not NOT1_106 (N579, N445);
not NOT1_107 (N580, N406);
not NOT1_108 (N581, N432);
not NOT1_109 (N582, N445);
not NOT1_110 (N583, N419);
not NOT1_111 (N584, N432);
not NOT1_112 (N585, N445);
not NOT1_113 (N586, N367);
not NOT1_114 (N587, N393);
not NOT1_115 (N588, N367);
not NOT1_116 (N589, N380);
not NOT1_117 (N590, N354);
not NOT1_118 (N591, N393);
not NOT1_119 (N592, N354);
not NOT1_120 (N593, N380);
and AND4_121 (N594, N554, N555, N556, N393);
and AND4_122 (N595, N557, N558, N380, N559);
and AND4_123 (N596, N560, N367, N561, N562);
and AND4_124 (N597, N354, N563, N564, N565);
and AND4_125 (N598, N574, N575, N576, N445);
and AND4_126 (N599, N577, N578, N432, N579);
and AND4_127 (N600, N580, N419, N581, N582);
and AND4_128 (N601, N406, N583, N584, N585);
or OR4_129 (N602, N594, N595, N596, N597);
or OR4_130 (N607, N598, N599, N600, N601);
and AND5_131 (N620, N406, N566, N432, N567, N602);
and AND5_132 (N625, N406, N568, N569, N445, N602);
and AND5_133 (N630, N570, N419, N432, N571, N602);
and AND5_134 (N635, N572, N419, N573, N445, N602);
and AND5_135 (N640, N354, N586, N380, N587, N607);
and AND5_136 (N645, N354, N588, N589, N393, N607);
and AND5_137 (N650, N590, N367, N380, N591, N607);
and AND5_138 (N655, N592, N367, N593, N393, N607);
and AND2.139 (N692, N354, N620);
and AND2.140 (N693, N357, N620);
and AND2.141 (N694, N380, N620);
and AND2.142 (N695, N393, N620);
and AND2.143 (N696, N354, N625);
and AND2.144 (N697, N367, N625);
and AND2.145 (N698, N380, N625);
and AND2.146 (N699, N393, N625);
and AND2.147 (N700, N354, N630);
and AND2.148 (N701, N367, N630);
and AND2.149 (N702, N380, N630);
and AND2.150 (N703, N393, N630);
and AND2.151 (N704, N354, N635);
and AND2.152 (N705, N367, N635);
and AND2.153 (N706, N380, N635);
and AND2.154 (N707, N393, N635);
and AND2.155 (N708, N406, N640);
and AND2.156 (N709, N419, N640);
and AND2.157 (N710, N432, N640);
and AND2.158 (N711, N445, N640);
and AND2.159 (N712, N406, N645);
and AND2.160 (N713, N419, N645);
and AND2.161 (N714, N432, N645);
and AND2.162 (N715, N445, N645);
and AND2.163 (N716, N406, N650);
and AND2.164 (N717, N419, N650);
and AND2.165 (N718, N432, N650);
and AND2.166 (N719, N445, N650);
and AND2.167 (N720, N406, N655);
and AND2.168 (N721, N419, N655);
and AND2.169 (N722, N432, N655);
and AND2.170 (N723, N445, N655);
xor XOR2.171 (N724, N1, N692);
xor XOR2.172 (N725, N5, N693);
xor XOR2.173 (N726, N9, N694);
xor XOR2.174 (N727, N13, N695);
xor XOR2.175 (N728, N17, N696);
xor XOR2.176 (N729, N21, N697);
xor XOR2.177 (N730, N25, N698);
xor XOR2.178 (N731, N29, N699);
xor XOR2.179 (N732, N33, N700);
xor XOR2.180 (N733, N37, N701);
xor XOR2.181 (N734, N41, N702);
xor XOR2.182 (N735, N45, N703);
xor XOR2.183 (N736, N49, N704);
xor XOR2.184 (N737, N53, N705);
xor XOR2.185 (N738, N57, N706);
xor XOR2.186 (N739, N61, N707);
xor XOR2.187 (N740, N65, N708);
xor XOR2.188 (N741, N69, N709);
xor XOR2.189 (N742, N73, N710);
xor XOR2.190 (N743, N77, N711);
xor XOR2.191 (N744, N81, N712);
xor XOR2.192 (N745, N85, N713);
xor XOR2.193 (N746, N89, N714);
xor XOR2.194 (N747, N93, N715);
Chapter A: Benchmark Circuits

xor XOR2_195 (N748, N97, N716);
xor XOR2_196 (N749, N101, N717);
xor XOR2_197 (N750, N105, N718);
xor XOR2_198 (N751, N109, N719);
xor XOR2_199 (N752, N113, N720);
xor XOR2_200 (N753, N117, N721);
xor XOR2_201 (N754, N121, N722);
xor XOR2_202 (N755, N125, N723);

endmodule

The layout implementation of the circuit use a total area of $2300 \times 1400 \mu m^2$, and the final layout is shown on Figure A.6.

Figure A.6: Layout of the C499 circuit, generated on Mentor Graphics IC-Studio.
A.3 ISCAS 85 C499: 32-Bit Single-Error-Correcting Circuit:
Appendix B

Highly correlated Paths Selection

B.1 Simple Correlation Approach

The Algorithm 2 implements the heuristics proposed in section 4.3, which are used to select the most suitable set of path to implement the simple correlation approach of the methodology proposed in chapter 2.

Algorithm 2 Paths Selection on a Simple Correlation Approach.

1: Set: objective path $PO$  
2: Read: locations of each objective path’s gates  
3: $N_O =$ Number of gates in objective path  
4: $Num_cand = $ Number Of candidate paths  
5: $CP =$ Candidate path  
6: $k = 1$  
7: while $Num_cand \geq 0$ do  
8: $N_C =$ Number of gates in $CP(k)$  
9: Aux=AIGD between $PO$ and $CP(k)$  
10: $Num_cand --; k ++$  
11: end while  
12: Paths Pre-selection: $SetA =$the 5 paths with the lowest AIGD  
13: Selected path $PA =$ the shortest path in $SetA$  
14: ::
B.2 Multiple Correlation Approach

Algorithm 3 implement the heuristics proposed in section 4.3.1.2 that selects those paths that maximize the multiple correlation and minimize the effects of multicollinearity in the multiple correlation approach of the methodology proposed in section 2.

Algorithm 3 Paths Selection on a Multiple Correlation Approach.

1: Set Objective Path $PO$ $\triangleright$ Previously Selected Path
2: Read: locations of each objective path’s gates
3: $NO =$ Number of gates in objective path
4: $Num\_cand =$ Number Of candidate paths $\triangleright$ Any other paths on the circuit
5: $CP =$ Candidate Path
6: $k = 1$
7: if Structural Correlation is allowed then $\triangleright$ Implementation of H-structural and H-multiple
8: while $Num\_cand \geq 0$ do $\triangleright$ Implementation of H-spatial
9:  $NC =$ Number of gates in $Candidate\_path(k)$
10:  Calculate AIGD between $PO$ and $Candidate\_Path(k)$
11:  $Num\_cand -=; k +=$
12: end while
13:  ...

if $PA$ is structurally correlated with $PO$ then

$Num\_cand = Number\_Of\_candidate\_paths$

$PO_1 =$ common gates between $PA$ and $PO$

while $Num\_cand \geq 0$ do

if $CP(k)$ is non-structurally correlated with $PO_1$ then

$NC =$ Number of gates in $CP(k)$

Aux=AIGD between $PO_1$ and $CP(k)$

end if

$Num\_cand -=; k +=$

end while

$Num\_cand -=$

$SetB =$ the 5 paths with the lowest AIGD

Selected path $PB =$ the shortest path in $SetB$ $\triangleright$ Implementation of H-length

else

Only one path is needed

end if

Selected paths are $PA$ and $PB$
Chapter B: Highly correlated Paths Selection

14:
First Path Pre-selection: $SetA=$ the 5 paths with the lowest AIGD
15:
Selected path $PA=$ the shortest path in $SetA$                  \> Implementation of $H$-length
16: if $PA$ is Correlated with $PO$ then
17: Set: $PO_1=$ Gates common between $PO$ and $PA$
18: Set: $PO_2=$ Gates that are not common between $PO$ and $PA$
19: $Num_{cand}=$ Number of candidate paths
20: $k = 1$
21: while $Num_{cand} \geq 0$ do $N_C =$ Number of gates in $CP(k)$
22: Aux1(k)= AIGD between $PO_1$ and $CP(k)$
23: Aux2(k)= AIGD between $PO_1$ and $CP(k)$
24: Aux3(k)=Aux1(k)-Aux2(k)            \> Implementation of the negative form of $H$-spatial
25: $Num_{cand} -=; k +=$
26: end while
27: Second Path Pre-selection: $SetB=$ the 5 paths with the lowest Aux3
28: Selected path $PB=$ the shortest path in $SetB$
29: end if
30: Selected Paths are $PA$ and $PB$
31: else
32: Set: $N_P=$ Number of Predictor Paths Considered.
33: $NSP=0$
34: for $j=$number of predictor paths do
35: while $Num_{cand} \geq 0$ do
36: if $CP(k)$ is not structurally correlated with $PO$ then
37: $N_C =$ Number of gates in $CP(k)$
38: Aux1(k)= AIGD between $PO$ and $CP(k)$
39: for $i=1:NSP$ do
40: Aux2(k)$i=$= AIGD between $CP$ and the $i$-th Previously selected Path
41: end for
42: Aux3(k)=Aux1(k)$- \sum_{i=1}^{NSP} Aux(k)_i$            \> Negative form of $H$-spatial
43: end if
44: $Num_{cand} -=; k +=$
45: end while
46: Path Pre-selection: $SetX=$ the 5 paths with the lowest Aux3
47: Selected path $P_j= $ the shortest path in $SetX$
48: $NSP++$
49: end for
50: Selected Paths are $P_1\ldots NSP$
51: end if
B.2 Multiple Correlation Approach
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