Study of the MOS Transistor for Applications in RF Circuits

by

Fabián Zárate Rincón

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Advisors:

Dr. Roberto Murphy Arteaga, INAOE
Dr. Reydezel Torres Torres, INAOE

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Resumen

En los últimos años se han incrementado los intereses en el diseño de circuitos basados en tecnología CMOS para aplicaciones de más altas frecuencias en la academia y en la industria tales como las empresas taiwanesas TSMC y UMC. Por ejemplo en el diseño de amplificadores de bajo ruido (LNA, por sus siglas en inglés), osciladores controlados por voltaje (VCO, por sus siglas en inglés) y otros. Esto se suma a la disminución de la longitud del canal de los dispositivos que en un comienzo pronosticó la ley de Moore, lo cual da como resultado el aumento en la velocidad y en la transconductancia. Actualmente, las empresas líderes del mercado en cuanto a la fabricación de circuitos como son UMC y TSMC trabajan en tecnologías desde 40 nm hasta 250 nm y avanzan en la implementación de 28 nm. De hecho, la caracterización de transistores sobre oblea en altas frecuencias da como resultado nuevas metodologías de extracción de los elementos del circuito equivalente de pequeña señal y sugerencias para modelos compactos como BSIM, PSP y EKV.

Aunque el transistor es un dispositivo de 4 terminales, este es usualmente medido a través de un analizador de redes vectorial (VNA, por sus siglas en inglés) de dos puertos a causa de las limitaciones existentes en algunos laboratorios, colocando en corto las terminales de fuente y substrato. Como consecuencia de esto, la evaluación de cada parámetro no puede ser modelada como una función del voltaje entre fuente y substrato. Esto es resuelto mediante el uso de dispositivos con una terminal separada para el substrato y una punta de prueba de DC, siendo útil no solo para desarrollar una metodología de extracción precisa sino también para establecer una condición apropiada del estrés de dispositivos por la inyección de portadores calientes en la compuerta. Así, una metodología de extracción de los elementos del circuito equivalente en pequeña señal es propuesta, incluyendo el análisis de la degradación del MOSFET por portadores calientes.

Por otro lado, la correspondiente variación del transistor MOS como consecuencia de la dependencia de las parásitas con la geometría intrínseca y extrínseca es estudiada. Para este propósito, un conjunto de dispositivos con

diferente longitud de compuerta y otro con diferentes números de dedos fueron medidos en alta frecuencia. Posteriormente, un modelo escalable que está en concordancia con los datos experimentales es obtenido.

Abstract

In recent years, there has been a growing interest in circuit design based on CMOS technology for higher frequency applications in academia and industry such as Taiwanese companies TSMC and UMC. For instance, this is the case in the design of low noise amplifiers (LNA) and voltage controlled oscillator (VCO). Moreover, the channel length is scaled down as it was initially predicted by Moore's Law, which results in an increasing of switching speed and transconductance. Currently, market leader companies in terms of circuit manufacturing such as TSMC and UMC are working in technology nodes from 40 nm to 250 nm and the implementation of 28 nm is in progress. Indeed, on-wafer MOSFET characterization at high frequency gives place to new extraction methods of equivalent circuit elements and suggestions for compact models such as BSIM, PSP and EKV.

Even though the transistor is a four-terminal device, this is usually measured by means of a 2-port vector network analyzer because of the limitation in some laboratories and then, the source and substrate terminals are tied each other. As a consequence of this, the assessment of each parameter cannot be modeled as a function of the bulk-to-source voltage. In order to address this, a separate bulk terminal and a DC probe are used to properly take into account the effect of the substrate, which is not only useful for developing a correct extraction methodology but also for establishing a suitable hot-carrier stress condition. As a result of this, an accurate extraction methodology of the small-signal equivalent circuit elements under different bulk-to-source voltages is proposed, including the analysis of the MOSFET degradation induced by hot carrier injection.

On the other hand, due to the geometry-dependent parasitics of the MOSFET, its corresponding variation with both intrinsic and extrinsic components is studied. For this purpose, a set of devices with different gate length and another one with different number of fingers were measured at high frequency. Then, a suitable scalable model that is in a good agreement with experimental data is provided.

1 INTRODUCTION

CMOS process has been studied for many years with the aim of understanding how the applied input signal and the corresponding output signal are related to each other, which allows us to propose adequate models. Consequently, its behavior in each of the different regions of operation has been described by a variety of small signal models. These can be added to compact models such as BSIM, which have been used by integrated circuit designers with the purpose of developing simulations prior to manufacturing prototypes. Due to the constant and rapid advancement of technology focused on down-scaling and the use of higher frequencies, new challenges and problems must be continuously evaluated and overcome. Thus in this chapter, the state of the art associated with the study of the MOS transistor and the importance of characterization of this device through RF measurements are presented.

1.1 STATE OF THE ART

Even though CMOS process was not initially considered for applications at high frequencies due to the lower switching speed in comparison with bipolar technology and materials with high electron mobility, it has been currently considered after shrinking the gate length. Following this trend, MOSFET plays an important role because it is a very well-established mass-production and low cost technology with a considerable cut-off frequency [**1**], [**2**]. Indeed, the boom in modern RF systems is mainly associated with the development of the transistor, which is based on the increasing of switching speed and a higher level of integration [**3**]. As a result of the widespread usage of CMOS circuitry[**4**], a thorough knowledge about these devices has become mandatory. The continuous development of the MOSFET with the aim of achieving a better performance makes necessary the characterization and modeling of the device. In this direction, measured S-parameters can be used to develop suitable extraction methodologies for the circuit equivalent elements. It can be obtained through a single device without involving data regressions requiring either devices with different geometries or multiple bias points.

In most of the MOSFET models, equivalent circuit elements used to reproduce S-parameter measurements are related to physical parameters such as mobility, threshold voltage, carrier concentration, junction depth and others [**5**]. Based on this, there is a variety of studies that determine important parameters or put in evidence the existence of new effects when geometry and biasing change. For instance, it has been reported the reliability characterization to study the MOSFET degradation [**6**], the voltage limit where diffusion and drift mechanisms overlap [**7**], the non-quasi-static effect of gate resistance [**8**], the inductive behavior under breaking regime [**9**], and the variation of junction capacitances, threshold voltage and transconductance with the substrate voltage [**10**]. In this way, valuable information for IC manufacturer and those who make compact models including DC operating point, large signal and small signal is provided. Furthermore, circuits at higher frequencies have been designed, which requires of the correct characterization of the transistor [**11**] , [**12**], [**13**].

1.2 MOSFET CHARACTERIZATION

Currently, MOSFETs have reached cutoff frequencies of the order of hundreds of gigahertz, which has given place to the use of these devices in modern microwave applications. In this way, the characterization stage plays an important role in the analysis of the associated parasitics and the influence of these in the figures-of-merit. This should be done in both RF and DC regimes to obtain a complete knowledge about the variation of the transistor parameters with biasing, frequency and geometry. After performing high frequency measurements, important equivalent circuit elements can be extracted from experimental data such as the substrate parasitic network, the series parasitic resistances, the channel resistance and the transconductance. It is remarkable that all of these impact the MOSFET performance in a certain degree. As a result of this, the channel resistance limits its use as an ideal current source, the series parasitic resistances generate a voltage drop and reduce the drain current, the substrate elements provide a path to the flow of an uncontrolled current through the substrate and the transconductance is directly related to the cut-off frequency.

As a result of the characterization of RF CMOS, the development of parameter extraction methodologies and the suggestion of improvements in compact models

like EKV, PSP and BSIM is done. Recently, the University of California in Berkeley released its new model known as BSIM6, which includes both DC and RF analysis [**5**]. Thus, different small signal equivalent circuit topologies to represent the transistor have been proposed, indicating the steps to determine each one of its elements. However, these topologies are modified to maintain good predictions of the device characteristics when it is scaled down. In old technologies (gate length greater than or equal to 1 micron), second order effects such as channel length modulation (CLM) and drain induced barrier lowering (DIBL) do not drastically impact the transistor. On the contrary, the current technologies have a high dependence on secondary effects and these should be considered in the models. In the industry, there is a large set of dimensions available and for instance in the case of the Taiwanese manufacturer UMC, they are fabricating devices with channel length from 28 nm to 40 microns [**4**].

In order to characterize the transistor under different biasing and geometry, a set of multi-finger RF MOSFETs under ground-signal-ground (GSG) pads configuration, varying gate length, number of fingers and considering various operation points, are necessary. Furthermore, the calibration of the experimental assembly should be done to subtract the effects associated with cables, connectors and probes. After doing this, the undesirable effects due to the pads are removed by using a de-embedding procedure. Once corrected data are available, it is possible to obtain the small signal equivalent circuit elements that represent the behavior of the transistor. It is noteworthy that as the MOSFET has 4 terminals, the study of variations of it with substrate voltage is needed.

1.3 Calibration of Experimental Assembly

When frequency increases, it is not possible to make a perfect open circuit or short circuit because of the presence of parasitic inductances and capacitances; thus, Z- or Y-parameters cannot be used to directly measure the device under test (DUT). Therefore, S-parameter measurements related to the transmission and reflection of signals are carried out by using a vector network analyzer (VNA). Then, the Z- and Y-parameters are determined by means of the transformation from S parameters [**14**].

To perform S parameter measurements, a high frequency AC signal and a DC bias related to the operating points in a transistor are simultaneously applied to DUT. In particular bias regions of the MOSFET, the effects of some elements of the equivalent circuit are stronger than the others. Thus, the number of equations can be reduced, neglecting the elements that do not significantly influence the simulations. Furthermore, the AC input signal is called incident wave (a_1). Part of a_1 is reflected towards the source (b_1), while the other part is transmitted to the load (b_2). In turn, if the load is not matched, there will be reflection on port 2 (a_2). The values of a_1, a_2, b_1 and b_2 are given in function of the square root of the power. The S parameter matrix can be written as follows:

$$\begin{aligned} b_1 &= S_{11} \cdot a_1 + S_{12} \cdot a_2 \\ b_2 &= S_{21} \cdot a_1 + S_{22} \cdot a_2 \end{aligned} \tag{1.1}$$

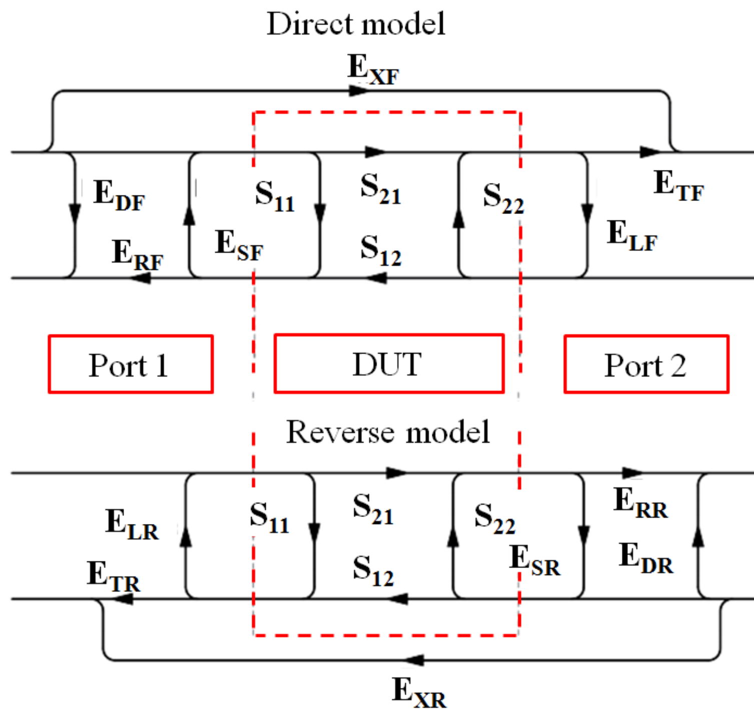

Figure 1.1. *Diagram of error terms for a two-port network in which the notations of the subscripts are F – forward, R – reverse, D - directivity, S – coupling to the source, R - reflection, X - isolation, L – coupling to the load, T - transmission. S-parameters are also shown.*

After locating probes on pads and ensuring that the successful landing of all needles is done, calibration is performed by using a well-known standard procedure, which must be completed for each measurement session. As a result of this, the subtracting of the undesirable effects associated with cables, connectors and probes is achieved. It should be noted that there are three general types of errors such as:

1. Systematic errors: These are due to imperfections in components, connectors, test structures, among others.
2. Random errors: These unpredictably vary with time and cannot be removed, for example when a noise signal is presented.
3. Derivatives errors: These are caused by changes in the characteristics after calibration has been done due to temperature, humidity and other environmental variables.

The effects related to systematic errors can be removed from the S parameters of the DUT using calibration techniques [**15**], [**16**], [**17**]. In this way, the correct measurement of the studied structure is guaranteed and a calibration plane is obtained. A set of error terms involved with the transmission and reflection coefficients of the different standards is illustrated in Figure 1.1. Following this, a system of equations which results from the known standard substrates and measured values is obtained. Currently, measurement equipments are based on 12 errors terms.

The structures, thru, load, open and short, required to completely calculate the error terms are grouped into the standard substrate, which is provided by the equipment manufacturer. For this work, the reference 101-190C and serial SN 45085 from CASCADE was used, bringing together the test structures previously mentioned. In the literature, there are several calibration algorithms such as SOLT (Short-Open-Load-Thru), TRL (Thru-Reflect-Line) [**18**] and LRM (Line-Reflect-Match) [**19**], which have been implemented in the VNA and allow solving a series of equations that involve the errors terms. Thus, the error due to the deviation between true measurements of the device under test (DUT) and measurements obtained in practice is eliminated. For clarity in Figure 1.2, standards schemes are presented, indicating the input and output ports.

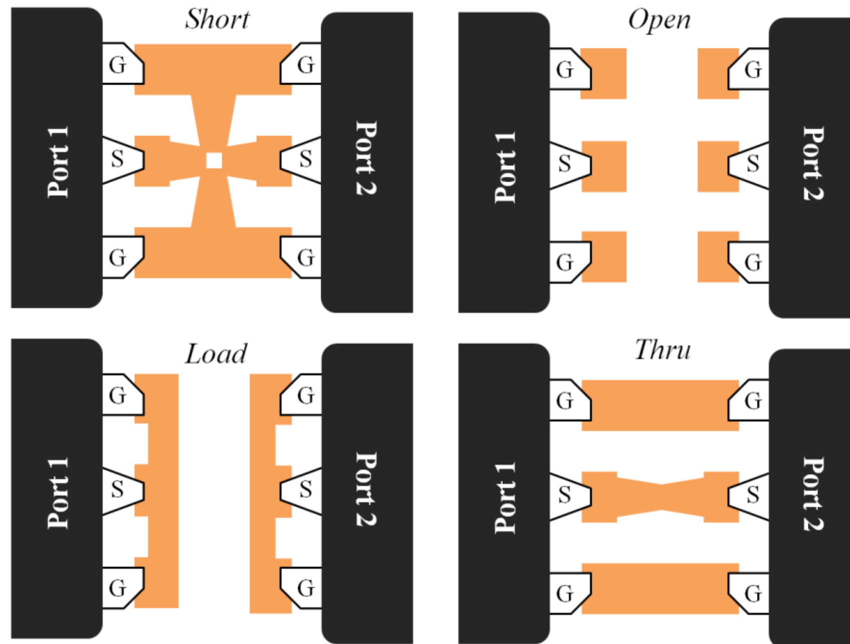

Figure 1.2. *Common structures in an impedance standard substrate (ISS).*

1.4 EXPERIMENTAL ASSEMBLY

Figure 1.3 and Figure 1.4 show schematics of the experimental setup, indicating the necessary equipment to carry out measurements MOSFETs at high frequency. Basically, this is formed by Agilent E8361A vector network analyzer (VNA) and Keysight B1500A semiconductor device analyzer (SDA) that allow us to apply the corresponding AC signal and biasing. Furthermore, the power supply is connected to the DUT via the VNA, which is enable by a bias-T. The GSG coplanar probes for microwave frequencies with 100 microns of separation between needles, connected to the input and output ports of the device pads, are also illustrated.

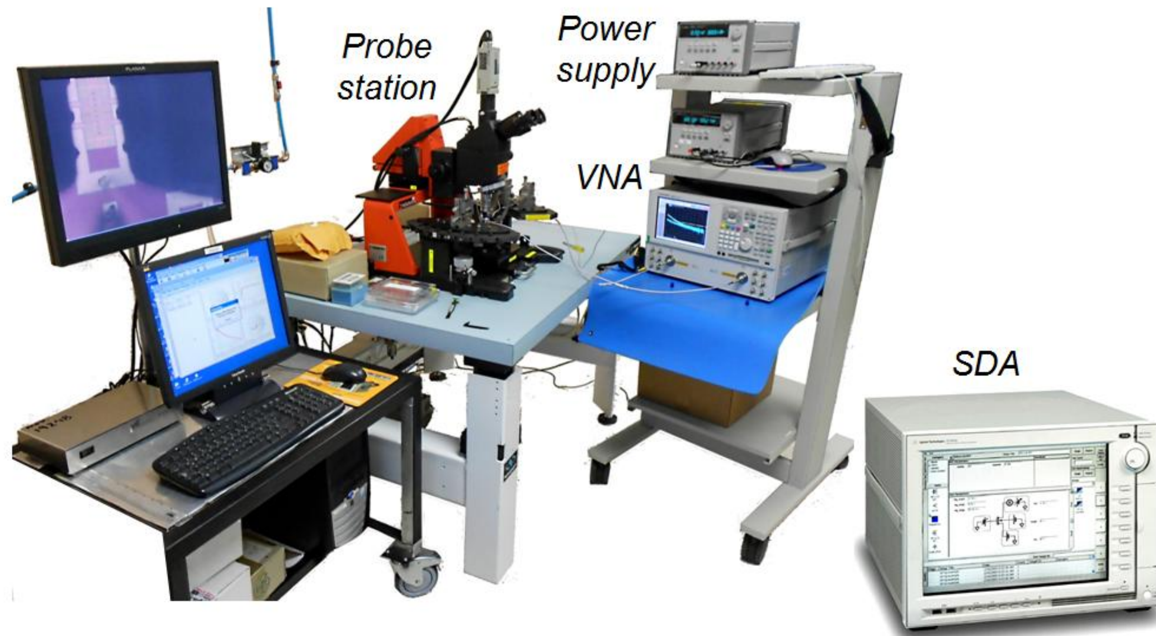

Figure 1.3. *Experimental setup for measurements of RF NMOSFET devices with separate terminal for the substrate.*

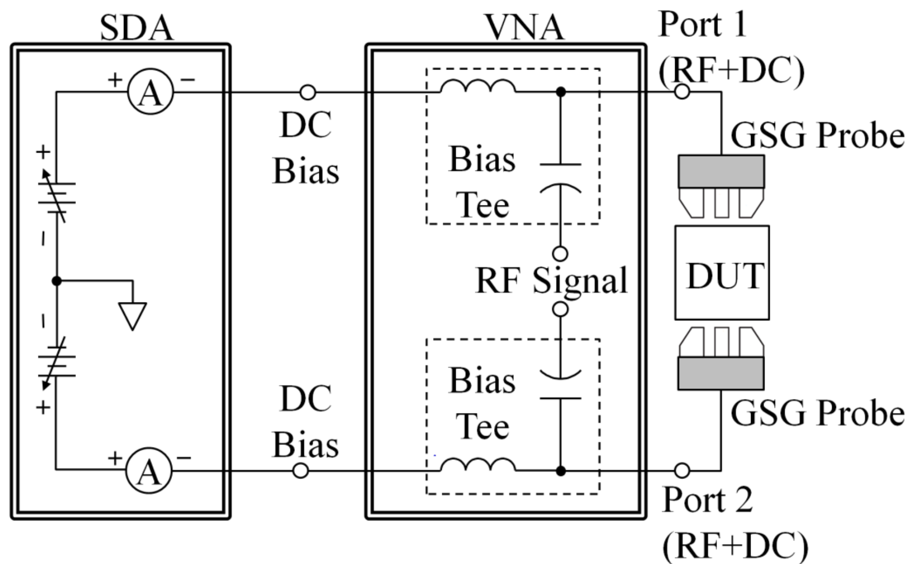

Fig. 1.4. *Schematic of the experimental setup used to perform RF measurements under different bias conditions.*

1.5 DE-EMBEDDING OF THE DEVICE UNDER TEST

In order to do the proper characterization of the DUT of micrometer dimensions, a pad with the right size is also fabricated to locate the probes, see Figure 1.5. However, this involves a parasitic effect that can be seen as a set of admittances or impedances configured at π or T circuit topologies, respectively. The procedure of removing these elements is known as de-embedding [**20**], [**21**], which is a following step to the equipment calibration. For this purpose, it is necessary to implement the open and short structures on the same silicon wafer where the DUT will be measured. In [**22**], the previously mentioned dummy structures are represented through an equivalent circuit. For this, the corresponding inductances, capacitances and resistances are due to the copper conductors, the levels of metal, and the insulating paths.

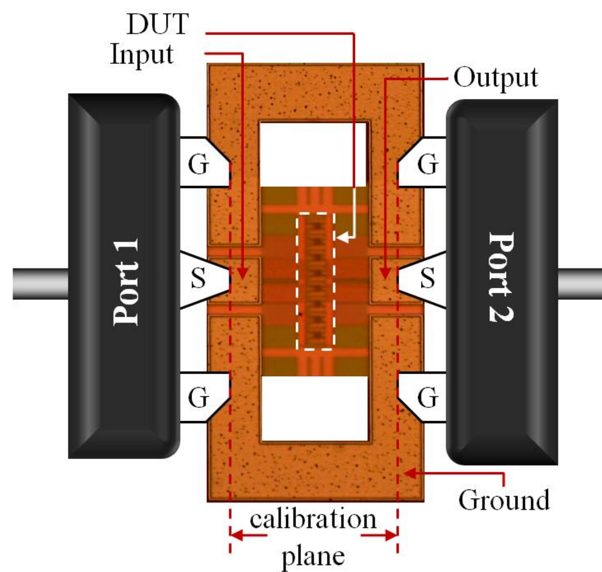

Figure 1.5. *Scheme of the ground-signal-ground pads, the device under test and the input and output probes, indicating the calibration plane.*

1.6 SMALL SIGNAL MODEL

Basically, the idea of the MOSFET is to control the flow of current between source and drain by using the gate voltage [**23**], [**24**]. For this reason, one of the most important parameters to take into account is the transconductance that is

related to the input voltage and the output current. Furthermore, the value of this parameter is proportionally dependent on the ratio of the width of the channel to its length. However, this consideration has certain limitations in respect with the fabrication process and the parasitic effects. For instance in the case of a short and wide channel design, a large resistance value distributed along the gate becomes evident. This undesirable effect can be reduced through the fabrication of MOSFETs with multiple fingers, as shown in Figure 1.6. This figure also illustrates the shallow trench isolation (STI), the lightly doped drain (LDD) regions and the terminals. STI reduces the uncontrolled current that flows through the substrate [**24**] and LDD regions decreases the electric field between source and drain. In addition, much research has been done with the aim of reducing the thickness of the oxide and of developing high dielectric constant insulators such as hafnium, nitrogen and other chemical elements. Even when hafnium is a good candidate to replace the silicon dioxide, it has the drawback that the charge is trapped into the insulator, which will be reflected in the gate-to-source and gate-to-drain capacitances.

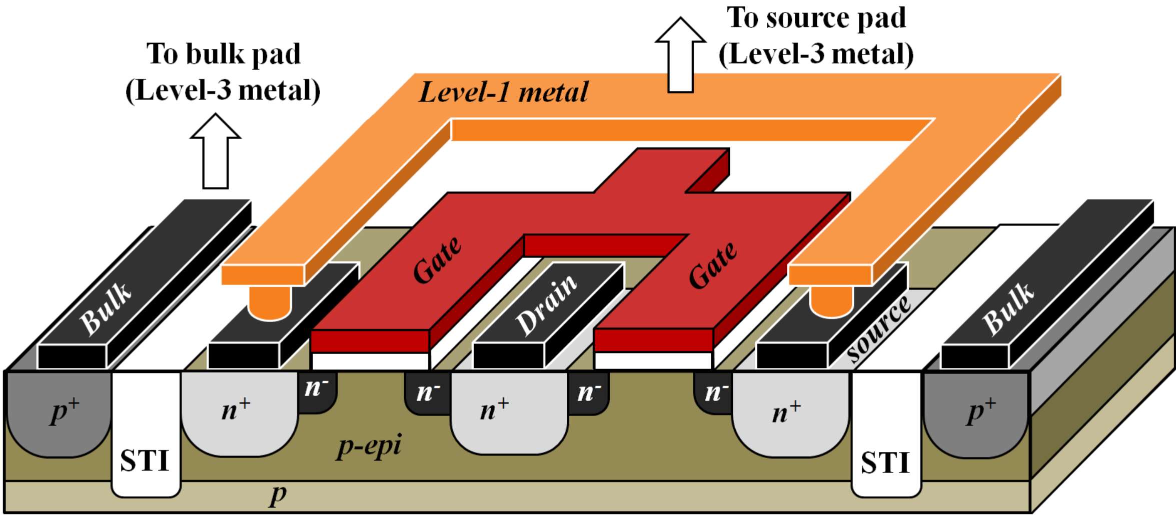

Figure 1.6. *Scheme of an RF MOSFET with two fingers.*

Even though the MOSFET has been studied for many years, the analysis of its equivalent circuit elements and physical parameters is still a recent topic because of its continuous development and use at higher operating frequencies. This is due to the need of fabricating high performance RF circuits, which can currently reach

frequencies of the order of tens of gigahertz [**12**] and even more [**13**]. Subsequently, this brings new challenges to be solved. For example, in sub-micron technologies for the case of MOS transistors, the slope of the drain current as a function of drain voltage in saturation is greater than zero, which is attributed to the short channel effects, DIBL and CLM. In turn, the DIBL effect involves variations in the threshold voltage.

In order to assume a linear relationship between the input signal and its response, the amplitude of the AC signal is much smaller than the values given for the DC operating point[**25**]. This facilitates the extraction methodology of the MOSFET parameters to describe the electrical behavior of the device. In turn, prior knowledge of the physics of the device provides enough information to consider a given equivalent circuit topology. Thus, there is a wide range of research getting involved with the development of appropriate small signal models for a given operating region. In Figure 1.7, the elements associated with the small-signal equivalent circuit is illustrated.

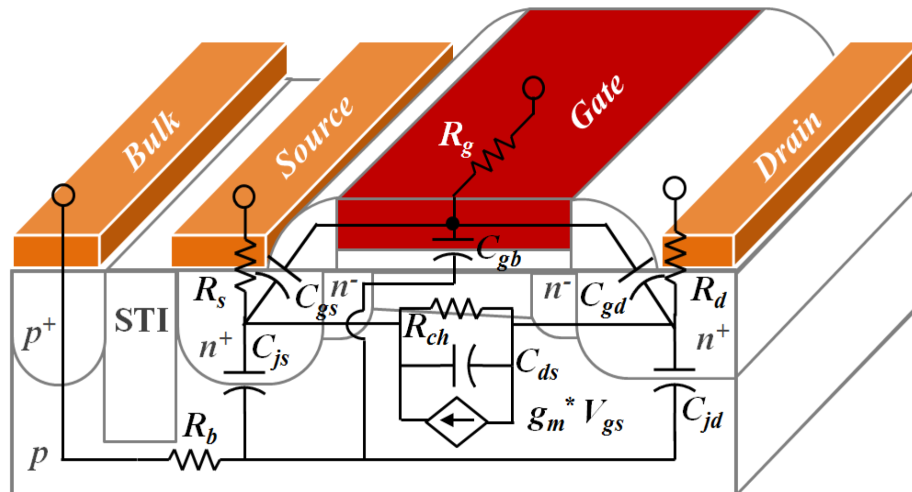

Figure 1.7. *Scheme of the MOSFET, illustrating the small-signal equivalent circuit.*

The MOSFET is essentially a transconductance amplifier with a very large resistance in the input and a current gain in the output. However in practice, it is a non-ideal active device, which should be taken into account to characterize it through small signal regime. The equivalent circuit elements can be separated into two groups in accordance to their influence in the normal operation of the device, which are intrinsic and extrinsic elements [**26**] , [**27**]. In the first place, the intrinsic elements are directly related to the control of the inversion charge into the channel that allows the flow of the drain current. These are integrated by the gate

capacitances C_{gs}, C_{gd} and C_{gb}, the drain-to-source capacitance C_{ds}, the channel resistance R_{ch} and the transconductance g_m. Furthermore, R_{ch} provides information on the presence or absence of charge into the channel due to the electric field generated by the gate voltage, and g_m gives an idea of the ease or difficulty of modulating the inversion charge. Secondly, the extrinsic elements are given by the substrate parasitic network involving the junction capacitances C_{js}, C_{jd} and the substrate resistance R_b, and by the parasitic series resistances R_g, R_s and R_d. It is important to notice that the elements obtained for an RF multiple finger transistor represent the effective values of its corresponding distributed behavior. The equivalent circuit elements are helpful to evaluate different manufacturing processes and identify new effects that become evident in advanced technologies.

In order to fully characterize the transistor, different bias schemes are employed. This is due to the fact that depending on the operating region, some components dominate over others, and fewer components have to be determined in each step. Generally, the first step measures the transistor in the "off" state; the second considers the transistor in strong inversion but without any flow of current (V_{ds} = 0); and the last step measures the transistor in any of the "on" states.

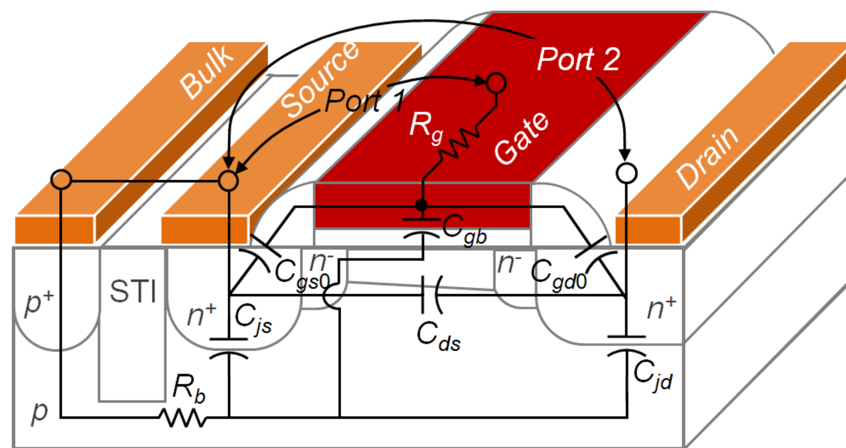

Figure 1.8. *RF-MOSFET at $V_{gs} = V_{ds} = V_{bs} = 0V$.*

The equivalent circuit of the MOSFET in the "off" state (cold condition) in which all applied voltages are fixed at zero is shown in Figure 1.8. Under these bias conditions, the components associated with the extrinsic part of the transistor can be determined, since the transistor is in the "off" state and the intrinsic components do not play a part in the response. A quick glance of the Smith Chart, shown in

Figure 1.9, provides the basic information on input and output impedances. The input impedance is due to the Gate resistance and the oxide capacitance, whereas S_{22} gives information on the parasitic capacitances due to Gate overlap and junction capacitances.

As can be seen, S_{11} traces a curve following the r = 0.2 curve, which upon denormalizing can be interpreted as an effective input resistance of about 100 Ω. The output impedance is initially higher, following the r = 0.5 circle, but tends to lower values as the frequency increases.

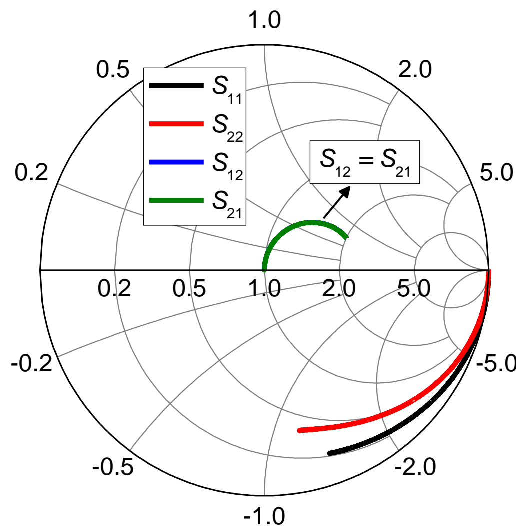

Figure 1.9. *S-Parameters for the MOST under "cold condition" bias.*

Figure 1.10 shows the transistor biased in strong inversion, but with V_{ds} = 0, while Figure 1.11 presents the corresponding S-Parameter Smith Chart. Under this bias condition, the channel is inverted, providing conduction from Drain to Source, but since the potential difference between these terminals is zero, there is no current flow. S_{11} still shows a capacitive behavior, the curve being traced under the r = 0.2 circle. S_{22}, however, is purely resistive, and basically consists of the combination of Source and Drain resistances, in series with the channel resistance, which constitute the output impedance, close to the r = 0.1 circle or equivalent to 50 Ω.

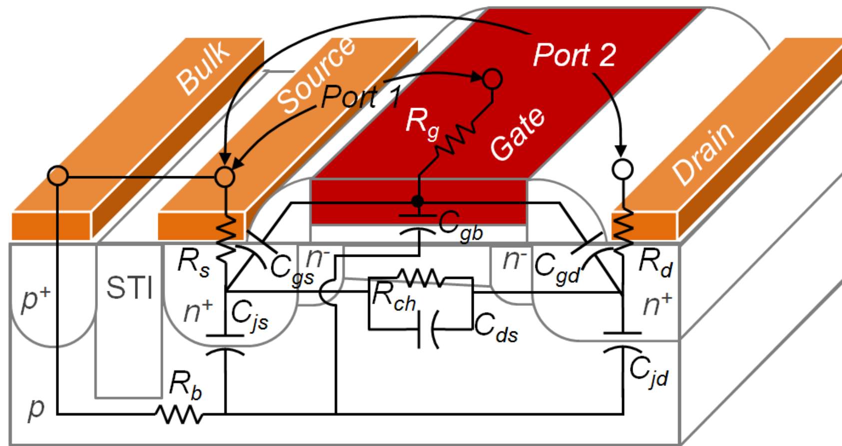

Figure 1.10. *RF-MOSFET in strong inversion at* $V_{gs} = 0.6V$ *and* $V_{ds} = V_{bs} = 0V$.

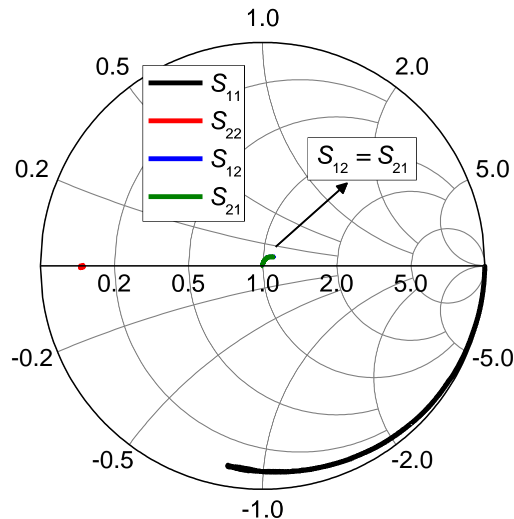

Figure 1.11. *Smith Chart showing the S-Parameters for the MOST biased in strong inversion.*

The device is then biased in the active region; $V_{gs} > V_{th}$ and $V_{ds} > 0$. The channel is formed, and there is a current flow from Drain to Source. Figure 1.12 shows the equivalent circuit for the device, whereas Figure 1.13 presents the S-Parameters for the device operating in the saturation region.

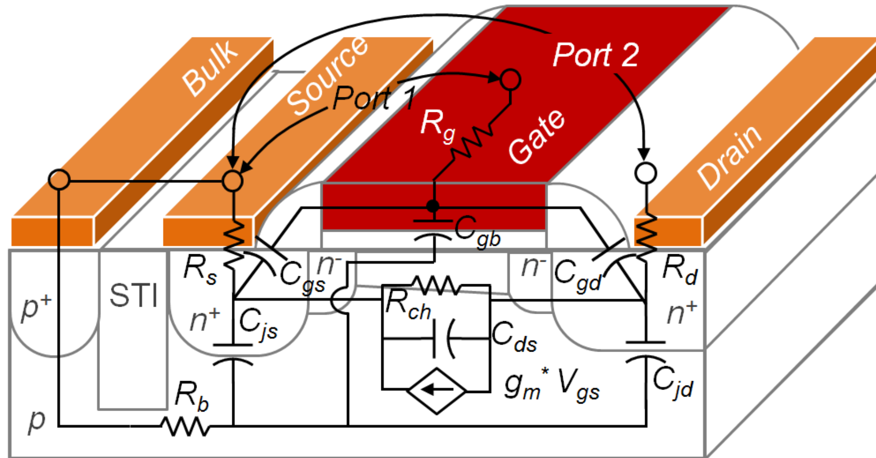

Figure 1.12. *RF-MOSFET in the active region at $V_{gs} = 0.6V$, $V_{ds} = 0.7V$ y $V_{bs} = 0V$.*

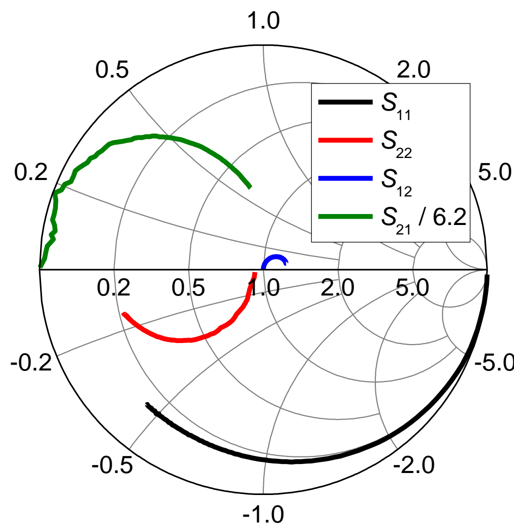

Figure 1.13. *S-Parameter Smith Chart for the device operating in the saturation region.*

S_{11} traces a curve almost following the r = 0.2 circle, but deviates lo lower values as the frequency increases. S_{22} is now purely capacitive for the measurement frequency range, but tending to the upper plane of the chart as frequency increases.

1.7 IMPACT OF THE SUBSTRATE TERMINAL IN MOSFETS

The characterization of the MOSFET in high frequency range is done by S parameter measurements; for this, a vector network analyzer with two ports is commonly used, using a common source-substrate configuration. Thus, the input signal is applied to the gate terminal while the output signal is monitored in the drain terminal. However, this involves that the substrate voltage will be fixed at zero, which is a special case that is not always presented in a real circuit. A more practical configuration is to do not tie the substrate and source terminals with the purpose of analyzing the response of the transistor under various biasing schemes. The flow of current through the substrate parasitic network is undesirable because it is not possible to control it. Notably, the effect due to the parasitic elements becomes more significant at higher operating frequency; therefore, they must be considered in the analysis of circuits. For example, the resistance of the substrate significantly influences the behavior of the cascode amplifier, which is formed by the source-common and gate-common topologies as shown in Figure 1.14. In this amplifier at high frequencies, the maximum gain, minimum noise figure, and the output impedance are improved by the increasing of the substrate resistance of the common-gate transistor in such a way that the operating frequency range can be expanded [**28**].

In addition, some emerging wireless applications such as sensor networks and medical implants must operate with low power consumption. In this regard, the sub-threshold region and the bulk effect have been studied intensively in recent years to maintain the desired decreasing trend in the power consumption. In fact, mixers have been built through the use of body-driven differential amplifiers. However, the transconductance g_{mb} associated with the substrate is less than gm by a factor of 2 to 5 [**29**], [**30**], reducing the cutoff frequency of the transistor. This can be enhanced by appropriate design techniques to avoid affecting the performance of the device. For instance in [**31**], additional differential pairs are introduced to boost g_{mb}, which was manufactured under a CMOS process of 0.35 μm. Additionally, it should be noted that the pn junction between source and substrate may be polarized in reverse or direct; on the contrary, this does not occur in the transistor driven by gate [**29**]. These considerations must be taken into account in the models.

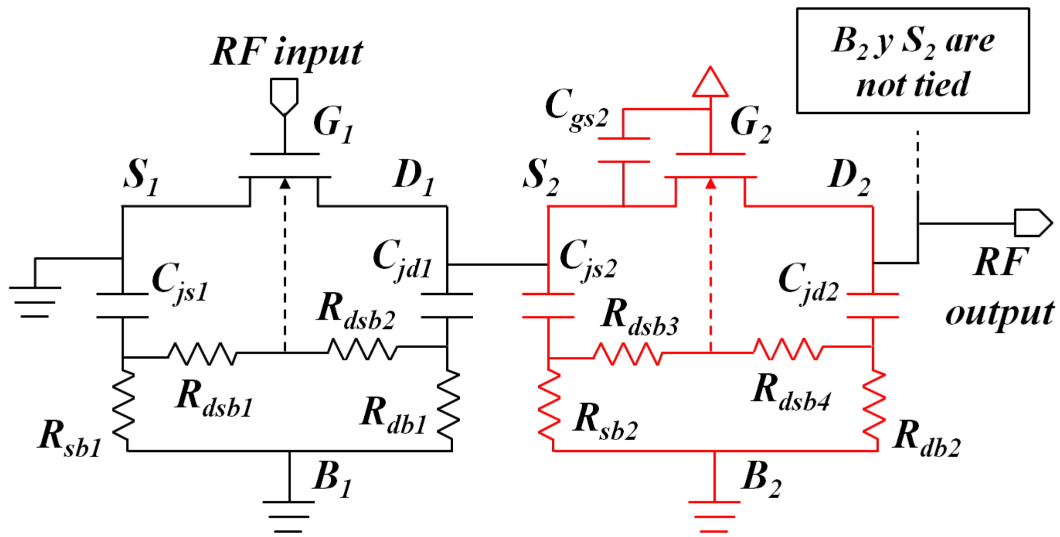

Figure 1.14. *RF CASCODE Amplifier.*

1.8 Purpose and Outline of this Dissertation

The work presented in this dissertation is related to the development of small-signal parameter extraction methodologies of modern MOSFET with the aim of providing enough information for the improvement of compact models for high-frequency applications. In order to achieve this, conventional proposals are reviewed, giving place to important suggestions that allows avoiding the misrepresentation of the circuit equivalent elements associated with the transistor. Accordingly, a novel and significant contribution of the operation of state-of-the-art devices at microwave frequencies is carried out.

The assessment of the performance for microwave MOSFETs is addressed by analyzing the dependence of their corresponding parameters with geometry, forward substrate biasing and reliability in the coming chapters. First of all, in **Chapter 2**, the variation of the bias-dependent channel and series parasitic resistances with the intrinsic geometry is taken into consideration to adjust the traditional DC methods with the purpose of properly determining physical parameters. In addition to this, the undesirable effect of extrinsic geometry on source and drain resistances is also studied through the change of the number of fingers with a fixed total gate width, which allows providing a suitable scalable

model. Furthermore, the analysis of the transistor with a separate DC pad for the substrate terminal operating in the active region at high frequency under different bulk-to-source voltages is presented in **Chapter 3**, extending the study that was previously performed in my master's degree. Once the resultant small-signal models considering geometry and biasing have been developed, the evaluation of the MOSFET degradation due to hot-carrier is made in **Chapter 4** after establishing an appropriate stress condition. Finally, the conclusions are summarized in **Chapter 5**.

2 Analysis of Geometry Dependent Parameters for RF-MOSFETs

Even when there is much research related to the variation of MOSFET's parameters with geometry, its use in challenging applications that requires aggressively scaled devices and operating frequencies of tens of gigahertz makes necessary the continuous characterization of the transistor. In order to address this issue, the dependence of equivalent circuit elements with both intrinsic and extrinsic geometries should be carefully considered to properly remove the undesirable effect of the parasitics, which are more accentuated in sub-100 nm technologies. Therefore, in this chapter, an accurate extraction methodology of small-signal parameters, varying gate length and number of fingers with a fixed gate total width is performed. This procedure is divided into two sections to independently study the impact of the intrinsic and extrinsic geometry on the devices.

2.1 Characterization of the Intrinsic Geometry of the Transistor

The determination of parameters for microwave MOSFETs using DC methods requires that the effect of the bias dependent S/D resistances be removed. This becomes more important as technologies evolve, since this procedure becomes less straightforward. If not taken into account, incorrect values for the basic parameters for the MOSFET are obtained, especially those associated with the channel. To solve this problem, RF measurements can be performed at different bias conditions to extract and subtract the parasitic components from the total resistance, which allow us to accurately define the desired parameters.

2.1.1 Test Structures for Intrinsic Geometry

With the purpose of characterizing the intrinsic geometry of the transistor, a set of multi-finger RF-MOSFETs in a common source-bulk configuration with three different values of L_g, 80 nm, 90 nm, and 120 nm, were measured. For all devices,

the finger width (W_f) is 3 µm and the number of fingers (N_f), 64. To reduce the coupling through the substrate, a shallow trench isolation (STI) and a ground shield were taken into account for the fabrication process. In turn, the metal-dielectric interface of the gate is based on polysilicon and SiON. The pads formed for probing purposes are made of aluminum and are placed at the top metal layer.

2.1.2 Extraction of the Channel Resistance and the Series Parasitic Resistances

The proposed methodology is focused on the analysis of R_{ch} extracted from the *S*-parameter measurements of MOSFETs with different L_g up to 60 GHz under different applied voltages. To develop this, V_{ds} is fixed at 0 V and V_{gs} is swept in such a way that the operation of the transistor varies from sub-threshold to strong inversion. In these bias conditions, it is possible to guarantee that the device is working in the linear region, in which the assumption that the channel is uniformly inverted can be taken into account. With the aim of accurately determining R_{ch} associated with I_d and V_{th}, much work has been carried out [**32**], [**33**]. This requires the extraction of R_s and R_d, which are defined as functions of V_{gs}. Nevertheless, since the substrate losses in sub-micron technology nodes are considerable when frequency increases, the undesirable effect of the substrate parasitics, R_b, C_{jd} and C_{js}, should be removed from the experimental data previous to finding R_s and R_d.

In order to determine the substrate parasitics, the zero-bias cold-FET condition in which both V_{gs} and V_{ds} are fixed at 0 V is used. As a consequence of this, the inversion channel related to R_{ch} is not formed under the gate dielectric. In this way, it does not make sense to consider R_{ch} in the small-signal equivalent circuit, which allows us to neglect it and facilitate the extraction of C_{jd} and R_b [**34**]. Given that the fabrication process of the source and drain regions are similar each other, C_{js} is more or less equal to C_{jd}. After determining the substrate elements, the removal of their contribution on the experimental *Y*-parameters ($\mathbf{Y_{DUT}}$) can be done, resulting in a corrected *Y*-parameter matrix as follows:

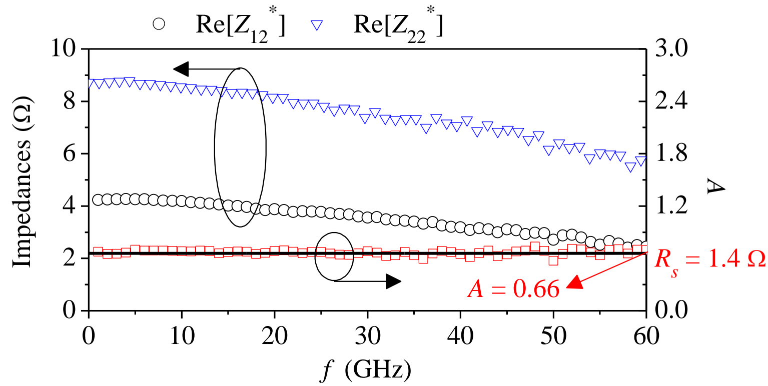

Figure 2.1. *Real part of Z_{12} and Z_{22}, and A with the corresponding linear regression (continuous line) of MOSFETs with L_g = 90 nm at V_{ds} = 0 V and V_{gs} = 0.5 V.*

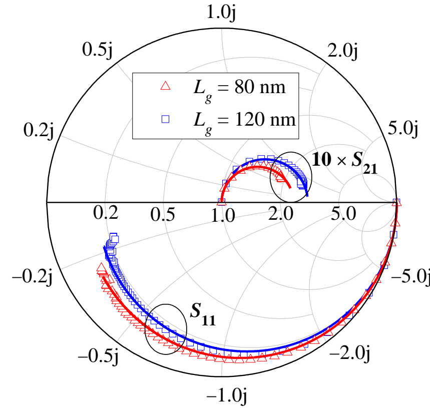

Figure 2.2. *Simulated (continuous line) and measured (symbols) S-parameters up to 60 GHz of MOSFETs with two different gate lengths at V_{ds} = 0 V and V_{gs} = 0.9 V.*

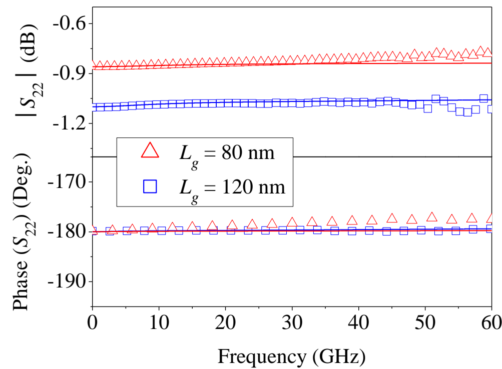

Figure 2.3. *Magnitude and phase of simulated (continuous line) and measured (symbols) S_{22} up to 60 GHz of MOSFETs with two different gate lengths at V_{ds} = 0 V and V_{gs} = 0.9 V.*

$$Y^* = Y_{DUT} - \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{\omega^2 C_{jd}{}^2 Z_b}{1+\omega^2 C_{jd}{}^2 Z_b{}^2} + j\dfrac{\omega C_{jd}}{1+\omega^2 C_{jd}{}^2 Z_b{}^2} \end{bmatrix}, \tag{2.1}$$

In this expression, Z_b takes into consideration the parallel combination of R_b and C_{js} when source and substrate terminals are tied each other. Notice that the superscript notation (*) states the Z- or Y-parameters at $V_{gs} > 0$ V after subtracting the substrate parasitics. Once the inversion channel is formed, it behaves as a conductive shield, screening the electric field between gate and substrate related to C_{gb}. For this reason, C_{gb} becomes smaller than all other capacitances and thus, its effect into the equivalent circuit is negligible. Following this assumption, Z_b can be written as:

$$Z_b = \left[(1/R_b) + j\omega C_{js}\right]^{-1}. \tag{2.2}$$

Even though R_b, C_{jd} and C_{js} are functions of V_{bs}, it is not an issue for the measured devices because both source and substrate terminals are grounded. In addition, these elements are weakly dependent of the gate and drain biasing voltages, which means that they can be considered constant for all bias conditions. As a result of this, the removal of C_{js}, C_{jd} and R_b extracted at the zero-bias FET condition can be used for all high frequency measurements under different values of V_{gs} at V_{ds} = 0 V. Then, to define the series parasitic resistances, it is better to use Z-parameters ($\mathbf{Z}^*$) instead of $\mathbf{Y}^*$ since a direct relationship and easy interpretation can be achieved. In the case of the transistor operating within the strong inversion regime at V_{ds} = 0 V, the components of matrix $\mathbf{Z}^*$ satisfy the following expressions [**35**]:

$$\mathrm{Re}[Z_{12}{}^*]\big|_{\omega=0} = R_s + (1/2)R_{ch}, \tag{2.3}$$

$$\mathrm{Re}[Z_{22}{}^*]\big|_{\omega=0} = R_s + R_d + R_{ch}, \tag{2.4}$$

Furthermore, the imaginary part of Y-parameters ($\mathbf{Y}^*$) is given by

$$\mathrm{Im}[Y_{12}^{\ *}] = -\omega C_{gd}, \tag{2.5}$$

$$\mathrm{Im}[Y_{22}^{\ *}] = \omega\left(C_{gd} + C_{ds}\right)A, \tag{2.6}$$

with

$$A = \frac{2Rs^2 - 4\,\mathrm{Re}[Z_{12}^{\ *}]\big|_{\omega=0} Rs + 4\,\mathrm{Re}[Z_{12}^{\ *}]\big|_{\omega=0}^{\ 2}}{\mathrm{Re}[Z_{22}^{\ *}]\big|_{\omega=0}^{\ 2}}, \tag{2.7}$$

$$C_{ds} = \mathrm{Im}[Y_{22}]\big|_{V_{gs}=0} + \mathrm{Im}[Y_{12}]\big|_{V_{gs}=0} - C_{jd}. \tag{2.8}$$

where $\mathrm{Im}[Y_{22}]|_{Vgs=0}$ and $\mathrm{Im}[Y_{12}]|_{Vgs=0}$ correspond to the Y-parameters at zero-bias. In order to extract R_s, the equations (2.5) through (2.8) can be employed. After following this procedure, R_{ch} can be easily determined by (2.3) and R_d, by (2.4). In Figure 2.1, the real part of Z_{12}^* and Z_{22}^* and the corresponding values of parameter A at V_{ds} = 0 V and V_{gs} = 0.5 V are presented. As one can expect from sub-micron transistors, the plotted Z-parameters, that incorporate the contribution of R_{ch}, R_s and R_d are in the order of magnitude of a few ohms. In the case of R_g, it can be found by means of the linear regression of $\mathrm{Re}[Y_{11}^*]/(\mathrm{Im}[Y_{11}^*])^2$ as a function of ω^2 at lower frequencies. Consequently, as soon as the series parasitic resistances are obtained, it is feasible to assess the impact on the MOSFET's input and output impedances by making a comparison of these curves.

To perform an accurate assessment of the resulting elements related to the MOSFET, the simulated data of the small-signal equivalent circuit are compared with the measured S-parameter data at high frequency considering different L_g and bias conditions, as shown in Figure 2.2 through Figure 2.5. According to this, it is possible to correctly reproduce experimental data up to 60 GHz by means of the extracted parameters. Even though the proposal is in agreement with experiment in the major part of frequency range, this is acceptable beyond 50 GHz because the experimental data is scattered, which is due to the open-short de-embedding technique that shows evidence of limited accuracy at these frequencies [**22**].

In order to extend the proposal toward advanced technologies, a similar methodology can be followed because the small-signal equivalent circuit does not significantly change, taking into consideration additional contributions that can exist to some elements. For instance, in the case of finFETs, the effect of the set of parasitic capacitances related to the fin should be included in the gate

capacitances, C_{gs} and C_{gd}. Basically, the fin can be defined in terms of the intrinsic capacitances, C_{gsi} and C_{gdi}, and the external and internal capacitances, C_{fext} and C_{fint}. The relationship of these parameters with C_{gs} and C_{gd} is given by [**36**]:

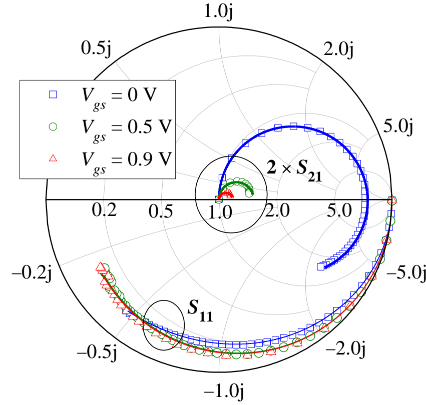

Figure 2.4. *Simulated (continuous line) and measured (symbols) S-parameters up to 60 GHz of MOSFETs with L_g = 80 nm at different V_{gs} and V_{ds} = 0 V.*

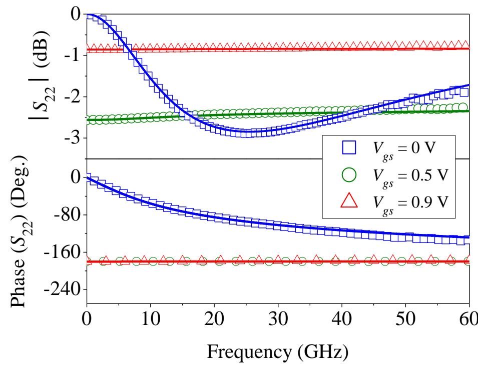

Figure 2.5. *Magnitude and phase of simulated (continuous line) and measured (symbols) S_{22} up to 60 GHz of MOSFETs with L_g = 80 nm at different V_{gs} and V_{ds} = 0 V.*

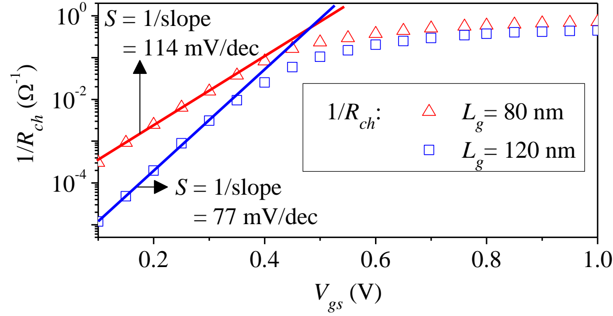

Figure 2.6. *Determination of the subthreshold swing.*

$$C_{gs} = C_{gsi} + C_{fext} + C_{f\,\mathrm{int}}, \tag{2.9}$$

$$C_{gd} = C_{gdi} + C_{fext} + C_{f\,\mathrm{int}}, \tag{2.10}$$

2.1.3 Extraction of Physical Parameters for RF MOSFETs

In view of the fact that R_{ch} for sub-micron technologies in strong inversion is smaller than that for old ones and can reach a value of a few ohms that is of the order of magnitude of R_d and R_s, it is difficult to extract R_{ch} by using DC measurements due to the bias-dependent components of the series parasitic resistances. This issue takes place because LDD regions in both source and drain terminals are used, which becomes also a concern in bulk finFETs [**37**]. As a consequence of this, the resultant voltage drop across R_d and R_s that happens when there is a current flowing from drain to source varies with V_{gs}, which complicates the accurate modeling of I_d. Furthermore, all of the corresponding parameters associated with the transistor can be properly determined by means of RF data. This is an efficient alternative given that the values of all involved resistances can be found at V_{ds} = 0 V, which lets fixing the voltage drop across R_s and R_d at zero.

Even though there is no a flow of current through the channel when the transistor is measured in RF regime under zero-bias condition, an eventual current (I_{ch}) can be observed when an intrinsic voltage (V_{ch}) is applied in the extremes of the channel. Notice that These two parameters allow one to define a relationship between the R_{ch} extracted by using an RF-measurement-based methodology and the MOSFET's parameters that are involved with the I-V characteristic curve. This procedure can be seen for the subthreshold swing (S) as follows

$$S = \left(\frac{d\left[\log_{10}\left(I_{ch}\right)\right]}{dV_{gs}} \right)^{-1}, \tag{2.11}$$

It is important to mention that this equation is defined for a constant value of V_{ch}. Following this fact, S can be rewritten as

$$S = \left(\frac{d\left[\log_{10}\left(I_{ch}\right) - \log_{10}\left(V_{ch}\right)\right]}{dV_{gs}} \right)^{-1}. \tag{2.12}$$

The previous step to describe S is required to express this parameter in terms of $R_{ch} = V_{ch}/I_{ch}$, which is given by

$$S = \left(\frac{d\left[\log_{10}\left(1/R_{ch}\right)\right]}{dV_{gs}} \right)^{-1} \tag{2.13}$$

Notice that S is related to the slope on a semi-logarithmic scale of the inverse of R_{ch} as a function of V_{gs} in the subthreshold region. Once this procedure is employed, the results for S considering transistors with two different gate lengths are presented in Figure 2.6. In this fashion, the extracted values of S are 114 mV/dec for L_g = 80 nm and 77 mV/dec for L_g = 120 nm.

Additionally, in the case of g_m, it can be divided by V_{ch} with the purpose of finding a relationship of this one with R_{ch}, which is given by

$$g_m/V_{ch} = \left(1/V_{ch}\right) \times \left(dI_{ch}/dV_{gs}\right) = d\left[1/R_{ch}\right]/dV_{gs} \tag{2.14}$$

The advantage of applying this equation to analyze g_m instead of the conventional procedure using DC measurements is that it is independent from the series parasitic resistances, which are also related to V_{gs}. Indeed, the common methodology based on the expression dV_{ds}/dI_d involves not only the characteristics of the channel, source and drain regions but also those of the pads. For this reason, in order to avoid any confusion between the total resistance of the transistor (i.e., $R_{total} = R_d + R_s + R_{ch}$) and the resistance extracted from DC data that also includes the pad resistance (R_{pad}), the term R_{DC} (i.e., $R_{DC} = V_{ds}/I_d = R_{total} + R_{pad}$) is defined. Since (2.14) is associated with the I-V characteristic of the MOSFET, the linear extrapolation method can be also performed to obtain V_{th}.

After doing this, V_{th} is found to be equal to 0.33 V for L_g = 80 nm, which is illustrated in Figure 2.7. With the purpose of comparing this result, the second derivative of the logarithm (SDL) method is carried out using[**38**] and then, a similar value for V_{th} is obtained as shown in Figure 2.8. The agreement of RF and SDL techniques happens because in both cases the undesirable effect of R_d and R_s is subtracted from the experimental data. Take into consideration that the second approach is very sensitive to the measurement noise due to the use of the second order derivative that amplifies this noise.

On the other hand, even when a linear trend of R_{DC} as a function of L_g would be expected, this does not occur because of the bias dependence of R_s and R_d, which difficult the extraction of L_{eff} by means of the extrapolation of L_g to the point in which R_{DC} = 0 Ω. Based on this issue, R_s and R_d should be removed from R_{DC} for all considered gate lengths at each value of V_{gs}. In fact, R_{ch} for a transistor operating in the linear region is given by

$$R_{ch} \propto L_{eff} = L_g - \Delta L \tag{2.15}$$

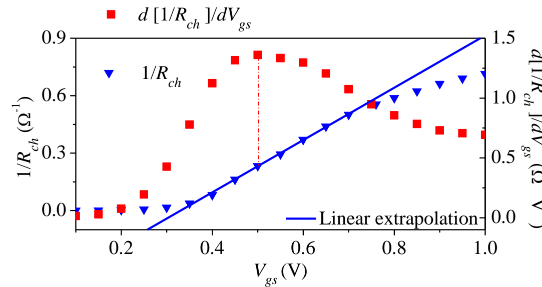

Figure 2.7. *Linear extrapolation of 1/R_{DC} and 1/R_{ch} against V_{gs} at its maximum slope point with L_g = 80 nm.*

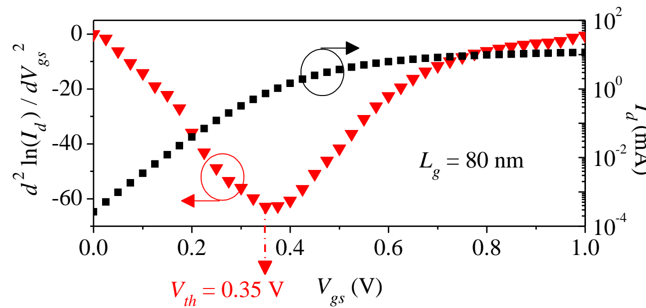

Figure 2.8. *Extraction of V_{th} through the SDL method.*

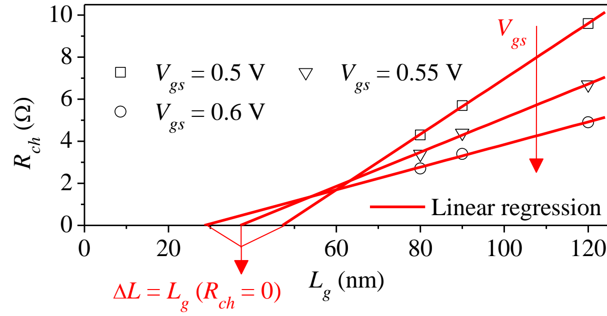

Figure 2.9. *Linear regressions to obtain ΔL at different V_{gs} voltages using R_{ch} obtained from RF measurements at V_{ds} = 0 V.*

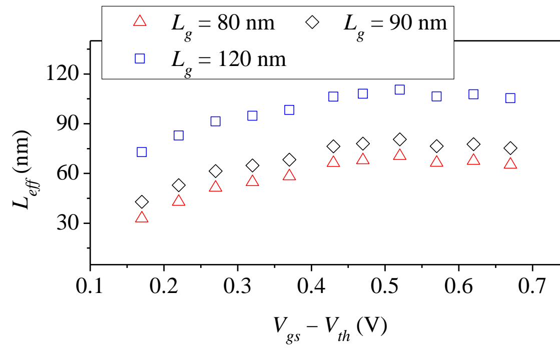

Figure 2.10. *L_{eff} versus V_{gs} curves showing the noticeable difference for devices presenting different L_g.*

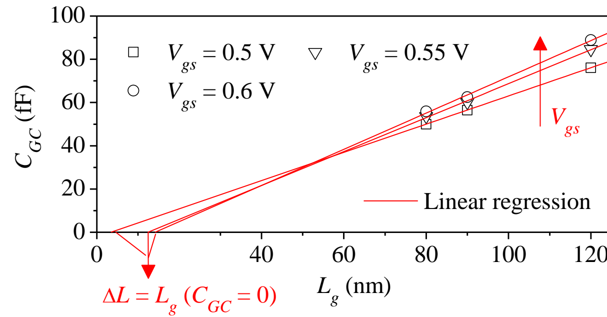

Figure 2.11. *Linear regressions to obtain ΔL at different V_{gs} voltages using C_{GC} obtained from RF measurements at V_{ds} = 0 V.*

As one can deduct from (2.15), L_g is decreased down to ΔL when R_{ch} varies from a given value to zero wherein L_{eff} can be found. This requires that the points of R_{ch} as a function of L_g at a fixed V_{gs} fall on a line with the aim of doing the corresponding linear regression and extrapolation of data, which is achieved in

Figure 2.9 for three different values of V_{gs}. Following this procedure, L_{eff} can be estimated for different voltages in strong inversion. In Figure 2.10, the results for MOSFETs with different gate mask length are presented. Notice that the observed difference between the curves for L_{eff} in Figure 2.10 highlights the necessity of taking into consideration changes in the parameters of transistors when there is a variation of the intrinsic geometry. Due to the inversion of the channel under the gate terminal, some part of the LDD regions is also inverted and then, L_{eff} comes close to L_g when V_{gs} is greater than V_{th}. Given that the doping profile does not significantly vary with the gate lengths, all devices have the same curve trend.

For comparison purposes, the RF capacitance method to determine L_{eff} is as well implemented by following the procedure presented in [**39**]. First of all, the gate-to-channel capacitance (C_{GC}) associated with L_g is defined as

$$C_{GC}(V_{gs}) = C_G(V_{gs}) - C_G(V_{gs} = 0) \propto L_g - \Delta L, \tag{2.16}$$

whit

$$C_G(V_{gs}) = \mathrm{Im}(Y_{11}) / \omega. \tag{2.17}$$

After calculating C_{GC} through (2.16), it is plotted as a function of L_g for different V_{gs}, which is presented in Figure 2.11 that also shows the linear regression of data. Consecutively, in the same way like R_{ch}, ΔL must be determined from the extrapolation to the point where C_{GC} is equal to zero. Furthermore, in Figure 2.12, all results obtained by both the proposal and the RF capacitance technique are compared one to each other, showing similar trends when $V_{gs} - V_{th}$ is over 0.4 V in which the channel region is fully inverted. It is essential to point out that C_{GC} depends not only on intrinsic but also on extrinsic characteristics, which results in an inaccurate extraction of it at lower voltages.

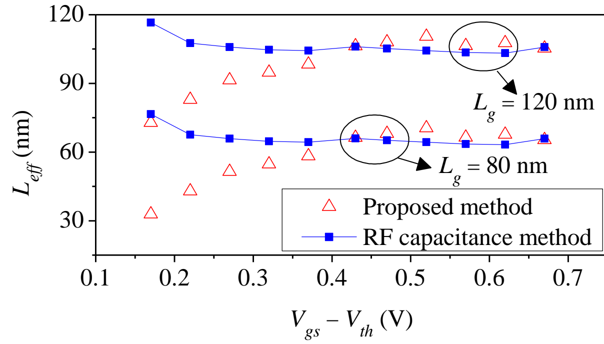

Figure 2.12. *Comparison of L_{eff} versus V_{gs} obtained from proposed method and RF capacitance method.*

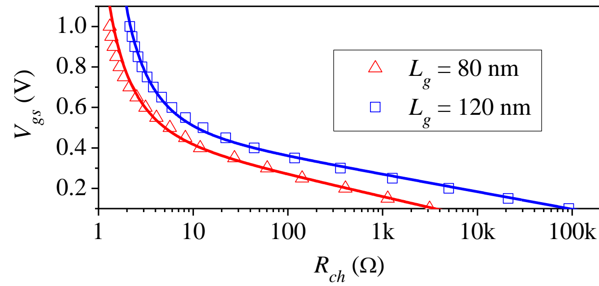

Figure 2.13. *Correlation of equation (2.19) with experimental data for different L_g.*

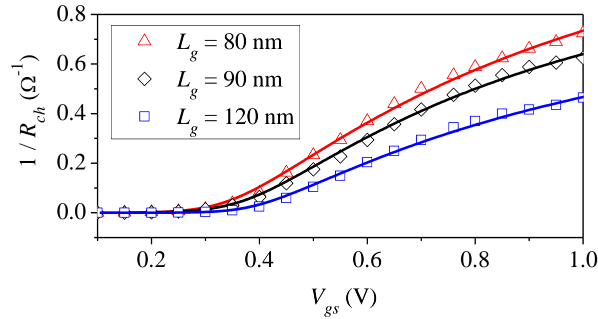

Figure 2.14. Inverse of extracted (symbols) and simulated (continuous lines) R_{ch} as a function of V_{gs} for different L_g.

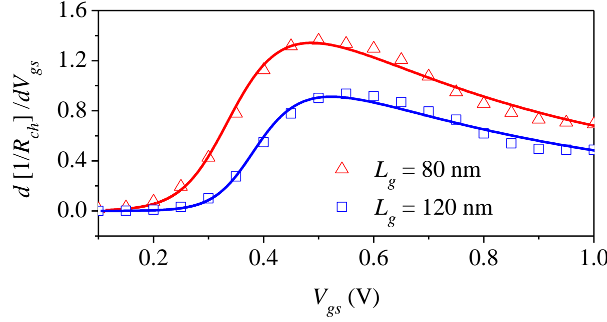

Figure 2.15. Derivative of the inverse of extracted (symbols) and simulated (continuous lines) R_{ch} against V_{th} for different L_g.

2.1.4 Validation of the Proposed Methodology

For the sake of giving a validation of the proposal, an expression to reproduce the MOSFET's I-V characteristic from R_{ch} obtained by high frequency measurements is required. According to this, the following semi-empirical equation can be employed [**38**]:

$$I_{ch} = \frac{I_0}{1+\theta V_{gs}} \mathrm{W}_0\left[K\left(1+\theta V_{gs}\right)\right]\exp\left(\frac{V_{gs}}{N}\right), \tag{2.18}$$

where W_0 is the main branch of the Lambert W function, K and I_0 are fitting parameters, θ is the mobility degradation coefficient and N is equal to the ideality factor (n) times the thermal voltage (V_t). It is necessary to mention that the equation (2.18) is valid for both subthreshold and strong inversion biasing conditions. As R_{ch} is associated with I_{ch}, R_{ch} can be determined by means of (2.18) as follows

$$\frac{1}{R_{ch}} = \frac{I_{ch}}{V_{ch}} = \frac{1}{R_0\left(1+\theta V_{gs}\right)} \mathrm{W}_0\left[K\left(1+\theta V_{gs}\right)\right]\exp\left(\frac{V_{gs}}{N}\right), \tag{2.19}$$

where $R_0 = V_{ch} / I_0$. Given that the previous equation involves the Lambert W function that cannot be expressed in terms of elementary functions, it is more suitable to express V_{gs} versus R_{ch} to simplify (2.19). Based on this procedure, R_{ch} is obtained as follows

$$V_{gs} = \frac{NR_0 - NR_{ch}\ln\left[KR_{ch}/R_0\right]}{R_{ch} - NR_0\theta}. \tag{2.20}$$

This allows one to represent the values of R_{ch} when V_{gs} varies from subthreshold to strong inversion. After using (2.20), a consistent fitting of the

experimentally obtained data $R_{ch}(V_{gs})$ is achieved as shown in Figure 2.13 for different L_g. As the equation (2.20) has a non-linear behavior, the Levenberg-Marquardt algorithm was employed to find the resulting parameters by least squares optimization. Moreover, their corresponding values are listed in Table 2.1. With the aim of extracting information from the results of the model, it is better to show the curves of the inverse of R_{ch} and its derivative obtained from the explicit expression (2.19), which are respectively presented in Figure 2.14 and Figure 2.15.

In the case of the series parasitic resistances, they can be defined in terms of the bias condition as follows [**40**], [**41**]

$$R_d = R_{d_const} + R_{d_bias} = R_{d_const} + \frac{\upsilon_d}{V_{gs} - V_{th}}, \tag{2.21}$$

$$R_s = R_{s_const} + R_{s_bias} = R_{s_const} + \frac{\upsilon_s}{V_{gs} - V_{th}}, \tag{2.22}$$

where R_{d_const} and R_{s_const} are the bias-independent components, R_{d_bias} and R_{s_bias} are the bias-dependent components, and υ_d and υ_s are fitting parameters. After performing the linear regressions of R_{d_bias} and R_{s_bias}, it is found that υ_d is 2.2×10^{-1} ΩV and υ_s is 1.7×10^{-1} ΩV for L_g = 80 nm, which is illustrated in Figure 2.16. On condition that the uncertainty of the fabrication process can impact the LDD regions, υ_d will not be necessarily equal to υ_s. This issue is also due to the design of the RF MOSFET that is divided into several fingers wherein drain and source have different areas.

TABLE 2.1

Parameters used for implementing the V_{gs}–R_{ch} model given by (2.20).

Parameter	L_g = 80 nm	L_g = 90 nm	L_g = 120 nm
θ (V^{-1})	7.2	7.2	8.2
N (V)	4.4×10^{-2}	4.6×10^{-2}	3.6×10^{-2}
R_0 (Ω)	2.1	2.2	3.4
K	5×10^{-5}	5×10^{-5}	2.4×10^{-6}

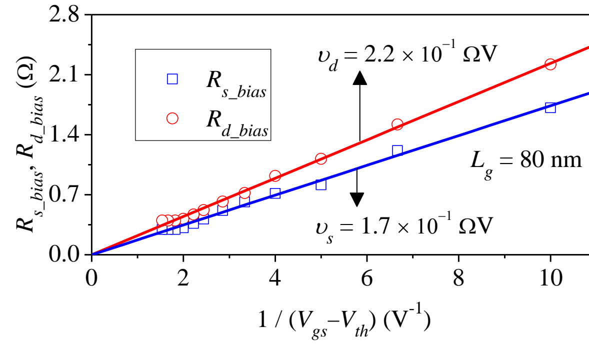

Figure 2.16. *Linear regressions (continuous lines) of R_{s_bias} and R_{d_bias} as a function of $1/(V_{gs}-V_{th})$. These regressions are used to analytically obtain the parameters in (2.21) and (2.22).*

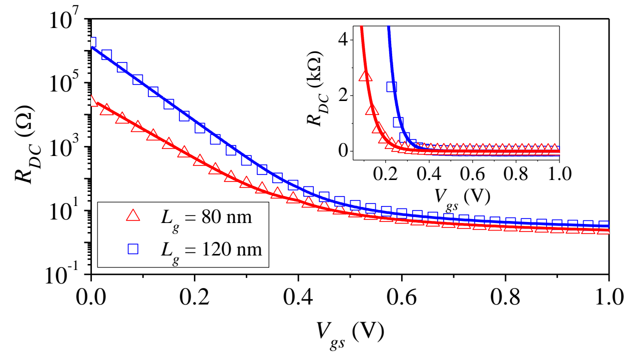

Figure 2.17. *Measured (symbols) and simulated (continuous lines) R_{DC} as a function of V_{gs} for different L_g.*

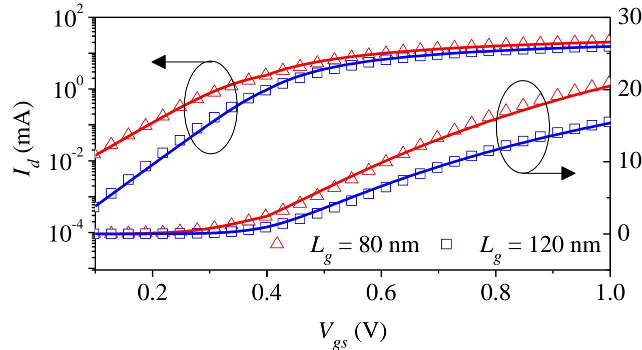

Figure 2.18. *Measured (symbols) and simulated (continuous lines) I_d as a function of V_{gs} for different L_g at V_{ds} = 50 mV.*

Thus, R_{DC} is given by

$$R_{DC} = \frac{V_{ds}}{I_d} = R_{ch} + R_s + R_d + R_{pad}, \tag{2.23}$$

After replacing (2.20) through (2.22) in (2.23), the following expression is obtained as

$$R_{DC} = \frac{V_{ds}}{I_d} = B + \frac{R_0\left(1+\theta V_{gs}\right)}{\mathrm{W}_0\left[K\left(1+\theta V_{gs}\right)\right]\exp\left(\frac{V_{gs}}{N}\right)} + \frac{\upsilon_s}{V_{gs}-V_{th}} + \frac{\upsilon_s}{V_{gs}-V_{th}}, \tag{2.24}$$

with $B = R_{d_const} + R_{s_const} + R_{pad}$. It is important to notice that equation (2.24) can be only used when V_{gs} is greater than V_{th}. Nevertheless, in order to estimate the value of R_{ch} for $V_{gs} \leq V_{th}$, the assumption that R_{ch} is higher than $R_d + R_s$ is considered since the channel is no formed, and thus, R_{DC} is approximately equal to $R_{ch} + R_{pad}$. The measured and simulated values of R_{DC} are presented in Figure 2.17.

Once R_{DC} is extracted by using (2.24), I_d can be determined through RF data for a given V_{ds} in which the transistor is operating in the linear region. The comparison between experimental and simulated data for I_d achieves a good agreement, which is illustrated in Figure 2.18. Based on this, it is confirmed that DC and RF measurements can be correlated by means of semi-empirical equations, bearing in mind the bias-dependent component of R_s and R_d. Thus, the characterization of bulk MOSFETs with LDD regions can be done while maintaining the consistency between DC and RF data.

2.2 CHARACTERIZATION OF THE EXTRINSIC GEOMETRY OF THE TRANSISTOR

With the purpose of enhancing the capacity to handle the flow of current through the inversion channel, the total gate width is increased for a given gate length, but this negatively impacts the value of Rg. To reduce this undesirable effect, the transistor is divided in multiples fingers in which all fingers have the same width and length. Furthermore, if a very wide transistor is required, several cells corresponding to a multi-finger transistor can be vertically connected in parallel to efficiently use the design area while allowing the use of scalable models. This is suitable because the parasitic resistance associated with the interconnection between single cells in which the cross-sectional area is much larger than L_g and W_{total} does not considerably increase R_s and R_d [**42**], [**43**]. In

addition, a significant reduction of the value of the gate resistance (Rg) is achieved. This is an important issue because Rg considerably affects the noise figure and the maximum frequency of oscillation. Even though much research related to Rg has been dedicated to characterize and represent this parameter for modeling purposes, it has been also focused on the development of new improved devices. As a result of this, Rg has been determined as a function of the geometry, obtaining models that consider multi-cell and double-sided gate electrodes. It is well known that the variation of the transistor in geometry does not only affect Rg but also the rest of the extrinsic elements involved with the performance of the transistor. For this reason, the study of Rb that varies with the number of cells (N_c) even when W_{total} is fixed has been carried out in the literature. However, since the geometry dependence of other extrinsic parameters such as Rs, Rd, Cjs and Cjd is also becoming important for advanced devices, scalable models for these parameters still need to be developed.

As a result of this, W_{total} is equal to 192 μm for a specific gate length (Lg). Even when the series parasitic resistances are often represented through effective elements, it is well known that they have a distributed behavior. To clarify this concept, a resistance network in the case of the MOSFET's source terminal for 4 cells and 3 vias per finger is shown in Figure 2.19, where R_{cell_s} and R_{cell_d} are the cell resistances, R_{met_s} and R_{met2_s} are the metal resistances, R_{cont_s} is the contact resistance and R_{series_s} includes the effect of the resistances associated with the highly doped drain (R_{HDD_s}) and lightly doped drain (R_{LDD}) regions. This scheme can be also used for the resistance network of the drain terminal, changing the subscript _s for _d.

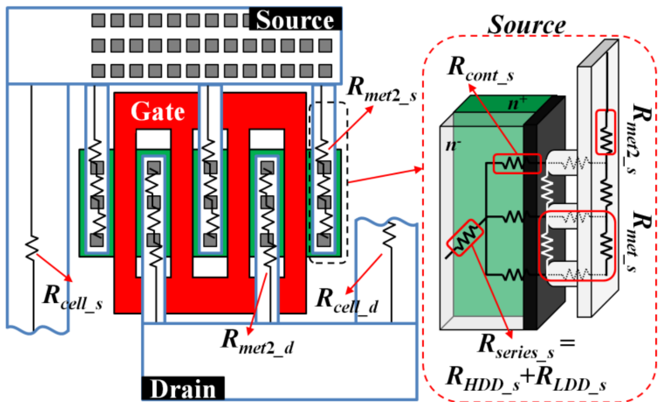

Figure 2.19. *Layout for a four-finger cell MOSFET showing a distributed model for the source resistance.*

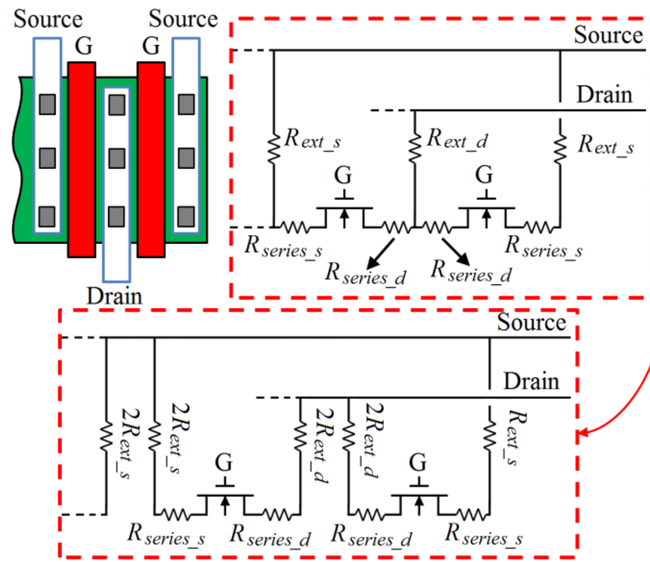

Figure 2.20. *Equivalent circuit for the microwave MOSFET, considering the device symmetry of the two fingers of the right end of the Figure 2.19.*

In order to represent the undesirable effect of the parasitcs of a multi-fingered MOSFET, its equivalent circuit can be seen as a set of transistors that are associated with each finger. Consequently, these devices can be connected by means of a resistance network as shown in Figure 2.20 to completely characterize the MOSFET. This does not only include the effect of R_{series_s} and R_{series_d} but also the series external resistances (R_{ext_s} and R_{ext_d}) that takes into account the parasitic component of the interconnection of adjacent single devices. Thus, in the case of the drain terminal, the total resistance R_{ext_d} based on the circuit formed by R_{met_s}, R_{met2_s} and R_{cont_s} allows us to facilitate the drawing and the easy understanding of the circuit of the device. Due to the symmetry of the fingers, R_{ext_s} or R_{ext_d} in which source or drain are shared between single transistors can be divided into two resistances with the goal of putting in parallel the corresponding equivalent circuit of each finger, as shown in Figure 2.20. Since source and drain regions are shared between adjacent unit transistors in the case of multi-finger MOSFETs, their total number of vias and total source/drain area become smaller than that for single-finger MOSFETs. In this way, the use of multi-finger layout gives place to the decreasing of R_{ext_s} or R_{ext_d}, which is an important issue for nanometer-scale devices due to the reduced channel resistance (R_{ch}).

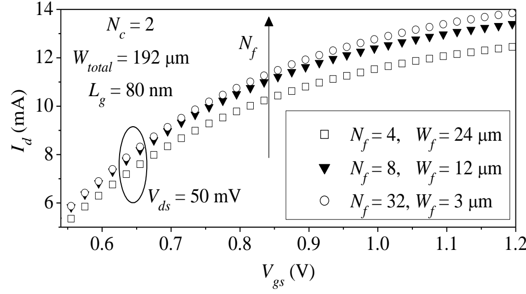

Figure 2.21. *I_d as a function of V_{gs} for different N_f with a fixed total gate area.*

Even though all structures have the same W_{total} and L_g in Figure 2.21, drain current (I_d) increases when N_f varies from 4 to 32, which becomes more significant at higher gate-source voltages (V_{gs}). This behavior is based on the variation of the resistance associated with extrinsic geometry that is comparable to R_{ch} when channel is completely inverted. Notice that the separations and dimensions of vias do not change, maintaining constant R_{met}, $R_{met\ 2}$ and R_{cont}. In order to take into account the trend of I_d with N_f for a fixed W_{total}, a scalable model that considers the effect of extrinsic geometry needs to be performed, which should not be only focused on R_g, but also on R_s and R_d. It is important to mention that the bias-dependent component, due to the LDD regions, does not significantly vary and thus, R_s and R_d are essentially modified by the bias-independent component. Indeed, the changing of the bias-dependent component is generated by the difference between fabrication processes. Once N_f reaches a given value, the I-V characteristics of the multi-finger devices are almost the same each other because of the small change of the total number of vias and the total source/drain area.

With the purpose of representing an RF MOSFET layout, the parallel combination of the equivalent circuits of each finger can be used, as indicated before. Note that all vias in source regions are shared between adjacent single transistors with the exception of the extreme ones, which correspond to N_f – 2 fingers per cell. This condition should be taken into account to obtain a correct expression of the total resistance (R_{total}), which can be written for one cell as follows:

$$R_{total_cell} = \frac{R_1 + 2R_{ext_s}}{N_f - 2} \Bigg\| \frac{R_1 + R_{ext_s}}{2}, \tag{2.25}$$

with $R_1 = R_{series_s} + R_{series_d} + R_{ch} + 2R_{ext_d}$. Furthermore, R_{total} for a microwave MOSFET with two cells is given by:

$$R_{total} = \left[\frac{R_1 + 2R_{ext_s}}{N_f - 2} \middle\| \frac{R_1 + R_{ext_s}}{2} \right] \Bigg\| \left[\left(\frac{R_1 + 2R_{ext_s}}{N_f - 2} \middle\| \frac{R_1 + R_{ext_s}}{2} \right) + R_{cell_s} + R_{cell_d} \right]. \tag{2.26}$$

In view of the fact that the dimensions of the connections between cells are three orders of magnitude greater than the source/drain diffusion region and gate lengths, R_{cell_s} and R_{cell_d} can be neglected. Following this assumption, (2.26) can be rewritten for several cells with the purpose of finding a general expression of R_{total} as follows:

$$\begin{aligned} R_{total} &\approx \frac{R_1 + 2R_{ext_s}}{N_c(N_f - 2)} \Bigg\| \frac{R_1 + R_{ext_s}}{N_c(2)} \\ &\approx \frac{(R_1 + R_{ext_s})(R_1 + 2R_{ext_s})}{N_c\left(2R_{ext_s} + N_f(R_1 + R_{ext_s})\right)}. \end{aligned} \tag{2.27}$$

Notice that $2R_{ext_s}$ is smaller than $N_f\ (R_1 + R_{ext_s})$ because $N_f\ (R_1 + R_{ext_s})$ is of the order of tens of ohms whereas $2R_{ext_s}$ is of the order of fractions of ohms. In this fashion, (2.27) can be simplified as:

$$R_{total} \approx \frac{R_1}{N_f N_c} + \frac{2R_{ext_s}}{N_f N_c}, \tag{2.28}$$

where

$$R_{ext_s} = (A/B) + R_{met2_s} \tag{2.29}$$

Equation (2.29) is obtained by using Figure 2.22. The parameters A and B for the case of the source region are given by:

$$\frac{A}{R_{cont_s}} = R_{cont_s}{}^{N_v - 1} + \sum_{i=1}^{(N_v - 1)} \left[\frac{R_{cont_s}{}^{(N_v - 1) - i} R_{met_s}{}^{i}}{(2i)!} \prod_{j=-i}^{i-1} (N_v + j) \right] \tag{2.30}$$

And

$$B = \sum_{k=1}^{N_v} \left[\frac{R_{cont_s}{}^{N_v - k} R_{met_s}{}^{k-1}}{(2k-1)!} \prod_{l=-k+1}^{k-1} (N_v + l) \right]. \tag{2.31}$$

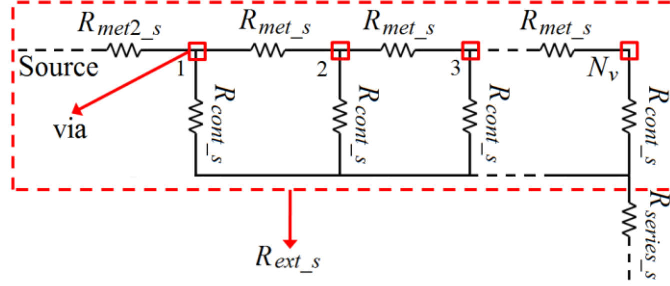

Figure 2.22. *Corresponding circuit for the source external resistance.*

In order to get practical equations for A and B with the aim of fitting the experimental data, these can be simplified under the fact that R_{met_s} is much smaller than R_{cont_s} related to the resistance of the metal-to-semiconductor interface. In this way, the term R_{met_s} can be neglected when its exponent is greater than 2, which allows obtaining the following:

$$\begin{aligned} \frac{A}{R_{cont_s}} \approx R_{cont_s}{}^{N_v - 1} + \frac{R_{cont_s}{}^{N_v - 2} R_{met_s}}{2} (N_v - 1) N_v \\ + \frac{R_{cont_s}{}^{N_v - 3} R_{met_s}{}^{2}}{24} (N_v - 2)(N_v - 1) N_v (N_v + 1) \end{aligned} \tag{2.32}$$

and

$$\begin{aligned} B \approx R_{cont_s}{}^{N_v - 1} N_v + \frac{R_{cont_s}{}^{N_v - 2} R_{met_s}}{6} (N_v - 1) N_v (N_v + 1) \\ + \frac{R_{cont_s}{}^{N_v - 3} R_{met_s}{}^{2}}{120} (N_v - 2)(N_v - 1) N_v (N_v + 1)(N_v + 2), \end{aligned} \tag{2.33}$$

where $N_v = (\beta W_{total}) / (N_f N_c)$, β is the number of vias per unit length, which is a constant, and $N_v \geq 3$. In this work, β is equal to 2 vias per 1 µm. In this way, R_s and R_d resistances can be determined by:

$$R_s(V_{gs}, N_f) = \frac{R_{LDD_s}}{N_f N_c} + \frac{R_{HDD_s}}{N_f N_c} + \frac{2R_{ext_s}}{N_f N_c}, \tag{2.34}$$

$$R_d\left(V_{gs},N_f\right)=\frac{R_{LDD_d}}{N_f N_c}+\frac{R_{HDD_d}}{N_f N_c}+\frac{2R_{ext_d}}{N_f N_c}. \tag{2.35}$$

Since W_{total} = N_f N_c W_f remains constant for the considered devices, W_f decreases and N_f increases at the same rate. Subsequently, R_{LDD} and R_{HDD} are inversely proportional to W_f. Following these trends, $R_{LDD}/(N_f N_c)$ and $R_{HDD}/(N_f N_c)$ becomes independent of N_f. It is important to remark that the only bias-dependent component is introduced into R_{LDD}, which is due to the part of the LDD region under the gate [**40**]. In this way, the behavior of the series parasitic resistances, R_s and R_d, in microwave MOSFETs can be accurately modeled as follows:

$$R_s\left(V_{gs},N_f\right)=\frac{\upsilon_{_s}}{\left(V_{gs}-V_{th}\right)}+R_{ind_s}+\frac{2R_{ext_s}}{N_f N_c}, \tag{2.36}$$

$$R_d\left(V_{gs},N_f\right)=\frac{\upsilon_{_d}}{\left(V_{gs}-V_{th}\right)}+R_{ind_d}+\frac{2R_{ext_d}}{N_f N_c}, \tag{2.37}$$

where υ is a fitting parameter associated with the bias-dependent resistance; V_{gs} is the gate-to-source voltage; V_{th} is the threshold voltage; R_{ind} is the bias-independent resistance that is due to the HDD region and the part of the LDD region which is not under the gate; and the subscripts *_s* and *_d* denote the source and drain regions, respectively.

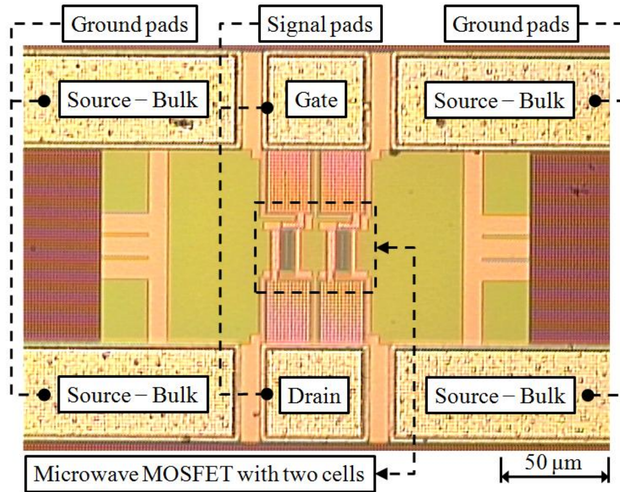

Figure 2.23. *Micrograph of one of the considered transistors.*

2.2.1 Description of the Device under Test

Microwave MOSFETs with different N_f that varies from 4 to 32 were measured up to 60 GHz. These are configured in common bulk-source and thus, source and bulk terminals are tied and connected to ground, as shown in Figure 2.23. Notice that the total gate width ($W_{total} = W_f N_f$) and gate length (L_g) are fixed for all devices at 192 μm and 80 nm, respectively. In order to reduce leakage currents and hot carrier effects, shallow trench isolation (STI) and LDD regions in both source and drain sides are considered for the fabrication process of DUT.

2.2.2 Analysis of the dependence of the extrinsic parameters with the number of fingers

In view of the fact that the flow of current through the substrate becomes significant at higher frequencies, the corresponding parasitics associated with this should be subtracted from the experimental data to properly determine R_s and R_d, as mentioned in chapter 1. In order to do this, the RF-MOSFET is biased at $V_{gs} = 0$ V and $V_{ds} = 0$ V and the proposal given by [**10**] is performed. Subsequently, the voltages of the transistor are fixed in such a way that V_{gs} is greater than V_{th} (i.e., 0.38 V for the considered devices). At this bias condition, R_s and R_d are in the same order of magnitude of R_{ch} because the inversion channel is fully formed under the gate. After processing the RF Measurements, it is found that R_s and R_d decrease when V_{gs} and N_f increase, which is presented in Figure 2.24 and Figure 2.25. These trends are based on the changes of number of vias and of carrier concentration in the LDD regions when the MOSFET is folded into several individual transistors connected one to each other in parallel and the concentration of the inversion channel is higher than that of the LDD regions, respectively. Furthermore, it can be deduced that I_d increases with N_f for fixed values of W_{total} and L_g, since I_d is inversely proportional to the series parasitic resistances. The importance of considering the variation of R_s and R_d with the extrinsic geometry into the small-signal equivalent circuit is mandatory. The analysis of the parasitic components involved in R_s and R_d is carry out for different values of N_f and V_{gs} at $V_{ds} = 0$ V, which is necessary to correctly characterize the devices.

In Figure 2.24 and Figure 2.25, a non-linear fitting of the extracted R_s and R_d based on Levenberg-Marquardt algorithm is performed and thus, the unknown

variables of (2.36) and (2.37) can be found. These are presented for the source as follows; R_{cont_s} = 69.4 Ω, R_{met_s} = 0.1 Ω, $R_{met\ 2_s}$ = 0.05 Ω, R_{ind_s} 0.08 Ω and $\upsilon_{_s}$ = 0.3 ΩV. Furthermore, the variables for the drain are R_{cont_d} = 67.1 Ω, R_{met_d} = 0.06 Ω, $R_{met\ 2_d}$ = 0.05 Ω, R_{ind_d} 0.08 Ω and $\upsilon_{_d}$ = 0.3 ΩV. Notice that the corresponding values of R_{cont} and R_{met} allow us to confirm the assumptions in (2.32) and (2.33), which states that R_{met} is much smaller than R_{cont} for both source and drain sides.

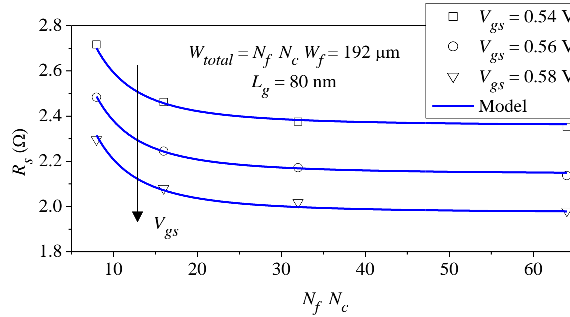

Figure 2.24. *Fit of the source resistance against total number of fingers with different V_{gs} at V_{ds} = 0 V.*

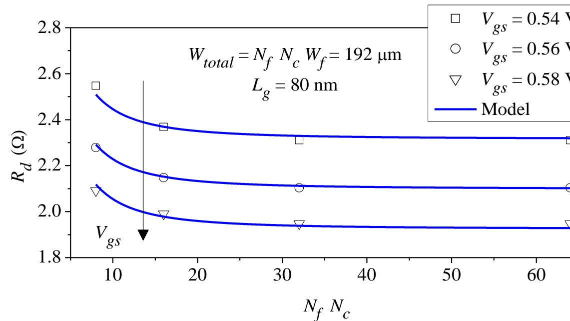

Figure 2.25. *Fit of the drain resistance against total number of fingers with different V_{gs} at V_{ds} = 0 V.*

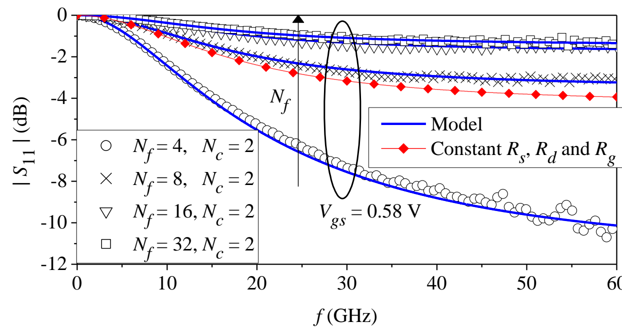

Figure 2.26. *Simulated and experimental S_{11} of microwave MOSFETs for different number of fingers at V_{gs} = 0.58 V and V_{ds} = 0 V. The dashed curve corresponds to the simulation of the MOSFET with the obtained average values of R_s, R_d and R_g.*

In order to evaluate the effect of R_s, R_d and R_g that are extrinsic geometry dependent, the experimental S-parameter data of the input (S_{11}) and output (S_{22}) ports, collected by the VNA, are monitored. As a consequence of the reduction of R_{ch} when L_g is scaled down to tens of nanometers, R_s and R_d significantly impact S_{22} whereas R_g affects the magnitude of S_{11}. The results of all considered devices are presented in Figure 2.26 through Figure 2.28. For this, the applied voltages, V_{gs} = 0.58 V and V_{ds} = 0 V, to the MOSFET ensure its operation in strong inversion because the condition of $V_{gs} > V_{th}$ is accomplished. The comparison between the proposal and the assumption of constant R_s, R_d and R_g is also carried out. In this way, if each one of the series parasitic resistances is fixed in a given value, the simulation will not match the experimental data. This shows the importance of considering the variation of the series parasitic resistances with the extrinsic geometry at high frequency. It is remarkable to note that S_{11} and S_{22} do not vary for devices with a large number of fingers. On the other hand, the devices are biased in strong inversion at V_{ds} > 0 V to take into consideration the active region. In Figure 2.29, S_{11} and S_{22} are presented up to 60 GHz at V_{gs} = 0.50 V and V_{ds} = 0.7 V.

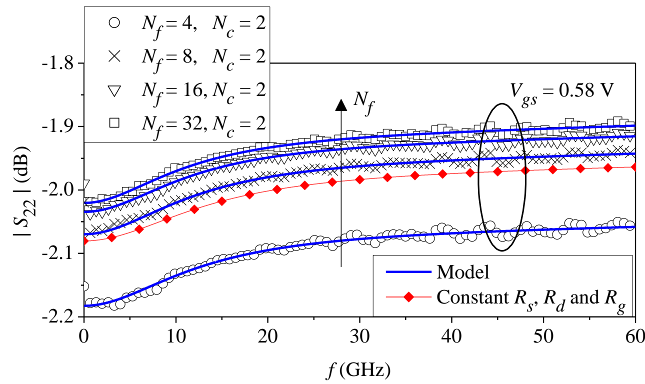

***Figure 2.27**. Simulated and experimental S_{22} of microwave MOSFETs for different number of fingers at V_{gs} = 0.58 V and V_{ds} = 0 V. The dashed curve corresponds to the simulation of the MOSFET with the obtained average values of R_s, R_d and R_g.*

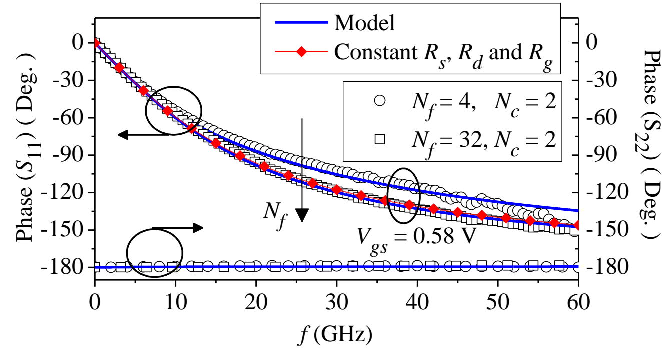

Figure 2.28. *Simulated and experimental phase of microwave MOSFETs for different number of fingers at V_{gs} = 0.58 V and V_{ds} = 0 V. The dashed curve corresponds to the simulation of the MOSFET with the obtained average values of R_s, R_d and R_g.*

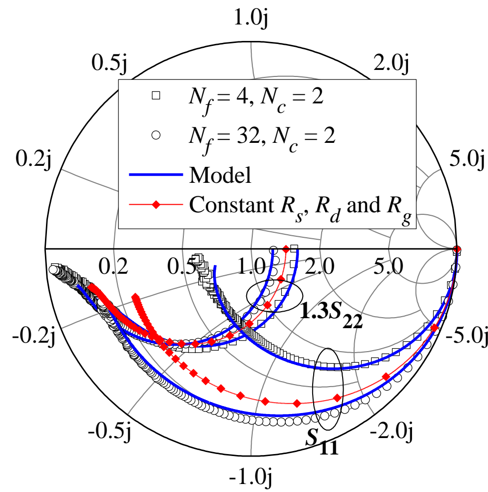

Figure 2.29. Simulated and experimental S_{11} and 1.3S_{22} of microwave MOSFETs for different number of fingers at V_{gs} = 0.50 V and V_{ds} = 0.7 V. The dashed curve corresponds to the simulation of the MOSFET with the obtained average values of R_s, R_d and R_g.

3 CHARACTERIZATION OF RF MOSFETS CONSIDERED AS A FOUR-TERMINAL DEVICE

In order to accurately represent the RF-MOSFET's features required by IC-design-oriented simulations, it is mandatory to consider the characterization of the transistor as a four-terminal device. For this purpose, the pads should be configured with three- or four-ports to determine the corresponding small-signal S-parameters. However, the necessary measurement equipment is still not available in many microwave laboratories and then, much recent research has been focused on the analysis of the MOSFET's characteristics as a two-port device in a common source/bulk configuration [**44**], [**45**]. Even though this restriction does not allow us to directly determine the bulk bias dependence of the model parameters, some alternatives have been developed. For instance, S-parameter measurements obtained from a two-port vector network analyzer (VNA) can be used for multiport characterization by either considering a set of devices in different configurations [**46**], or performing multiple combinations of measurements on a single device [**47**]. In the case of the first previously mentioned methodology, it requires additional space in die for the extra structures. Furthermore, in the second proposal, the accuracy of the renormalization algorithms related to these approaches is strongly dependent on the knowledge of the loads used to terminate the remaining ports, which are frequency dependent and difficult to determine. These disadvantages can be efficiently overcome through a separate bulk DC bias pad to characterize the bulk-bias dependent effects in RF-MOSFETs using a two-port VNA.

3.1 DETERMINATION OF MOSFET PARAMETERS IN LINEAR REGIME

A set of multi-finger RF MOSFETs in a common-source configuration with channel length of 80 nm, width of 3 µm and 64 fingers was fabricated on a silicon wafer. For this purpose, the substrate and source terminals are not tied. Indeed, an extra DC terminal to bias the substrate with respect to the source was considered

for the design of the transistors, which is illustrated in Figure 3.1. First of all, the DUT is biased at V_{ds} = V_{gs} = 0 V with the aim of neglecting the effect associated with the transconductance and then, the number of variables is reduced. In order to clarify how the voltages are applied to the DUT, a schematic of the pads for a given transistor is presented. The equations related to the small-signal Y parameters of the MOSFET for the previously mentioned bias condition is shown as follows [**48**], [**49**]:

$$Y_{11} \approx \omega^2 R_g \left(2C_{gd0} + C_{gb}\right)^2 + j\omega\left(2C_{gd0} + C_{gb}\right) \tag{3.1}$$

$$Y_{12} \approx -j\omega C_{gd0} \tag{3.2}$$

$$Y_{22} \approx \omega^2 R_b C_{jd}{}^2 + j\omega\left(C_{jd} + C_{gd0}\right) \tag{3.3}$$

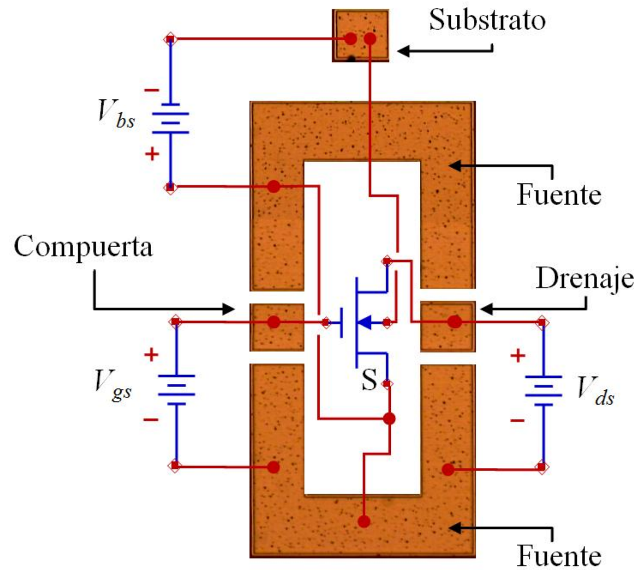

Figura 3.1. *Schematic of the applied voltages to the MOSFET.*

Using the equations (3.1) through (3.3), a linear regression of the experimental data can be done up to 4 GHz. This frequency limit guarantees that Cjs which is in parallel with Rb do not significantly affect the behavior of the device and the consequent extraction methodology. Then, the elements of the small-signal model, and in particular the substrate parasitics, are obtained, as shown in Figure 3.2. It is important to remark that the current do not only flow through the channel but also through the substrate, which is more notable when frequency increases. On the other hand, Cjs can be found by means of the subtraction of the elements of the

equivalent circuit from the admittance Y22 in frequencies greater than 6 GHz based on equation (3.4), which are presented in Figure 3.3.

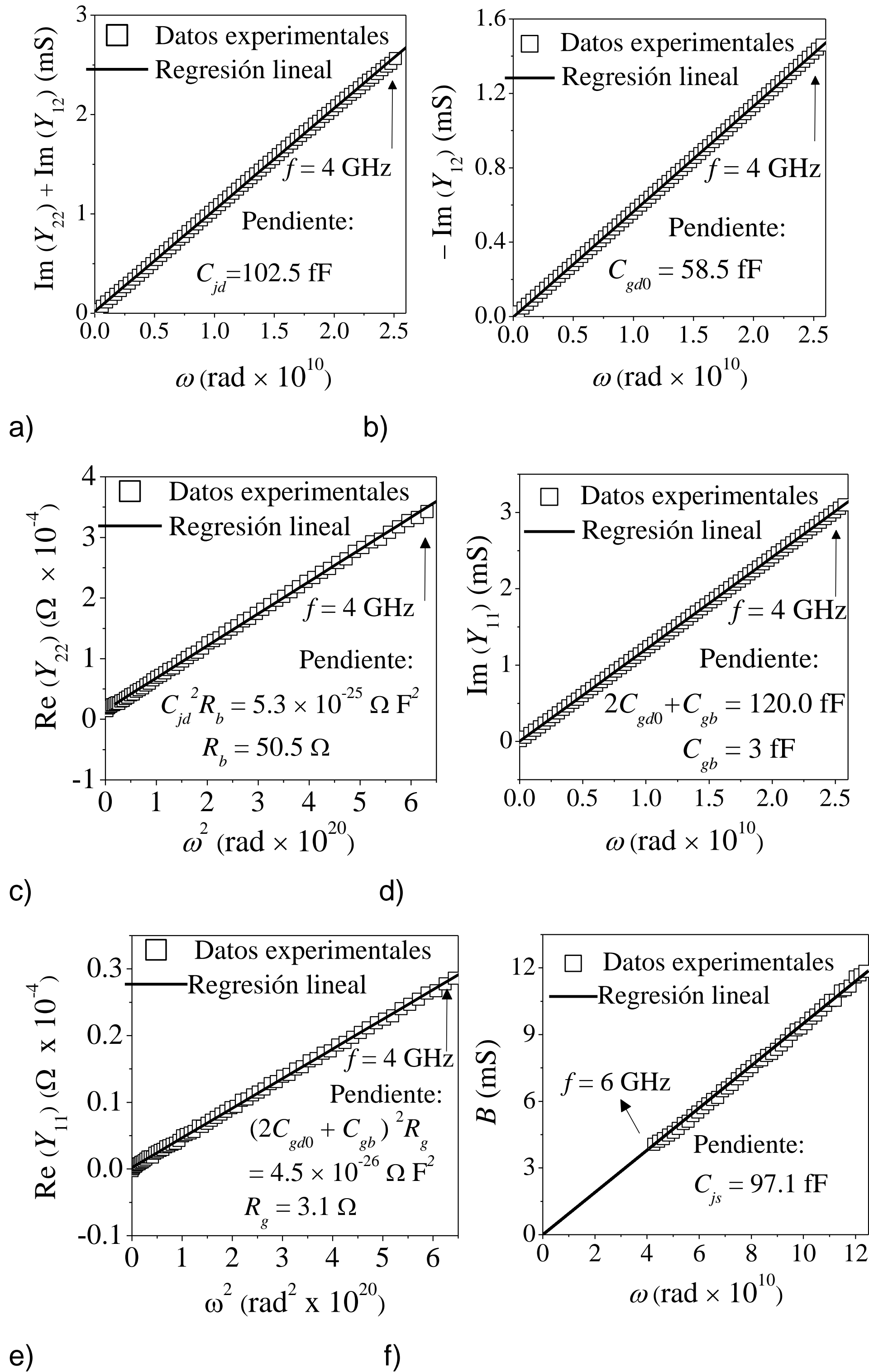

Figure 3.2. *Linear regressions to determine the elements of the small-signal model, C_{jd}, C_{gd0}, R_b, C_{gb}, R_g and C_{js} at $V_{gs} = V_{bs} = V_{ds} = 0$ V.*

$$B = \mathrm{Im}\left[\left(\left(\left(Y_{22}^{-1} + Z_2\right)^{-1} - \left(Z_1 + Z_4\right)^{-1}\right)^{-1} - Z_3\right)^{-1}\right] = \omega C_{js} \quad (3.4)$$

where the impedances Z_1 through Z_4 are defined as a function of the elements of the equivalent circuit for Y_{22}, which is illustrated in figure 10.

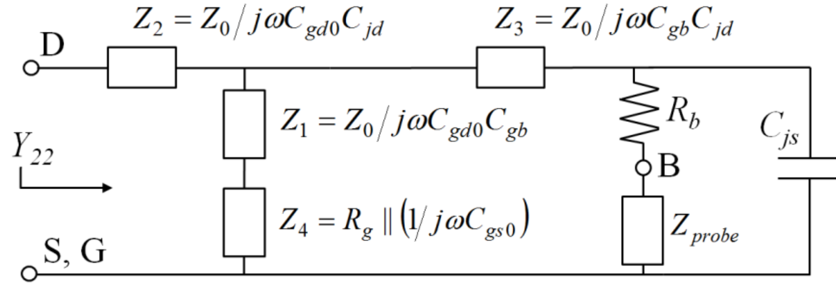

Figure 3.3. *Equivalent circuit for the admittance Y_{22}.*

Once the analysis of the MOSFET in off state regime has been done, the following step consists of biasing the device in strong inversion in which the constraint of $V_{gs} > V_{th}$ should be ensured. In order to do this, it is used the procedure described in [**40**], considering a range of voltage between 0.55 V and 0.65 V. In this way, important parameters such as the parasitic series parasitic resistances R_s, R_d and the channel resistance R_{ch} can be determined. As it is well known, R_{ch} is related to the threshold voltage V_{th}. Indeed, V_{th} can be determined by means of the linear regression of the inverse of R_{ch} as a function of V_{gs} for a given V_{bs} at $V_{ds} = 0$ V.

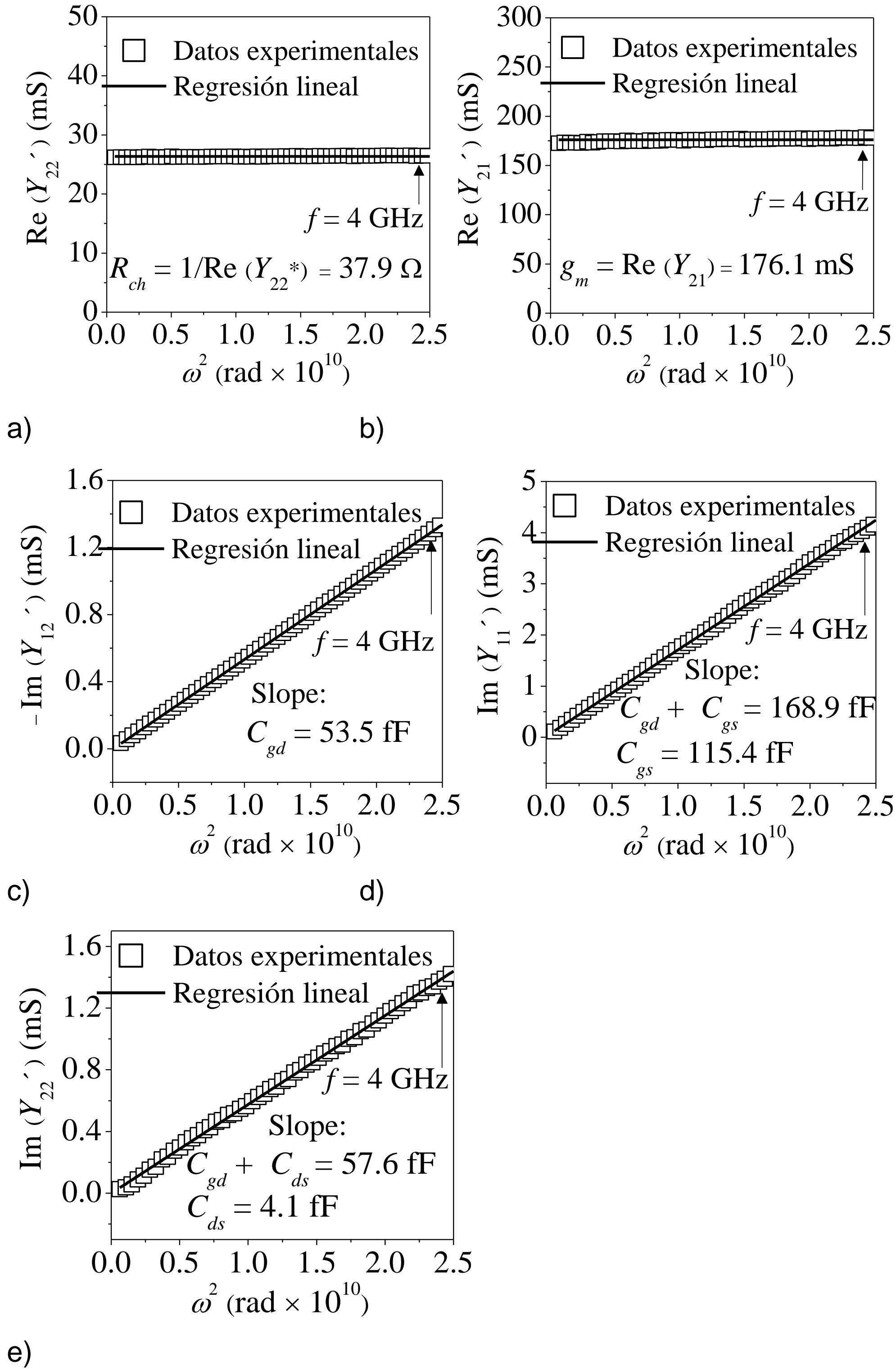

Figure 3.4. *Linear regressions to obtain: a) R_{ch}, b) g_m, c) C_{gd}, c) C_{gs} and d) C_{ds} at $V_{gs} = 0.6$ V, $V_{bs} = 1$ V and $V_{ds} = 0.7$ V.*

3.2 DETERMINATION OF MOSFET PARAMETERS IN SATURATION REGIME

After fully characterizing the MOSFET when Vds is fixed at zero, the substrate parasitic network and the series parasitic resistances can be determined while gm is neglected. As a result of this, S21 and S12 are equal to each other. However, in practice, the operation of the transistor is normally established to be in strong inversion under different values of Vds, which requires the comparison between the experimental and simulated data in the active region. Consequently, Vds is varied in three different values, 0.5 V, 0.6 V and 0.7 V. In addition, it was considered a Vgs of 0,6 V to ensure the inversion of the channel, varying Vbs from -1.2 V to 0 V in steps of 0,1 V.

To extract the elements of the small-signal equivalent circuit, the previously obtained values for R_d and R_g are removed from experimental Z parameters for the DUT, which is given by:

$$Z_1 = Z_{DUT} - \begin{bmatrix} R_g & 0 \\ 0 & R_d \end{bmatrix} \tag{3.5}$$

Then, the elements of the substrate parasitic network C_{jd} and R_b are subtracted from Z_1, which can be written as:

$$Y_2 = Z_1^{-1} - \begin{bmatrix} 0 & 0 \\ 0 & \dfrac{\omega^2 C_{jd}{}^2 R_b}{1+\omega^2 C_{jd}{}^2 R_b{}^2} + j\dfrac{\omega C_{jd}}{1+\omega^2 C_{jd}{}^2 R_b{}^2} \end{bmatrix} \tag{3.6}$$

The capacitance C_{js} has not been considered in equation (15). This assumption is valid up to 4 GHz for the studied devices. Finally, the matrix Y_2 is corrected by subtracting the value of R_s. This is presented in the following equation:

$$Y' = \left(Y_2^{-1} - \begin{bmatrix} R_s & R_s \\ R_s & R_s \end{bmatrix} \right)^{-1} \tag{3.7}$$

where Y' is the matrix of the corrected experimental data that describe the intrinsic parameters C_{gs}, C_{gd}, C_{ds}, g_m and R_{ch} of the MOSFET. In this way, the real

and imaginary parts of the admittance matrix Y' can be written in term of the elements of the intrinsic parameters, which is given by:

$$Y_{11}' = j\omega\left(C_{gs} + C_{gd}\right) \tag{3.8}$$

$$Y_{12}' = -j\omega C_{gd} \tag{3.9}$$

$$Y_{21}' = g_m - j\omega C_{gd} \tag{3.10}$$

$$Y_{22}' = R_{ch}^{-1} + j\omega\left(C_{ds} + C_{gd}\right) \tag{3.11}$$

Furthermore, the intrinsic parameters can be determined by using the linear regression of the experimental data and the equations (3.8) through (3.11), which is presented in Figure 3.4. In turn, in Figure 3.5 and Figure 3.6, it is illustrated the comparison between measurements and simulations of S parameters up to 20 GHz at V_{gs} = 0,6 V, V_{bs} = 1 V and V_{ds} = 0.7 V, and thus, a good agreement is achieved. This procedure should be followed by all bias conditions given for the different values of Vbs and V_{ds}.

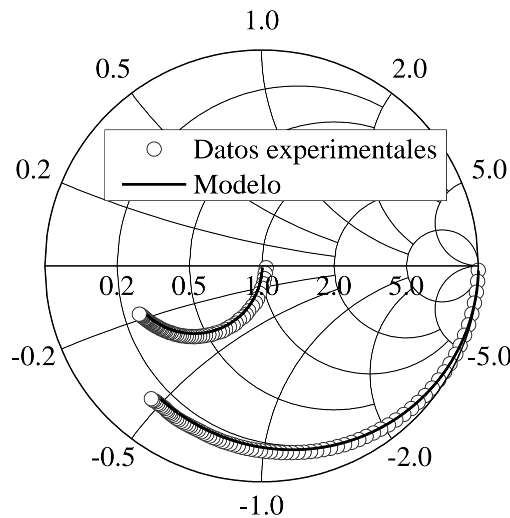

Figure 3.5. *Validation of the model up to 20 GHz for S_{11} and S_{22} at V_{gs} = 0.6 V, V_{bs} = 1 V and V_{ds} = 0.7 V.*

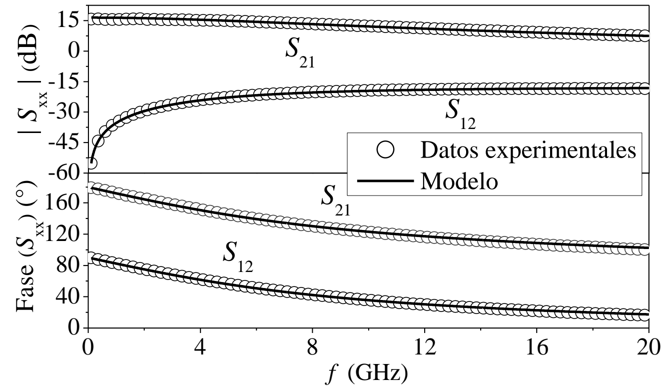

Figura 3.6. Validation of the model for S_{12} and S_{21} at V_{gs} = 0.6 V, V_{bs} = 1 V and V_{ds} = 0.7 V.

On the other hand, the dependence of g_m on V_{bs} for different values of V_{ds} is shown in Figure 3.7. In this fashion, g_m becomes smaller when the magnitude of V_{bs} increases or of V_{ds} decreases. This behavior is due to the increases of the depletion region in both source and drain sides with V_{bs} and to the electric field in horizontal direction because of V_{ds}.

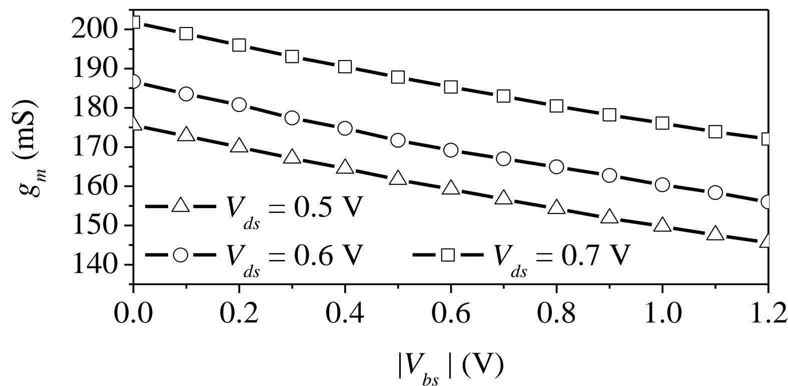

Figura 3.7. *g_m against V_{bs} for different values of V_{ds} at V_{gs} = 0.6 V.*

4 DEGRADATION OF RF MOSFET PARAMETERS

Due to the aggressive scaling down of CMOS in advanced technologies, the transistor has to operate at a high magnitude of electric field when it is biased, which originate hot-carrier-injection (HCI) [**50**], [**51**]. For this reason, in order to predict possible IC failures, the study of semiconductor device reliability is required. In spite of the fact that MOSFET's degradation under DC bias condition has been extensively analyzed, the understanding of it in AC regime is currently required because of its corresponding application at RF and microwave frequencies. Thus, in order to incorporate HCI effects into an RF model, it is necessary to take into account that the undesirable effects of HCI stress affect some equivalent circuit elements.

4.1 HOT CARRIER STRESS CONDITION

In order to do the evaluation of bulk MOSFETs degradation induced by HCI, a given i_d is applied to the drain terminal and simultaneously, I_b related to impact ionization is monitored, which can be considered as a suitable figure of merit to characterize HCI. To achieve this, the substrate and source terminals are not tied together as it was previously mentioned. This is a remarkable issue given that conventional pad configurations for measuring two-port S-parameters of transistors does not provide an independent substrate terminal, which does not allow controlling HCI degradation by means of an immediate quantification of the value of I_b. With the aim of formalizing the methodology here presented, it is convenient to define two parameters, (I_{bHC}) and (t_{HC}), to establish the magnitude of I_b wherein hot-carrier mechanism is evident and the time intervals that allows one to examine the gradual degradation of the device, respectively. As a result of the eventual variations of MOSFET's parameters due to the uncertainty of the fabrication process and to the advanced technology nodes that involves a continuous scaling, there is no an analytical way to find both I_{bHC} and t_{HC} bearing in mind all these

differences. Consecutively, a prior method states that I_{bHC} can be fixed at the point in which I_b reaches 1 % of I_d and then, a noticeable device degradation is generated with t_{HC} in the order of minutes [**52**]. In this approach, however, relatively large transistor sizes, in which the minimum L_m is equal to 0.18 µm, are taken into account. On the contrary, in this work, L_m is fixed at 80 nm for the measured devices and then, it is necessary a reduction of I_{bHC} and t_{HC} to perform a gradual degradation.

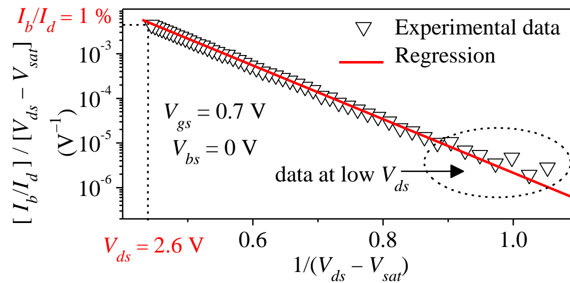

Figure 4.1. *Data regression to obtain the drain voltage to perform degradation.*

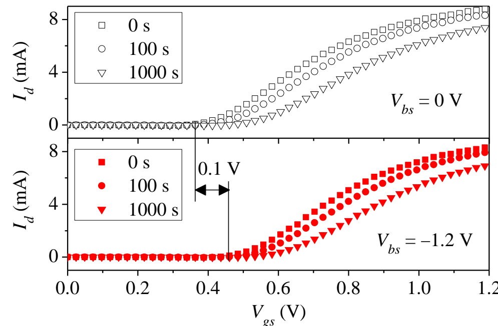

Figure 4.2. *Experimental I_d versus V_{gs} curves at V_{ds} = 50 mV at different times and two different bulk biasing conditions V_{bs} = 0 (top) and −1.2 V (bottom).*

Once a suitable assessment of a thorough set of measurements in DC regime was accomplished, I_{bHC} should be 1 % of I_d. With the aim of determining the required bias condition to do this, a relationship between the I_b/I_d ratio and applied voltages should be carried out. For it, the following estimated expression can be used [**53**]:

$$\frac{I_b}{I_d} = \frac{A_i}{B_i} \times (V_{ds} - V_{sat}) \times \exp\left(-\frac{l_d B_i}{V_{ds} - V_{sat}}\right), \tag{4.1}$$

where l_d is the effective ionization length, V_{sat} is the drain saturation voltage obtained, and A_i and B_i are the ionization constants. In accordance to equation (1), it is possible to linearize it while plotting on a semi-logarithmic scale the values of $(I_b/I_d)/(V_{ds}–V_{sat})$ as a function of $1/(V_{ds}–V_{sat})$. For this, (I_b/I_d) can be experimentally obtained by varying V_{ds} for a given V_{gs} and V_{sat} can be found by following the proposal in [**54**]. Consecutively, in Figure 4.1, the linear regression of experimental data is presented. In this fashion, it provides a good linear fitting for almost all considered values of V_{ds} with the exception of data at lowest V_{ds}. In this range of voltages, however, there is no a perceptible degradation and then, it does not significantly affect the results. In order to guarantee that I_b is eventually generated by HCI instead of the applied voltage to the substrate, V_{bs} is fixed at zero. Following this condition, the corresponding V_{ds} to perform the HCI degradation experiment from an initial measurement is found, which requires the damage of one of the devices. It is remarkable to point out that this can be avoided by extrapolating data at relatively low V_{ds} to determine the degradation condition without practically modifying the characteristics of the device before starting the degradation experiment. With the purpose of achieving a value of I_{bHC} of 1 % of I_d that corresponds to 0.67 mA, the required bias condition should be set at V_{gs} = 0.7 V, V_{ds} = 2.6 V, and V_{bs} = 0 V. This gives as a result an electric field along the channel length of ~30 MV/m for the employed devices.

In accordance to the experiment, the parameters of the transistor vary in a more emphasized way at the first degradation time intervals and on the contrary, this is insignificant when the degradation time goes up. Following this trend, t_{HC} is selected to be shorter at the initial degradation stage and gradually larger while the MOSFET's degradation process is in progress, which allows reducing the total time of measurements without penalizing the resolution of the characterization technique. For this reason, t_{HC} changes from 0 s to 1000 s by using different steps of 25 s, 50 s, 100 s and 500 s, taking into account more points at lower time instants.

As a consequence of the charge trapping into the gate oxide that is generated by HCI stress, the charge carrier concentration formed in the inversion channel is considerably decreased, which increases the subsequent channel impedance

while reducing I_d. This trend can be observed in Figure 4.2 that illustrates two groups of I-V characteristic curves, corresponding to two different values of V_{bs}, 0 V and –1.2 V. Notice in this figure that a voltage shift on the V_{gs} axis of about 0.1 V is obtained when V_{bs} changes from 0 to –1.2 V, which is mainly due to the dependence of V_{th} with V_{bs}. V_{th} was extracted by using the conventional linear region extrapolation method and then, an increasing of it with t_{HC} is evidenced, as shown in Figure 4.3. Indeed, the slope of V_{th} becomes smaller for larger time intervals, resulting in a power law trend as follows [**55**]:

$$\frac{|\Delta V_{th}|}{V_{th0}} \times 100 = A \times t_{HC}{}^{n}, \tag{4.2}$$

where A is the magnitude of degradation that is related to the number of excess carriers caused by impact ionization at the drain side when carrier-carrier collisions happen, V_{th0} is V_{th} at 0 s, $|\Delta V_{th}| = |V_{th} - V_{th0}|$ and n is a fitting parameter that takes into account the power law trend. Since A is bias dependent, A is determined by means of the linear regression in a logarithmic scale of $|\Delta V_{th}|/V_{th0}$ versus t_{HC} data for a given V_{bs}. In a similar way, n can be found. The extraction of A and n is presented in Figure 4.4 for two different values of V_{bs}. In this fashion, A and n are equal to 0.78 $s^{-0.5}$ and 0.5 at V_{bs} = 0 V and to 1.18 $s^{-0.5}$ and 0.5 at V_{bs} = −1.2 V. It means that A increases a 51% while V_{bs} changes from 0 to –1.2 V, which is due to holes that get enough energy by impact ionization to reach the bulk terminal.

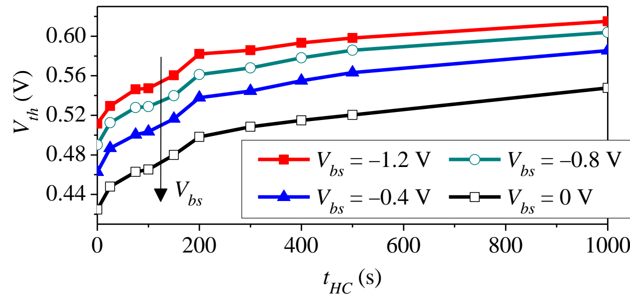

Figure 4.3. *Extracted V_{th} as a function of stress time under different V_{bs}.*

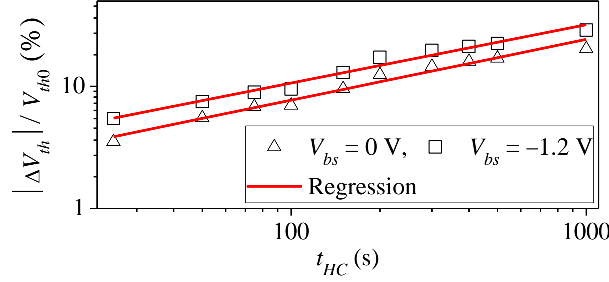

Figure 4.4. *Logarithmic* $|\Delta V_{th}|/V_{th0}$ *versus stress time data regressions at two different* V_{bs} *to obtain the parameters in (4.2).*

4.2 Extraction of Small-Signal Parameters for RF MOSFETs in the Linear Regime

To start the degradation assessment of RF-MOSFET extrinsic parameters, the corresponding applied voltages is established to be in the linear region in which the inversion channel is approximately uniform. The required methodology for the extrinsic parameter extraction is explained in a previous section, where the zero-bias FET and strong inversion conditions are used. Once R_s, R_d, R_b and C_{jd} are correctly determined for all considered t_{HC}, it can be observed that these equivalent circuit elements are practically independent of t_{HC}, as shown in Figure 4.5. Furthermore, an increase trend of R_{ch} associated with the excess of carriers into the gate oxide is noticeable. The dependence of R_{ch} on V_{gs} can be written as follows:

$$1/R_{ch} = \left(\mu_{eff} C_{OX} W_{total} / L_{eff}\right) \times (V_{gs} - V_{th}), \tag{4.3}$$

This equation can be rearranged as

$$\mu_{eff} C_{OX} / L_{eff} = \left[R_{ch} W_{total} \times (V_{gs} - V_{th})\right]^{-1}, \tag{4.4}$$

where μ_{eff} is the effective mobility, C_{OX} is the oxide capacitance per unit area, $W_{total} = W_f N_f$ is the total gate width, and L_{eff} is the effective gate length. Notice that the parameters on the right side of (4.4) has been previously obtained and then, the term $\mu_{eff}C_{OX}/L_{eff}$ can be found. The curve of the values of $\mu_{eff}C_{OX}/L_{eff}$ as a function of t_{HC} is illustrated in Figure 4.6. This exhibits a monotonically decreasing

behavior from 0 s to 400 s related to the decreasing of L_{eff} and C_{OX}, and the increasing of μ_{eff}. Indeed, the variation of C_{OX} and L_{eff} are due to the damage of the gate oxide and to the reduction of the carrier concentration into the channel, respectively. Given that the scattering process involved in carrier-carrier collisions is lower than normally, a change of μ_{eff} makes evident. Once the charge carrier concentration of the inversion channel goes down to less than that of LDD regions for a particular V_{gs} value at V_{ds} = 0 V, L_{eff} is almost independent of t_{HC}. In addition, C_{OX} decreases and μ_{eff} increases at the same rate. For these two reasons, $\mu_{eff}C_{OX}/L_{eff}$ is approximately constant in Figure 4.6 with a value of ~0.5×10^4 $\Omega^{-1}V^{-1}m^{-1}$ over 400 s.

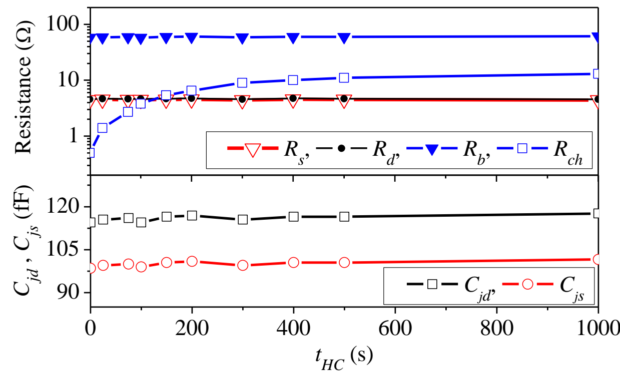

Figure 4.5. *Extracted R_{ch}, R_s, R_d and R_b as a function of stress time at V_{ds} = 0 V, V_{gs} = 0.7 V and V_{bs} = −1.2 V.*

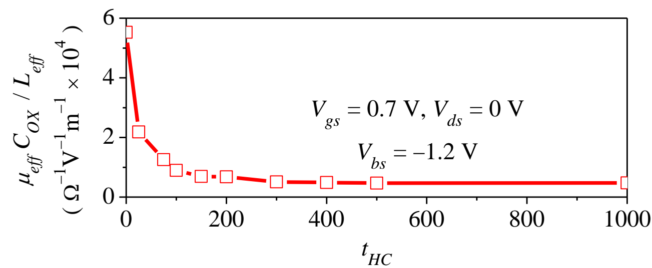

Figure 4.6. *μ_{eff} C_{OX} / L_{eff} as a function of stress time.*

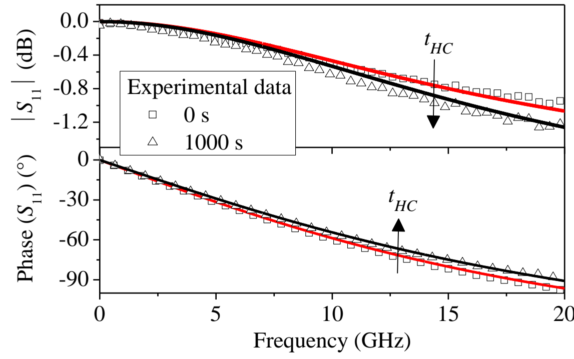

Figure 4.7. *Experimental (symbols) and simulated (continuous line) data of S_{11} up to 20 GHz varying stress time at $V_{ds} = 0$ V, $V_{gs} = 0.7$ V and $V_{bs} = -1.2$ V*

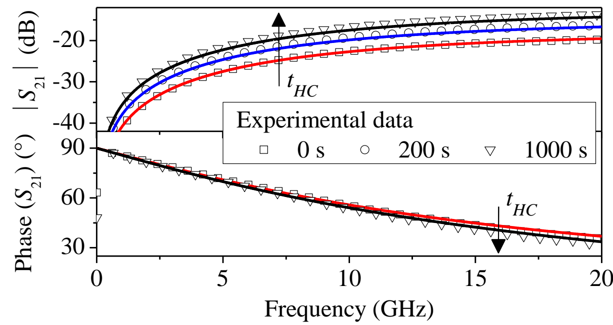

Figure 4.8. *Experimental (symbols) and simulated (continuous line) data of S_{21} varying stress time at $V_{ds} = 0$ V, $V_{gs} = 0.7$ V and $V_{bs} = -1.2$ V.*

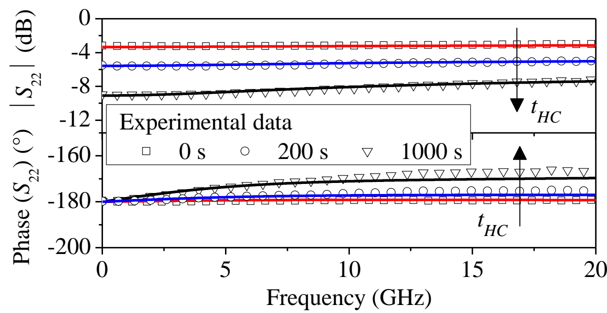

Figure 4.9. *Experimental (symbols) and simulated (continuous line) data of S_{22} varying stress time at $V_{ds} = 0$ V, $V_{gs} = 0.7$ V and $V_{bs} = -1.2$ V.*

After obtaining all parameters at each considered t_{HC}, a model-experiment

assessment was carry out by comparing the S-parameters of the RF-MOSFET in the linear region up to 20 GHz. Accordingly, it is achieved a good agreement between measured and simulated data that validates the extraction procedure, as shown in Figure 4.7 through Figure 4.9.

4.3 Extraction of Small-Signal Parameters for RF MOSFETs in the Saturation Regime

In order to perform the analysis of the MOSFET with an emphasis on practical applications, the subsequent voltages applied to the device are assumed to be in the active region for which V_{gs} is set to a given value in strong inversion regime while varying V_{ds} and V_{bs} [**56**]. Notice that this DC bias is required to study the small-signal intrinsic parameters stressed under HCI conditions at room temperature and then, the impact of aging on the device can be evaluated. Therefore, before measuring the transistor at high frequency, V_{gs} should be chosen to be well above V_{th} for all bias conditions even after the transistor is degraded. Using Figure 4.3 as a reference, V_{gs} was fixed at 0.7 V in the present analysis. Moreover, V_{ds} was considered to be equal to 1.2 V that corresponds to the nominal value for the studied devices and V_{bs} was changed from –1.2 V to 0 V. As it was previously mentioned in **Chapter 3**, linear regressions of the experimental data were done after subtracting the undesirable effects of the substrate parasitics and the source and drain resistances [**34**]. Once the intrinsic parameters, R_{ch}, g_m, C_{gd}, C_{gs} and C_{ds}, are known, the degradation of each one of them can be analyzed as the sum of its respective value at 0 s plus its variation for a particular t_{HC}, as shown in Figure 4.10.

In accordance to the gate oxide damage due to the aging process, g_m.decreases and R_{ch} increases with t_{HC} affecting the MOSFET reliability of the device, which is illustrated in Figure 4.11. This trend is because of the charge carriers in the saturation regime that flows toward the pinch-off zone by ballistic transport, which means that there are no scattering events. Furthermore, high energy carriers generated near the drain edge can be redirected and injected into the gate oxide. Similarly to V_{th}, the relationship between g_m and R_{ch} with t_{HC} can be represented by means of a power law trend, as shown in Figure 4.12. By the way, it is important to point out that the slopes of the regressions to find the respective models for $|\Delta g_m|/g_{m0}$ and $|\Delta R_{ch}|/R_{ch0}$ do not significantly vary with V_{bs}, and are

equal to 0.5 and 0.6, respectively.

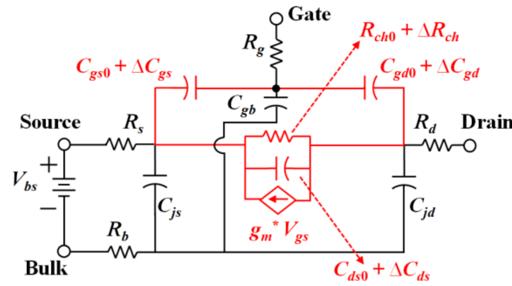

Figure 4.10. *Equivalent circuit in the saturation regime, considering the degradation of the MOSFET´s intrinsic parameters. Here,* $g_m{}^* = g_m\, e^{-j\omega\tau}$ *and* $g_m = g_{m0} + \Delta g_m$.

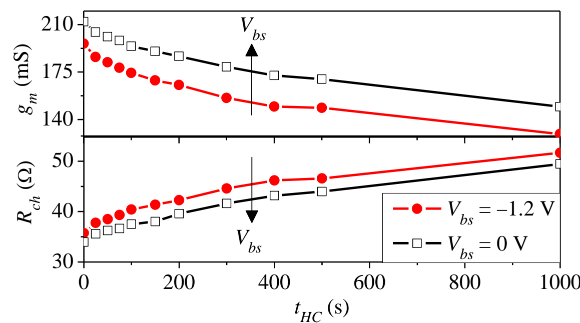

Figure 4.11. *Extracted* g_m *and* R_{ch} *as functions of stress time at* V_{ds} *= 1.2 V and* V_{gs} *= 0.7 V.*

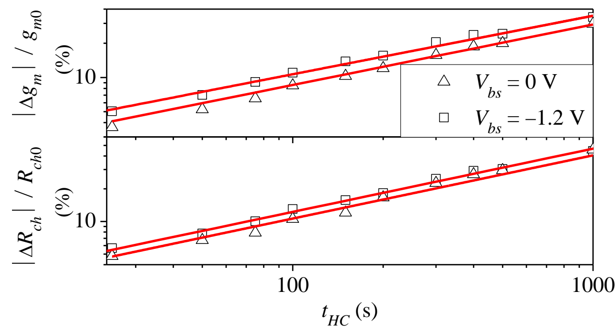

Figure 4.12. $|\Delta g_m| / g_{m0}$ *and* $|\Delta R_{ch}| / R_{ch0}$ *versus stress time at* V_{ds} *= 1.2 V and* V_{gs} *= 0.7 V.*

In the case of C_{gd}, a small change of it as a function of t_{HC} is observed due to

the charge reduction of the inversion region near the drain diffusion region in the saturation regime. Given that this behavior is also presented at the source side, C_{gs} goes down with the aging of the device. C_{gd} and C_{gs} are plotted for two values of V_{bs} in Figure 4.13 and their corresponding regressions to extract the model parameters are shown in Figure 4.14. Similarly, the decreasing of C_{ds} with t_{HC} is noted, which is illustrated in Figure 4.15. Consecutively, the regression of $|\Delta C_{ds}|/C_{ds0}$ can be seen in the inset of Figure 4.15. The slopes of $|\Delta C_{gs}|/C_{gs0}$, $|\Delta C_{gd}|/C_{gd0}$ and $|\Delta C_{ds}|/C_{ds0}$ seem to be independent of V_{bs}. Accordingly, their intercepts are influenced by V_{bs}, which bears in mind the number of excess carriers caused by impact ionization. All obtained parameters are summarized in Table 4.1, which allows calculating each element at any time of the transistor aging.

The intrinsic elements of the small-signal equivalent circuit are corroborated by means of the comparison between measured and simulated two-port S-parameters varying t_{HC} at V_{ds} = 1.2 V, V_{gs} = 0.7 V and V_{bs} = –1.2 V, is shown in Figure 4.16 wherein the shift to the right of S_{22} and S_{21} becomes evident. Following the equations in Table 4.1 and the equivalent circuit in Figure 4.10, the simulation was done. As the impedance of the output port is dependent on R_{ch}, the change of S_{22} with t_{HC} is more appreciable at low frequencies. On the other hand, the decreasing of g_m that is associated with the real part of admittance Y_{21} modifies S_{21}.

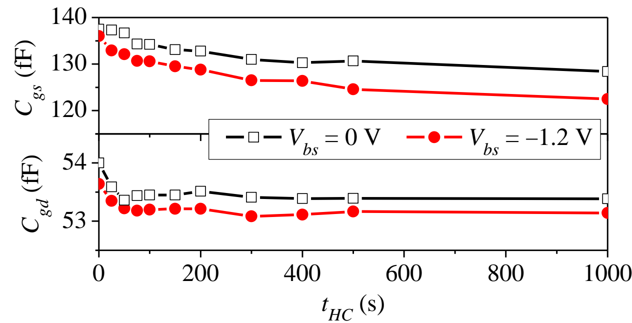

Figure 4.13. *Extracted C_{gs} and C_{gd} as functions of stress time at V_{ds} = 1.2 V and V_{gs} = 0.7 V.*

TABLE 4.1

EXPRESSIONS FOR THE INTRINSIC PARAMETERS

Intrinsic parameter	Equation at V_{bs} = 0 V	Equation at V_{bs} = −1.2 V
$g_{m0} + \Delta g_m$ (mS)	$212 (1 – (0.7/100)\times t_{HC}^{0.5})$	$196 (1 – (1/100)\times t_{HC}^{0.5})$
$R_{ch0} + \Delta R_{ch}$ (Ω)	$34 (1 + (0.007/100)\times t_{HC}^{0.6})$	$36 (1 + (0.008/100)\times t_{HC}^{0.6})$
$C_{gs0} + \Delta C_{gs}$ (fF)	$138 (1 – (0.4/100)\times t_{HC}^{0.4})$	$136 (1 – (0.6/100)\times t_{HC}^{0.4})$
$C_{gd0} + \Delta C_{gd}$ (fF)	$54 (1 – (0.6/100)\times t_{HC}^{0.07})$	$53.6 (1 – (0.7/100)\times t_{HC}^{0.07})$
$C_{ds0} + \Delta C_{ds}$ (fF)	$91 (1 – (1.4/100)\times t_{HC}^{0.5})$	$85 (1 – (1.8/100)\times t_{HC}^{0.5})$

With the aim of accomplishing the comparison of the proposal here presented with a previously published methodology to characterize the MOSFET degradation, reference [**1**] was employed using the experimental data from this work. This was done at V_{ds} = 1.2 V, V_{gs} = 0.7 V and V_{bs} = –1.2 V for a stress time of 1000 s, as shown in Figure 4.17. Despite the fact that the dependence of intrinsic parameters on the applied voltages are correctly modeled by means of [**1**], the absence of taking into account the effect of the substrate elements and of the bias dependent components of R_s and R_d exhibits visible inconsistencies in the simulated data at higher frequencies. This means that the influence of HCI stress on the intrinsic elements of the device should be studied without neglecting the extrinsic characteristics to make a suitable model. Otherwise, their effects will be erroneously incorporated on other parameters.

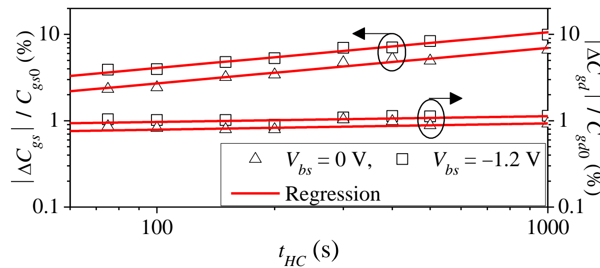

Figure 4.14. *$|\Delta C_{gs}| / C_{gs0}$ and $|\Delta C_{gd}| / C_{gd0}$ as a function of stress time at V_{ds} = 1.2 V and V_{gs} = 0.7 V.*

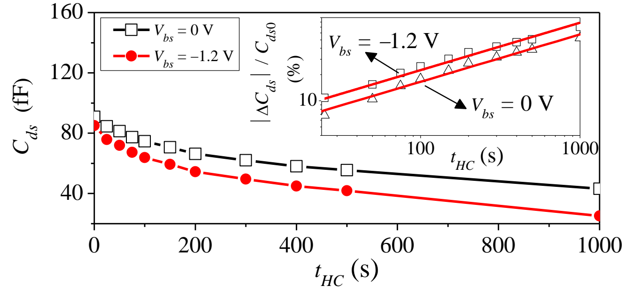

Figure 4.15. *C_{ds} and $|\Delta C_{ds}| / C_{ds0}$ (inset) as a function of stress time at V_{ds} = 1.2 V and V_{gs} = 0.7 V.*

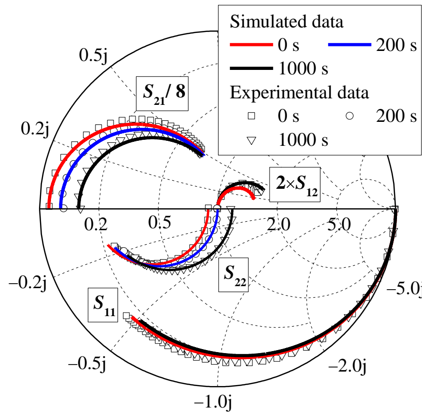

Figure 4.16. *Two-port S-parameters up to 20 GHz at V_{ds} = 1.2 V, V_{gs} = 0.7 V and V_{bs} = −1.2 V for three different stress times.*

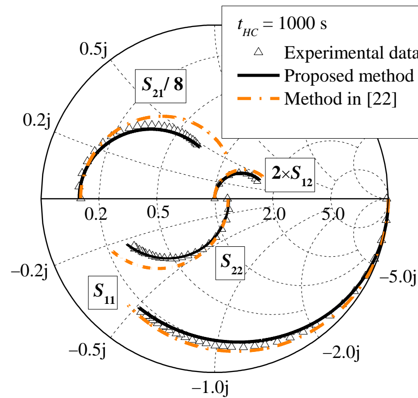

Figure 4.17. *Experimental and simulated two-port S-parameters up to 20 GHz at V_{ds} = 1.2 V, V_{gs} = 0.7 V and V_{bs} = −1.2 V, using the proposed method and the method in* [**1**].

5 CONCLUSIONS

After performing DC and RF measurements on multi-fingered bulk MOSFETs operating in linear regime, the implementation of an accurate extraction methodology of parameters was developed to properly represent I-V characteristic and high-frequency small-signal AC response for the considered devices. An excellent model-experiment agreement was accomplished, considering different bias-conditions and geometry. Moreover, physical parameters such as the drain-to-source conductance, the subthreshold swing, the effective gate length and the threshold voltage were determined by applying well-known DC techniques to RF measured data instead of current–voltage curves. With the aim of providing a validity of the proposal, the resultant drain currents measured with a semiconductor device analyzer for various gate voltages were accurately reproduced by processing experimental S-parameters. It is important to remark that complete comparisons were also carried out to demonstrate the advantages of directly implementing DC models using experimental RF data.

Once an exhaustive analysis of the possible dependence of small-signal parameters with extrinsic geometry was done, it was found that there were considerable variations not only in the gate resistance but also in the series parasitic resistances, which would eventually affect the design and simulation of RF circuits with multi-fingered MOSFETs. As a consequence of this, the effect of the previous mentioned parasitics should be taken into account to avoid the misrepresentation of S-parameters of the considered devices and the associated derived quantities. A scalable model to characterize the source and drain resistances for RF bulk MOSFETs varying the number of fingers with a fixed total gate area was developed. It follows an excellent correlation to RF measured data, and puts emphasis on the effects associated with multi-fingered layouts that cannot be neglected. Furthermore, this is particularly accentuated when the number of fingers becomes smaller or the operation frequency increases.

On the other hand, the assessment of degradation induced by hot carrier injection into gate oxide for small-signal model parameters of microwave MOSFETs under different bulk bias conditions was studied. With the aim of establishing a suitable

stress condition to gradually degrade the device, the bulk current was monitored to obtain the necessary drain-to-source voltage and degradation time steps. For this purpose, a separate bulk terminal is provided to measure the bulk current and to vary the bulk-to-source voltage. Hence, the variations in the small-signal equivalent circuit elements and in the threshold voltage were calculated by means of thorough measurements and extraction methodologies at several degradation stages. Based on the fact that the aging of the resultant parameters follows a power law trend, the high-frequency behavior of the device as degradation takes place was well represented.

6 List of Published Work

6.1 Journal Publications

A. Sucre González, F. Zárate-Rincón, A. Ortiz conde, R. Torres Torres, F. J. García Sánchez, J. Muci and, R. S. Murphy-Arteaga, "A DC method to extract mobility degradation and series resistance of Multi-Finger Microwave MOSFETs," *IEEE Trans. on Electron Devices*, pp. 1 - 6, 2016.

F. Zarate-Rincon, D. Garcia-Garcia, V. H. Vega-Gonzalez, R. Torres-Torres, R. S. Murphy-Arteaga, "Characterization of Hot-Carrier-Induced RF-MOSFET Degradation at Different Bulk Biasing Conditions From *S*-Parameters," *IEEE Trans. on Microwave Theory and Techniques*, pp. 125 - 132, 2016.

F. Zarate-Rincon, R. Torres-Torres, R. S. Murphy-Arteaga, "Consistent DC and RF MOSFET Modeling Using an *S*-Parameter Measurement-Based Parameter Extraction Method in the Linear Region," *IEEE Trans. on Microwave Theory and Techniques*, pp. 4255 - 4262, 2015.

F. Zarate-Rincon, R. S. Murphy-Arteaga, R. Torres-Torres, A. Ortiz-Conde, and F. J. García-Sánchez, "Modeling the Impact of Multi-Fingering Microwave MOSFETs on the Source and Drain Resistances," *IEEE Trans. on Microwave Theory and Techniques*, pp. 3255 - 3261, 2014.

F. Zarate-Rincon, G. A. Alvarez, R. Torres, R. S. Murphy, and S. Decoutere, "Characterization of RF-MOSFETs in Common-Source Configuration at Different Source-to-Bulk Voltages From S-Parameters," *IEEE Trans. on Electron Devices*, vol. 60, no. 8, pp. 2450 – 2456, 2013.

6.2 PUBLICATIONS IN CONFERENCE PROCEEDINGS

F. Zarate, V. Vega, I. Ciofi, C. Wilson, M. van der Veen, P. Roussel, J. Boemmels, Z. Tokei, R. Torres, and R. S. Murphy "Pitch Walking Assessment after Self-aligned Double Patterning for the 10 nm Logic Technology Node," in *Materials for Advanced Metallization - MAM*, Brussels, 2016.

F. Zarate-Rincon, R. Torres-Torres, R. S. Murphy-Arteaga, "Correction of DC extracted parameters for microwave MOSFETs based on S-parameter measurements," in *IEEE MTT-S International Microwave Symposium*, Phoenix, 2015, pp. 1 - 4.

F. Zarate-Rincon, G. A. Álvarez-Botero, R. S. Murphy-Arteaga, R. Torres-Torres and A. Ortiz-Conde, "Impact of Multi-Finger Geometry on the Extrinsic Parasitic Resistances of Microwave MOSFETs," in *IEEE MTT-S International Microwave Symposium*, Tampa, 2014, pp. 1–3.

R. S. Murphy, R. Torres, and F. Zarate-Rincon, "Understanding the Properties of Rf-MOSFETs Using the Smith Chart," in *WEEF*, Cartagena, 2013.

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