PVT Compensated PLL in 45nm SOI-CMOS Technology

By

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INAOE

“ A mi toda mi familia, en especial a mi madre Q.E.P.D.
A Mildred”

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RESUMEN

TÍTULO: PLL compensado ante PVT en tecnología SOI-CMOS de 45nm.

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PALABRAS CLAVE: PLL, PVT, compensación, oscilador de anillo, jitter, *SOI-CMOS*.

DESCRIPCIÓN:

En este trabajo se plantea el diseño de un PLL compensado ante variaciones de proceso, voltage y temperatura —PVT—, el cual se basa en un oscilador de anillo para su funcionamiento; el circuito es diseñado en una tecnología nanométrica, específicamente en el proceso de 45nm SOI-CMOS de IBM.

Inicialmente se presenta el impacto de las variaciones PVT en un circuito analógico; a su vez se hace una descripción de la tecnología en uso, así como de sus desventajas para diseñar circuitos analógicos.

Seguido a esto, se realiza una descripción del funcionamiento de un PLL y la influencia de las variaciones PVT en sus parámetros de desempeño, tales como ancho de banda y tiempo de establecimiento. Se realiza una descripción de cada uno de los bloques que conforman el PLL resaltando su variabilidad con PVT. Posteriormente se realiza el diseño de cada uno de estos, haciéndo énfasis en ciertas consideraciones de diseño que aumentan la rubustes del circuito. Se selecciona una topología de máquina de estados para el detector de fase por su elevado rango de excursión. En cuanto a la bomba de carga se propone la conexión de un amplificador de voltage en su nodo de salida con el fin de reducir su rango dinámico; esto reduce el mismatch entre las corrientes UP y DOWN debido al efecto de modulación de canal.

Para el oscilador de anillo se selecciona una topología pseudo-diferencial controlada por corriente, con el fin de garantizar la simetría de la oscilación y reducir la variabilidad de la ganancia de entonado. Además, se propone un circuito de compensación específico, el cual ajusta su corriente de polarización de acuerdo al estado del proceso y la temperatura. Con esto se reduce la variación de la frecuencia central a 2.9% sobre 7.2GHz. En adición, se presenta el impacto del efecto historia de un transistor SOI en el establecimiento de la frequencia del oscilador.

Finalmente se implementa todo el PLL y se verifica su fincionamiento mediante la estimación de la respuesta en frecuencia mediante la caracterización de la respuesta transitoria. Como resultado se obtiene un PLL con una variación reducida en su ancho de banda, cuyo consumo de potencia es 5.4mW y *jitter* de 1.6ps RMS.

ABSTRACT

TITTLE: PVT Compensated PLL in 45nm SOI-CMOS Technology

AUTHOR: ANDRÉS FELIPE AMAYA BELTRÁN

KEY WORDS: PLL, PVT, compensation, ring oscillator, jitter, *SOI-CMOS*.

DESCRIPTION:

In this work the design of a compensated to process, voltage and temperature —PVT— PLL is presented, which is based in a ring oscillator. The circuit is designed in a nanometer technology, in the 45nm IBM SOI-CMOS process specifically.

At first, the impact of PVT variations on the performance of a analog circuit is presented; also, a description of the used technology as well as its disadvantages in the design of analog circuits is made.

The behavior of a PLL and the influence of PVT variations on its performance are described; the sensitivity of performance metric like bandwidth and settling time is presented. In addition, the behavior of all the components that form a PLL is studied, highlighting their variability to PVT. Then, the design of each one of them is made, making emphasis in some design considerations that increase the robustness of the circuit. The states-machine topology for the phase detector is selected because of high excursion range. For the charge pump, the use of an amplifier at its output is proposed, with the aim to reduce its dynamic range; this decrease the mismatch between the UP and DOWN currents due to the channel modulation effect.

For the ring oscillator a pseudo-differential current controlled topology is selected, in order to guarantee the symmetry of the oscillation waveform and to reduce the variability of the tuning gain. Moreover, a compensation network is proposed, which adjust the bias current based on the process condition and temperature. With this network a reduction of the variability of the free-running frequency to 2.9% over 7.2GHz is achieved. Furthermore, the impact of history-effect of a SOI transistors over the settling of the frequency of a ring oscillator is presented.

Finally, all the PLL is implemented and its performance is verified by the estimation of the frequency response through the characterization of the transient response. As a result, a PLL with a reduced variability of its bandwidth is achieved, whose power consumption is 5.4mW and jitter of 1.6ps RMS.

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CHAPTER 1

INTRODUCTION

The continuous scaling of the integrated circuits fabrication process has allowed the implementation of very high speed signal processors —mostly in the digital domain— at a high integration scale, that demand the increasing requirements of new emerging communications protocols. Data rates of Gigabits are actually present in today's very common communication devices as could be a cellular phone.

No matter the application for which the device is focused, these high speed processors need always reference or synchronism signals with a high accurate timing and stability, in order to guarantee a correct data transmission and processing; and a Phase Locked Loop —PLL— has became the standard solution to provided this kind of signals.

A PLL is a feedback system whose principal function is to control a high frequency oscillator based on a stable low frequency reference signal. Despite the oscillator is controlled by a feedback system, very common variations in the fabrication process, temperature or supply voltage (known as PVT variations) can disturb important parameters such as bandwidth, phase margin and settling time in the PLL. This variations are reflected in the spectral purity and timing of the output oscillation, because the noise level has a strong dependency of them. Moreover, in some cases all the circuit can become unstable wherefore all the system loses its functionality completely.

For those reasons, each circuit that is part of the PLL has been the focus of a large number of research by both academy and industry, looking for smaller, faster and cheaper solutions which can always work in any environment condition with tolerance to process and power supply variations.

Although the reduction in the dimension of the transistors is very beneficial to the digital circuits due to the increased operation speed as a consequence of the reduction of the parasitic capacitances, some undesired effects for the analog design such as channel modulation and

threshold voltage variation are getting worse. This is evidenced in the ease to obtain circuits which operate at Gigahertz scales, in contrast with the difficulty to develop voltage gains higher than 20 dB and 30 dB [19]. However, there is the necessity to include both analog and digital circuits in high speed mixed signal systems. For that reason, the develop of new design techniques that allow the use of nanometer devices in analog circuits is required.

Taking into account the above, this work addresses the design of a ring oscillator based PLL whose performance is robust to PVT variations. The system is implemented with the standard IBM 45 nm Silicon on Insulator - CMOS SOI technology.

This document is organized as follows: chapter 1 describes the importance of PVT variations in the design of analog circuits and some concepts about the SOI technology. In chapter 2 some ideas about the operation of a PLL are presented as well as the effect of PVT variations on its performance. In the next chapter, the methodology and all the considerations taken into account for the design of the low frequency components of PLL are described. Then, chapter 4 presents the design of a robust ring oscillator. Finally, chapter 5 presents the simulations results of the PLL and some conclusions result of this work.

1.1 PVT variations in the analog design

Process, voltage and temperature variations are defined as a set of random and deterministic variations which include changes in the electric parameters of the active and passive devices (such as transistors, resistors, capacitors and interconnections), the supply voltage and the temperature. This has a big influence in the performance of any circuit, specially in analog designs. In digital circuits, the power consumption and time delay are the parameters which have the highest sensitivity to PVT; however, no matter the kind of variations, its logic function tends to be correct. In the case of analog circuits, performance metrics like gain, bandwidth, phase margin, dynamic range and noise level are some of the specifications that PVT affect more dramatically. This aspect can lead to several problems, for example, a change in the dynamic range of a mixer could increase the distortion and make impossible a correct transmission; also, as was said before, changes in phase margin and bandwidth can lead to instability of the system, leaving the circuit useless.

With the purpose to understand in more detail the influence of PVT in analog circuit design, the source of these variations, as well as an example of their influence in a very common analog circuit is presented in the next paragraphs.

1.1.1 Process variations

First of all, it is important to introduce the concept of a stable fabrication process. A stable process means that its results are consistent, repeatable and its key process parameters do not vary over time; and it is important to stand out that this is the kind of process that all foundries offer. Nevertheless, despite the stable condition, it has some degree of variability

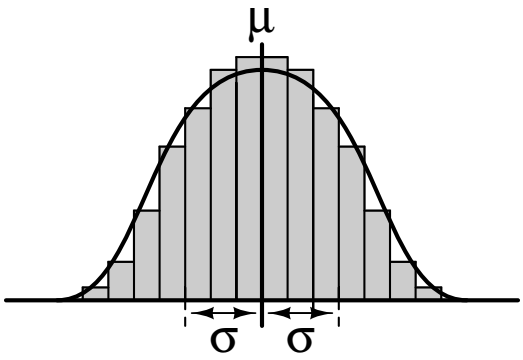


Figure 1.1: Typical Gaussian distribution of a parameter in a stable process

Parameter	$W = 3\ \mu m$	$W = 400\ nm$
V_T NMOS	13.8 mV	30.9 mV
I_D NMOS	2.64%	5.48%
V_T PMOS	12 mV	24.9 mV
I_D PMOS	2.39%	4.75%

Table 1.1: Standard deviation of some parameters of the IBM-SOI 45 nm technology. $L = 40\ nm$

which must occur around a mean, whereby the parameters of the devices will not be exactly the same in each fabrication; also, the results of the data collected for any of those should form a Gaussian distribution, as figure 1.1 shows [1]. For instance, table 1.1 presents the standard deviation of some of the parameters of the transistors that the IBM-SOI technology has [2]. In addition, all improvements in process control will tighten up the distribution (i.e. reduce the standard deviation σ) and will not modify the mean value of the parameter.

There are a lot of causes whereby process variations occur; lithographic, doping concentration and Chemical Mechanical Polishing - CMP - errors are the most influential, because they produce non-uniform and non-aligned layers as well as diffusions with different doping across all the wafer.

The inclusion of process variations in the model of the transistor and, therefore, in the circuit design, is made by grouping the maximum 3σ variations (i.e. the maximum and the minimum possible values of each parameter of both types of transistor) so that two kinds of devices are identified: fast ones and slow ones. The fast transistors involve those variations which increase their current capability, and cover for example a reduction in the threshold voltage and an increase in the carrier mobility. On the other hand, the slow transistors are the opposite to the fast ones, because they include variations that reduce their current capacity, for example an increase in the effective channel length.

Considering that the process variations are random and limited by their probabilistic dis-

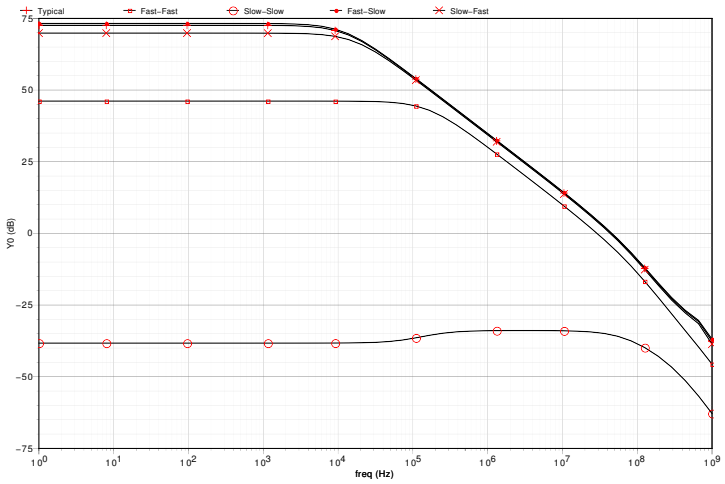


Figure 1.2: Frequency response of an OTA with process variations

tribution, a design procedure of robust circuits must evaluate the performance of the circuit in all the cases described above, taking into account each type of transistor and their combinations: when both are fast or slow, and when NMOS devices are fast while PMOS ones are slow and vice versa; these combinations correspond to the corners of the fabrication process. So, if the circuit meets its specifications in all the corners, it is assumed that the design is robust to any variation of the process because all of them will be less than the corners, i.e. less than the 3σ values [1]. It is important to note that, although there is some degree of correlation between the fabrication of NMOS and PMOS transistors in the same wafer, there is a big probability to produce transistors with opposite variations, specially in nanometer technologies.

As an example of the impact of process variations in analog circuits, figure 1.2 shows the changes of the frequency response of a one stage symmetric current amplifier with all the corners of the fabrication process. It could be appreciated a variation of 28 dB in its gain, and 100 MHz in its bandwidth; in addition, in the Slow-Slow corner the bias of the circuit is modified drastically wherefore some transistors enter in cut-off region.

1.1.2 Voltage variations

There are three main sources of variations of the power supply voltage:

- Most of the portable devices are battery powered, but batteries are not ideal power supplies because its voltage is subject to variations due mainly to its own discharge and temperature. Figure 1.3 shows the discharge curve of a 1.2 V battery for different loads; changes greater than 10% can be appreciated regardless its load.

- At intra-chip level, process variations and physical phenomena like electromigration could increase the resistance of the power distribution rails, hence the voltage applied

to each circuit of the chip is different and lower than the battery voltage. The amount of difference is dependent upon the current consumption.

- Any kind of noise coupled to the supply, such as from high switching digital circuits, could be considered as a voltage variation.

Power supply voltage has an strong influence in the performance of analog and digital circuits. In the case of digital circuits, it is one of parameters that defines the delay of logic gates, and thus the operating frequency of all the system; in analog circuits, a variation in supply voltage could lead to a change the operation region of some transistors and a modification in some characteristics, for example the output resistance and the gain.

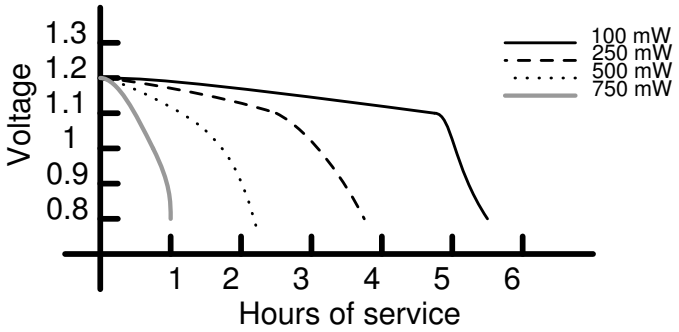


Figure 1.3: Discharge curves of a 1.2 V battery.

Figure 1.4 shows the frequency response of the same amplifier with changes in the supply voltage. A difference of 25 dB between the maximum and minimum value can be seen. When the supply voltage is 10%, the circuit does not work because of the dramatic change in the bias.

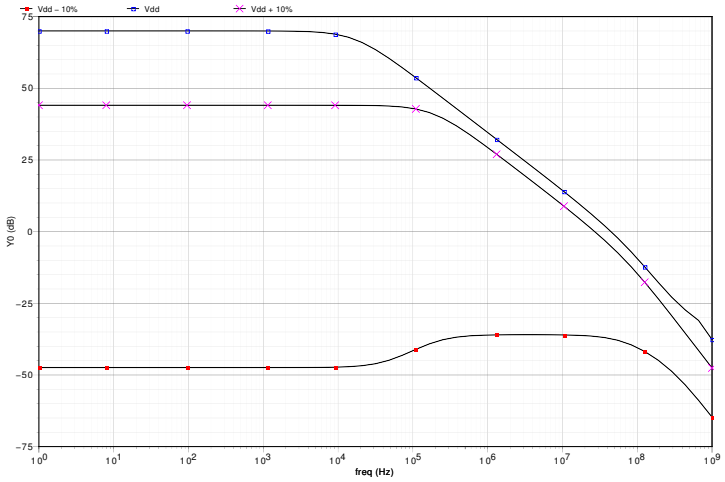


Figure 1.4: Frequency response of an OTA with power supply variations

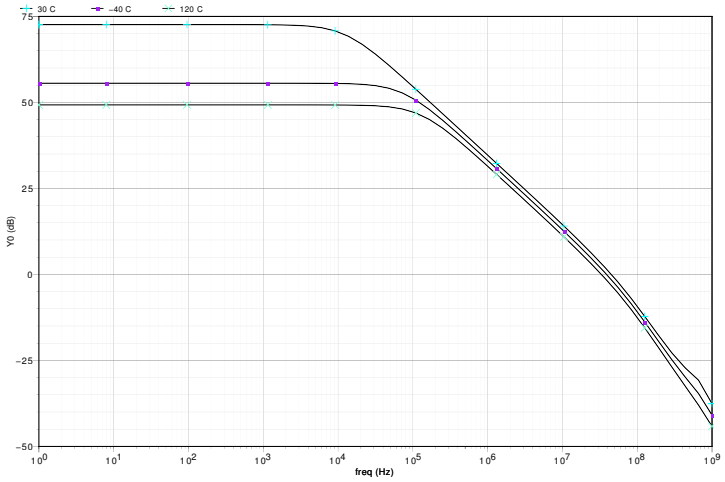


Figure 1.5: Frequency response of an OTA with temperature variations

1.1.3 Temperature variations

Temperature fluctuations has an important impact in some transistor parameters such as carriers mobility, threshold voltage and transconductance. This together with the impact over the interconnections and power rails results in a degradation of the performance at higher temperatures.

Variations in the temperature of the circuits can be produced by changes in the operating frequency of the device (the higher the frequency, the higher the current consumption and thus its temperature), self-heating effects as will be explained in the next section, and changes in the environment (weather).

To illustrate this behavior, figure 1.5 shows the variation in the gain and bandwidth of the same example with respect to the temperature. Low temperatures increase the current capability of the transistors, wherefore the transconductance of them is raised leading to an increase in the gain.

1.2 Silicon on Insulator - SOI technology

Silicon on Insulator technology is considered as an evolution to the traditional bulk CMOS technology. Its objective is to reduce some of the short channel effects that are getting worse with the continuous scaling of the transistors dimensions, and therefore to continue the Moore's law. Although its develop begun in the beginnings of 80's with the purpose to build circuits able to operate in high radiation and high temperature environments (military and space applications), only in the finals of 90's SOI devices were used in high-volume production applications. This was possible with the development of process and techniques that let a reduction in the fabrication costs. Moreover, some years later and with its continuous study, it could be appreciated that SOI technology constitute a solution to increase the performance

of nanometer transistors i.e. with channel length of 100 nm or less; this is due to some special behaviors explained later. These reasons justified the popularity of SOI technology today [3].

Figure 1.6 shows the structure of a wafer in this technology in contrast with a bulk CMOS one. The structure of a SOI wafer consists of a thin-film silicon layer where the devices are laid out over an insulator layer, which can be made of an oxide, sapphire or air. An important issue of SOI devices is the lack of an external polarization to the body like it is known in a bulk technology; it means that SOI devices have a floating body. As a consequence, it is common to refer a SOI transistor as a three terminals device. This characteristic allows that some undesired effects occur in the transistors, as will be explained bellow.

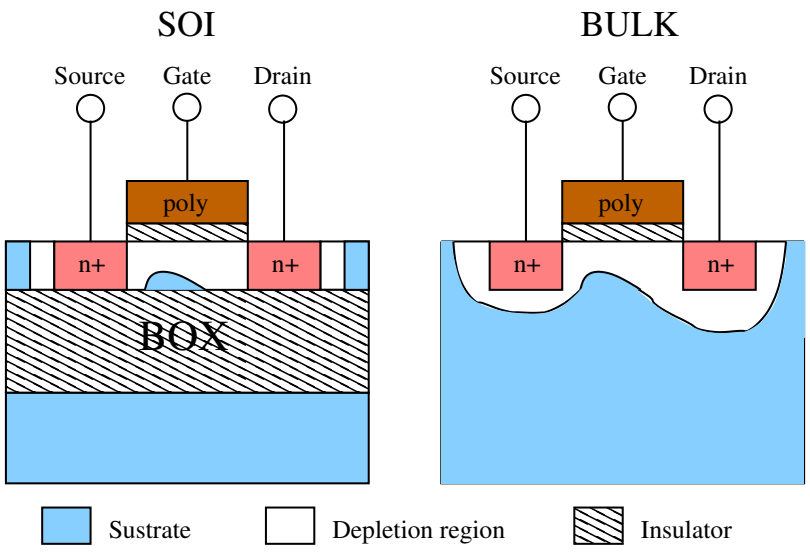


Figure 1.6: Cross section of SOI and Bulk CMOS wafers

There are two types of SOI transistors: fully depleted and partial depleted, and their difference lies on the thickness of the silicon layer, as figure 1.7 shows. When the thin-film silicon layer is thicker than the depletion region of the device, it corresponds to a partial depleted transistor; in this case, there is some portion of the body whose charge can be modified during its operation. This charge, whose origin can be associated with the absence of the body polarization, gives rise to some problems such as history and kink effects [4], that are explained later. On the other hand, when the silicon layer is thinner than the depleted depth, typically about 100 nm or less, all the body is completely depleted and its charge can not be changed with its operation; so, there are a large number of undesired effects that are avoided. However, due to the very low thickness of the silicon layer, it has a significant variation over the wafer, which results in a variation in the threshold voltage. For that reason, the fabrication process of fully depleted devices become very difficult and expensive [3].

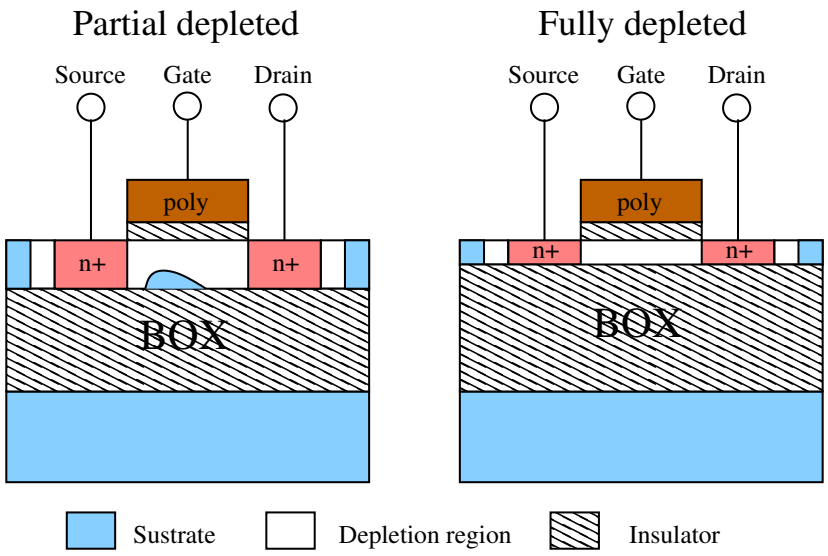


Figure 1.7: Partial depleted Vs Fully depleted transistors.

1.2.1 SOI devices Vs Bulk devices

Besides its structure, there are some important differences between SOI and bulk devices that are going to be explained bellow:

Doping density and leakage

In the traditional bulk technology, due to the scaling of the channel length, it is necessary to increase the concentration of the channel in order to reduce the length of the depletion region of the *pn* junctions and avoid a direct current path between drain and source. However, this increase reduce the mobility of channel and thus the current drive capability of the device. To compensate this loss, the thickness of the gate oxide is reduced so that the gate capacitance is increased. Nevertheless, a reduction in the oxide thickness causes an increment in the gate leakage current and channel coupling. For that reason, it is crucial the use of another dielectric with higher permittivity that allows a larger thickness.

For a partially depleted device, there is some portion of undepleted body by which the channel coupling can occur. Therefore, in the same way as in bulk technology, this is countered by increasing the doping concentration and reduce the dielectric oxide, but in a lower extent. For that reason, partial depleted transistors have a lower leakage and coupling with respect to bulk transistors; also, the mobility of the channel is higher which is favorable for current drive capability. In the case of fully depleted devices, due to their completely depleted body, there is no way to form a direct current path between drain and source, thus doping concentration can be decreased and thicker oxides could be used; consequently, gate leakage is reduced dramatically. In addition, because of the dimensions of the body in a partial depleted transistor are lower than in a bulk one, the leakage of the *pn* junctions is reduced.

Finally, it is common to assume that SOI transistors have around 40% to 90% of less leakage than bulk ones. Moreover, in nanometer technologies leakage is dominated by the subthreshold and *pn* junctions currents, instead of the induced by the gate [3].

Parasitic capacitance reduction

As it was mentioned before, the SOI transistors *pn* junctions have lower areas, thus their diffusion capacitances are reduced; this contributes considerably to the increment of the unit-gain frequency of the device and the operation speed of the circuit. Also, due to the use of a thicker oxide, the gate capacitance is also reduced. It follows that, in general, SOI transistors have parasitic capacitances about four to seven times smaller than bulk devices. For that reason, some authors mention that SOI technology is one generation ahead of the bulk technology, in terms of device speed [5]. It is important to note that the speed is maximum with the use of fully depleted transistors, because the reduction in the gate capacitance caused by the absence of undepleted body [3].

Latch-up reduction

In SOI transistors, due to their condition of floating body, the positive feedback configuration of the two parasitic bipolar transistors, needed to cause latch-up, will never be reached. For that reason, SOI technology is latch-up free. This is because the NMOS and PMOS devices are always separated by a buried oxide layer, which makes impossible the physic contact of the two bipolar devices. In addition, because of this latch-up immunity, the minimum allowed distance between different transistors, which is defined only by the constrains in the minimum width of the buried oxide, is much lower than in a bulk technology. Therefore, with the same minimum channel length, it is possible to achieve a higher integration density with SOI technology than with bulk CMOS [4, 5].

Reduced short channel effects

Short channel effects refer mainly to the variation of the threshold voltage with the length of the transistor; typically, the shorter the channel, the smaller the threshold. This variation is reduced strongly with the use of SOI technology, because of the small amount of charge than could be modified in the floating body, specially in fully depleted devices. The charge contained in the undepleted region defines the potential of the body, therefore the threshold voltage; also, as was explained before, this region is very small compared with the conventional body of bulk technology. So, there is a very lower amount of charge free charge, thus a reduced threshold variability. Figure 1.8 shows a comparison of the changes with channel length of SOI and bulk devices, where a considerable difference could be seen [5].

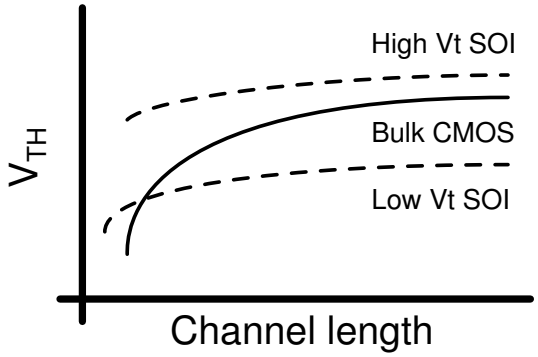


Figure 1.8: Variation of the threshold voltage of SOI and bulk devices

1.2.2 Floating body effects

A floating body has some benefits like the latch-up immunity and the reduction of the threshold voltage variation. Nevertheless, the floating condition leads to some undesired effects as will be explained next:

History effect

Despite the floating condition of the body in SOI transistors is beneficial for the reduction of the variation of the threshold voltage with channel length, the charge that could be changed in the undepleted region introduce some degree of variability with respect to the dynamic operation of the device. It means that the threshold voltage has a dependence of the previous state of the transistor [3]. This effect is known as history effect.

The causes of history effect can be explained as follows: the charge contained in the body is function of diode leakage, gate-to-body tunneling, slew rate of the gate signal, drain and source potentials, temperature, etc. If the charge produced by any of this sources tends to accumulate in the undepleted region, because its limited recombination constant and the lack of polarization. Hence, this accumulation modify the body potential and thereby the threshold voltage. This has enormous effects in dynamic circuits such as digital gates, because their delay is strongly modified [5].

It is important to note that history effect has a high relevance in partially depleted devices, because, in a well controlled process, the fully depleted devices do not have any undepleted region, thus there is no way to accumulate charge.

Self-heating effect

In a bulk transistor, most of the heat generated by its own operation is transferred to the substrate, and only a little part is transferred to the neighboring devices. But, in SOI technology, due to the low thermal conductivity of the oxide layer (around 100 times lower than

silicon substrate), most of the generated heat remains in the device and is transmitted to the others; this of course increases the temperature of all the transistors in the chip, specially those that are near to high frequency and high power consumption devices [3, 4].

An important consequence of this effect is the fact that an increase in temperature causes a decrease in the mobility of the channel, so the current capability is decreased too, and thus the drain current; a variation of 20% to 25% of that could be produced. In addition, self-heating effect has a time constant of some microseconds, for that reason, it has a lower importance in fast switching circuits than in slow ones, because those will be in thermal equilibrium.

Elevated DIBL

Drain Induced Barrier Lowering - DIBL its known as an increase in the subthreshold due to high drain to source electric field, wherefore the potential barrier lowers and charge carriers could cross the channel easier. This is a description proper to bulk devices, but, in SOI technology, the increase of subthreshold leakage is due another effect. With high drain potential, the leakage of the *pn* junction becomes higher too, so, there is more charge injected to the floating body by which its potential rises; finally, a higher body potential cause a decrement in the threshold voltage, therefore an increment in leakage [5].

1.2.3 IBM 45 nm SOI-CMOS technology

Characteristics

As was said before, the technology wherein the PLL will be implemented is IBM 45 nm Silicon On Insulator CMOS, specifically the SOI12S0 fabrication process. Some of its characteristics are listed below [2]:

- Minimum lithographic resolution of 40 nm.
- Seventeen different metal layers with four different thickness.
- Floating body and body contact devices. It means the availability of transistors that have a way to biasing its body and thus with similar characteristic to bulk CMOS technology.
- Fifty six different types of transistor divided as follow:
  - Five different threshold voltage in floating body devices.
  - Seven different oxide thickness in both floating body and body contact devices.
  - Eight different transistor optimized for SRAM memory cells.
- Seven capacitors including a varactor, and two resistors.
- Two types of inductors including central tap type.

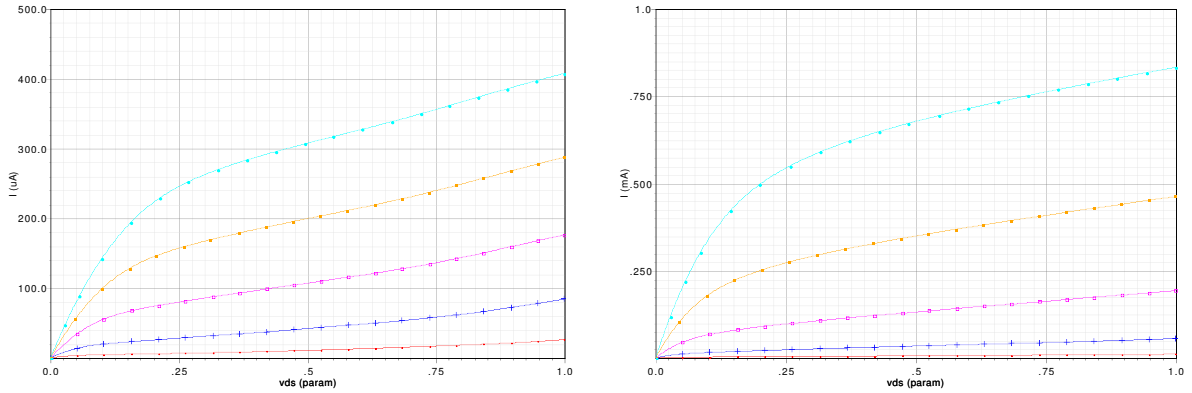
- Nominal supply voltage of 1 V.

Models restrictions

A very important characteristic of this technology is the strong restriction in the channel length of the devices. It means that the models provided by the foundry are valid exclusively for one length. For example, the model of all the transistors with thin oxide is valid only for the minimum channel length (40 nm); for transistors with body contact is valid for three different dimension (56 nm, 112 nm and 256 nm); and for transistors with tick oxide is valid for four lengths (232 nm, 412 nm, 1000 nm and 2000 nm). In addition, there are some restrictions in their width, whereby the models are optimized for $w = 400\,\text{nm}$; all the constrains can be found in the reference manual given by the foundry [2].

These restrictions involves several challenges in the design of any analog circuit; one of them is the low output resistance due to the increased channel modulation effect. As an instance, figure 1.9 shows the I_{ds} Vs V_{ds} curves of a floating body and body contact transistor with $L = 40 - 56\,\text{nm}$. A change of of 100% and 70% in the drain current of a 40 nm and 56 nm transistor respectively can be seen, for a change of 500 mV in the V_{DS} voltage and when the devices are in saturation; this implies a output resistances less than 15 kΩ. For that reason, achieving high or moderate gain is complicated, hence the performance of feedback systems such as a PLL is very degraded.

In addition, transistors with nanometer dimensions are much more sensitive to process variations than those ones with micrometer dimensions, specially in inter-device variations (mismatch) like in the channel length. A rule of thumb to decrease the impact of mismatch is to make as big as could be possible both length and width. But, due to the geometry restrictions mentioned before, this rule does not have any validity in this technology. For that reason, the design of robust circuits in nanometer technologies is a bigger challenge than with



(a) Floating body transistor

(b) Body contact transistor

Figure 1.9: Drain current Vs Drain-Source voltage in SOI transistors

CMOS traditional ones.

Finally, a traditional design methodology involves the extraction of some parameters such as threshold voltage, modulation channel factor, intrinsic gain, saturation velocity, and others that level 1 or 3 MOSFET model includes; hence, some hand calculations can be made with the aim of finding the dimensions of each device based, for instance, on a small signal analysis. However, due to the mentioned restrictions on the length and width of the transistors, narrow and short channel effects as well as floating body potential makes cumbersome the formulation of a model which allows hand calculations.

1.3 Summary

In this chapter the causes of PVT variations were explained, as well as their impact in the analog design. A voltage amplifier —a very common analog circuit— was used to show the importance of considering all these kind of variations in the traditional design flow. Moreover, the Silicon on Insulator technology was described, including some of its advantages and disadvantages in both digital and analog design. Threshold voltage variability, latch-up, leakage and parasitic capacitances are some of the non-ideal effects that are reduced. However, the floating body characteristic introduces some non-desired effects such as history or memory of the threshold voltage, self heating, high DIBL and others, which could degrade the performance of both analog and digital circuits. Finally, a description of the IBM SOI-CMOS 45 nm technology, which is the one used to design the PLL, was presented, highlighting its restrictions on the dimensions of the transistors.

In the next chapter the main ideas about the behavior of a PLL will be presented. Also, the impact of PVT variations on each component of the system will be explained too. This is done with the purpose to identify some key aspects for a design methodology of robust PLLs.

CHAPTER 2

PLL BASICS AND ITS PERFORMANCE UNDER PVT VARIATIONS

As was mentioned in the previous chapter, a PLL is a system whose main function is to provide an accurate timing and stability signal based on a reference one. However, despite it is a feedback system, its performance is strongly affected by PVT variations.

Accordingly, in order to identify the components of a PLL that are affected by PVT variations in most, this chapter the basics of a PLL are presented as well as the changes on its performance due to PVT variations; this includes the operating principle, types of implementation, principal specifications and performance metrics, etc. Moreover, at the end of the chapter the state of the art in PVT compensated PLL is presented, with the propose to explain some of the techniques used nowadays.

2.1 PLL fundamentals

Generally, a PLL is a circuit that causes a particular system to track with another one. More precisely, it synchronizes in phase as well as in frequency an output signal, generally given by an oscillator, with a reference; when the two signals are synchronized —called the locked state— the phase error between those is zero or constant. If the phase error rises, a control mechanism acts on the oscillator so that the phase error is again reduced to the minimum. Besides, in such a control system, the phase of the output is locked to the phase of the reference, for that reason is called a Phase-Locked Loop [6].

Despite the kind of implementation of the PLL —which could be built by analog, mixed signal or all digital circuits, or by a computer software— its operating principle could be explained by the same basic model; this consists of a voltage controlled oscillator (VCO), a

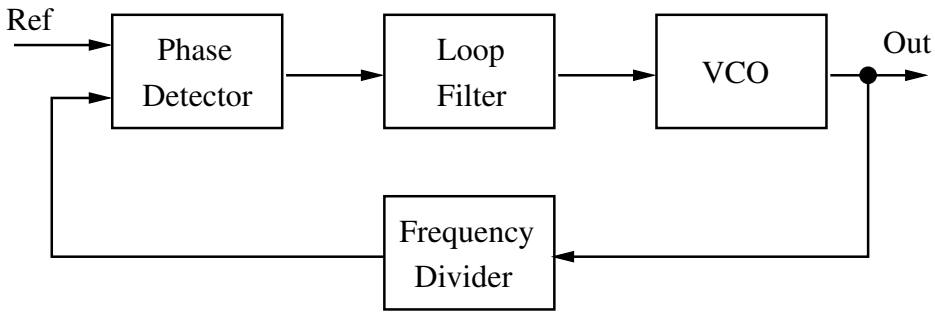


Figure 2.1: Basic model of a PLL

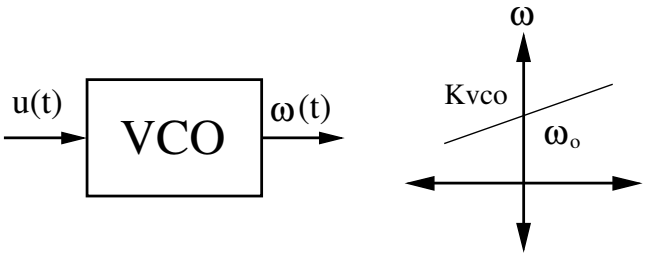


Figure 2.2: Ideal VCO tuning curve

phase detector (PD), a loop filter (LF), and a frequency divider, as is shown in figure 2.1.

The VCO oscillates at an angular frequency ω_2, which is determined by the output signal of the loop filter $u_f(t)$. Furthermore, the tuning curve of the VCO has a linear behavior (figure 2.2), and can be modeled by the following expression:

$$\omega_2(t) = \omega_0 + K_{VCO} \times u_f \tag{2.1}$$

where ω_0 is the central or free running frequency of the VCO and K_{VCO} rad/Vs is its gain.

The PD —also referred as a phase comparator— senses the phases of its two input signals and generates an output signal $u_d(t)$ in function of their phase difference $\Delta\phi$. Ideally, the relationship between the phase error and the output voltage is linear (figure 2.3), and defined by:

$$u_d(t) = K_{PD} \times \Delta\phi \tag{2.2}$$

where K_{PD} is the gain of the phase detector expressed in V/rad. The output of $u_d(t)$ is generally a DC component with a superimposed AC component. This AC component is an undesired signal that should be canceled by the loop filter.

The frequency divider (FD) downgrades the frequency of the frequency of the VCO output by a integer —M— or fractional —N— factor:

$$\omega_{out} = \frac{\omega_{in}}{N, M} \tag{2.3}$$

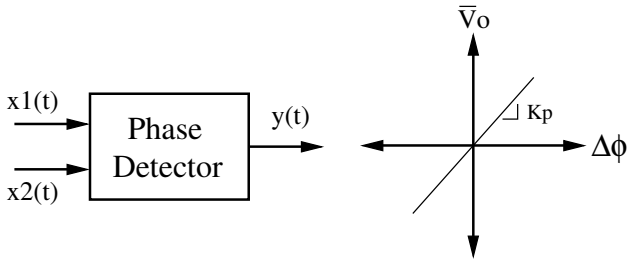


Figure 2.3: Ideal Phase Detector

In an ideal FD, its output waveform is the same as the VCO signal; also, it does not introduce any delay by which the VCO and reference could have some phase offset [7].

Assuming that the frequency of the input signal $u_r(t)$ is ω_0 and the division factor of the FD is one, then the VCO will oscillate at its central frequency. For that reason, the phase error and hence the output of the loop filter must be zero. Therefore, the oscillator remains in steady state oscillating at ω_0.

If the phase error were not zero initially, which means that the frequency of the VCO is different to the reference, the PD would develop a nonzero output signal. So, after some time delay, the loop filter would also produce a finite output that causes a change in the VCO operating frequency, and in such a way that the phase error tends to be zero or the minimum possible.

Now, assuming that the PLL is established in a initial frequency ω_1 and the reference frequency changes suddenly at time t_0 by an amount $\Delta\omega$, a transient behavior begins with the purpose of adjust the frequency of the oscillator. As figure 2.4 shows, the input signal starts leading the output, giving rise to a phase error that increases with time. Furthermore, the phase detector generates a signal which also increases with time; in the same manner, after some time delay given by the loop filter, $u_f(t)$ also rises. This causes that the VCO increase its frequency so that the phase error becomes smaller, and after some settling time, the VCO will oscillate at the same frequency that the input signal. Depending on the type of the loop filter, the final phase error could be zero or a constant finite value [6].

2.2 Building blocks of a PLL

In this section some ideas and characteristics about the building blocks mentioned in the last section are presented, as well as some types of implementation.

2.2.1 Phase detector

There are different types of implementations whereby a phase detector can be built; some of them are described below.

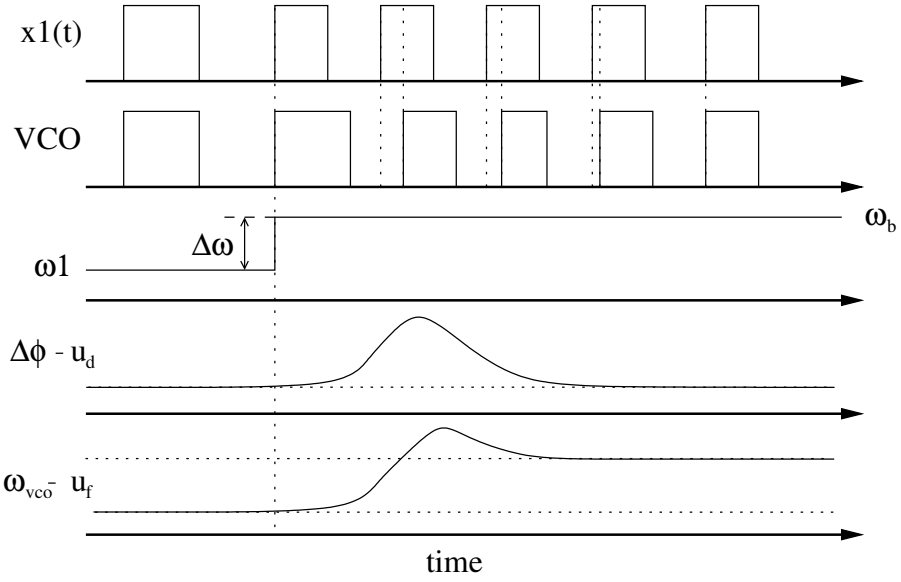


Figure 2.4: Dynamics of a PLL at a frequency change

Analog multiplier

Phase difference detection could be done by an analog multiplier. Consider two sinusoidal signals $x_a(t) = A_1 \sin(\omega_1 t + \phi_1)$ and $x_b(t) = A_2 \cos(\omega_2 + \phi_2)$, whose product is:

$$\begin{aligned} V_{out} &= K \times x_a(t) \times x_b(t) = K A_1 A_2 \sin(\omega_1 t + \phi_1) \cos(\omega_2 + \phi_2) \\ &= \tfrac{K A_1 A_2}{2} \sin(\omega_1 t + \phi_1 - \omega_2 t - \phi_2) + \tfrac{K A_1 A_2}{2} \sin(\omega_1 t + \phi_1 + \omega_2 t + \phi_2) \end{aligned} \tag{2.4}$$

if the frequency of the two signals is the same $\omega_1 = \omega_2$, the equation (2.4) could be rewritten as follows:

$$\begin{aligned} V_{out} &= \tfrac{K A_1 A_2}{2} \sin(\phi_1 - \phi_2) + \tfrac{K A_1 A_2}{2} \sin(2\omega_1 t + \phi_1 + \phi_2) \\ &= \tfrac{K A_1 A_2}{2} \sin(\Delta\phi) + \tfrac{K A_1 A_2}{2} \sin(2\omega_1 t + \phi_1 + \phi_2) \end{aligned} \tag{2.5}$$

The equation (2.5) shows that the output voltage has two components: a constant term that is function of the phase difference $\Delta\phi$, and a sinusoidal wave whose frequency it twice as the input. So, if a low-pass filter is used after the multiplier, the high frequency component could be removed and the DC component is used to obtain information about the phase error.

An important characteristic of this detector is the nonlinear relationship between phase and voltage; linear behavior is obtained for small phase differences only. Also, the frequency of the input signals must be the same with the aim to produce a DC component, for that reason this circuit only can sense phase and not frequency. In addition, the maximum detectable phase difference is $\frac{\pi}{2}$ because of the periodic voltage vs phase behavior [6].

Logic gates: XOR

In nanometer technologies, where supply voltage is reduced dramatically but the noise level of the devices not, it is very important to use signals with the large dynamic range near to V_{DD}. For that reason, logic gates are used as phase detectors, specially the XOR one, as will be explained in the following lines.

Figure 2.5 shows the waveforms of two square signals with different frequencies that are applied to a XOR gate, as well as the output waveform; the propose of the frequency difference is to generate several phases errors. When the states of the two signals are the same, the output is a low state, on the other hand when the inputs are different, the output is a high level. The phase difference detection is made as follows: if the two signals were in phase, there were no difference between their states at any time, thus the output will be always low; on the contrary, if any phase difference exists, there will be some time intervals in which the two signal have different logic levels and the output will be at high logic state. An important issue is that the higher the phase difference, the wider the high state pulses, so that a pulse-width modulated wave is obtained. For that reason, a low-pass filter must be following the gate with the intention that extract the DC component [7].

Another issue in this type of phase detector is the linear relationship between phase and average output voltage. Nevertheless, it has a restricted phase error range, which is less than $\pi/2$. For that reason, a logic gate only can detect phase difference and do not frequency.

Phase and frequency detector: Finite State Machine —FMS—

The fact that a phase detector can only detect small phase errors imposes a restriction in the settling time of the PLL. This is due to the limited control action that would be produced. As an example, consider the start-up instant of the PLL; in his moment, the initial frequency of the oscillator is unknown and, generally, fairly distant of the reference. For that reason, high

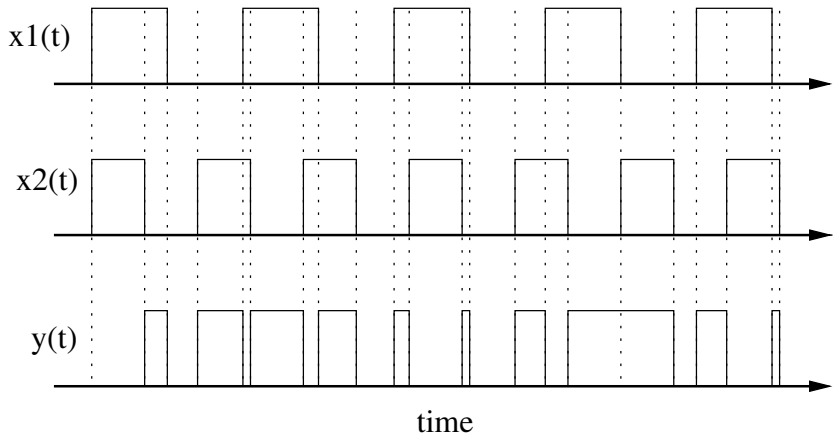


Figure 2.5: XOR based phase detector

phase errors are produced and the PD will saturate, so that a nonlinear behavior appears. For that reason, the settling time is different to the one in which the PD will not saturate i.e. only small frequency changes.

High phase difference range phase detectors —also known as Phase and Frequency Detectors— are typically implemented by finite state machines (figure 2.6), that consists of two D Flip-Flops and an AND gate as the reset path. The circuit works as follows: when a rising or falling edge of the reference signal reach the flip-flop —depending the type of flip-flop— the UP signal goes to a high level, and will remain in this state until another edge of the VCO signal arrives. At this moment, the DOWN signal goes to high state and the AND gate output too. Then, the two flip-flops are reset so that UP and DOWN go low. It is important to note that no matter how many edges of the reference signal reach the flip-flop, the UP output will stay high until a edge of the other signal arrives; for that reason, the phase error range of this PD is much greater than the logic gates and multipliers have, and is independent of the frequency of the signals.

Another characteristic of the FSM is that it is built based on digital gates, therefore the dynamic range goes from ground to the power supply, and similar to XOR gates, it needs a low pass filter to extract the DC component of the output.

The main drawback of this circuits is the fact that the information about phase error is contained in two signals —UP and DOWN—, leading to the requirement of an extra circuity so as to subtract them and extract the mean value. This function is generally done by a Charge Pump, which is explained in the next section. This extra component introduce both desired and undesired effects like a pole in the origin and nonlinear behavior [6].

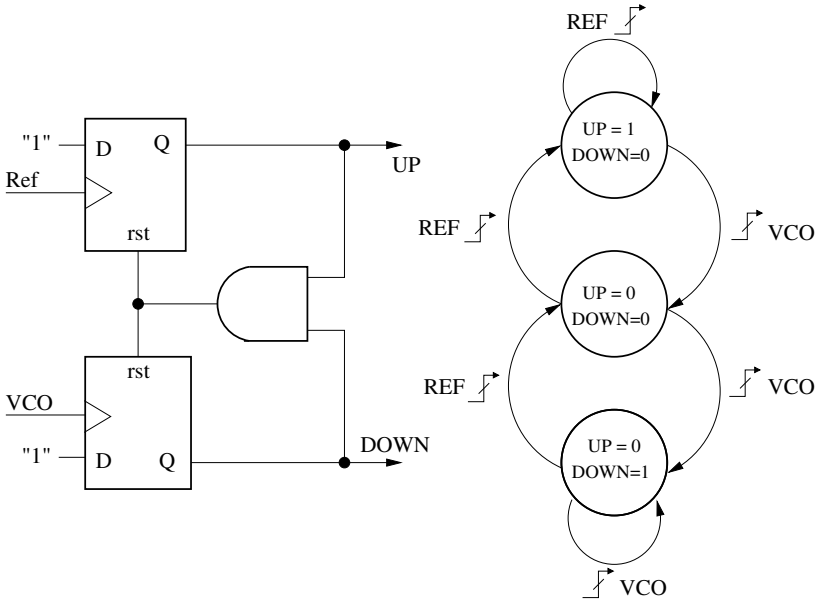


Figure 2.6: Finite State Machine based phase detector

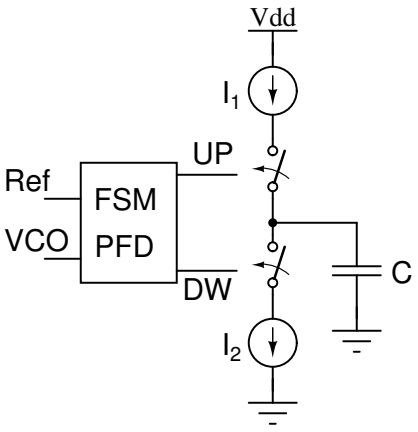


Figure 2.7: Charge Pump structure

2.2.2 Charge Pump

A charge pump (CP) consists of two switched current sources that drive the loop filter; figure 2.7 shows the structure of a CP when the loop filter is a capacitor only. The switching activity is controlled by the UP and DOWN signals from the phase detector. The main function of a CP is to control the voltage of the capacitor by controlling the amount of current injected to it. If the reference signal leads the VCO signal, the UP signal goes high and the current source I_1 drive its current into the capacitor, so that its voltage increases; when the VCO edge appear, DOWN goes high too and I_2 is turned on. Because of $I_1 = I_2$ zero current will be driven into the capacitor when both sources are on, thus its voltage will remain constant. The opposite occurs when the VCO signal leads the reference; in this case, the DOWN signal goes high first, thus the source I_2 discharge the capacitor, and when UP goes high, the voltage of the capacitor remains constant. As an instance, figure 2.8 shows the output voltage of a charge pump for two signals with different phase.

One way to build a charge pump is to use simple or cascode current mirrors in addition with two switches, and a single ended or fully differential structure. This imposes some restrictions in the dynamic range of its output voltage and nonlinearity due the finite on and off time of the switches. Also, any difference between the current of the two sources introduces a phase error in the locked state; this differences could be due to devices mismatch in the current mirrors and different output resistance between NMOS and PMOS transistors, thus an extra circuitry is required to control these two currents [7].

2.2.3 Loop Filter

The loop filter of a PLL consists of a lag-lead network which could be active or passive. Its main function is to set the frequency response, and therefore the transient one, of the whole system. Stability, settling time and phase noise are some of the parameters that can be

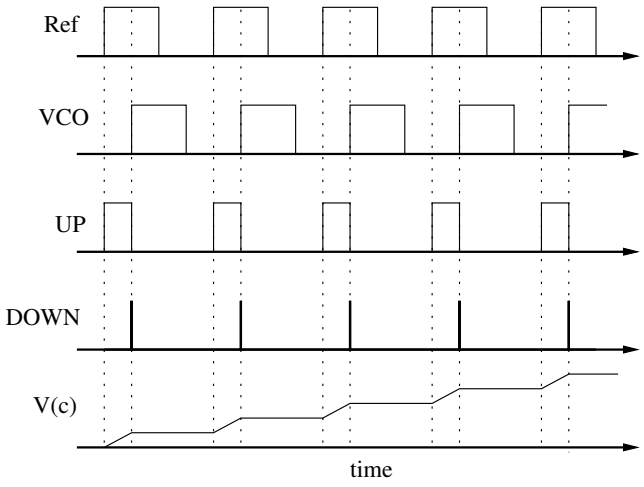


Figure 2.8: Charge pump behavior

modified by the poles and zeros locations of the loop filter. In PLLs without charge pump, the loop filter is also used to extract the DC component of the phase detector output signal. For that reason its characteristic corresponds to a low-pass circuit. Furthermore, some glitches due the finite on time of the switches, which produce frequency spurs, could also be removed [8].

Figure 2.9 shows some implementations of loop filters and figure 2.10 shows their frequency response. The first filter corresponds to a passive one, whose transfer function is:

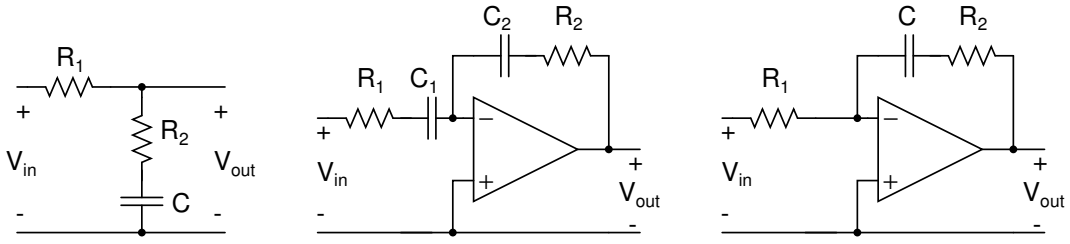
$$H(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \qquad \tau_1 = R_1 C \qquad \tau_2 = R_2 C \tag{2.6}$$

This filter is a lag-lead network because the action of its pole comes first, thus a lag in the control signal phase is produced at low frequencies.

The second filter is an active network, whose transfer function is:

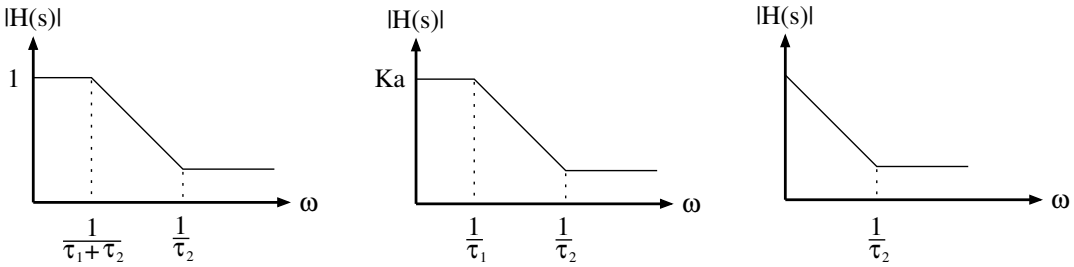
$$H(s) = K_a \frac{1 + s\tau_2}{1 + s\tau_1} \qquad \tau_1 = R_1 C_1 \qquad \tau_2 = R_2 C_2 \qquad K_a = C_1/C_2 \tag{2.7}$$

Its transfer function is very similar to the passive filter, but has an additional low frequency



(a) Passive loop filter (b) Active loop filter (c) Active PI loop filter

Figure 2.9: Different kind of implementations of loop filters



(a) Passive loop filter (b) Active loop filter (c) Active PI loop filter

Figure 2.10: Bode plots for loops filters

gain K_a which can be fixed to a value greater than one.

The third filter is an active PI loop filter because it has a proportional and integral path; its transfer function is:

$$H(s) = \frac{1 + s\tau_2}{s\tau_1} \qquad \tau_1 = R_1 C \qquad \tau_2 = R_2 C \tag{2.8}$$

Other more complex loop filter structures are build based on the above filters, and correspond to second and third order networks. The use of these filters is given by the desired purity of the output oscillation: the higher the order of the filter, the higher the suppression of noise in some bandwidth. In some cases, due to the complexity of the noise models of each device, the filter should be selected based on simulations [6].

2.2.4 Voltage Controlled Oscillator

There are three types of controlled oscillators: voltage controlled, current controlled oscillators and digitally controlled oscillators, and as their names indicates, their difference lies in the type of control (a voltage, a current or a digital word).

As was explained before, in an ideal controlled oscillator its frequency varies linearly in function of a voltage or a current and around a central frequency. However, in any oscillator, there are some non-idealities such as non-linear frequency variation, hysteresis and saturation which degrade the purity of the oscillation.

In addition, there are several ways to make a circuit oscillates; most of them are based on resonance and positive feedback. Nevertheless, LC tank based oscillator and Ring oscillator are the most used. Some ideas about their behavior are listed below.

LC tank oscillator

A LC tank oscillator consist of a Inductor-Capacitor network in which the energy stored in any of the two elements —such as produced by noise— will circulate between them, producing an oscillation at the resonant frequency ω_0:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.9}$$

In the ideal case, the oscillation will remain because there is no way to dissipate the stored energy, so that it will recirculate indefinitely. However, due to the finite series resistance of an inductor, or the finite parallel conductance of a capacitor, there will be some mechanism to dissipate the energy. For that reason, an extra circuit to compensate this loss is required [7].

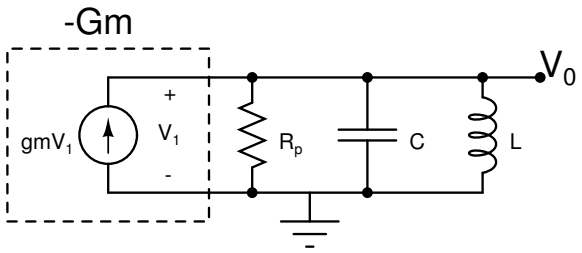


Figure 2.11: Parallel RLC equivalent circuit of a LC tank oscillator

Figure 2.11 illustrate the RLC parallel equivalent circuit of an LC tank oscillator, and the compensation mechanism denoted as $-Gm$. The goal is to emulate the behavior of a negative resistance or conductance so that the parasitic element will be canceled. This could be done using active devices such as transistors, and figure 2.12 shows a implementation known as a cross coupled pair.

A very common method to control the oscillation frequency is to vary the capacitance of the tank by changing the DC voltage of a varactor (which corresponds to a *pn* junction in inverse bias). It is important to note that, although the varactor was an ideal component with a linear relationship between capacitance and voltage, the oscillator would not have a linear behavior because the frequency is a inverse square-root function of the capacitance. Nonetheless, there have been developed some linearization techniques which includes the control of the current of the maximum current of the circuit.

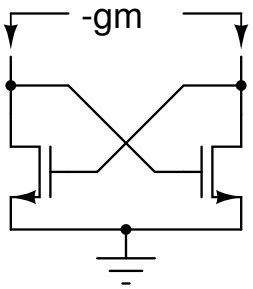


Figure 2.12: Implementation of $-Gm$ by a cross coupled pair

Ring oscillator

Is composed by a chain of delays inverter cells in which its output is connected directly to the input, wherefore a positive feedback configuration is reached (figure 2.13). An oscillation is achieved because there is the sufficient delay along the chain, so that the phase shift of a signal crossing the chain is greater than 180°. Accordingly, the frequency of the ring is given by the following expression:

$$f_o = \frac{1}{2NT_D} \tag{2.10}$$

with N the number of stages and T_D the delay of only one. In single ended implementations there must be an odd number of delay cells because otherwise the total phase shift would be 360° or any multiple of it; thus the ring would a latch instead an oscillator. Nevertheless, in differential implementations there is no restriction in the number of stages because it is possible to configure one stage such that it does not invert.

The delays cells could be implemented by linear one-pole stages such as the common-source configuration or a differential pair (figure 2.14), or by non linear stages like the digital inverter (figure 2.15). The main difference between those is the amplitude and waveform of the oscillation. In a ring with linear cells the output amplitude has to be kept low, so that the small signal analysis remains valid; for that reason, the oscillation contains less harmonic content and is similar to a sine wave. On the contrary, when digital inverters are used, the output amplitude can reach the power supply levels due to the high dynamic range of the cell; also, the harmonic content is greater than in the linear case, because the waveform tends to be square [8].

As was described, the frequency of the ring can be adjusted by changing the number of stages in the chain or by modifying the delay of each one. The first alternative involves a change in the structure of the circuit with the connection of one or more stage to the chain; thus only a discrete and limited range of frequency is achieved; also, this would not be compatible with the PLL architecture explained before. On the other hand, the delay of a cell can be modified by the change of a bias current, or the control the ON resistance of a transistor; with this method a continuous and wide tuning range is reached, giving the possibility to make a control by the loop filter.

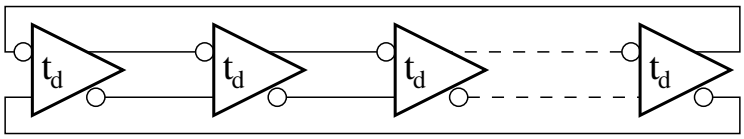


Figure 2.13: General structure of a ring oscillator

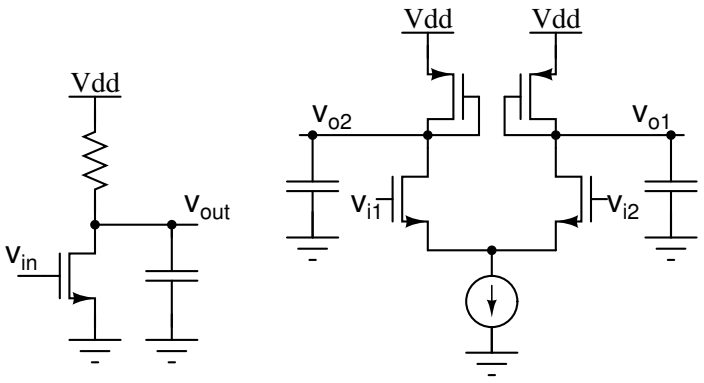


Figure 2.14: Linear delay cells

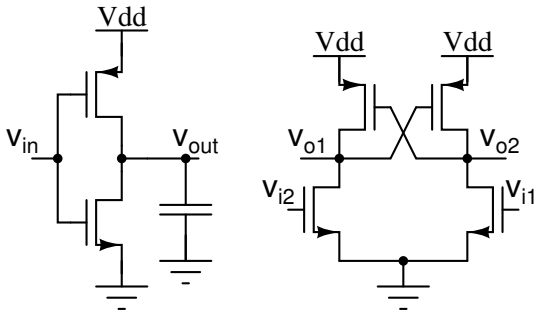


Figure 2.15: Digital inverter delay cells

2.3 PLL Performance

If a PLL is in the locked state it is possible to develop a linear mathematical model for the whole system. Therefore, the behavior of the circuit to changes in the frequency or phase of the reference signal, as well as changes in the division factor of the frequency divider, can be predicted. The model corresponds to a transfer function which relates the phase of the output signal with the phase of the input signal:

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} \tag{2.11}$$

Here $\Theta_1(s)$ and $\Theta_o(s)$ are the Laplace transform of the input and output phase signal $\theta_i(t)$ and $\theta_o(t)$ respectively. For that reason, it is necessary to know the linear approximation of each component of the PLL.

2.3.1 Linear models

Phase detector

As was said before, a phase detector can be analyzed as a constant gain K_{PD} expressed in V/rad which amplifies the phase difference between its inputs, as figure 2.3 shows. It produces

the error signal if the PLL is seem as a feedback control system. Also, the PD gain is related to the maximum average voltage that could be generated from the subtraction of the UP and DOWN signals, and correspond to a half of the power supply [6].

Charge pump

A charge pump can be modeled as a constant gain K_{CP} that relates the mean output voltage of the phase detector with the output current of the pump. This gain corresponds to the current of the sources [6].

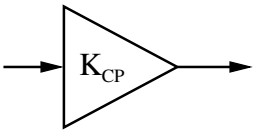


Figure 2.16: Linear model of a charge pump

Loop filter

The linear model of the loop filter is the same as the one explained in the last section. In some cases, the load of the charge pump is not only a capacitor, but the loop filter. For that reason, the transfer function of this component relates a current input with a voltage output.

Voltage controlled oscillator

A controlled oscillator could be represented as a constant gain K_{VCO} rad/V. Nevertheless, this gain relates a frequency with a control voltage, wherefore it is necessary to transform a frequency signal to a phase one; this is done by including a continuous integrator after the gain block, as is shown in figure 2.17 [6].

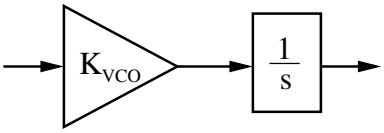


Figure 2.17: Linear model of a VCO

Frequency divider

The linear model of a frequency divider is a constant gain which corresponds to the division factor N. Because it divides the frequency of the VCO, it also scales down the phase [6].

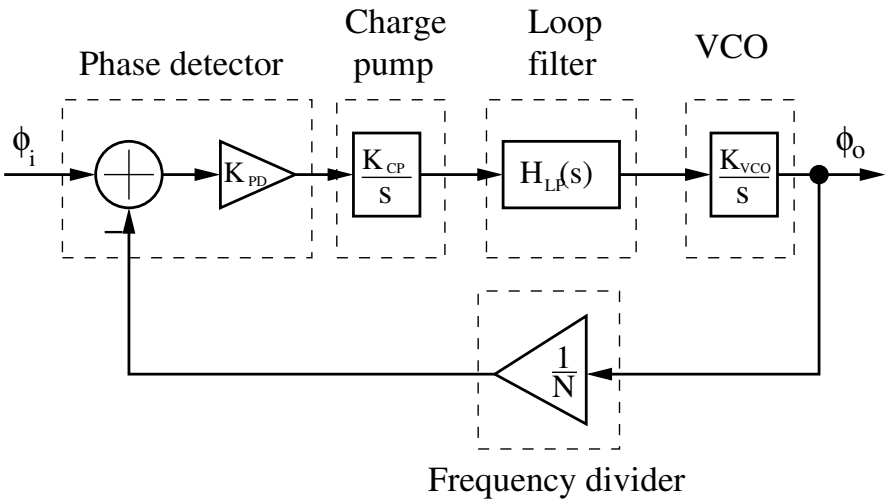


Figure 2.18: Linear model of whole the PLL

2.3.2 Transfer function

The previous linear models lead to construct the diagram of figure 2.18 which represents all the PLL. Supposing that the loop filter is a RC series network that serves as load for the charge pump, the overall phase transfer function is:

$$\begin{aligned} H(s) &= \frac{H(s)_{PD}H(s)_{CP}H(s)_{VCO}}{1+\frac{H(s)_{PD}H(s)_{CP}H(s)_{VCO}}{N}} \\ &= \frac{K_{PD}K_{CP}K_{VCO}\frac{(1+sRC)}{s^2C}}{1+\frac{K_{PD}K_{VCO}K_{CP}}{N}\frac{(1+sRC)}{s^2C}} \\ &= \frac{K_{PD}K_{CP}K_{VCO}}{C} \times \frac{1+sCR}{s^2+\frac{K_{PD}K_{CP}K_{VCO}}{N}Rs+\frac{K_{PD}K_{CP}K_{VCO}}{NC}} \end{aligned} \tag{2.12}$$

The equation (2.12) represents a second order system which is characterized by a natural frequency ω_N, a damping factor ζ, and a stabilizing zero ω_z, as is described below [8]:

$$H(s) = N\omega_N^2\frac{(1+\frac{s}{\omega_z})}{s^2+2\omega_N\zeta s+\omega_N^2} = N\frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\omega_N\zeta s+\omega_N^2} \tag{2.13}$$

$$\omega_N = \sqrt{\frac{K_{PD}K_{CP}K_{VCO}}{NC}} \qquad \zeta = \sqrt{\frac{K_{PD}K_{CP}K_{VCO}}{NC}} \times \frac{RC}{2} = \frac{\omega_n RC}{2} \qquad \omega_z = \frac{1}{RC}$$

The term $K_{PD}K_{CP}K_{VCO}/N$ is called the *loop gain*. In addition, the error-transfer function $H_e(s)$, defined as the difference between the phase of the reference and feedback signals, corresponds to:

$$H_e(s) = 1 - H(s) = \frac{s^2}{s^2+2\zeta\omega_n+\omega_n^2} \tag{2.14}$$

It is important to note that high order PLL with more complex loop filters could be analyzed with a transfer function, as the same way as was done previously. However, the purpose of the use of a simple loop filter to built a second order system, is to identify the key aspects in the PLL performance, such as bandwidth, settling time and steady state error.

With the aim of get an idea about transient response of a PLL, some Bode plots of the

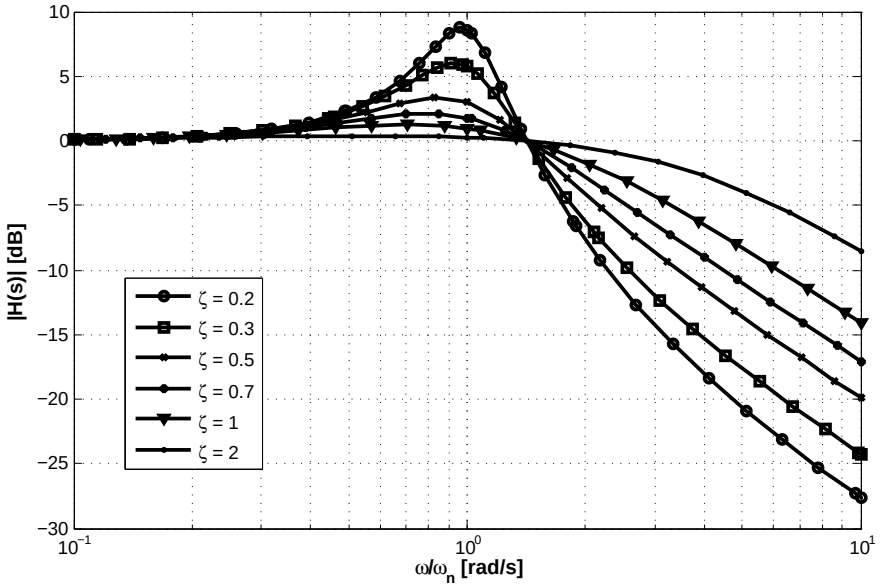


Figure 2.19: Frequency response of the phase transfer function of a second order PLL for different damping factors ζ

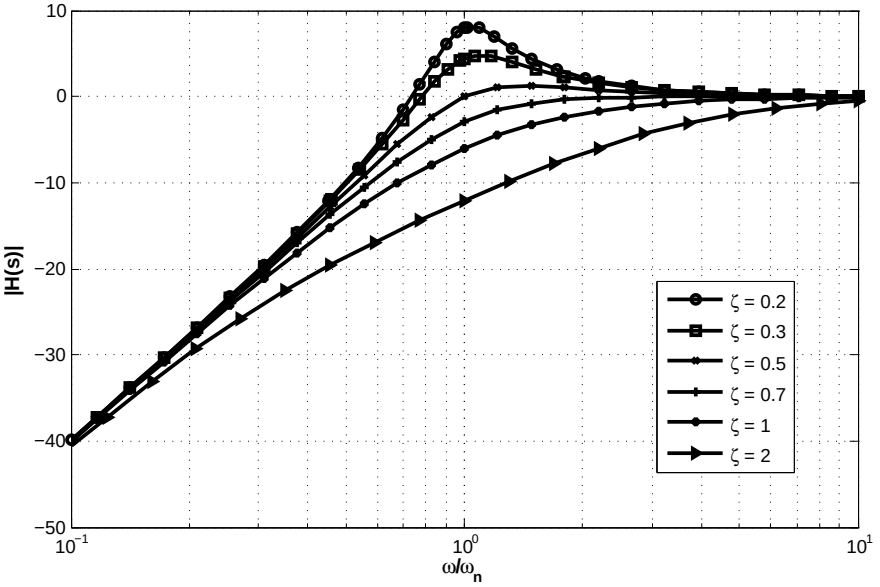


Figure 2.20: Frequency response of the error transfer function of second order PLL for different damping factors ζ

transfer function $H(s)$ and error-transfer function are presented in figures 2.19 and 2.20. From figure 2.19 it is concluded that a PLL is a low pass system whose frequency spectrum if flat between zero an approximately the natural frequency ω_n. This means that a second order PLL is able to track phase and frequency changes or modulations as long as those remain within zero and ω_n.

The damping factor ζ has an important influence in the dynamic performance of the PLL. For $\zeta = 1$ the system is critically damped. If ζ is made smaller than the unity, the transient response becomes oscillatory, so that the smaller the damping factor, the larger becomes the overshoot. On the other hand, damping factors considerably larger than unity make the transfer function flattens out and the dynamic response becomes sluggish. The transfer function is optimally flat for $\zeta = 1/\sqrt{2} \approx 0.707$, which corresponds to a second-order Butterworth low-pass filter.

In addition, from figure 2.20 similar conclusions can be made about the transient performance of a PLL. For slow frequencies changes or modulations in the input, the phase error remains relatively small. For frequencies greater than ω_n the phase error reach the reference phase, which means than the PLL is not able to follow that changes [6].

As in amplifiers, the bandwidth of a PLL is specified by the frequency in which the gain falls 3 dB below the flat band, called the corner frequency $\omega_{-3\,\mathrm{dB}}$. For a second order system, this could be calculated by the following expression:

$$\omega_{-3\,\mathrm{dB}} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{(1 + 2\zeta^2)^2 + 1}} \tag{2.15}$$

For example, if the damping factor is approximately 0.707, the $\omega_{-3\,\mathrm{dB}}$ becomes $2.06\omega_n$, which about twice the natural frequency.

Steady state error is another critical issue in the performance of a PLL. Due the pole in $s = 0$ given by the oscillator, a PLL by itself has a zero steady state error for step phase inputs, such as phase modulations. For that reason, the output phase will always track the input phase; figure 2.21 shows the transient response of the phase error for different damping factor for a phase step. But, when a frequency step is applied —the same as a phase ramp— there is a finite error wherefore the output frequency will not be the same as the input. Hence, another pole in $s = 0$ must be placed. This pole is given by the charge pump, and will make that both input and output frequencies will be the same. In addition, figure 2.22 shows also the transient response of the phase error, in which its finally value is always zero for a frequency step.

Finally, another point to stand out of the previous analysis is that if the PLL is in the unlocked state i.e. the frequency of the output and reference are distantly different, its behavior does not corresponds to a linear system. Thus, settling time and overshoot will differ from the explained before. For that reason, linear analysis could be done only when the PLL is in a previous locked state and small changes in frequency of the reference signal are made [8].

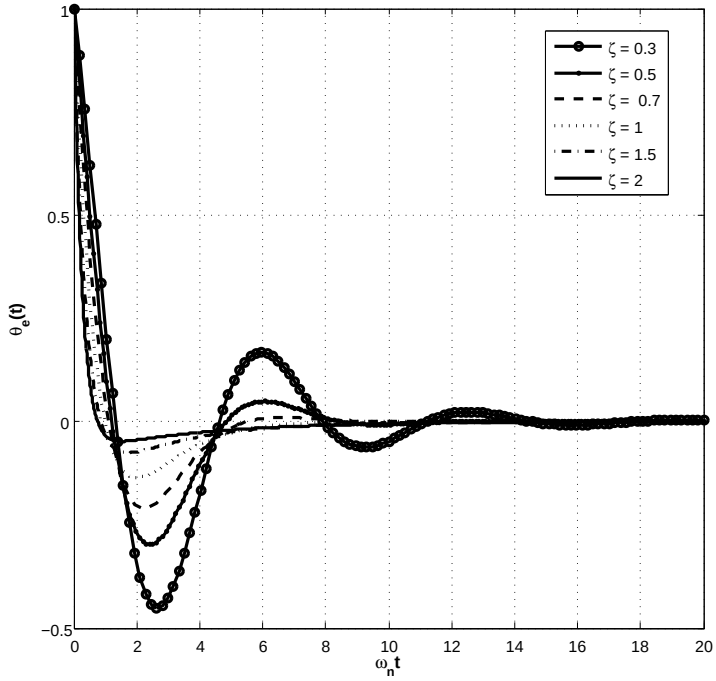


Figure 2.21: Transient response of the phase error for a step phase input

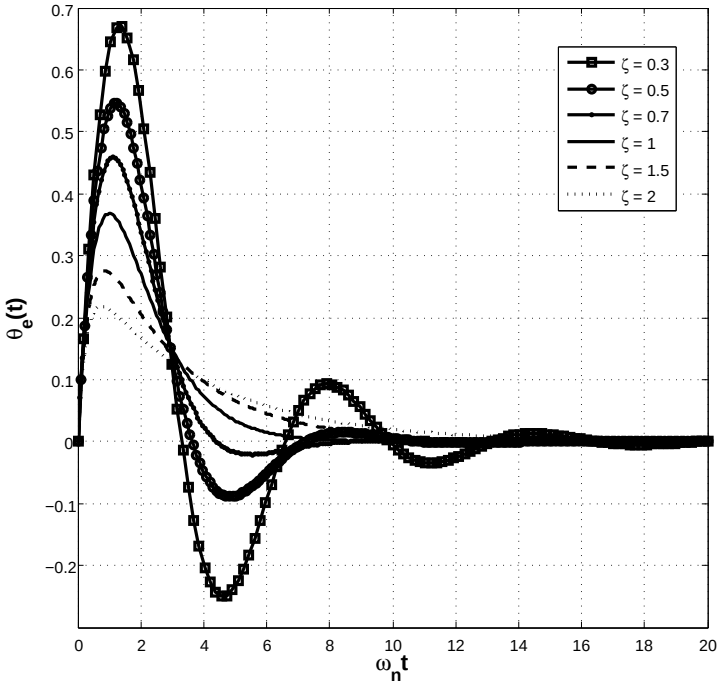


Figure 2.22: Transient response of the phase error for a step frequency input

2.3.3 Noise in a PLL

Phase Noise

First of all, it is important to explain the concept of phase noise. As another analog circuits, a PLL, specially the oscillator, is susceptible to electric noise. Noise injected into a PLL may influence both the amplitude and frequency of the output signal. In most of the cases, the disturbance in amplitude is not as important as in frequency and could be negligible. Thus, only the random deviation of the frequency is considered [7].

Supposing that a noise signal $n(t)$ is added to a carrier $v_c = A\sin(\omega_c t)$, and $|n(t)| \ll A$, the result can be expressed as:

$$\begin{aligned} V_c(t) + n(t) &= A\sin(\omega_c t) + x_n(t)\sin(\omega_c t + \phi_n(t)) \\ &\approx [A + x_n(t)]\sin(\omega_c t + \phi_n(t)) \approx A\sin(\omega_c t + \phi_n(t)) \end{aligned} \tag{2.16}$$

From equation (2.16) the function $\phi_n(t)$ is called *phase noise*, and represents small and random excess phase which produces variations in the period of the signal. Phase noise is caused by any noise source in the circuit such as passive devices, transistors, signal couplings, etc. If $|\phi_n(t)| \ll 1$ rad, then $v_n + n \approx A\cos(\omega_c t) - A\phi_n \sin(\omega_c t)$ so that the spectrum of $\phi_n(t)$ is translated to $\pm\omega_o$ [7].

In communication systems, phase noise is characterized in the frequency domain. For an ideal oscillator its spectrum must have the shape of an impulse $\delta(f)$ —or many of these separated by ω_c if the signal is not a sinusoidal wave—. But, for a real oscillator its spectrum exhibits some kind of skirts around the carrier, as figure 2.23 shows. To quantify the phase noise, the logarithmic Noise to Carrier Relation is used; this is calculated by the relation between the power of the spectrum in 1 Hz bandwidth at an offset $\Delta\omega$ with respect to the carrier frequency ω_c, and the power of the carrier.

$$\text{Phase Noise} = 10\log\left(\frac{P(\Delta\omega)|_{1\text{ Hz}}}{P_{\text{carrier}}}\right)\text{ dBc} \tag{2.17}$$

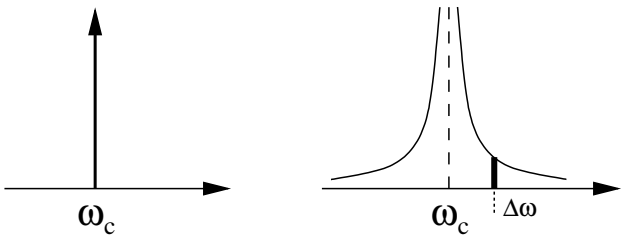


Figure 2.23: Spectrum of a phase noiseless and phase noisy carrier

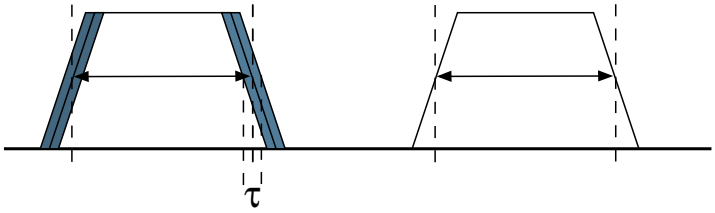


Figure 2.24: Presence of jitter in a square oscillation

Jitter

Another point of view to characterize the noise of a PLL is in the time domain. In an ideal oscillator the spacing between different transitions in constant. However, in real systems this spacing varies randomly; this variation is known as jitter (figure 2.24) [23]. Jitter is caused by any noise source in a oscillator, and is a direct consequence of phase noise. When a ring oscillator is implemented, it is more common to characterize its noise with jitter instead of phase noise because of its square waveform.

Noise sources in a PLL

There are many source of noise in the PLL, which includes noise from the reference signal, from the charge pump and loop filter, from the oscillator and from the frequency divider. Figure 2.25 shows the linear model of a PLL with the mentioned noise sources. For each one of them, it is possible to calculate a phase transfer function, and therefore the total output phase noise. Although that noise is a random voltage or current signal, it can be related to a phase variations and therefore include it in the phase to phase transfer function; thus, the linear analysis is valid.

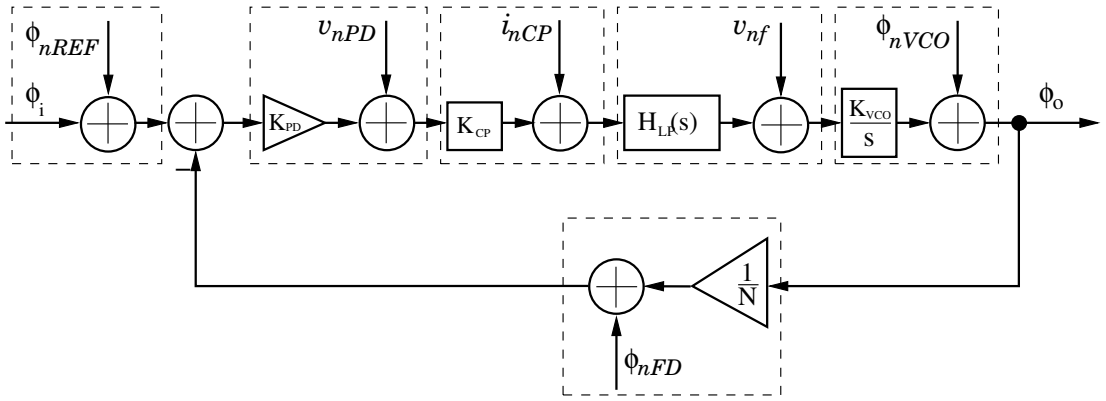


Figure 2.25: Noise sources in a PLL

Noise from the reference signal is filtered by the same transfer function of the PLL. Noise in the current of the charge pump and the frequency divider are also filtered by the same

function. But, noise from the loop is filtered by a pass-band transfer function because there is only one integrator (VCO) in the direct path between the source v_{nf} and the output:

$$H_{LF}(s) = \frac{K_{VCO}s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.18}$$

Furthermore, the noise from the VCO is high-pass filtered by the error transfer function, as shown in equation (2.14). Finally, equation the total output phase noise due to all the noise sources in a PLL corresponds to:

$$\begin{aligned} PN = \quad & (\phi_{nREF}^2 + \phi_{nFD}^2) \times \left(N \frac{\omega_n^2(1+\frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)^2 + v_{nPD}^2 \times \left(\frac{\frac{N\omega_N^2}{K_{PD}}(1+\frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)^2 \\ & + i_{nCP}^2 \times \left(\frac{\frac{N\omega_N^2}{K_{PD}K_{CP}}(1+\frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)^2 + v_{nLP}^2 \times \left(\frac{K_{VCO}s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)^2 \\ & + \phi_{nVCO}^2 \times \left(\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \right)^2 \end{aligned} \tag{2.19}$$

It is possible to note that there is a trade-off between the bandwidth of the PLL and the noise contribution of each block. A high bandwidth PLL will attenuate more noise from the VCO and will have a faster lock acquisition time, but will pass more noise from the reference, charge pump and frequency divider. On the other hand, a low bandwidth system will suppress high quantities of noise from the reference, but will pass more noise from the VCO and will have a lower lock acquisition time. The choose of the bandwidth of the PLL depends of the noise power of each block and the desired settling time for frequency changes: in some cases the VCO is the circuit that contributes more noise to the system, so that a fast PLL is desired; however, it the PLL has frequency dividers in both the reference and feedback signals and a low charge pump current, the most of the noise is at low frequency, wherefore a low bandwidth circuit is needed [8].

2.4 PLL performance under PVT variations

As it was shown in the last section, the natural frequency and damping factor of a PLL have a strong dependence of the gain of each block of the system, as well as the passive elements of the loop filter. Therefore, any change of these parameters, produced by PVT variations, modifies the settling time and the noise transfer function for each block of the system, degrading the spectral purity of the output signal. It is important to note that the corners Fast-Fast, Slow-Slow, Fast-Slow, Slow-Fast and Typical-Typical will be considered as the process variations; also, the temperature will be varied from $-40\,^{\circ}\text{C}$ to $120\,^{\circ}\text{C}$; additionally, a variation of $\pm 10\%$ will be made for the supply voltage.

2.4.1 Oscillator

In a LC tank oscillator, its gain can be affected by changes in threshold voltage, doping concentration, length mismatch and oxide thickness of the varactor. Also, variations in the parasitic resistance of the inductor can change its quality factor; in some cases, the quality factor may be low enough so that the transconductance of cross coupled pair is insufficient, and the oscillation will never start. In ring oscillators, PVT variations could change the channel mobility and therefore the delay of each cell; in addition, its gain is modified by variations in the control transistors, which change their effective resistance and capacitance.

Figure 2.26 shows the variation of the tuning characteristic of a traditional five stages ring oscillator (figure 2.27) due to PVT. Besides a change in the free running frequency of 150% (from 5.05 GHz to 17.6 GHz), there is a variation in its gain of more than 100% (from 3 GHz/V to 12 GHz/V) because the strength of the lacth that controls the frequency is modified. Also, there is a strong non-linearity in the tuning characteristic, and a non-monotone behavior which means that for a single frequency there are two possible voltages that generate it; a more detailed description of the causes of this variations are given in chapter 4. In addition, figure 2.28 shows the phase noise variation of the same VCO due to PVT, where a change of 11 dB is noted at 1 MHz of offset frequency.

2.4.2 Phase detector

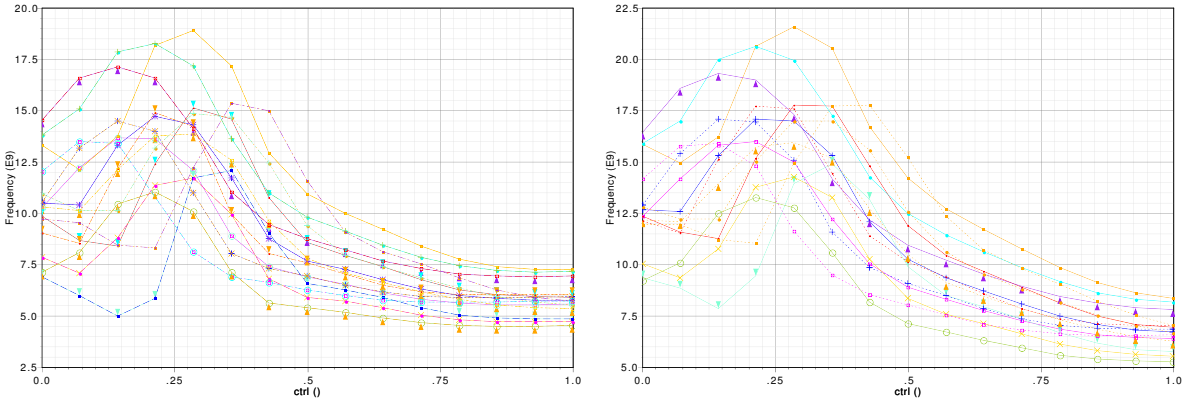
Despite a phase detector can be made by only digital circuits, it introduces some degree of variability in the performance of the PLL because the delay of the UP and DOWN signals is modified, specially by mismatch. PVT variations changes threshold voltage and channel mobility of switching transistors, thus modifying the delay of the gate.

Any difference between the UP and DOWN signals path introduce some amount of extra current to the loop filter; therefore, the phase steady error between the reference and oscillator signal is not zero, despite there is two poles at $s = 0$. Inter-device —mismatch— can change the on and off times of the switches, modifying the delay.

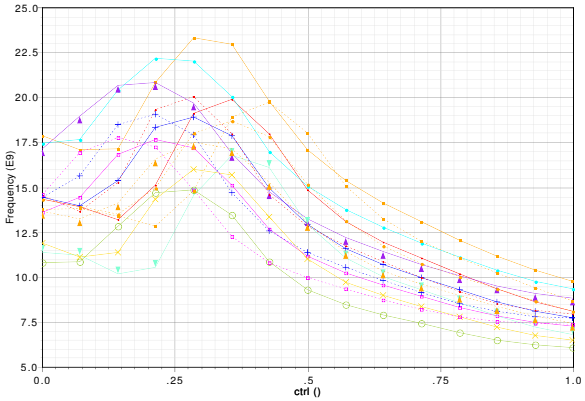
On the another hand, the gain of the phase detector is related to the maximum average output voltage that is able to produce, which is proportional to the supply voltage: the greater the supply voltage, the greater the gain of the phase detector. Changes of $\pm 10\%$ in supply voltage will produce a variation of $\pm 10\%$ in the gain.

2.4.3 Charge pump

The gain of a charge pump depends exclusively of the current of its sources, which are very sensitive to PVT; output impedance is the parameter that is affected by PVT in the most, because it depends of the transconductance of the devices. Furthermore, changes in the threshold voltage affect the excursion range of the output level, thus degrading the linearity of the system. An important issue in charge pumps is the fact that the current of the charge



(a) $V_{DD} = 0.9\,\mathrm{V}$ (b) $V_{DD} = 1\,\mathrm{V}$



(c) $V_{DD} = 1.1\,\mathrm{V}$

Figure 2.26: Effect of PVT variations in the tuning characteristic of a ring oscillator

and discharge sources must be equal, because otherwise steady state error would appear as well as nonlinear behavior. Process corners that involves opposite variations between NMOS a PMOS transistors (Fast-Slow and Slow-Fast) have the biggest impact on this. In addition, differences in the threshold voltage of the switches produce that their on ad off times are different. This could also inject additional current to the loop filter because there is some time interval in which one switch is on but the other off when the UP and DOWN signals are in low state.

Figure 2.30 shows the current of a conventional charge pump, like the one shown in figure 2.29, under PVT. There is a variation 14% in the injected current for the same output voltage. In addition, figure 2.31 presents the variation of the output voltage of the pump with an ideal capacitor as the loop filter, where a change in the dynamic behavior of the control signal could be appreciated.

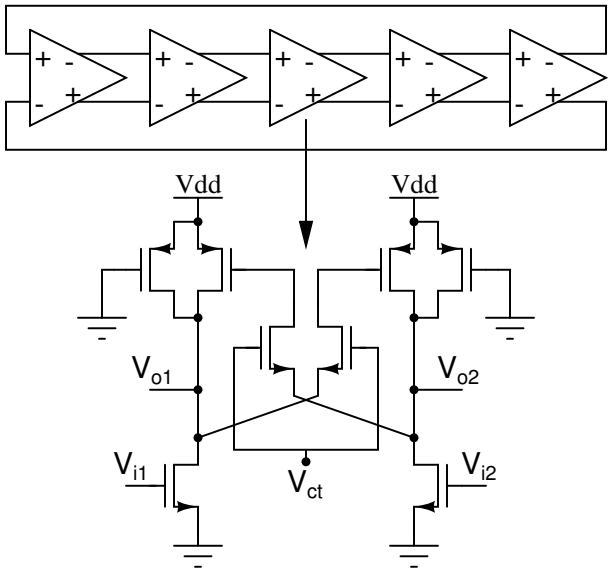


Figure 2.27: Five stage ring oscillator

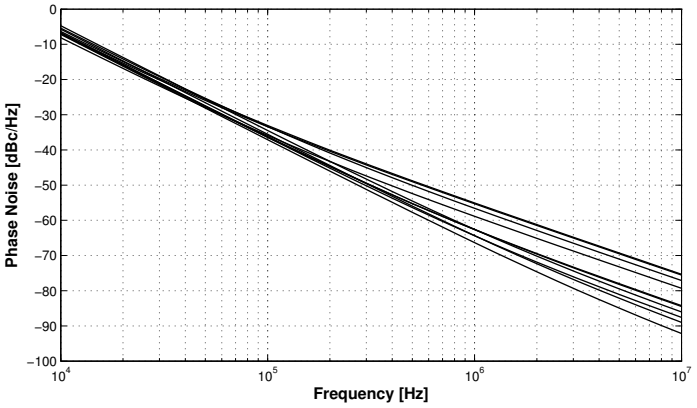


Figure 2.28: Phase noise of a current starved ring oscillator with PVT variations

2.4.4 Loop Filter

Although the loop filter could be made by only passive devices, which with careful layout techniques could have less variations to PVT than the active devices, any change in its pole-zero distribution lead to a change in the closed loop response of the PLL; as was said before, variations in the bandwidth of the PLL implies that more of less noise is transmitted to the output as well as a change in the settling time. The use of active loop filter may be the option which could introduce more variability in the design, because it depends of the stability of the feedback loop aside from phase and gain margin of the operational amplifier; if this is not designed with a robust frequency response it may restrict the bandwidth of the system.

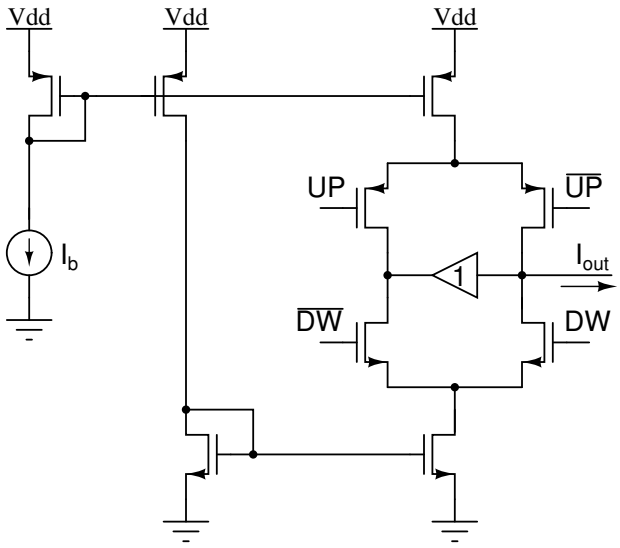


Figure 2.29: Charge pump

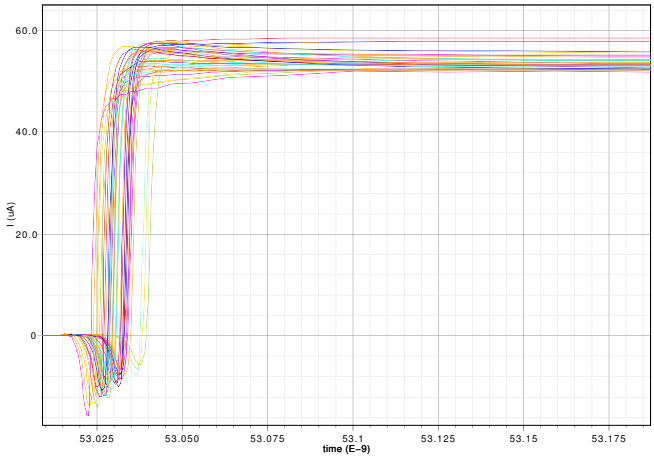


Figure 2.30: Effect of PVT variations on the output current of the charge pump

2.4.5 Frequency divider

The frequency divider is one of the most higher source of variability in the performance of a PLL. Besides that it could also be made by only digital components, changes in the delay of them, specially in the nearest to the VCO, lead to phase differences between output and reference signals in steady state. Further, the frequency divider introduces an considerable amount of low frequency noise, which power changes depending of the operation condition.

PVT variations are not taken into consideration for the frequency divider in this work, wherefore an ideal circuit with a fixed and constant delay is used. For that reason, this thesis will focus in the design of a robust controlled oscillator, a robust phase detector-charge pump, and a robust loop filter.

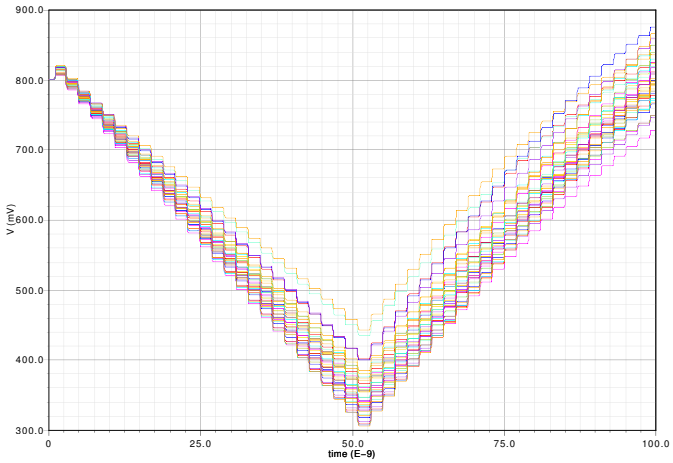


Figure 2.31: effect of pvt variations on the output voltage of the charge pump

2.4.6 Overall PLL

All the variations explained before for each block could be summarized in the closed loop response of the PLL, so that it is possible to get an idea about the variability of the output referred noise and settling time. Figure 2.32 shows the frequency response of all the circuit with PVT. A variation of 69 MHz (300%) in the -3 dB bandwidth and 7 dB (50%) in the resonant peak is observed. Is important to note that some of the circuits do not follow the second order low-pass filter behavior because some more than one flat gain region is observed, wherefore its poles are not complex-conjugated. Finally, figure 2.33 shows the transient response of the PLL with PVT variations. A variation of 200 ns (85%) is observed; moreover, a difference of 75% in the overshoot of the output phase is present.

Taking into account all the explained variation on the performance of both each section of the PLL and whole the system, there is the necessity to develop some design techniques and structures that could reduce the variability of its performance, and therefore synthesize a signal with a constant spectral purity, no matter the operation condition. The above can be summarized in the design of a constant bandwidth system, which filter the same amount of noise from each block of the PLL. For that reason, in the next chapter some design considerations about each circuit are explained.

2.5 State of the art

Many alternatives have been proposed in order to reduce the variability of the performance of a PLL to PVT. Most of them consider digital calibration as the most effective way to compensate the behavior of the circuit, no matter if it is made by either a embedded circuit or an external one. Taking into consideration that the free running frequency of the VCO could vary more than 60% with PVT, the main purpose of calibration is to adjust this frequency to

a constant value. Thus, the loop gain could be kept small, which is favorable for the stability of the loop.

[9] include a digital calibration circuit for the VCO which sets its free running frequency, similar to a coarse tuning loop; this is done by the switching of digital controlled current sources at the startup of the PLL. With this method the VCO gain is kept small wherefore the jitter and phase noise performance is improved. The main drawback of digital calibration is the fact that the circuitry that it needs could consume more power and area than the PLL itself.

In the same manner, [10] develop an algorithm to reduce the sensitivity to supply voltage of a ring oscillator, which is built on-chip. It uses a resistive voltage divider, a SAR analog to digital converter, and two operational amplifier to correct the performance of the oscillator. Likewise, the area covered by these extra circuits is bigger than the occupied by the oscillator.

In [11] a continuous background frequency calibration is performed in the same manner than [9], but instead of calibrate the circuit at the startup, this is done along all the operation time; thus, continuous changes in environment such as temperature could be compensated. In addition, the calibration circuit is built into the divider, so that the increment in area is less than the last alternatives.

Both [12] and [13] use two control loops so as to provide a coarse and fine tuning of the VCO using two charge pumps and loop filters. In [12] the coarse control loop is controlled by a digital word. Also, the charge pump is characterized by its small output resistance, which is opposite to the traditional design methodologies. However, its output voltage is kept constant by a set of resistor that are part of the loop filter. For that reason, the effect of PVT variations is reduced because the charge pump always has the same polarization

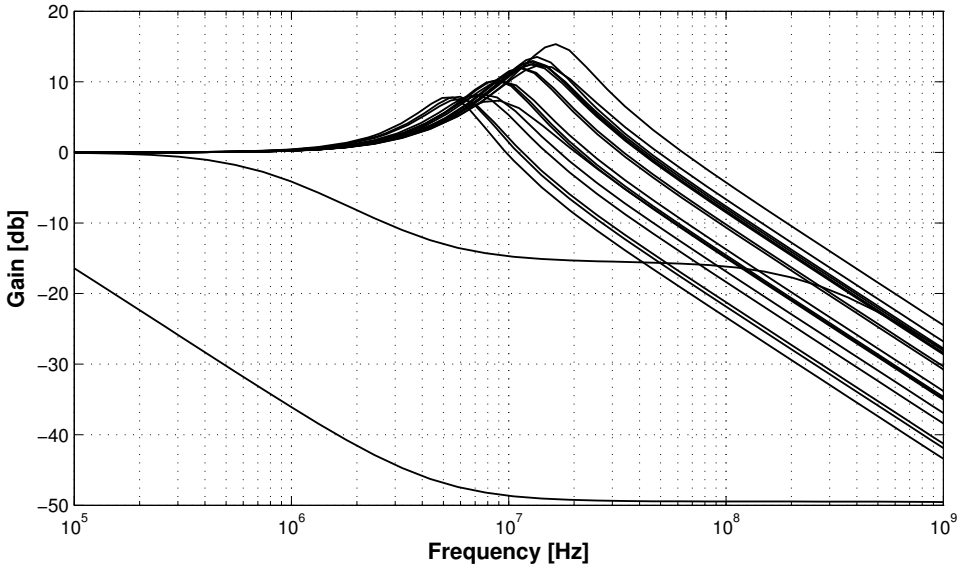


Figure 2.32: Closed loop frequency response of a second order PLL with PVT variations

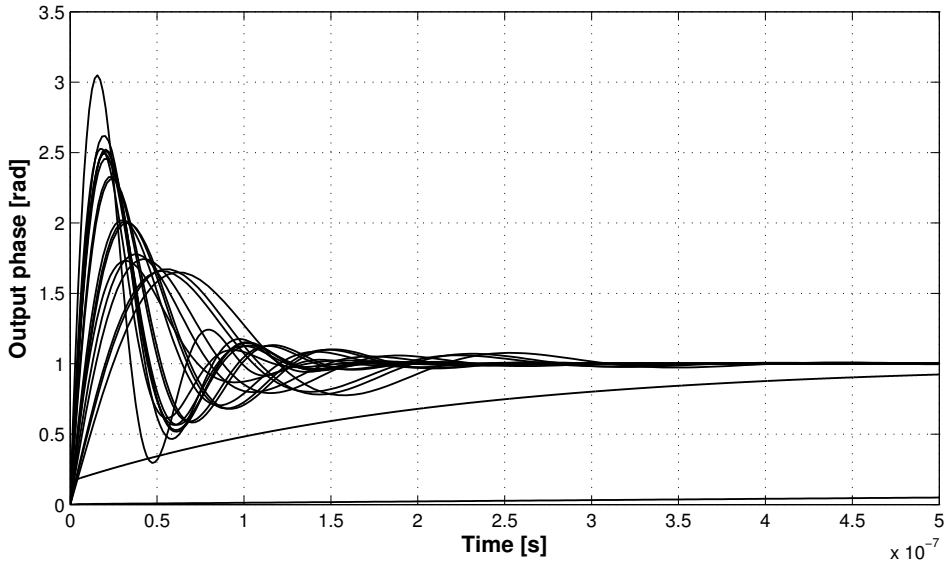


Figure 2.33: Closed loop phase step response of a second order PLL with PVT variations

conditions. Meanwhile, [13] makes use of the commutation of a resistor in the slow control loop to increment the gain of the VCO and adjust its central frequency.

Another technique to compensate a PLL to PVT is explained in [14], where the use of buffer delay stage based on symmetric loads for a self biased ring oscillator is proposed. The buffer consists in a source coupled differential pair; the symmetric load is a diode-connected transistor in shunt with a equally sized device biased at the control voltage. The tolerance to PVT is achieved by the use of a self-biased network which adjust the tail current of the buffer depending of the operation condition. For that reason, the need of digital calibration and external polarizations is avoided. Charge pump is also based on the symmetric load principle, which gives more tolerance to PVT variations.

Finally, [15] presents another kind of background calibration which is done on the transistors for which the PLL performance has the highest sensitivity, such as the ones that form the current sources of the charge pump and the bias of the delay stages. The main idea of this technique is to adjust the I-V characteristic of those transistors, so that a current that follows PVT variations is added to the device. This method needs some extra circuits such as a robust reference current, a low gain amplifier and an analog buffer, wherefore the increment in area is less than with the use of digital calibration.

2.6 Summary

In this chapter the main concepts about the operation of a PLL were given. Additionally, a description of the variations with PVT of each block of it has been presented too, as well as its impact on the performance of the whole system. From this analysis is possible to conclude

that phase noise an settling time are the most affected specifications by PVT, because the bandwidth of the PLL is strongly modified.

Gain and free running frequency of the VCO has a high sensitivity to PVT due to the alteration of the transconductance and mirroring properties of the control transistors; also, supply voltage has a strong influence in the delay of each stage of the oscillator; mismatch in the charge and discharge current of the charge pump could introduce phase differences between the output and reference signal, no matter the inclusion of two poles at $s = 0$ in the direct path; variations of the pole-zero distribution of the loop filter could be reduced by some layout techniques, because it could be made by only passive devices.

Taking the above into consideration, the next chapters describes some guidelines and circuit topologies that decrease the sensitivity of the PLL performance to PVT, in order to design a constant bandwidth circuit.

CHAPTER 3

DESIGN OF A ROBUST PLL: LOW FREQUENCY COMPONENTS

As was shown in chapter two, the performance of a PLL is strongly affected by PVT variations. PVT can produce mismatch in the delay of the outputs of the phase detector, mismatch in the UP and DOWN current of the charge pump, and changes in the tuning range and gain of the oscillator, which are the main factors that change the dynamic behavior and noise performance of the PLL, and could even made the circuit unstable. For that reason, in this chapter the design of the low frequency components of a PLL —phase detector, charge pump and loop filter— is addressed.

This chapter is organized as follows: first section gives some insights about how to reduce the PVT variability in the performance of a circuit; then, for each low frequency component some topologies are contrasted, in order to identify the key aspects of their robustness.

3.1 Robust circuits

In general, there are three ways to reduce the PVT variability of the performance of a circuit: the use of a negative feedback, to identify a flat performance solution for all the variables of the circuit, and the use of a compensation network. All of them can be applied to any kind of circuit, no matter it is a voltage amplifier, and oscillator, a data converter, etc. These three alternatives of PVT compensation are explained below.

3.1.1 Negative feedback

Consider the general negative feedback configuration, as shown in figure 3.1, where A_{ol} is the open loop gain and β is the feedback factor. The relation between the output and input

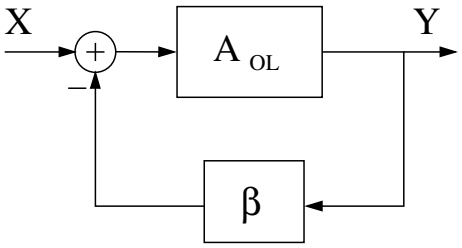


Figure 3.1: General negative feedback configuration

signals —closed loop gain— is:

$$\frac{Y_i}{X_i} = \frac{A_v}{1 + A_v\beta} \tag{3.1}$$

Moreover, if the open loop gain is much higher than the feedback factor, the closed loop gain can be approximated as follows:

$$\frac{Y_i}{X_i} \approx \frac{1}{\beta} \tag{3.2}$$

Equation 3.2 shows that the closed loop gain is independent of the open loop gain. So, if a robust feedback network, like a passive one, is used, the variation of the performance of the whole circuit to PVT is reduced. For instance, if the circuit correspond to a voltage amplifier which gain can vary from 1000 V/V to 2000 V/V (a change of 100%), and the feedback network is resistive voltage divider composed of two equal resistances ($\beta = 0.5$), the closed loop gain vary from 1.996 V/V to 1.998 V/V (a change of 0.1%).

3.1.2 Flat performance solution

In the design process of any kind of electric circuit, no matter if it is analog or digital, it is very common to try to obtain the highest performance; this includes both the selection of an specific architecture and the sizing of the transistors. The cruel reality is that, in most of the cases, this optimal solution does not correspond to a robust design.

For instance, figure 3.2 shows the signal to noise —SNR— of a second order Sigma-Delta modulator as a function of the gain of the two integrators. The modulator can achieve a SNR of 150 dB for a small set of integrator gains; however, any variation of any gain reduces the SNR by 40 dB, for that reason, this is not a robust solution. On the other hand, if the modulator is designed to develop a SNR of 100 dB, there is a large set of integrator gains for which the same SNR is achieved. For that reason, this is in fact a robust solution.

3.1.3 Compensation

Another way to reduce the variation of the performance of a circuit to PVT is to use a compensation signal, as open loop control system. It will adjust the performance of the

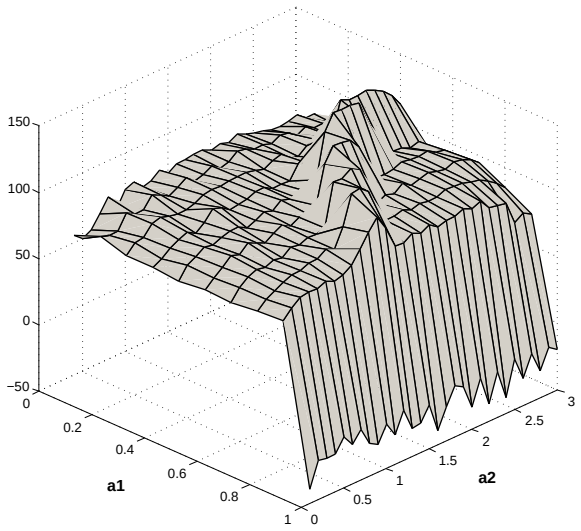


Figure 3.2: SNR of a Sigma-Delta modulator

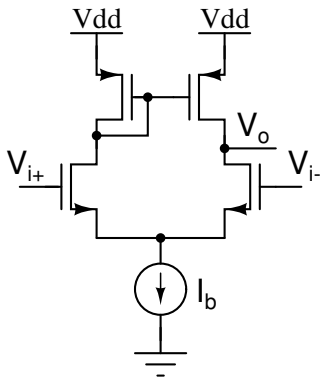


Figure 3.3: One stage-single ended differential amplifier

circuit based on the operation temperature, supply voltage and fabrication condition or state of the process. For that reason, there must be some method to sense these parameters and make the control action.

For example, consider a differential amplifier, as shown in figure 3.3, whose gain is defined by the transconductance of the input transistor. If a variation of temperature is taken into account, the transconductance has a complementary behavior because the mobility of the charge carriers decreases with an increment in temperature. For that reason, a method to make constant the transconductance is to apply a Proportional to Absolute Temperature — PTAT— current to the circuit, so that the decrement of the carrier mobility is compensated with an increment on the device's current. As a result, a robust to temperature amplifier can be obtained.

3.2 Design of robust low frequency components of a PLL

As was explained in chapter two, a PLL consists basically of a phase detector, a charge pump, a loop filter, a controlled oscillator and a frequency divider. Frequency divider and controlled oscillator are circuits which operate at the highest frequencies because they drive the oscillation output. Phase detector, charge pump and loop filter work at the reference frequency, which is tens or more times less than the output frequency. For that reason, those are called the low frequency components and their design is going to be explained below.

3.2.1 Phase Detector

As was explained in the last chapter, a phase detector can be built based on analog circuits —multipliers— or digital circuits —finite states machine—, and each of them has a different tolerance to PVT variations.

Analog multipliers has the advantage of develop a high operation speed because of their smaller dynamic ranges —compared with the supply voltage— in both input and output; this is done in order to guarantee some degree of linearity between the inputs phase difference and the output voltage. However, both the gain and speed depend strongly of intrinsic parameters of the input transistors, such as transconductance, which do not correspond to a robust topology. It is important to note that the transconductance of a MOSFET transistor depends strongly of the charge carriers mobility, which is a function of the doping concentration of both channel and substrate; for that reason, it is very sensitive to fabrication process variations. Also, carriers mobility is a function of the temperature too, which decreases as temperature increases.

In addition, the outputs nodes of a multiplier are in general high impedance nodes, so that their the DC voltage i.e. the output common mode level is a function of the channel modulation factor, which is very sensitive to PVT variation.

Another type of analog phase detector corresponds to a sample and hold circuit, as shown in figure 3.4. If V_i is in phase with V_o, the same voltage will be held on the capacitor; otherwise, if their frequencies are different, successive and different values of V_i will be sampled, and the output voltage will vary. One advantages of this phase detector is that if its inputs are in phase, its output does not have any high frequency component, reducing the noise in the control line. Also, its dynamic range, limited by the input range of the buffer and switches is higher compared with multipliers.

This simple design could be seen as a robust circuit because its gain depends of a capacitor and a feedback amplifier, instead of a transconductance or a output resistance. However, charge injection, clock feedthrough and leakage currents can degrade the precision of the detector, because some amount of charge is injected into the capacitor at each cycle. In addition, taking into account that the supply voltage for the used technology is 1 V, the transistors acting as switches will not operate in the deep triode region, so that their ON

resistance degrades the sampling speed and accuracy.

Taking into consideration that an analog phase detector introduces a high degree of variability and imprecision in the PLL, digital detectors are quite suitable for a robust design. Finite State Machine —FSM— is the selected phase detector because it can detect both phase and frequency differences. Also, as was said in chapter two, the dynamic range of this circuit corresponds to the entire supply voltage, giving some robustness to the noise. In addition, if the temperature and supply voltage of all the devices is the same and only process corners are taken into consideration, the delay of both outputs of the phase detector —UP and DOWN signals— will vary in the same quantity, no matter the operation condition; for that reason, these remain always in synchronism. Moreover, if this delay is small enough so that the continuous approximation is still valid, there is no change in the performance of the PLL.

Nevertheless, if inter-device variations —mismatch— are considered, there is a difference between the UP and DOWN signals path, thus their delay differ one to each other. Mismatch could produce, for example, a difference in the high to low transitions of UP and DOWN, wherefore they will not be zero at the same time; therefore, the switches of the charge pump will not turn off at the same time and some extra current is applied to the loop filter. For that reason, a phase difference between the reference and the VCO signal exists, no matter that the transient behavior of the PLL has finished and the insertion of two poles at $s = 0$ in the direct path.

To mitigate the impact of mismatch, figure 3.5 shows the proposed phase detector whose main characteristic is to reduce the reset path of both outputs. This is done by the insertion of three NOR gates at the output of the flip-flops. The operation of the circuit can be summarized as follows: when an edge of the reference signal arrives, the output of the first flip-flop goes to zero and the UP signal goes to one; in the same manner, when an edge of the VCO signal arrives, the output of the second flip-flop goes to zero and the DOWN signal goes to one. When both outputs of the flip-flops are zero, the output of the NOR gate A is one and thus UP and DOWN go to zero directly. A reduction in the difference between the reset path is achieved because gates B and C are reset by gate A, instead of the outputs of the flip-flops, so that the difference in the reset time of UP and DOWN is produced only by the difference in the performance between B and C gates, instead of the reset path of each flip-flop; it is

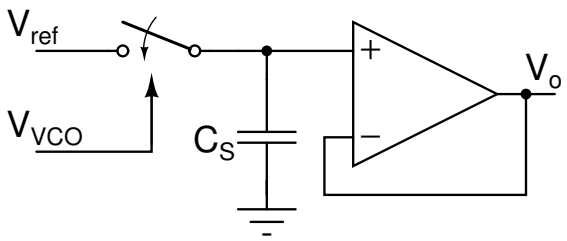


Figure 3.4: Sample and Hold phase detector

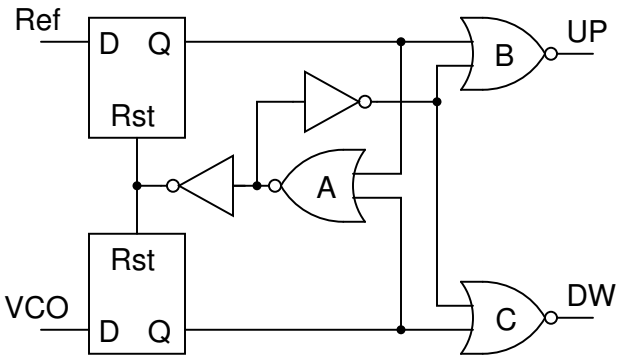


Figure 3.5: Proposed phase detector

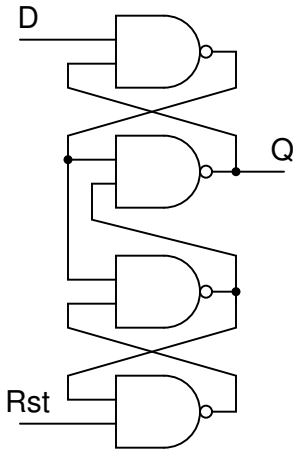


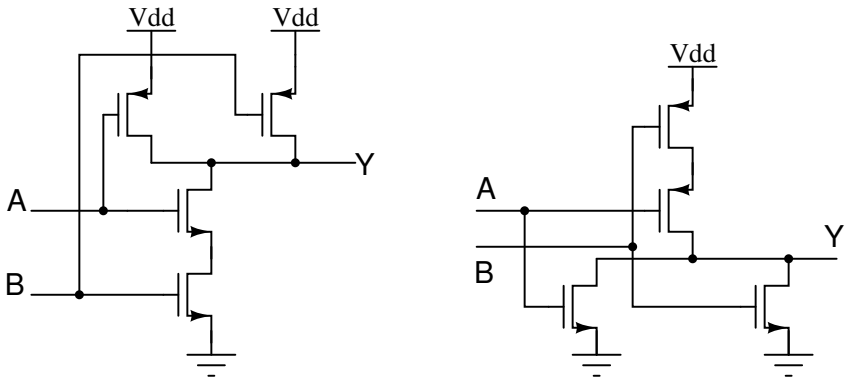
Figure 3.6: Static Flip-Flop used for the phase detector

important to note that the reset path of the flip-flops is bigger than the conformed by the NOR gates, so that the impact of mismatch is less than in a conventional circuit.

The flip-flops of the phase detector were implemented with a static structure, as shown in figure 3.6, which correspond to a robust type of logic. The circuit for the NAND gates is shown in figure 3.7a, while the circuit for the NOR gates is presented in figure 3.7b; as was said, all the logic circuits correspond to static logic. All the transistors are floating-body type with the minimum channel length in order to develop the highest possible speed.

Simulation results

Figure 3.8 shows the UP and DOWN signals of the phase detector for two inputs with equal frequency but a phase difference, for all the operation conditions; this includes 45 corners with three different temperatures ($-40, 60, 120\,^{\circ}\mathrm{C}$), three different supply voltage ($0.9, 1, 1.1\,\mathrm{V}$), and five process corners (Fast-Fast, Slow-Slow, Typical-Typical, Fast-Slow and Slow-Fast). As was expected, when a falling edge of the first input signal arrives at first the phase detector, the UP signal goes to a high state; then, when the falling edge of the second input arrives,



(a) NAND gate circuit (b) NOR gate circuit

Figure 3.7: Logic gates used for the phase detector

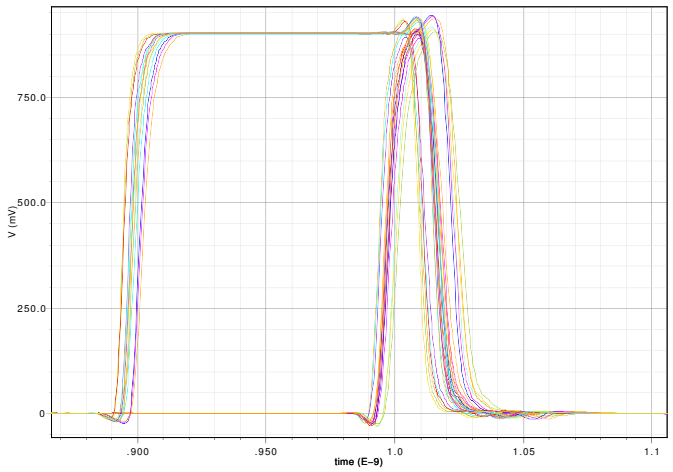
the DOWN signal goes high; immediately after the two signals reach the supply voltage, both goes down at the same time. The delay for both outputs since the edge of the inputs signals reach the flip-flops is 16 ps for nominal operation condition (typical corner, 60 °C and 1 V for supply voltage). In the worst case operation (Slow-Slow corner, 120 °C and 0.9 V) the delay increases to 25 ps, while in the best case operation (Fast-Fast corner, −40 °C and 1.1 V) the delay decreases to 12 ps. It is important to note that no matter the operation condition, the function of the circuit remains correct, including that the UP and DOWN signals reach the supply voltage before the reset pulse is applied, so that both switches of the charge pump are turned on and off completely.

When mismatch is taken into consideration with a Monte-Carlo analysis, the difference in the delay of the reset path between both outputs has a mean of 1.003 ps with a standard deviation of 240 fs. Considering than the traditional structure (figure 2.6) has a delay difference with of 3.02 ps, this design can be considered as a robust circuit.

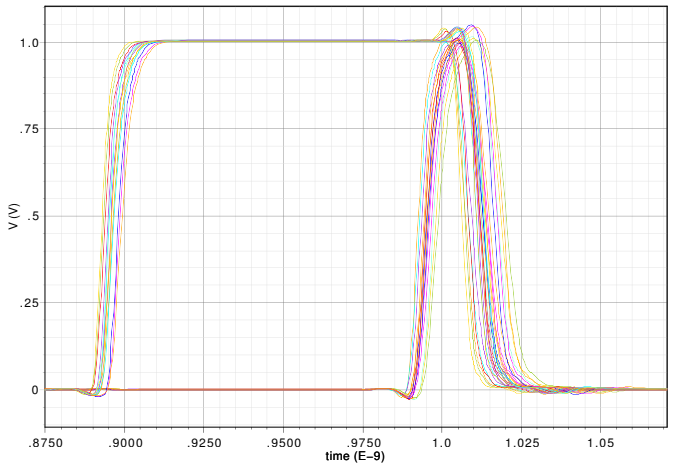
3.2.2 Charge pump - Loop Filter

Considering that a charge pump is composed by two current sources, it is important to keep attention to the output impedance and the amplitudes of the UP and DOWN currents in order to reduce the ripple in the control voltage of the oscillator. In addition, it is required to take into account charge sharing and clock feedthrough effects originated by the switches.

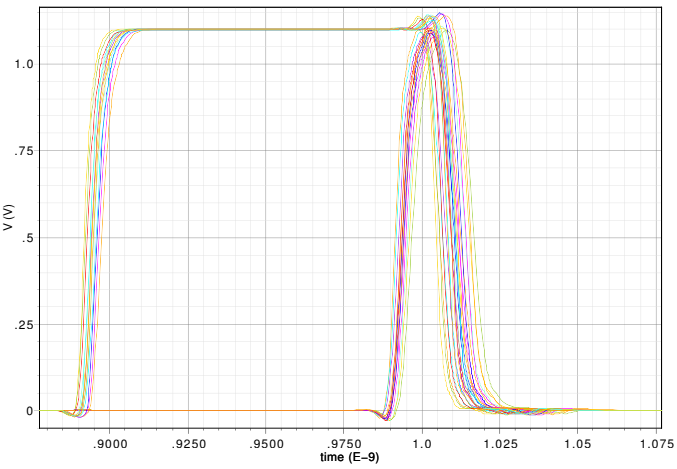
Figure 3.9 shows a current steering charge pump with a mechanism to make equal the UP and DOWN currents [16]; the control mechanism is similar to a Common Mode Feedback, where the main aim is to make equal the current of a NMOS and PMOS current sources, no mater the output voltage. This topology constitute a robust one due to the feedback loop that the amplifier A1 make, so that any variation in the intrinsic parameters of the transistors is compensated with a change in the gate voltage of the PMOS mirror. Furthermore, to mitigate the mismatch in the commutation time of the switches, a buffer (unity feedback configuration)



(a) $V_{DD} = 0.9\,\mathrm{V}$



(b) $V_{DD} = 1\,\mathrm{V}$



(c) $V_{DD} = 1.1\,\mathrm{V}$

Figure 3.8: Output waveform of the phase detector for all operation conditions

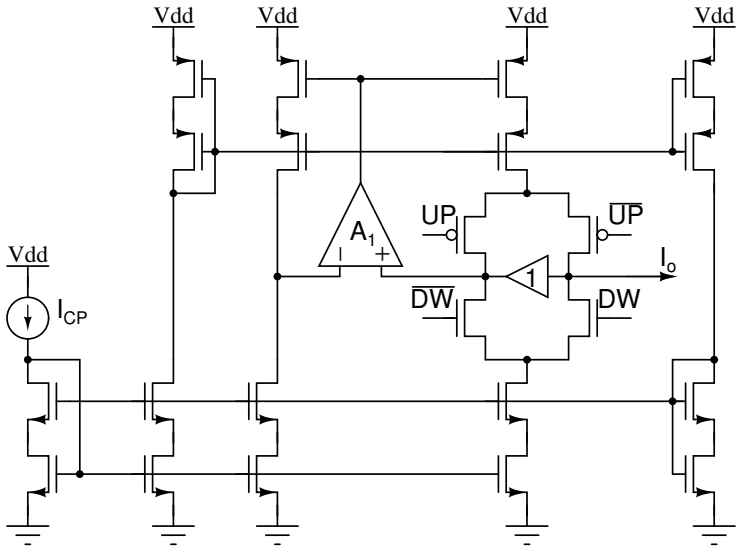


Figure 3.9: Classic current steering charge pump

is inserted between the output node and the complementary branch, so that M_{UP}-M_{UPN} and M_{DW}-M_{DWN} always have the same drain to source voltage. Finally, charge sharing and clock feedthrough effects are minimized by the use of complementary switches, so that the extra charge introduced is canceled.

An important issue in the design of the charge pump is the small output resistance that the transistors of the selected technology have, as was shown in chapter one. For that reason, the use of cascode or another type of high output impedance mirrors is needed. However, taking into account that the dynamic range of these mirrors is lower than that a simple one has, and that the supply voltage is only 1 V, the excursion range for the control voltage is very low. Further, to use a cascode mirror in addition with the feedback configuration could introduce some degree of instability, because the positive and negative feedback path are equal and the open loop gain increases.

In addition, it is very important to emphasize that the transistors connected as switches do not reach the deep triode region in the on state; for that reason their on resistance is not as low as could be in a higher voltage technology, thus degrading the speed and introducing some mismatch; for instance, when the output voltage is low, the transistors that controls the UP current have a high V_{DS}, so that do not even reach the triode region and remain in saturation.

To reduce the impact of the mentioned behaviors, figure 3.10 shows a charge pump with and additional amplifier at the output node, whose feedback network corresponds to the integration capacitor. The main advantage of this configuration is that the output node of the current sources does not have any voltage excursion, and remains at a half of the supply voltage; wherefore, the drain-source voltage of the switches is always the same and low enough

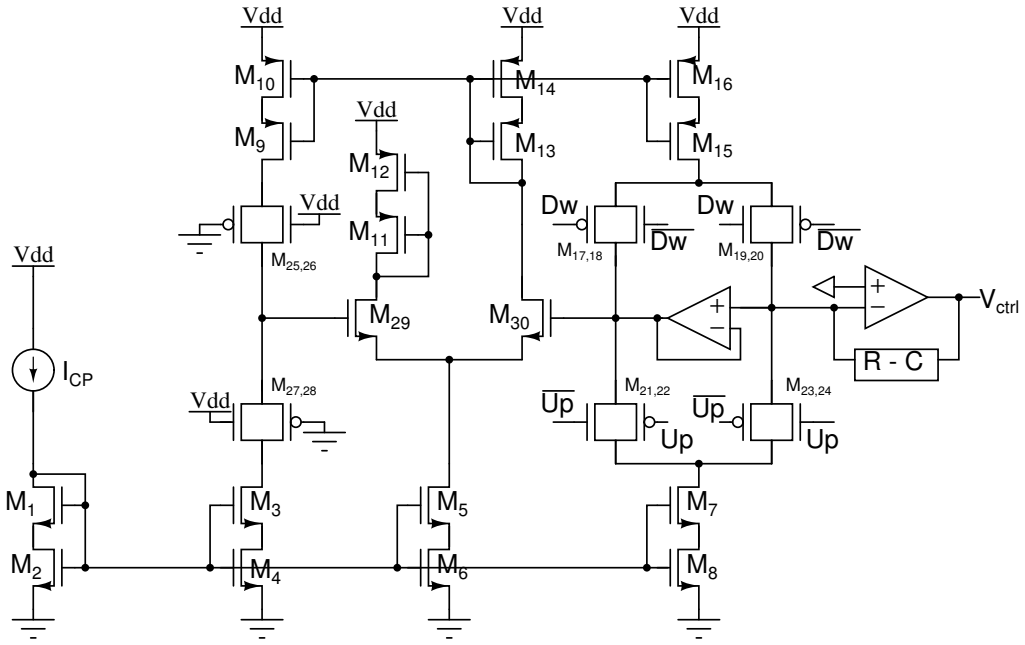


Figure 3.10: Robust current steering charge pump

to keep them in the triode region no matter the operation condition. Also, the impact of the variations in the output resistance of current mirrors due to PVT is minimized, because, as was said before, their voltage excursion is zero.

On the other hand, the main drawback of this topology is that the operation speed is limited generally by the output amplifier —given by GBW and slew rate constrains—, instead of the setting time of the current sources; also, the power consumption and area increase. Nevertheless, this is compensated by the fact that a robust circuit is obtained.

The mirrors of the pump are simple type; however, due to the restriction in the dimensions of the devices, specially in the channel length, all the transistors of the pump are compounds or self-cacoded [17]. A compound transistor (figure 3.11) is an array of two or more transistors in a series connection, whose main aim is to emulate the behavior of a single transistor with different dimensions. If two transistors with equal sizes are connected in series, their behavior is similar to a transistor with the same width but with twice the length of a single transistor. For instance, if a compound transistors is made with to devices with channel length equal to 40 nm, the electric behavior of structure is similar to a transistor with channel length of 80 nm; in addition, it output resistance is also multiplied by two. It is important to note that, on account of the lower transistor of the structure is in the triode region, the effective voltage needed to saturate the upper device is the same as only a single transistor is used [17, 18]. It follows that a compound transistor is an alternative to increase the precision of a current mirror without the implementation of complex topologies.

The main drawback of a compound transistor is related to the increase of the area occupied

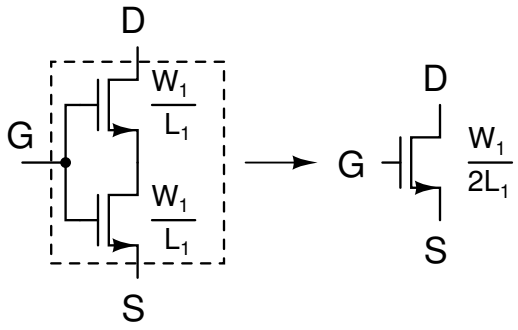


Figure 3.11: Compound or Self-cascode transistor

	Type	Width	Length	Multiplicity
M_{1-2}	Body-Contact	1.3 µm	56 nm	10
M_{3-6}	Body-Contact	1.3 µm	112 nm	10
$M_{7-8,11-12}$	Body-Contact	1.3 nm	112 nm	20
$M_{9-10,13-14}$	Body-Contact	1.3 nm	112 nm	18
M_{15-18}	Body-Contact	1.3 nm	232 nm	10

Table 3.1: Transistor's dimensions of the amplifier

by the structure. Due to that the effective length is increased, the current capability of the structure decrease. For that reason, it is necessary to double the width of each device; if three or more transistor are used in the compound one, it would be necessary to made three of four times bigger the width of each device.

The amplifier used at both the output of the pump and as a buffer is presented in figure 3.12 [19]. Its behavior is similar to a class AB amplifier, because the output transistors are driven by positive and negative input signal, so that the circuit has an additional current capability —needed to drive the capacitors of the loop filter—. Alike was explained before, in order to increase the precision of the current mirrors, self-cascode transistors are used in the amplifier; also, body-contact transistors are used in the whole amplifier in order to reduce the low-frequency gain distortion. Figure 3.13 shows the frequency response of the amplifier; the circuit achieves a gain of 57 dB and a unity gain frequency of 550 MHz for the typical operation condition, 62 dB and 820 MHz for the best case, and 53 dB and 410 MHz for the worst case, for a load capacitance of 500 fF; the power consumption is 280 µW for typical case, and table 3.1 summarizes the dimensions for each transistor.

To ensure the stability of the pump, a low gain amplifier is used to control the left and right branches of the circuit; although its gain is low, it is enough to guarantee that all high impedance nodes are at the half of the supply voltage in any operation condition. Also, dummy switches are inserted in the left branch to maintain the symmetry.

Finally, any difference in the on and off time of the switches can be reduced with the use of

	Type	Width	Length	Multiplicity
M_{1-8}	Body-Contact	1.3 µm	232 nm	15
M_{9-16}	Body-Contact	1.3 µm	232 nm	20
M_{17-28}	Floating-body	400 nm	40 nm	1

Table 3.2: Transistor's dimensions for the charge pump

complementary transistors. This structure not only reduce the effect of charge sharing, it also guarantees that all the four switches has the same characteristics, so that their performance vary in the same proportion for all of them. If the Fast-Slow and Slow-Fast corners are present, or if the temperature coefficients of NMOS and PMOS transistors are different, the variations of the slow transistor is compensated with the variation of the fast transistor, so that the performance of the switch remains constant. Table 3.2 summarize the dimensions for each transistor that is part of the charge pump.

Loop Filter

The loop filter can be one of the most important components of the PLL because it has a strong influence in the phase to phase transfer function of the whole system; any variation in one of its components can even make unstable all the circuit. Passives filters constitute a robust alternative, because its transfer function does not depend of intrinsic parameters of

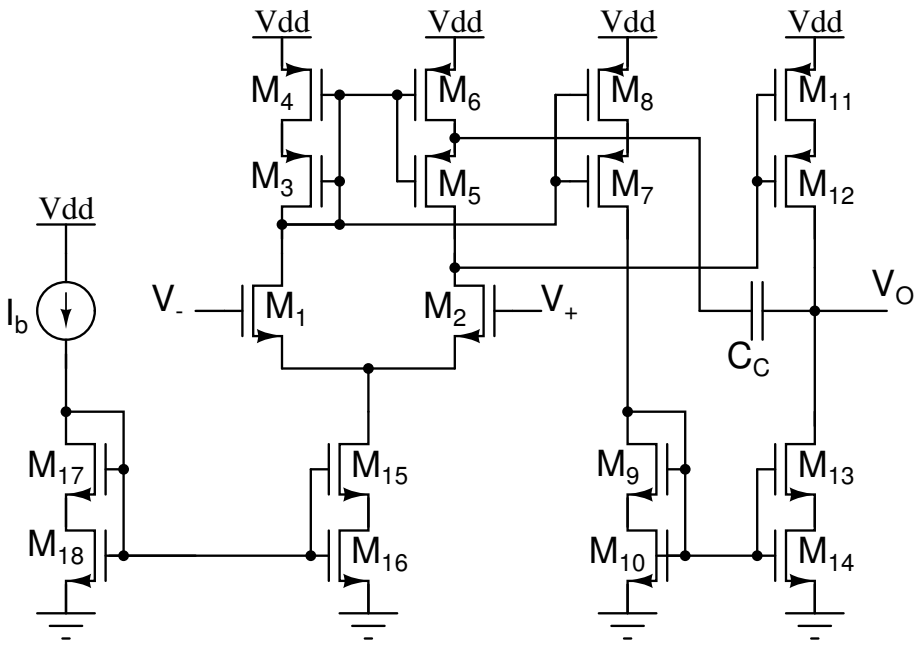


Figure 3.12: Single ended class AB like amplifier

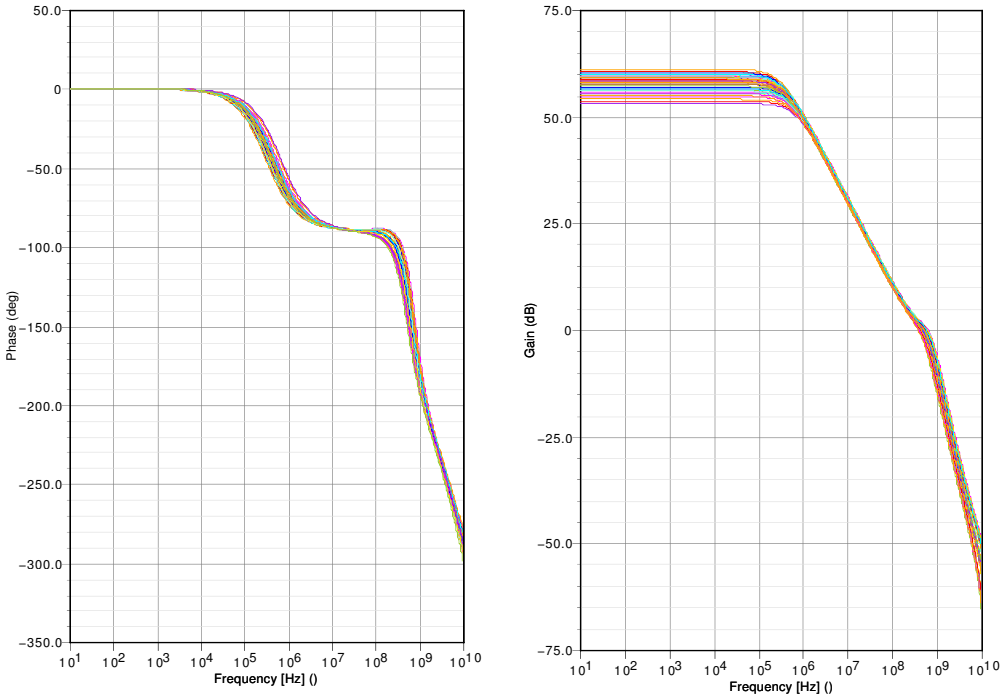


Figure 3.13: Frequency response of the amplifier of figure 3.12

transistor such as transconductance and output resistance. In addition, a passive network is more stable with temperature variations than an active one, and its temperature coefficients are well defined. Moreover, with some appropriated layout techniques the effect of mismatch can be reduced.

Other advantages of the use of passive networks as loop filters is to add a low level of noise —there is less thermal noise and no flicker noise—, very high PSRR because there is no connection with the supply rail. Nevertheless, in some low noise applications, there is the need to use large capacitors, so that there is a trade-off between area and bandwidth.

Current mode circuits constitute another alternative for the implementation of the loop filter. However, due to the low output resistance of the transistors, the parasitic effect of the drain to source conductance degrades the frequency response of the filter. In addition, this conductance has a strong dependence of PVT variations, so that the total transfer function can not be controlled.

Taking into account that the feedback network of the output amplifier corresponds to the integrator capacitor, it can be replaced by a RC network which defines the frequency of the stabilizing zero, as figure 3.14 shows.

Simulation results

Figure 3.15 shows the output current of the charge pump for all operation cases. The charge pump was simulated altogether with the phase detector, so that two signals with equal fre-

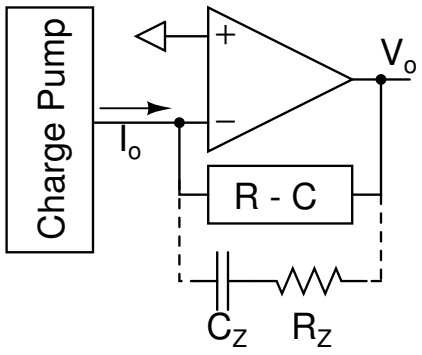
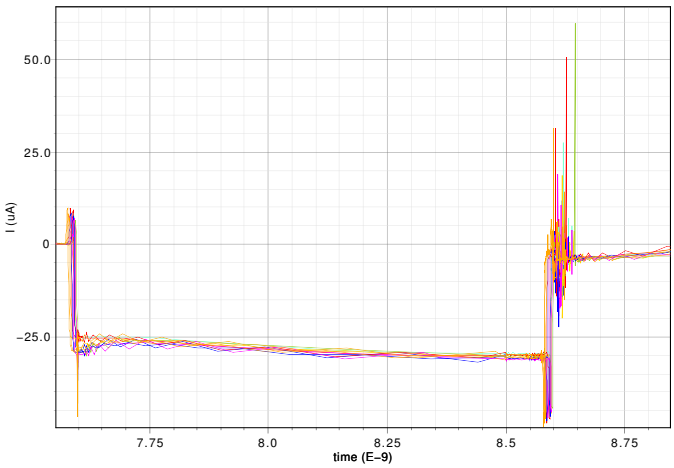


Figure 3.14: Loop filter topology.

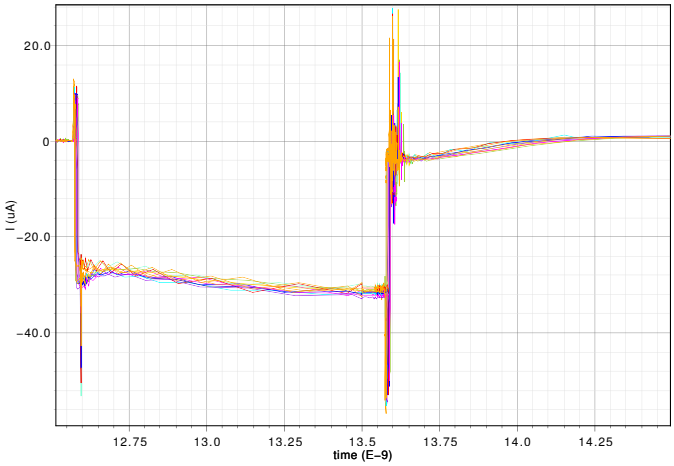
quency but different phase were used too; these signals were applied to the phase detector, then its UP and DOWN output signals control the switches of the charge pump. As was expected, when the falling edge of the second signal arrives the phase detector at first, the DOWN signal goes to high and the DOWN current discharges the loop filter; then, when the falling edge of the first input signal arrives, the UP signal goes to high and the UP current is directed to the loop filter so that no net current flow across it. A maximum variation of $\pm 1.25\ \mu A$ (4.1%) —over a nominal current of $30\ \mu A$— of the output current can be appreciated. Moreover, the difference between the UP and DOWN current for all operation conditions is less than 1.5%; this proves that both current are matched despite the low output resistance of the devices.

In addition, figure 3.16 shows the output voltage of the loop filter when it is conformed only by the integration capacitor, for all the operation cases; a rail-to-rail operation is always achieved, which is very appropriated for a low voltage PLL.

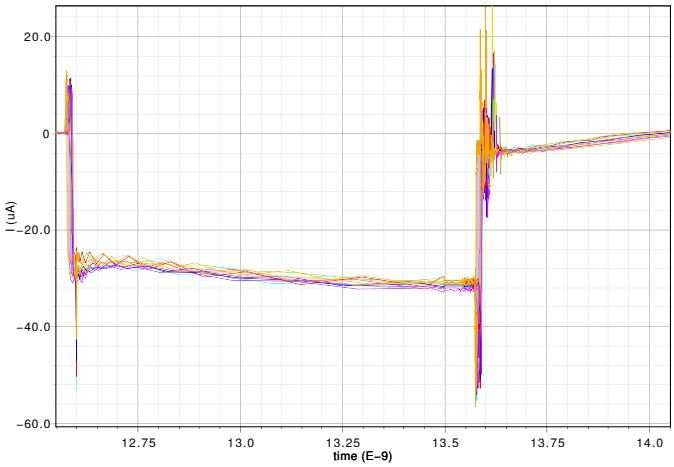
It is important to highlight that the current of the charge pump can be varied from 5 μA to 60 μ A without any lose in its characteristic and precision, which allows to define different transfer functions, based on the required setting time and noise; if a higher current is needed, it would be necessary to add an output stage to the output amplifier of the charge pump.



(a) $V_{DD} = 0.9\,\mathrm{V}$

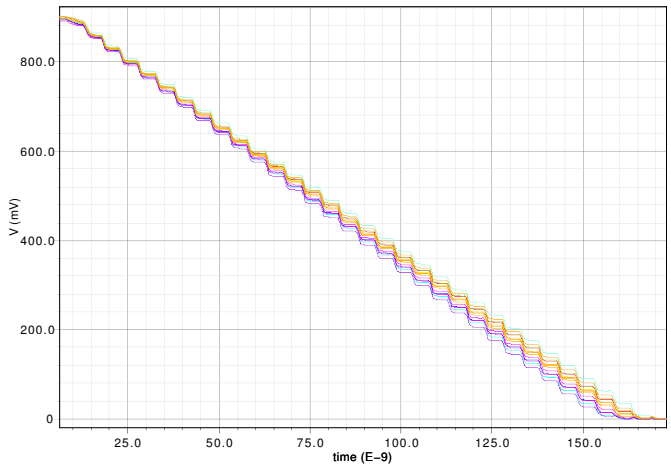


(b) $V_{DD} = 1\,\mathrm{V}$

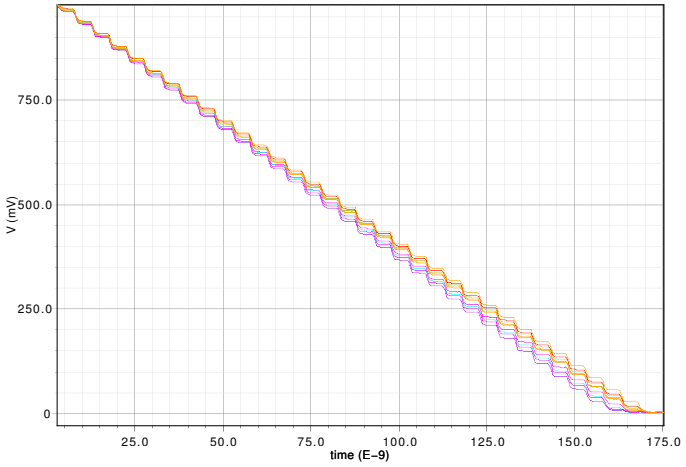


(c) $V_{DD} = 1.1\,\mathrm{V}$

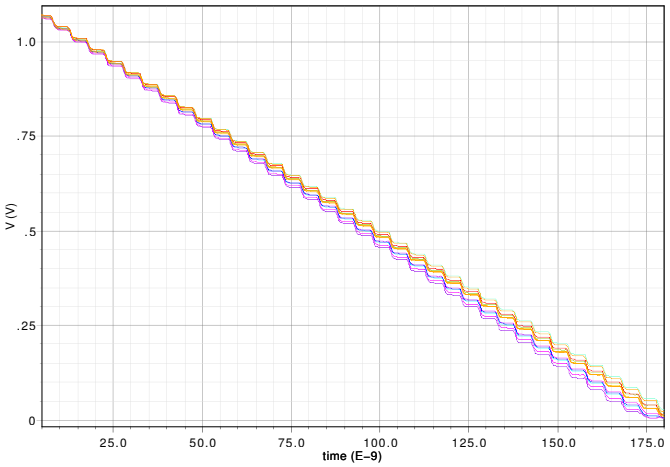
Figure 3.15: Output current of the charge pump for all operation conditions



(a) $V_{DD} = 0.9\,\mathrm{V}$



(b) $V_{DD} = 1\,\mathrm{V}$



(c) $V_{DD} = 1.1\,\mathrm{V}$

Figure 3.16: Output voltage of the charge pump-loop filter for all operation conditions

3.3 Summary

In this chapter some design considerations for decrease the sensitivity of the performance of any circuit to PVT was given; these include the use of feedback networks, , and to implement some compensation network which adjust the performance of the circuit based on the current operation case. Based on this, a robust topology for the charge pump was presented, which mitigates the systematic mismatch of the UP and DOWN currents due to the low output resistance of the transistors; this is done by building current sources that do not have voltage excursion. For the loop filter, a passive implementation was selected because it transfer function does not depend of any parameter of transistors; also, its temperature coefficients are well defined and constants, and has a high PSRR. Simulations results shows a variation of ± 1.25 µA over 30 µA in the current of the charge pump, and a difference of 1.5% between the UP and DOWN current with a rail to rail operation.

Taking the above into consideration, the next chapter explains the design of the high frequency components of a PLL, specially the oscillator. Some design considerations for build an oscillator with a linear and robust tuning curve are given, as well as a compensation circuit which adjusts its free running frequency.

CHAPTER 4

DESIGN OF A ROBUST RING OSCILLATOR

So far the design of robust low frequency components of a PLL, specially the phase detector, charge pump and loop filter was addressed. For these, the use of feedback loops was the main design consideration to reduce the sensitivity to PVT of their performance. In this chapter, the design of a ring oscillator that has a low variability to PVT is explained, so that it can be included in a feedback loop to build the PLL. Some topics about the type of transistors used for the ring are discussed, as well as different method for tune the oscillator. Moreover, a bias network that compensates its central frequency for temperature variations and process corners is presented.

4.1 Impact of History Effect on ring oscillators

History effect, as was explained in chapter one, is the variation of the threshold voltage of a SOI partial depleted transistor due to the charge accumulation in the undepleted region of the floating body. Because of the absence of polarization of the body, its charge can vary with diode leakage, gate tunneling, and its own drain to source current. In analog and static circuits the history effect does not constitute a problem because the current that the device drives is constant, so that the charge of the body is altered only at the startup of the circuit. However, for dynamics circuits, as could be a simple logic gate or a ring oscillator, the body charge is varying with each transition of the input voltage until a steady state is reached [20].

For a ring oscillator specifically, on account of the change in the threshold voltage of all transistors with each transition, which is reflected in an change of the commutation threshold of the delay cell, another time constant appears for the circuit; this time constant is related

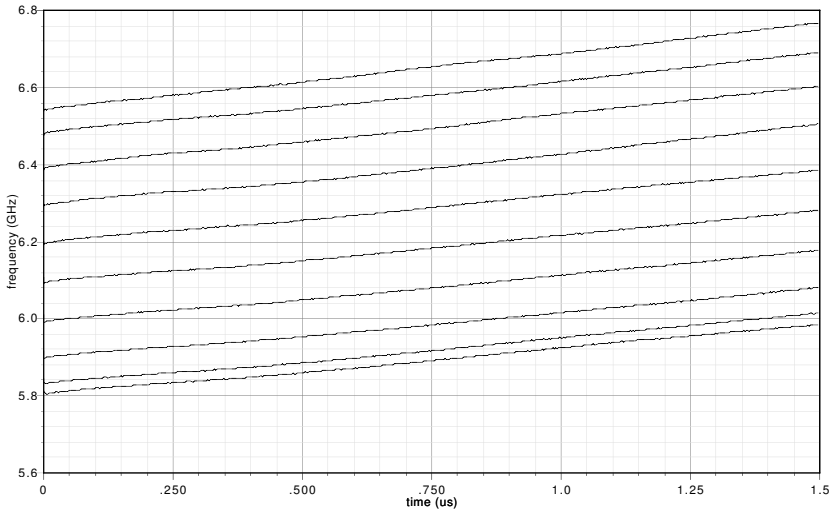


Figure 4.1: Frequency of a floating-body ring oscillator as a function of time

to the settling of the oscillation frequency and is totally independent of the settling time of the PLL; on the contrary, it is a function only of the intrinsic parameters of the transistors for a given technology.

Figure 4.1 shows the frequency of a voltage controlled fifteen stages ring oscillator as a function of time, and for different control voltages. For each case, it can be seem a change of more than 200 MHz without any change in the control system; additional simulations show that the settling time of the oscillation due to history effect is about 70 µs, which is much higher than the settling time of the whole PLL. This result is supported by [20], where a settling time of 20 µs in the delay of each stage of a 100 nm ring oscillator is reported. It is important to note that the settling time for the frequency of a ring oscillator could be greater than the settling time for the delay of an inverter chain. This can be explained as follows: in a single chain of inverters, the first gate is driven by a voltage source —or at least a well defined input— which has its transitions times well defined and constant, wherefore it always operates under the same conditions, and the stabilizing process for its body charge begins at the startup of the circuit. However, during this transient behavior for the first gate, the other ones has inputs signals with different characteristic each transition, so that they can not begin the stabilizing process. Once the body potential of the first gate has entered in a steady state, its delay will be constant and the second one begins the same process. Again, the third gate can not establish its body charge until the second one has done it. The process continues in the same way until the last gate has a constant delay. Nevertheless, in a ring oscillator, due to the feedback between the output and the input of the chain this process gets worst; the main reason is that the first gate is not driven by a signal with the same characteristics, wherefore it can not begin the body charge stabilizing process at the startup of the circuit. For that reason, the required time to set the frequency of the oscillator is higher.

In addition, a high frequency oscillator requires more time to set itself than a low frequency

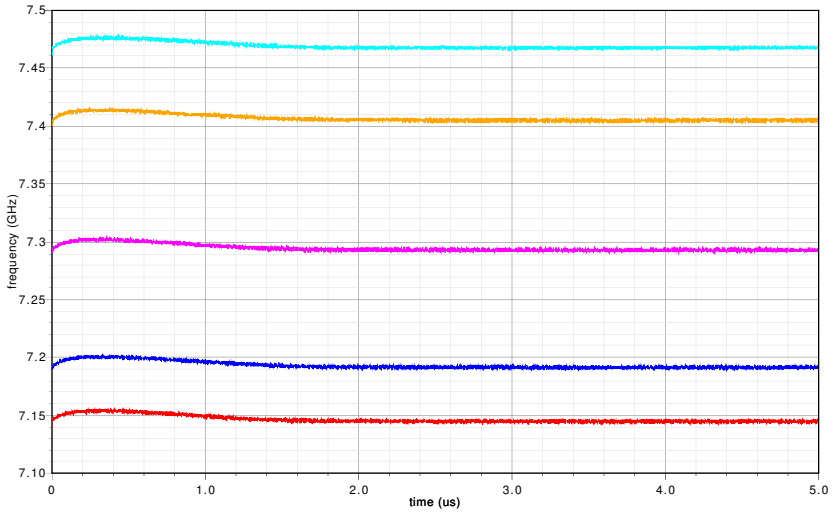


Figure 4.2: Frequency of a body-contact ring oscillator as a function of time

one. On account of the fast transitions at the input of each gate, the time to carry out all the recombination processes that set the body charge is less.

It is important to note that in steady state, the body potential is not a constant value; on the contrary, it vary at the same frequency of the output signal. For that reason, the threshold voltage of the transistors that form the cell is varying with time. This effect introduces some kind of modulation to the delay of the cell, which degrades the phase noise and jitter specification.

In addition, history effect is influenced by the temperature of the circuit and its supply voltage. [21] reports an history effect of 14% for $-40\,^{\circ}\mathrm{C}$ and $V_{DD} = 1.1\,\mathrm{V}$ and 6% for $120\,^{\circ}\mathrm{C}$ and $V_{DD} = 0.9\,\mathrm{V}$, for the technology used.

An alternative to mitigate the explained behavior is to use body-tied or body-contact transistors, which corresponds to some kind of SOI transistors with an additional implant that is used as a contact to the body [20]. Their performance is similar to a bulk transistor whose body resistance is very high —between $30\,\mathrm{k\Omega}$ and $50\,\mathrm{k\Omega}$—. They are available with a channel length of 56 nm, 112 nm and 232 nm; the first ones will be used in the oscillator in order to develop the maximum operation frequency.

Figure 4.2 shows the frequency of the same oscillator as a function of time and for different control voltages, but with body-contact transistors. A transient behavior can be seen, which duration is less than $2\,\mu\mathrm{s}$, before the frequency enter in a steady state. This behavior is due to the high body resistance of the devices, which makes that the body potential is not exactly the same that the source potential. However, this settling time is much lower and comparable when the time constant of the PLL, than when floating-body devices are used.

4.2 Realizations of ring oscillators

As was said in chapter two, a ring oscillator is composed by a chain of delay-inverter cells, in which the output of the last cell is connected directly to the input of the first cell. If there is enough delay across the chain a positive feedback configuration is achieved, whose frequency is given by the following equation:

$$f_o = \frac{1}{2NT_D} \tag{4.1}$$

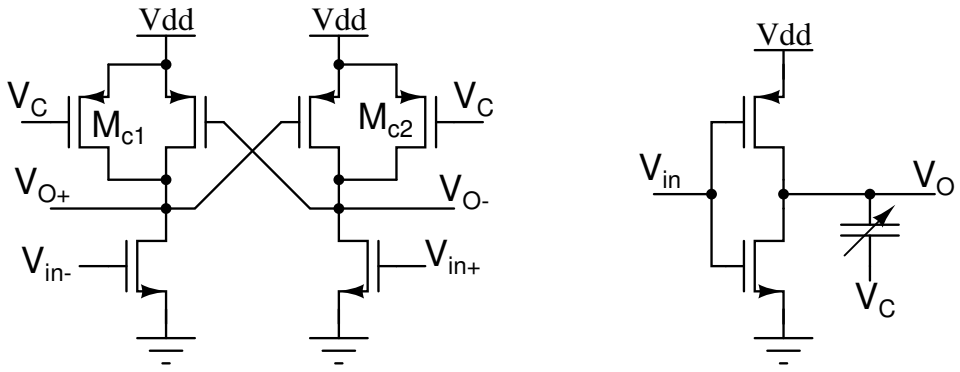
There are many types of implementations for the delay cell, which include from a basic digital inverter to differential pairs or transconductance cells; in addition, the delay of each one could be controlled by either a voltage or a current or both. Linear cells, as could be a differential pair, do not constitute a robust circuit because the conditions for oscillation starts —Barkhausen conditions [22][1]— depends of the transconductance of the cell and its load capacitance, parameters that are very influenced by PVT. Also, the finite output resistance of the cell —which uses to be very low for the used transistors— can vanish the oscillation; in [14] the use of a feedback network to adjust the current of the cell with the purpose of guarantee the oscillation no matter the operation condition is proposed. However, the small amplitude of the oscillation that a linear cell achieves —compared with the supply voltage— causes that the jitter and phase noise increase. For that reason, in a low voltage application, it would be preferred to use a digital delay cell, which can achieve a rail to rail oscillation.

4.2.1 Voltage controlled ring oscillators

When a voltage is used to control the delay of a cell, it is possible to change its load which can be either the effective resistance of a transistor or the capacitance of a varactor; figure 4.3 shows the implementation of these control methods on a digital cell [23].

If the resistance of the load transistors is modified (figure 4.3a), an almost linear and wide tuning range —several gigahertz—- is obtained because it can vary from some hundreds of ohms —when the control signal V_c is near to ground— to almost a open circuit —when the control signal V_c is V_{DD}—. However, this could be the tuning method that has the highest sensitivity to PVT, because the effective resistance of a transistor has a strong dependency of its intrinsic parameters such as carrier mobility, doping concentrations, etc. On the other hand, if the capacitance of a varactor is controlled (figure 4.3b), a small non linear tuning range is obtained because the nonlinear V-C relationship of the varactor; in addition, the sensitivity to PVT of the tuning curve is comparable with the last method, because the capacitance of the varactor depends of its intrinsic parameters too.

[1] There are two conditions that any circuit must meet so as to generate a stable oscillation: the magnitude of its open loop gain at the oscillation frequency must be one, and the phase must be 180°



(a) Tuning by an effective resistance

(b) Tuning by a capacitance

Figure 4.3: Voltage controlled delay cells

4.2.2 Current controlled ring oscillator

When current is used to control the frequency of the oscillator, the main aim is to restrict the maximum current that can flow across the cell, so that the load capacitor is charged and discharged with a limited slew rate; figure 4.4 shows the structure of a current controlled delay cell, which delay is given by the follows expression:

$$T_d = \frac{C_L V_T}{I_{CT}} \rightarrow f_{osc} = \frac{I_{CT}}{2NC_L V_T} \tag{4.2}$$

where N is the number of stages of the chain, I_{CT} is the control current, C_L the load capacitance and V_T the commutation threshold of the cell. Equation 4.2 shows a linear relationship between the oscillation frequency and the control current. Unlike the voltage control method —wherein the resistance of the load transistors is modified— this one has a lower sensitivity to PVT; this can be explained as follows: the differences in the tuning gain of a current controlled oscillator between different operation conditions is due to the variation of the commutation threshold principally. However, for a logic gate, its V_T is a function of the ratio between the aspect ratios and intrinsic gains of the PMOS and NMOS transistors, so that, if the variations make that the both types of transistors vary in the same quantity —temperature variations and Fast-Fast and Slow-Slow corners— this relation keeps constant and the gate commutes at the same input voltage; the possible difference in the commutation threshold is due to the difference between the thermal coefficients of both types of transistors. In addition, when cross corners like Fast-Slow and Slow-Fast are present, the variation of V_T is mitigated because both NMOS and PMOS transistors are involved in the transition process, therefore the difference on their performance are compensated.

The main drawback with a current controlled cell is that, on account of the high output resistance of control transistors M_{c1} and M_{c2} of figure 4.4, the dynamic range of the output voltage can be lower than the supply voltage and degrading the jitter and phase noise per-

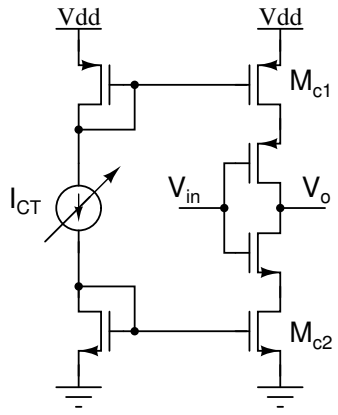


Figure 4.4: Current controlled delay cell

formance. However, on account that the channel modulation effect in the transistors used for this work has a high influence, the output excursion is almost V_{DD}. Further, the output of the loop filter is a voltage signal, so that a voltage-to-current converter is need, which might introduce some additional variability to PVT.

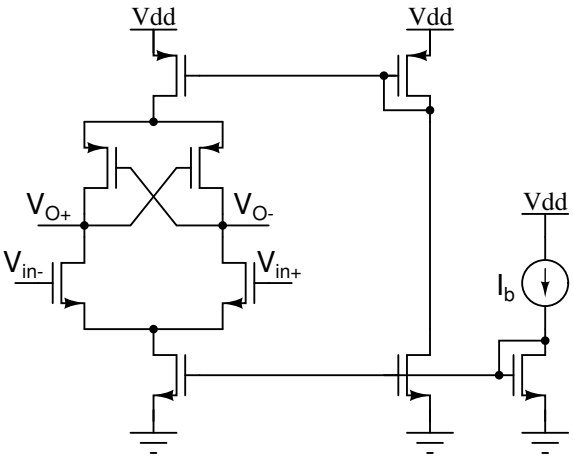
4.2.3 Oscillator's core

Digital delay cells can be implemented by singled-ended, fully-differential or pseudo-differential inverters; figure 4.5 shows the transistor level diagram for each one of them. In a fully-differential implementation a unique control current bias the cell so as to guarantee the symmetry of the output waveform; for that reason, the low-frequency $1/f$ noise up-conversion is reduced as well as the coupling from the power supply [16]. However, this kind of cell needs a large supply current —compared with others cells— for a given operating frequency.

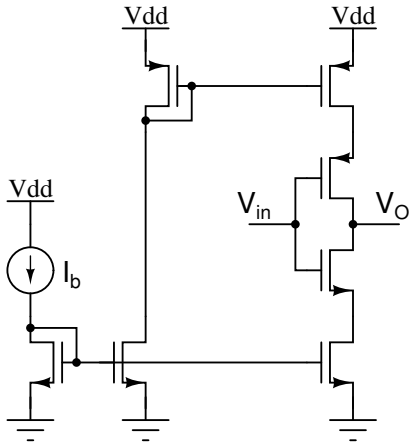
In a singled-ended cell the noise coupling from the power supply increases, as well as the up-conversion of the flicker noise. In addition, the symmetry of the waveform is very sensitive to PVT due to the variation of the commutation threshold. However, it can develop a higher operation frequency for the same supply current.

A pseudo-differential cell takes the advantages of both types of implementations: a high symmetry output waveform which reduce the noise coupling and modulation, and a high operation frequency. Through the latches that link the to chains, a 50% duty cycle waveform is obtained with a low variation with PVT; it is important to note that these latches must have relative small dimensions compared with the inverter, otherwise the oscillation could not start.

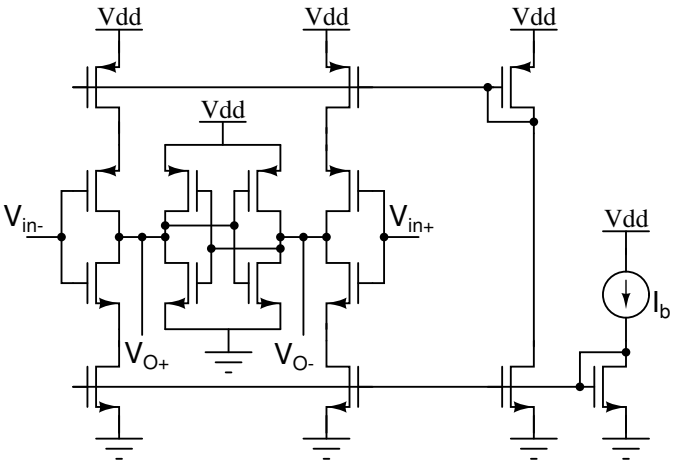
Taking on account the explained before, a pseudo-differential delay cell is used for the oscillator; figure 4.6 shows its transistor level diagram. Three stages are used with the aim of minimize the device's noise contribution and develop the highest operation frequency. Furthermore, only two current sources are used to control all the ring, in order to reduce the



(a) Fully-differential delay cell



(b) Single-ended delay dell



(c) Pseudo-differential delay dell

Figure 4.5: Different types of delay cells

noise contribution too: the first one (M_{1-2}) is used for bias the ring at a fixed free running frequency; the second one (M_{3-4}) is used for tune the oscillator in a small frequency range. As was said before, all the transistors that form the oscillator, including those of the latches, are body-contact type to minimize the floating-body effects; table 4.1 summarizes the dimensions of each transistor.

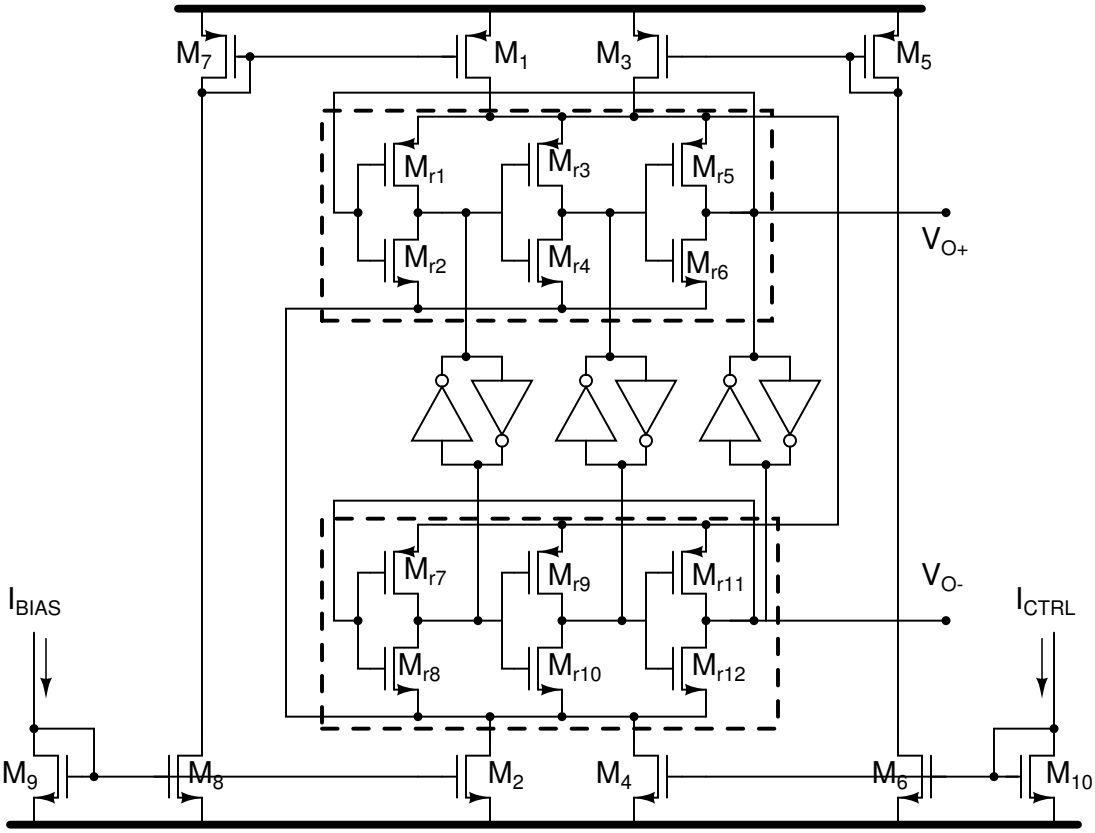


Figure 4.6: Selected pseudo-differential ring oscillator

	Type	Width	Length	Multiplicity
$M_{1-2,7-9}$	Body-Contact	1.3 µm	112 nm	30
$M_{3-6,10}$	Body-Contact	1.3 µm	112 nm	15
M_{r1-r12}	Body-Contact	1.3 nm	56 nm	6
M_{latch}	Body-Contact	1.3 nm	56 nm	4

Table 4.1: Transistor's dimensions of ring oscillator

4.2.4 Voltage to current —V/I— converter

The output signal of the loop filter is voltage type, however the oscillator is controlled by a current type one, so that there must be a mechanism to convert the information of the output of the loop filter to a current signal. This is done by a voltage-to-current converter.

A robust V/I converter must have a linear and constant relationship between its input voltage and output current no matter the operation condition; in addition, due to the low supply voltage allowed, its input voltage excursion needs to be almost V_{DD}. Many types of V/I converter are based in the small signal relationship of the drain current of a transistor; however, its input range is very restricted and the sensitivity of the gain to PVT is very high because it correspond to the transconductance of the device:

$$i_d = gm \times v_{gs} \tag{4.3}$$

In order to increase the input range and to reduce the variability of the gain the input transistor degenerated by a resistor (figure 4.7); if the transconductance is high enough, the gain of the converter is defined by the degeneration resistor and its linearity increases. Nevertheless, the input voltage range is restricted by the threshold voltage of the input transistor, which is very sensitive to PVT; figure 4.8 shows the output current of the V/I converter of figure 4.7 for all the operation conditions, wherein a variation of 400 mV in the input range and 8% in its gain are seem.

For the purpose of reduce the variation of the gain of the converter to PVT, an auxiliary amplifier is used to build the feedback network (figure 4.9). As was explained in chapter three, if the gain of the amplifier is high enough the closed loop gain is only defined by the resistance, which has a less variability to PVT:

$$I_o = \frac{gm_1 r_{o1} A_v}{1 + gm_1 r_{o1} A_v R} \times V_{in} \approx \frac{V_{in}}{R} \tag{4.4}$$

Nonetheless, the input voltage range is also restricted. When the input voltage is near

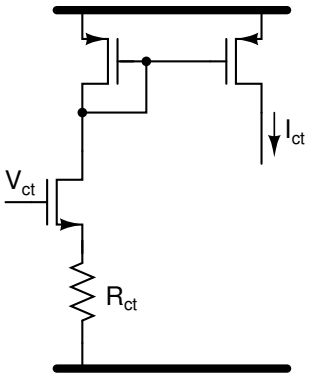
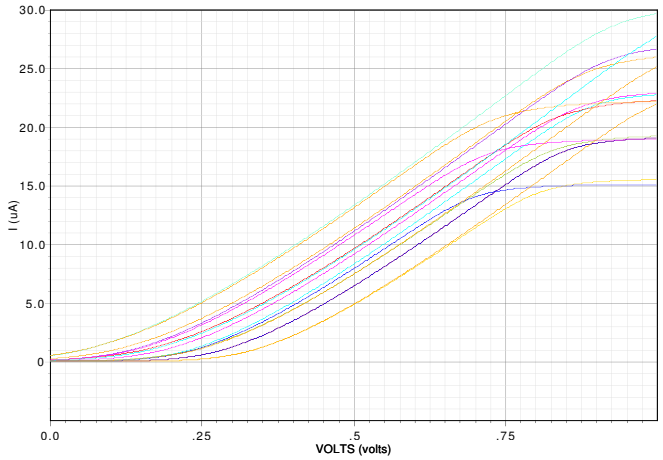
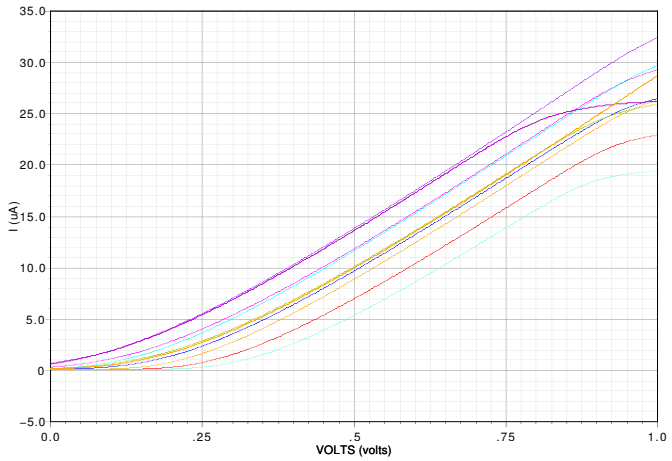


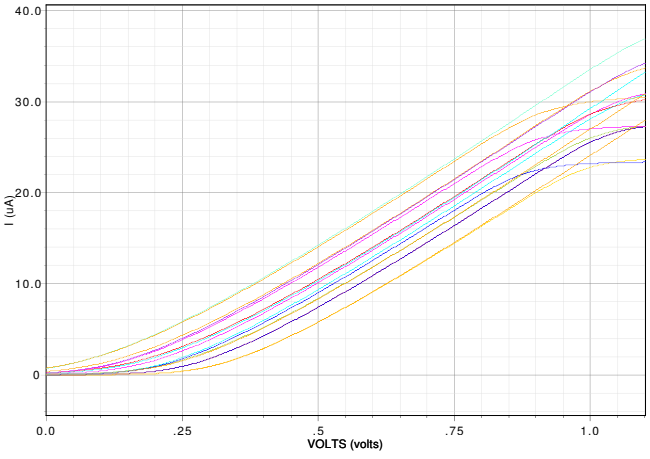
Figure 4.7: Traditional voltage-to-current converter



(a) $V_{DD} = 0.9\,\mathrm{V}$



(b) $V_{DD} = 1\,\mathrm{V}$



(c) $V_{DD} = 1.1\,\mathrm{V}$

Figure 4.8: Output current of the V/I converter of figure 4.7

to V_{DD} transistor M_1 enters in the triode region, but the feedback loop is still closed and the current that flows across the resistance corresponds the given by equation (4.4); so, when transistor M_2 attempt to copy the current of M_1, if it is the triode region the output current does no correspond to that flowing through the resistance.

Taking into account the drawbacks that traditional V/I converters have in both input dynamic range and variability with PVT, figure 4.10 shows the proposed voltage-to-current converter, with is based on the circuit of figure 4.9, but the resistance that defines the gain is connected between the drain of transistor M_1 and a low-impedance node instead ground. Transistors M_{a1}, M_{a2}, M_{a3} and M_{a4} conforms the auxiliary amplifier of figure 4.9, while transistors M_2, M_3, M_4 and M_5 forms the low impedance node; M_2 and M_3 are part a low voltage cascode mirror, so that through the feedback loop between the gate of M_2 and the drain of M_3, the input impedance seem at the source of M_3 is low.

With the circuit of figure 4.10 a rail to rail operation is reached because the current of M_1 is not copied by another transistor, this current is summed to another branch with some quiescent current. For that reason, no matter that M_1 enters in the triode region, the current that is summed to the circuit corresponds to:

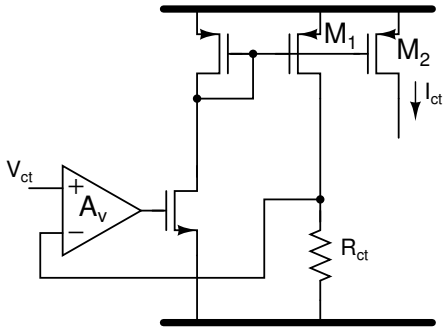


Figure 4.9: Improved voltage-to-current converter

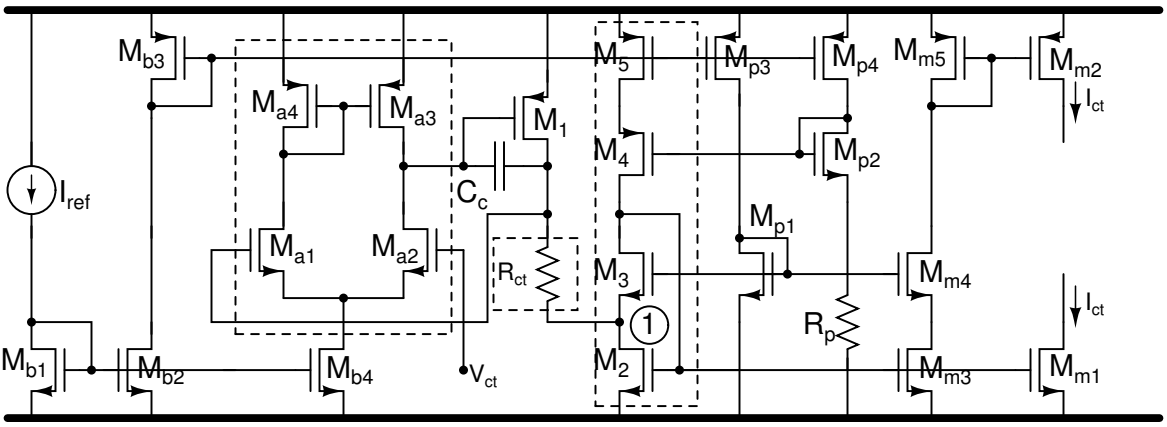


Figure 4.10: Proposed voltage-to-current converter

	Type	Width	Length	Multiplicity
M_{a1-a4}	Body-Contact	1.3 µm	56 nm	10
M_1	Body-Contact	1.3 µm	232 nm	15
M_{2-3}	Body-Contact	1.3 nm	112 nm	10
M_{4-5}	Body-Contact	1.3 nm	112 nm	12
M_{p1}	Body-Contact	1.3 nm	232 nm	2
M_{p2}	Body-Contact	1.3 nm	232 nm	5
M_{p3-p4}	Body-Contact	1.3 nm	112 nm	10
M_{b1-b4}	Body-Contact	1.3 nm	112 nm	15
M_{m1-m5}	Body-Contact	1.3 nm	112 nm	20
I_{ref}	25 µA			

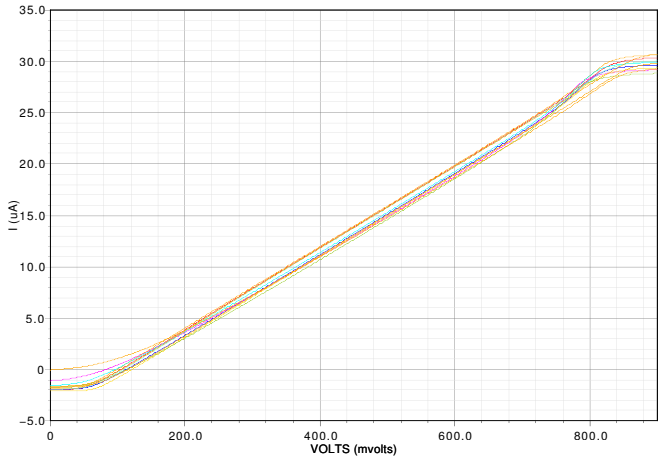
Table 4.2: Transistor's dimensions of the voltage to current converter

$$I_{ct} = I_{ref} + \frac{V_{ct} - V_1}{R_{ct}} \tag{4.5}$$

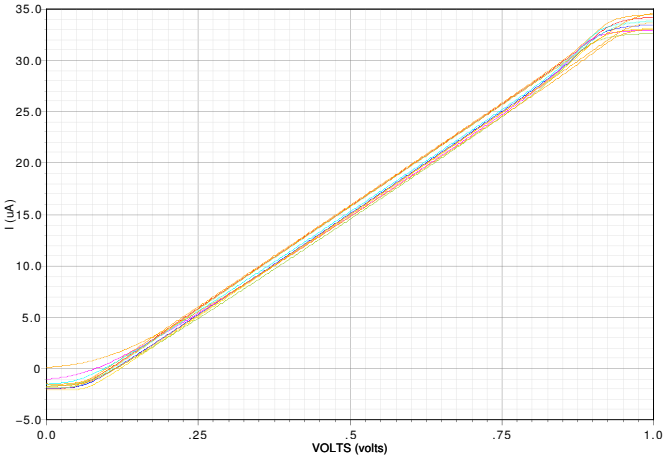
where V_1 is the DC level of the low impedance node.

The main drawback of this implementation is to keep as constant and low as possible the DC level of node 1 to PVT variations. For this, the gate of the transistor is bias by a diode connected device M_{p1}. When process or temperature variations reduce the V_{th} of transistors, the DC level of node 1 tends to be higher, however the gate-source voltage of M_{p1} decreases, so that forces node 1 to return to its original level. A variation of 25 mV over all the corners and operation conditions is achieved, for a DC level of 75 mV.

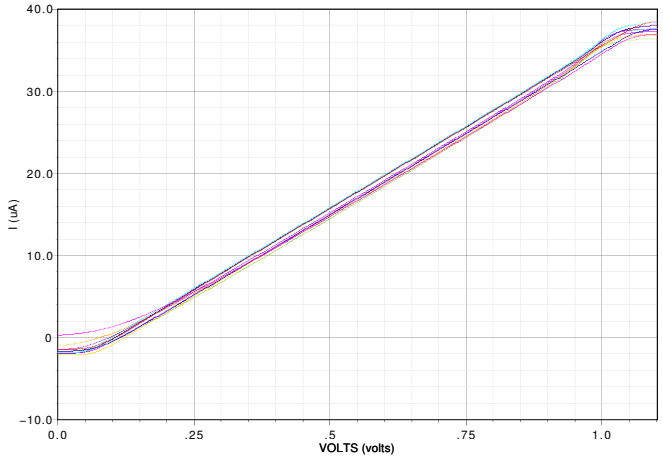
Figure 4.11 shows the output current of the circuit for for all PVT variations. An almost rail to rail operation is achieved, limited by the input excursion range of the auxiliary amplifier mainly. Also, a variation of less than 0.5% is obtained for the gain of the converter attributed to the thermal coefficient of the resistor, with proves the robustness of the circuit to PVT. Table 4.2 presents the dimensions of the transistors that form the V/I converter.



(a) $V_{DD} = 0.9\,\mathrm{V}$



(b) $V_{DD} = 1\,\mathrm{V}$



(c) $V_{DD} = 1.1\,\mathrm{V}$

Figure 4.11: Output current of the V/I converter of figure 4.10

4.3 Compensation network

Despite the oscillator is controlled by a current, which reduce the variation of its tuning gain with PVT, its free running frequency is still very sensitive to theses variations. For that reason, a compensation method that adjust the bias current of the oscillator according to the operation condition is needed. It is important to note that the voltage variations are not taken into account for the oscillator because it is assumed that it is connected to a voltage regulator; the following reason support this assumption:

- The supply voltage of a ring oscillator has a big impact in the amplitude of the oscillation, no matter if it is controlled by a voltage or a current. For that reason, the phase noise and jitter are functions of the supply voltage too. The higher the amplitude of the oscillation, the smaller the impact of the noise source of the transistors on the oscillation frequency. If there is some restriction over this parameters, it must be necessary to over-design the circuit so that those are met in the worst case for the supply voltage. This over-design implies an increment in the power consumption and area of the circuit.

- All the noise coupled to the power supply (for instance a battery) of the circuit is directly injected to the oscillator, so that phase noise an jitter are degraded too.

- In general, it would be desired that all the PLL is supplied by a regulator instead by the battery directly. A regulator has a finite bandwidth, wherefore it serves as a filter for the high frequency noise that could be coupled.

Consequently, the proposed compensation circuit adjust the bias current of the ring based on the operation temperature and fabrication condition. Figure 4.12 shows the variation of the free running frequency of the circuit Vs temperature and for all the corner process; a variation of 3.45 GHz —44%— is appreciated. For Fast-Fast process, the ring develops the highest frequency, while for Slow-Slow corner the slowest. For Typical-Typical and cross corners, the circuit achieves an intermediate frequency which is almost the same for the three conditions; the circuit compensates these variations by itself because both PMOS and NMOS transistors are involved in each transition of the cell, so that the differences on their behaviors are compensated. In addition, a CTAT performance for the frequency is present for all corners.

Figure 4.13 shows the behavior of the bias current needed to keep constant the free running frequency of the ring. A PTAT behavior is always present, but its thermal coefficient vary with the process corners; table 4.3 summarizes the needed currents for a fixed frequency of 7 GHz.

The required behavior for the bias current can be obtained with the circuit of figure 4.14. It uses two differential pairs as current switches, which are controlled by a voltage that is only a function of the fabrication process condition and not of temperature; this control voltage senses only when the performances of both types of transistors vary in the same proportion,

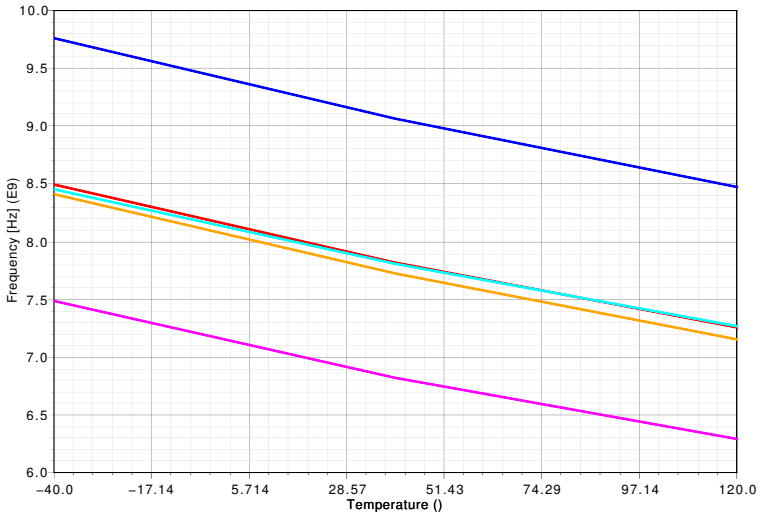


Figure 4.12: Variation of the free-running frequency of the oscillator with process corners and temperature

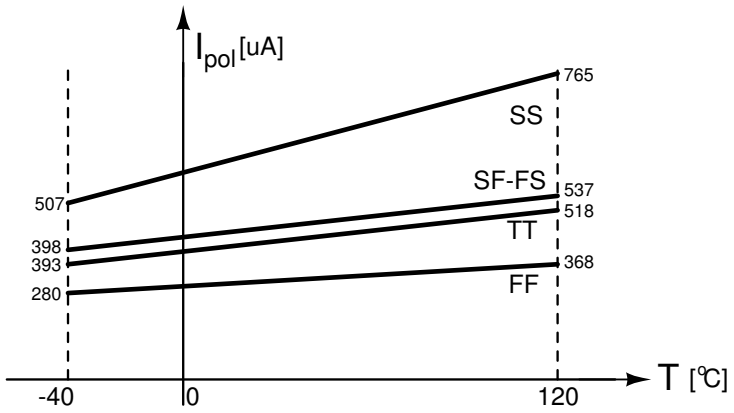


Figure 4.13: Needed currents to compensate the free-running frequency of the ring oscillator

	TT	FF	SS	FS	SF
−40 °C	393 µA	280 µA	507 µA	398 µA	398 µA
60 °C	450 µA	327 µA	610 µA	460 µA	453 µA
120 °C	518 µA	368 µA	765 µA	537 µA	518 µA
T_c	781.2 nA/°C	550 nA/°C	1.61 µA/°C	868.8 nA/°C	750 nA/°C

Table 4.3: Needed behavior of the bias current of the ring oscillator

because, as was said before, the cross corners are compensated by oscillator itself. The tail current of each pair is a PTAT function that satisfies the conditions for the Fast-Fast corner —first pair—, and for the Slow-Slow corner —second pair—, as figure 4.13 shows. The compensation works as follows: if the corner FF is present, all the tail current from the first

pair is directed to the transistor M_1 and the current from the second pair to M_2, so that the ring is biased with I_{FF}; in the same way, if the SS corner is present, the oscillator is biased with I_{SS} only. When a Typical case or cross corners are presented, the half of the current of each pair is directed to M_1 and M_2, so that the ring is biased with the mean of the two tail currents $(I_{FF} + I_{SS})/2$. If any other process condition is presented, the required amount of current from each pair will be directed to M_1 so that the free-running frequency is kept constant. Finally, I_{FF} and I_{SS} currents are generated by a bandgap core and a reference current, as figure 4.15 shows.

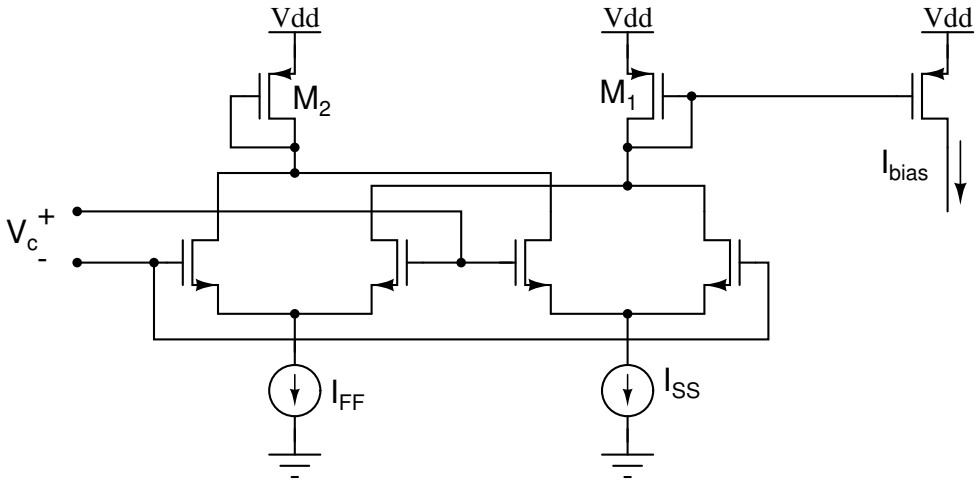


Figure 4.14: Generation of the bias current of the oscillator

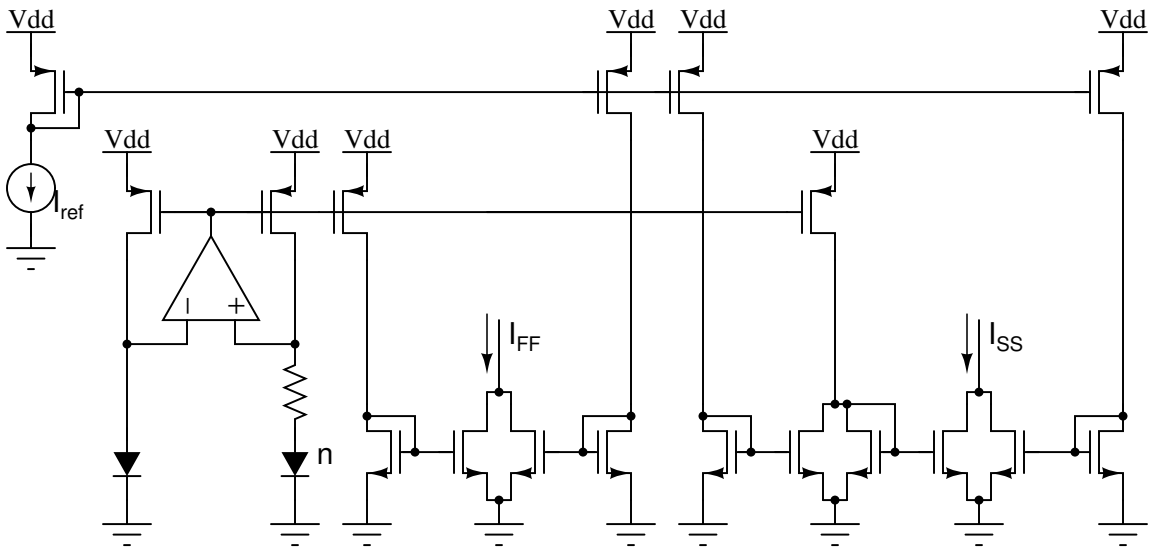


Figure 4.15: I_{FF} and I_{SS} generation

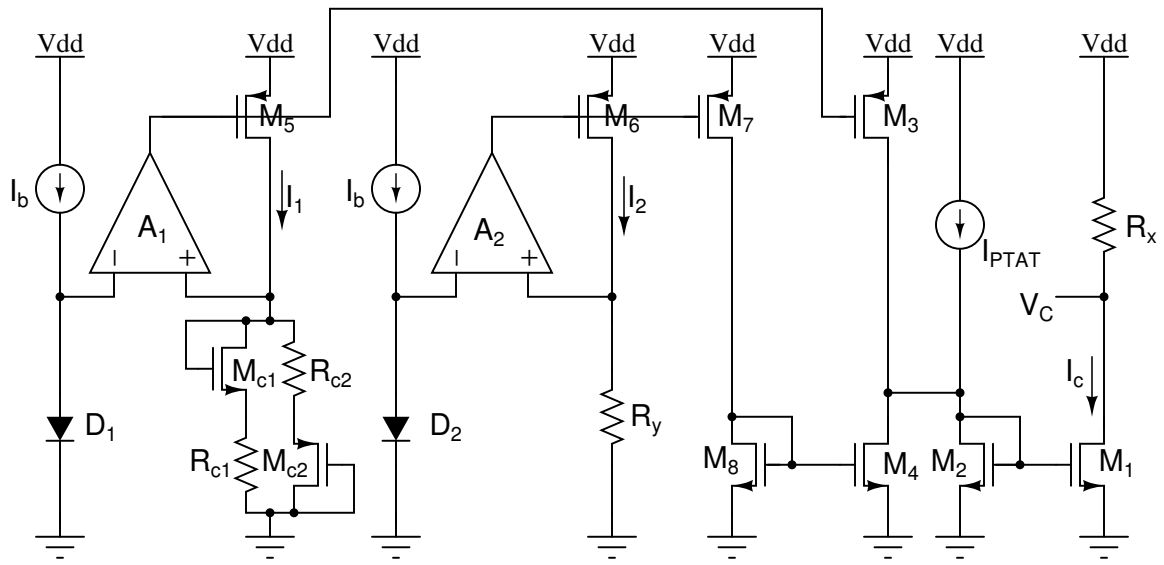


Figure 4.16: Generation of the compensation voltage V_c for the control of the bias current of the oscillator

To generate the compensation voltage, the circuit of figure 4.16 is implemented. It uses two CTAT cells to generate two different currents: one that has a well defined behavior with temperature —same thermal coefficient— and different offset with respect to the fabrication process corner (I_1), and another that has a constant thermal coefficient as well but no dependence with process corners (I_2). Hence, if this two currents are subtracted, a temperature-independent current that vary only with the fabrication process condition is obtained:

$$\begin{aligned} I_1 = K_1T + K_2 \rightarrow \text{With } K_1 \text{ constant and } K_2 \text{ process sensitive} \\ I_2 = K_3T + K_4 \rightarrow \text{With } K_3 = K_1 \text{ and } K_4 \text{ constant} \\ I_C = I_1 - I_2 = (K_1 - K_3)T + K_2 - K_4 = K_5 \rightarrow \text{Process-sensitive current} \end{aligned} \tag{4.6}$$

Finally, the compensation current is converted to a voltage by a resistance for example.

Transistors M_{c1} and M_{c2} of the circuit from figure 4.16 are included in a classic CTAT cell to generate different current offset with respect to the fabrication process. It is important to make emphasis that the current offset changes only when the performance of both transistors M_{c1} and M_{c2} vary in the same proportion because their parallel connection, so that if opposite variations are present, the current offset keeps constant. The resistances R_{c1} and R_{c2} are used to degrade the current of both transistors and improve the linearity of the output current. In addition, figure 4.16 shows an additional PTAT current connected to the subtraction node, to reduce even more the dependence with temperature of the output current; this PTAT current is derived from the same bandgap core of figure 4.15. Finally, the compensation current is converted to a voltage by the resistance R_x.

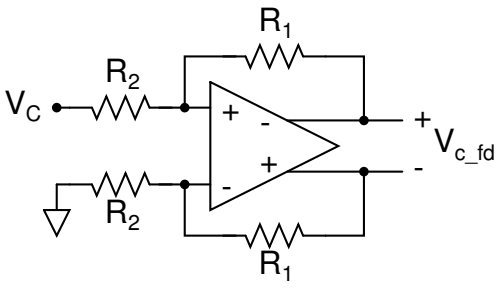


Figure 4.17: Single-ended to Fully-differential converter

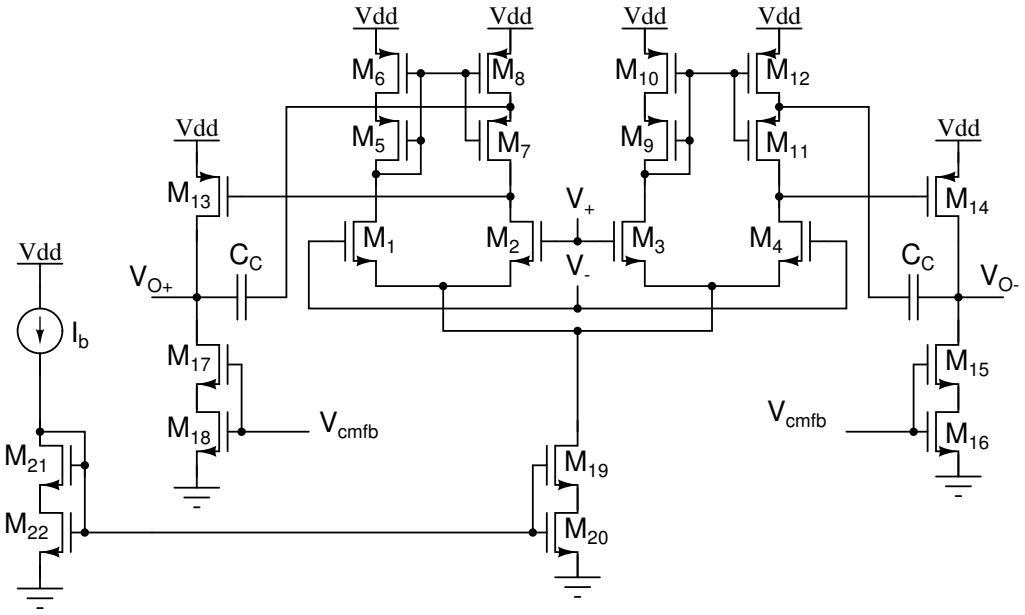


Figure 4.18: Proposed fully-differential amplifier

Nevertheless, the output voltage of the compensation circuit is singled-ended type, but a fully differential signal is needed to control the differential pairs of figure 4.14. For that reason, a singled-ended to fully-differential converted is used, which consists in a fully-differential amplifier inside a feedback loop (figure 4.17). The amplifier is implemented with the proposed circuit of figure 4.18. It uses two singled-ended differentials biased by only one current as its first stage; the robustness to PVT is achieved through the use of this pairs, due to the following reasons: a singled-ended differential pair with a current mirror as its load always tries to make equal the voltages of both drains of its input transistor, due to the symmetry of the circuit; so, taking into account that one drain is connected to a low impedance node —diode connected transistor— the sensitivity to PVT of its voltage is low, for that reason the sensitivity of the output node is low too, leading that parameters such as transconductance and output resistance keep almost constant. Another advantage of the proposed topology is that the input signal has always two paths to the second stage: one that pass across a low impedance

	Type	Width	Length	Multiplicity
M_{1-4}	Body-Contact	1.3 µm	56 nm	15
M_{5-12}	Body-Contact	1.3 µm	232 nm	15
M_{13-14}	Body-Contact	1.3 nm	232 nm	12
M_{15-18}	Body-Contact	1.3 nm	232 nm	15
M_{19-22}	Body-Contact	1.3 nm	232 nm	15
I_{ref}	35 µA			

Table 4.4: Transistor's dimensions of the proposed fully-differential amplifier

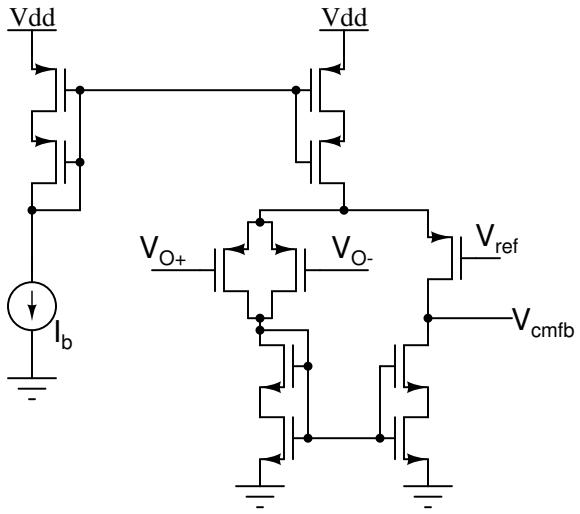


Figure 4.19: Common-Mode Feedback for the proposed fully-differential amplifier

node and other that injects current to a high impedance node directly, so that the variations of each path are compensated by the other. The second stage of the amplifier is a common source topology with active load. Due to the amplifier is a fully differential circuit, it requires a Common-Mode Feedback loop, which is shown in figure 4.19. In addition, body-contact compound transistors are used is all the current mirrors and active loads of the circuit. The frequency response of the amplifier is shown in figure 4.20; it achieves a gain of 65 dB and a GBW of 250 MHz for the typical operation condition, 63 dB and 180 MHz for worst operation case, and 67 dB and 300 MHz for best operation case; the power consumption is 210 µW for typical condition. Table 4.4 presents the dimensions of the devices that form the proposed amplifier.

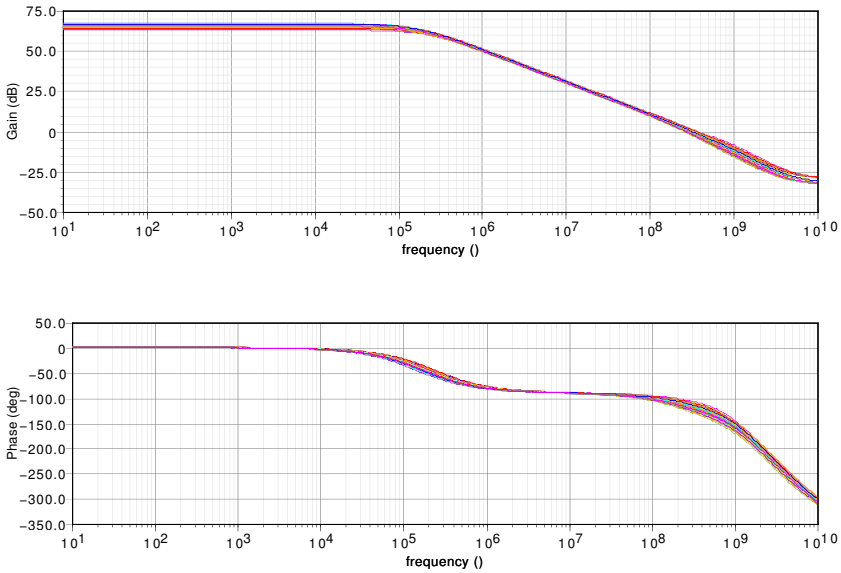


Figure 4.20: Frequency response of the amplifier of figure 4.18

4.4 Simulation results of the robust ring oscillator

Figure 4.21 shows the process-sensitive current with a low dependency of temperature. The difference between the SS and FF currents is 13.75 µA, while between typical and cross corners is 0.2 µA; this proves that the compensation circuit responds when the performance of both types of transistors vary in the same proportion and direction: both get fast or both get slow. In addition, figure 4.22 shows the compensation voltage applied to the singled-ended to differential converter; this voltage has a thermal coefficient of 112 µV/°C for the typical operation case.

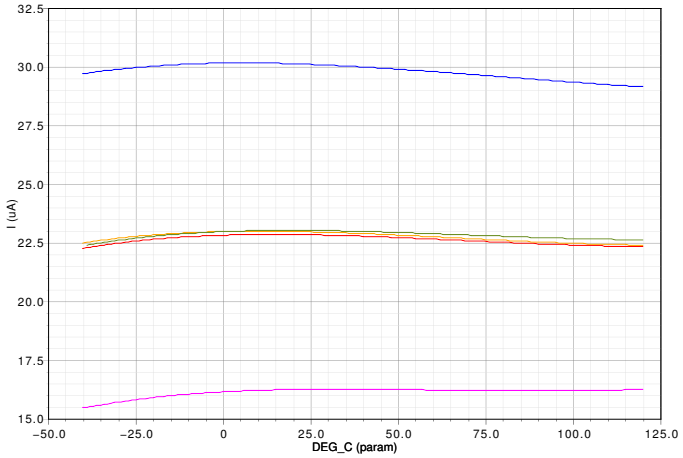


Figure 4.21: Process-sensitive current with low dependence of temperature

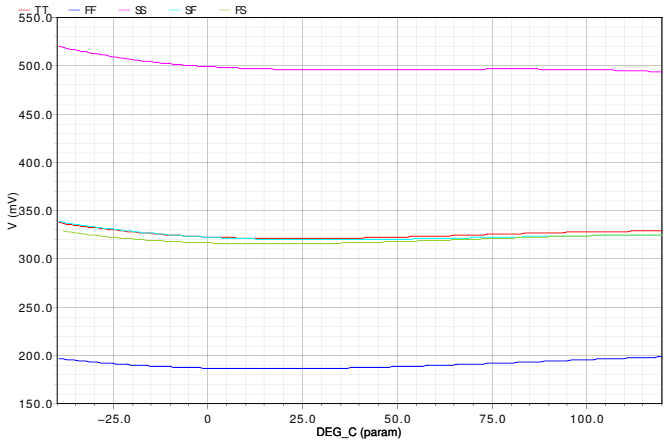


Figure 4.22: Process-sensitive voltage with low dependence of temperature

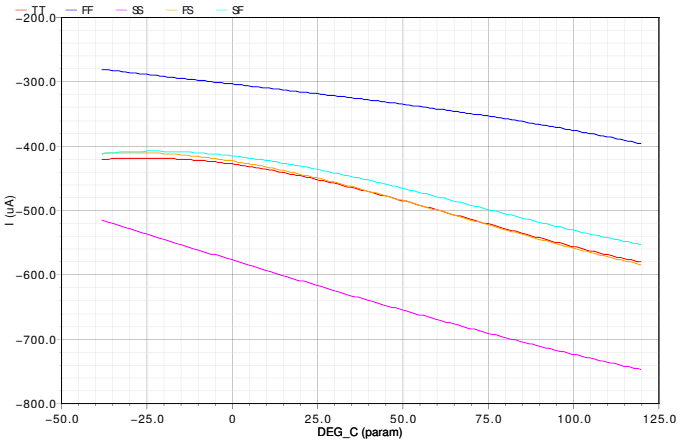


Figure 4.23: Bias current for the compensated ring oscillator

Figure 4.23 shows the bias current of the oscillator that was generated with the explained circuits. A high-order behavior with temperature is seem because the thermal coefficient of the voltage that controls the two differential pairs is no zero or constant. However, the required current are meet with an maximum error of 8.2% for the typical case.

Finally, figure 4.24 shows the tuning curve for temperature and process variations. A maximum difference of ±210 MHz, which means 2.91% only, over 7.2 GHz can be appreciated. Moreover, the input control voltage range is approximately 75 mV for the lower limit and 920 mV for the upper limit for all the operation conditions. Furthermore, the duty cycle of the output is 50% with a variation of ±2%. Table 4.5 summarizes the obtained results, while table 4.6 compares this design with others presents in the literature.

		TT	FF	SS	FS	SF
Frequency [GHz]	−40 °C	7.09-7.55	6.82-7.54	6.94-7.33	6.96-7.39	6.98-7.42
Ctrl Volt [mV]		72-920	70-919	75-927	75-854	75-909
Gain [MHz/V]		542	848	457	551	527
Duty cycle [%]		49	50	51	50.5	49.5
Frequency [GHz]	60 °C	**7.14-7.53**	6.93-7.4	7.11-7.42	7.06-7.44	6.99-7.38
Ctrl Volt [mV]		**71-925**	74-920	71-925	75-859	76-924
Gain [MHz/V]		**456**	555	362	484	459
Duty cycle [%]		**50**	50.5	51	50	49
Frequency [GHz]	120 °C	7.28-7.61	7.16-7.57	7.00-7.26	7.2-7.52	7.15-7.49
Ctrl Volt [mV]		76-923	106-927	79-925	88-856	79-930
Gain [MHz/V]		389	499	307	416	399
Duty cycle [%]		50.5	50	49.5	51	49

Table 4.5: Tuning ranges of the compensated ring oscillator for all the operation conditions

Author	[24]	[25]	[26]	[27]	This work
Year	2006	1999	2009	1999	2012
Technology	0.25 µm	0.6 µm	90 nm	0.35 µm	45 nm
Central frequency	7 MHz	680 kHz	1.22 GHz	2 GHz	7.2 GHz
Freq variation	±2.64%	±4.7%	±4.1%	±1.7%	±2.9%
Temp range	−40, 120 °C	35, 115 °C	−40, 120 °C	0, 100 °C	−40, 120 °C
Power	-	0.4 mW	-	-	4.7 mW

Table 4.6: Comparison with others process and temperature compensated ring oscillators

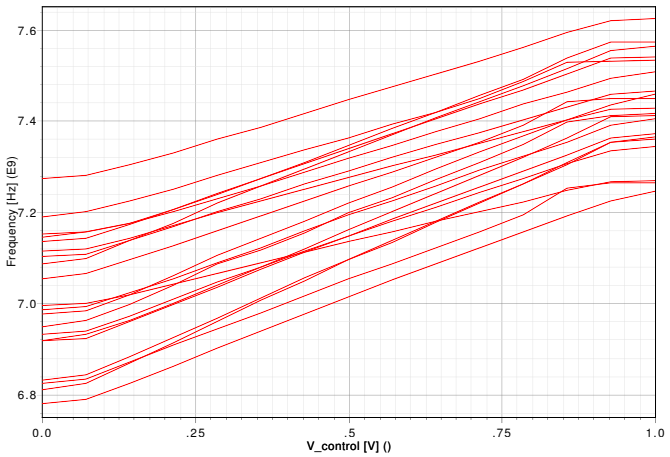


Figure 4.24: Tuning curves of the compensated ring oscillator

4.5 Summary

In this chapter the design of process and temperature compensated ring oscillator was addressed. First, the influence of history effect on the oscillation frequency is explained; it was showed how history effect introduces a time constant higher than the settling time of the PLL, as well as degrades the jitter and phase specifications, for that reason body-contact transistor are used in the core of the oscillator. Then, the advantages and disadvantages of different control methods for the frequency of the ring as well as types of delay cell were explained; pseudo-differential current-controlled ring oscillator was selected because of its linear and low-sensitivity tuning gain. Furthermore, some design considerations about rail-to-rail V/I converter with robust performance were given. Then, with the aim of compensated the free-running frequency of the oscillator to process and temperature variations, a bias network was proposed which modifies the bias current of the ring based on the operation condition. Finally, simulations results of the oscillator were presented, in which a variation of $\pm 2.91\%$ in the central frequency is obtained over 7.2 GHz.

CHAPTER 5

SIMULATIONS RESULTS OF THE PLL

In the last two chapters the design of each component of the PLL with low sensitivity to PVT was explained, and their performance were proved by separated each one. In this chapter, all those ones are merged into only one circuit to build the PLL. The transient behavior of the PLL to small frequency changes that allows the circuit works in its linear region is characterized, as well as its noise performance. Moreover, a comparison with other PLLs is made, in order to position the design in the state of the art. Then, some conclusions about all the design process and results are made, as well as some recommendations for future works.

5.1 PLL performance characterization

The architecture of the designed PLL is shown in figure 5.1. It has only one direct loop to control the oscillator, so that the need of any control logic is avoided. Each block corresponds to those described in chapters three and four.

The compensation and biasing network of the oscillator does not interfere in the behavior of the PLL on account that it is an open-loop control system which sense parameters —process and temperature— which change rates are about seconds or minutes.

The division factor of the frequency divider is set to 32, according to the bandwidth and slew rate restriction of the output amplifier of the charge pump; the divider is implemented by a behavioral description using Verilog-A because the focus of this works was only to design the analog blocks of the PLL. The stabilizing zero is located at $s = 33$ Mrad whereby the PLL is stable for all the operation conditions. An additional capacitor is connected in parallel with the zero branch in order to reduce the ripple of the control voltage; this capacitor introduces a high-frequency pole that does not affect the transient behavior of the circuit.

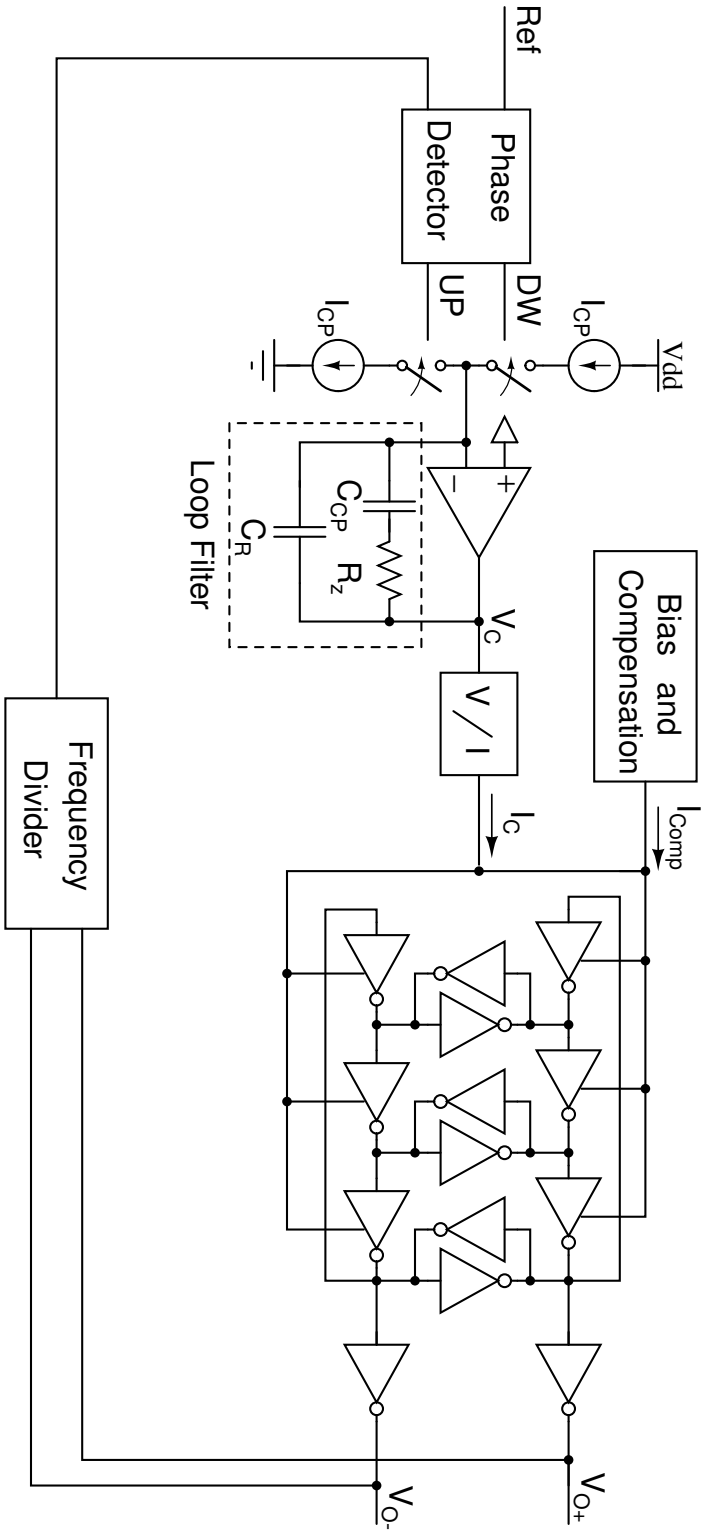


Figure 5.1: Architecture of the designed PLL

As was explained in chapter two, the main characteristic of a robust PLL is to have a constant bandwidth no matter the operation condition, whereby the transient behavior and noise performance keep constant. A way to estimate the bandwidth of a PLL is to measure the settling time and overshoot of the control signal of the oscillator and then calculate the damping factor and natural frequency of the circuit:

$$OS = e^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}} \qquad t_s = \frac{4}{\zeta\omega_n} \tag{5.1}$$

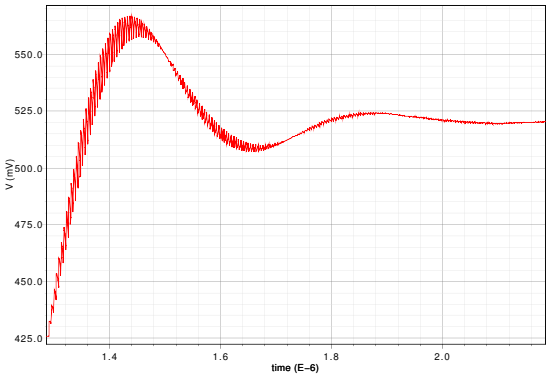
Nevertheless, it is important to highlight that at the startup of the PLL, the transient response to acquire the lock state for a first frequency corresponds to a non-linear system because the initial frequency of the VCO is unknown, so that the initial phase and frequency error is so high that the phase detector and loop filter output can saturate [6]. For that reason, to measure the setting time and overshoot at startup is a wrong way to estimate the bandwidth of the PLL.

An alternative to produce the adequate transient response is to lock the PLL in a initial frequency and then change it in a small amount compared with the lock range, so that any signal of the circuit will saturate; for the designed PLL this frequency step corresponds to 50 MHz.

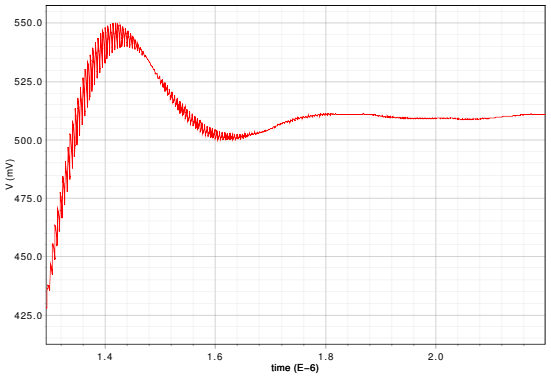
Figure 5.2, 5.3 and 5.4 shows the control signal of the oscillator for a frequency step as was described for all process corners at $-40\,^{\circ}\text{C}$, $60\,^{\circ}\text{C}$ and $120\,^{\circ}\text{C}$ respectively, noting that all of them have a second-order system behavior. Table 5.1 summarizes obtained the settling times and overshots.

Based on data of table 5.1 and equation (5.1), table 5.2 shows the natural frequency and damping factor for each operation case, and figure 5.5 shows the frequency response of the phase-to-phase transfer function. All the possible variations in those parameters are due to the variations in oscillator's gain principally; although it gain is controlled by a current, temperature variation has a strong effect in the current capability of each transistors, wherefore as temperature increases more current is need to obtain the same tuning gain. In addition, the voltage-to-current converter has a finite bandwidth that can introduce additional low frequency poles in the direct loop, which vary with PVT. It is important to note that the results presented are only for process and temperature variations with a constant supply voltage —$V_{dd} = 1\,\text{V}$—, because, as was mentioned in the last chapter, it is not proper to build a PLL without a voltage regulator especially for the oscillator, otherwise jitter and phase noise specifications change dramatically.

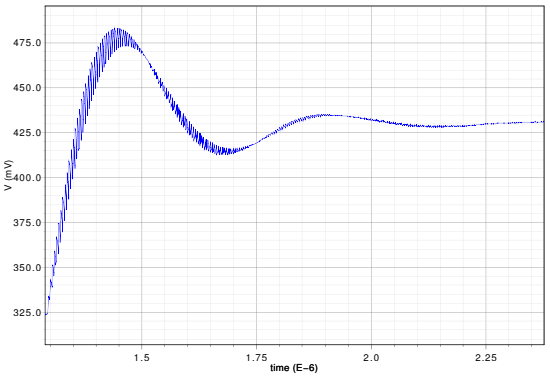
Finally, the lock frequency range of the PLL correspond to the tuning range of the oscillator given in table 4.5 because the control signal of the loop filter has a rail-to-rail operation, and the power consumption is 5.4 mW for the typical case.



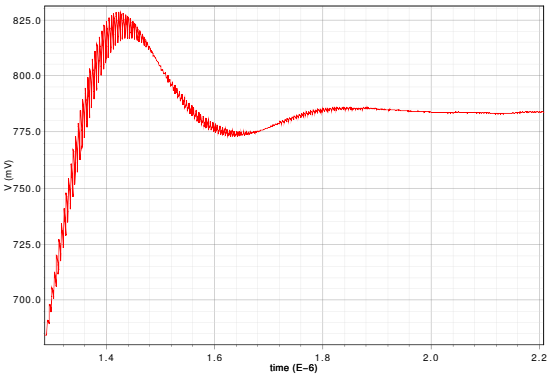
(a) Typical-Typical process



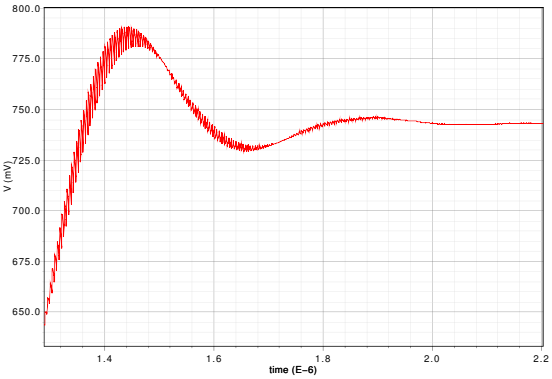
(b) Fast-Fast process



(c) Slow-Slow process

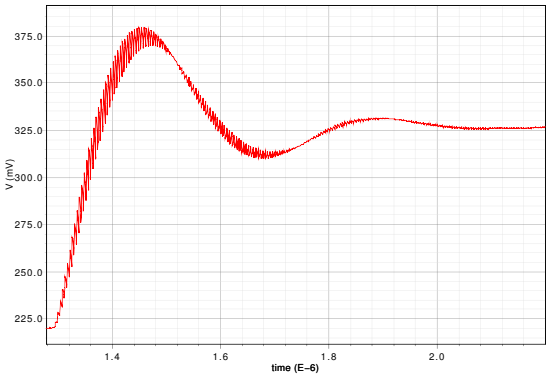


(d) Fast-Slow process

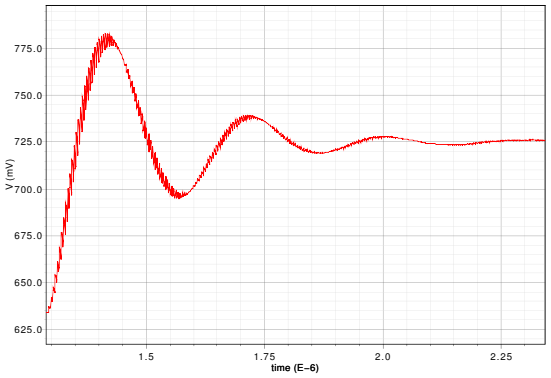


(e) Slow-Fast process

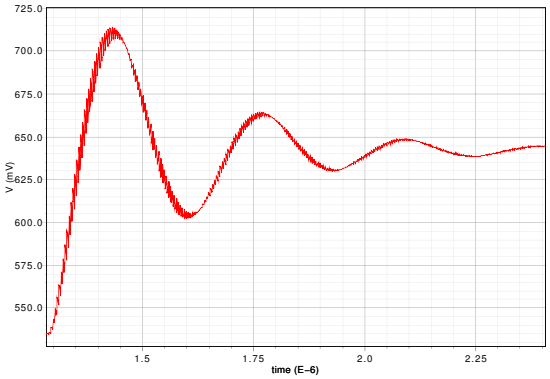
Figure 5.2: Transient response of the PLL for $T = -40\,^{\circ}\mathrm{C}$



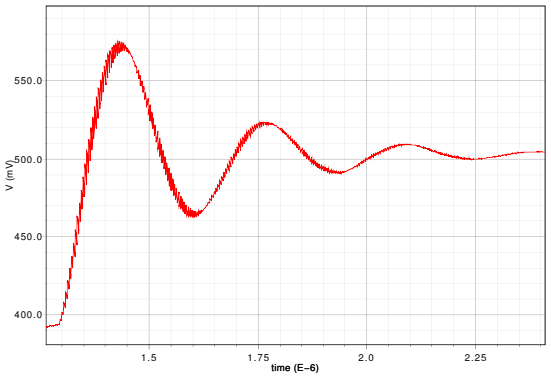
(a) Typical-Typical process



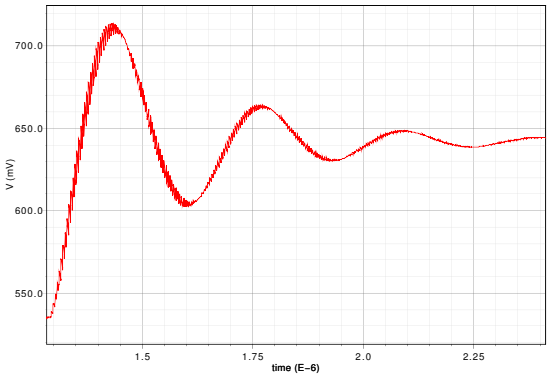
(b) Fast-Fast process



(c) Slow-Slow process

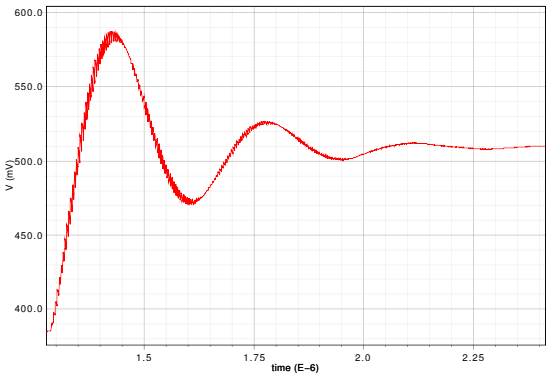


(d) Fast-Slow process

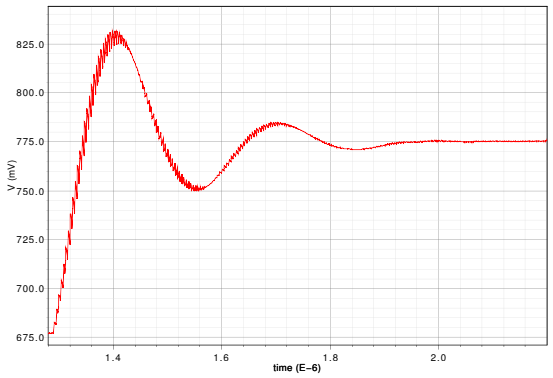


(e) Slow-Fast process

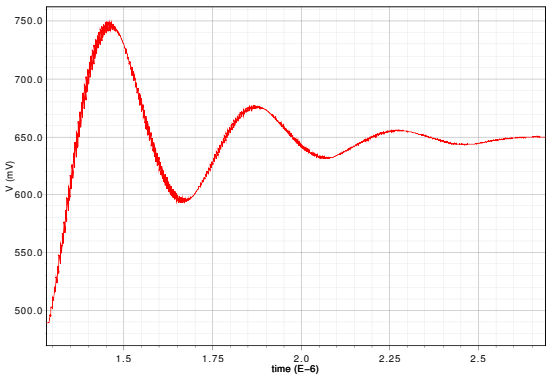
Figure 5.3: Transient response of the PLL for $T = 60\,^{\circ}\mathrm{C}$



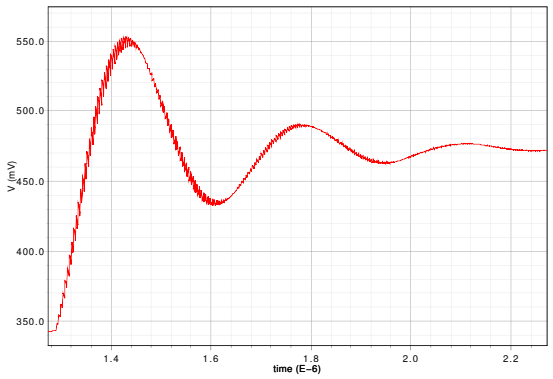
(a) Typical-Typical process



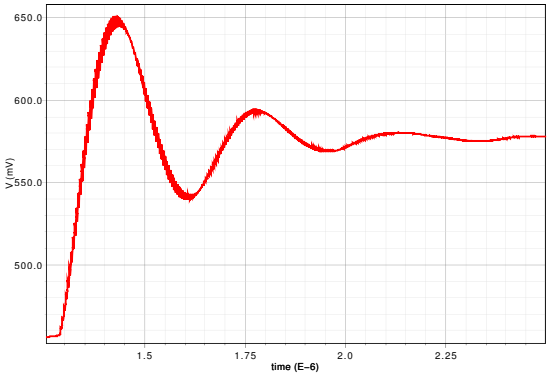
(b) Fast-Fast process



(c) Slow-Slow process



(d) Fast-Slow process



(e) Slow-Fast process

Figure 5.4: Transient response of the PLL for $T = 120\,^{\circ}\mathrm{C}$

		TT	FF	SS	FS	SF
Settling Time [ns]	−40 °C	880	840	970	870	830
Overshoot [%]		38	29	39	31	38
Settling Time [ns]	60 °C	860	970	1120	1110	1100
Overshoot [%]		40	50	52	51	52
Settling Time [ns]	120 °C	1125	770	1130	1020	1170
Overshoot [%]		52	51	56	55	48

Table 5.1: Transient performance of the designed PLL

		TT	FF	SS	FS	SF
ω_n [rad/s]	−40 °C	15.46	13.01	14.36	15.63	15.87
ζ		0.294	0.366	0.287	0.349	0.294
ω_n [rad/s]	60 °C	16.61	19.18	17.59	17.24	17.91
ζ		0.28	0.215	0.203	0.209	0.203
ω_n [rad/s]	120 °C	17.51	23.85	19.55	21.08	15.06
ζ		0.203	0.209	0.181	0.186	0.227

Table 5.2: Natural frequency and damping factor of the designed PLL

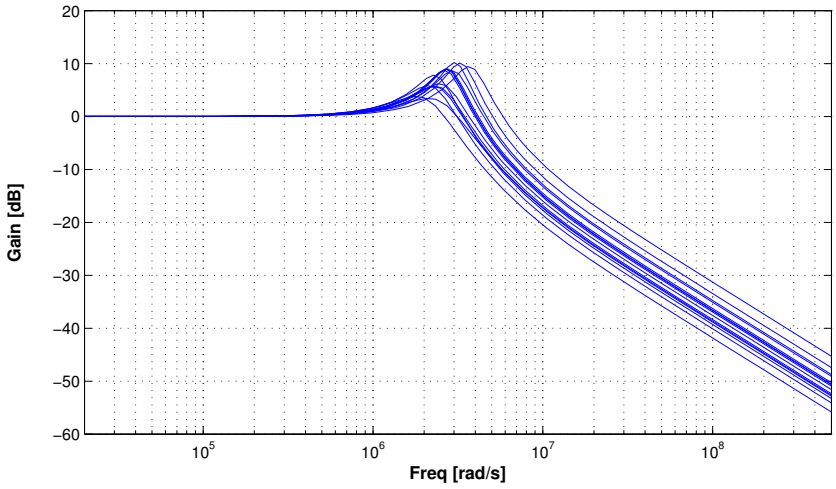


Figure 5.5: Frequency response of the phase-to-phase transfer function of the designed PLL

5.1.1 Noise performance - Jitter

Ring oscillators have a poor noise performance compared with a LC tank or a crystal oscillator. Each active device that form the oscillator is an additional noise source that increase the jitter. In addition, due to that the ring is controlled by a current, all the flicker noise of the control sources is translated to high frequency —oscillation frequency— on account of the commutation of the delay cell [23]. The compensation and biasing network of the ring and the voltage to current converter are also circuits that introduce an extra amount of noise to the circuit, which has to be filtered by the phase-to-phase function to the PLL. For that reason, there is a trade-off between the required extra circuits added to the oscillator —and needed to compensate it— and its jitter.

As was said before, the compensation circuit uses several bandgap references and current mirrors to produce a low-temperature dependence voltage that senses the fabrication process condition; this voltage controls the differential pairs that set the bias current. For that reason, any kind of noise coupled to the compensation voltage will modulate the bias current of the ring, thus increasing the jitter too.

In the same way, with the purpose of increase the robustness of the charge pump, the number of active devices has been increased with the use of an amplifier to drive the output current; noise from those transistors is added to the control voltage directly thus increasing jitter. In addition, highlighting that the body potential of a body-floating transistor is not a constant value (on the contrary, it reach a steady state oscillation), history effect of those devices that form the phase detector and buffers introduce some uncertainty to the commutation threshold and time of each signal of the PLL. For that reason, it is expected that the output signal does not have a high spectral purity.

Some transient simulations that incorporate noise sources where made so as to estimate the jitter of the oscillation. The main advantage of this type of simulation is that all the noise sources of each transistor are taken into account at the same time, as well as their variations in time. In addition, jitter can be measured from the output signal directly, instead by an estimation from a phase noise spectrum. With traditional simulation methods it is necessary to simulated the noise of each block of the PLL by separately; then, based on the transfer function of each component, refer all those noise sources to an output phase noise; finally, jitter is calculated from this phase noise figure based stochastic process theory [23]. This of course is an approximation of the jitter and not all kinds of it —period, cycle to cycle and long term or accumulated jitter— can be measured. With a transient noise analysis jitter measurements can be done from the output waveform directly, wherefore all types of jitter can be measured.

	Period	Cycle-Cycle
RMS [ps]	1.6	0.33
PK-PK [ps]	11.6	3.1

Table 5.3: Jitter measurements of the PLL

	Power [mW]	Frequency [GHz]	Tuning range %	Jitter [ps]	Tech
This Work	5.4	7.2	6	1.6	45nm
[9]	0.94	1.6	100	3.1	65nm
[12]	180	10.2	11.7	-	0.25μm
[28]	28	4.75	100	0.99	45nm

Table 5.4: Performance comparison

Table 5.3 presents the jitter measurements of the output oscillation for the typical operation case. The low bandwidth of the PLL contributes to reduce the noise contribution of all the low frequency components; in addition, the bandwidth of the voltage-to-current converter attenuates the variation of the control current due to the ripple of the control voltage. However, all the compensation circuit contributes to degrade the jitter performance.

Finally, based in the results presented before, table 5.4 compares the performance of the designed PLL with others found in different references.

5.2 Conclusions

In this work the design of a robust to process, voltage and temperature PLL in a nanometer technology was addressed. For this, some design considerations and techniques such as the use of feedback loops, not to the maximum performance of a circuit, and to use a compensation signal were implemented. An output frequency of 7.2 GHz was achieved with a three-stages pseudo-differential current controlled ring oscillator, with a maximum variation of 2.9% for all process corners and temperatures between $-40\,^{\circ}$C and $120\,^{\circ}$C. Based on this, some conclusions about the design procedure can be made:

- Finite-states-machine is the most suitable topology for the phase detector in a nanometer PLL. Its rail-to-rail operation and the low variability of its delay with a static-logic implementation, are appropriated characteristic for a robust PLL. In addition, the reduction in the reset path of both of its outputs with the addition of two nor gates mitigates the difference in the high-to-low transition times, and thus reduces the output spurs.

- With the aim of reduce the impact of the low output resistance of nanometer transistors,

the voltage excursion of the charge pump was restricted by inserting an amplifier at its output node, so that the output voltage is given by it instead of the current sources. Although that this amplifier imposes a restriction in the speed, it reduces the mismatch between the UP and DOWN currents and therefore the output spurs.

- A passive implementation for the loop filter was selected in order to reduce the variability and noise than active networks introduce.
- History effect of silicon-on-insulator body-floating transistor has a strong influence on the settling time of the frequency of a ring oscillator, which can be much greater than the time constant of the PLL. For that reason, body-contact transistors have to be used in all the delays cells of the oscillator.
- A current based control method was used to tune the ring oscillator because it reduces the variability of the tuning gain to PVT and improves its linearity; only one current source was implemented to control all the delay cells so as to reduce the noise contribution.
- A compensation network that adjust the bias current of the ring oscillator and reduce the variability of the free-running frequency was proposed. It uses an arrangement of bandgap sources switched by two differential pairs. These pairs are controlled by a low-sensitive to temperature voltage, that sense the process condition only.
- Taking into account that the jitter and phase noise specifications of any kind of oscillator has a strong dependence of the supply voltage, this parameter was not considered in the compensation network. For that reason, the use of a voltage regulator is needed.

5.3 Future work

Based on the previous conclusion, some recommendations for future works in the same area can be made:

- To do a noise analysis of the compensation network of the ring oscillator, and therefore reduce it jitter contribution.
- To make the layout of the circuit with the purpose to verify the functionality and robustness of the design taking into account all the parasitic elements.
- To do an analysis about the use of a voltage-controlled resistor looking for reducing the variability of the tuning-gain of the oscillator.

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