Development of Low-temperature Ambipolar a-SiGe:H Thin-film Transistors Technology

presented by
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ABSTRACT

Electronic devices and systems fabricated on flexible substrates are growing attention within both the research and the industrial communities. Thin-film transistors (TFTs) based on a-Si:H technology have attracted interest due to potential low-temperature process to be integrated in flexible electronics technology. Although complementary metal oxide semiconductor (CMOS) logic circuits, based on separated n- and p-type doped deposited layers, are currently under development, the use of ambipolar TFTs, operating as either p- or n-type transistors, can simplify the design and reduce the cost for the fabrication of the complementary logic circuits. Hydrogenated amorphous silicon (a-Si:H) has been typically used as the active layer of TFTs. However, due to the preference for unipolar operation (n-type), other materials have been proposed for such applications. An alternative to improve the electrical characteristics of low-temperature ambipolar TFTs is hydrogenated amorphous silicon germanium (a-SiGe:H). Recently, we have demonstrated a-SiGe:H with excellent electronic properties. The a-SiGe:H films show an estimated mobility higher than that of a-Si:H which indicates probably ambipolarity. In this thesis the fabrication and characterization of the ambipolar a-SiGe:H TFTs at 200 °C are presented. Also, the characterization of each one of the films present in the TFT structure in order to obtain the best deposition conditions is presented. Moreover, simulations of the device using physical and spice models are performed to get a comprehensive study on the main transport mechanism of the device.

RESUMEN

Recientemente, los transistores de Película Delgada (TFTs) han resultado atractivos para la industria y la comunidad científica debido a su potencial aplicación en Electrónica flexible y de área grande. La posibilidad de desarrollar circuitos lógicos a bajo costo con un bajo consumo de potencia usando estos dispositivos ha ido adquiriendo mayor importancia. Actualmente, se están desarrollando dispositivos basados en películas separadas tipo n y p como capas activas. Sin embargo el uso de TFTs ambipolares, que operan como transistores tipo n o p dependiendo de la polarización, pueden simplificar el diseño y reducir el costo de fabricación de los circuitos lógicos. El Silicio amorfo hidrogenado ha sido el material mas utilizado como capa activa en TFTs. Sin embargo, debido a su operación unipolar (tipo n) se han buscado otros materiales alternativos para estas aplicaciones. Una alternativa para obtener ambipolaridad a bajas temperaturas (≤200°C) es el Silicio-Germanio Amorfo Hidrogenado (a-SiGe:H). Investigaciones realizadas en el Laboratorio de Microelectrónica del INAOE estiman que la película de a-SiGe:H posee valores de movilidad de electrones y huecos relativamente altos, esto es necesario para obtener ambipolaridad. En este trabajo se describe el proceso de fabricación y caracterización de los TFTs ambipolares de a-SiGe:H a 200°C. Así como la caracterización de las películas que componen el dispositivo, para obtener las mejores condiciones de depósito. Además, por medio de simulaciones se logra comprender los mecanismos de transporte que dominan el funcionamiento del dispositivo.

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CHAPTER 1

INTRODUCTION.

Electronic devices and systems fabricated on flexible substrates are growing attention within both the research and the industrial communities. The development of rollable light-weight displays, flexible solar cells and inexpensive flexible electronics were enabled by the use of flexible substrates. Furthermore, the fabrication cost of electronic devices on flexible substrates can be reduced compared to existing planar or flat-panel technology because the implementation of high-throughput roll-to-roll technology. In this technology, a roll of thin plastic or metal foil used as the substrate can be kilometers long and meters wide compared to a silicon wafer diameter of 10–12'' in integrated circuit technology, or a glass sheet size of about 2m x 2m in a flat-panel display (FPD) manufacturing process [1, 2].

Unlike of the traditional electronics, where the value is added by downscaling the devices, in flexible and large-area electronics the value is added by increasing the fabrication area. This makes the device size requirements more relaxed. Therefore, the equipment cost in flexible electronics is lower, and a larger part of the product costs falls onto the materials with a wide variety of electronic materials that can be used in flexible electronics among which we can mention: high-temperature inorganic semiconductors, such as polycrystalline Si (poly-Si), organic semiconductors and low-temperature materials.

Currently, an option to the development of flexible electronics is the transfering of the existing high-temperature semiconductor technology to flexible substrates that can afford higher working temperatures, as metal foils. This move facilitates the use of high fabrication temperature and electronic

materials with improved device performance, as poly-Si. However, high-temperature substrates and high process costs restrict this technology to a limited number of applications, mainly very high added-value products (such as high-resolution displays and high-end radio frequency (RF) ID tags).

On other hand, organic semiconductors are attractive due to its low-temperature and large-area process compatibility. Also, organic semiconductors can be deposited at room temperature by low-cost spin coating or by roll-to-roll technology compatible with ink-jet printing. However, these materials degrade in air, so they need an encapsulation which is based on inorganic thin-film [3]. This encapsulation results in an increase of its cost. Furthermore, the carrier transport in organic semiconductors, such as pentacene, is sensitive to contamination and is strongly interface-dependent demanding very smooth substrates and various interface preparation procedures [4]. All these make the applications for organic semiconductors in flexible electronics a promise for the future.

Another approach to integrate high-performance devices on low-temperature substrates is to reduce the fabrication temperature of thin-film transistors (TFTs) based on inorganic amorphous, nanocrystalline or polycrystalline materials to a level compatible with the thermal budget of the low-cost substrates [5-7]. This approach offers the advantage of a wider variety of substrate materials available, as low-cost plastics or paper. Besides, other lower thermal budget materials can be integrated in the process, such as adhesives or polymers. Moreover, materials science, device physics and equipment are already well established, as in a-Si:H technology.

In summary, development of inorganic amorphous, nanocrystalline, or polycrystalline thin-film technology through the reduction of deposition temperature for being deposited on low-cost flexible substrates seems to be the most promising approach to enable flexible electronics in the near future.

1.1 Low-temperature Thin-film Transistors.

As already mentioned above, Thin-Film Transistors (TFTs) based on a-Si:H technology have attracted interest because its potential for flexible and large-area electronics technology. However, the temperature range used in industrial a-Si:H TFTs technology on Glass is of 300 to 350 °C which is higher than that used on plastic and low-cost flexible substrates. Therefore, it is necessary to reduce the temperature of the fabrication process. It is well know that TFTs fabricated at low-temperatures (≤200°C) have poor stability, higher off-current and higher values of subthreshold slope than those deposited at higher temperatures [5, 6]. Thus, in order to get better performance of Low-temperature TFTs, semiconductors and insulator materials deposited at low-temperatures need further research.

Due to the low maximum working temperatures of most low-cost plastics, the temperature in the fabrication process is limited to the range of 150–200°C [7]. This low temperature severely restricts the process conditions for plasma deposition, sputtering, and photolithography.

The passivation and gate insulators in a-Si:H TFTs are usually based on plasma deposited silicon nitride (SiNx), whereas for poly-Si TFTs, silicon oxide gate insulator is preferred [8]. In order to meet the requirements for a good gate insulator, the gate insulator material has to withstand electric fields of about 2 MV/cm without breakdown, must have good insulating properties and low charge-trapping rate at low electric fields, and should form a high-quality interface with the a-Si:H semiconductor layer (insulator-semiconductor interface). While plasma enhanced chemical vapor deposition (PECVD) SiNx gate insulator technology at ~300 °C is well established, the reduction of its deposition temperature in order to make it compatible with flexible plastic substrates often leads to a material with poor dielectric performance. At low deposition temperatures (below 300 °C), the leakage current through SiNx and SiOx films increases rapidly due to low film mass density [9, 10]. The

oxide mass density can be increased using high-density plasma systems (e.g., electron cyclotron resonance [11]). The maximum deposition area in such systems, however, is limited by 10–12'', which is insufficient for large-area fabrication. Besides, those systems are not conventional in the a-Si:H technology. Despite on this, silicon oxide films (SiO_2) deposited by Spin-On Glass (SOG) at low temperatures results very attractive. Its advantages include a low defect density, low process cost, excellent for planarization applications by filling gaps, and smoothing the surface with multiple coatings. All these using conventional equipment for a-Si:H technology. Thus, in order to improve the insulator-semiconductor interface, insulator materials deposited at low-temperatures require new and alternative deposition techniques.

On the other hand, the requirements for getting a high-quality metal-semiconductor interface are not less complex. In amorphous semiconductors the doping efficiency drops at high doping levels. Le Comber and Spear [12] reported that amorphous silicon prepared by PECVD can effectively be doped by adding small amounts of phosphine (PH_3) or diborane (B_2H_6) to the silane (SiH_4) in the discharge gas. In amorphous semiconductors the donors deliver their electrons to empty states at the Fermi Level (deep states). Therefore, the shift of Fermi level depends on the density of states distribution [13]. Figure 1.1 displays the variation of the dark conductivity with the gas phase concentration of the doping gases [13]. For phosphorus doping the conductivity increases at low doping levels. At higher doping levels, conductivity decreases presumably due to the generation of defect states. For boron doping, conductivity decreases at low doping levels, at higher doping levels it increases and then decreases too. Therefore, the doped film used as contact region for low-temperature TFTs needs to be optimized.

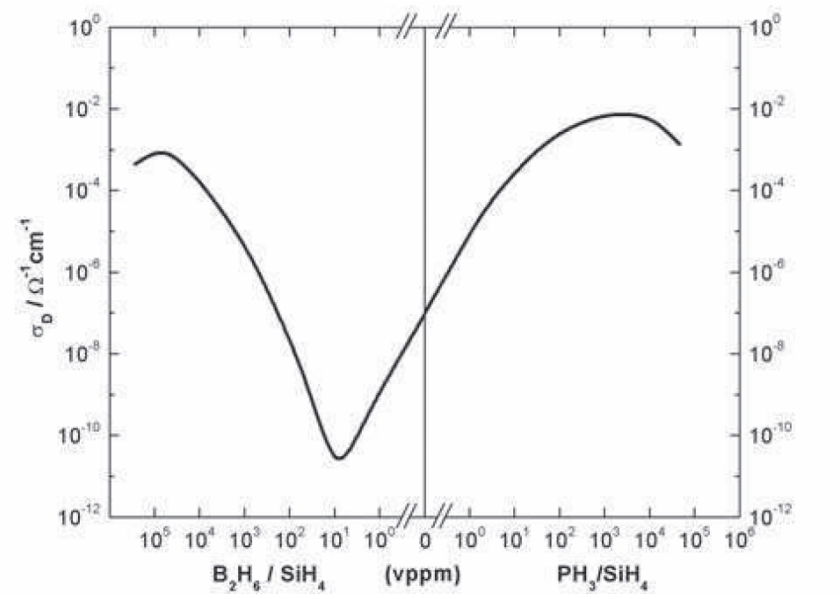


Fig 1.1 Room temperature conductivity of a-Si:H as a function of the dopant concentration in the gas phase [13].

The properties of the active layer obtained at low-temperature also require a hard research. In traditional PECVD a-Si:H TFTs technology, the substrate temperature is in the range of 300–350 °C. Reducing the deposition temperature below 300 °C leads to a change in the deposition mechanisms. The concentration of defects (dangling Si bonds) increases, the mass density decreases, and the doping efficiency drops [14]. The films have low mass density and high charge trapping, and their electronic properties are generally poor [14]. The low temperature can be compensated by using “soft” ion bombardment by light ions (H+, He+) with the energy less than 50 eV, or by producing exothermic chemical reactions [15, 16]. Following this approach, the deposition parameters can be adjusted for low substrate temperature to increase the surface energy and thus to provide the growth conditions similar to those at higher temperatures but without overheating the substrate. For this reason, achieving good quality materials for its use as active layer for low-temperature TFTs is a current field of research.

Since the approach is to use these devices in flexible and large-area electronics technology. The active layer requires higher carrier mobility (both electrons and holes) in order to have better driving current capabilities and enable its use on p- and n-type TFTs. In this application, ambipolar TFTs operating as either p- or n-type transistors, can simplify the design and reduce the cost for the fabrication of the logic circuits.

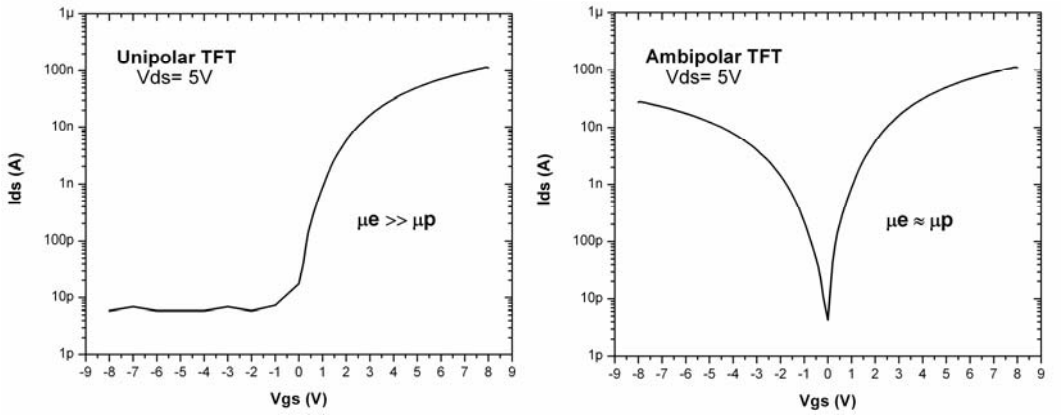
1.1.2 Ambipolar Thin-film Transistors.

The ambipolar behavior is characterized by a superposition of electron and hole currents. As opposed to unipolar silicon metal oxide semiconductor (MOS) devices whose p-type or n-type behavior is determined during fabrication, ambipolar devices can be switched from p-type to n-type by changing the gate bias. Although complementary thin-film CMOS logic circuits, based on separated n- and p-type doped deposited layers, are currently under development [17], the use of ambipolar TFTs can simplify the design and reduce the cost for the fabrication of the complementary logic circuits. Ambipolar and unipolar conductions are illustrated by the transfer curves of TFTs in Figure 1.2. For positive gate bias the transfer characteristic of both ambipolar and unipolar shows an n-type TFT behavior, whereas for negative gate bias only ambipolar shows a p-type TFT behavior. This is due probably, to the relatively same values of mobility for both electrons and holes.

The development of an ambipolar TFT technology requires good quality in both, the formation of source and drain ohmic contacts (metal-semiconductor interface), and the use of a high-quality gate insulator (insulator-semiconductor interface). In previous published results in the literature, the ambipolar behavior has been observed only in devices with a gate insulator based on SiO_2 [18-22]. Therefore, alternative techniques that

allow the deposition of high quality SiO_2 at low temperatures (< 300 °C) are a current field of research.

As previously mentioned, ambipolar TFTs are an alternative to implement low-cost logic circuits. However, due to the preference for unipolar operation (n-type) of a-Si:H TFTs, polycrystalline silicon and other microcrystalline materials have been proposed for such applications. Nevertheless, polycrystalline materials are deposited at temperatures above 450 °C or are obtained using equipment such as an excimer laser which not offers uniformity and are not conventional for a-Si:H technology [23-25]. Therefore, Development of Low-temperature ambipolar TFTs based in a-Si:H technology (taking the advance in the materials science, equipment and device physics well established) can be an alternative to establish the fabrication of low-cost Logic Circuits to use on Flexible and Large-Area Electronics.



a) b)

Fig 1.2 Transfer curves for a) Unipolar TFT and b) Ambipolar TFT.

Since conventional analog and digital circuits are based on unipolar devices, the ambipolar behavior was initially considered undesirable and several techniques were applied to suppress this behavior [26, 27]. However, recent work has shown that the ability to control device switch from p-type to n-type presents new design opportunities in both analog and digital domains.

1.2 Hydrogenated amorphous Silicon Germanium.

An alternative to improve the electrical characteristics of low-temperature ambipolar TFTs without increasing the deposition temperature is hydrogenated amorphous silicon germanium (a-SiGe:H). This film is barely used as active layer for TFTs, since a high content of germanium increases the density of states (DOS) in the films. However, a low incorporation of germanium improves some properties of the amorphous films [28-30]. Recently, we have demonstrated a-SiGe:H deposited by Low Frequency (LF) plasma enhanced chemical vapor deposition (PECVD) at 300°C with excellent electronic properties [29, 30]. The a-SiGe:H obtained at 110 kHz with a relation in gas phase [$GeH_4/(SiH_4+GeH_4)$] of 0.10 has excellent electronic properties. For this relation in gas phase, the a-SiGe:H films show an estimated mobility higher than that of a-Si:H. In these films, electron and hole mobilities have been estimated with relatively the same magnitude, which indicates probably ambipolarity. However, for its use on low-temperature ambipolar TFTs, a-SiGe:H films need to reduce the deposition temperature at ≤200°C. As mentioned in the section 1.1, the reduction of deposition temperature below 200 °C leads to the change in deposition mechanisms. Mainly, the concentration of defects (dangling bonds) increases. Therefore, the preparation of high-quality a-SiGe:H films at low temperatures is subject of current research.

1.3 Objectives.

The aim of the thesis is to develop a Low-temperature ambipolar TFT Technology based in a-SiGe:H which can offers the advance of a-Si:H technology with an ambipolar behavior and higher carrier mobility. All these using low fabrication temperatures and equipment which is conventional for

the a-Si:H technology. To success on this objective, the following goals need to be achieved.

- Good electrical properties in a-SiGe:H films at 200°C.
- Good quality in metal-semiconductor interface. In order to get this target, we propose the use of a light n-type doped amorphous germanium film (a-Ge:H) as source/drain contact layer to obtain ohmic contacts.
- A high quality insulator-semiconductor interface. To get this, we propose the use of Spin-On Glass (SOG) to obtain high quality SiO_2 films at 200 °C.
- The simulation of the device using physical and spice models to get a comprehensive study on the transport mechanism.

In the following chapter the physics and electrical characteristics of ambipolar TFTs (valid also for Unipolar) are studied. In chapter 3, the characterization of each one of the layers present in the TFT structure is presented and discussed. Then, in chapter 4, the development of the low-temperature ambipolar a-SiGe:H TFTs is also presented and discussed. In chapter 5 the simulations and fit of the measured data of the a-SiGe:H TFTs are analyzed. Finally, the conclusions of the thesis are presented.

CHAPTER 2

PHYSICS OF AMBIPOLAR THIN-FILM TRANSISTORS.

The conduction mechanisms in amorphous TFTs are determined by the properties of the channel material. The electronic properties of amorphous films are largely determined by the density of states (DOS) in the Bandgap. In a-Si:H TFTs, the DOS is responsible for the threshold voltage, the field-effect mobility and the Fermi level position [31]. Although there is a consensus between researchers on the general view of the DOS in amorphous materials, the particular structure of the energy spectrum is not known for most amorphous materials. From the theoretical point of view the problem of calculating this spectrum is enormously difficult. There have been many attempts to deduce the shape of the DOS in amorphous semiconductors by fitting various experimental data using some particular assumptions on the energy spectrum [32]. However, in order to make any conclusions, one should use the appropriate theory and compare its results with experimental data to estimate the shape of the DOS.

2.1 Density of states (DOS) in amorphous films.

For many years, it was thought that the DOS distribution is a stable property of amorphous films. This, however, is not the case. The DOS distribution can vary with doping level, carrier injection, temperature, light absorption or voltage stress. As a result, most of the electronic properties depend on sample treatment and history [33].

The DOS is composed by tail and deep states which are localized. Above the conduction band and beneath the valence band the states are

extended. Theoretical studies led to a model where the transition from extended to localized states occurs sharply at distinct energies εc and εv [34, 35]. Since at εc and εv the carrier mobility is expected to drop by orders of magnitude these energies are called mobility edges.

The tail states are the result of variations of bond length, bond angles and dihedral angles. These are localized in the sense that they have finite amplitude in limited spatial regions only [36]. Deep states are formed as a result of unsaturated Si bonds for which the term “Si dangling bonds” is generally used, these are commonly product from unfavorable deposition conditions. The incorporation of hydrogen in amorphous films saturates dangling bonds and reduces deep states in the DOS [37]. Therefore, good quality hydrogenated amorphous films can be obtained by increasing the hydrogen content. However, it is found that Si-H bonds introduce additional states in the valence band and induce a shift of the valence band edge to higher binding energy [38]. Since the conduction band is less affected by hydrogen bonding, the bandgap of hydrogenated amorphous silicon increases. This may be the main reason why the bandgap of a-Si:H is larger than in crystalline silicon and increases with the hydrogen content.

Numerous experimental techniques have been applied for the investigation of intrinsic and extrinsic defects states, leading to the model represented in figure 2.1 [39, 40]. In this one, the DOS is composed of acceptor-like states (near the conduction band) given by the sum of tail states and deep states, and donor-like states (near the valence band) given by the sum of tail states and deep states. A numerical approximation of the DOS distribution $g(E)$ is given by [39]:

$$g(E) = g_{A1} \exp(E/E_{A1}) + g_{A2} \exp(E/E_{A2}) + g_{D1} \exp(-E/E_{D1}) + g_{D2} \exp(-E/E_{D2}) \qquad (2.1)$$

Where g_{A1} and g_{A2}, are the minimum density of sates of tail-acceptor and deep-acceptor states, respectively, and g_{D1} and g_{D2} are the minimum

density of states of tail-donor and deep-donor states, respectively. While E_{A1} and E_{A2}, are the characteristics energies of tail-acceptor and deep-acceptor states, respectively, and E_{D1} and E_{D2} are the characteristic energies of tail-donor and deep-donor states, respectively.

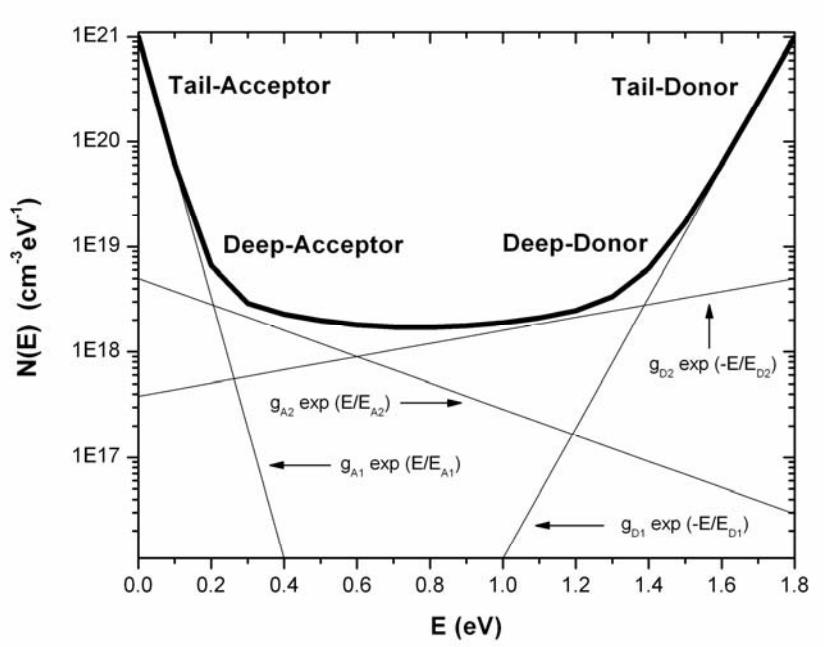


Fig 2.1 Model of the density of states distribution in the bandgap of amorphous films.

Unfortunately the precise structure of the DOS, even in the band tails, is not known for almost all amorphous materials. The whole variety of optical and electrical techniques has not yet proven be able to determine the energy spectrum. Some of the experimental techniques for determining DOS are described in [41]. Although these techniques provide some estimates for the DOS, the problem is still far from its solution. Since the information on the energy spectrum provided by experimental techniques is rather vague, it is difficult to develop a consistent theoretical description of charge transport from first principles. The absence of reliable information on the energy spectrum and on the structure of the wavefunctions in the vicinity and below the mobility edges can be considered as the main problem to describe

quantitatively the charge transport properties of amorphous materials [32]. Observations in experiments led to the conclusion that the DOS distribution in the bandgap of a-Si:H is the result of a chemical thermal equilibrium process. A detailed description of chemical reactions and theoretical concepts basing on thermodynamical arguments can be found in [42].

2.2 Electrical characteristics of ambipolar TFTs.

The figure 2.2 shows the transfer characteristic of typical ambipolar TFTs. For positive gate bias the transfer characteristic shows an n-type TFT behavior, whereas for negative gate bias shows a p-type TFT behavior. From this figure the subthreshold slope, threshold voltage V_T, off-current, on-current and on/off-current ratio for both n-type and p-type are depicted.

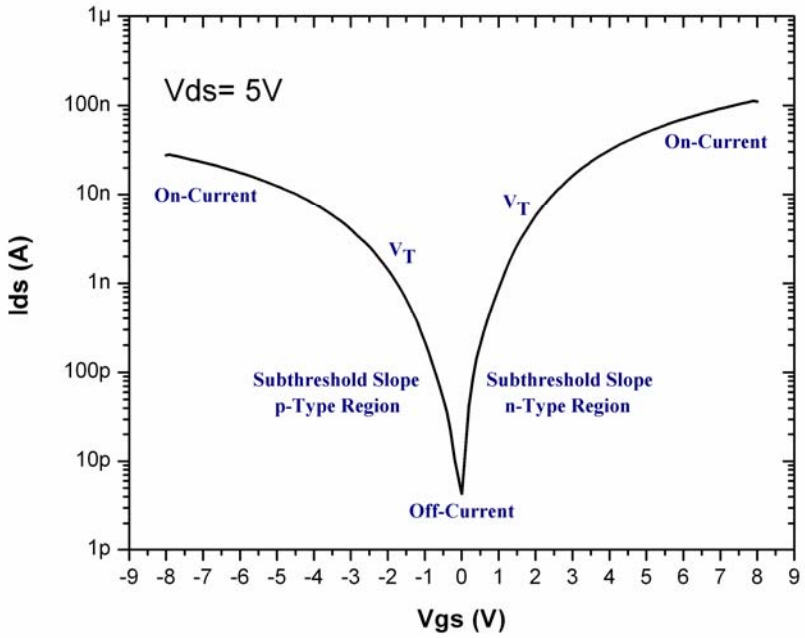


Fig 2.2 Transfer characteristics of ambipolar TFTs.

A low value of the off-current is desirable in order to have a high on/off-current ratio, low values of off-current are easily achieved in a-Si:H TFTs

because of the typically low conductivity of the a-Si:H [43]. In conventional a-Si:H TFTs the on/off-current ratio is almost 6 orders of magnitude [43]. The on-current is limited by the channel conductivity and the contact resistance, and the switching occurs within the range of low Vgs and is characterized by the subthreshold slope $S = [d(\text{Log Ids})/ d\text{Vgs}]^{-1}$. The value of the subthreshold slope should be low enough in order to assure fast transition between on- and off-states. In conventional a-Si:H TFTs the value of subthreshold slope is in the range of 0.4 to 1 V/DEC [44, 45]. It is strongly dependent on the DOS in the channel material near of the gate insulator (insulator-semiconductor interface).

The TFT drain current (in saturation) depends on the gate voltage as:

$$Ids = \mu_{FE} \cdot C_{ox} (W/2L) (Vgs-V_T)^2 \qquad (2.2)$$

Where μ_{FE} is the Field-effect mobility, C_{ox} is the capacitance per unit area of the gate insulator, W and L are the channel width and the length, respectively, and V_T is the threshold voltage. Note that the TFT mobility μ_{FE} extracted from the transfer characteristics using Eq. (2.2) may be significantly affected by the source/drain contact resistance and thus is lower than the real field-effect mobility in the channel. The V_T is defined as the Vgs voltage at which conduction electrons begin to appear in the channel. Low V_T is needed to assure working regime at reasonable low voltage ranges.

The principle of operation of the TFT is as follows, for positive gate bias less than V_T, electrons are induced in the active layer near of the insulator-semiconductor interface. These electrons begin to fill the available deep states, as a result, the Fermi level moves through the deep states which are then occupied. At the same time, some electrons are located in the tail states, but the occupancy of these states is low, since they are well above the Fermi level and so the total charge is dominated by the deep states. The increase in current Ids is due to the small fraction of the electrons in tail states

that are swept by the drain-source voltage Vds. The electrons in the deep states increase in proportion to the increase in gate voltage, but the current increases exponentially. Above the V_T, the deep states are filled and the charge in the tail states exceeds the charge in the deep states. Then, the Fermi level enters in the tail states near of the conduction band but only a small fraction of the induced charge goes into the conduction band. Now, both the total charge and the Ids increase with the applied gate voltage and we have well defined field-effect mobility. This explanation is analogue for valence band and holes at negative gate bias.

The density of states can be determined from the analysis of the transfer characteristic. However, it is usual to make the assumption that the density of states is homogeneous throughout the active layer and that there are no surface states [46]. In reality, there is some evidence that the DOS is not homogeneous. Therefore, the derived DOS reflects contributions from interfaces.

Several models have been reported in the literature in order to characterize the ambipolar behavior of the TFTs from the transfer and output characteristics [18-20, 47]. Since the problem of calculating the DOS is enormously difficult, in the sake of simplicity, it was used the method proposed by B. Wu *et al* [18] to obtain the characteristic energies for the deep localized states of the a-SiGe:H film, the flat-band voltages and V_T among other device parameters for the ambipolar TFTs. This model consists in the calculation and plotting of the parameter M, which is the ratio of the Ids current (at Vds = Vgs) to the transconductance (Eq. 2.3) for both, n-type and p-type regions of the TFT. Two tangential lines are drawn to the M curve, one in the regime below threshold (L1), and another above the threshold regime (L2) (Fig. 2.3). The intercepts of L1 and L2 with the Vgs axis are equal to the flat-band voltage and V_T, respectively. From the slope (S1) of L1, we can obtain the characteristic energies of deep states, E_{A2} from the n-type region and E_{D2} from the p-type region (Eq. 2.4).

$$M = Ids / (dIds/ dVgs) \quad (2.3)$$

$$E_{A2}, E_{D2} = KT /2S1 \quad (2.4)$$

Where K is the Boltzmann's constant and *T* is the temperature in Kelvin.

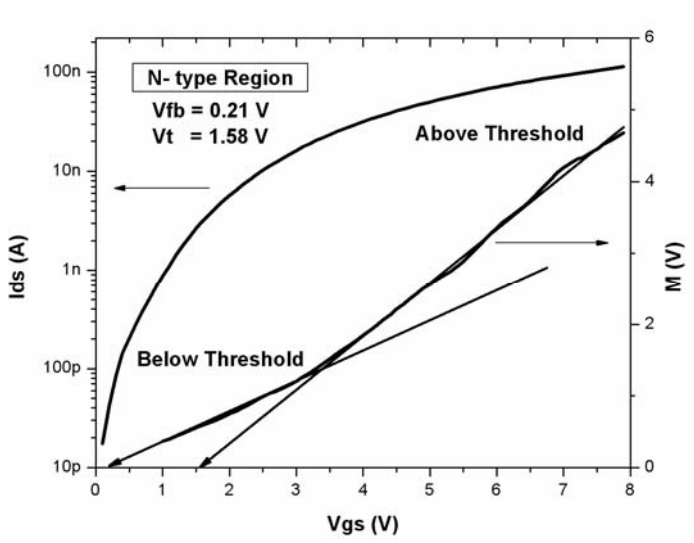


Fig 2.3 Plotting of the parameter M and Ids [48].

Typically, in amorphous TFTs, the subthreshold slope is largely decided by the quality of gate insulator/ active layer interface. In the a-SiGe:H TFT, the subthreshold slope is dependent on the trap density in the active layer a-SiGe:H (N_T) and at the SiO_2/a-SiGe:H interface (D_{it}). The subthreshold slope can be approximated as the following equation [49]:

$$S = qKT (N_T ts + D_{it})/C_{ox} \log(e) \quad (2.5)$$

Where q is the electron charge, K is the Boltzmann constant, T is the absolute temperature, ts is the a-SiGe:H thickness and C_{ox} is the SiO_2

insulator capacitance per unit area (Fcm^{-2}). If N_T or D_{it} is separately set to zero, the respective maximum values of N_T and D_{it} are obtained.

The ideal output characteristics are shown in figure 2.4. They represent the dependence of the Ids current on the Vds voltage at different Vgs voltages. The Ids current increases linearly at low Vds voltages (linear regime) and saturates at high Vds voltages (saturation regime). Note at negative gate bias (p-type region) Ids current is lower than at positive gate bias (n-type region).

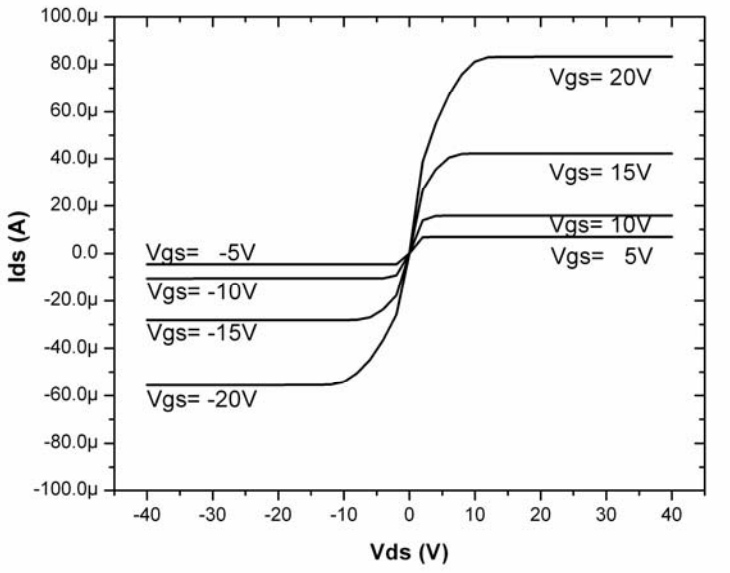


Fig 2.4 Ideal output characteristics of ambipolar TFTs.

The output characteristics can be affected by a high contact resistance. In the presence of high contact resistance it appears dependencies of extracted field-effect mobility and V_T on the channel length. These dependencies are larger in short channel TFTs. In the case of long channel TFTs with low contact resistance, the field- effect mobility is almost not affected. If the contact resistance is considerable high, then the Ids current is affected, and the extracted field-effect mobility value is lower than the true field-effect mobility. From the extrapolation of the width-normalized

total resistance (obtained in the linear region of the output characteristics) for different channel lengths, the width-normalized contact resistance (RcW) can be extracted [50]. It is well know that at lower deposition temperatures the contact resistance increases, which is attributed to a lower doping efficiency in the contact region film. High contact resistance also explains the on-current reduction at lower deposition temperatures.

2.3 Stability of ambipolar TFTs.

Although amorphous silicon based TFTs are economical, these devices have the disadvantages of threshold voltage shifts after a prolonged application of gate bias stress. It adversely affects the operation of TFT circuits. Although the threshold voltage shift mechanisms have been extensively studied to predict the long-term behavior of silicon based TFT circuits, the present available models in the literature do not fit to the experimental results. Because of the ever-growing application of the ambipolar TFTs in flexible and large area electronics, a more accurate model for threshold voltage shift is still needed.

The defect state creation and charge trapping in the gate dielectric are believed to be the mechanisms responsible for the threshold voltage shift of silicon based TFTs. A comprehensive study of the defect state creation and charge trapping mechanisms can be found in [51].

During the application of gate bias stress, the charge trapping and the defect state creation occur simultaneously; therefore, the experimental results of threshold voltage shift do not provide any particular information about the quantitative effect of each of these mechanisms on the threshold voltage shift of the TFT. In addition, relaxation of the threshold voltage appears after the termination of bias stress. The possible mechanisms for this relaxation such as the annealing of the defect states in the active layer and the charge back tunnelling of trapped electrons inside the gate insulator are explained in [51-

53]. The experimental obtained results for the relaxation of threshold voltage do not support the defect state annealing mechanism. While the calculations of charge trapping and de-trapping in and from gate insulator traps show a good agreement with the kinetics of threshold voltage relaxation. Therefore, of the threshold voltage shift mechanisms, charge trapping in the gate insulator is reversible [51, 54]. This provides a quantitative distinction between the defect state creation in the active layer and the charge trapping mechanisms in the gate insulator. Based on the calculated results for the charge trapping and the defect state creation components of threshold voltage shift, a general conclusion cannot be drawn since the kinetics of both mentioned mechanisms strongly depends on the fabrication process of TFT. More importantly, the qualities of the insulator-semiconductor and metal-semiconductor interfaces strongly influence the kinetics of threshold voltage shift and relaxation of TFTs [51]. The deposition conditions of the active layer also affect the rate of the creation of the extra defect states in the active layer by changing the number of weak bonds inside the layer [51].

2.4 Structures of ambipolar TFTs.

Ambipolar TFTs are fabricated by using a variety of structural topologies and materials. For TFT topologies, there are four types of planar topologies: staggered, inverted staggered, coplanar and inverted coplanar structures [46]. In the coplanar structure, the source, drain and gate electrodes are placed on the same side of the active layer, whereas in the staggered TFTs, the source and drain are placed on one side and the gate on the opposite side of the active layer. The difference between the inverted and non-inverted structures is in the sequence of the deposition of the active and gate electrode layers. In an inverted structure, the gate electrode is placed at the bottom of the structure (bottom-gate structure), but in a non-inverted structure, the gate metal is on top (top-gate structure).

The most popular structure of a-Si:H TFTs which is responsible for the state-of-the-art performance is the inverted staggered structure (bottom-gate) in Figure 2.5. However, in ambipolar TFTs the staggered structure (top-gate) is the most used (Fig. 2.6)[21, 22]. The main reason is because as the film grows the structure relaxes and the residual stress at the top is reduced. Therefore, the transport properties at the top of the film are better than those at the bottom. Thus, in the staggered structure the channel will form at the top of the active layer close to the insulator-semiconductor interface, where the best transport properties are present. However, the main problem is that the use of staggered structure will lead to change the whole fabrication process of the commercial applications, such as commercial LCDs and future flexible displays, where the inverted staggered structure is well established (because the gate metal protects the active layer from back-panel light illumination). For this reason, high performance ambipolar TFTs using the inverted staggered structure can reduce the cost and make simpler the design of these applications without changing the established fabrication process. In this thesis, it is going to be used the inverted staggered structure in the ambipolar a-SiGe:H TFTs.

Usually silicon oxide (SiO_2) is used as the gate insulator of ambipolar TFTs, because the ambipolar behavior has been observed only in devices with a gate insulator based on SiO_2. The gate, source, and drain electrodes are made of Cr, Mo or Al metals.

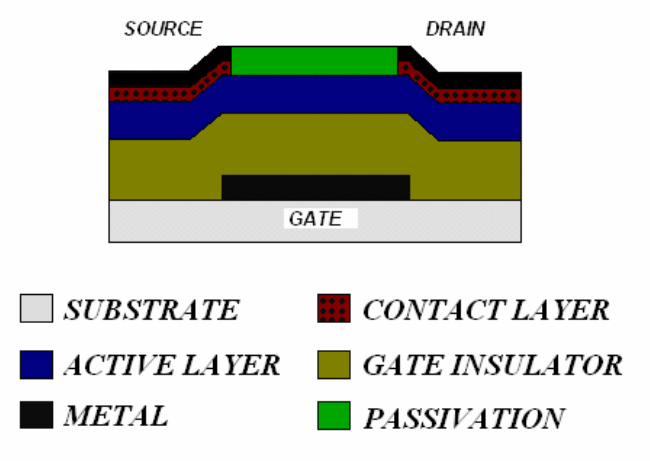


Fig 2.5 Inverted staggered structure of ambipolar TFTs.

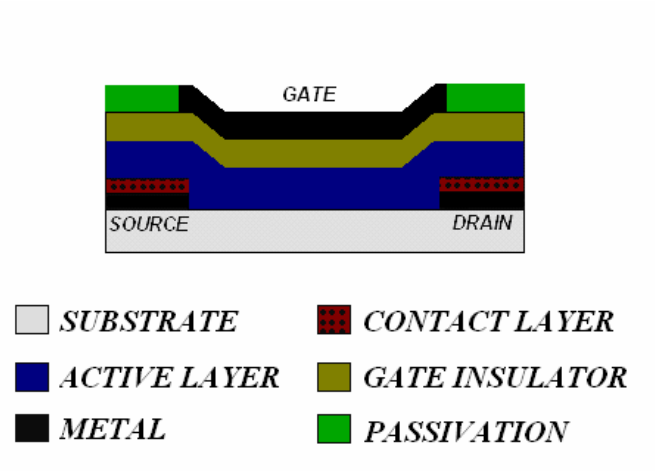


Fig 2.6 Staggered structure of ambipolar TFTs.

CHAPTER 3

CHARACTERIZATION OF LOW-TEMPERATURE MATERIALS.

As mentioned in section 1.1, deep states are formed generally from unfavorable deposition conditions. Therefore, the deposition conditions of the active layer affect the rate of the creation of the defect states in the film. Also, the qualities of the insulator-semiconductor and metal-semiconductor interfaces strongly influence the electrical characteristics and the stability of the TFTs. For this reason is important to obtain the best deposition conditions for the preparation of the films in the TFT structure. Each film needs to be optimized in order to have high-quality interfaces and lower DOS possible in the active layer.

3.1 Characterization of gate insulator.

Insulators obtained at temperatures below 300 °C show lower performance characteristics when are compared with those obtained at high temperatures (>800 °C) in Complementary Metal-Oxide-Semiconductor technology [55]. Therefore, alternative techniques that allow the deposition of high quality insulator materials at low temperatures (< 300 °C) are an issue.

In this respect, silicon oxide films (SiO_2) deposited by Spin-On Glass (SOG) at low temperatures results very attractive. The advantages of SOG include a low defect density in the films deposited, low process cost, excellent for planarization applications, filling gaps and smoothing the surface with multiple coatings.

SOG is an interlevel insulator that is supplied in liquid form. The SOG solution forms an arrangement of silicate polymers with a Si-O structure, these polymers are in an alcohol solvent system. The datasheet of SOG suggests an annealing in the range of 400 – 900°C to obtain a SiO_2 thin film. However, for flexible substrate applications it is necessary to use much lower temperatures for curing.

To study the deposition of SiO_2 films using SOG cured at 200°C, two solvents (2-propanol and deionized water - DI) were used as diluents for the SOG in order to observe its effect on the electrical, optical and compositional characteristics of the SiO_2 films produced.

Silicon wafers were used as substrates and, before the SOG deposition, they were chemically cleaned. First, the wafers were cleaned in trichloroethylene for 10 min, followed with acetone also for 10 min. in ultrasonic bath. Later, the samples were cleaned with the RCA1 solution ($NH_4OH:H_20_2:H_20$=1:1:5 at 75°C for 15 min.), followed with the RCA2 solution ($HCL:H_20_2:H_20$=1:1:6 at 75°C for 15 min.). Finally, after rinsing the wafers with deionized water, buffered HF was used for 10 sec to remove the thin native oxide on the silicon surface. After that, the SOG was deposited on the silicon wafers with the following procedure:

• For measurements of the refractive index: Liquid application of SOG by spinning at room temperature on the silicon wafers at 3000, 4000 and 5000 revolutions per minute (RPM) for 30 sec.

• For Fourier transform infrared (FTIR) spectroscopy: Liquid application of SOG at room temperature at 3000 RPM for 30 sec.

• For Atomic Force Microscope (AFM): Liquid application of SOG at room temperature at 3000 RPM for 30 sec.

• For Metal-oxide-semiconductor (MOS) Capacitors: Liquid application of SOG at room temperature at 3000 RPM for 30 sec.

• Annealing at 100°C for 15 min. to reduce humidity and evaporate most of the solvents.

• Curing for 6.5 Hrs at 200°C in N_2 ambient.

To measure refractive index it was used a Gaertner ellipsometer L117. The IR absorption spectra of the films were measured with a "BRUCKER" FTIR spectrometer, Model Vector-22. The IR spectrum was observed for wave numbers between 4000 and 400 cm^{-1}. The absorbance spectrum is converted to absorption coefficient (α) using equation 3.1, where A is the absorbance and t the thickness of the sample (260 ±10 nm for undiluted SOG, 160 ±4 nm for SOG diluted with 2-Propanol and 26 ±4 nm for SOG diluted with DI).

$$\alpha = -\ln (1 - A) / t \qquad (3.1)$$

For the determination of dielectric constant k, MIM (Metal- Insulator-Metal) structures were fabricated. Then, its capacitance was measured with a PM 6303 automatic RLC meter and using the equation 3.2, k was calculated.

$$C = k\varepsilon A/d \qquad (3.2)$$

In equation 3.2, ε is permittivity, A is the area of the capacitor, d is the insulator thickness and k is dielectric constant. The MIM structures also were used to calculate the insulator breakdown field, which is an important parameter that supply information related to the quality of the SiO_2 films produced. Also, MOS capacitors were made with diluted SOG above p-type silicon wafers. Aluminum was evaporated by e-gun to form the contacts. The curves of capacitance as function of the applied voltage were measured with a capacitance – voltage (C – V) station. The MIM structures and MOS capacitors have an area of 0.015006 cm^2.

To measure roughness of the films, it was used an Atomic Force Microscope (AFM) on SOG samples (diluted and undiluted) deposited on silicon wafers.

Figure 3.1 shows the refractive index as function of the spinner speed for the SOG deposition, for three different solutions: A) Undiluted SOG, B) SOG diluted with DI and C) SOG diluted with 2-Propanol. The refractive index of undiluted SOG films shows a strong dependence with the spinner speed. At low spinner speed refractive index is low, close to 1.25 (for 3000 RPM), while increasing the spinner speed it increases as well, to about 1.6 (for 5000 RPM).

On the other hand, the films produced from diluted SOG do not show a significant change on refractive index. A possible reason is that the solvents used as diluents for SOG provide an easier way for the evaporation of the organic materials contained in the SOG solution. The refractive index value of the films produced from diluted SOG is close to that of thermally grown stoichiometric SiO_2.

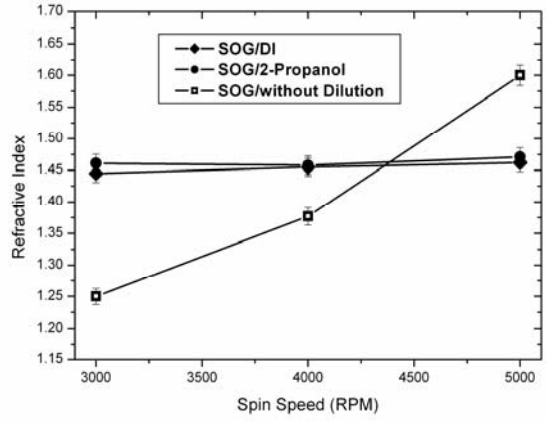


Fig 3.1 Refractive index of SOG vs Spin speed.

Figure 3.2 shows the absorption coefficient of the films prepared from SOG. It was identified the Si-O bond (at 1072 cm^{-1}), which is also found on thermally grown SiO_2 [56]. The Si-OH (at 920 cm^{-1}), O-H (at 3490 cm^{-1}), C-H

and C-O (at 1139 cm^{-1}) bonds are probably related to the organic solvent material present on the SOG [56]. It was observed a considerable reduction of Si-OH (920 cm^{-1}) and O-H bonds (3490 cm^{-1}) in the films produced from diluted SOG, which is an indication of a good quality film.

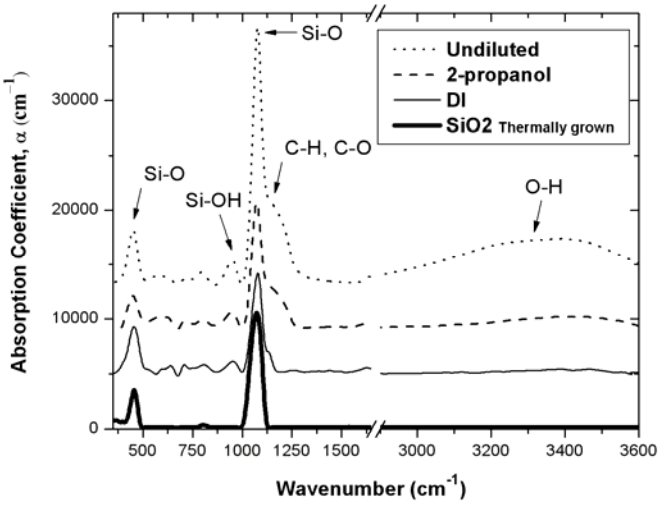
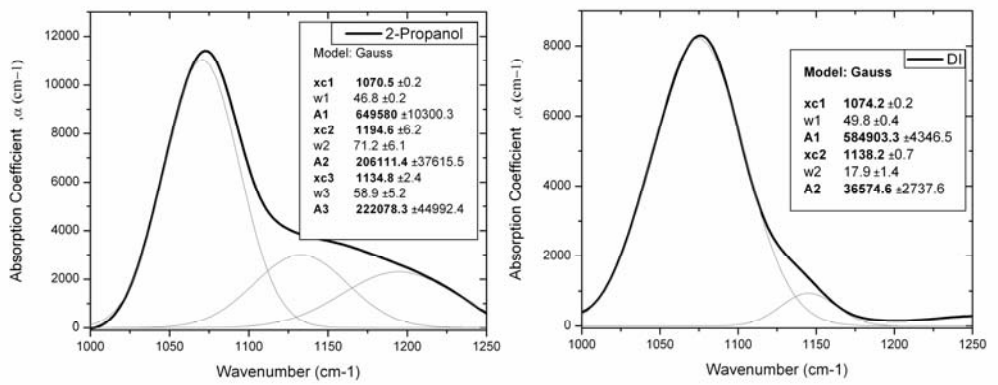


Fig 3.2 Absorption coefficient versus wavenumber for diluted and undiluted SOG samples.

The deconvolution of the peaks in the region from 1250 cm^{-1} to 1000 cm^{-1} for the films produced from diluted SOG is shown in Figure 3.3a) SOG diluted with 2-propanol and 3.3b) SOG diluted with DI.



a) b)

Fig 3.3 Deconvolution of the FTIR peaks located at 1000 – 1250 cm^{-1} of the SiO_2 films produced from a) SOG diluted with 2-propanol and b) SOG diluted with DI.

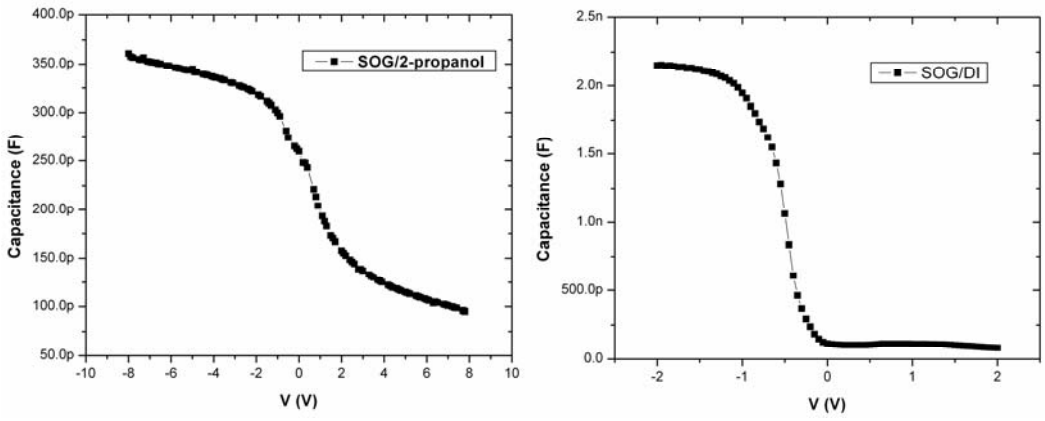
It was found a shift in the position of the Si-O stretch peaks for samples produced from diluted SOG. For the films obtained from SOG diluted with 2-propanol the position was 1070 cm^{-1} and for that obtained from SOG diluted with DI the position was 1074 cm^{-1}. We believe that this is because the properties of the films produced from SOG diluted with DI approach a thermal oxide. In accordance with this, M. P. Woo *et al.* found that the Si-O peak shift to higher wave numbers when the organic solvents are completely removed from the film, converting the siloxane into a silicate structure [57]. This occurs when the Si-O peak position approaches to 1080 cm^{-1} during the curing. Also, they found that as the SOG transforms into a silicon dioxide, the area ratio of asymmetric Si-O stretch (1070 cm^{-1}): Si-O-Si stretch (1200 cm^{-1}) approaches 5.7:1. In the films produced from SOG diluted with 2-propanol the area ratio is 3.1:1, while in the films produced from SOG diluted with DI the area ratio is much higher than 5.7:1, which is possibly related to the fact that the Si-O-Si stretch apparently is imperceptible. From the above mentioned, we believe that the films produced from SOG diluted with DI have a similar structure to that of the thermally grown SiO_2. On the other hand, the deconvolution shows a reduction of the C-H, C-O peaks (1139 cm^{-1}) in films produced from diluted SOG samples. That supports the assumption that the solvents (2-Propanol and DI) make easier the evaporation of the organic material presented in the SOG.

Table 3.1 shows the content of the areas of the Si-O stretch bonds and the C-H, C-O bonds. The ratio of the areas is shown also. In the films produced from undiluted SOG the area ratio is 0.86 due to the higher content of C-H and C-O bonds, while in the films produced from SOG diluted with 2-propanol is 2.92 and for the films produced from SOG diluted with DI is 16 due to the much lower content of C-H, C-O bonds. These results are in agreement with those obtained above.

Table 3.1 Area content of Si-O and C-H, C-O bonds and the area ratio of them.

	Content Si-O Stretch (Area cm^{-2})	**Content C-H, C-O (Area cm^{-2})**	**Area ratio Si-O : C-H, C-O**
Undiluted SOG	$1.0x10^6$	$1.2x10^6$	0.86
SOG/DI	584903	36574	16
SOG/2-Propanol	649580	222078	2.92

The dielectric constant k, obtained from the equation 3.2, of the SiO_2 films prepared from diluted SOG was approximately 4.1. This was corroborated by the measurements of the MIM structures and by the C-V curves of the MOS capacitors in figure 3.4.



a) b)

Fig 3.4 C-V curves of MOS capacitors produced from diluted SOG, a) SOG diluted with 2-propanol and b) SOG diluted with DI.

From the C-V curves of the MOS capacitors, it can be see a higher slope and well defined oxide capacitance C_{ox} for the MOS capacitor made

with SiO_2 films from SOG diluted with DI, which is an indicating of good insulator properties.

On the other hand, the current - voltage characteristics in the MIM structures were measured in order to obtain the insulator breakdown field. Figure 3.5 shows the breakdown field for the MIM structures containing a film produced from SOG diluted with 2-propanol and SOG diluted with DI. The maximum voltage applied to the samples was 100 V. The insulator breakdown field for the MIM structure containing a film produced from SOG diluted with 2-propanol was approximately 4.5 MV/cm, while for the MIM structure containing a film produced from SOG diluted with DI was approximately 21 MV/cm. These results of SiO_2 film produced from SOG diluted with DI show an improvement in the insulator properties when are compared to those obtained from methylsiloxane SOG deposited at 425 °C, SiO_2 deposited by CVD or PECVD, and without the residual stress that appears in SiNx films deposited by PECVD as gate insulator in TFTs [58-62].

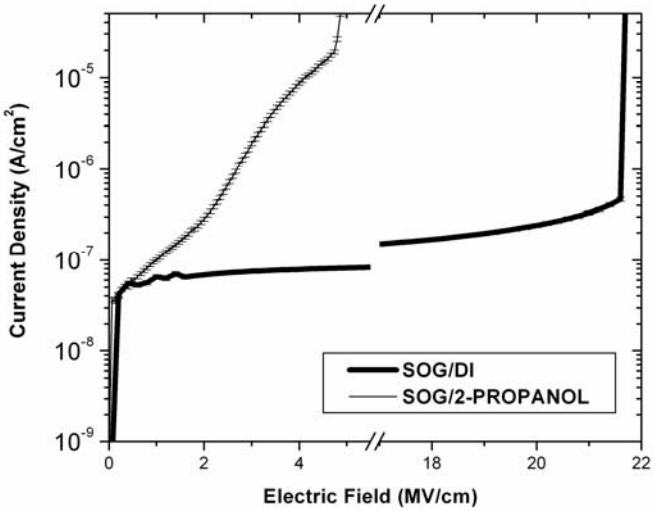


Fig 3.5 Breakdown field for the MIM structures containing a SiO_2 film produced from SOG diluted with 2-propanol and diluted with DI.

Figure 3.6 shows AFM images of SOG samples diluted with 2-propanol and DI compared with undiluted SOG. As it is evident from these images, films produced from diluted SOG show less rugosity than that from undiluted SOG. This is because with the dilution we change the viscosity of SOG previous to deposition.

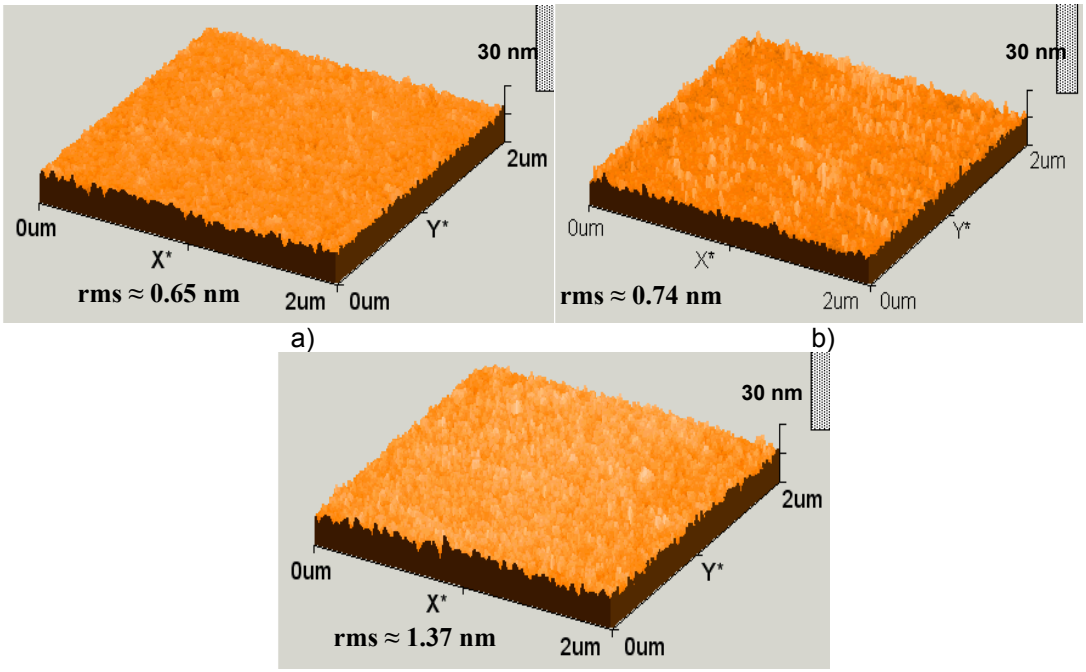


Fig 3.6 AFM images of, a) SOG diluted with 2-propanol, b) SOG diluted with DI compared with c) undiluted SOG.

3.1.1 Effects of curing time in the properties of SiO_2 films produced from SOG diluted with DI.

In the preceding section, the assumption that the solvents (2-Propanol and DI) made easier the evaporation of the organic material contained in the SOG was supported with experimental results. However, figure 3.7 shows a dependency of refractive index on curing time for films produced from SOG

diluted with DI. The highest refractive index may be caused by the short curing time of 1 Hr, which is not enough for complete evaporation of the organic material presented in the SOG. While for 6.5 Hrs the organic material is almost completely evaporated. This was corroborated using AFM measurements, MIM structures and FTIR spectroscopy.

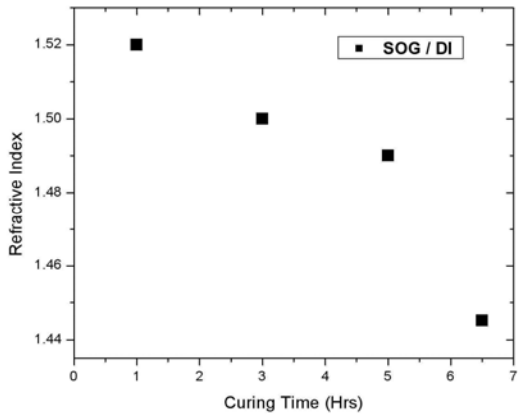
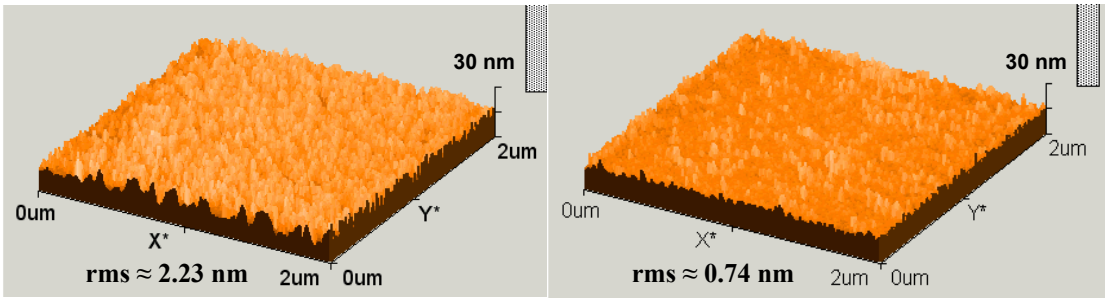


Fig 3.7 Refractive index of films produced from SOG diluted with DI vs. curing time.

As can be see in figure 3.8, from the AFM measurements, the film produced from SOG diluted with DI cured for 6.5 Hr. show less rugosity than the film cured for 1 Hr. This agree with the current - voltage measurements of the MIM structures where the breakdown field was obtained (Fig. 3.9). The insulator breakdown field for the MIM structure containing a film produced from SOG diluted with DI cured for 6.5 Hr. was approximately 21 MV/cm, while for the MIM structure containing the film cured for 1 Hr. was approximately 4 MV/cm.



a) b)

Fig 3.8 AFM images for SOG diluted with DI for a) 1 Hr., b) 6.5 Hrs. of curing time.

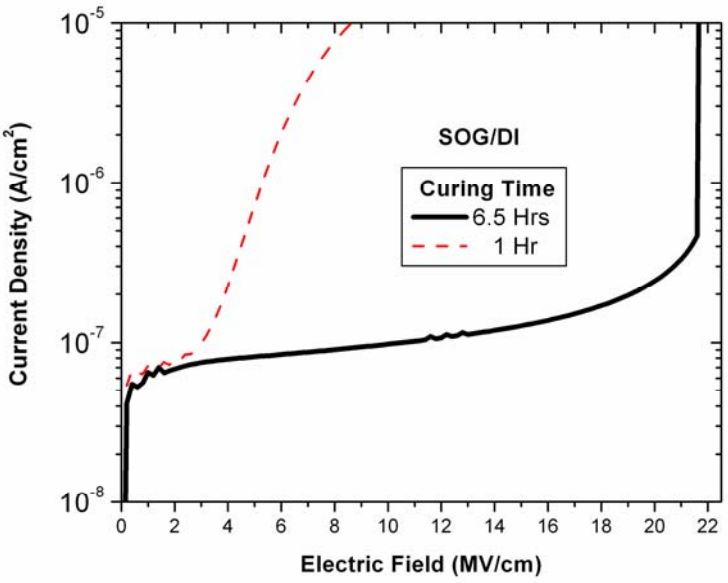


Fig 3.9 Breakdown field for the MIM structures containing a SiO_2 film produced from SOG diluted with DI for 1 Hr. and 6.5 Hrs. of curing time.

Figure 3.10 shows the absorption coefficient of the films from 700 cm^{-1} to 1500 cm^{-1}. It was found a shift in the position of the Si-O stretch peaks. For the films obtained from SOG diluted with DI cured for 6.5 Hrs. the position was 1074 cm^{-1} and for that cured for 1 Hr. the position was 1064 cm^{-1}. The shift in the position of the Si-O peaks is because the properties of the films cured at 6.5 Hrs. approaches that of a thermal oxide. This is in accordance with afore mentioned where the Si-O peaks shift to higher wave numbers

when the organics solvents are completely removed from the film. On the other hand, for the films obtained from SOG diluted with DI cured for 1 Hr. apparently there are a reduction in Si-O (at 1064 cm^{-1}) bonds and an increase in C-H and C-O (at 1139 cm^{-1}) bonds. This can corroborate the previous assumption that the short curing time (1 Hr.) is not enough for complete evaporation of the organic solvents contained in the SOG.

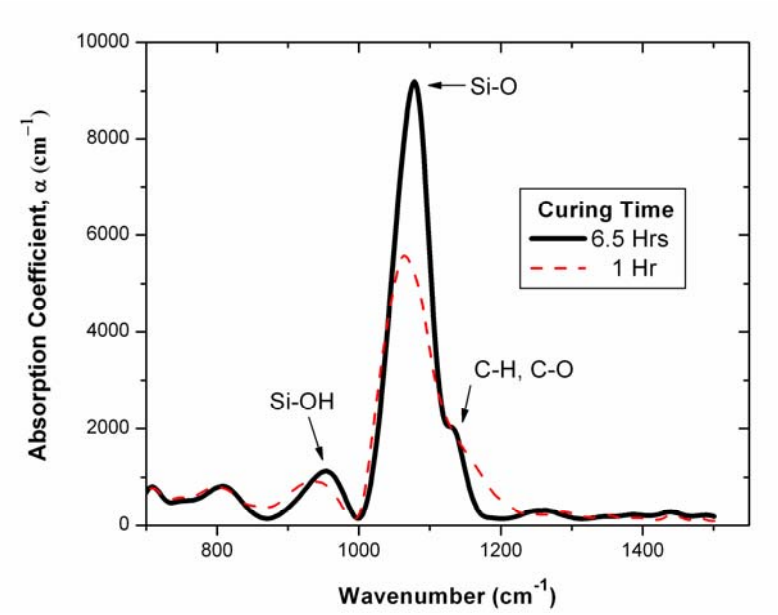


Fig 3.10 Absorption coefficient versus wavenumber for films cured for 1 and 6.5 Hrs.

3.2 Characterization of a-SiGe:H active layer.

Because a high-content of germanium increases the DOS, the preparation of high quality a-SiGe:H films becomes an important research issue. In this section, a-SiGe:H films deposited by low frequency PECVD at 300 °C and later at 200 °C were characterized by FTIR spectroscopy, measurements of temperature dependence of conductivity and UV-Visible spectroscopic ellipsometer.

The a-SiGe:H films were deposited by LF PECVD at 300 °C, pressure of 0.6 Torr and an RF power of 300 W from silane (SiH_4) and germane

(GeH_4) feed gases diluted with H_2. The flow rate of SiH_4 (10 % H_2 diluted) and H_2 was fixed at 45 sccm and 1000 sccm, respectively. The flow rate of GeH_4 (90 % H_2 diluted) was in the range of 25 to 185 sccm, in order to address the effects of germanium in the quality of a-SiGe:H films. Table 3.2 summarizes the deposition conditions for the a-SiGe:H films.

Table 3.2 Deposition conditions for the a-SiGe:H films at 300 °C.

a-SiGe:H	SiH4 (sccm)	GeH4 (sccm)	H2 (sccm)	Pow (W)	Temp (°C)	Pres (Torr)	Time (min)
I	45	25	1000	300	300	0.6	25
II	45	65	1000	300	300	0.6	25
III	45	105	1000	300	300	0.6	25
IV	45	145	1000	300	300	0.6	25
V	45	185	1000	300	300	0.6	25

We prepared a-SiGe:H samples on corning 1737 substrate and on silicon wafers. The characterization equipment used was UV-Visible spectroscopic ellipsometer (Jobin Yvon - MWR UVISEL) to measure the imaginary part of the pseudo-dielectric function (Im[ε]) of the films deposited over the corning glass. The model used in order to obtain the bandgap was the Tauc-Lorentz dispersion law. The IR absorption spectra of the films were measured with a “BRUCKER” FTIR spectrometer, Model Vector-22 in the range of 4000 to 400 cm^{-1}. The DC conductivity at different temperatures of the a-SiGe:H layers were measured using a Low Temperature Micro Probe (LTMP) system from MMR- Technologies Inc (Model LTMP-2). The dark conductivity measurements were done in the temperature range from T= 300

to 410 K. Applying the ohm's law we obtain the Resistance of the film. From this value it can be determined the conductivity using the following equation:

$$\sigma = L / RWt \quad (3.3)$$

Where L is the separation between contacts, W is the width of the contacts and t is the thickness of the film. With the conductivity values at different temperatures, the temperature dependence of conductivity was plotted versus 1/KT. The experimental curves can be described and analyzed according to the Arrhenius expression:

$$\sigma (T) = \sigma_0 \exp^{-(Ea/KT)} \quad (3.4)$$

Where Ea is the activation energy, K is the Boltzmann constant, T is the absolute temperature.

The values of bandgap obtained in a-SiGe:H films are lower than expected and decrease with the increment of GeH_4 flow. Typically the bandgap of the a-Si:H films are of 1.8 eV, for a-SiGe:H films with GeH_4 flow of 25 sccm the bandgap was of 1.1 eV, while for 105 and 185 sccm the respective values were 0.81 and 0.77 eV. Therefore, the conductivity of the a-SiGe:H film is increased as the GeH_4 flow is increased.

Figure 3.11 shows the activation energy obtained from measurements of temperature dependence of conductivity. As can be see, the a-SiGe:H film with GeH_4 flow of 105 sccm shows the highest activation energy. The activation energy indicates the intrinsic level of the a-SiGe:H film, thus, in amorphous films, dopants and contaminants increase the DOS and reduce the activation energy. Therefore, higher activation energy could indicate a lower DOS which can translate in performance improvement of the TFT.

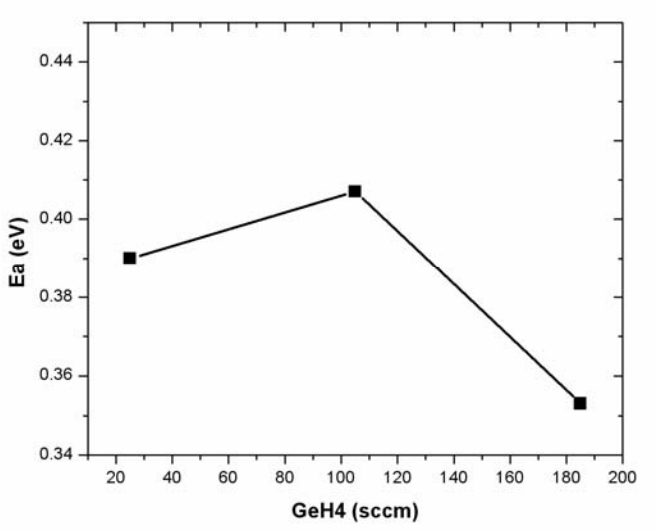


Fig 3.11 Activation energy as function of GeH_4 flow of the a-SiGe:H film.

The IR spectra of the a-SiGe:H films is show in figure 3.12. It can be observed the Si-H stretching and bending vibration modes (2000 y 630 cm^{-1}) and, the Ge-H stretching and bending vibration modes (1895 y 565 cm^{-1}) [63-65]. The Hydrogen content for Si-H and Ge-H bonds is show in figure 3.13. As expected, the Hydrogen content due to Si-H bonds was decreasing with the increment of GeH_4 flow. However, it was observed an increase of Hydrogen content in films with a GeH_4 flow of 105 sccm. Also, the hydrogen content due to Ge-H bonds (Figure 3.13b) show the highest value in a-SiGe:H films with a GeH_4 flow of 105 sccm. The hydrogen incorporated in the a-SiGe:H film saturates dangling bonds while reduces deep states in the DOS [37]. This increase of hydrogen incorporation in both figures and the highest activation energy makes us suppose that probably the films with GeH_4 flow of 105 sccm may have a lower DOS.

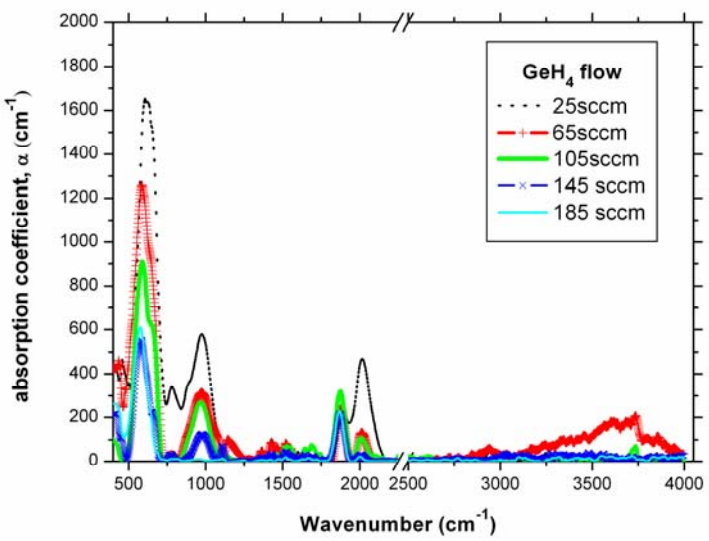
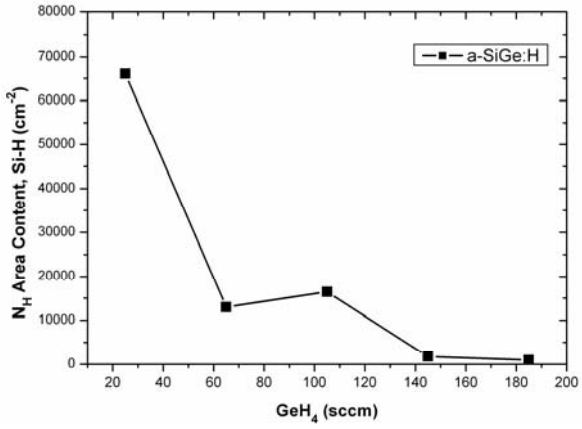
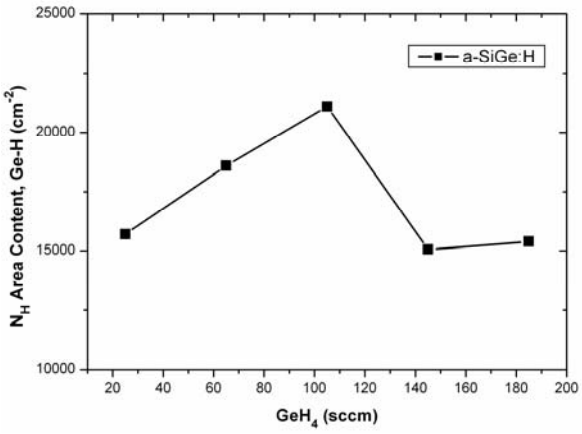


Fig 3.12 Absorption coefficient versus wavenumber for a-SiGe:H films at different GeH_4 flow.



a)



b)

Fig 3.13 Hydrogen concentration in a) Si-H and b) Ge-H bonds of the a-SiGe:H films.

From the previous assumption that a-SiGe:H films with GeH_4 flow of 105 sccm may have a higher quality, a-SiGe:H films were deposited by LF PECVD at 200 °C with the same GeH_4 flow (105 sccm). These films were characterized and compared with the film at 300 °C.

Figure 3.14 shows a comparison between the bandgap and conductivity for the a-SiGe:H films deposited at 300 °C and 200 °C. As can be seen at 200 °C the bandgap is larger and the conductivity is lower than those measured for the films deposited at 300 °C. This increase in the bandgap is important in order to reduce the off-current and increase the on/off-current ratio in the TFTs.

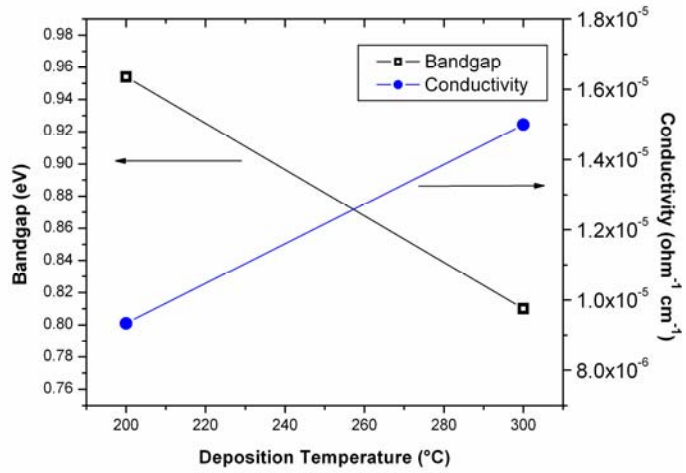


Fig 3.14 Bandgap and conductivity as function of deposition temperature of the a-SiGe:H films.

The activation energy for the a-SiGe:H film deposited at 200°C was of 0.416 eV and for the a-SiGe:H film deposited at 300 °C was of 0.407 eV.

The IR spectra of the a-SiGe:H films at 200 °C and 300 °C are shown in figure 3.15. In this figure it can be seen the Si-H stretching and bending vibration modes (2000 y 630 cm^{-1}) and Ge-H stretching and bending vibration modes (1895 y 565cm^{-1}). Figure 3.16 shows the hydrogen concentration (area content) of Ge-H and Si-H bonds of the a-SiGe:H films at 200 °C and

300 °C. From the FTIR analysis, it is clear that the a-SiGe:H film at 200 °C has incorporated more Si-H bonds and less Ge-H bonds than the film at 300 °C.

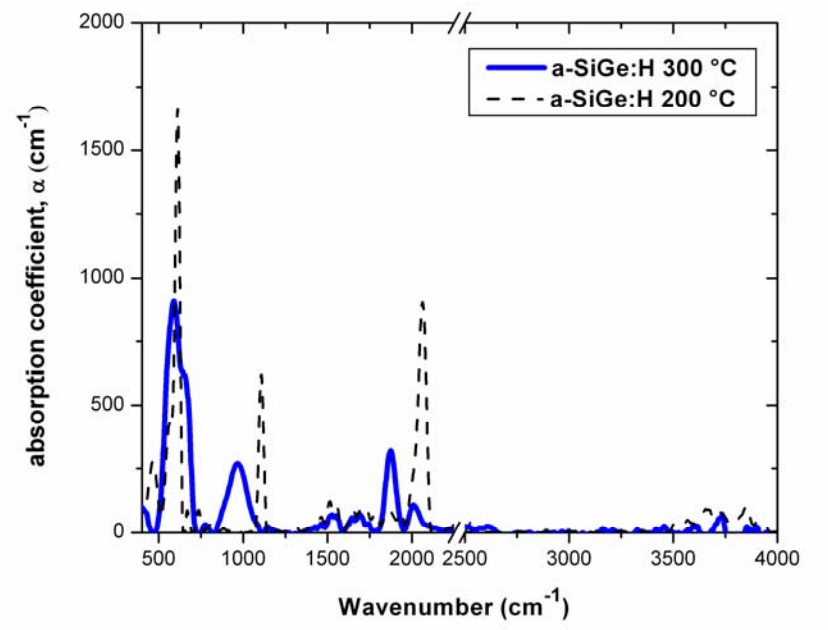


Fig 3.15 IR spectra of the a-SiGe:H films deposited at 200 °C and 300 °C.

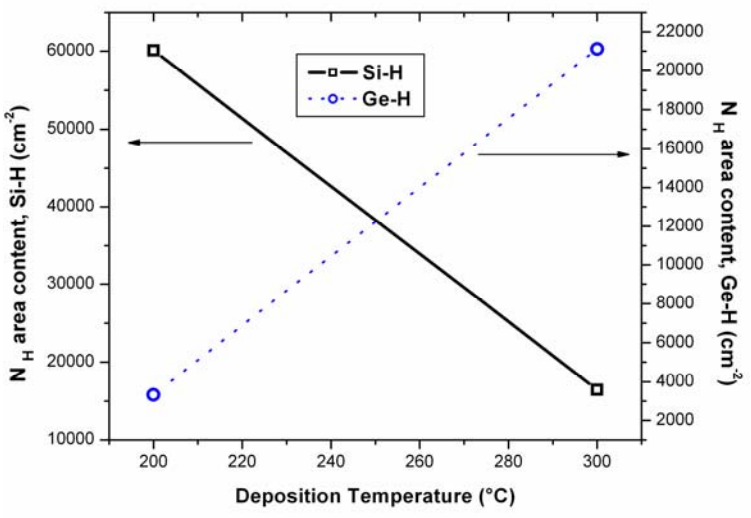


Fig 3.16 Hydrogen concentration in Si-H and Ge-H bonds of the a-SiGe:H films.

The higher bandgap in the film at 200 °C resulted from a possible reduction in the Ge content as can it see in the FTIR results. This higher bandgap reduces the carrier concentration at thermal equilibrium reducing the conductivity. The analysis of FTIR not only shows a possible reduction in the Ge content but also suggests higher hydrogen content in the film at 200 °C. The hydrogen incorporated in the a-SiGe:H film saturates dangling bonds and reduces deep states in the DOS, this is a possible explanation about the increase in the activation energy for a-SiGe:H films at 200 °C. Also recall, the bandgap increases with increasing hydrogen concentration.

3.3 Characterization of Contact Region Films.

As mentioned in section 1.1, in amorphous semiconductors the doping efficiency drops at high doping levels. Le Comber and Spear [12] reported that amorphous silicon prepared by PECVD can effectively be doped by adding small amounts of phosphine (PH_3) or diborane (B_2H_6) to the silane (SiH_4) in the discharge gas. For phosphorus doping the conductivity increases at low doping levels. At higher doping levels, conductivity decreases presumably due to the generation of defect states. For boron doping, conductivity decreases at low doping levels and attains, at higher doping levels it increases and then decreases too (Fig 1.1).

As contact region film, it was characterized a light doped a-Ge:H film in order to have ohmic contacts and low contact resistance. To measure this, it was used the Transfer Length Method (TLM) which consist in current - voltage measurements of contacts at different separation [66]. The resistance measured between the contacts is described by:

$$R_T = \rho_s d/Z + 2R_C \qquad (3.5)$$

Where ρ_s is the resistivity, d is the separation between the contacts, Z is the width of the contact and R_C is the contact resistance.

To calculate the contact resistance, the resistance measured as function of d are plotted and the interception at d=0 gives the value of $2R_C$. The measurements were done under dark conditions using a Keithley 6517A Electrometer/High Resistance Meter. The a-Ge:H films were deposited by LF PECVD at 300 °C and later at 200 °C, pressure of 0.6 Torr and an RF power of 300 W, with a GeH_4 flow of 250 sccm, H_2 flow of 3500 sccm and PH_3 flow from 5 to 50 sccm.

The current - voltage measurements of the a-Ge:H film with PH_3 flow of 20 sccm are show in figure 3.17 and the extracted contact resistance as function of the PH_3 flow is shown in figure 3.18. It is important to note the symmetry of the current – voltage measurements for positive and negative voltages applied. In figure 3.18, it can be see the effect of the PH_3 flow in the contact resistance, where at low flow of PH_3 the contact resistance decreases but at higher flow it increases. From the values of contact resistance, the lowest is obtained with PH_3 flow of 20 sccm and is close to 1kOhms.

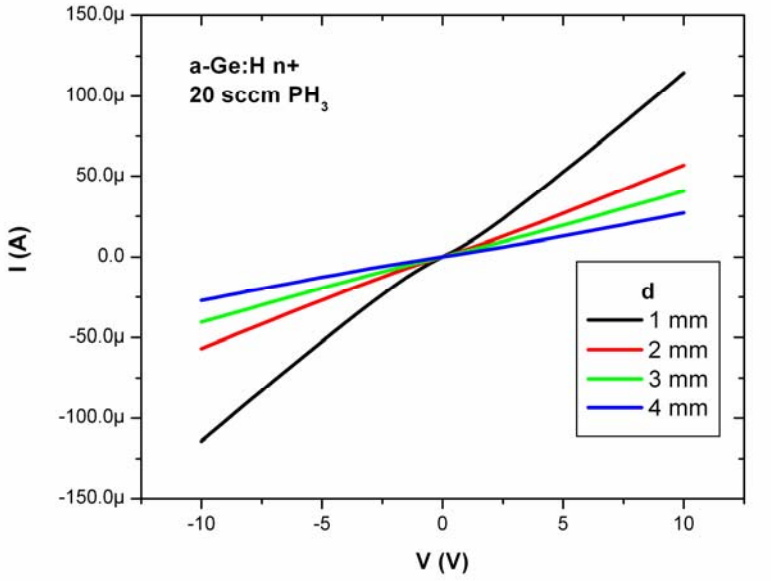


Fig 3.17 Current - voltage measurements of the a-Ge:H film with PH_3 flow of 20 sccm.

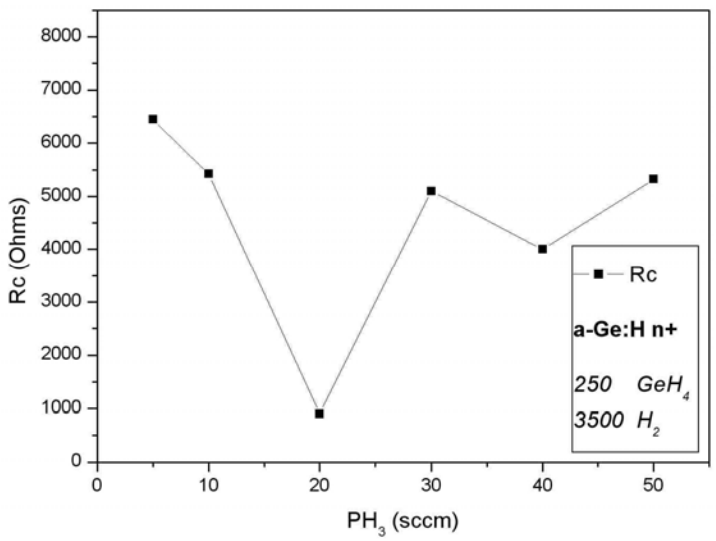


Fig 3.18 Contact resistance of the a-Ge:H film at 300 °C as function of the PH_3 flow.

In order to have a contact region film at low-temperature, the a-Ge:H film was characterized at 200 °C using the same approach as at 300 °C. Figure 3.19 shows the contact resistance of the a-Ge:H film at 200 °C as function of the PH_3 flow. The effect of the PH_3 flow in the contact resistance seems to be similar as at 300 °C, where at low flow of PH_3 the contact resistance decreases but at higher flow it increases. This behavior agrees with the characteristics of conductivity showed in figure 1.1. Also, the lowest value of contact resistance is obtained with PH_3 flow of 20 sccm and is close to 1kOhms.

The characterization of p-type a-Ge:H film at 200 °C was also done. Figure 3.20 shows the contact resistance of the p-type a-Ge:H film as function of the B_2H_6 flow. The characteristics of conductivity showed in figure 1.1 could explain the effect of the B_2H_6 flow in the contact resistance, where at low flow of B_2H_6 the contact resistance increases but at higher flow it decreases and finally increases again. However, in the p-type film the lowest contact resistance was higher than n-type with a value close to 6 kOhms.

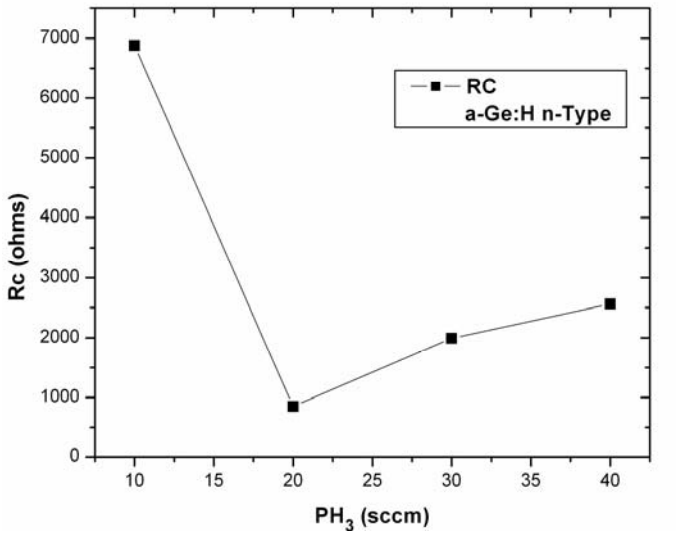


Fig 3.19 Contact resistance of the a-Ge:H film at 200 °C as function of the PH_3 flow.

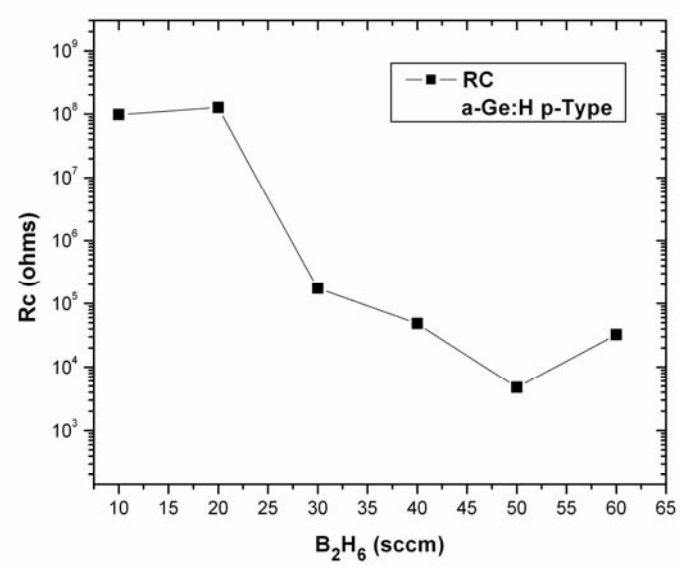


Fig 3.20 Contact resistance of the a-Ge:H film as function of the B_2H_6 flow.

3.4 Conclusions.

We demonstrated that dilution of SOG and long curing time are necessary to obtain good quality films annealed at 200°C. From FTIR spectroscopy we observed a considerable reduction of Si-OH bonds (920 cm^{-1}) and O-H bonds (3490 cm^{-1}) in diluted samples. The films produced from

diluted SOG showed a refractive index and dielectric constant very close to those of the thermally grown SiO_2. The insulator breakdown field for the MIM structures with SiO_2 films produced from SOG diluted with DI was approximately 21 MV/cm. All these results suggest that SOG diluted with DI is an excellent candidate to be used as insulator on flexible and large-area electronics.

The characterization of the a-SiGe:H films makes us suppose that probably the films with GeH_4 flow of 105 sccm may have a lower DOS. Also, the analysis of FTIR of the a-SiGe:H films shows a possible reduction in the Ge content and an increase in hydrogen content when the a-SiGe:H films are deposited at 200 °C.

On the other hand, the characterization of contact region films was done. The effect of the PH_3 and B_2H_6 flows in the contact resistance seems to be explained with the characteristics of conductivity as function of gas phase concentration of the doping gases, showed in figure 1.1. The lowest value of contact resistance at 200 °C for n-type and p-type films is obtained with PH_3 flow of 20 sccm and B_2H_6 flow of 50 sccm, respectively. It seems to be these films deposited at low temperatures have the properties suitable for contact region in TFT applications.

CHAPTER 4

DEVELOPMENT OF LOW-TEMPERATURE a-SiGe:H TFTS.

In previous chapter it has been presented the characterization of each one of the films necessary to build the TFT structure. From these results one can see that these films deposited at low temperatures could lead to a good performance in the electrical characteristics of the TFT. However, to develop a low-temperature ambipolar a-SiGe:H TFTs technology, the improvement in the device interfaces is required. In this respect, interface preparation procedures (which are conventional for a-Si:H technology) are necessary for improving the performance in the electrical characteristics.

4.1 Fabrication of Low-temperature a-SiGe:H TFTs.

The structure used in the ambipolar TFTs was the inverted staggered (Figure 4.1). However, in this structure some changes should be made. For example, after deposition of the gate insulator and the active layer, it must be deposited either the passivation or the contact region films. The selection of any of these options may change the quality of the metal-semiconductor interface.

On the other hand, the inverted staggered structure is well established in the fabrication process for commercial applications, such as LCDs, because the gate metal protects the active layer from back-panel light illumination. However, since the LCDs become larger, the number of address lines must increase and the gate lines must be longer and narrower. To avoid the gate delay affects the LCD performance, the gate line must be thicker in

order to reduce its resistance. Therefore, the problem associated with this thicker gate is that in the TFT structure around the corners of the gate the gate insulator tends to be thinner [67]. This causes that the insulator may suffer strong leakage due to the high electric field at the corner.

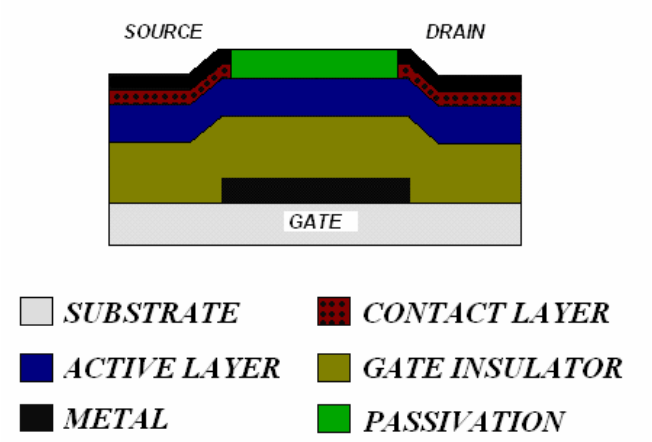


Fig 4.1 Inverted staggered structure of ambipolar TFTs.

In order to avoid that the high electric field affects the performance of the TFT, mainly at the insulator-semiconductor interface, in this thesis was developed a method for planarizing the gate by using Spin-On Glass. The method is described as follows:

The cross section of the planarization process is shown in figure 4.2. First, we deposited 100nm of SOG diluted with deionized water (DI) by Spin-coating and cured at 200°C for 6.5 Hrs. Then, photoresist is applied and patterned to leave uncovered the place that will be used for the gate. Later, the SOG is etching by Reactive Ion Etching (RIE) leaving the place of the gate. The SOG was etched with CF_4 plasma at a pressure of 160 mTorr and RF power of 50 Watts. Finally, the planarized gate is formed by lift-off process and 100nm of e-gun evaporated Al.

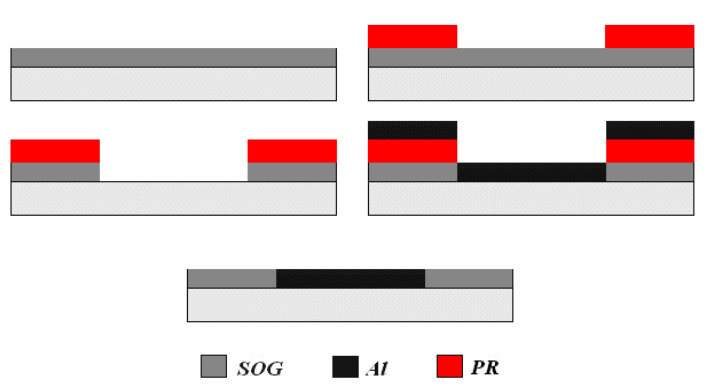


Fig 4.2 Process flow of the planarization.

The planarization process is not complex and does not require high-cost vacuum facilities. Also, the process is compatible with plastic or flexible substrates in flexible and large-area electronics.

Planarized and unplanarized a-SiGe:H TFTs were fabricated in order to compare their electrical characteristics. Also, were fabricated two kind of inverted staggered a-SiGe:H TFTs. The difference is in the film used as passivation, silicon nitride (SiNx) or SOG, and the order in which passivation and contact region films were deposited.

The a-SiGe:H TFTs were fabricated on silicon wafers and on Corning 1737 substrate. The process flow and cross section of the unplanarized and planarized a-SiGe:H TFTs using SiNx as passivation are shown in Figure 4.3. The simplified process flow is as follows: first, for planarized TFTs it was used the planarization process described above. For unplanarized TFTs, a 200nm-thick Aluminum layer is e-gun evaporated and patterned as a bottom gate above the substrate (Fig 4.3a). Next, for both unplanarized and planarized, 160 nm-thick of SOG diluted with 2-propanol for silicon wafers and 80 nm-thick of SOG diluted with DI for corning 1737 substrates both cured at 200 °C were used as the gate insulator (Fig 4.3b). Then, a 100 nm-thick undoped a-SiGe:H and 100 nm-thick SiNx films (Fig. 4.3c) were deposited using low frequency (110 kHz) PECVD at 200 °C, pressure of 0.6 Torr and an RF power of 300 W. Later, the SiNx film was patterned as passivation film above

the active layer using RIE (Fig. 4.3d). After that, 40 nm-thick n-type a-Ge:H films (Fig. 4.3e) were deposited using low frequency (110 kHz) PECVD, pressure of 0.6 Torr and an RF power of 300 W. Then, 300 nm-thick Aluminum was e-gun evaporated and patterned to form the source and drain electrodes (Fig. 4.3f). After, the n-type a-Ge:H film was etched using RIE (Fig. 4.3g). Finally, a thermal treatment at 180 °C for 40 minutes was done.

To compare the electrical characteristics of the TFTs the deposition temperature was at 300 °C and, later, at 200°C. In this way, there are a-SiGe:H TFTs fabricated with maximum temperature of 300 °C and others at 200 °C. Where the a-SiGe:H TFTs fabricated at 200 °C are the most important contribution of this thesis.

The process flow and cross section of the unplanarized and planarized a-SiGe:H TFTs using SOG as passivation, are shown in Figure 4.4. The simplified process flow is as follows: first, for planarized TFTs it was used the planarization process described above. For unplanarized TFTs, a 200nm-thick Aluminum layer is e-gun evaporated and patterned as a bottom gate above the substrate (Fig 4.4a). Next, for both unplanarized and planarized, 160 nm-thick of SOG diluted with 2-propanol for silicon wafers and 80 nm-thick of SOG diluted with DI for corning 1737 substrate both cured at 200 °C were used as the gate insulator (Fig 4.4b). Later, a 100 nm-thick undoped a-SiGe:H and 40 nm-thick n-type a-Ge:H films (Fig. 4.4c) were deposited using low frequency (110 kHz) PECVD at 200 °C, pressure of 0.6 Torr and an RF power of 300 W. After that, 300 nm-thick Aluminum was e-gun evaporated and patterned to form the source and drain electrodes (Fig. 4.4d). Then, the n-type a-Ge:H film was etched using RIE to self-align and to form the source and drain regions (Fig. 4.4e). Finally, a passivation 80 nm-thick layer of SOG diluted with DI cured at 200°C was deposited and patterned (Fig 4.4f).

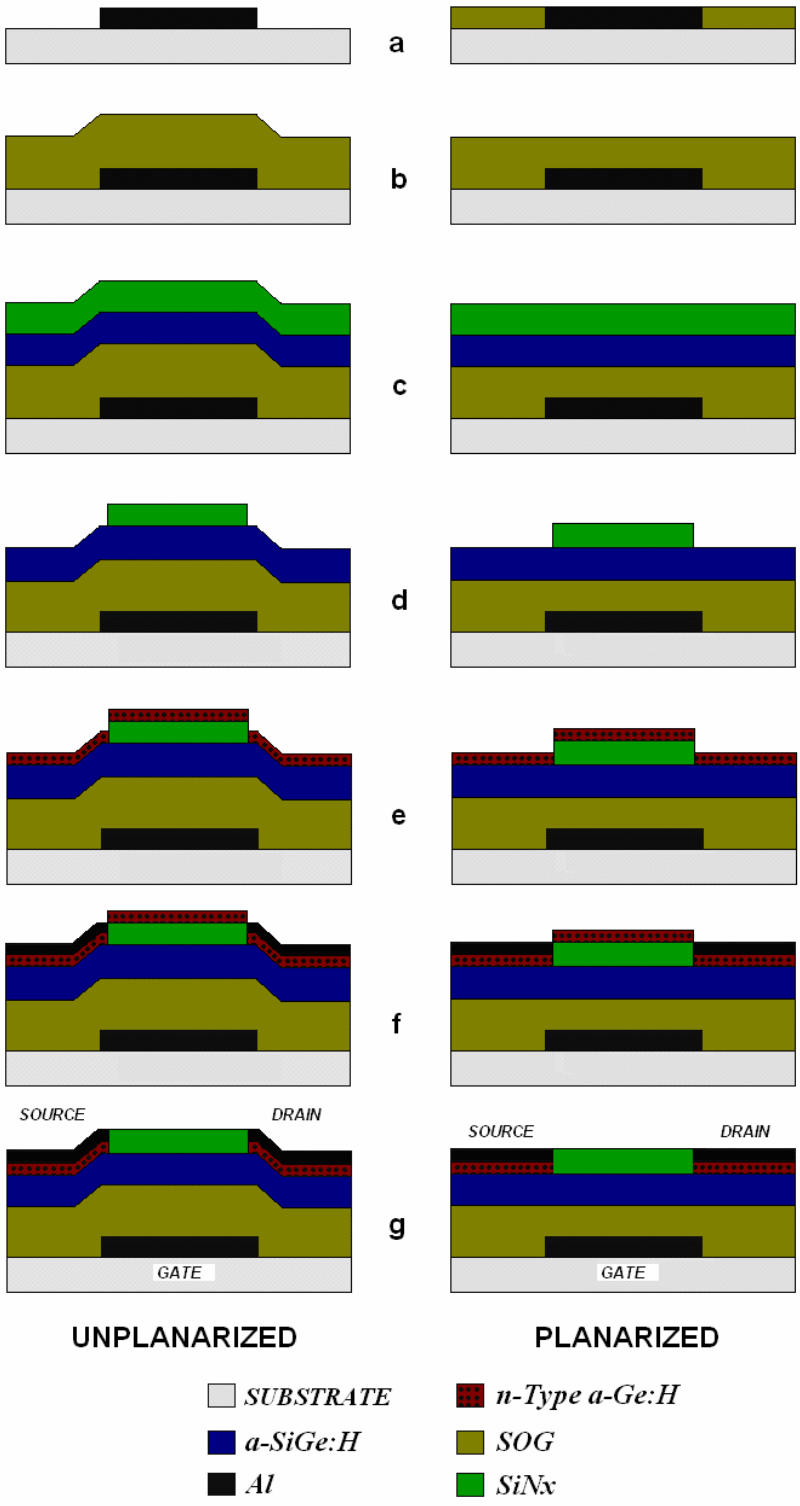


Fig 4.3 Process flow and cross section of the unplanarized and planarized a-SiGe:H TFTs using SiNx as passivation (not to scale).

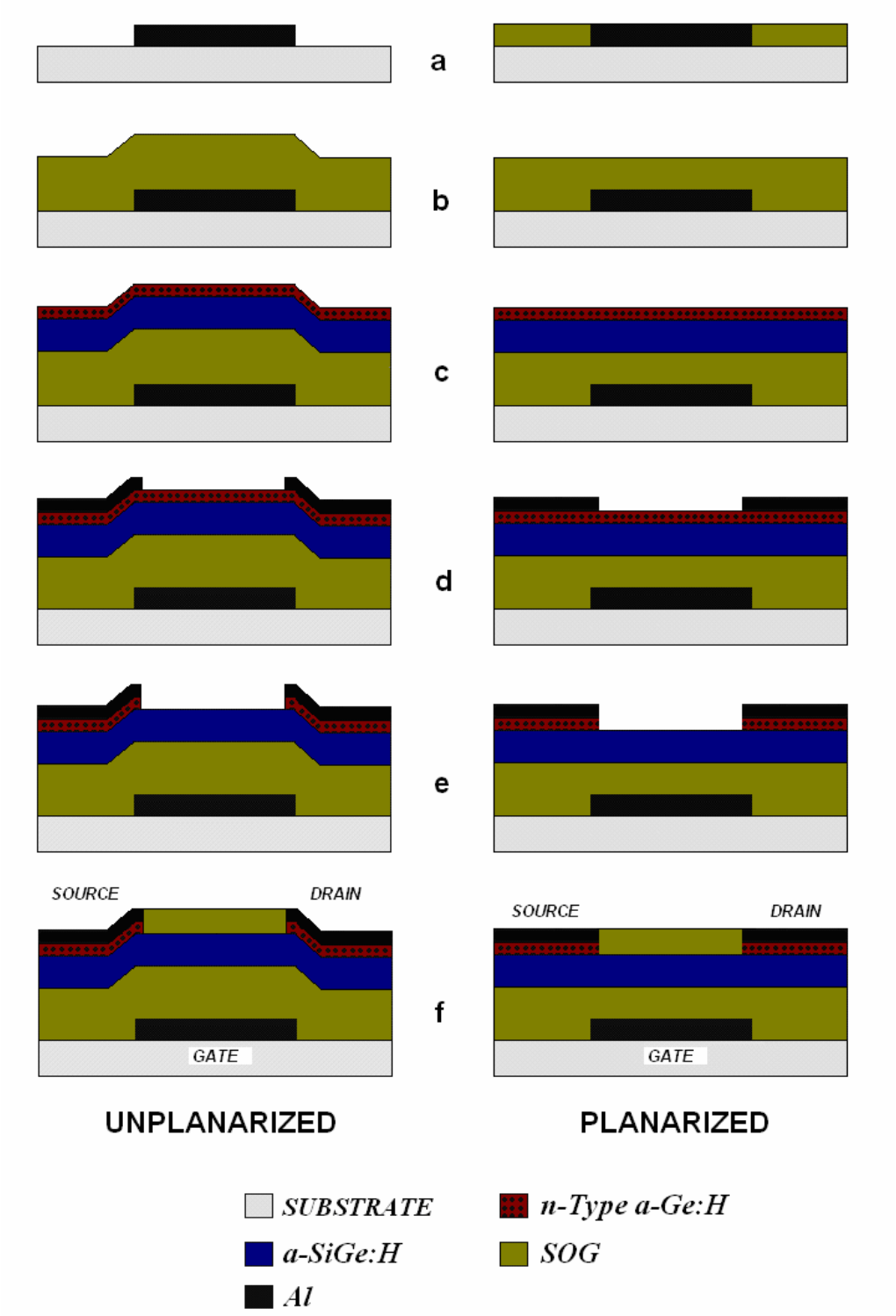


Fig 4.4 Process flow and cross section of the unplanarized and planarized a-SiGe:H TFTs using SOG as passivation (not to scale).

4.2 Characterization of Low-temperature a-SiGe:H TFTs.

In our knowledge, in literature has not been reported the effects of the deposition conditions in the performance of a-SiGe:H TFTs. Thus, just for compare the a-SiGe:H film with expected lower DOS presented in the previous chapter, it was used other 2 films with different GeH_4 flow to fabricate TFTs as depicted in table 4.1. The fabricated devices were unplanarized a-SiGe:H TFTs at 300 °C using SiNx as passivation on silicon wafers as substrate.

Table 4.1 Deposition conditions for the a-SiGe:H films at 300 °C.

a-SiGe:H	SiH4 (sccm)	GeH4 (sccm)	H2 (sccm)	Pow (W)	Temp (°C)	Pres (Torr)	Time (min)
I	45	25	1000	300	300	0.6	16
III	45	105	1000	300	300	0.6	13
V	45	185	1000	300	300	0.6	8.5

The electrical characterization of all devices was conducted using the *HP 4156B Semiconductor Parameter Analyzer*. All the measurements were done under dark conditions. Figure 4.5 shows the transfer characteristics of a-SiGe:H TFTs with different GeH_4 flow. The subthreshold slope was 0.9 V/DEC for TFTs with GeH_4 flow of 105 sccm, while for 25 sccm and 185 sccm were of 1.1 and 1.5 V/DEC, respectively. The V_T values were approximately 1V for TFTs with GeH_4 flow of 105 sccm and 3V for TFTs with GeH_4 flow of 25 and 185 sccm, respectively. Figure 4.6 show the subthreshold slope and on/off-current ratio versus GeH_4 flow. The lowest value of subthreshold slope, lowest value of V_T and highest on/off-current ratio for a-SiGe:H TFTs with

GeH_4 flow of 105 sccm could confirm our previous assumption that this film has a lower DOS. However, the device has a high off-current (~100 pA). The relation between off-current and bandgap versus GeH_4 flow for the a-SiGe:H TFTs is show in figure 4.7. The off-current increases with lower bandgap, as expected, due to the increment in the carrier concentration at thermal equilibrium. Low values of off-current are easily achieved in a-Si:H TFTs because of the typically low conductivity of the a-Si:H due to a larger bandgap (~1.8 eV). Therefore, to reduce the off-current and increase the on/off-current ratio of the a-SiGe:H TFTs it is necessary to increase the bandgap of the a-SiGe:H film maintaining their good electronic properties.

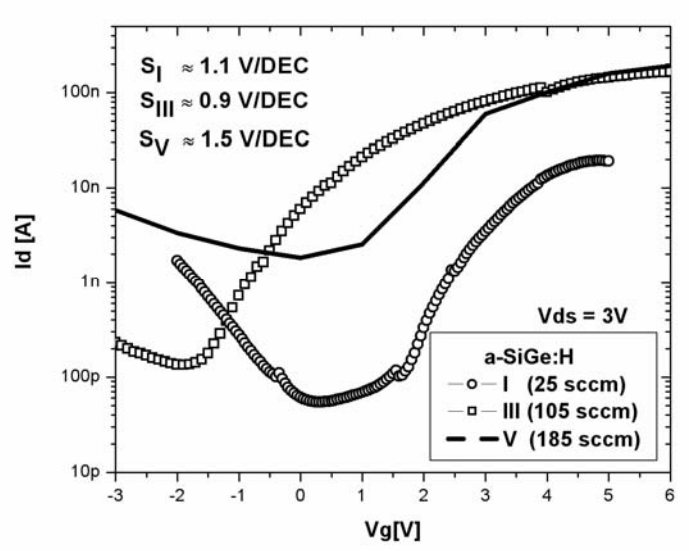


Fig 4.5 Transfer characteristics of the unplanarized a-SiGe:H TFTs using SiNx as passivation with different GeH_4 flow.

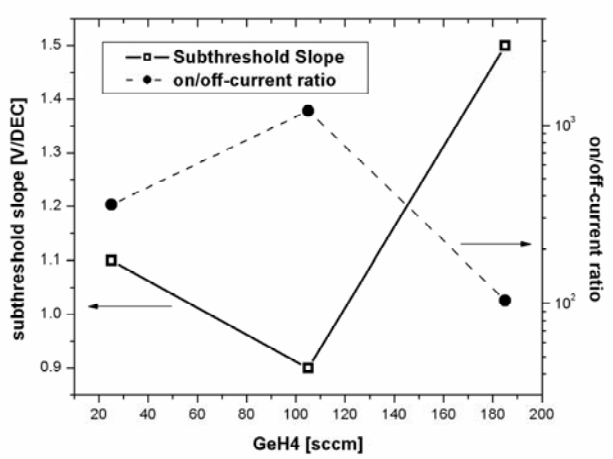


Fig 4.6 Subthreshold slope and on/off-current ratio as function of GeH_4 flow.

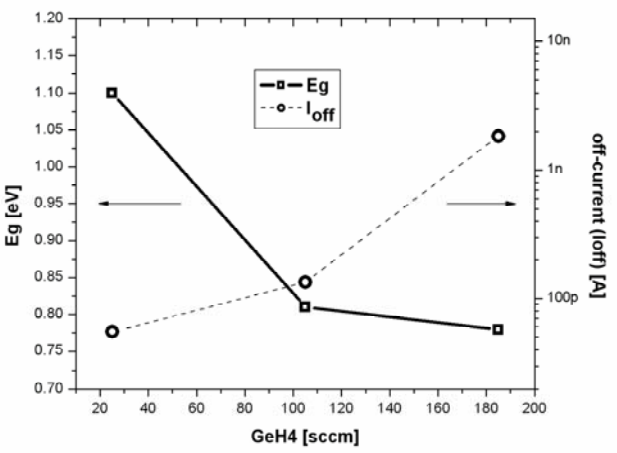
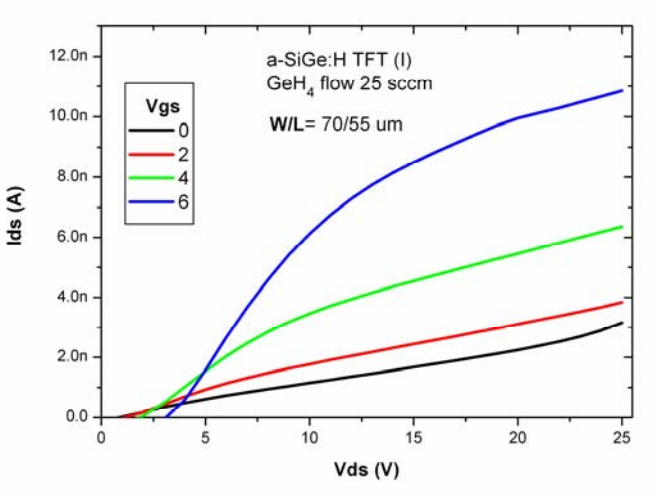


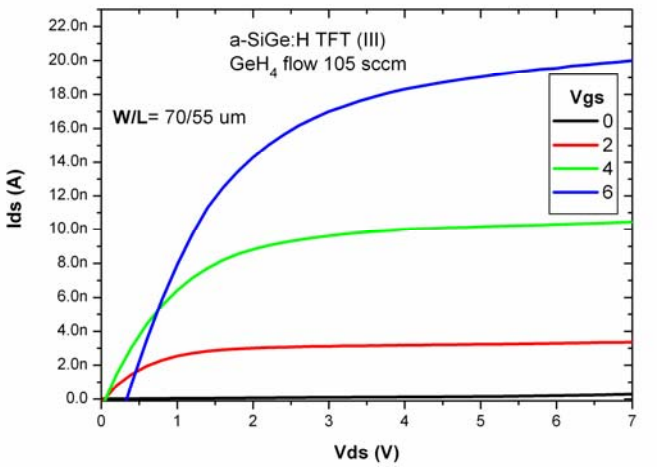
Fig 4.7 Off-current and bandgap as function of GeH_4 flow.

The output characteristics of the a-SiGe:H TFTs are shown in figure 4.8. A high contact resistance appears at the output characteristics in low bias range of Vds. This high contact resistance limits the on-current of the TFT and indicates a poor quality in the metal-semiconductor interface. However, a-SiGe:H TFTs with GeH_4 flow of 105 sccm (Fig. 4.8b) show a good saturation regime at high bias range of Vds. On the other hand, it can be seen in figure 4.8c that the a-SiGe:H TFT with GeH_4 flow of 185 sccm has higher driving current, however, this higher current is attributed to the

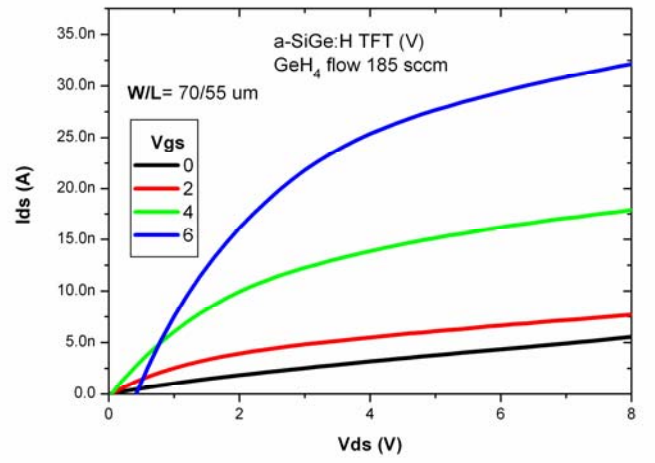
increment in the carrier concentration at thermal equilibrium resulted from the lower bandgap of the film, as indicate figure 4.7, but not due to a higher mobility. Also, its higher values of subthreshold slope and off-current do not make feasible the use of this film as active layer on TFTs.



a)



b)



c)

Fig 4.8 Output characteristics of the unplanarized a-SiGe:H TFTs using SiNx as passivation with different GeH_4 flow. a) 25 sccm, b) 105 sccm and c) 185 sccm.

Although the ambipolar behavior was not seen in the devices, the characterization served to find the relation between parameters of the device and properties of the film. Also, the effects of the deposition conditions of the active layer (GeH_4 flow) on the electrical characteristics of the a-SiGe:H TFTs were analyzed. Since the device and film with the best properties were obtained with GeH_4 flow of 105 sccm, SiH_4 flow of 45 sccm and H_2 flow of 1000 sccm, these conditions were used on the following a-SiGe:H TFTs. In the next subsections the characterization of a-SiGe:H TFTs fabricated at 200 °C is presented.

4.2.1 Characterization of planarized a-SiGe:H TFTs using SiNx as passivation fabricated at 200 °C.

It is pertinent to say that were only fabricated planarized a-SiGe:H TFTs using SiNx as passivation on corning 1737 substrates.

Considering the high contact resistance which appeared in the output characteristics of the a-SiGe:H TFTs at 300 °C, an interface preparation procedure is proposed. In order to improve the TFT performance, it has been

reported procedures which reduce the contact resistance and improve the main device interfaces [68-72]. In the inverted staggered structure, as the thickness of the active layer is reduced, the series resistance associated to this thickness decreases while the contact and channel resistances remain unchanged [73]. However, it is well know, that the DOS increases as the amorphous film becomes thinner. For this reason, an overetching in the source/drain regions of the active layer prior to deposit the n+ contact layer can reduce the series resistance of the TFT, without reducing the thickness of the active layer. Therefore, because the n+ contact layer and the induced-channel get close, some parameters can be improved such as the on/off-current ratio.

The procedure was done as follows: after the deposition of the a-SiGe:H and SiNx films above the SOG (Fig. 4.9a), the SiNx film was patterned as passivation film above the active layer using RIE (Fig. 4.9b). However, in this step, an overetching was done as shown in the Fig 4.9c. The time of the overetching was of 30 seconds (20% of the a-SiGe:H film thickness). After that, hydrogen plasma was done at 200 °C, with H_2 flow of 3500 sccm, pressure of 0.6 Torr and an RF power of 300 W for 5 minutes. To compare the effects of this hydrogen plasma in the electrical characteristics of the TFT, other TFTs without hydrogen plasma were done. Finally, the fabrication process continues as indicated in section 4.1 (Fig. 4.9d).

The transfer characteristics of planarized a-SiGe:H TFTs using SiNx as passivation on corning 1737 substrates with and without applied hydrogen plasma are shown in figure 4.10. Better electrical characteristics, such as subthreshold slope, on-current, off-current and on/off-current ratio, are observed for a-SiGe:H TFTs with applied hydrogen plasma. The poor electrical characteristics of a-SiGe:H TFTs without hydrogen plasma application are due to plasma-induced damage occasioned by the overetching process [74, 75].

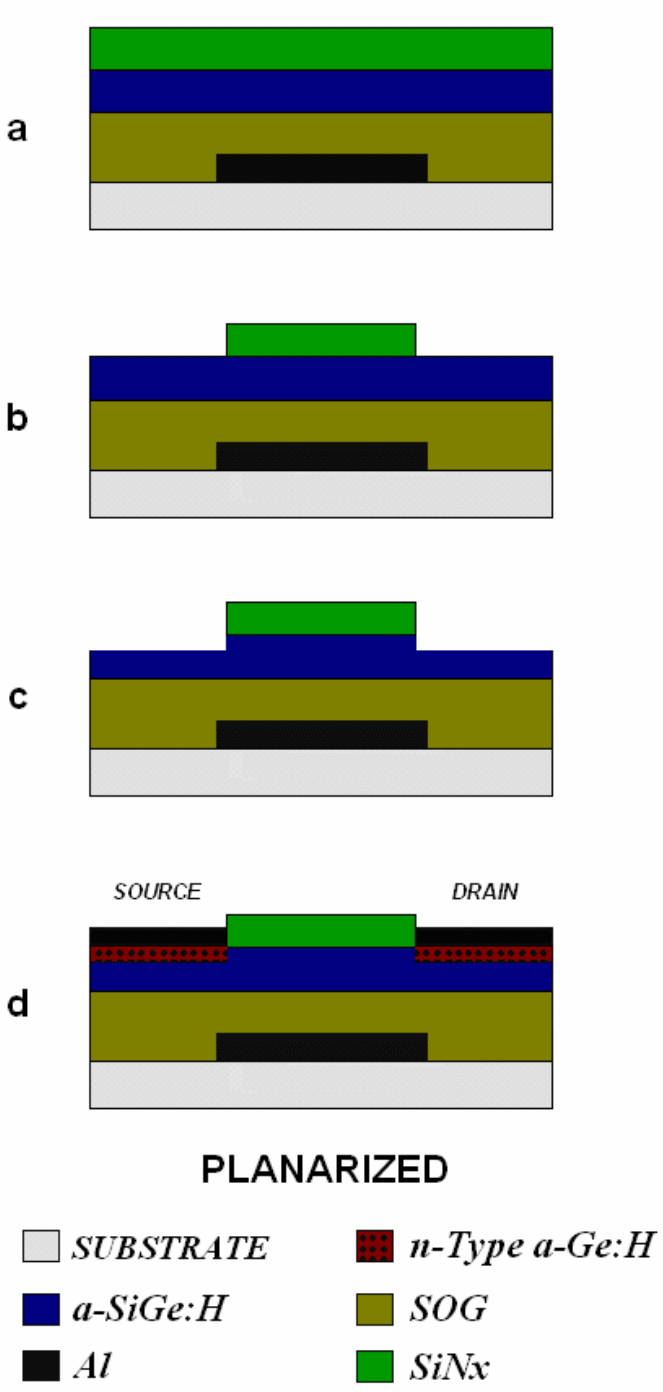


Fig 4.9 Process flow and cross section of the planarized a-SiGe:H TFTs with an overetching in the contact regions (not to scale).

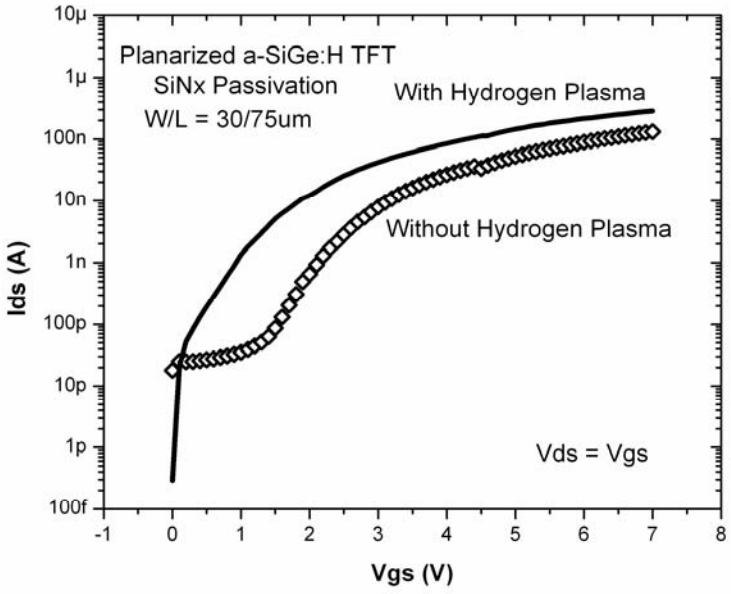


Fig 4.10 Transfer characteristics of the planarized a-SiGe:H TFTs using SiNx as passivation with and without hydrogen plasma.

The subthreshold slopes values for the a-SiGe:H TFTs with and without applied hydrogen plasma were 0.56 and 0.61 V/DEC, respectively. The N_T and D_{it} values for a-SiGe:H TFTs were of $2.64x10^{17}$ $cm^{-3}eV^{-1}$ and $2.64x10^{12}$ $cm^{-2}eV^{-1}$ for TFTs with applied hydrogen plasma, respectively, and for TFTs without hydrogen plasma application the values were of $2.88x10^{17}$ $cm^{-3}eV^{-1}$ and $2.88x10^{12}$ $cm^{-2}eV^{-1}$, respectively. Because the error estimates of the subthreshold slope are ±0.03 V/DEC for both a-SiGe:H TFTs, the differences in subthreshold slope, N_T and D_{it} values are considered as a statistical fluctuation. Since both of the a-SiGe:H TFTs have identical insulator-semiconductor interface and the overetching process only affects the source/drain regions, we do not expect any difference in the quality of the insulator-semiconductor interface of the devices.

Figure 4.11 shows the transfer characteristics of the planarized a-SiGe:H TFTs using SiNx as passivation with applied hydrogen plasma at different Vds voltages. It can be observed an on/off-current ratio approximately of 10^6 and an off-current approximately of 300 fA at 0 Vgs.

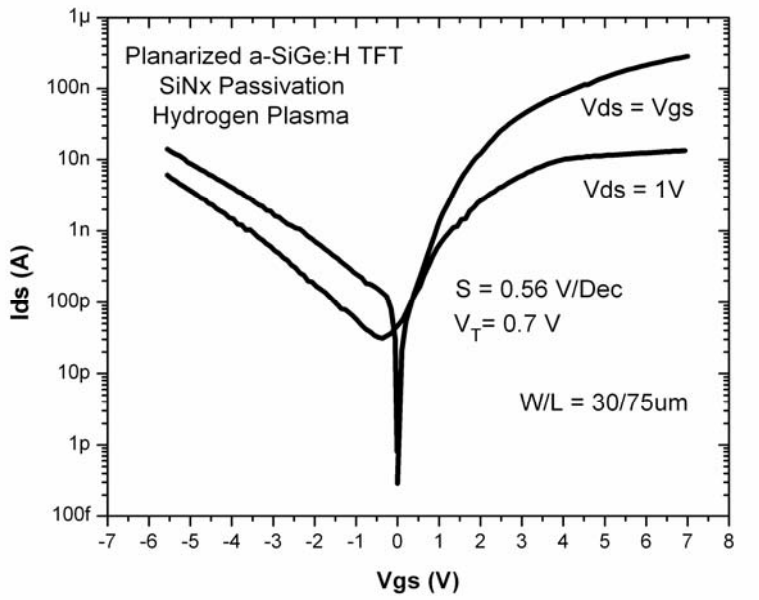


Fig 4.11 Transfer characteristics of the planarized a-SiGe:H TFTs using SiNx as passivation with hydrogen plasma at different Vds.

Figure 4.12 shows the relation between square root of Ids and Vgs of the TFT at saturation mode (Vds = Vg). In this relation the threshold voltage and field-effect mobility can be extracted from the intercept with Vg axis, using the equation 2.2 for the saturation region. The measured threshold voltage and field-effect mobility for planarized a-SiGe:H TFTs were of 0.7 V and 0.85 cm^2/Vs for TFTs with applied hydrogen plasma, respectively, while 1.86 V and 0.52 cm^2/Vs were for TFTs without applied hydrogen plasma, respectively. It is well known that hydrogen saturates dangling bonds in the amorphous film. Thus, since the mobility can be affected by the quality of the metal-semiconductor interface, the higher mobility means that the applied hydrogen plasma improves the metal-semiconductor interface by reducing the plasma-induced damage and, hence, the contact resistance. Because the SiNx passivation film could let remains between the n+ contact layer and a-SiGe:H active layer due to process variations, the overetching process assures the etching of the SiNx passivation film and gets close the n+ contact layer and the electron induced-channel at positive gate bias.

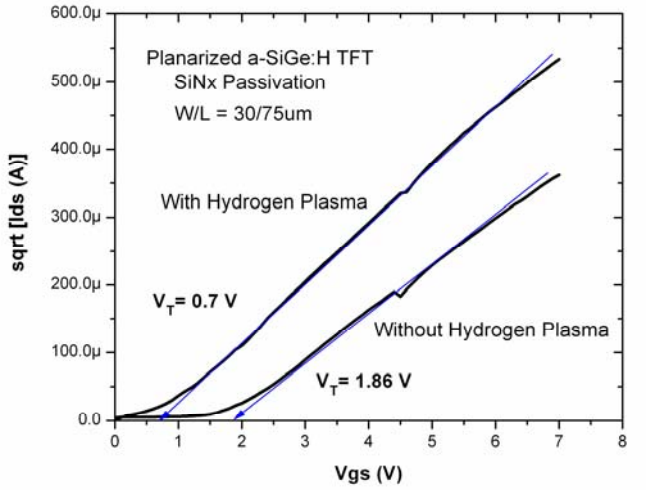
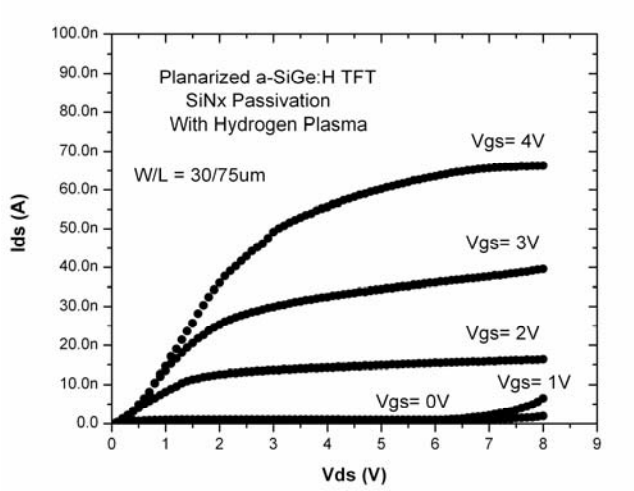
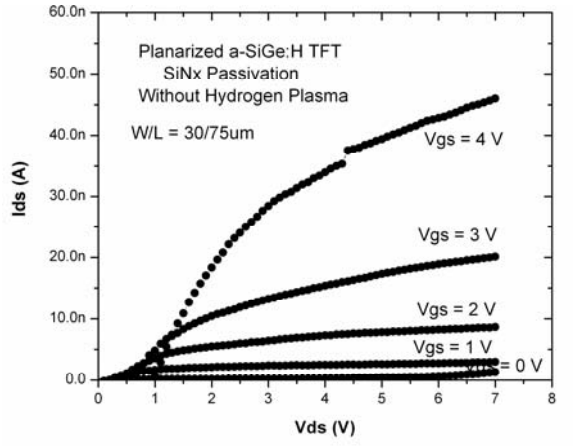


Fig 4.12 Square root of Ids vs Vgs of planarized a-SiGe:H TFTs with and without hydrogen plasma at Vg = Vds (saturation).

From the figure 4.13 can be observed the improvement in the metal-semiconductor interface for planarized TFTs with applied hydrogen plasma. In the output characteristics of TFTs without applied hydrogen plasma a high contact resistance appears in the bias range of 0 to 1V of Vds. The high contact resistance not appears in TFTs with applied hydrogen plasma. Also, the values of Ids of TFTs with applied hydrogen plasma indicate their better driving current capability.



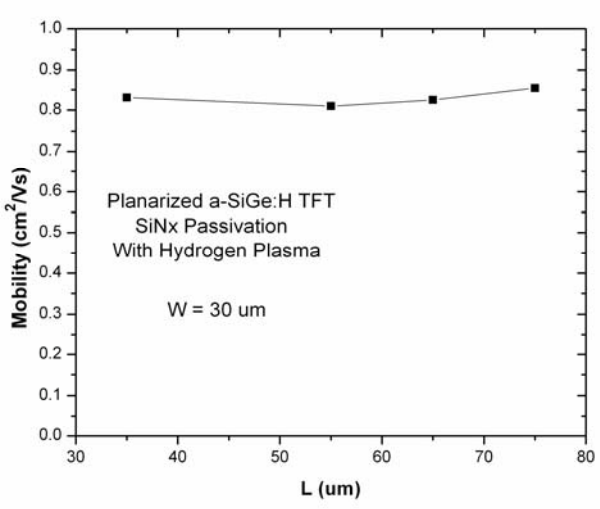
a)



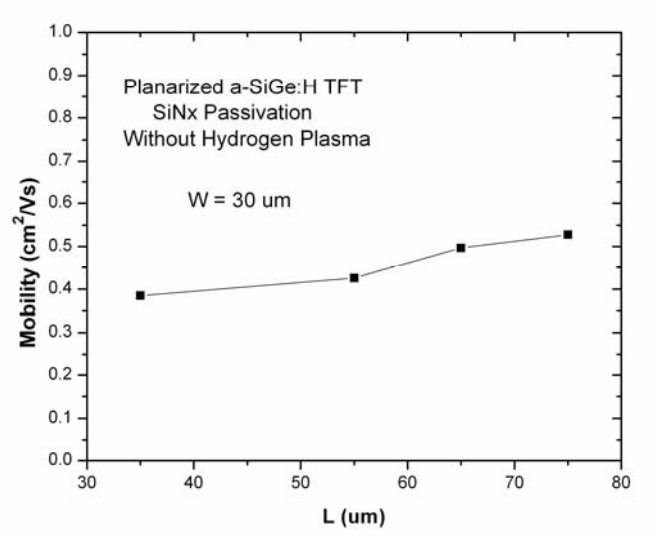
b)

Fig 4.13 Output characteristics of planarized a-SiGe:H TFTs using SiNx as passivation, a) with and b) without hydrogen plasma.

Figure 4.14 shows the dependency of field-effect mobility on the channel length for planarized a-SiGe:H TFTs with and without hydrogen plasma application. For a-SiGe:H TFTs without hydrogen plasma application there is a dependency product of the high contact resistance, while for a-SiGe:H TFTs with applied hydrogen plasma there is no dependency of the field-effect mobility on the channel length confirming the good quality of the metal-semiconductor interface.



a)



b)

Fig 4.14 Dependence of field-effect mobility on the channel length for planarized a-SiGe:H TFTs, a) with and b) without hydrogen plasma.

The above results confirm that plasma-induced damage by the overetching process is reduced with the applied hydrogen plasma and the interface preparation procedure in the source/drain regions leads to form good ohmic contacts. Also, is clear the improvement in the insulator-semiconductor interface by the planarization of the gate. These interfaces improvements translate in higher mobility, lower off-current, higher on-current, higher on/off-current ratio, lower subthreshold slope and lower V_T when are compared to the unplanarized a-SiGe:H TFTs fabricated at 300°C. More detailed description of the effects of the planarization process in the electrical characteristics of the TFTs is presented in chapter 5.

In order to compare the effects of the overetching process, a-SiGe:H TFTs with a higher overetching were fabricated. The time of the overetching was of 2 minutes (80% of the a-SiGe:H film thickness). Also, hydrogen plasma and thermal treatment were done.

The transfer characteristics of planarized a-SiGe:H TFTs using SiNx as passivation with higher overetching on corning 1737 substrates are shown in

figure 4.15. Poor electrical characteristics are obtained, even with the applied hydrogen plasma and thermal treatment, the subthreshold slope was of 0.98 V/DEC, the on/off-current ratio was approximately 10^3 and the off-current was approximately 200 pA at 0 Vgs.

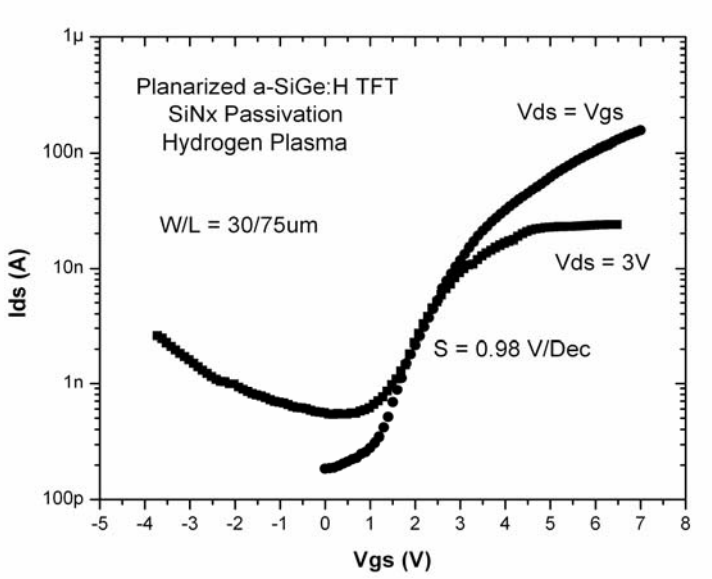


Fig 4.15 Transfer characteristics of planarized a-SiGe:H TFTs using SiNx as passivation with higher overetching on corning 1737 substrates.

The calculated maximum values of the trap density in the active layer a-SiGe:H (N_T) and in the SOG/a-SiGe:H interface (D_{it}) were $4.63x10^{17}$ $cm^{-3}eV^{-1}$ and $4.63x10^{12}$ $cm^{-2}eV^{-1}$, respectively.

Since the subthreshold slope is related to the quality of the insulator-semiconductor interface and the higher overetching process finishes near of this interface, the higher value of subthreshold slope may be because the higher overetching process could induce damage near of the insulator-semiconductor interface.

Figure 4.16 shows the relation between square root of Ids and Vgs of the TFT at saturation mode (Vds = Vg). The measured threshold voltage and

field-effect mobility for the planarized a-SiGe:H TFTs were of 1.58 V and 0.56 cm^2/Vs, respectively.

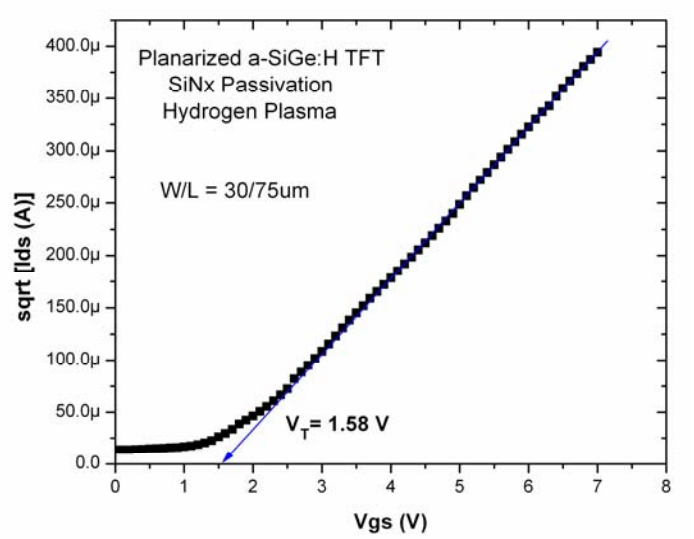


Fig 4.16 Square root of Ids and Vgs of the planarized a-SiGe:H TFTs using SiNx as passivation with higher overetching at saturation mode (Vds = Vg).

On the other hand, in the output characteristics a high contact resistance appears in the bias range of 0 to 1V of Vds (Fig. 4.17). This high contact resistance causes a dependency of field-effect mobility on the channel length. Figure 4.18 show the field-effect mobility as function of the channel length for the planarized a-SiGe:H TFTs.

From these results, the poor quality in the metal-semiconductor interface by the higher overetching process is evident. The plasma-induced damage results in high contact resistance and cannot be reduced even with the applied hydrogen plasma and thermal treatment.

Previously it was mentioned that we did not expect any difference in the quality of the insulator-semiconductor interface of the devices, since the overetching process only affects the source/drain regions. However, the increase in the value of the subthreshold slope from 0.56 to 0.98 V/DEC is not explained at all by the high contact resistance [43]. Therefore, the

subthreshold behavior may also be affected by other mechanism and the plasma-induced damage near of the insulator-semiconductor interface by the higher overetching process seems to be the main reason.

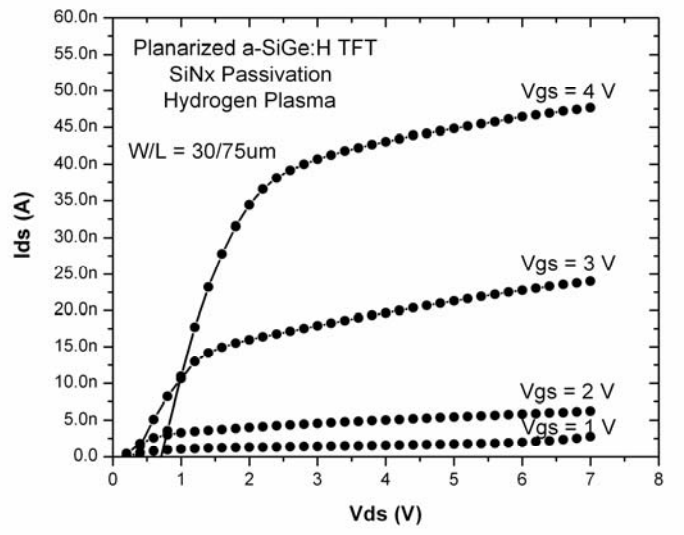


Fig 4.17 Output characteristics of planarized a-SiGe:H TFTs using SiNx as passivation with higher overetching.

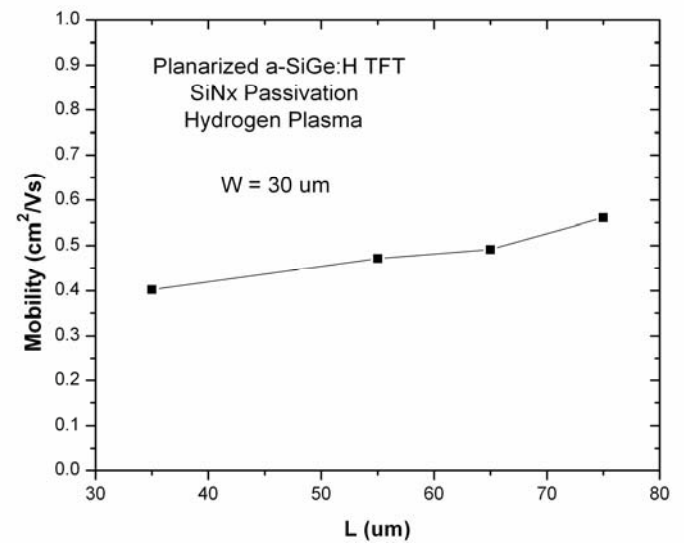


Fig 4.18 Dependence of field-effect mobility on the channel length for planarized a-SiGe:H TFTs using SiNx as passivation with higher overetching.

The ambipolar behavior was not seen in the planarized devices, probably due to the SiNx as passivation or/and to the final steps of the fabrication process, such as deposit (above the active layer) the passivation film instead of the contact region film. For corroboration of this assumption, in the next section, the characterization of unplanarized and planarized a-SiGe:H TFTs using SOG as passivation is presented and discussed.

4.2.2 Characterization of the unplanarized and planarized a-SiGe:H TFTs using SOG as passivation fabricated at 200 °C.

In this section, the characterization of unplanarized and planarized a-SiGe:H TFTs using SOG as passivation is presented. In these devices, above the active layer, the contact region film is deposited first instead of the passivation film (see section 4.1). For the characterization of the a-SiGe:H TFTs, first, unplanarized TFTs were fabricated on silicon wafers as substrate at 200 °C. After that, unplanarized and planarized TFTs were fabricated on corning 1737 substrates at 200 °C.

Figure 4.19 shows the transfer characteristics of the unplanarized a-SiGe:H TFT on silicon wafer. For positive gate bias, the a-SiGe:H TFTs show a subthreshold slope of 0.32 V/DEC. For negative gate bias, the transfer characteristic shows a p-type TFT behavior with a subthreshold slope of 0.18 V/DEC. On the other hand, the on/off-current ratio was 10^5 for the n-type region and 10^4 for the p-type region. The off-current for both regions was approximately 2 pA at 0 Vgs.

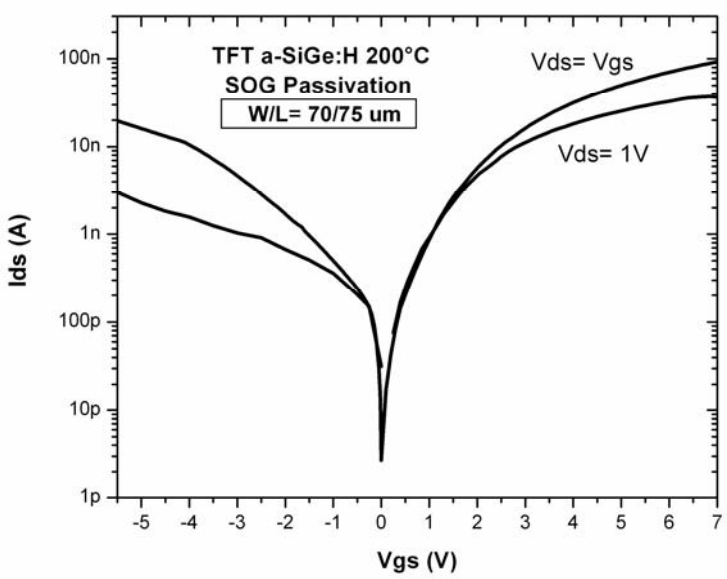
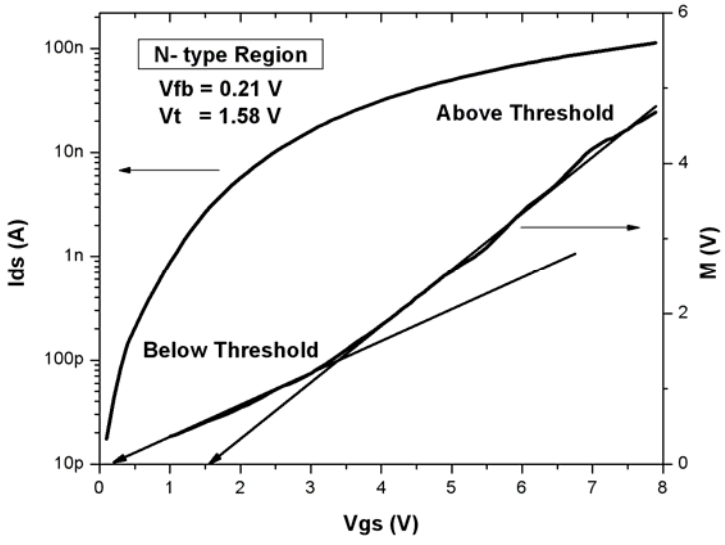
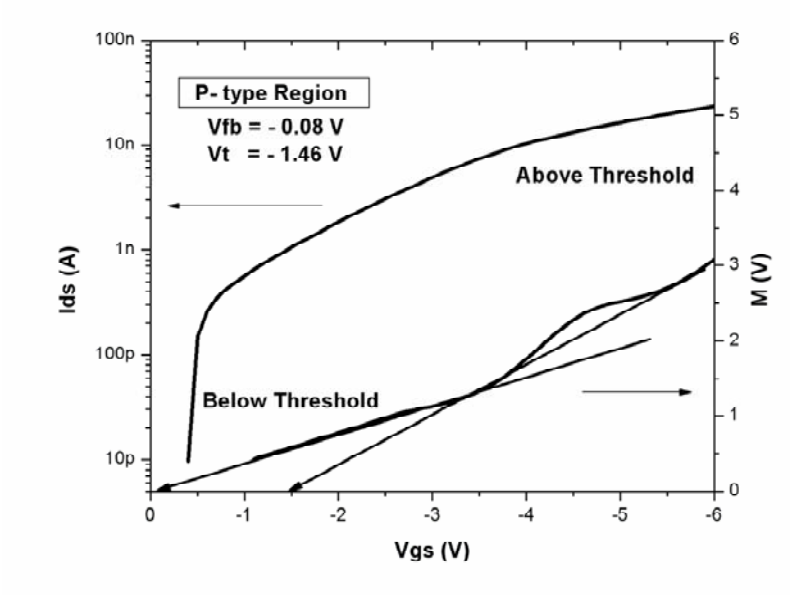


Fig 4.19 Transfer characteristics of the unplanarized a-SiGe:H TFTs using SOG as passivation on silicon wafers.

It was used the method proposed by B. Wu et al [18], described in section 2.2, to extract the most important parameters of the ambipolar TFTs. Figure 4.20 shows the plot of the M curves for n- and p-type regions, the V_T and flat-band voltages values were 1.58 and 0.21 V for n-type region and -1.46 and -0.08 V for p-type region, respectively. Table 4.2 summarizes results of the electrical measurements.



a)



b)

Fig 4.20 Ids and M curves for the a) n-type and b) p-type regions of unplanarized a-SiGe:H TFTs using SOG as passivation on silicon wafers.

Table 4.2 Parameters of the unplanarized a-SiGe:H TFTs using SOG as passivation on silicon wafers.

Parameter	**p-type Region**	**n-type Region**
V_T	-1.46 V	1.58 V
Vfb	-0.08 V	0.21 V
$\|V_T - Vfb\|$	1.38 V	1.37 V
ΔVfb	0.29 V	
E_{D2}, E_{A2}	72 meV	35 meV
SS	0.15 V/DEC	0.34 V/DEC

The characteristic energies of deep localized states for a-SiGe:H films are lower than those presented by a-Si:H films [18, 40]. This is because the a-SiGe:H film has a higher DOS due to the incorporation of Ge. On the other hand, as expected, the flat-band voltages are lower than the threshold voltages for each region. The difference in flat-band voltages, for the n-type and p-type regions, is due to the trapping and detrapping of charge carriers between the a-SiGe:H film and the SOG insulator [47]. Electrons are trapped in the n-type region and holes are trapped in the p-type region. Thus, the flat-band voltage for the n-type region is more positive than that observed for the p-type region.

The measured field-effect mobility was of 0.4 cm^2/Vs for n-type region, while 0.06 cm^2/Vs was for p-type region, respectively. Considering that hole mobility in a-Si:H is almost two orders of magnitude smaller than the electron mobility, which makes unfeasible the application of p-type a-Si:H TFTs, the hole mobility (p-type region) obtained shows a considerable improvement.

Figure 4.21 shows the output characteristics of the unplanarized ambipolar a-SiGe:H TFTs for both positive and negative gate bias. For positive gate bias, the output characteristics show a high contact resistance which appears at low Vds voltages. For negative gate bias, the output characteristics show an exponential behavior, however, it can be see a good modulation of the p-type channel with the applied gate bias. This behavior is also reported in ambipolar nanocrystalline silicon TFTs [21, 22].

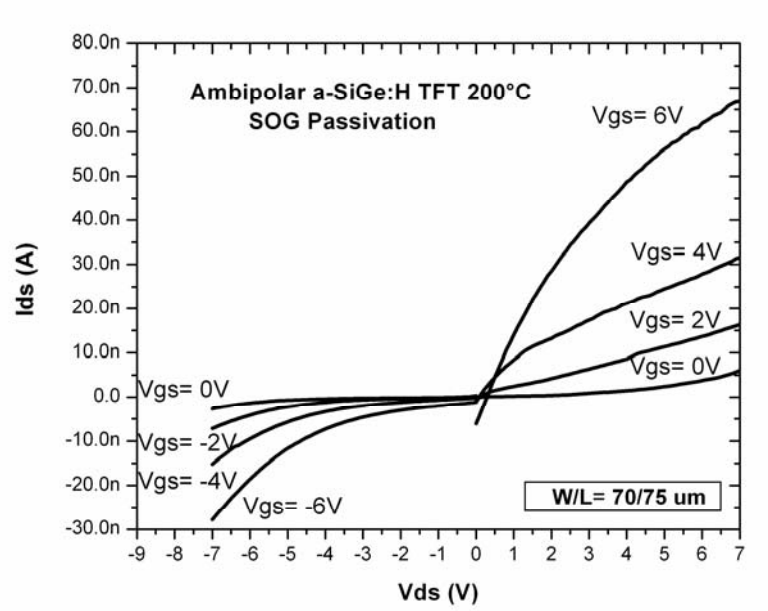


Fig 4.21 Output characteristics of the unplanarized ambipolar a-SiGe:H TFTs for both positive and negative gate bias on silicon wafers.

Ambipolar behavior is observed in unplanarized a-SiGe:H TFTs using SOG as passivation on silicon wafers as substrate. However, the aim of this thesis is propose the low-temperature ambipolar a-SiGe:H TFTs in flexible and large-area electronics, where rough substrates (like plastic, glass or some flexible substrates) are used. Therefore, in order to assess the impact of the rough substrates on the performance of the low-temperature ambipolar a-SiGe:H TFTs, these were fabricated on Corning 1737 substrate at 200 °C. Unplanarized and planarized a-SiGe:H TFTs were fabricated as was indicated in section 4.1.

Figure 4.22 shows the transfer characteristics of the unplanarized and planarized a-SiGe:H TFT on Corning 1737. For positive gate bias both unplanarized and planarized a-SiGe:H TFTs show an n-type TFT behavior, whereas for negative gate bias show a p-type TFT behavior. As expected, the planarized a-SiGe:H TFTs show better electrical characteristics. For positive gate bias, the planarized TFT show a subthreshold slope of 0.45 V/DEC while unplanarized TFT shows approximately 1 V/DEC. For negative gate bias, the

planarized TFT show a subthreshold slope of 0.49 V/DEC while unplanarized TFT shows 1.3 V/DEC. On the other hand, for planarized TFTs the on/off-current ratio was 10^5 for the n-type region and close to 10^5 for the p-type region, while for unplanarized TFTs was close to 10^4 for the n-type region and 10^3 for the p-type region. The off-current of the planarized TFTs for both regions was approximately 0.95 pA at 0 Vgs, while of the unplanarized TFTs for both regions was 11 pA at 0 Vgs.

Figure 4.23 shows the transfer characteristics of the planarized a-SiGe:H TFTs using SOG as passivation at different Vds voltages. Figure 4.24 shows the plot of the M curves for n- and p-type regions, the V_T and flat-band voltages values were 1.11 and 0.16 V for n-type region and -2.18 and -0.29 V for p-type region, respectively. Table 4.3 summarizes results of the electrical measurements.

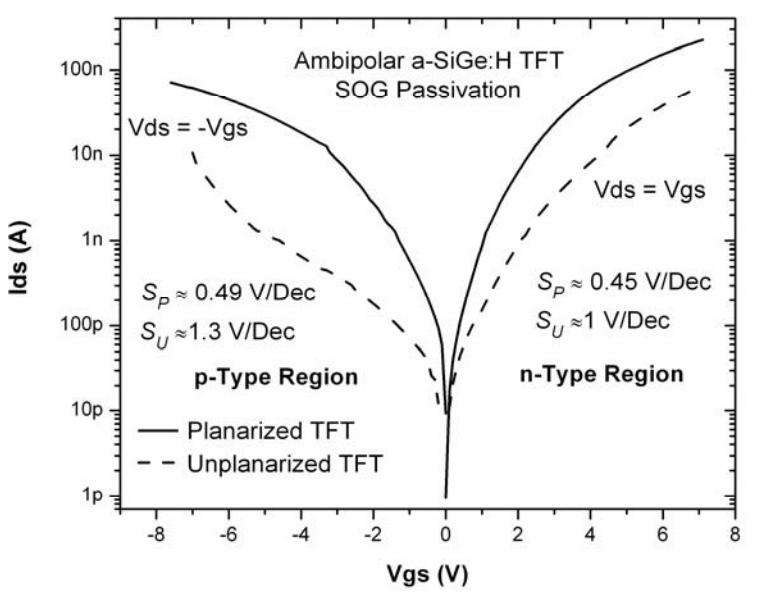


Fig 4.22 Transfer characteristics of the unplanarized and planarized ambipolar a-SiGe:H TFTs on Corning 1737.

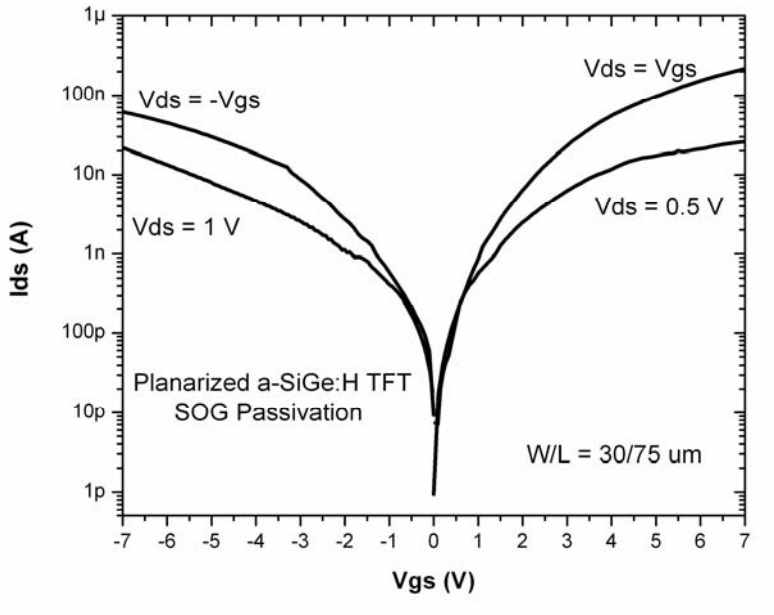
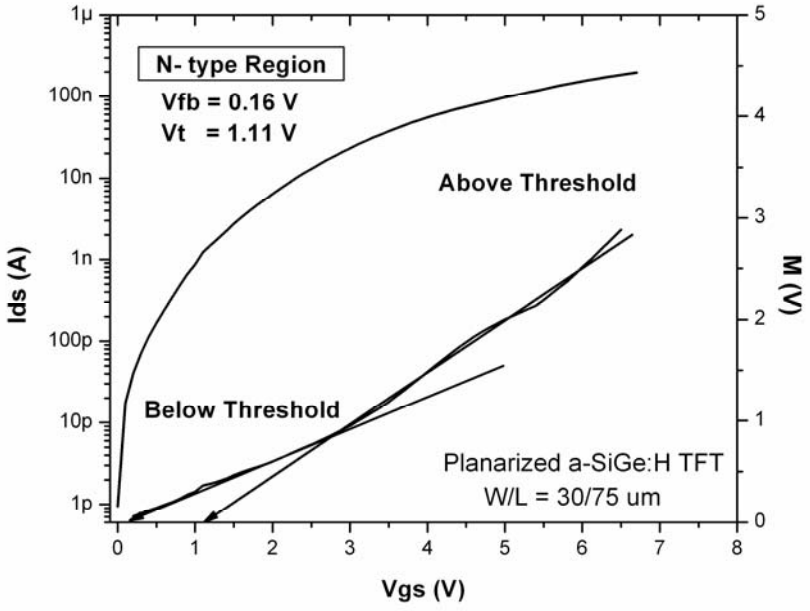
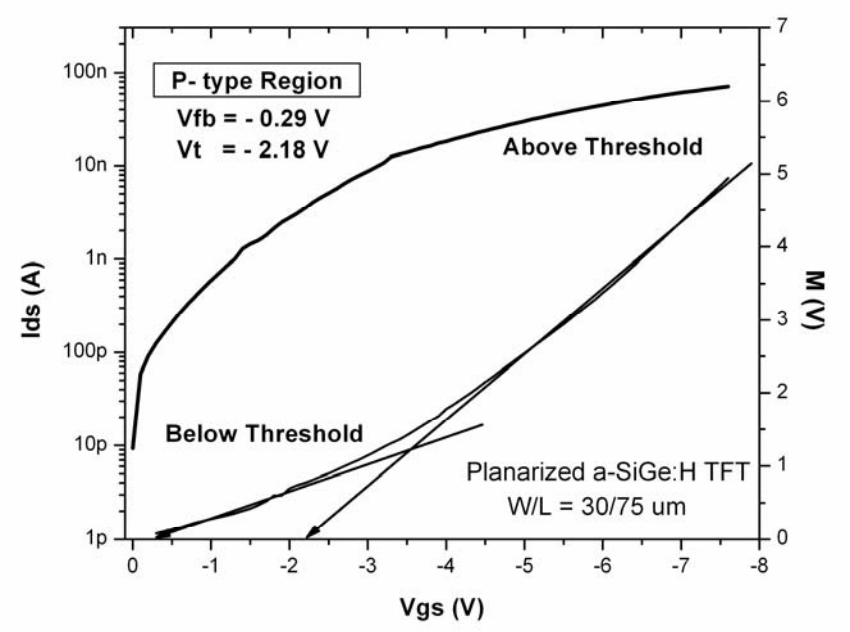


Fig 4.23 Transfer characteristics of the planarized ambipolar a-SiGe:H TFTs on Corning 1737 at different Vds voltages.



a)



b)

Fig 4.24 Ids and M curves for the a) n-type and b) p-type regions for planarized ambipolar a-SiGe:H TFT on Corning 1737.

Table 4.3 Parameters of the planarized ambipolar a-SiGe:H TFTs on Corning 1737.

Parameter	**p-type Region**	**n-type Region**
V_T	-2.18 V	1.11 V
Vfb	-0.29 V	0.16 V
$\|V_T - Vfb\|$	1.89 V	0.95 V
ΔVfb	0.45 V	
E_{D2}, E_{A2}	47 meV	26 meV
SS	0.49 V/DEC	0.45 V/DEC

The characteristic energies of deep localized states for a-SiGe:H films on corning 1737 are lower than those presented on silicon wafers. This is due to the roughness of the corning 1737 substrate which results in higher DOS. Considering that the DOS reflects contributions from interfaces, the characteristics energies obtained agree with the measured electrical characteristics where the subthreshold slopes for ambipolar TFTs on silicon wafers are better than those for ambipolar TFTs on corning 1737.

The measured field-effect mobility was of 0.68 cm^2/Vs for n-type region, while 0.15 cm^2/Vs was for p-type region, respectively. The hole mobility (p-type region) obtained is of the same order of magnitude than mobility of electrons (n-type region). The value of electron mobility of planarized ambipolar a-SiGe:H TFTs is in the range of low temperature a-Si:H TFTs mobilities [62, 76].

Figure 4.25 shows the output characteristics of the planarized ambipolar a-SiGe:H TFTs for both positive and negative gate bias. For positive gate bias, the high contact resistance not appears at low Vds voltages. For negative gate bias, the output characteristics also show an exponential behavior with a good modulation of the p-type channel with the applied gate bias. Figure 4.26 show the field-effect mobility as function of the channel length for the planarized ambipolar a-SiGe:H TFTs. There is no dependency of the mobility on the channel length which confirms the good ohmic contacts with low contact resistance.

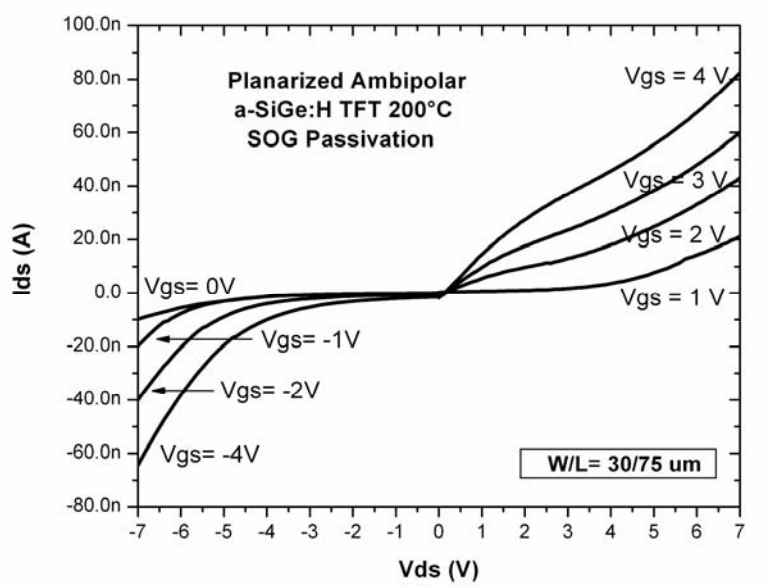


Fig 4.25 Output characteristics of the planarized ambipolar a-SiGe:H TFTs on Corning 1737 for both positive and negative gate bias.

Figure 4.27 shows the output characteristics of the unplanarized ambipolar a-SiGe:H TFTs as positive gate bias. A high contact resistance appears in the bias range of 0 to 2V of Vds.

From the comparison of the performance of unplanarized and planarized ambipolar a-SiGe:H TFTs, the improvement at the interfaces of the device can be seen. The quality of the insulator-semiconductor interface was improved because the planarization process causes a better distribution of the electric field around the corners of the gate. On the other hand, it is complicated to give an explanation why the planarization process which affects the corners of the gate can improve the metal-semiconductor interface (contact resistance). In chapter 5, these effects are explained using numerical simulations by ATLAS (Silvaco).

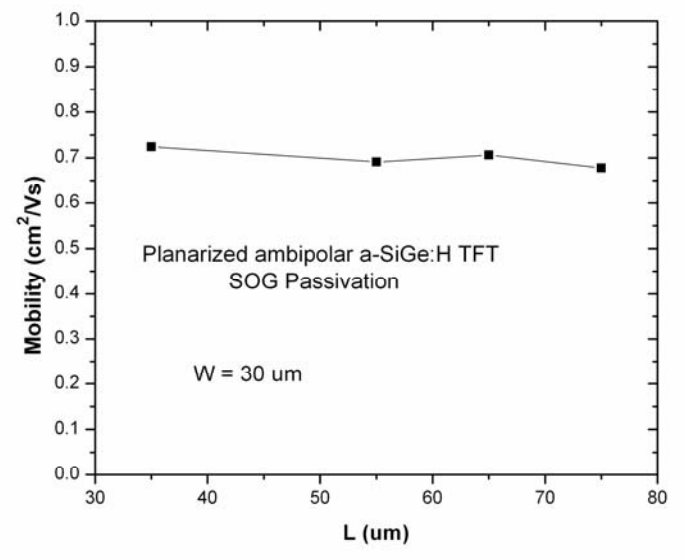


Fig 4.26 Field-effect mobility as function of the channel length for n-type region of planarized ambipolar a-SiGe:H TFTs on Corning 1737.

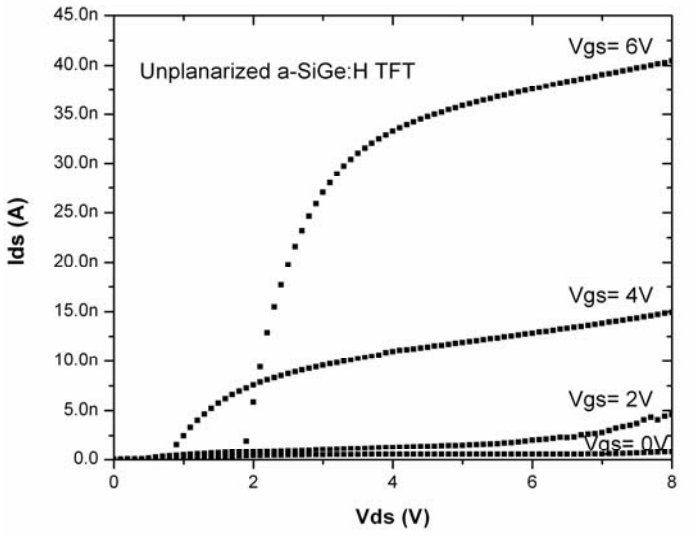
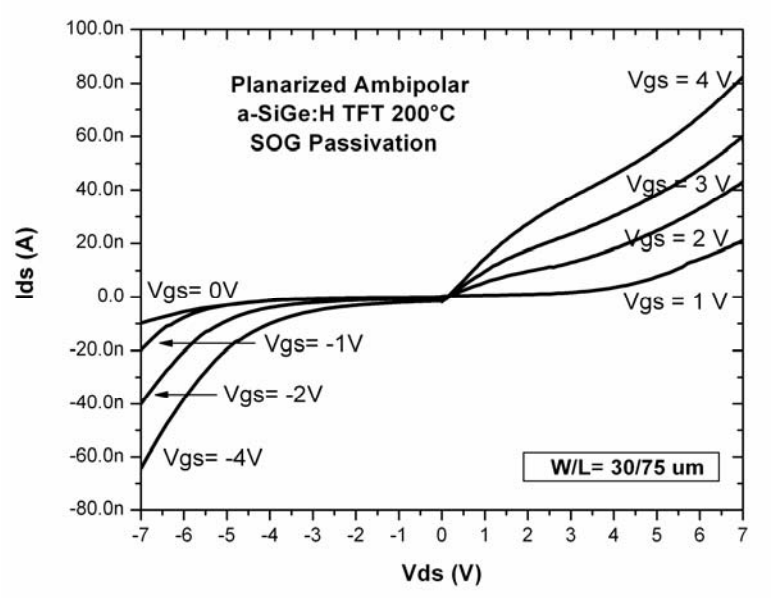


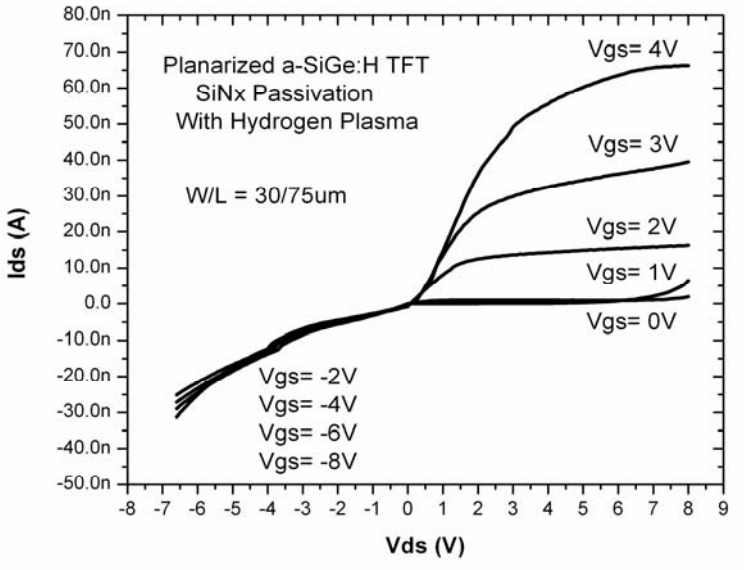
Fig 4.27 Output characteristics for n-type region of unplanarized ambipolar a-SiGe:H TFTs on Corning 1737.

In summary, the ambipolar behavior was not seen in the planarized a-SiGe:H TFTs using SiNx as passivation. However, unplanarized and planarized a-SiGe:H TFTs using SOG as passivation showed ambipolar behavior. In these devices, above the active layer, the contact region film was

deposited first instead of the passivation film (see section 4.1). This lead to form ohmic contacts instead of blocking contacts at negative gate bias as show figure 4.28. Blocking contacts in a-SiGe:H TFTs using SiNx as passivation were observed at negative gate bias (Fig 4.28b).



a)



b)

Fig 4.28 Output characteristics of the planarized a-SiGe:H TFTs. a) Using SOG and b) SiNx as passivation.

At the current time in which this work is defended, we demonstrate for the first time low- temperature ambipolar a-SiGe:H TFTs using the inverted staggered structure. A direct comparison of threshold voltage, subthreshold slope or mobilities between our devices and reported ambipolar devices is not possible because of the inherently different nature of the insulator-semiconductor interface in the top-gate structure used in reported ambipolar TFTs versus bottom-gate structure used in this thesis.

4.3 Stability of planarized a-SiGe:H TFTs.

One of the main drawbacks of TFTs based on a-Si:H is the threshold voltage shift (ΔV_T) as a result of a prolonged application of high electric field in the gate (gate bias stress). Charge trapping in the gate dielectric and defect creation in the channel layer are the two most important reasons for threshold voltage shift. Figure 4.29 shows the threshold voltage shift as function of the stress time, at gate bias stress of 20V and Vds = 0V, obtained for the planarized a-SiGe:H TFT using SiNx as passivation on Corning 1737. For the applied gate bias stress, the threshold voltage increases with the stress time.

Figure 4.30 shows the transfer characteristics of the a-SiGe:H TFT before and after of the applied gate bias stress. It can be seen that the on-current is almost two orders less after stress time of 6000 seconds than before the gate bias stress.

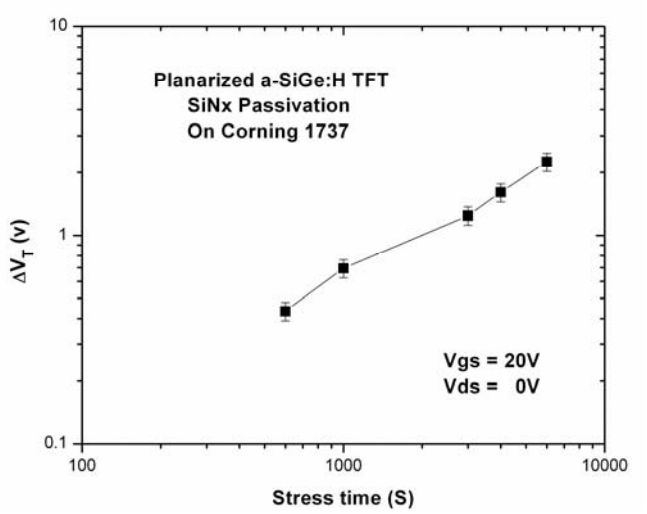


Fig 4.29 Threshold voltage shift (ΔV_T) with the stress time for planarized a-SiGe:H TFT using SiNx as passivation, at gate bias stress of 20V and Vds = 0V.

Figure 4.31 shows the threshold voltage shift as function of the stress time, at gate bias stress of 20V and Vds = 0V, obtained for the unplanarized ambipolar a-SiGe:H TFT on Corning 1737. The figure shows the threshold voltage shift for n-type and p-type regions.

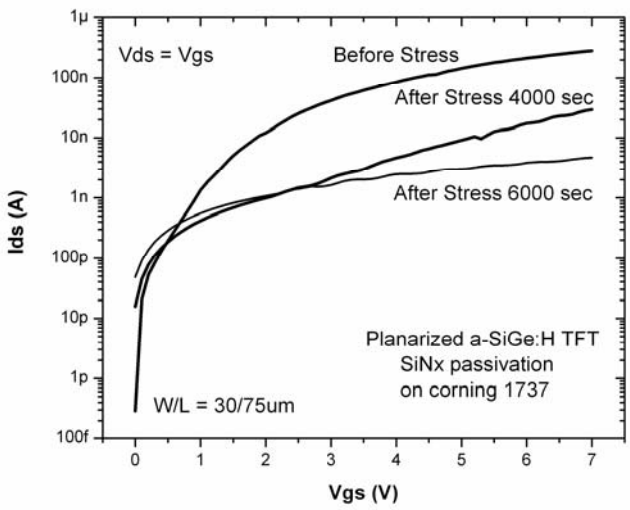


Fig 4.30 Transfer characteristics of the planarized a-SiGe:H TFT using SiNx as passivation before and after of the applied gate bias stress.

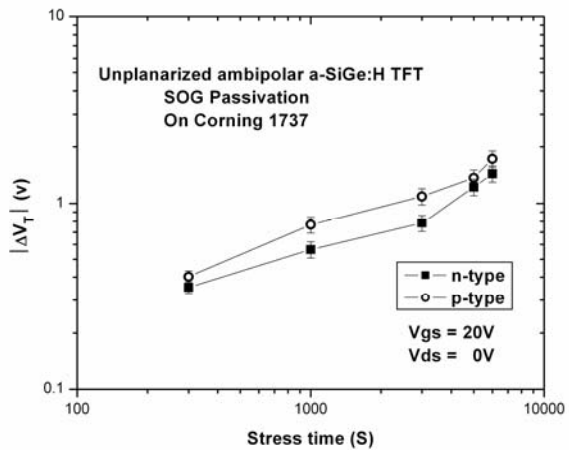


Fig 4.31 Threshold voltage shift (ΔV_T) with the stress time for unplanarized ambipolar a-SiGe:H TFT on corning 1737, at gate bias stress of 20V and Vds = 0V.

Figure 4.32 shows the transfer characteristics of the unplanarized ambipolar a-SiGe:H TFT before and after of the applied gate bias stress. It can be seen that the on-current is also less after stress time of 6000 seconds than before the gate bias stress. Note that the on-current after stress time of 6000 seconds is almost the same order than the on-current of planarized a-SiGe:H TFT using SiNx as passivation after the same stress time.

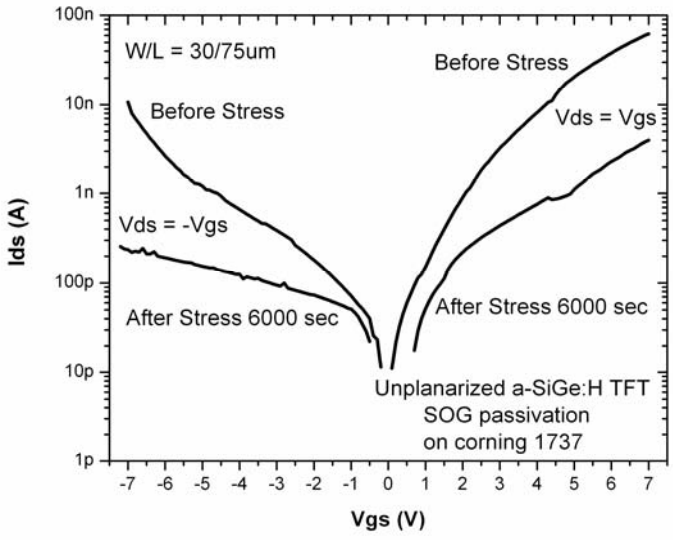


Fig 4.32 Transfer characteristics of the unplanarized ambipolar a-SiGe:H TFT before and after of the applied gate bias stress.

Figure 4.33 shows the threshold voltage shift as function of the stress time obtained for the planarized ambipolar a-SiGe:H TFT on Corning 1737. The figure shows the threshold voltage shift for n-type and p-type regions. As expected, the threshold voltage shift for n-type and p-type regions are lightly lower than unplanarized ambipolar TFTs. This is due to the better quality of the insulator-semiconductor interface. However, Figure 4.34 shows the transfer characteristics of the planarized ambipolar a-SiGe:H TFT before and after of the applied gate bias stress. It can be seen that the on-current has the same behavior than in the previous TFTs and is also almost the same order than the on-current of previous TFTs after the same stress time.

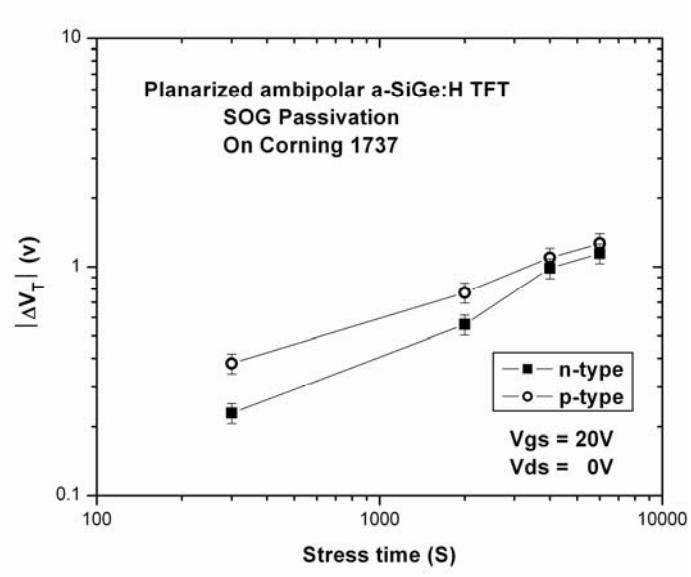


Fig 4.33 Threshold voltage shift (ΔV_T) with the stress time for planarized ambipolar a-SiGe:H TFT on corning 1737, at gate bias stress of 20V and Vds = 0V.

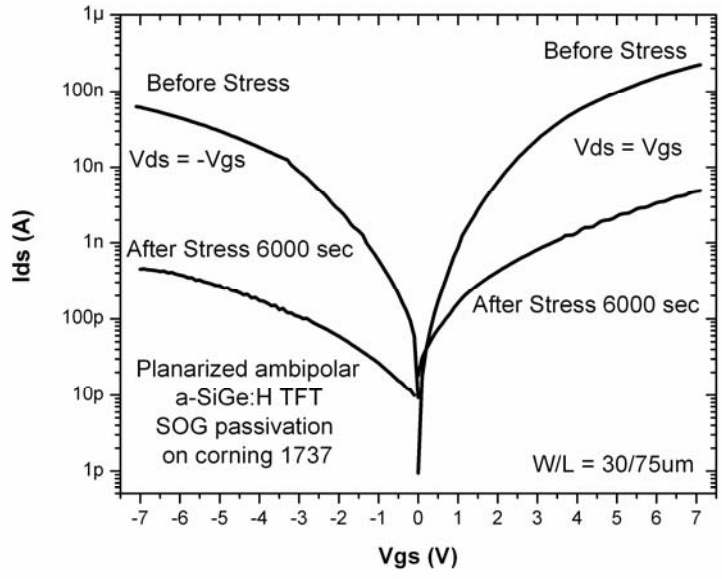
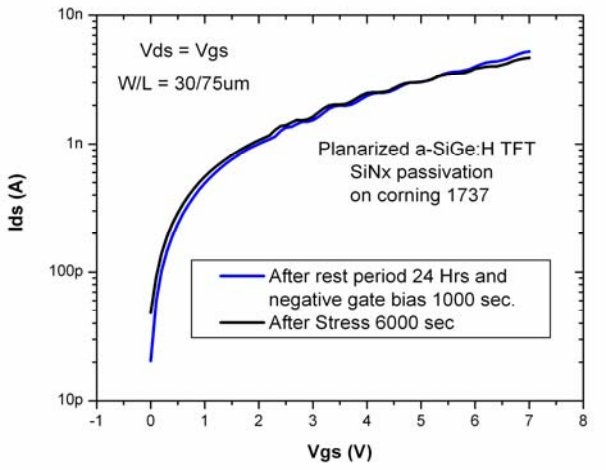


Fig 4.34 Transfer characteristics of the planarized ambipolar a-SiGe:H TFT before and after of the applied gate bias stress.

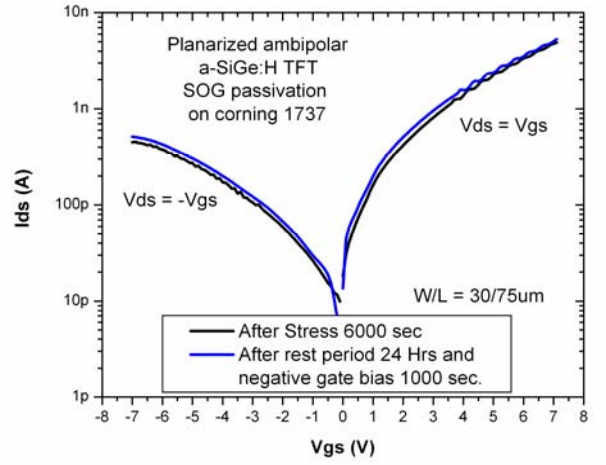
The observed threshold voltage shift for all a-SiGe:H TFTs could not be recovered after a rest period of several hours and under the application of negative gate bias, suggesting that the shift is irreversible. Of the threshold voltage shift mechanisms, charge trapping in the gate insulator is reversible [51, 54]. Therefore, under the applied gate bias conditions, this shift in the threshold voltage seems to be due to creation of states in the a-SiGe:H bandgap (deep states) [46, 68]. Figure 4.35 shows the transfer characteristics of the planarized a-SiGe:H TFTs after a rest period of 24 Hrs. and an application of negative gate bias (-20 V).

As mentioned in section 2.3, the quality of the insulator-semiconductor and metal-semiconductor interfaces strongly influences the threshold voltage shift of TFTs. Since both planarized a-SiGe:H TFTs, using SiNx and SOG as passivation, have identical insulator-semiconductor interface and apparently good quality in metal-semiconductor interface, the lower threshold voltage shift in a-SiGe:H TFTs using SOG as passivation can be due to the better quality in the top a-SiGe:H/SOG interface. Therefore, the slightly larger

threshold voltage shift in a-SiGe:H TFTs using SiNx as passivation is probably because the inherent fixed positive charge in the SiNx film may induce changes in the active layer.



a)



b)

Fig 4.35 Transfer characteristics of the planarized a-SiGe:H TFTs after a rest period. a) Using SiNx and b) SOG as passivation.

On the other hand, the lower threshold voltage shift in planarized a-SiGe:H TFTs when are compared with unplanarized a-SiGe:H TFTs is due to the better quality in the insulator-semiconductor interface as indicate its lower value of subthreshold slope.

The threshold voltage shift in the a-SiGe:H TFTs in general is lower than that in a-Si:H TFTs [68, 76, 77]. However, the lower on-current after the applied gate bias stress and the irreversible threshold voltage shift indicate that the a-SiGe:H film at 200 °C needs further research, since the deposition conditions of the film affect the rate of the creation of the extra defect states by changing the number of weak bonds inside the film.

Table 4.4 summarizes the parameters of the a-SiGe:H TFTs fabricated on corning 1737 at maximum temperature of 200°C.

Table 4.4 Parameters of the low-temperature a-SiGe:H TFTs on corning 1737.

Parameter	**TFT using SiNx passivation/ hydrogen plasma**	**TFT using SiNx passivation/ without hydrogen plasma**	**TFT using SiNx passivation/ higher overetching**	**Planarized TFT using SOG passivation**	**Unplanarized TFT using SOG passivation**
	Unipolar n-type	**Unipolar n-type**	**Unipolar n-type**	**Ambipolar n-type, p-type**	**Ambipolar n-type, p-type**
V_T	0.7 V	1.86V	1.58 V	1.11 V, -2.18 V	2.4 V, -3.35 V
SS	0.56 V/DEC	0.61 V/DEC	0.98 V/DEC	0.45, 0.49 V/DEC	1, 1.3 V/DEC
On/off-current ratio	10^6	~10^4	~10^3	10^5, ~10^5	~10^4, 10^3
ΔV_T (6000 sec)	2.25 V	No measured	No measured	1.14 V, -1.26 V	1.44 V, -1.72 V
Field-effect mobility	0.85 cm^2/Vs	0.52 cm^2/Vs	0.56 cm^2/Vs	0.68, 0.15 cm^2/Vs	0.11, 0.02 cm^2/Vs
Off-current	~0.3 pA	~18 pA	~200 pA	~0.95 pA	~11 pA

4.4 Conclusions.

In order to improve the insulator-semiconductor and metal-semiconductor interfaces, interface preparation procedures were proposed and demonstrated. The procedure to improve the insulator-semiconductor interface consists in the planarization of the gate. The planarization process is not complex and no need high-cost vacuum facilities. Also, the process is compatible with plastic or flexible substrates in flexible and large-area electronics. The procedure to improve the metal-semiconductor interface consists in an overetching in the source/drain region followed of a hydrogen plasma application prior to deposit the n+ contact layer. The interface preparation procedure leads to achieve a good quality metal-semiconductor interface, which translates in low contact resistance. This interface improvement translates in higher mobility and better values of off-current, on/off-current ratio, subthreshold slope and V_T.

The ambipolar behavior was not seen in the planarized a-SiGe:H TFTs using SiNx as passivation. However, unplanarized and planarized a-SiGe:H TFTs using SOG as passivation presented ambipolar behavior. In these devices, above the active layer, the contact region film was deposited first instead of the passivation film. This leads to form ohmic contacts instead of blocking contacts. Blocking contacts in a-SiGe:H TFTs using SiNx as passivation were observed at negative gate bias.

The subthreshold slope of planarized unipolar and ambipolar a-SiGe:H TFTs is an improvement for TFTs fabricated at low temperatures. The values of electron mobility of planarized unipolar and ambipolar a-SiGe:H TFTs are in the range of low temperature a-Si:H TFTs mobilities. Considering that hole mobility in a-Si:H is almost two orders of magnitude smaller than the electron mobility, which makes unfeasible the application of p-type a-Si:H TFTs, the hole mobility of 0.15 cm^2/Vs (p-type region) reported in this thesis shows a considerable improvement.

The characteristic energies of deep localized states for a-SiGe:H films using in ambipolar TFTs on corning 1737 are lower than those presented on silicon wafers. This is due to the roughness of the corning 1737 substrate which impoverishes the quality of the insulator-semiconductor interface. Considering that the DOS reflects contributions from interfaces, these contributions result in higher DOS for a-SiGe:H films on corning 1737.

The stability of the planarized a-SiGe:H TFTs under gate bias stress was analyzed. The observed threshold voltage shift for all a-SiGe:H TFTs did not recover following a rest period of several hours and under the application of negative gate bias, suggesting that the shift is irreversible. Of the threshold voltage shift mechanisms, charge trapping in the gate insulator is reversible. Therefore, under the applied gate bias conditions, this shift in the threshold voltage seems to be due to creation of states in the a-SiGe:H bandgap (deep states). Despite that threshold voltage shift in the a-SiGe:H TFTs is lower than that in a-Si:H TFTs, it was observed a reduction of the on-current after the applied gate bias stress.

Since both planarized a-SiGe:H TFTs, using SiNx and SOG as passivation, have identical insulator-semiconductor interface and apparently good quality in metal-semiconductor interface, the lower threshold voltage shift in a-SiGe:H TFTs using SOG as passivation can be due to the better quality in the top a-SiGe:H/SOG interface.

At the current time in which this work is defended, we demonstrate for the first time low- temperature ambipolar a-SiGe:H TFTs using the inverted staggered structure. A direct comparison of threshold voltage, subthreshold slope or mobilities between our devices and reported ambipolar devices is not possible because of the inherently different nature of the insulator-semiconductor interface in the top-gate structure used in reported ambipolar TFTs versus bottom-gate structure used in this thesis.

CHAPTER 5

SIMULATIONS OF LOW-TEMPERATURE a-SiGe:H TFTs.

As the technology matures, more accurate models must be developed. Modified crystalline metal-oxide semiconductor field effect transistor (MOSFET) models have been widely used to describe the characteristics of TFTs. Despite on this, these models are not capable of reproducing effects presented in TFTs due to the DOS in the bandgap. Recently, physical and analytical models for a-Si:H TFTs have been developed and implemented in several circuit simulators [78-81]. These models are based on theoretical studies of the TFTs physics and are in good agreement with the experimental characteristics obtained.

In our knowledge, since in literature there is no existence either physical nor spice models of a-SiGe:H TFTs, we use typical models used in a-Si:H TFTs because they are the most similar in behavior of our TFTs. In this chapter, simulations of the low-temperature a-SiGe:H TFTs are presented. These were performed in order to achieve a better understanding of the ambipolar behavior and of the planarized structure. First, the simulations using the physical simulators ATHENA and ATLAS from SILVACO are presented. Afterwards, the fit of the experimental data of the unipolar and ambipolar a-SiGe:H TFTs using a spice model are analyzed.

5.1 Simulations of a-SiGe:H TFTs using a physical model.

ATLAS and ATHENA are physically-based simulators. ATLAS is a physically-based device simulator which predicts the electrical characteristics

that are associated with specified physical structures and bias conditions. ATHENA is a physically-based process simulator which predicts the structures that result from specified process sequences.

Physically-based simulation is different from empirical modeling. The goal of empirical modeling is to obtain analytic formulae that approximate measured data with good accuracy and minimum complexity. Empirical models provide efficient approximation. However, they do not provide a physical insight, predictive capabilities, or theoretical knowledge [81].

Physically-based simulation has become very important for two reasons. One, it is almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure. The drawbacks of physically-based simulation are that all the relevant physics must be incorporated into a simulator, and numerical procedures must be implemented to solve the associated equations.

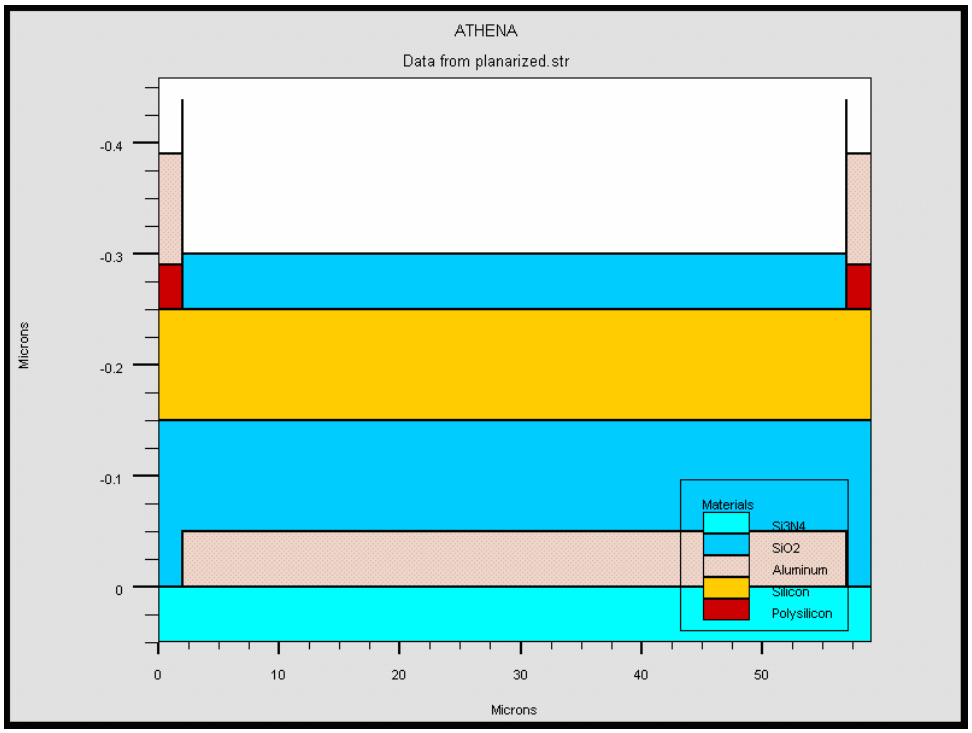
Recently, SILVACO has incorporated a specific module to simulation of amorphous semiconductors called TFT [81]. This module TFT enables one to define an energy distribution of defect states in the bandgap of semiconductor materials. This is necessary for the accurate treatment of the electrical properties of such materials as polysilicon and amorphous silicon.

In order to understand the main transport mechanism and the effects of the planarized gate in the a-SiGe:H TFTs, simulations using ATHENA and ATLAS were performed. The simulations were done as follows: using ATHENA, both unplanarized and planarized structures were generated. After that, using ATLAS, a positive gate bias of 5V (while Vds= 0V) was applied in order to study the effects of the planarization in the electric field around the corners of the gate. Finally, using the planarized structure generated by ATHENA, the transfer and output characteristics were simulated using ATLAS.

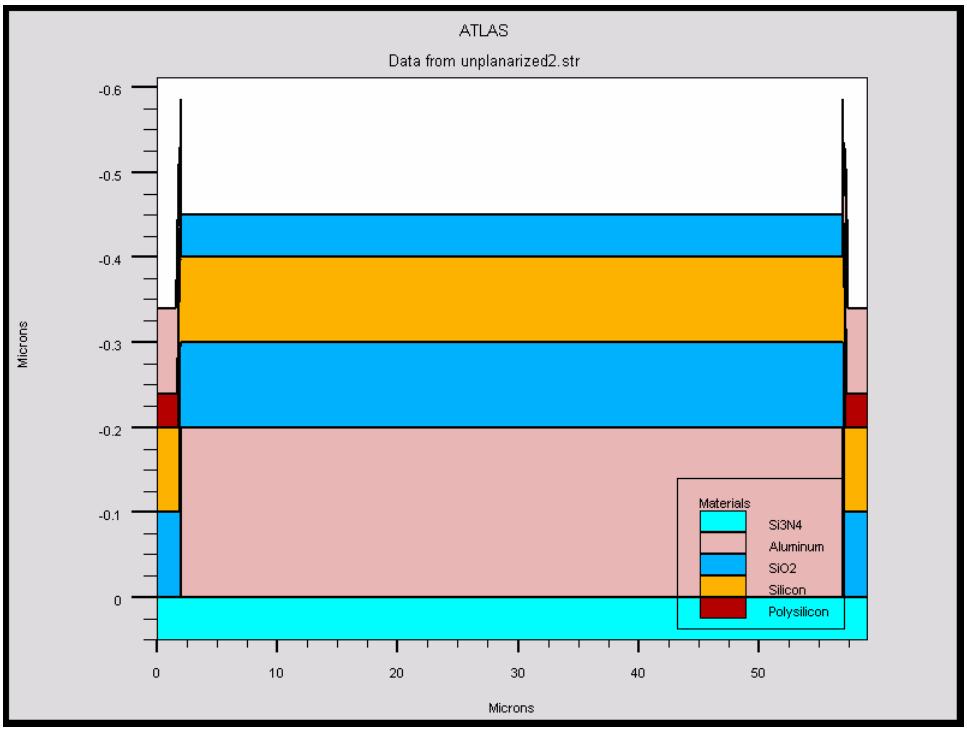
The main problem associated with the unplanarized gate is that in the inverted staggered TFT structure around the corners of the gate the gate

insulator tends to be thinner. This causes that the insulator may suffer strong leakage due to the high electric field at the corner. Figure 5.1 shows the cross section of planarized and unplanarized structures generated by ATHENA. In figure 5.1c can be seen the thinner gate insulator around the corners of the gate in the unplanarized structure.

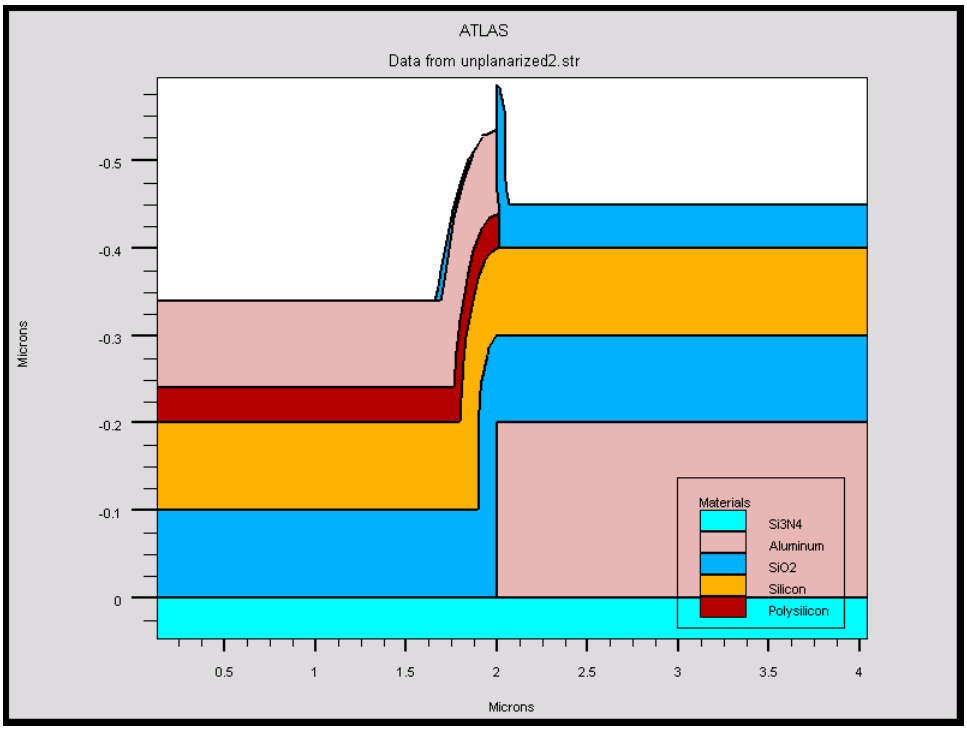
Figure 5.2 shows the electric field of the unplanarized and planarized structures obtained by ATLAS, a positive gate bias of 5V (while Vds= 0V) was applied. For the planarized structure, the electric field distribution is uniform through the insulator-semiconductor interface. On the other hand, for the unplanarized structure, the electric field distribution is not uniform through the insulator-semiconductor interface. It can be seen that around the corners of the gate, just beneath of the metal-semiconductor interface, there is an increase of the electric field. As expected, the electric field in the insulator-semiconductor interface for both planarized and unplanarized structures has almost the same value.



a)

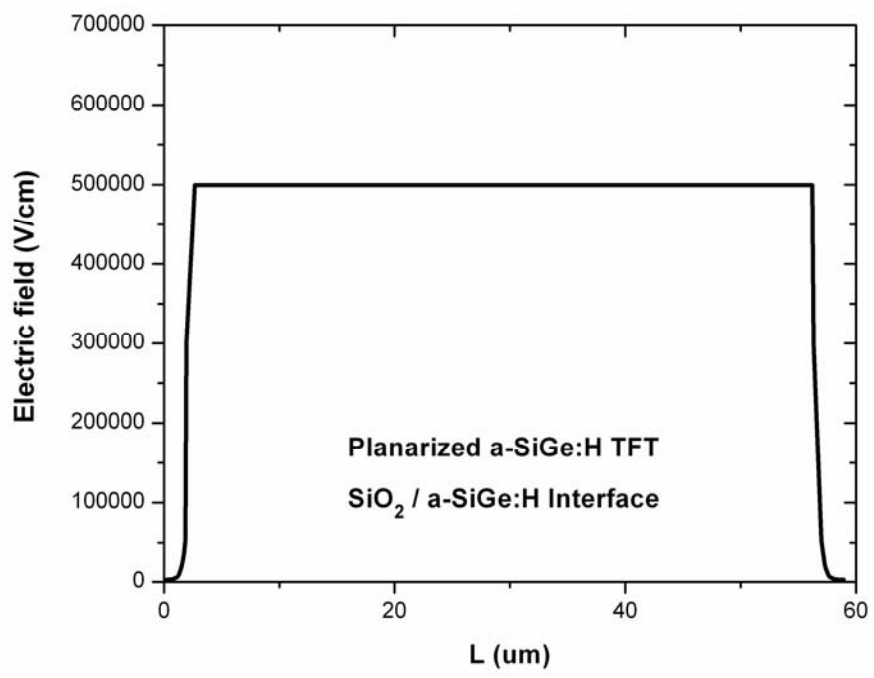


b)

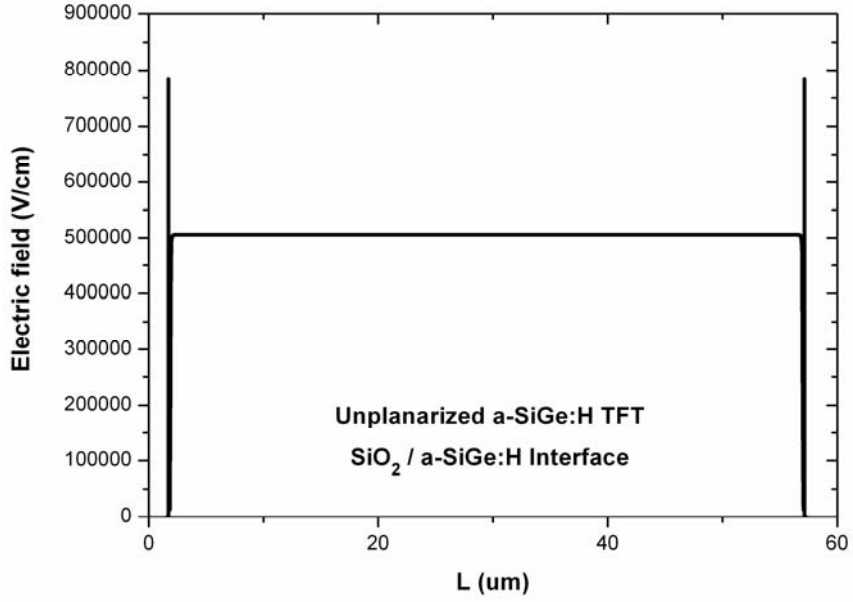


c)

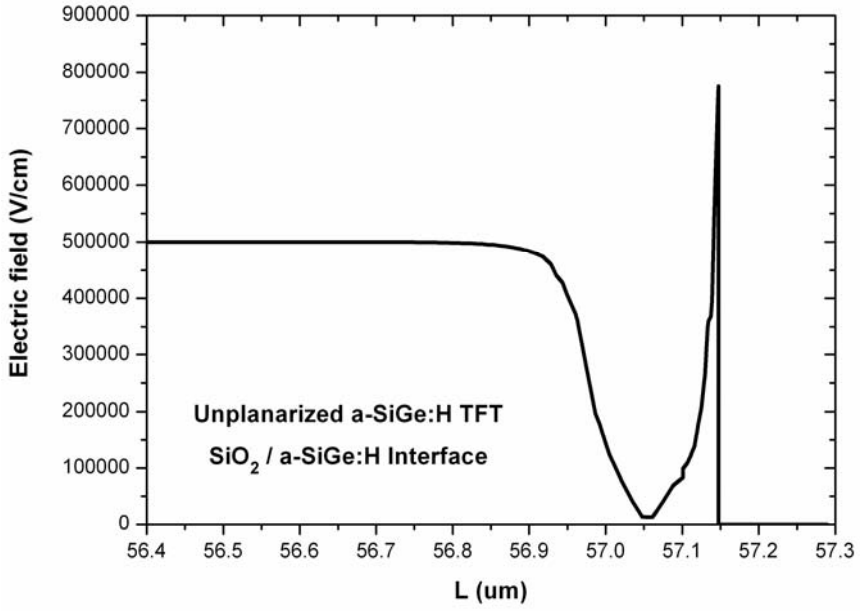
Fig 5.1 Cross section of planarized and unplanarized structures generated by ATHENA. a) planarized, b) unplanarized and c) thinner gate insulator in the unplanarized structure.


Electric field (V/cm)
700000
600000
500000
400000
300000
200000
100000
0
0
20
40
60
L (um)
Planarized a-SiGe:H TFT
SiO2 / a-SiGe:H Interface

a)


Electric field (V/cm)
900000
800000
700000
600000
500000
400000
300000
200000
100000
0
0
20
40
60
L (um)
Unplanarized a-SiGe:H TFT
SiO2 / a-SiGe:H Interface

b)

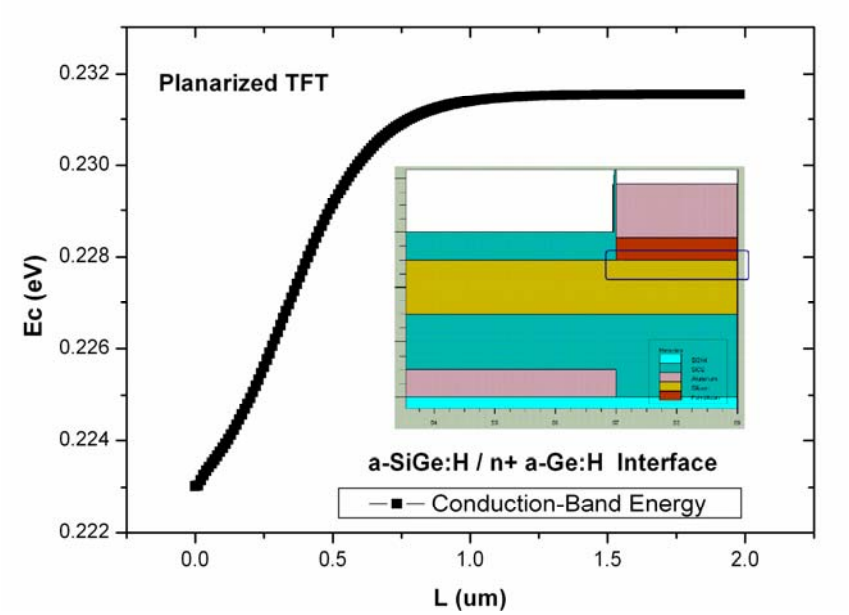


c)

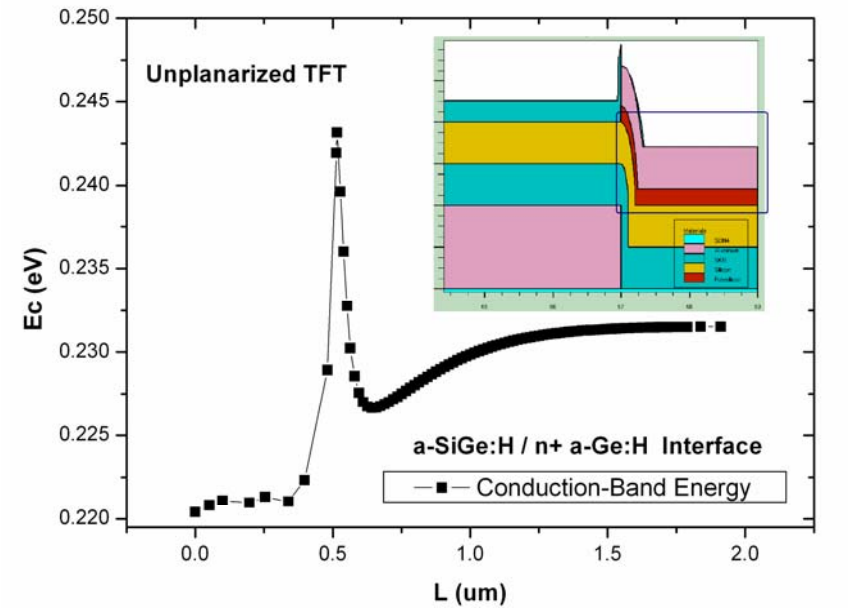
Fig 5.2 Electric field of a) planarized and b) unplanarized structures in the insulator-semiconductor interface, c) zoom of the electric field of unplanarized structure.

The field-effect mobility, which depends basically on the properties of the channel formed in the lower part of the active layer near of the gate insulator (insulator-semiconductor interface), will be improved since the planarization process causes a better distribution of the electric field around the corners of the gate and, hence, in the a-SiGe:H active layer. It is complex to understand why the planarization process, which affects the corners of the gate, will improve the metal-semiconductor interface (contact resistance). Since the a-SiGe:H active layer suffer strong electric field at the corners, hence, it is reasonable to think that the contact regions (above the gate corners) may also be influenced by the strong electric field as indicate the figure 5.2c. This high electric field causes an increase in the conduction band energy in the a-SiGe:H film near of the a-SiGe:H/ n+ a-Ge:H interface as show in figure 5.3. This increase in the conduction band energy acts as a barrier for the electrons. Therefore, as result, their contact resistance apparently increases. This can explain why the planarized ambipolar a-

SiGe:H TFTs fabricated on corning glass substrate have higher mobility than the unplanarized ambipolar TFTs fabricated on silicon wafers.



a)



b)

Fig 5.3 Conduction Band energy for a) planarized and b) unplanarized TFTs in the a-SiGe:H /n+ a-Ge:H interface.

As was shown in the last chapter, the planarized TFTs has better performance such as field-effect mobility, off-current, subthreshold slope, threshold voltage and on/off-current ratio which are due to the less gate leakage current, different electric field distribution around the corners of the gate and smaller contact resistance.

On the other hand, using the planarized structure generated by ATHENA, the transfer and output characteristics were simulated using ATLAS. The a-SiGe:H material parameters used for the simulations were taken from [82] and from the characterization of the device. Since the ambipolar behavior is lead with similar electron and hole mobilities, the mobilities used in the simulations were of 30 and 20 cm^2/Vs for electrons and holes, respectively.

The transfer characteristics of the simulated TFT are show in figure 5.4. It can be seen the ambipolar behavior presented in the experimental data of the ambipolar a-SiGe:H TFTs. Although, the values of subthreshold slope, threshold voltage and on/off-current ratio are different for the simulated device, the reproduction of the ambipolar behavior is the principal contribution of these simulations.

On the other hand, figure 5.5 shows the output characteristics for the simulated ambipolar a-SiGe:H TFT. While the output characteristics for p-type region of the TFT have the same behavior as in the experimental data, those of the n-type region not show the same apparently exponential behavior observed in the experimental data. Since in the literature some authors consider the ambipolarity as a phenomenon with different behavior of holes and electrons current contributions [19], such a phenomenon may not be described by the model used by ATLAS for the simulations.

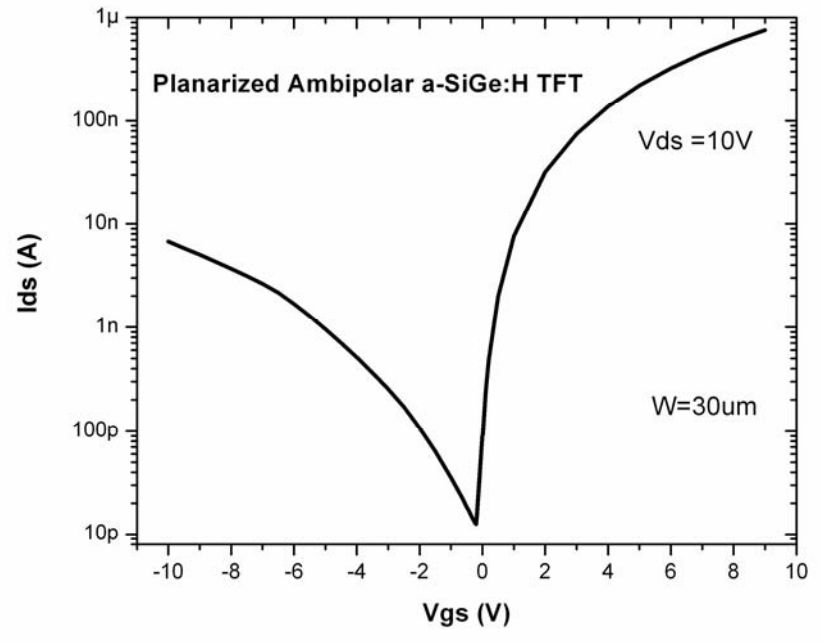
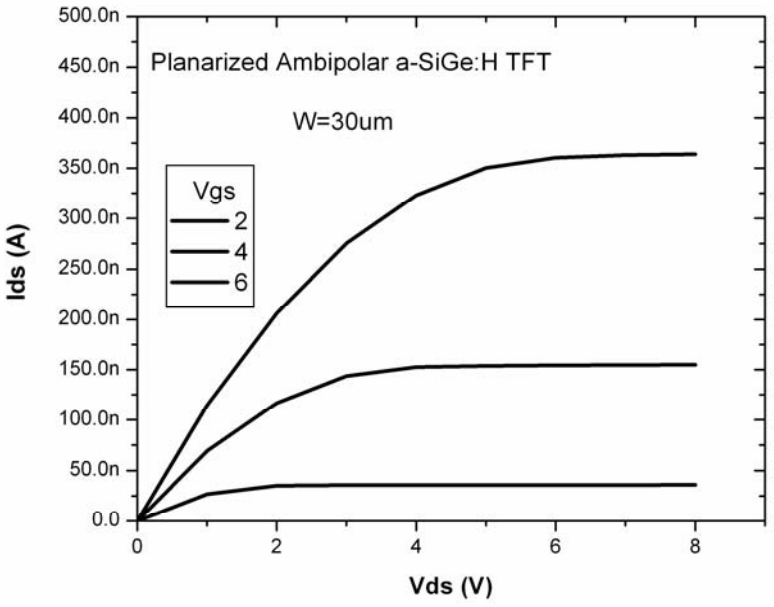
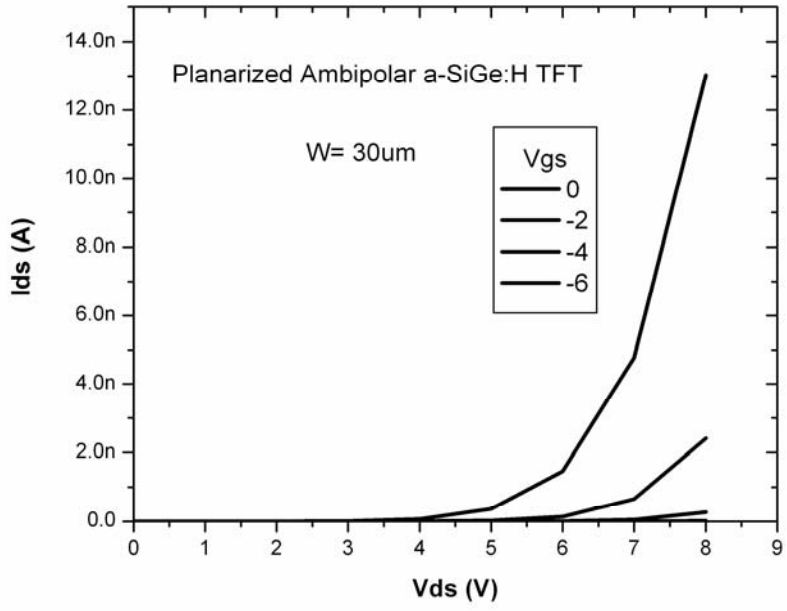


Fig 5.4 Transfer characteristics of simulated planarized ambipolar a-SiGe:H TFTs.



a)



b)

Fig 5.5 Output characteristics of simulated planarized ambipolar a-SiGe:H TFTs. a) n-type and b) p-type regions.

5.2 Simulations of a-SiGe:H TFTs using a SPICE model.

Since the measured characteristics of the a-SiGe:H TFTs are more closely to the characteristics of a-Si:H TFTs, the a-Si:H TFT model used was the presented by M. Shur *et al.* in [78]. This model has been implemented in AIM-SPICE [80]. The details of the a-Si:H TFT model are presented in [79].

The total drain current is represented by the equation 5.1.

$$Ids = I_{leak} + (1/I_{sub} + 1/I_{abv})^{-1} \quad (5.1)$$

Where I_{leak} is the leakage current, I_{sub} is the subthreshold current and I_{abv} is the above threshold current.

Since the unipolar (n-type) TFTs are not generally operated at large negative gate bias, the off-current is modeled by the leakage current using the empirical expression

$$I_{leak} = I_{0L} (\exp (Vds/V_{DSL}) - 1) \exp (- Vgs/V_{GL}) + \sigma_0 Vds \quad (5.2)$$

Where I_{0L} is the minimum leakage current, V_{DSL} and V_{GL} describe the dependence on Vds and Vgs, respectively, and σ_0 is determined by the resolution of the measurement equipment.

In the subthreshold regime, the Fermi level is dependent on the density of deep states in the bandgap. An exponential dependence of the deep states, $g(E) = g_0 \exp [(E- E_{F0})/E_{DD}]$, has been demonstrated in this region [78, 79]. Where E_{DD} is the characteristic energy of the deep states and E_{F0} is the energy corresponding to the zero-bias Fermi level position where the zero-bias density of deep states is given by g_0. From this dependence, the position of the Fermi level can be related to the DOS to obtain the sheet electron carriers induced by the gate bias, n_{sb}, as a function of the material parameters and the density of deep states. Using this dependence, the subthreshold current can be described as a drift current as in Equation 5.3.

$$I_{sub} = q\mu_n W/L \, V_{DSe} \, n_{Sb}$$
$$= q\mu_n W/L \, V_{DSe} \, n_{S0} [(t_m/d_i) (V_{GFBe}/V_0) (\varepsilon_i/\varepsilon_s)] \, ^2V_0/V_e \quad (5.3)$$

Where d_i is the insulator thickness, ε_i and ε_s are the insulator and amorphous semiconductor permittivities, respectively, n_{S0} is the dark sheet carrier density and t_m is the charge channel thickness. The complete set of equations and parameters of the subthreshold current are presented in Appendix A.

In the above threshold regime, the field-effect mobility is a weak function of gate bias and can be adequately described by a power law with a constant exponent as show equation 5.4.

$$\mu_{FET} = \mu_n (Vgs - V_T / V_{AA})^{\gamma} \quad (5.4)$$

Where μ_n, V_{AA} and γ are mobility parameters which model the mobility dependence on gate bias.

The above threshold current can be described by the equation 5.5. The complete set of equations and parameters of the above threshold current are presented in Appendix A.

$$I_{abv} = \mu_{FET} C_i W/L V_{DSe} (1 + \lambda Vds) V_{GTe} \quad (5.5)$$

Where C_i is the gate insulator capacitance per unit area, μ_{FET} is the field-effect mobility given in equation 5.4 and the multiplicative factor (1 + λVds) includes the effect of channel length modulation.

In the following subsections the simulations of unipolar and ambipolar a-SiGe:H TFTs using the spice model are presented. For the unipolar a-SiGe:H TFTs, the a-Si:H TFT model was used with the respective material and device parameters changes. For the ambipolar a-SiGe:H TFTs, the a-Si:H TFT model was adapted to describe the n- and p-type behavior for positive and negative gate bias, respectively.

From the electrical characterization of the low-temperature a-SiGe:H TFTs some material and device parameters were obtained, such as the maximum trap density (N_T) and the characteristic energies of the deep states of the a-SiGe:H active layer, besides the threshold voltage V_T and flat-band voltage of the devices. Moreover, from the characterization of the low-temperature materials (Chapter 3), important material parameters such as the Fermi level (obtained from the activation energy) of the a-SiGe:H film and the dielectric constant of the SiO_2 obtained from SOG/DI were also obtained. The use of all these parameters in the spice model is necessary in order to obtain good agreement between the simulated and the experimental data of the a-SiGe:H TFTs.

5.2.1 Simulations of unipolar a-SiGe:H TFTs using a SPICE model.

Previously, it was mentioned the importance of the density of deep states on the subthreshold region of the device performance. In a-Si:H films, the typical value of minimum density of deep states g_0 is $1x10^{23}$ $m^{-3}eV^{-1}$ [78, 79]. Since the electrical characterization of the a-SiGe:H TFTs showed a relatively higher DOS due to the incorporation of germanium, the value of g_0 used to simulate the unipolar a-SiGe:H TFTs was higher than that in a-Si:H TFTs but lower than the maximum trap density (N_T) in the a-SiGe:H film ($2.648x10^{17}$ $cm^{-3}eV^{-1}$ or $2.648x10^{23}$ $m^{-3}eV^{-1}$). The value of g_0 was of $1.9x10^{23}$ $m^{-3}eV^{-1}$ and was corroborated by the agreement of the simulated with the experimental data.

The value of the μ_n used in the subthreshold current and field-effect mobility equations (eq. 5.3 and 5.4) was of 30 cm^2/Vs, same as in the device simulations by ATHENA and ATLAS, while the threshold voltage V_T was the extracted in the electrical characterization of the TFT (0.7 V). The other parameters were V_{AA} = 16 $x10^3$ V and γ = 0.6, both of them in the range of those in a-Si:H TFTs [78, 79].

Figure 5.6 shows the transfer characteristic measured and simulated for the n-type a-SiGe:H TFTs with W/L = 30/75 um. It is demonstrated the agreement between the simulated and the experimental data of the unipolar devices.

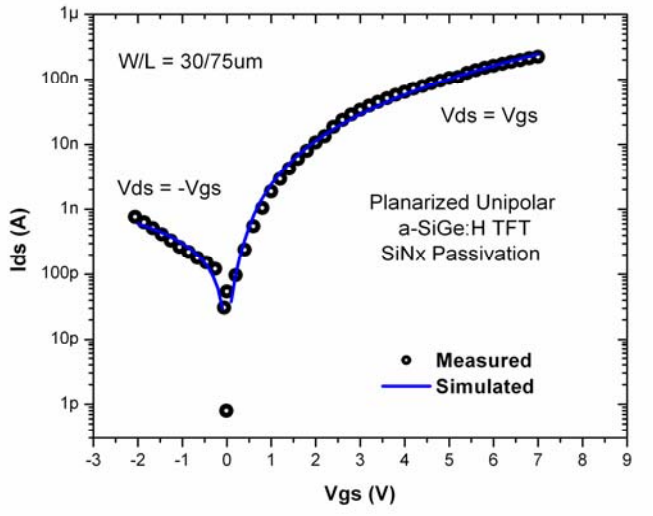


Fig 5.6 Measured and simulated transfer characteristics of the planarized unipolar a-SiGe:H TFT.

The simulated transfer characteristic agrees very well with the measured data. The same parameter set, also results in accurate description of the output characteristics as shown in Figure 5.7. The model successfully reproduces both measured transfer and output characteristics over a wide range of Vgs and Vds voltages. The complete parameter set is presented in appendix A.

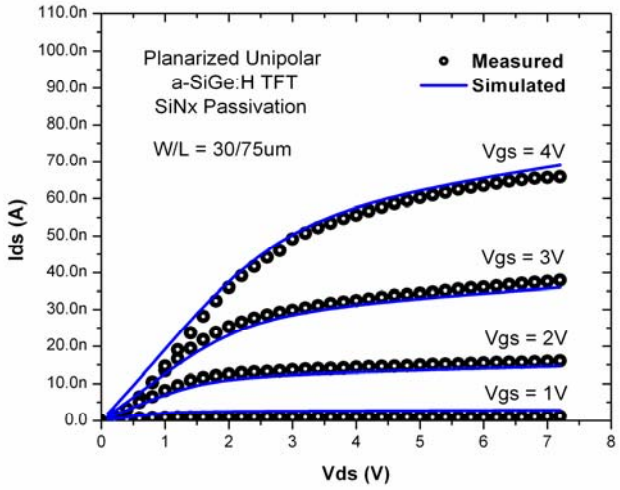


Fig 5.7 Measured and simulated output characteristics of the planarized unipolar a-SiGe:H TFT.

5.2.2 Simulations of ambipolar a-SiGe:H TFTs using a SPICE model.

Since the ambipolar TFTs present both n- and p-type behavior, the model used for the unipolar a-SiGe:H TFTs needs to be adapted. The model describes the off-current as leakage current for negative gate bias, however, ambipolar TFTs present a p-type behavior for negative gate bias. Therefore, the model was adapted in order to describe the p-type TFT behavior. The total drain current is represented by the equation 5.6

$$Ids = I_{leak} + I_n + I_p$$
$$= I_{leak} + (1/I_{subn} + 1/I_{abvn})^{-1} + (1/I_{subp} + 1/I_{abvp})^{-1} \quad (5.6)$$

Where I_{subp} is the p-type subthreshold current and I_{abvp} is the p-type above threshold current, both currents replaced the off-current (leakage current) for negative gate bias in a-Si:H model. The p-type currents keep the same equations set with the respective sign change of Vgs. Considering that the p-type and n-type regions of the ambipolar TFTs have different device parameters, such as threshold voltage and flat-band voltage, some of the fit parameters are different between p-type and n-type current models. However, the material parameters such as g_0, the characteristic energy of deep states and the ones previously mentioned in section 5.2, are fixed for both p-type and n-type current models.

An exponential dependence of the deep states, $g(E) = g_0 \exp [(E-E_{F0})/E_{DD}]$, has been demonstrated in the subthreshold region where the deep states have a strong influence. E_{DD} is the characteristic energy of the deep states and its typical value is ~120 meV [78, 79]. The electrical characterization of the ambipolar a-SiGe:H TFTs showed characteristic energies of 26 meV and 47 meV for n-type (acceptor-deep states) and p-type (donor-deep states), respectively. The value of E_{DD} used to simulate the ambipolar a-SiGe:H TFTs was approximately an average of the acceptor and

donor characteristic energies (E_{DD} = 40 meV for both n-type and p-type current models). The values of E_{DD} and g_0 were kept equal for both current models because this generally reports better fit of the experimental data, since both models contribute to simulate a single TFT [21].

The value of the μ_n used in the n-type and p-type (μ_p) current models was of 28 and 10 cm^2/Vs, respectively. While the other parameters were V_{AA}= 16 $x10^3$ V and γ= 0.6 for both n-type and p-type current models. The complete set of equations and parameters of the ambipolar model are presented in Appendix A.

Figure 5.8 shows the transfer characteristic measured and simulated for the ambipolar a-SiGe:H TFTs with W/L = 30/75 um. The complete parameter set is presented in appendix A.

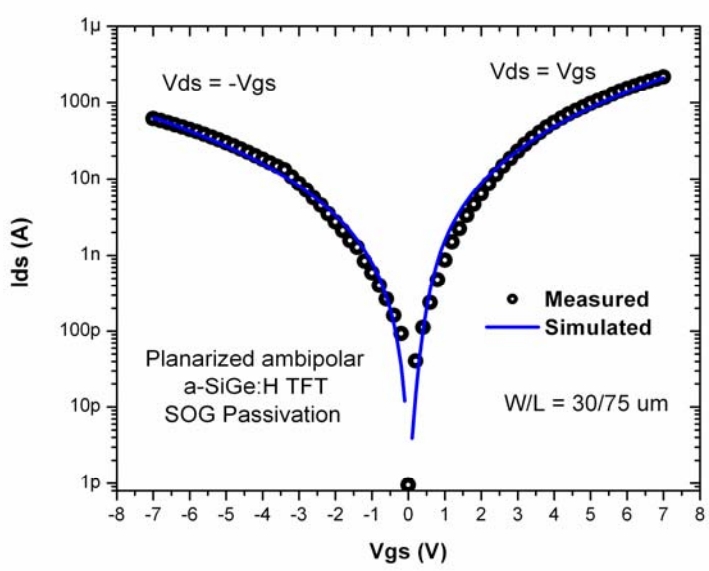


Fig 5.8 Measured and simulated transfer characteristics of the planarized ambipolar a-SiGe:H TFT.

As in the unipolar devices, the simulated transfer characteristic agrees very well with the measured data. The same parameter set, was used to simulate the output characteristics as shown in Figure 5.9. However, in the

output characteristics there is not good agreement between the simulated and measured data. Despite on this, it can be see an accurate description of the output characteristics at values of Vds<Vgs. While at values of Vds>Vgs there is an increase in the drain current due to the superposition of the currents flow of electrons and holes, in the literature this behavior is called the *ambipolar phenomena* [19].

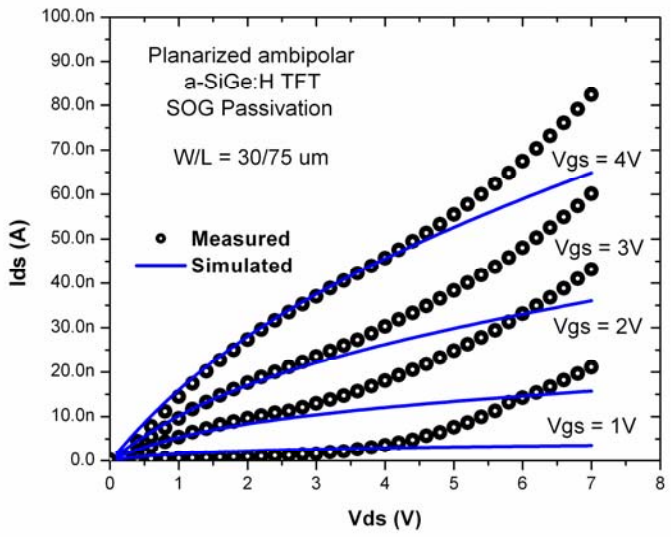
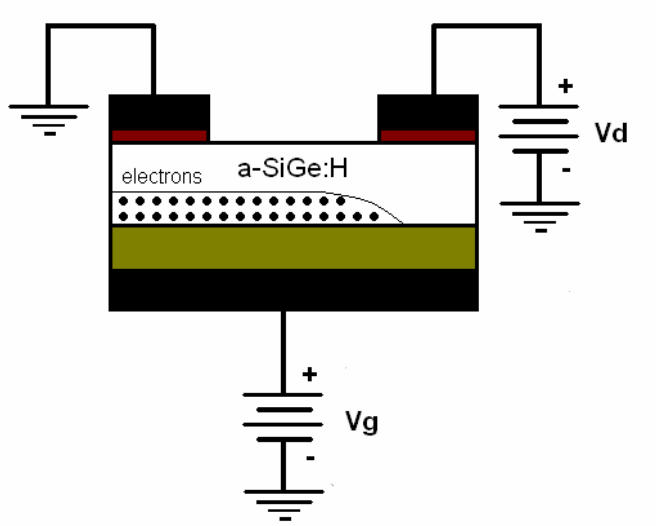


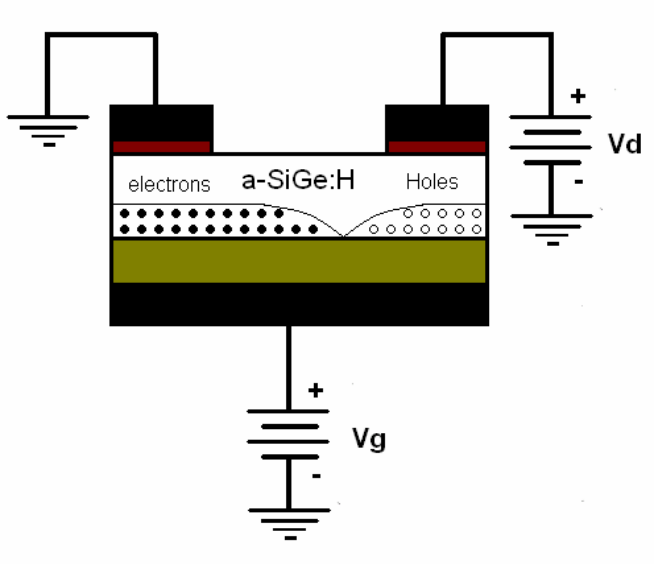
Fig 5.9 Measured and simulated output characteristics of the planarized ambipolar a-SiGe:H TFT.

Take for example figure 5.10, as the drain voltage Vds is increased above 0V, electron current through the device increases linearly. While this Vds is increasing, the electron channel close to the drain region is being depleted of electrons causing the electron channel to shrink, leading a pinch-off region as shown in Figure 5.10a. This pinch-off in the channel causes that the current rises only slightly as Vds increases (saturation region). While the device is operating in saturation region, an enhanced hole layer begins to form at the pinch-off region of the device where previously was occupied by the electron layer (see Fig. 5.10b). This hole layer forms as a result of the drain potential being larger than the gate potential, the drain-gate voltage

Vdg. A reversed biased situation then exists causing the formation of the enhanced hole layer. The effects of this hole layer are not observed in the device performance until the device enters to condition of Vds>Vgs. As the device enters to condition of Vds>Vgs, the current begins to increase at a faster rate than in saturation region. This increased rate is due to the superposition of the currents flow through the electron and hole layers, thereby demonstrating the ambipolar phenomena.



a)



b)

Fig 5.10 Channel formation of a-SiGe:H TFT. a) Pinch-off and b) ambipolar phenomena.

The existence of a p-n diode at the a-SiGe:H interface where the enhanced electron and hole layers meet is of the correct polarity for Ids to continue to increase, resulting in the exponential current rise. This behavior can be seen in figure 5.11, where the transitions of linear to saturation regions and then to ambipolar phenomena are appreciated.

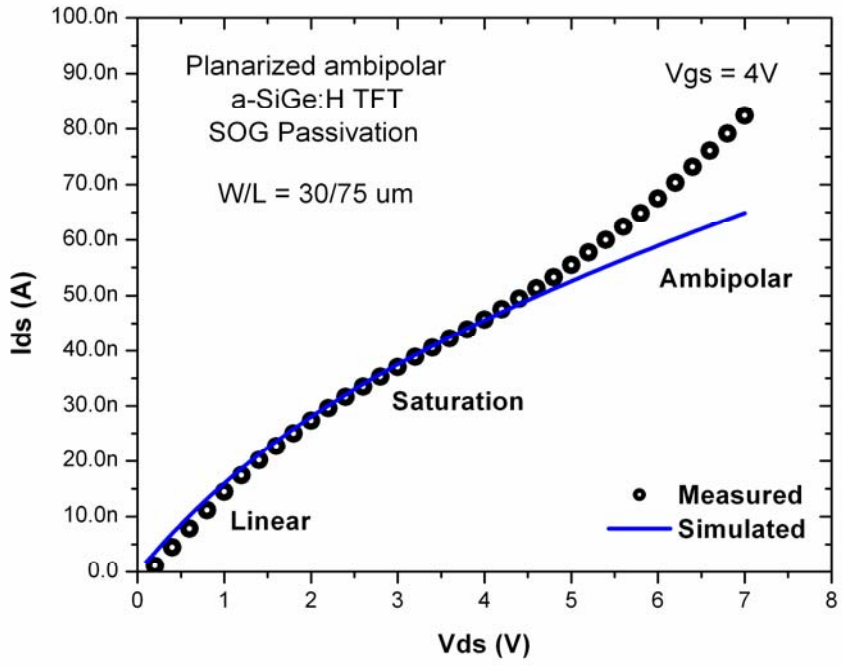


Fig 5.11 Measured and simulated output characteristic of the planarized ambipolar a-SiGe:H TFT where the ambipolar phenomena is presented at Vds>Vgs.

By reversing the polarity of the applied biases and alternating the n- and p-channel device formation, a description similar to that given above could be presented to explain the p-type device output characteristics.

The model agrees with the experimental data in transfer characteristics and in the linear and saturation regions of the output characteristics (at Vds<Vgs). However, the model needs to be adapted to reproduce the ambipolar phenomena.

5.3 Conclusions.

The simulations using the physical simulators ATHENA and ATLAS from SILVACO help us to understand the main transport mechanism and the effects of the planarized gate in the a-SiGe:H TFTs. It was observed for the planarized structure, the electric field distribution is uniform through the insulator-semiconductor interface. Meanwhile, for the unplanarized structure, the electric field distribution is not uniform through the insulator-semiconductor interface. It can be seen that around the corners of the gate, just beneath of the metal-semiconductor interface, there is an increase of the electric field. Since the a-SiGe:H active layer suffer strong electric field at the corners, hence, it is reasonable to think that the contact regions (above the gate corners) may also be influenced by the strong electric field. Therefore, as result, their contact resistance apparently increases. This can explain why the ambipolar a-SiGe:H TFTs fabricated on corning glass substrate have higher mobility than the ambipolar TFTs fabricated on silicon wafers. On the other hand, the transfer characteristics of the simulated TFT show the ambipolar behavior presented in the experimental data of the ambipolar a-SiGe:H TFTs. The mobilities used in the simulations (30 and 20 cm^2/Vs for electrons and holes, respectively) lead to reproduce the ambipolar behavior, this agrees with the measurements reported in literature where the ambipolar behavior is obtained with similar values of both electrons and holes mobilities. The output characteristics for p-type region of the TFT have the same behavior as in the experimental data, those of the n-type region not show the same apparently exponential behavior observed in the experimental data.

On the other hand, as expected, the simulations using the spice model agrees with the experimental data of the unipolar TFTs. However, in the output characteristics of the ambipolar TFTs there is not good agreement between the simulations and measured data. Despite on this, it can be see an accurate description of the output characteristics at values of Vds<Vgs. While

at values of Vds>Vgs there is an increase in the drain current due to the superposition of the currents flow of electrons and holes, in the literature this behavior is called the *ambipolar phenomena*. Such a phenomenon may not be described by the models used for the simulations.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK.

6.1 Conclusions.

To date, we demonstrate for the first time low- temperature ambipolar a-SiGe:H TFTs using the inverted staggered structure. A direct comparison of threshold voltage, subthreshold slope or mobilities between our devices and reported ambipolar devices is not possible because of the inherently different nature of the insulator-semiconductor interface in the top-gate structure used in reported ambipolar TFTs versus bottom-gate structure used in this thesis. Also, the low-temperature process (200 °C) and the good performance on corning glass substrates make the ambipolar a-SiGe:H TFTs a promising alternative to enable flexible and large area electronics in the near future.

From the characterization of the materials in the TFT structure, we demonstrated that dilution of SOG and long curing time are necessary to obtain good quality SiO_2 films cured at 200°C. The films produced from diluted SOG showed a refractive index and dielectric constant very close to those of the thermally grown SiO_2. The insulator breakdown field for the MIM structures with SiO_2 films produced from SOG diluted with DI was approximately 21 MV/cm. All these results suggest that SOG diluted with DI is an excellent candidate to be used as insulator on flexible and large-area electronics. Meanwhile, the characterization of the a-SiGe:H films makes us suppose that probably the a-SiGe:H films with flow rate of SiH_4 of 45 sccm, H_2 flow of 1000 sccm and GeH_4 flow of 105 sccm may have a lower DOS. Finally, the characterization of contact region films was done. The lowest value of contact resistance at 200 °C for n-type and p-type films is obtained

with PH_3 flow of 20 sccm and B_2H_6 flow of 50 sccm, respectively. It seems to be these films deposited at low temperatures have the properties suitable for contact region in TFT applications.

In order to improve the insulator-semiconductor and metal-semiconductor interfaces, interface preparation procedures were demonstrated. The procedure to improve the insulator-semiconductor interface consists in the planarization of the gate. The planarization process is not complex and no need high-cost vacuum facilities. Also, the process is compatible with plastic or flexible substrates in flexible and large-area electronics. The procedure to improve the metal-semiconductor interface consists in an overetching in the source/drain region followed of a hydrogen plasma application prior to deposit the n+ contact layer. Due to the sequence of the fabrication process, this procedure only applies in a-SiGe:H TFTs with SiNx as passivation. The interface preparation procedure leads to achieve a good quality metal-semiconductor interface, which translates in low contact resistance. This interface improvement translates in higher mobility and better values of on-current and on/off-current ratio.

The ambipolar behavior was not seen in the planarized a-SiGe:H TFTs using SiNx as passivation. However, unplanarized and planarized a-SiGe:H TFTs using SOG as passivation presented ambipolar behavior. In these devices, above the active layer, the contact region film was deposited first instead of the passivation film. This leads to form ohmic contacts instead of blocking contacts. Blocking contacts in a-SiGe:H TFTs using SiNx as passivation were observed at negative gate bias.

The values of electron mobility of planarized unipolar and ambipolar a-SiGe:H TFTs are in the range of low temperature a-Si:H TFTs mobilities. Considering that hole mobility in a-Si:H is almost two orders of magnitude smaller than the electron mobility, which makes unfeasible the application of p-type a-Si:H TFTs, the hole mobility of 0.15 cm^2/Vs (p-type region) reported in this thesis shows a considerable improvement.

The stability of the planarized a-SiGe:H TFTs under gate bias stress was analyzed. Despite that threshold voltage shift in the a-SiGe:H TFTs is lower than that in a-Si:H TFTs, it was observed a reduction of the on-current after the applied gate bias stress. The observed threshold voltage shift for all a-SiGe:H TFTs did not recover following a rest period of several hours and under the application of negative gate bias, suggesting that the shift is irreversible. Of the threshold voltage shift mechanisms, charge trapping in the gate insulator is reversible. Therefore, under the applied gate bias conditions, this shift in the threshold voltage seems to be due to creation of states in the a-SiGe:H bandgap (deep states).

Since both planarized a-SiGe:H TFTs, using SiNx and SOG as passivation, have identical insulator-semiconductor interface and apparently good quality in metal-semiconductor interface, the lower threshold voltage shift in a-SiGe:H TFTs using SOG as passivation can be due to the better quality in the top a-SiGe:H/SOG interface.

The simulations using the physical simulators ATHENA and ATLAS from SILVACO help us to understand the main transport mechanism and the effects of the planarized gate in the a-SiGe:H TFTs. On the other hand, as expected, the simulations using the spice model agrees with the experimental data of the unipolar TFTs. However, in the output characteristics of the ambipolar TFTs there is not good agreement between the simulations and measured data. Since the ambipolar phenomena may not be described by the models used for the simulations.

6.2 Future work.

The optimum thickness of the materials used in the TFT structure is necessary in order to obtain the best performance of the unipolar and ambipolar a-SiGe:H TFTs.

The low value of the bandgap showed in the a-SiGe:H film, the reduction of the on-current after the applied gate bias stress and the irreversible threshold voltage shift of the a-SiGe:H TFTs indicate that the a-SiGe:H film at 200 °C needs further research.

The modeling of the ambipolar a-SiGe:H needs to be developed, in order to model the ambipolar phenomena.

Since SiNx films as passivation were used in unipolar TFTs and SOG films were used in ambipolar TFTs. A study of the advantages in the use of SOG or SiNx as passivation film can be made using SOG as passivation in unipolar TFTs and SiNx films in ambipolar TFTs.

APPENDIX A

SET OF EQUATIONS OF DC SPICE MODEL FOR UNIPOLAR AND AMBIPOLAR a-SiGe:H TFTS.

A.1 Set of equations of unipolar a-SiGe:H TFTs.

Main current equation

$$Ids = I_{leak} + (1/I_{sub} + 1/I_{abv})^{-1}$$

Leakage regime

$$I_{leak} = I_{0L}\left[\exp\left(\frac{Vds}{V_{DSL}}\right) - 1\right]\exp\left(\frac{-Vgs}{V_{GL}}\right) + \sigma_0 Vds$$

Subthreshold regime

$$I_{sub} = q\mu_n \frac{W}{L} V_{DSe}\, n_{S0}\left[\left(\frac{t_m}{d_i}\right)\left(\frac{V_{GFBe}}{V_O}\right)\left(\frac{\varepsilon_i}{\varepsilon_s}\right)\right]^{\frac{2V_O}{V_e}}$$

$$V_{DSe} = \frac{Vds}{\left[1+\left(\frac{Vds}{V_{sate}}\right)^{msat}\right]^{\frac{1}{msat}}}$$

$$V_{sate} = \alpha_{sat}\, V_{GTe}$$

$$V_{GTe} = V_{th}\left[1 + \frac{V_{GT}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GT}}{2V_{th}} - 1\right)^2}\right]$$

$$V_{GT} = Vgs - V_T$$

$$n_{S0} = N_C t_m \left(\frac{V_e}{d_i}\right) \exp\left(\frac{-dE_{F0}}{V_{th}}\right)$$

$$V_{GFBe} = V_{th}\left[1 + \frac{V_{GFB}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GFB}}{2V_{th}} - 1\right)^2}\right]$$

$$V_{GFB} = Vgs - Vfb$$

$$t_m = \sqrt{\frac{\varepsilon_s \varepsilon_0}{2q \cdot g_O}}$$

$$V_e = \frac{2V_O V_{th0}}{2V_O - V_{th}}$$

$$V_0 = \frac{E_{DD}}{q}$$

Above threshold regime

$$I_{abv} = \mu_{FET}\, C_i\, W/L\, V_{DSe}\, (1 + \lambda Vds)\, V_{GTe}$$

$$\mu_{FET} = \mu_n \left(\frac{V_{GTe}}{V_{AA}}\right)^{\gamma}$$

A.1.1 Parameters of unipolar a-SiGe:H TFTs.

Table A.1 Unipolar a-SiGe:H TFTs parameters summary.

Parameter	Symbol	Description	Value
VFB (V)	Vfb	Flat-band voltage	-0.16
VTO (V)	V_T	Threshold voltage	-0.7
EDD (eV)	E_{DD}	Characteristic energy of deep states	0.04
g0 (m^{-3}/eV)	g_0	Zero-bias density of deep states	$1.9x10^{23}$
MUBAND (m^2/Vs)	μ_n	Band mobility	$30\ x10^{-4}$
GAMMA	γ	Power law mobility parameter	0.6
VAA (V)	V_{AA}	Characteristic voltage for μ_{FET}	16000
ALPHASAT	α_{sat}	Saturation parameter	0.6
LAMBDA (V^{-1})	λ	CLM parameter	$5\ x10^{-2}$
DELTA	δ	Transition width parameter	2
MSAT	m_{sat}	Knee shape parameter	3.5
VTH (V)	V_{th}	Thermal voltage	0.02
VTHO (V)	V_{th0}	Thermal voltage at room temperature	0.02
I0L (A)	I_{0L}	Zero-bias leakage current	$3x10^{-14}$
VDSL (V)	V_{DSL}	Vds leakage dependence	7
VGL (V)	V_{GL}	Vgs leakage dependence	7
SIGMA0 (A)	σ_0	Minimum current	$3x10^{-10}$
TOX (m)	d_i	Oxide thickness	$80x10^{-9}$
DEF0 (eV)	dE_{F0}	Dark Fermi level position	0.56
EPSI	ε_i	Permittivity of gate insulator	4.1
EPS	ε_s	Permittivity of a-SiGe:H	11.8
NC (m^{-3}/eV)	N_C	Conduction band density	$3x10^{25}$

A.2 Set of equations of ambipolar a-SiGe:H TFTs.

Main current equation

$$Ids = I_{leak} + (1/I_{subn} + 1/I_{abvn})^{-1} + (1/I_{subp} + 1/I_{abvp})^{-1}$$

Leakage regime

$$I_{leak} = I_{0L}\left[\exp\left(\frac{Vds}{V_{DSL}}\right) - 1\right]\exp\left(\frac{-Vgs}{V_{GL}}\right) + \sigma_0 Vds$$

Subthreshold regime

$$I_{subn} = q\mu_n \frac{W}{L} V_{DSen}\, n_{S0}\left[\left(\frac{t_m}{d_i}\right)\left(\frac{V_{GFBen}}{V_O}\right)\left(\frac{\varepsilon_i}{\varepsilon_s}\right)\right]^{\frac{2V_O}{V_e}}$$

$$I_{subp} = q\mu_p \frac{W}{L} V_{DSep}\, n_{S0}\left[\left(\frac{t_m}{d_i}\right)\left(\frac{V_{GFBep}}{V_O}\right)\left(\frac{\varepsilon_i}{\varepsilon_s}\right)\right]^{\frac{2V_O}{V_e}}$$

$$V_{DSen} = \frac{Vds}{\left[1 + \left(\frac{Vds}{V_{saten}}\right)^{msatn}\right]^{\frac{1}{msatn}}}$$

$$V_{saten} = \alpha_{satn}\, V_{GTen}$$

$$V_{GTen} = V_{th}\left[1 + \frac{V_{GTn}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{GTn}}{2V_{th}} - 1\right)^2}\right]$$

$$V_{GTn} = Vgs - V_{Tn}$$

$$V_{DSep} = \frac{Vds}{\left[1+\left(\frac{Vds}{V_{satep}}\right)^{msatp}\right]^{\frac{1}{msatp}}}$$

$$V_{satep} = \alpha_{satp}\, V_{GTep}$$

$$V_{GTep} = V_{th}\left[1+\frac{V_{GTp}}{2V_{th}}+\sqrt{\delta^2+\left(\frac{V_{GTp}}{2V_{th}}-1\right)^2}\right]$$

$$V_{GTp} = -Vgs - V_{Tp}$$

$$V_{GFBen} = V_{th}\left[1+\frac{V_{GFBn}}{2V_{th}}+\sqrt{\delta^2+\left(\frac{V_{GFBn}}{2V_{th}}-1\right)^2}\right]$$

$$V_{GFBn} = Vgs - Vfbn$$

$$V_{GFBep} = V_{th}\left[1+\frac{V_{GFBp}}{2V_{th}}+\sqrt{\delta^2+\left(\frac{V_{GFBp}}{2V_{th}}-1\right)^2}\right]$$

$$V_{GFBp} = -Vgs - Vfbp$$

$$n_{S0} = N_C t_m \left(\frac{V_e}{d_i}\right)\exp\left(\frac{-dE_{F0}}{V_{th}}\right)$$

$$t_m = \sqrt{\frac{\varepsilon_s \varepsilon_0}{2q\cdot g_O}}$$

$$V_e = \frac{2V_O V_{th0}}{2V_O - V_{th}}$$

$$V_0 = \frac{E_{DD}}{q}$$

Above threshold regime

$$I_{abvn} = \mu_{FETn} C_i W/L V_{DSen} (1 + \lambda_n Vds) V_{GTen}$$

$$I_{abvp} = \mu_{FETp} C_i W/L V_{DSep} (1 + \lambda_p Vds) V_{GTep}$$

$$\mu_{FETn} = \mu_n \left(\frac{V_{GTen}}{V_{AA}} \right)^{\gamma}$$

$$\mu_{FETp} = \mu_p \left(\frac{V_{GTep}}{V_{AA}} \right)^{\gamma}$$

A.2.1 Parameters of ambipolar a-SiGe:H TFTs.

Table A.2 Ambipolar a-SiGe:H TFTs parameters summary.

Parameter	Symbol	Description	Value
VFB (V)	Vfbn	Flat-band voltage n-type	-0.01
VFB (V)	Vfbp	Flat-band voltage p-type	-0.3
VTO (V)	V_{Tn}	Threshold voltage n-type	-1
VTO (V)	V_{Tp}	Threshold voltage p-type	-1.2
EDD (eV)	E_{DD}	Characteristic energy of deep states	0.04
g0 (m^{-3}/eV)	g_0	Zero-bias density of deep states	$1.8x10^{23}$
MUBAND (m^2/Vs)	μ_n	Band mobility n-type	$28\ x10^{-4}$
MUBAND (m^2/Vs)	μ_p	Band mobility p-type	$10\ x10^{-4}$
GAMMA	γ	Power law mobility parameter	0.6
VAA (V)	V_{AA}	Characteristic voltage for μ_{FET}	16000
ALPHASAT	α_{satn}	Saturation parameter n-type	0.6
ALPHASAT	α_{satp}	Saturation parameter p-type	0.55
LAMBDA (V^{-1})	λ_n	Output conductance parameter n-type	$9\ x10^{-2}$
LAMBDA (V^{-1})	λ_p	Output conductance parameter p-type	$6\ x10^{-2}$
DELTA	δ	Transition width parameter	2
MSAT	m_{satn}	Knee shape parameter n-type	1.2
MSAT	m_{satp}	Knee shape parameter p-type	1.1
VTH (V)	V_{th}	Thermal voltage	0.02
VTHO (V)	V_{th0}	Thermal voltage at room temperature	0.02
I0L (A)	I_{0L}	Zero-bias leakage current	$3x10^{-14}$
VDSL (V)	V_{DSL}	Vds leakage dependence	7
VGL (V)	V_{GL}	Vgs leakage dependence	7
SIGMA0 (A)	σ_0	Minimum current	$3x10^{-10}$
TOX (m)	d_i	Oxide thickness	$80x10^{-9}$
DEF0 (eV)	dE_{F0}	Dark Fermi level position	0.56
EPSI	ε_i	Permittivity of gate insulator	4.1
EPS	ε_s	Permittivity of a-SiGe:H	11.8
NC (m^{-3}/eV)	N_C	Conduction band density	$3x10^{25}$

LIST OF FIGURES

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