Instituto Nacional de Astrofísica Óptica y Electrónica

Electronics Department

SYSTEMATIC APPLICATION OF A FULL-WAVE SOLVER TO DEVELOPING SCALABLE MODELS FOR HIGH-SPEED INTERCONNECTS

by

Abraham Isidoro Muñoz

Thesis submitted in partial fulfillment of the requirements for the degree of M. Sc. In Electronics

Supervised by:
Dr. Reydezel Torres Torres

Tonantzintla, Puebla
February 2017

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A Dios, gracias.

Abstract

In order to contribute to the improvement in the design of multilayer boards used for high-speed electronic applications, this project presents closed-form expressions for the capacitance and inductance related to vias (vertical transitions) in interconnects implemented in PCB technology. The importance of this contribution relies on the fact that these parasitic effects critically impact the performance of data channels by introducing undesired signal reflections. The development of the proposal is based on the systematic analysis of measurements and 3D electromagnetic simulations of actual high-speed links. Hence, a set of physically-based equivalent circuit models valid for different via pad sizes (scalable models) is obtained. This allows for the performance assessment and optimization of electrical transitions in channels in a fast and accurate way.

Here, the proposal is applied to channels implemented in moderate-loss materials (loss tangent of about 0.035) and up to 10 GHz. Nevertheless, as the reader will infer, the application of the methodology proposed in this thesis can be extended to lower loss materials and channels operated at higher frequencies.

Resumen

Con el propósito de contribuir al mejoramiento en el diseño de tarjetas multicapa utilizadas en aplicaciones de electrónicas de alta velocidad, este proyecto presenta expresiones cerradas derivadas para la capacitancia e inductancia relacionadas con vías (transiciones verticales) en interconexiones de circuitos impresos (PCB). La importancia de esta contribución se debe al hecho de que estos efectos parásitos impactan el rendimiento de los canales de datos al introducir reflexiones indeseadas de la señal. El desarrollo de la propuesta está basado en el análisis sistemático de mediciones y simulaciones electromagnéticas en 3D de canales de alta velocidad. Esto permite la evaluación del desempeño y la optimización de transiciones eléctricas de una manera rápida y precisa.

Aquí la propuesta es aplicada a canales implementados en materiales con péridas moderadas (tangente de pérdias de alrededor de 0.035) y hasta 10 GHz. No obstante, como el lector inferirá, la aplicación de la metodología propuesta en esta tesis puede extenderse a materiales con menores pérdidas y canales operados a más altas frecuencias.

Table of Contents

List of Figures

Chapter 1

Introduction

In current electronic systems, interconnects exist at various levels such as on-chip, packaging structures and printed circuit boards (PCBs). Furthermore, multi-gigabit per second data transfer is demanded and supported by high-speed data processing and communication technologies nowadays, making neccesary the use of signal rise times down to ranges within tens of picoseconds. In this case, the components forming the interconnection channels must be adequately characterized due to the fact that distributed behavior becomes apparent, introducing significant signal attenuation and delay. Furthermore, problems analyzed through transmission line (TL) theory such as reflections due to impedance mismatch, frequency-dependent losses and crosstalk, as well as the increase of design complexity, require the determination of corresponding electrical characteristics to systematically develop reliable models.

This chapter presents a brief overview of basic concepts related to the study of interconnects at integrated circuit and PCB levels. In addition, a description of popular approaches to overcome barriers imposed by signal propagation on interconnects, which limit the performance of electronics systems is discussed. Finally, a general explanation and implications related to the use of scalable models for design-oriented purposes, as well as their relevance within the context of the present work are presented.

1.1. Demand for high-speed interconnects in current applications

1.1.1. Moore's Law

In 1965, Intel co-founder Gordon Moore made the observation that the number of components in integrated circuits will double approximately every year. In 1975, looking forward to the next decade, he revised the forecast to doubling every two years; Moore predicted that this trend would continue for the foreseeable future. Based on this, the electronics industry started using Moore's Law not just as a descriptive, predictive observation, but as a target that the entire industry should hit (see Fig.1.1) [1-4]. In this regard, the exponential improvement that the law describes transformed the first home computers of the 1970s into the powerful machines of the 1990s. Later, it also allowed for the advent of services and devices such as high-speed Internet, laptops, as well as the handheld devices that are prevalent today.

Over the years, problems to keep pace with Moore's law formulation were solved through techniques such as migration to smaller technologies relative to the transistor channel's length [5]. For instance, for the 90-nm technology node strained silicon was introduced, for the 45-nm one it was necessary using engineered dielectrics to increase the gate capacitance in nanometer scale transistors, whereas for the 22-nm node FinFET tri-gate transistor technology was used. In fact, not too long ago a second generation of FinFET tri-gate technology was introduced for maintaining the scaling. But even these new techniques have been barely sufficient to follow Moore's prediction because factors related to the photo-lithographic processes and dissipation of energy increased the complexity in the scaling and added cost to chip fabrication. One example of how these problems impact the scaling today is that Intel originally planned to switch to 10 nm in 2016 with a new processor family, a shrunk version of the 14 nm Core-i7 (6th generation) launched in August 2015, according to its 'Tick-Tock' architecture optimization model; nevertheless, on July 16th of 2015, the company changed this plan. An extra processor generation was planned to be released in the second half of 2016, still using the 14 nm process, and a second wave of this Intel's processors family was launched recently on January 3rd of 2017. At the time

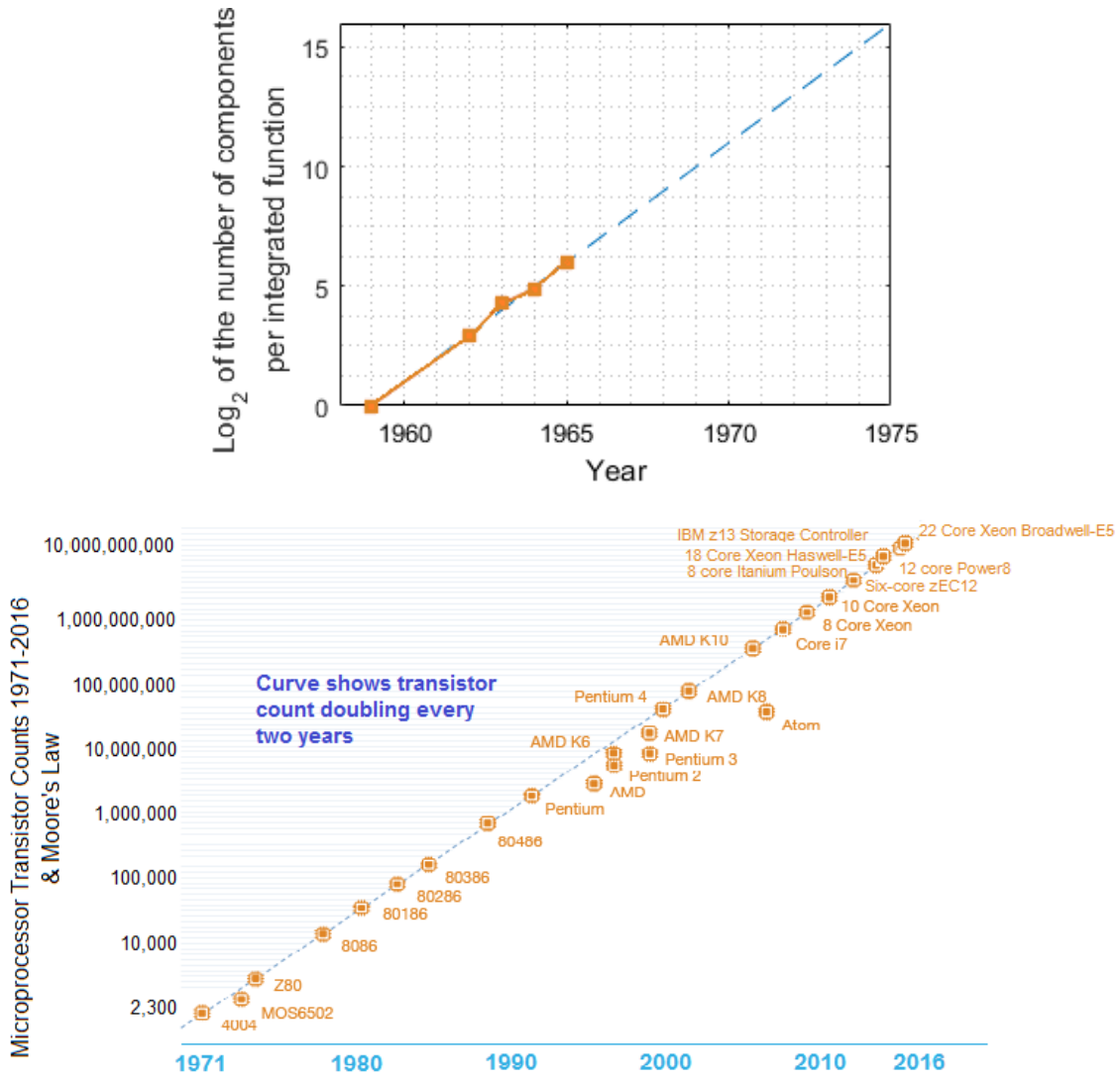

Figure 1.1: Top - Original graph describing Moore's prediction for the transistor count in integrated circuits [1]. Bottom - Microprocessor transistor count from 1971 to 2016 [1][3]. Observe the transistor count doubling each year in Moore's first observation and the trend to doubling each 2.1 years for the real count in the second graph.

this document is written, the 10 nm transistor technology is supposed to be released the second half of 2017. In consequence, Intel reported that their cadence is closer to 2.5 years than two [6]. This is one of the reasons why it is considered that Moore's law's age as a guide of what will come next and as a rule to be followed is coming to an end.

Now, how does Moore's law affect high-speed interconnect design? As noticed, Moore's law predicts a doubling in the transistor count for a chip every two years.

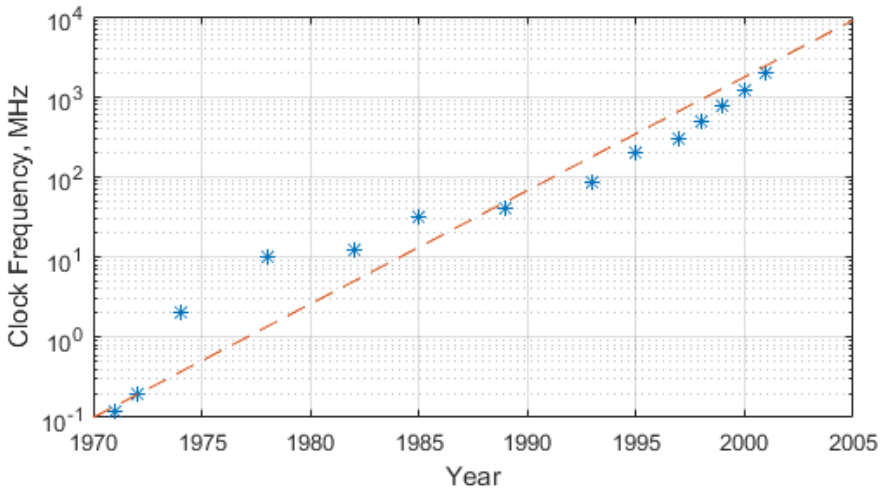

Figure 1.2: Historical trend in the clock frequency used by Intel in processors based on the year of introduction. The trend is doubling in the frequency every two years [7].

This scaling applies also for clock frequency (see Fig. 1.2) because as the gate channel length of transistors is manufactured at a smaller size, the switching speed of the transistor increases, reducing the time required for one operation cycle to occur [7]. As clock frequency increases, rise time of signals must be decreased, meaning a shorter time left for the signal to be correctly read. This implies higher data transfers at the expense of a higher susceptibility to undesired effects, which tightens the design budget [8]. Moreover, the higher integration density of components implies a major number of interconnects, aggravating signal integrity problems due potential interaction of communication channels which should be idealy isolated from each other.

1.1.2. Requirements for high-speed interconnects

Nowadays, one of the most important applications for high-speed communication systems is Internet. According to a publication of 2015 in the U.K. [9], it is supposed that around 2023 the cables and fiber optics that send and retreive information to and from electronic devices of common use will reach their limit. Fig. 1.3 shows a simplified view of fiber optic connections around the world. This represents a great challenge for scientists and engineers.

Regarding the currently active generation of devices for civil applications: the

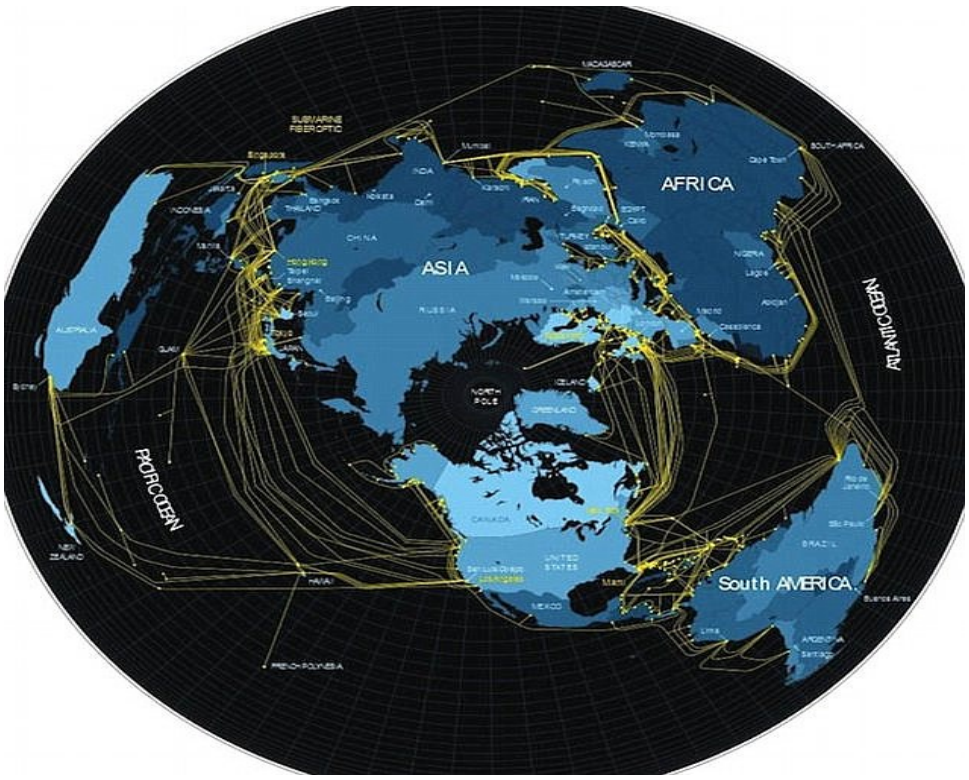

Figure 1.3: Illustration of what the Internet connections around the world look like [14]. Each yellow line represents one of the major fiber-optic cables that carry Internet traffic around the world; many of these are routed undersea.

USB 3.1 generation 2 (which is an industry standard), and the HDMI 2.0 interface support bit rates of 10 Gbps and 18 Gbps, respectively. This overcomes their predecessors (USB 3.0/USB 3.1 Gen 1 and HDMI 1.4) which supported maximum data transfers of 5 Gbps and 10.2 Gbps [10-11]. It must be mentioned that the increase in speed for USB obeys to a large number of contacts and the use of double differential signaling as can be observed in Fig.1.4. On the other hand, the main problem in designing the interconnects in PCB platforms of such kind of high-speed signals is the susceptibility to crosstalk, as well as the undesired signal reflections at corners and at via transitions. In this regard, some solutions involve increasing the distance between independent signal paths and including additional drivers for boosting signals. Nevertheless, because the amount of components and signals for platforms presenting the same size is increasing and using more drivers adds cost to the production and finally to consumers, better techniques for transmission of signals must be implemented.

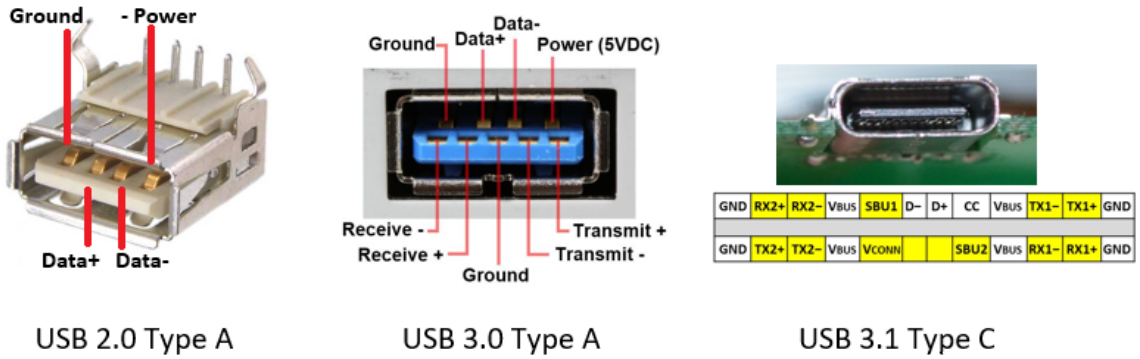

Figure 1.4: USB connectors. Left - USB 2.0 type A connector. Center - USB 3.0 type A connector. Right - USB 3.1 type C connector. Notice the increase in pinout for data transmission, and the fact that USB type C connector allows reversible connection.

1.2. Assessment of performance

1.2.1. Prototyping

In past years, the operation frequency of electronic devices was not as high as to originate serious signal integrity problems. Therefore, the traditional challenges faced by engineers were related to size, power consumption, and heat dissipation, among others. Thus, considering the transmission line nature of interconnects was not strictly necessary. In fact, in many cases, few tests were performed by validation teams to ensure correct functioning before approving a product. Conversely, today, with shorter lifetime cycles for the products and the trends in technology discussed before, it is necessary to take into account several previously neglected effects at different stages of the design that may substantially impact the performance. Hence, for the development of current electronics, prototypes and simulations of components must be carefully consider high-frequency effects. This is crucial for the designers and signal integrity engineers, because it allows to understand and identify the physical origin of effects influencing the operation of circuits and devices. In this case, better design guidelines can be followed before practical implementation. This increases the reliability of the product, and though this methodology increases the costs of development and production, it allows to reach the specifications easier and thus to faster get improved technology.

From the signal integrity point of view, the implementation and measurement of

the electrical properties of materials, circuits and devices through prototyping allow for the analysis of effects occurring at specific stages of the system provided that the external parasitic effects are removed from the experimentally collected data. In other words, the measurements have to exactly represent what would be happening in the analyzed part of the system (see Fig. 1.5). Thus, to completely characterize an interconnection channel or a specific part of it, sometimes even measurements performed with great care are not sufficient since de-embedding techniques or equivalent models accounting for systematic errors may be required to fully characterize desired device under test.

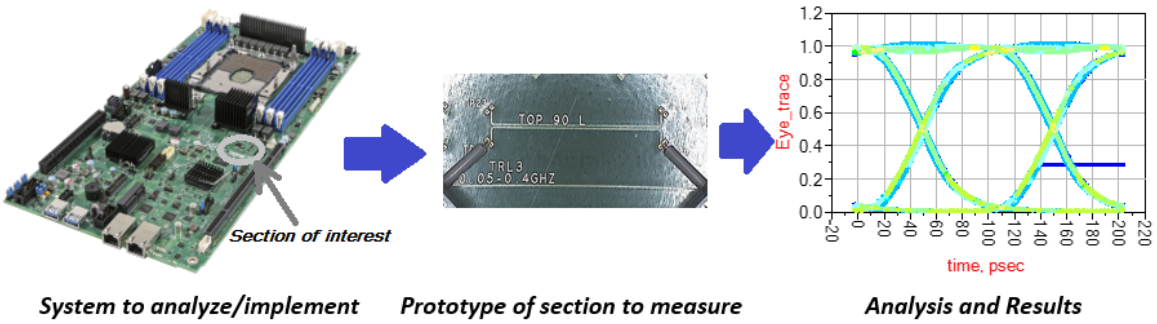

Figure 1.5: Purpose of prototyping: obtaining the electrical response of a DUT of interest.

1.2.2. Simulations

As stated before, to be useful for analysis, most of the times measured data require processing for the remotion of undesired effects. This is typical, for instance, when analyzing striplines or structures attached to them, which need the de-embedding of the effects associated with the transition vias or connectors. In this regard, some solutions reported in the literature perform physical remotion of certain parts of the channels [12], with the possibility of damaging the structure. Alternatively, structural models (to perform electromagnetic simulations) or equivalent circuit models can be very useful for representing the interconnect of interest. Nevertheless, there are advantages and constraints for each simulation approach. For instance, electromagnetic simulations yield accurate responses at the expense of considerable time for model implementation and substantial computing time. On the other hand, circuit simulations are faster, but highly susceptible to errors if models do not correctly represent the involved physical phenomena.

1.3. Design Flow

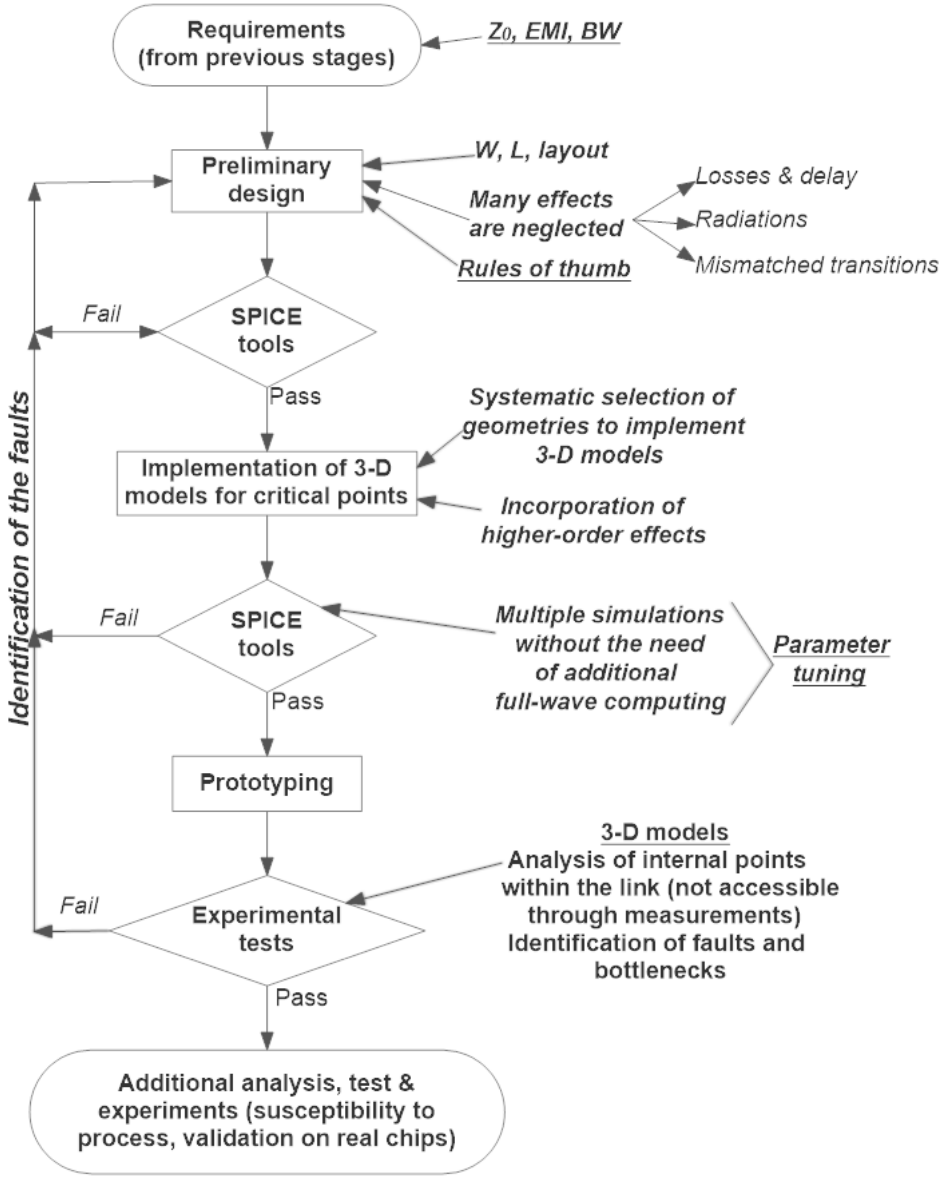

Figure 1.6: Simplified flowchart illustrating a design process which involves intensive modeling and measurement of interconnection structures.

Simulations are very important when developing interconnection platforms for high-speed electronic systems. In fact, intensive simulation work performed in a systematic way is of great help throughout the design cycle. In this regard, several steps must be followed by designers for achieving an adequate data transmission according to pre-established requirements. Fig. 1.6 shows a very simplified flowchart suggested

in this research project to be considered when designing an interconnection platform. Initially, the requirements are established, such as characteristic impedances, maximum return loss at the interfaces, data-transfer speeds or bandwidth of operation, maximum per-length attenuation and delay, etc. Afterwards, a preliminary design is carried out by making use of software and rules of thumb to determine approximate values of certain physical dimension of interconnects, sometimes neglecting undesired and second-order effects.

Later, depending on the requirements, it migth be necessary to analyzing the entire interconnection structure or certain segments of it where potential signal integrity problems may become accenctuated. At this stage, more information is needed to select the elements of interest and ensuring a correct determination of parameters to be observed in a practical implementation. The next step involves the generation of electromagnetic models to obtain accurate electrical responses with the possibility of tuning geometry in between the simulation cycles and generating improved models. After that, circuit equivalent models can be developed and implemented in order to become aware of the involved electromagnetic effects influencing the interconnect's performance. In this case, tuning the model can be realized in a simple and fast way so that structures with similar geometries can be analyzed now without the need of additional electromagnetic simulations.

Once these steps are completed, one can compare the results obtained from the application of the parameters using the corresponding model with the measured response. If a good correlation is observed, one could extract with great accuracy the electric effects of internal points within the interconnection channel that could not be accessed through simple measurement of prototypes. This allows for the identification, for example, of possible bottlenecks or faults in the structures that may degrade the signal integrity.

Further steps involve the analysis and implementation of structures under other variations in order to ensure a functional model in many conditions. These variations can consider susceptibility to processes, temperature and validation on more complex designs.

1.4. Considerations for practical models

The design of circuits using microwave and millimeter-wave components requires models which accurately describe the behavior of the different elements. These models must cover the widest possible range of variables, both geometric and electrical. If this cannot be done, a large number of discrete models have to be generated so that all the sizes and frequencies that are likely to be needed in a design are available. This process can be very time consuming when generating the required model libraries; moreover, it would probably require exhaustive electromagnetic simulations. In addition, considerable space within the prototype would be needed for test structures. Furthermore, the optimization and tuning for performing the model parameter determination would be difficult when only discrete device sizes are available.

Another subject to be considered when experimentally characterizing devices is de-embedding. This is because the effect of the pads and interconnects allowing to collect experimental data must be de-embedded so that the electrical performance at the device's intrinsic behavior can be determined. Nevertheless, it is necessary to bear in mind that many de-embedding methods do not take into account distributed effects, which occur in the device. This limits the range of frequencies and the size of the interconnects they are valid for. In this regard, in [13] it has been demonstrated that a correct de-embedding of pads taking into account frequency-dependent effects can be of great value to analyze complex structures with relatively simple experiments.

In general, it is desirable to have models for representing the parasitics associated with the test fixture that are scalable with geometry. In this case, measurements of devices presenting different geometries can be easily de-embedded. Thus, more accurate characteristics can be analyzed for sophisticated systems or presenting different sizes.

1.5. Chapter conclusions and purpose of this work

As mentioned in this chapter, the fast communication speed between electronic devices and high-density integration of components have increased the problems and

the complexity in the analysis of interconnection structures. To solve this, the correct identification and modeling of structures is required specially at critical points of the interconnects. Thus will allow the improved implementation of interconnects for preserving the integrity of the propagated signals.

In general, a methodology using full-wave simulations for characterization has the penalty of time consumption. On the other hand, the use of circuit simulations can provide less accuracy if the models do not correctly consider the effects related to the structure. For this reason, it is recommendable to use a methodology which accounts for the best of each, reducing time of analysis and computation, and providing acceptable accuracy in the characterizations. The purpose of this thesis is, through a systematic use of full-wave and circuit simulations, to achieve these goals and to develop new and more accurate models for specific structures: vias in PCB interconnects.

Chapter 2

Considerations for interconnection structures

2.1. Introduction

From a general point of view, packaging is the embodiment of electronic equipment. However, for a better understanding within the context of the present work, we can define it as the set of analyses and techniques for establishing interconnections between electronic components to form reliable circuits. Indeed, major functions for packaging that enrich the previous definition are [14]:

- signal distribution involving topological and electromagnetic considerations,
- power distribution involving electromagnetic, structural and material aspects,
- heat dissipation involving structural and material considerations, and
- protection of components and interconnects involving mechanical, chemical and electromagnetic aspects.

Thus, the objective of packaging is to ensure that the devices and interconnections are embedded with efficiency and reliability.

Since an electronic system is conformed by different parts, there are different levels to classify the types of interconnects within a package. These are [15-16] (see Fig. 2.1):

- Level 0 (chip-level packaging): Includes chip metalization and provides for chip-package interconnection.
- Level 1 (device-level package): It is the assembly of chips and a substrate to form a single or a multichip module.
- Level 2 (board-level packaging): Assembly of chip modules and other components on PCBs.
- Level 3 (motherboard level packaging): Depending on the sophistication of the system, it may involve several PCBs plugged into a motherboard.

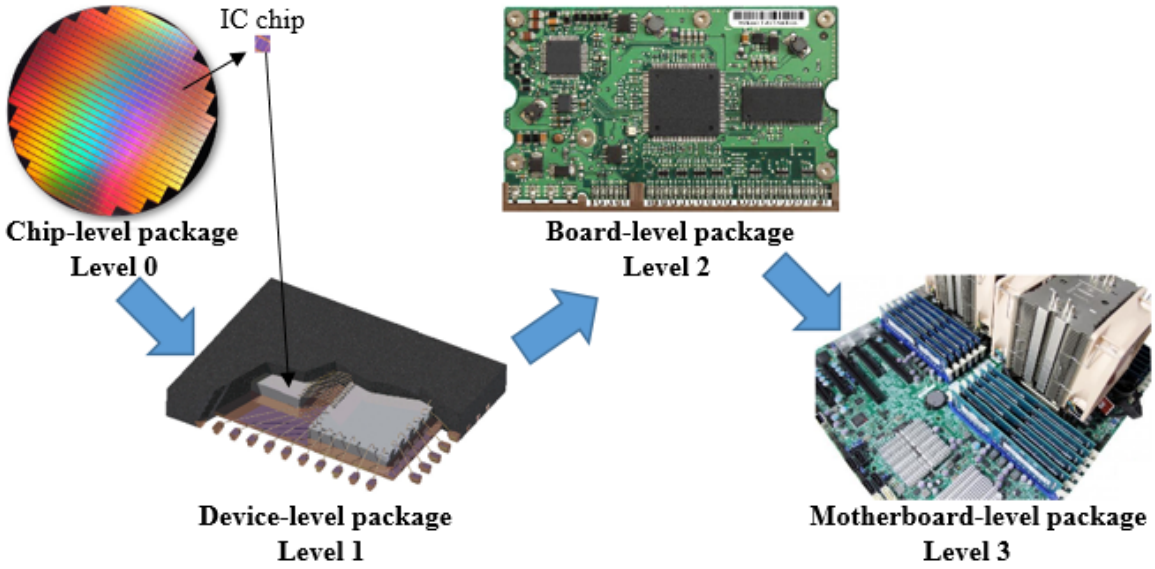

Figure 2.1: Packaging hierarchies within a typical electronic system.

This chapter is focused on interconnects at level 2 of packaging; nonetheless, the analysis can be easily expanded to other levels. At this second level, for better explanation, interconnects are used either to transmit information between ICs or to power them. In such way, there exist specific networks for each function. Also, they can be used to connect passive elements mounted on PCBs. Furthermore, since ICs need to interact with other devices within a system, it is necessary to efficiently handle the corresponding input and output signals to exchange information. So, this can only be achieved through the careful selection of the most appropriate materials and structures to implement the interconnects.

2.2. Multilayer packaging

Two approaches have traditionally been used to scale up the performance of electronic systems: i) increasing the speed of processing, and ii) increasing the number of interconnects [17]. The first one involves higher data rates and thus wider bandwidth is required per interconnect, whereas the second one needs more spacing to be implemented. Nowadays, in modern electronic platforms, these two approaches need to be simultaneously considered. Hence, the arrangement of the electronic devices plays a key role when designing a PCB. For this reason, the use of multilayer structures has emerged as an alternative to overcome the problematic of achieving a more space-efficient system.

In this section, the geometrical description of multilayer PCBs as well as other structures of major importance for signal transmission will be discussed.

2.2.1. Geometry of multilayer PCBs

The most common way to connect ICs and transmit signals between them is by using PCB platforms. PCBs provide, as described for packages, electrical connection and mechanical support. PCBs can be as simple as a conductor plane attached to a dielectric laminate. Other times, PCBs can be very complex such as in the case of arrays of dielectric and metallic planes with components embedded in its structure. Whichever the case, the impact of geometry and material properties in the performance of the circuit needs to be accurately described to ensure the correct type of interconnects for a given application.

A PCB is geometrically described by means of two patterns, the layout and the stackup. The first one shows a top-view of the several layers of the PCB, showing all the horizontal interconnects. Transmission lines, power and ground planes, location of vias, and other components, are observed in this perspective. On the other hand, the transversal information of the stacked layers is provided by means of the stackup. Emphasis is placed on the dielectric and metallic levels, thicknesses, surface roughness, permittivities and losses, as well as the purpose of each metallic level. Fig. 2.2 depicts some examples.

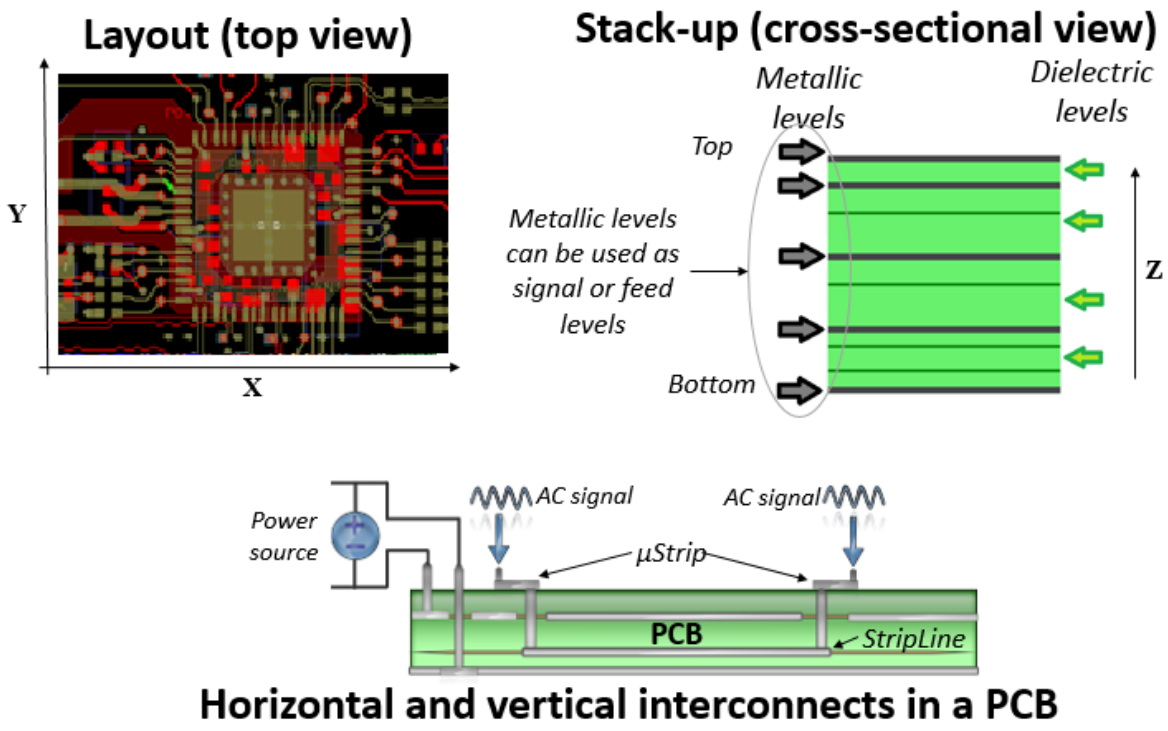

Figure 2.2: Layout and stackup for a PCB design. Top left - Example of the layout displaying horizontal interconnects in a xy plane for a three-dimensional model. Top right - Example of PCB stackup accounting for the description of dielectric and metallic layers, related to the z axis in the three-dimensional model. Bottom - Example of a cross-sectional view showing interconnects in a PCB for a point-to-point transmission.

A correct selection of material properties is fundamental in the performance of the system. In this regard, it is very valuable to know in advance the electrical properties exhibited by a material within the frequency range of interest. This consideration allows to select, within a group of materials, the most suitable for the design.

2.2.2. Microstrip lines

Microstrip lines (called microstrips for short) were developed as competitors to striplines by ITT Federal Telecommunications Laboratories in the 1950s, but became popular when thin substrates were used in the early 1960s [18]. These substrates allowed for a better confinement of signals at higher frequencies compared to the thick-substrate versions.

The geometry and an example of a PCB microstrip are shown in Fig. 2.3. This

type of line consists of a conductor strip of width W and thickness t formed over a grounded dielectric substrate (resin-reinforced glass fabric for PCBs) of thickness h and permittivity ϵ. There exist variations of this basic geometry called coated and embedded microstrips, with the conductor strip being partially or fully covered by the substrate.

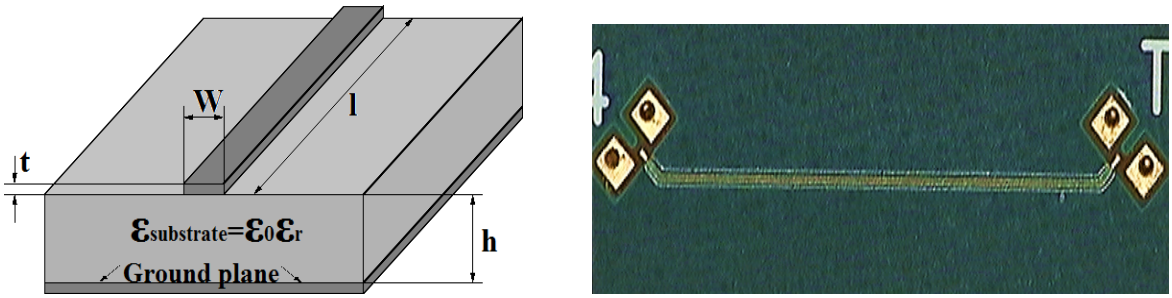

Figure 2.3: Structure of microstrip lines. Left - Perspective of a microstrip detailing the main geometry parameters. Right - Detail of a PCB prototyped microstrip.

Since the fields associated with the propagated signal travel in two media of different permittivity, an effective permittivity as well as an effective propagation constant must be considered for microstrips. This can be avoided if the conductor is suspended on air, or if it is embedded so deeply into the substrate that the fields are almost completely immersed within a homogeneous media, which is distinctive of a TEM transmission line. In addition, a third option occurs when another dielectric with higher permittivity and appropriate thickness is used as coating material, as demonstrated in [19]. Actually, the fields of microstrip lines constitute a hybrid TM-TE wave, as shown in Fig. 2.4. However, since the commonly used dielectric substrate is very thin when compared to the wavelength, the fields are considered quasi-TEM. This last consideration allows to obtain accurate solutions from either static or quasi-static analyses.

In structures where coupled microstrip lines are used to transmit signals, a special phenomenon occurs. Because the near proximity of conductor strips, the fields interact in such a way that the effective permittivity and transmission characteristics are modified. As a result, the propagation velocities and attenuation constants become dependent on this coupling. This dependence is due to the quasi-TEM consideration mentioned before. As an example, and in the scope of the present work, the use of common and differential signaling in a pair of coupled microstrip lines is mentioned. This originates two different propagation modes, called even and odd modes, respec-

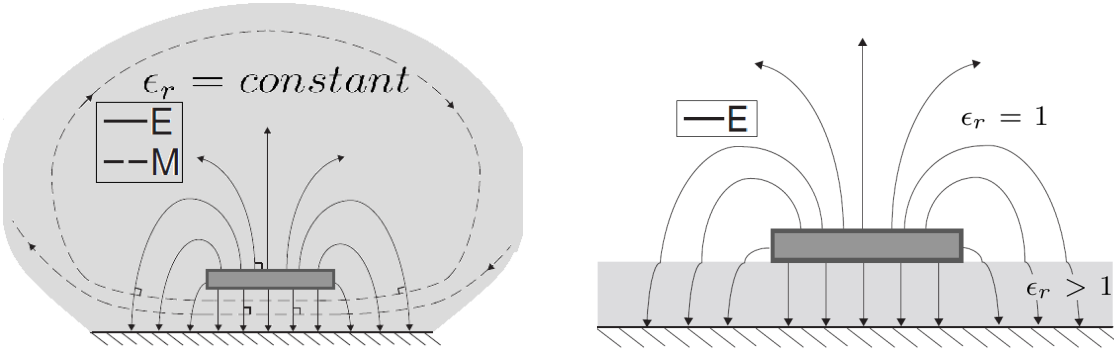

Figure 2.4: Electric and magnetic fields for microstrips formed on materials of: homogeneous permittivity (left), and different permittivity (right). Because the substrate is commonly very thin in current practical applications, the fields for the second case are considered quasi-TEM.

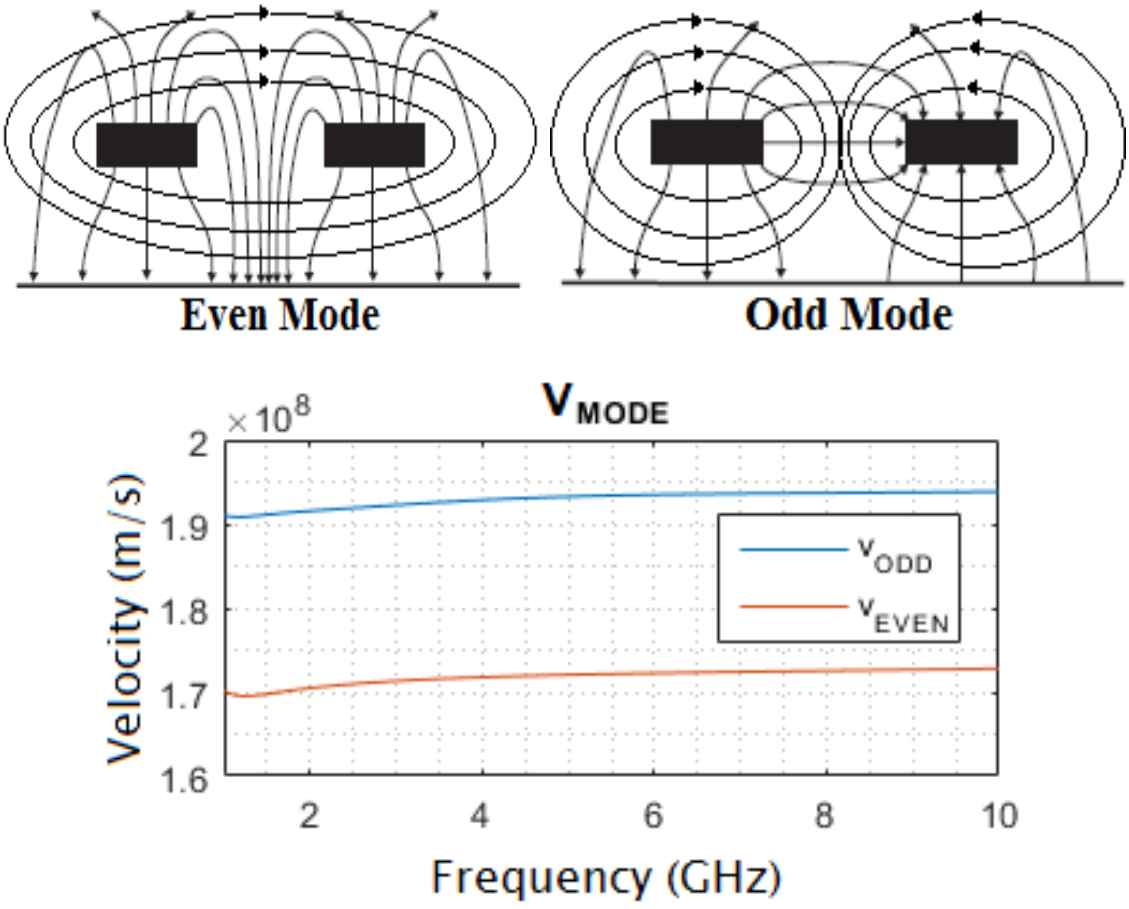

Figure 2.5: Fields for even and odd modes in coupled microstrips. Top - Conceptual depiction of the fields for even and odd modes. Bottom - Phase velocity versus frecuency curves for the two modes.

tively. The phase velocity according to each mode, v_e and v_o, are exemplified in Fig. 2.5. Notice in this figure that the signal travels faster when propagating in odd mode

since a higher percentage of electric field lines travels on air when compared to the even mode case.

2.2.3. Stripline

Striplines are commonly used in multilayer structures to perform interconnects within inner layers. They were invented by R. Barret in the 1950s [18], and were initially preferred over the first microstrips, as mentioned before.

The simplest geometry of a stripline and an example of a PCB stripline are shown in Fig. 2.6. In this figure, a conductor of width W and thickness t, is formed within a dielectric substrate of thickness b and permittivity ϵ, enclosed between two metallic planes ideally maintained at a constant potential, such as ground. There are special variations of this geometry. In one of these, known as asymmetrical stripline, the conducting strip is located in nearer proximity to a plane than the other. In others, dielectrics presenting different permittivity are used above and below the strip.

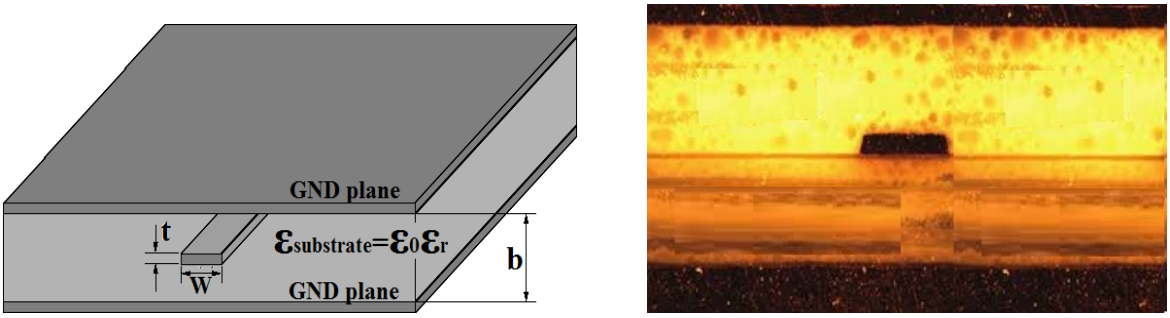

Figure 2.6: Stripline structures. Left - Perspective of a stripline detailing the corresponding geometrical parameters. Right - Transversal section of an actual PCB stripline [24].

Whichever the case, the fields are contained into the stripline structure so that they propagate in the TEM mode. Actually, the structure of the stripline can also support TE and TM modes; nevertheless, this is avoided by restricting the spacing between planes to less than $\lambda/2$. Thus, the velocity and propagation constant of the signals remain independent of the number of strips and the electrical signaling. Bear in mind, however, that even in the latter case the characteristic impedance depends on the propagation mode. In this regard, these structures differ electrically from microstrip. Fig. 2.8 depicts an example of the velocities, v_e and v_o, for a pair of coupled striplines as analyzed within the context of this project.

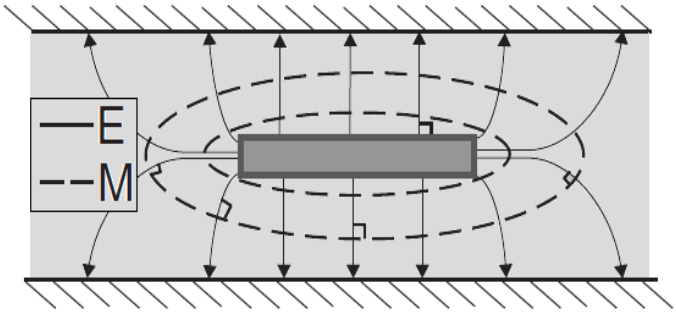

Figure 2.7: Electric and magnetic fields for a stripline. Because there are two conductors (conducting line and ground planes) and the dielectric media can be assumed to present homogeneous permittivity in many practical cases, the fields propagate in TEM mode. TE and TM modes (not shown here) can also be supported in this structure above certain frequencies.

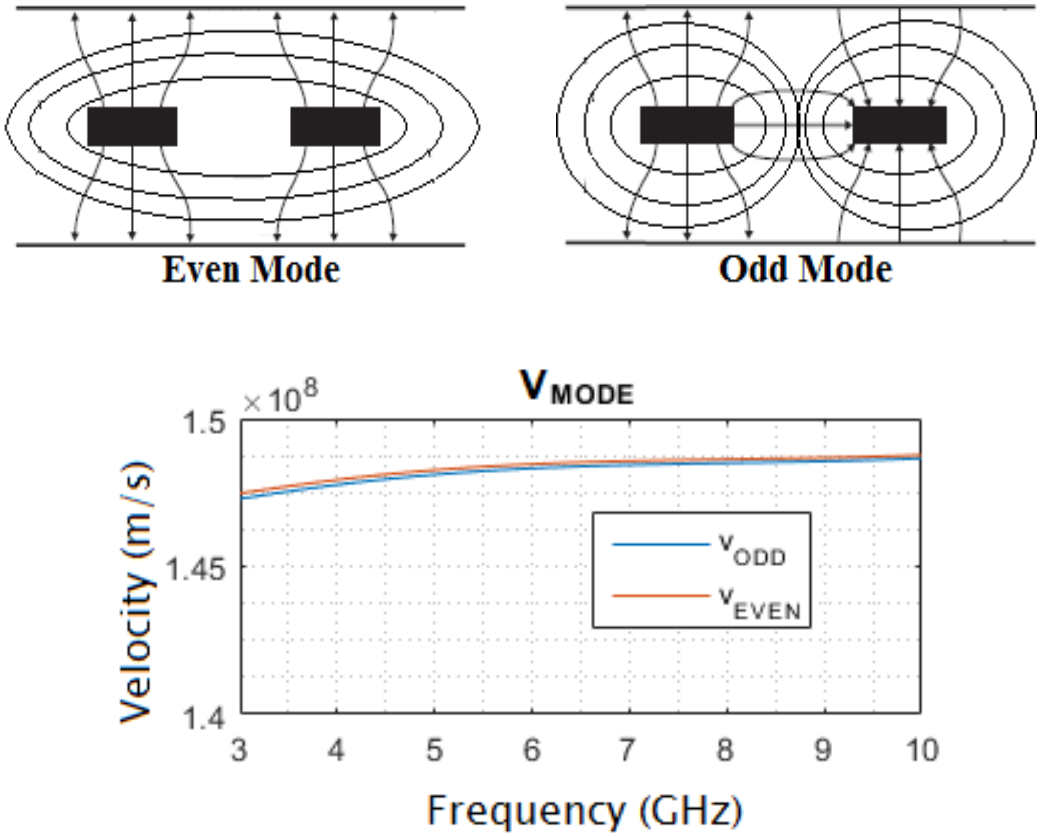

Figure 2.8: Fields for even and odd modes in striplines. Top - Electric and magnetic fields for even and odd modes in striplines. Bottom - Graph for velocities in a PCB case.

2.2.4. Vias

Vias are vertical interconnects that guide the signals between transmission lines formed at different layers of a multi-layered PCB. In this technology, a via is imple-

mented by means of a hole drilled through the multilayer structure and plated with a conducting material, known as barrel. For connecting this barrel to a transmission line at a certain level, a circular pad of conducting material is placed about it. These pads provide contacts for the transmission lines and also act as mechanical support. In most high-speed platforms, the barrel of the via passes through at least one plane destined to power delivery or ground reference. Therefore, clearance holes at these planes are left so that the barrel can pass without making contact to ground or power (unless there is need to do so). The most common type of via is the through-hole via, for which the hole is drilled trough all dielectric and metalic layers. Other types of vias are the blind via, the buried via, the step via, the stacked via, and the microvia. A top view of a via structure, as well as the different via types mentioned, is shown in Fig. 2.9.

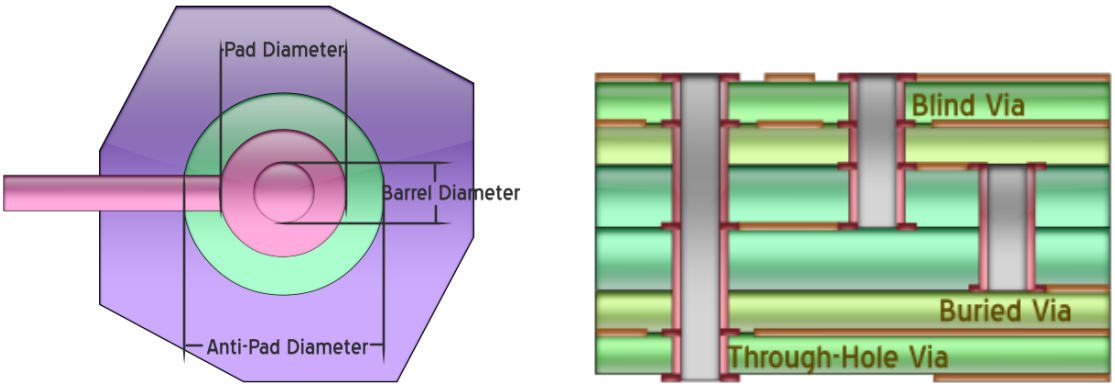

Figure 2.9: Structure of a via. Left - Top view denoting the different constitutive parts. Right - Three different types of vias.

The typical process for via fabrication makes use of mechanical drilling, although other manufacturing methods are available, as shown in Fig. 2.10. Among these, it is possible to count: the laser via technology, mechanically drilling blind via technology, photo process defined vias, plasma via technology, and insulation displacement [21-22].

Due to the enhancement in speed, density, and routing complexity for ICs, package and board design, vias are widely used to provide signal and return paths for the signals. However, a wide variety of other applications of these structures is available in the open literature. In fact, although this project is focused on effects occurring in signal vias, it must be mentioned that a design using appropriate configurations of vias can provide, for example, better control of undesired effects related to impedan-

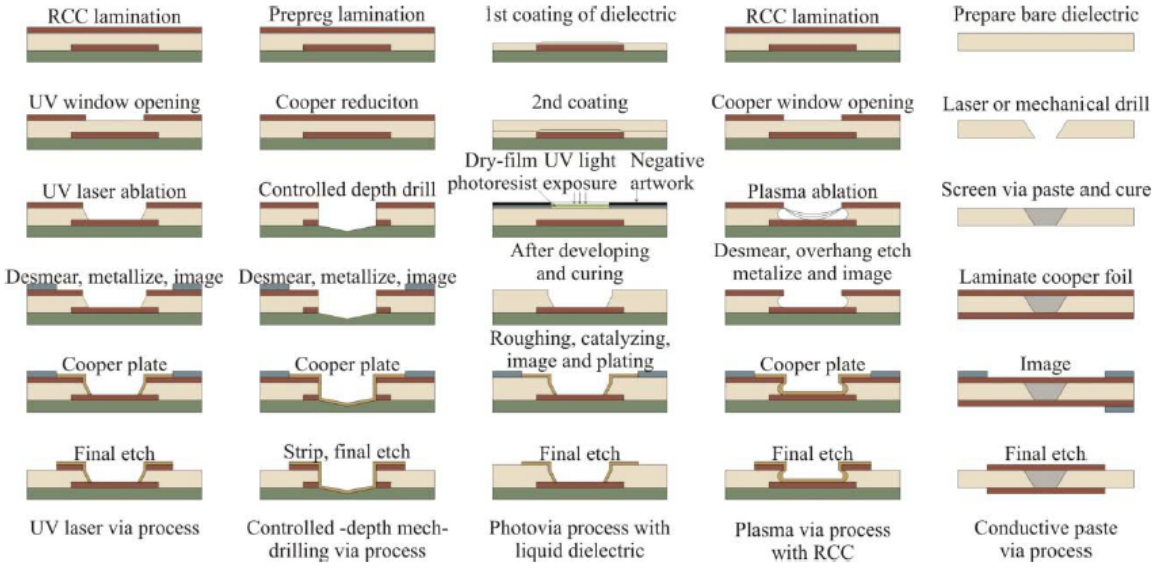

Figure 2.10: Methods of via fabrication [26].

ce mismatch and radiation. In this regard, improvement in the signal transmission is observed when a signal via is surrounded by two or more adjacent ground vias [23]. Nevertheless, these vertical interconnects are also used for short-circuiting metal planes to keep the potential as close as possible between ground planes and between power planes. Other applications include the use of vias as plug-in receptors for mounting a through-hole component to a board or other modules [24]. Just to mention one of the most important negative effects introduced by vias, mode conversion (reconfiguration of the electromagnetic fields to undesired propagation modes) usually seen as leakage of the signal occurs when these vertical interconnects are improperly designed. Although this effect is neglected in the present work because the vias are too short when compared with the signal wavelength, it is worth to mention that there are cases when this characteristic cannot be ignored; for example, when vias are purposely implemented to emit radiation. Consider for instance, mode conversion used in the excitation of a waveguide or when a smooth transition between different waveguides is required. In addition, another use for this characteristic is in substrate integrated waveguides (SIWs) [25-26]. Examples of the mentioned applications are shown in Fig. 2.11.

It has been reported that vias are related to many problems in interconnects at high-frequencies. These include impedance mismatch, electromagnetic interference,

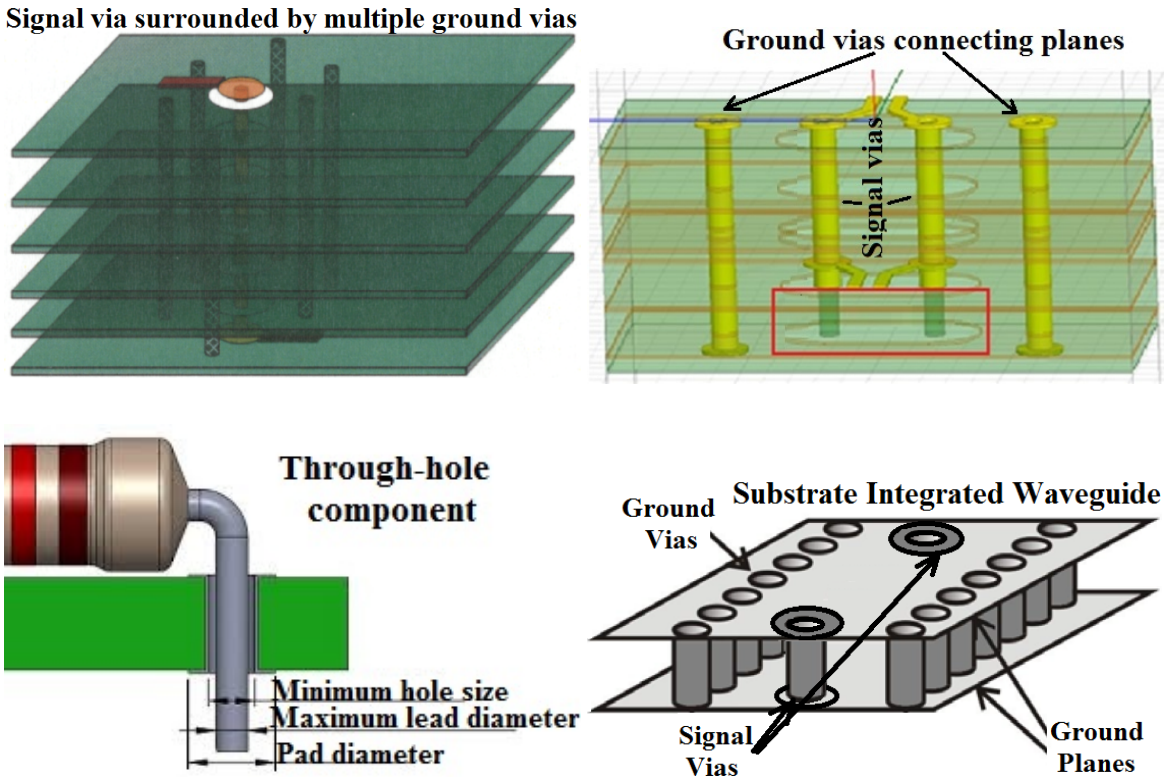

Figure 2.11: Applications of vias in multilayer structures. Top left: Signal via surrounded by multiple ground vias to achieve better control of reflections [27]. Top right: Ground vias used for short-circuiting metallic planes to keep a constant potential. Bottom left: Vias used as plug-in receptors for through-hole components [28]. Bottom right: Vias used in substrate integrated waveguides as signal launchers.

radiation, mode conversion, etc. In this regard, a correct modeling of vias typically entails complex equivalent structures for analyses, as shown in Fig. 2.12. Since the objective of this work is analyzing the electrical behavior of signal vias related to a particular variation of the structure, this aspect is studied later in this document.

2.3. Differential links

In digital electronics, the signaling scheme known as single-ended is that one where the interconnections between components, such as drivers and receivers, are implemented with a dedicated transmission line for each bit. This scheme works well enough for low frequencies up to hundreds of MHz or a few GHz. However, at higher frequencies, when the systems become notoriously noisy, it is difficult to maintain a good quality for the signals with this approach. A strategy commonly used to

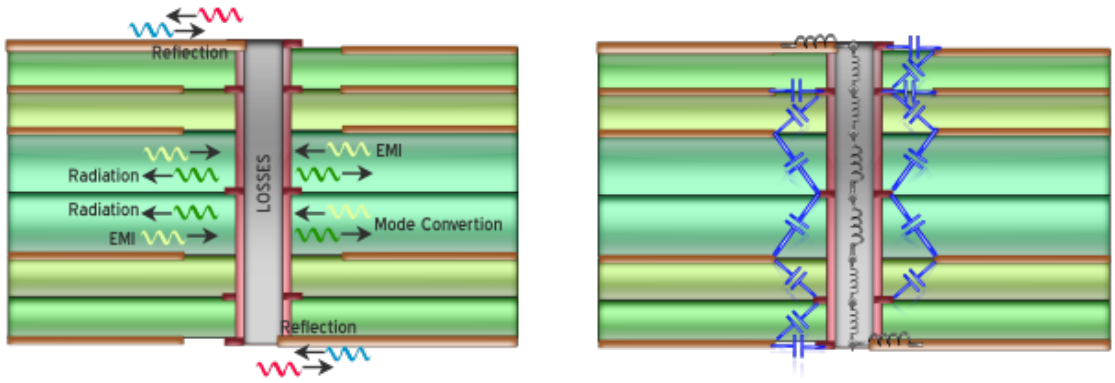

Figure 2.12: Left - Main problems related to vias at high-frequencies. Right - Approach for model of a via using an equivalent circuit.

overcome this limitation is the differential signaling.

For differential signaling, a pair of transmission lines is dedicated to transmit each bit on the communication bus. Thus, the signal transmitted through each one of these pairs consists of complementary voltage waves. In other words, the waves present the same magnitude, but a phase difference of 180 degrees. This provides the advantages of high common-mode noise rejection, avoidance of EMI at high frequencies, and less radiation. In consequence, many modern communication systems nowadays use the differential scheme. The characteristics for the aforementioned schemes are depicted in Fig. 2.13.

The common-mode noise immunity in the differential signaling scheme is because any noise induced to a pair of closed-parallel conductors generally appears equally on both conductors. So, since the receiver responds only to a voltage difference V_{diff}, the influence of noise is considerably reduced as shown in (2.3.1):

$$V_{\text{diff}} = (V_{\text{D+}} + V_{\text{common noise}}) - (V_{\text{D-}} + V_{\text{common noise}}) = V_{\text{D+}} - V_{\text{D-}} \tag{2.3.1}$$

Another advantage is that the complementary nature of differential signaling creates a virtual reference for the electric and magnetic fields, as shown in Fig. 2.14. Thus, a return path for the current with relative independence to the ground is provided. Hence, signal integrity can be preserved even when non-ideal references exist. Examples of issues mitigated by this characteristic are: the undesired effects in connectors and layer transitions, bounces in ground and power planes due to the switching of nearby devices (known as simultaneous switching noise, SSN), and splits in the reference

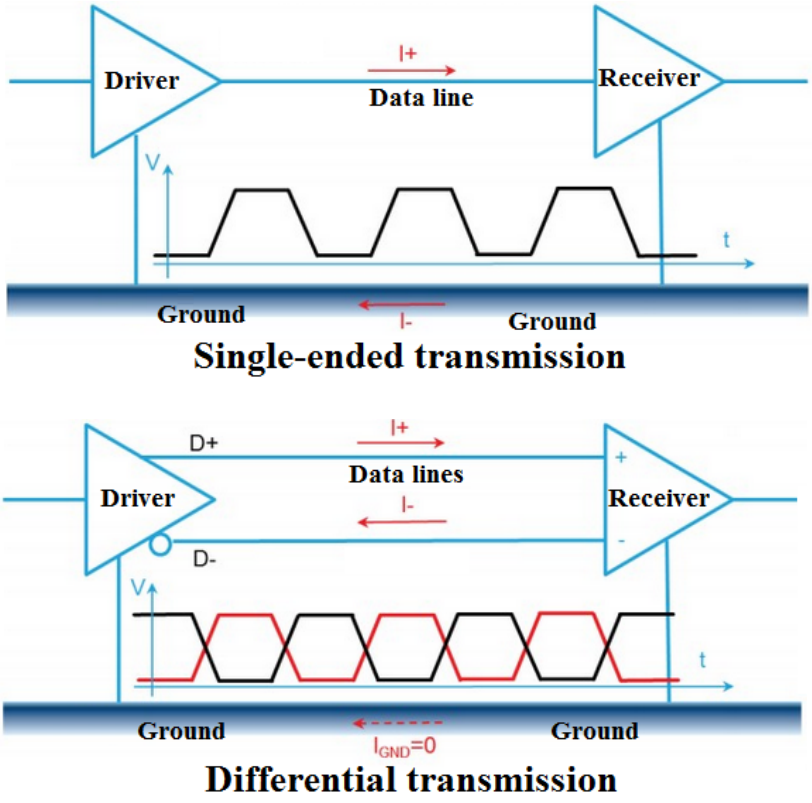

Figure 2.13: Illustration of the single-ended and differential signaling schemes. Notice that in the single-ended scheme, the ground serves as the return path for the signal. In the differential scheme, the complementary line acts as the return path, neglecting the contribution of the ground reference as long as the distance between lines is closer than the distance to ground.

planes for the location of different power supplies.

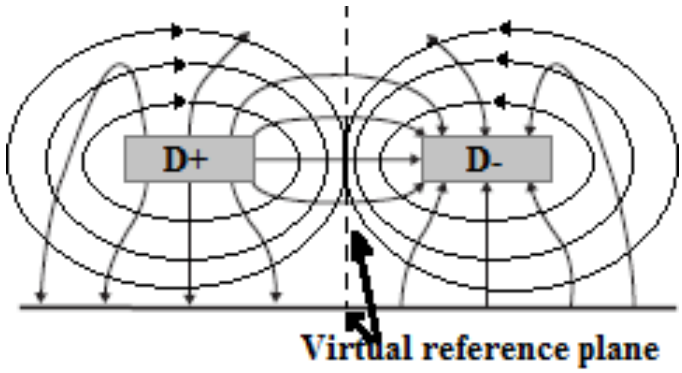

Figure 2.14: Virtual reference for electric and magnetic fields in a microstrip coupled pair. Notice that even if the ground plane suffers from non-idealities such as voltage variations, the virtual reference plane ensures a path for the current between the lines.

In addition to the aforementioned, interference and radiation within structures

carrying differential signaling is much smaller than in structures with single-ended configuration. This is easily explained using electrostatics concepts: as Electromagnetic Theory dictates, the electric field due to a point charge (a monopole) decreases with the inverse square of the distance to the charge. For a dipole charge configuration, the fields decrease with the inverse cube of the distance. This is shown in Fig. 2.15.

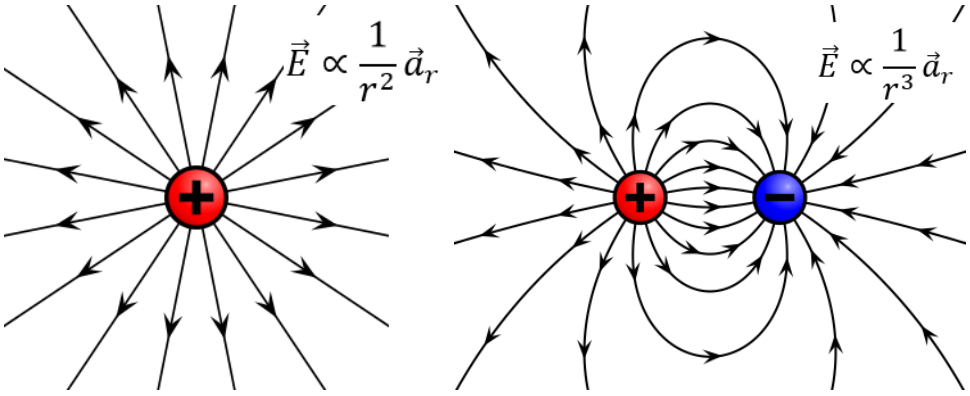

Figure 2.15: Electric field due to a monopole and to a dipole. Notice that the interaction between the opposite charges in the dipole reduces the influence of the electric field at a certain distance when compared with the monopole.

2.4. Effects degrading the signal on PCB channels

At high frequencies, losses in materials acquire great importance in the design of interconnects. The impact of these losses is easier observable when using currently considered low and medium performance materials.

In the case of conductor losses, temperature as well as conductor roughness play important roles. For this reason, for instance, when modeling interconnects at relatively high temperatures, some research [27-28] suggests considering metal conductivity values significantly smaller than the nominal ones at room temperature. In this regard, it is noticed that typical operation temperatures for electronic equipment might be as high as to be within the range of several tens of Celsius degrees above room temperature. In the case of roughness, the metal losses are significantly increased when compared with those expected when only considering the skin effect and smooth surfaces [29-30] (please see Fig. 2.16).

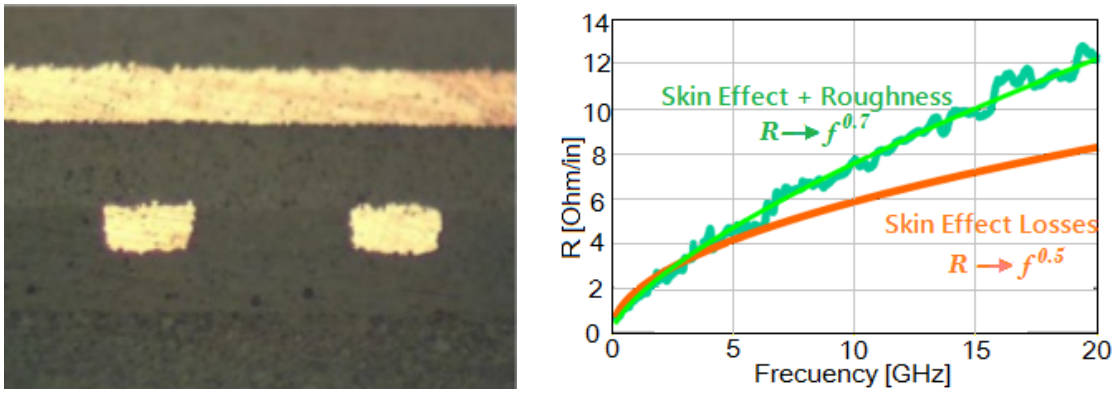

Figure 2.16: Effect of roughness in conductor materials. Left - Optical micrograph of the cross-section of a package showing copper traces presenting a rough surface [24]. Right - Frequency-dependence of the resistance for a rough metal trace.

On the other hand, dielectric losses are due to the polarization currents occuring within the dielectric substrate as time-varying fields propagate guided by the interconnects. In this regard, when accounting for the corresponding effects in PCB, it is worth to mention the importance of the glass-to-resin ratio effect. This is because current dielectric materials are made of woven glass fibers impregnated with resin. Since the dielectric properties of both materials differ (commonly with the resin as the lossier material but the lowest dielectric constant), the effective value of permittivity and loss tangent for the dielectric environment depend on the glass-to-resin ratio. The structure of a typical dielectric laminate used on PCB technology is shown in Fig. 2.17.

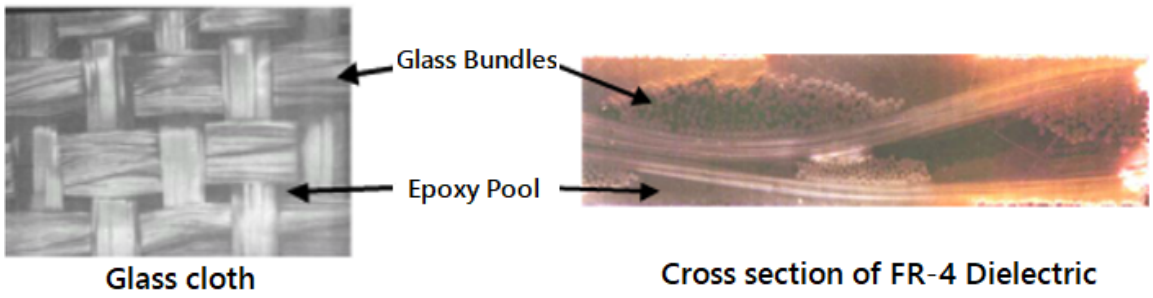

Figure 2.17: Glass-to-resin ratio effect. Left - Example of glass cloth. Right - Cross section of a FR-4 dielectric laminate showing the glass cloth and epoxy [17].

At this point, it is worthwhile to mention that dielectric losses reduce the coupling between adjacent elements, such as vias or traces, and the negative impact of reflections from discontinuities. This can contribute in a manner to the reduction of spaces

in electrical structures. In this regard, to some extent losses can bring some benefits to the routing schemes.

Now, in particular for differential signaling schemes, the most important issues degrading the signal quality are the losses (both due to the conductor and the dielectric materials. Nevertheless, EMI and noise coupling when the channel is not properly balanced or filtered are becoming important as the operation frequency increases to multi-gigabit per second data transmission rates. These effects may originate a significant common-mode component to the signal, as well as conversion from common-mode noise to differential-mode noise, which is potentially more dangerous for the appropriate interpretation of information by the receiver. These problems are more commonly observed in differential pairs where the individual lines present length variations, generally due to corners and folds. It is noticed that the negative impact of these variations can be diminished by means of length matching schemes (please see Fig. 2.18). Another downside is that, in order to transmit a differential signal, the system requires twice the number of signal lines used to transmit a single-ended signal. In this regard, modified single-ended geometries can be used as alternative. One of these includes the shielding of single-ended interconnects by surrounding the signal trace with guard lines, one by side. Unfortunatelly, at the end, this increases the problem of space, compared to the differential approach. Thus, why many designers select this type of single-ended approach? Because there are many additional principles to understand and a few key design guidelines for differential pairs, whereas single-ended lines are much easier to analyze.

A very interesting and yet undesired effect degrading the quality of differential signals, as well as single-ended configurations, is the fiber weave effect. This is observed in non-homogeneous materials, more specifically in composite materials such as PCB dielectric laminates [31-33]. As mentioned before, these materials are made of a composite of fiber fabric and resin. The yarns of fiber run perpendicular to each other. Depending on the orientation of the weave relative to the trace, there could be either resin or a fiber bundles beneath the trace, as shown in Fig. 2.19. Due to the different dielectric properties between these two materials, the phase skew between the supposedly complementary waves guided by the differential pair may be substantial. This skew manifests itself as common mode noise at the receiver, similar to the effect of difference in lengths, affecting both voltage and timing margins at the receiver.

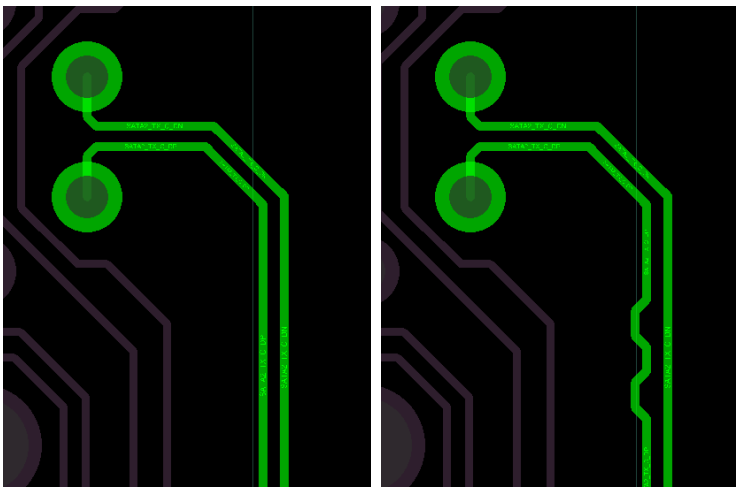

Figure 2.18: Length matching for a differential pair. Left - Differential pair with individual lines presenting different effective length; this pair is very susceptible to mode conversion and noise coupling. Right - Differential pair presenting bends but compensated using serpentine routing.

Among the techniques used to reduce this issue [34], one involves the routing of the trace in a straight line with offset in the middle equal to a glass bundle pitch, but this can differ by materials and direction, in addition to be dependent on the particular manufacturing process. Other techniques involve a zig-zag routing, maintaining a certain angle between the trace and the fiber weave, and rotating the weave relative to the edge of the PCB, maintaining differential trace routes aligned with edges of the PCB. A last option involves the use of alternate PCB materials.

2.5. Impact of the geometry on the performance of vias

Due to the importance of vias in defining the performance of a practical interconnection channel, different approaches for characterizing the signal reflections and losses that these structures introduce have been reported in the literature. Some basics on the modeling of this type of vertical interconnects are presented afterwards.

As a first example of an equivalent circuit for a via is the one shown in Fig. 2.20, which neglects losses and only accounts for the reactive parasitics that introduce signal reflections. According to the literature, this model provides acceptable accuracy

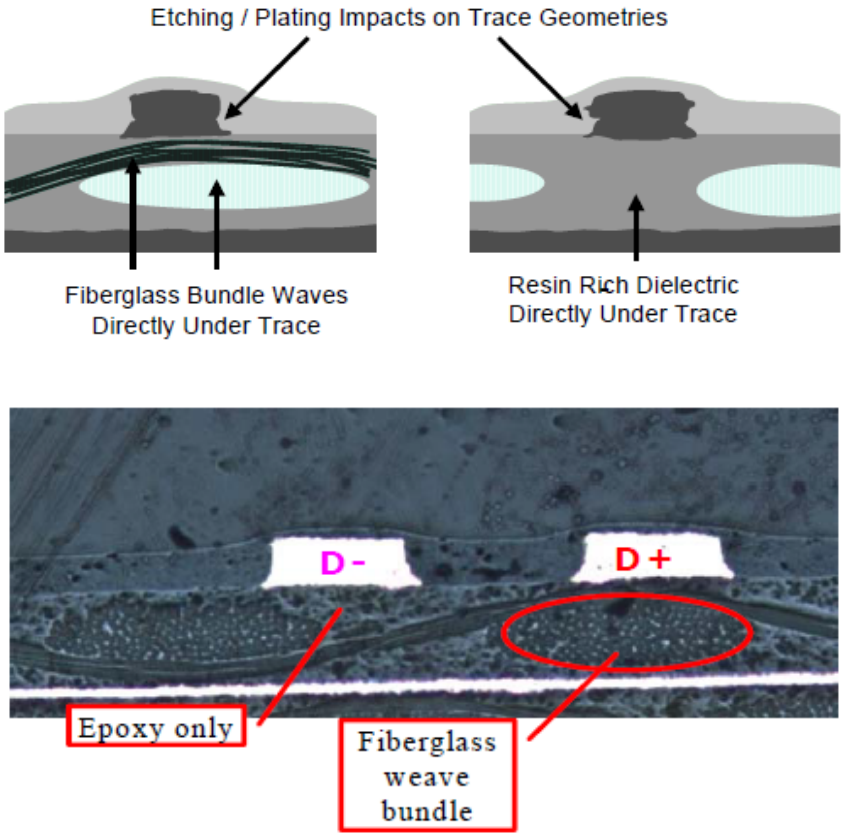

Figure 2.19: Fiber weave effect. Top - Illustration of traces on a typical PCB composite. Bottom - Image of a real PCB cross section. Differences in dielectric properties of a composite can cause signal degradation. Notice fiber weave bundle and epoxy regions. Courtesy of Intel.

up to frequencies of a few gigahertz. The idea behind this model is using a pi network to represent the via using lumped components. Thus, two capacitors are employed to represent the effects of the pads connecting the barrel to the transmission lines. Moreover, if stubs or additional unused pads are involved into the structure, their capacitive effects are also described by these capacitors. On the other hand, he inductor is related to the inductive effect of the barrel. Bear in mind that the inductance of the transition between the signal traces and the via pad is not considered. Simple close-form expressions related to this model are given in eq. (2.5.1) and eq. (2.5.2) [35].

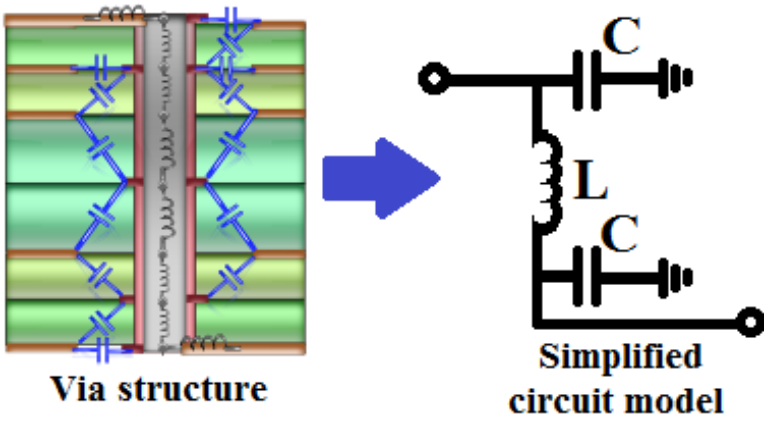

Figure 2.20: Basic circuit model for vias. The model does not consider any losses.

$$C = \frac{1.41\epsilon_r T D_{\text{pad}}}{(D_{\text{antipad}} - D_{\text{pad}})} \tag{2.5.1}$$

where
C = via capacitance (the obtained value must be divided by 2 in the model for each pad), pF
ϵ_r = dielectric relative permittivity
D_{pad} = pad diameter, in
$D_{antipad}$ = antipad diameter, in
T = thickness of the multilayer structure, in

$$L = 5.08 h_{via}[ln(\frac{4h_{via}}{D_{via}} + 1)] \tag{2.5.2}$$

where
L = via inductance, nH
D_{via} = via diameter, in
h_{via} = via length, in

One of the main problems observed when using the equations associated with this model is that the location of the pads where the traces are connected is assumed to occur at the external layers (i.e., for interconnecting microstrips). In addition, it is assumed that pads exist at each metal layer in multilayer PCBs so that a cylindrical capacitance can be assumed in the calculation. In addition, there is no consideration

for the fringing-fields outside the structure. Nevertheless, important information is obtained from these expressions. First, when the pad size approaches the clearance hole diameter, the capacitance increases remarkably. Afterwards, a linear relation with the thickness of the structure is observed, for both capacitance and inductance. Additionally, it is observed that for a big barrel diameter, the inductive effect is significantly lesser than for small diameters; furthermore, its capacitive effect increases.

A second model with a consideration for losses is described in [22] and depicted in Fig. 2.21. In this, a series resistor appears next to the inductor, representing the conductor losses associated to the barrel. For the case, an extraction based on admittance-parameters is proposed for the values in the model. It must be noticed that the resistor can be replaced by an equivalent impedance Z_{eq}, which can also account for leakages related to radiation, whose characterization was the main purpose of the project in reference.

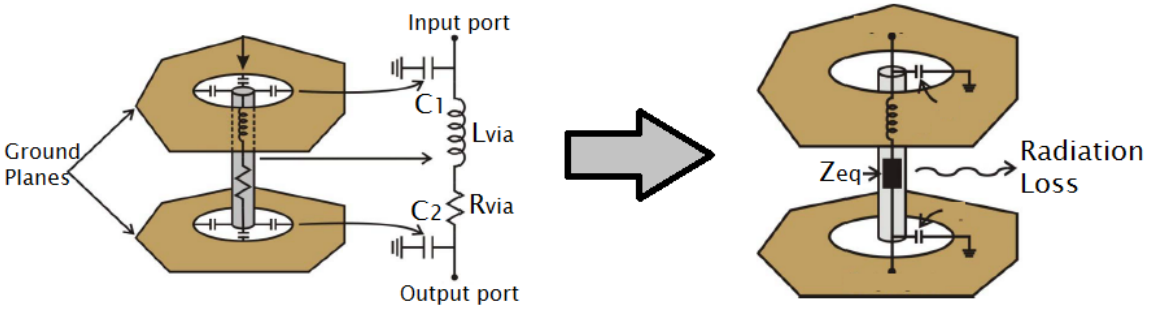

Figure 2.21: Basic circuit model for vias with losses [26]. The losses considered in the model represent conductor losses and leakage due to radiation.

Another model, the most complex of the three mentioned here, is the one developed in [36]. In this one, the interplanar spacing is considered, as shown in Fig. 2.22, and accurate results are obtained for some coupled structures but through complex expressions. However, effects related to fringe-fields and those related to multiple unused pads are neglected. Additionally, in the initial analyses considered for capacitance, $C = Q/V$, there are only geometrical considerations used in the calculation of the net charge, without care for the voltage due to a finite distribution of charge.

As observed, some of these models do not consider neither coupling effects nor the location of the pads in inner layers. In general, most of the published work commonly shows either complex equations accounting for high order effects or good approxi-

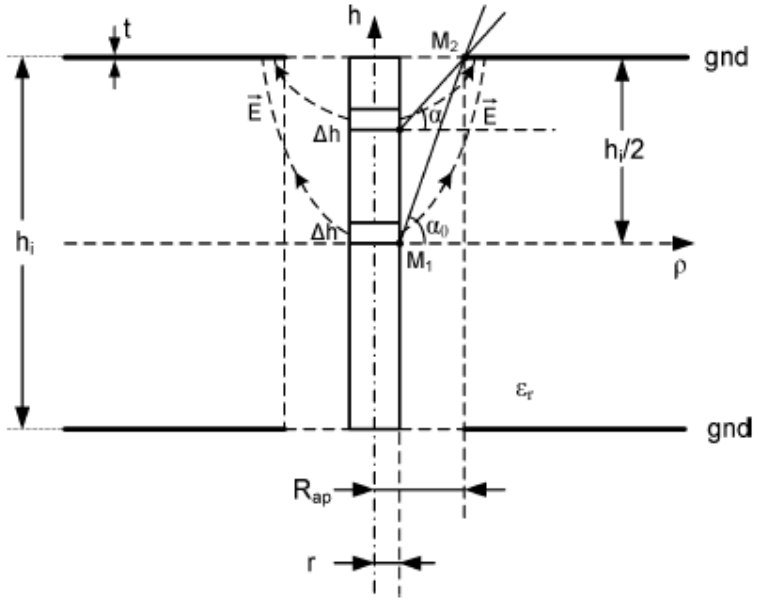

Figure 2.22: Basic circuit model for vias with losses [26]. The losses considered in the model include those associated with the conductor resistivity and the leakage due to radiation.

mations accounting for simple structures [36-37]. Therefore, it becomes necessary to develop new and simpler expressions for these components. In this regard, careful description of the physical phenomena occurring in these structures is of great importance for representing high-speed interconnects with better accuracy.

2.6. Problem statement and goals of the project

In high-speed system design, a correct characterization of interconnects is mandatory for achieving appropriate data transmission. In this regard, vias used to transmit signals in multilayer structures, can be seen as electrical discontinuities that must be characterized and modeled. This is due to the fact that, the associated reflections interpreted as impedance mismatch degrade the power delivery from one circuit stage to another.

The purpose of this project is to perform a correct characterization and modeling of effects related to the capacitance and inductance of coupled vias. For this purpose, the main interest is focused on the impact of the variation of the pad size on the electrical properties of a via. Therefore, the goal is to provide, based on full-

wave simulations and the application of the methodology described in section 1.3, an equivalent circuit model with the following characteristics:

- The model must be based on physics (scalable with geometry and must admit considerations for different material properties).
- The model must describe the via for both single-ended and coupled interconnects.
- The model must allow the assessment of the losses.
- The model must be easily implemented in simulation programs to admit fast tunning.

Chapter 3

Considerations for modeling

3.1. Introduction

In this project, S-parameters are used to perform a systematic analysis that leads to the development and assessment of the modeling and characterization proposal. The description of these network parameters has been available in the literature for many years and is the preferred choice to study and solve signal integrity problems since the beginning of the decade of the 2000's [17, 38, 39]. Moreover, with the availability of multiport test equipment [40-41], S-parameters associated with linear networks presenting several input and output terminals can be experimentally collected these days. This is the reason why this project also takes advantage of this fact to analyze differential data links using both simulated and measured four-port S-parameters [42]. For this purpose, the relatively recently developed mixed-mode S-parameter set is also employed in this work [43]. Nevertheless, due to the fact that much of this theory is currently considered as textbook knowledge, the detailed explanation of S-parameters (e.g. two-port, multi-port, and mixed-mode) is not included here.

On the other hand it is important to point out the fact that measured and simulated S-parameters are used in this project. Although all the processing and analysis is performed by the author of this thesis, the measurements were provided by engineers working for Intel in Guadalajara, Mexico. In addition, all the material and structure features of the implemented prototypes were also provided by them, which allowed implementing and applying 3D models in a commercially available electromagnetic solver to perform S-parameter simulations.

This chapter firstly presents a justification of the bandwidth selected for the S-parameters used through the development of the proposal, as well as the basic processing that allows to verify the correctness of the data. Afterwards, the description of the implementation of 3D models is described to ease the understanding of the results presented in Chapter 4.

3.2. Figures of merit

Return and insertion losses

Regarding the analysis based on S-parameters, the two most important figures-of-merit used in the frequency domain by signal-integrity engineers and academic researchers are the insertion loss (IL) and the return loss (RL) [39]. In fact, IL and RL are straightforwardly defined from the S-parameter set for a two-port network as:

$$IL = |S_{21}| \tag{3.2.1}$$

and

$$RL = |S_{11}| \tag{3.2.2}$$

Since in this work, only symmetrical passive channels are used, the following equations are also valid:

$$IL = |S_{12}| = |S_{21}| \tag{3.2.3}$$

and

$$RL = |S_{11}| = |S_{22}| \tag{3.2.4}$$

Furthermore, in a more explicit way and considering that RL and IL are typically interpreted in dB, these parameters applied on an n-port network are written as:

$$RL = 20\log|\Gamma_{ii}| = 20\log|S_{ii}|, dB \tag{3.2.5}$$

$$IL = 20\log|T_{ji}| = 20\log|S_{ji}|, i \neq j, dB \tag{3.2.6}$$

Rise time and bandwidth

On the other hand, bear in mind that the requirements for a high-speed channel for a given application are provided in data transfer rate, which is closely related to the signal rise time when observing the signal waveform in the time domain. Thus, the following paragraphs are dedicated to define, in practical terms, down to what rise time can be analyzed with transfer functions in the frequency domain (i.e., the S-parameters) described up to 10 GHz. The selection of this maximum frequency is based on the fact that FR4 dielectric laminates employed for constructing standard PCBs for most of current applications become unpractical beyond this frequency. This, however, does not limit the eventual application of the proposal in more advanced materials operating at higher frequencies provided that the corresponding considerations (e.g. lower losses and smaller feature size) are carefully incorporated during the analysis.

Digital signals can be seen as the composition of an infinite number of sinusoidal functions, as demonstrated by Fourier's Theory. Nevertheless, in order to simplify the analysis of digital waveforms, it is often necessary to estimate the frequency content that includes most part of the energy. For this, consider Fig. 3.1. The first harmonic puts a practical bound at the lower limit of its frequency content. However, since the edges contain the highest frequency harmonics, the rise and fall times put a practical upper bound on the spectrum energy envelope. So, the spectrum of a trapezoidal waveform representing current digital signals can be estimated by observing the harmonics of a square wave, eliminating part of the frequency content to produce the correct signal edge. For this, it is interesting to notice that the Fourier series coefficients of a 50 % duty cycle trapezoid take the form of a *sinc* function. In this regard, it is observed that the harmonic amplitude of a square signal will fall-off at 20 dB/dec above the fundamental frequency.

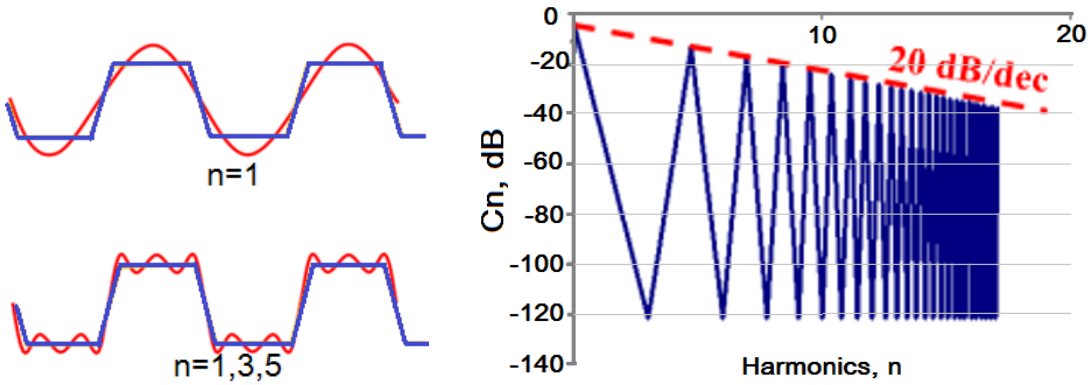

Figure 3.1: Harmonics of a digital signal. Left - Harmonics for a trapezoidal function, where the fist harmonic is related to the period and the last related to the limits imposed by rise/fall times. Right - Envelope of the harmonics for a sinc function.

To estimate the spectrum of a trapezoidal wave that reassembles a digital waveform, the harmonics corresponding to a square wave must be filtered to produce the correct rise and fall times. This can be done considering a step response to an infinite input edge rate of a first-order system, with the output filtered by a time constant τ, as shown in eq. (3.2.7). The time constant required to degrade a step to a specified 10-90 % rise time, is calculated by eq. (3.2.8)

$$V = V_{\text{input}}(1 - e^{-t/\tau}) \tag{3.2.7}$$

$$t_{\text{10-90\,\%}} = t_{\text{90\,\%}} - t_{\text{10\,\%}} = 2.3\tau - 0.105\tau = 2.195\tau \longrightarrow \tau = \frac{t_{\text{10-90\,\%}}}{2.195} \tag{3.2.8}$$

On the other hand, the frequency response of a one-pole network with a time constant of τ is given by eq. (3.2.9). Observe that the magnitude also falls off with $1/f$, or 20 dB/dec, as shown in eq. (3.2.10). So, substituting τ into the frequency response produces (3.2.11).

$$F_{\text{3dB}} = \frac{1}{2\pi\tau} \tag{3.2.9}$$

$$\tau = \frac{1}{2\pi F_{\text{3dB}}} \tag{3.2.10}$$

$$t_{\text{10-90\,\%}} = \frac{1.09}{\pi F_{\text{F3dB}}} = \frac{0.35}{F_{\text{3dB}}} \tag{3.2.11}$$

As it can be seen, in order to reconstruct a digital signal with specified rise and fall

times, harmonics as high as f_{3dB} must be included in the analysis. The amplitude of higher harmonics will fall-off at -40 dB/dec above this frequency with the presented approach.

3.3. S-parameters and TDR analysis

In order to verify the usefulness of the experimental S-parameters available for developing this project, it is important to establish a way to check their correctness. For this purpose, time-domain-reflectometry (TDR) curves can be obtained from the S-parameters using inverse Fourier Transform theory. In what follows, some basic theory to interpret the obtained data to describe what is expected to observe after processing the S-parameters of a prototyped channel is presented. In Chapter 4, Keysigth's Advance Design System (ADS) simulation software is used to apply this theory to the experimental data.

The TDR data of a uniform, perfectly matched channel looks as shown in Fig. 3.2. Nevertheless, when an unmatched termination is presented at the end of the line, the result illustrated in Fig. 3.3 is obtained. Notice in the latter case that the discontinuity is introduced by an unmatched real impedance. Nonetheless, even in this case, the length of the uniform interconnection can be calculated from the TDR data by considering that the delay time is half the time that takes the signal to travel to the load and go back to the source. Therefore, if a transmission line is prototyped presenting an unmatched real termination, it is clear that correct S-parameter data would allow to obtain TDR curves exhibiting the expected delay time which is inferred from the physical length of the line. In case that the measurements include additional effects (for instance pad or connector parasitics not appropriately de-embedded), these effects will be observed in the measurements and, depending on the magnitude of the discontinuities observed in the TDR data, a decision can be taken about the correctness of the S-parameters.

Now, for experimentally analyzing the particular cases of interest in this work, vias introducing capacitive and inductive effects are prototyped. Thus, the associated TDR data will evidence discontinuities when via transitions occur. Notice in Fig. 3.3 how discontinuities due do capacitive, inductive, and capacitive-inductive effects look

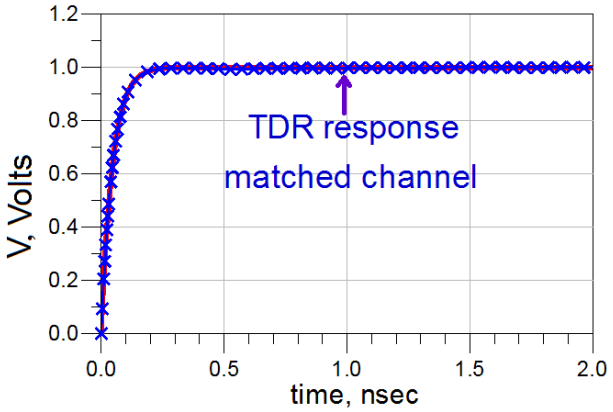

Figure 3.2: TDR data of a perfectly coupled channel.

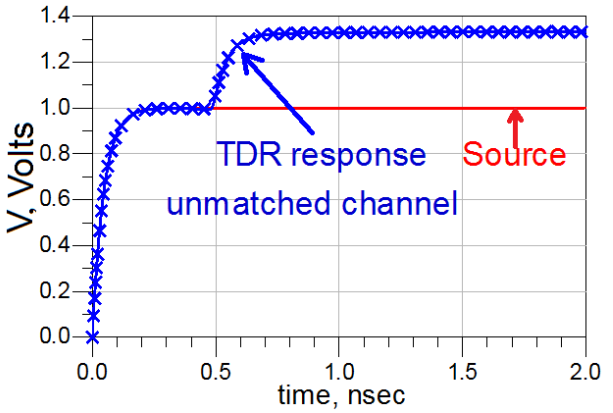

Figure 3.3: TDR data of a channel presenting an unmatched termination at the load. The illustrated case corresponds to a termination resistor whose value is twice that of the channel characteristic impedance value.

like in TDR curves. In Chapter 4, these concepts will be revisited when processing the experimental data.

3.4. Full-wave simulations. Methods and requirements

The solution to several electromagnetic problems found in current devices is not analytically calculable. In addition, analytical solutions in closed form are known for only a very limited number of special cases, which are hardly directly applicable to real-world applications. These problems are commonly caused by the multitude of

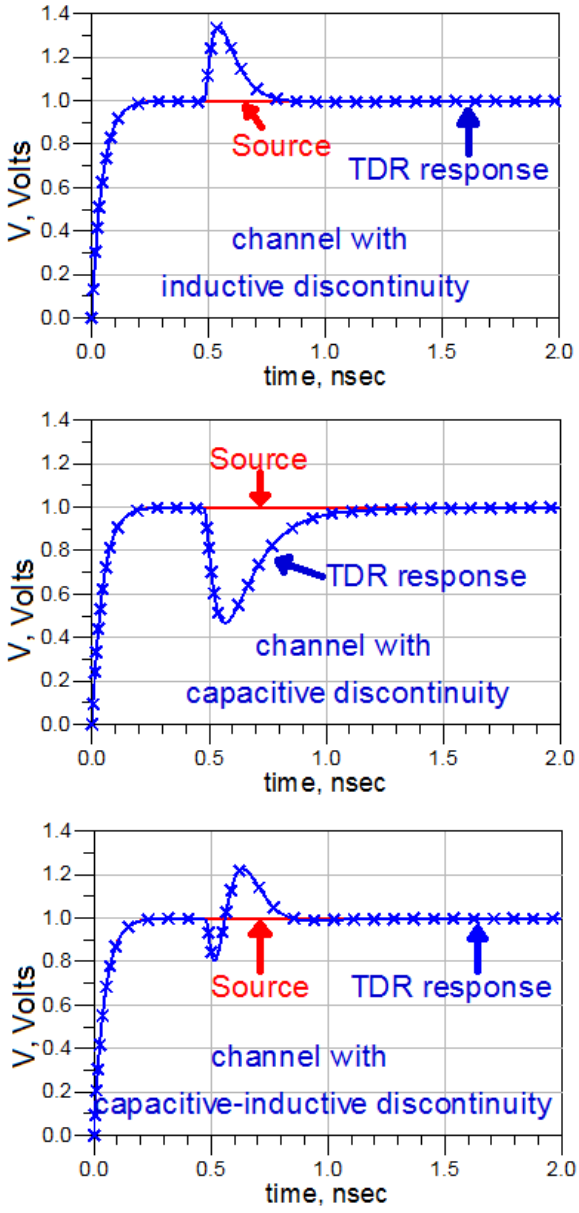

Figure 3.4: TDR data of channels with discontinuities. Top - Channel with inductive discontinuity. Center - Channel with capacitive discontinuity. Bottom - Channel with capacitive-inductive discontinuity. In general, for a capacitive discontinuity there will be a valley in the response. For an inductive discontinuity there will exist a crest (a peak) in the response.

irregularities in the geometry of the structures and materials, and the frequency-dependent behavior of material properties. The advent of powerful computational devices and their application to numerical techniques can overcome these issues. Actually, these tools provide important information and understanding relative to the operation of electromagnetic devices, which can be difficult to be obtained through

analytical calculations and measurements. In this regard, current commercial tools can provide results based on popular algorithms. However, in many cases a correct understanding of the structure is required on the part of the user to select the most reliable solution method. Furthermore, depending on the case, modifications must be performed on problems that extend beyond the capabilities of the software used [44].

Among the most popular numerical methods are the Finite Element Method (FEM), the Finite-Difference Time-Domain (FTDT) method, and the Method of Moments (MoM). Although all of them derive closed form solutions of Maxwell's equations under various constitutive relations of media and boundary conditions, there are important differences between them.

FEM is commonly used to find approximate solutions of partial differential and integral equations. It subdivides a large problem into smaller and simpler parts, called finite elements. This has the advantage of a more accurate representation of complex geometries, as well as the capture of local effects, and the inclusion of dissimilar material properties. In general, this is the most accurate method, but also the most time consuming.

FTDT is faster and easier to understand. Since it is a time-domain method, solutions can cover a wide frequency range, provided that the time step satisfies the Nyquist-Shannon sampling theorem. The derivatives respect to space and time are approximated by finite differences, typically formulated on a structured Cartesian grid. Nevertheless, the main weaknesses are related to boundaries that are not aligned with this Cartesian grid and limitations inherent to the time step. This method is generally used for geometries where the wavelength is comparable to the size of the structure.

MoM primarily uses, instead of the differential form of Maxwell's equations, their integral form. Conceptually, it works by constructing a mesh over the modeled surface. This can be easily applied to problems for which Green's functions can be calculated. In general, Green's function represents the electric potential produced by a unit charge point [45]. This condition is easy to be found for problems with a small surface-to-volume ratio. However, in general it is a less-efficient method compared to volume-discretization methods, like FEM.

Due to the accuracy presented by the method and its ability to deal with complex geometries, in the present work the simulations are performed with FEM analysis.

As mentioned, with FEM the problem is partitioned in smaller parts, or subdomains. Then, the field-solution can be expressed in terms of a low-order polynomial on each of these subdomains. Hence, a piecewise low-order polynomial representation of the fields is obtained for the entire domain. With this approach, to obtain an exact solution, the size of the subdomains should tend to zero, and the number of them tends to infinite. However, different approaches relax these requirements, attempting to find a field solution that fulfills the differential equation and its boundary conditions [44].

The ability to deal with complex geometries with FEM, is achieved by using unstructured grids, or meshes. These typically consist of triangles in two-dimensions and tetrahedra in three-dimensions. However, there are triangles and quadrilateral shapes for elements in two dimensions, and tetrahedra, prisms, pyramids, and hexahedra in three dimensions. This is shown in Fig. 3.5. This way to perform meshes used in FEM, allows for good representations for curved objects, like those involved in typical via structures. Moreover, these allow higher local resolution for fine structures and rapid variations of the solution to get better accuracy. In addition, it makes it possible to analyze properties concerning to stability and convergence.

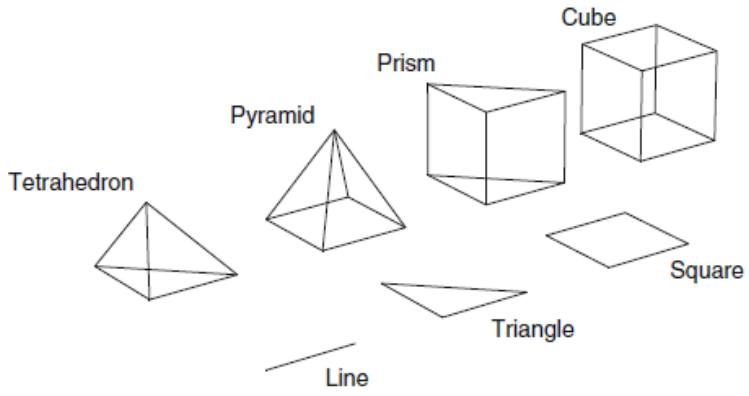

Figure 3.5: Geometries in FEM analysis. Different element shapes used [44].

Another important aspect for obtaining correct full-wave simulations is related to frequency. A correct selection of bandwidth, and an adequate frequency sweep, are required in order to get correct descriptions about the frequency behavior of the

structure with low computational-time. In this respect, some tools provide options to select between generating unique solutions for each point selected in frequency, in different ranges of frequencies, and even interpolation options optimized for smooth responses and low computational resources.

3.5. Analysis of single and coupled vias

In the previous chapter, different approximations and analyses for the electrical behavior of vias were discussed. In the present section, some considerations allowing to understand certain characteristics for capacitance relations in vias are explained.

3.5.1. Single via

Consider the electrical field associated with a via, as shown in Fig. 3.6. In this, a strong radial component spreading outside the barrel and pads in direction to the ground layers is observed. However, there is also a strong E_z field component accounting for the separation of planes and the nonexistence of coplanarity between pads and ground layers. It is also important to observe the contribution of the fringe-fields due to the barrel and the utmost pad.

It must be mentioned that for a correct characterization of the electrical behavior of the entire via, the analysis should be divided for the separated effects of the barrel and pads, so that:

$$C_{via} = C_{barrel} + C_{pads} \tag{3.5.1}$$

In the case of the barrel capacitance, the structure can be approximated by a cylindrical capacitor, for which there exists a well-known expression easily obtained by Gauss' law [46-47], applied in this case as eq. (3.5.2),

$$C_{\text{barrel}} = \frac{2\pi\epsilon_0\epsilon_r h_{\text{barrel}}}{\ln(D_{\text{antipad}}/D_{\text{barrel}})}, \tag{3.5.2}$$

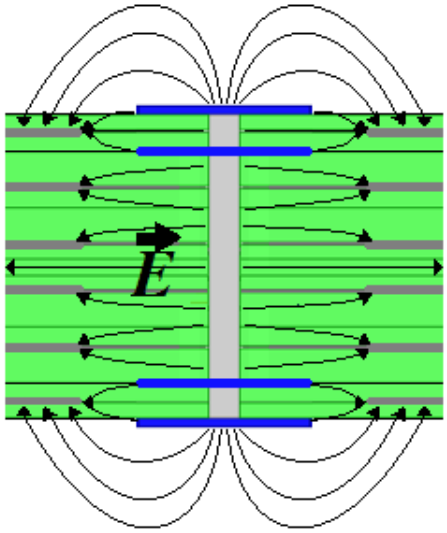

Figure 3.6: Depiction of the electic field in a single via.

where
C_{barrel} = Capacitance of the barrel approximated as a cilinder, pF (picoFarads)
ϵ_0 = Permittivity of free space, $2.249x10^{-4}$, pF/mil
ϵ_r = Relative permittivity of dielectric
D_{barrel} = Diameter of the barrel, mil
$D_{antipad}$ = Diameter of the antipad, mil
h_{barrel} = Height of the barrel, mil

With a similar expression, an approximation of the entire via capacitance could be described if there were pads in all of the layers, using the term D_{pad} instead of D_{barrel}. With this in mind, in order to explain the referenced equation for the via capacitance in the Chapter 2, it is worth writting the Taylor series for the natural logarithm of $(x+1)$,

$$\ln(x+1) = x - \frac{x^2}{2} + \frac{x^3}{3} + ... + (-1)^{n+1}\frac{x^n}{n} \tag{3.5.3}$$

For the case where $x+1 = D_{antipad}/D_{pad}$, it is observed that the first term in the series is $x = (D_{antipad} - D_{pad})/D_{pad}$. This result, applied instead the natural logarithm in the cylindrical capacitor eq. (3.5.2), gives the aforementioned eq. (2.5.1). As a result, this analysis serves as a corroboration for the present proposal based on

well-known references.

With the purpose of adding the contribution of fringing-fields outside the structure, it will be assumed that these are proportional to the barrel capacitance. Since, in general, the fields are immersed into different material permittivities (air or free space, and dielectric), the values obtained for this contribution will be dependent on their specific selection of materials. The general expression for this case is provided by eq. (3.5.4),

$$C_{\text{barrel}} = \frac{2\pi K_b \epsilon_0 \epsilon_r h_{\text{barrel}}}{\ln(D_{\text{antipad}}/D_{\text{barrel}})}, \tag{3.5.4}$$

where K_b represents the contributions due to the cylinder approximation (expected to be ≈ 1), plus the fringe fields contribution.

In consideration of the pad capacitance, although the fields are not exactly similar to the cylinder case, the same trend for the fields is observed. Actually, this is one of the approaches mentioned in [37]. As a corroboration, the following lines are dedicated to develop the equations considered to have a better understanding of the phenomena.

First, consider the Fig. 3.7. A finite linear distribution of uniform charge λ is represented. This serves to calculate the approximated form of the electric field due to the pad, with its total charge concentrated along the z axis. An element of charge dQ located on a point of that distribution is observed to produce an electric field $d\vec{E}$ over a point on the xy plane. This $d\vec{E}$ can be calculated by eq. (3.5.5),

$$d\vec{E} = \frac{\lambda dz}{4\pi\epsilon_0\epsilon_r|\vec{r}|^2}\hat{r} = \frac{\lambda\xi\sec^2\theta d\theta}{4\pi\epsilon_0\epsilon_r(\xi\sec\theta)^2}(\cos\,\theta\hat{r} - \sin\theta\hat{k}). \tag{3.5.5}$$

The electric field produced by the total charge distribution is obtained trough the integration of eq. (3.5.5) in the form of eq. (3.5.6),

$$\vec{E} = \frac{\lambda}{4\pi\epsilon_0\epsilon_r y_1}[\sin\theta\hat{r} - \cos\,\theta\hat{k}]_{\theta_2}^{\theta_1}. \tag{3.5.6}$$

This provides an approximation for the form of the electric field due to the pad on one of the reference layers (with a distance equal to $R_{antipad}$), as shown in Fig. 3.8.

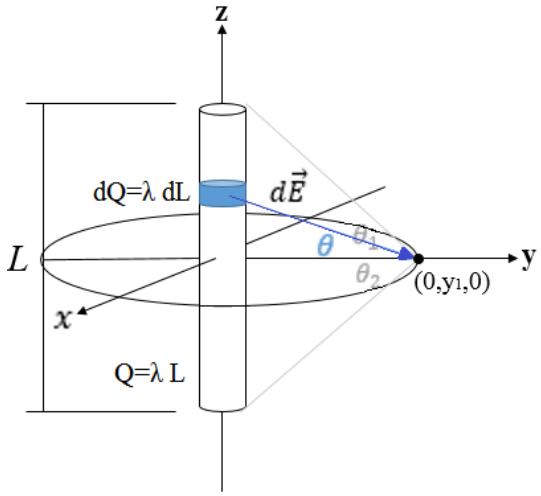

Figure 3.7: Uniform distribution of a linearly distributed charge to approximately calculate the electric field of a cylindrical capacitor.

Bearing this in mind, the capacitance can be calculated, when previously obtaining the electrostatic potential and the total charge, as shown by eq. (3.5.7) and eq. (3.5.8),

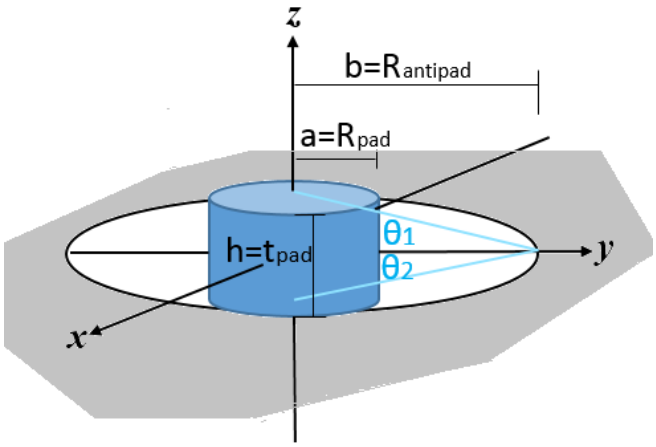

Figure 3.8: Pad and antipad geometries to calculate capacitance of the pad.

$$V = -\int_b^a \vec{E}\cdot d\vec{l} = -\int_b^a \vec{E}\cdot d\vec{r} = -\int_b^a \frac{\lambda}{4\pi\epsilon_0\epsilon_r r}[\sin\theta\hat{r}]_{\theta_2}^{\theta_1} dr = \frac{\lambda \ln(b/a)[\sin\theta]_{\theta_2}^{\theta_1}}{4\pi\epsilon_0\epsilon_r} \tag{3.5.7}$$

$$Q = \lambda L = \lambda t_{pad} \tag{3.5.8}$$

So, if $\theta_1 = \theta_2$, which is the case for coplanar pads and antipads, the capacitance is given by eq. (3.5.9)

$$C_{pad} = \frac{Q}{V} = \frac{2\pi\epsilon_0\epsilon_r t_{pad}}{\ln(D_{antipad}/D_{pad})} \approx \frac{2\pi\epsilon_0\epsilon_r t_{pad} D_{pad}}{D_{antipad} - D_{pad}} \tag{3.5.9}$$

However, it is noticed that, for situations where pads and the nearest ground layer are not coplanar, the dielectric thickness between these two must be considered. The expression obtained in this case is given by eq. (3.5.10)

$$C_{\text{pad}} = \frac{Q}{V} = \frac{2\pi\epsilon_0\epsilon_r t_{pad}}{\ln(D_{effective}/D_{pad})} \approx \frac{2\pi K_p\epsilon_0\epsilon_r t_{\text{pad}}}{\ln(\sqrt{D^2_{\text{antipad}} + T^2_D}/D_{\text{pad}})} \approx \frac{2\pi K_p\epsilon_0\epsilon_r t_{\text{pad}} D_{\text{pad}}}{\sqrt{D^2_{\text{antipad}} + T^2_D} - D_{\text{pad}}}, \tag{3.5.10}$$

where T_D represents the dielectric thickness previously mentioned, t_{pad} the pad thickness, and K_p a constant of proportionality which includes the effect of fringing-fields, as before. In addition, it is of great importance to observe that the total capacitance of each pad will be increased by the number of closest ground layers conforming the antipad, so that the previous calculation could be performed for each one, as shown by eq. (3.5.11).

$$C_{\text{pad total}} \approx \sum_{k=1}^{n} \frac{2\pi K_p\epsilon_0\epsilon_r t_{\text{pad}}}{\ln(\sqrt{D^2_{\text{antipad}} + T^2_{D,k}}/D_{\text{pad}})} \approx \sum_{k=1}^{n} \frac{2\pi K_p\epsilon_0\epsilon_r t_{\text{pad}} D_{\text{pad}}}{\sqrt{D^2_{\text{antipad}} + T^2_{D,k}} - D_{\text{pad}}}, \tag{3.5.11}$$

where n is the number of closest layers.

3.5.2. Coupled vias

To calculate mutual capacitance, the geometries can be modeled as a two-wire transmission line. In order to do this, the equations given in [48] were considered. Thus the proposed formulation is given by eq. (3.5.12). In this one, K_m is a constant representing variations in the structure and materials, as before.

$$C_{\text{mutual}} = \frac{K_m h_{\text{barrel/pad}} \pi \epsilon_0 \epsilon_r}{acosh(d_{\text{barrel to barrel}}/D_{\text{barrel/pad}})} \tag{3.5.12}$$

Here, $D_{barrel/pad}$ and $h_{barrel/pad}$ are related to the diameter and heights (thicknesses) of either the barrel or pads, and $d_{\text{barrel to barrel}}$ is the distance between the center of each structure.

3.6. Conclusions of the chapter

Appropriately complementing frequency with time domain analyses is necessary to get accurate results when modeling sections of interconnection channels. In this regard, it is necessary to bear in mind that the bandwidth of the transfer functions defined by the S-parameters and the minimum rise time associated with a digital signal are closely related. Thus, considering this fact is extremely important to obtain consistent and useful results.

In this chapter, it was also presented an overview of the aspects to be taken into account when performing 3D modeling of an interconnection structure consisting of different sections. In particular, selecting the meshing of a via in an adequate fashion will allow to perform effective simulations.

Finally, an overview of the Electromagnetic Theory basics to be used when developing a physically-based model for a via was presented. This allows to introduce the details of the proposal presented in the following chapter.

Chapter 4

Experimental results and validation

4.1. Introduction

The purpose of this chapter is describing the development of the methodology for modeling and characterizing via transitions in PCB technology. Particularly, the methodology is used for analyzing the impact of changing the diameter of the via pad on the performance of a channel implemented in a multilayer board. This case is of particular importance in the design of PCB links since it is one of the parameters to optimize when minimizing reflections and matching transitions between interconnects at different layers. Bear in mind, however, that the methodology, including the model development and parameter extraction procedure, can be applied to other cases such as interconnection bends, terminations, changes in interconnection width, etc. For reference, a synthesized description of the steps followed to carry out the modeling and characterization of the via transition in this project is shown in Fig. 4.1.

Full-wave simulations are performed in this work to ease the determination of the S-parameters associated with the via transition. Thus, based on information related to geometrical descriptions and measurements of coupled channels, calibrated 3-D models are obtained. With these, appropriate segmentations are performed to ensure quality in the extraction of the via model parameters. Then, a circuit-equivalent extraction is associated with each segment. For the model elements, the corresponding values are firstly obtained through the application of the expressions developed in

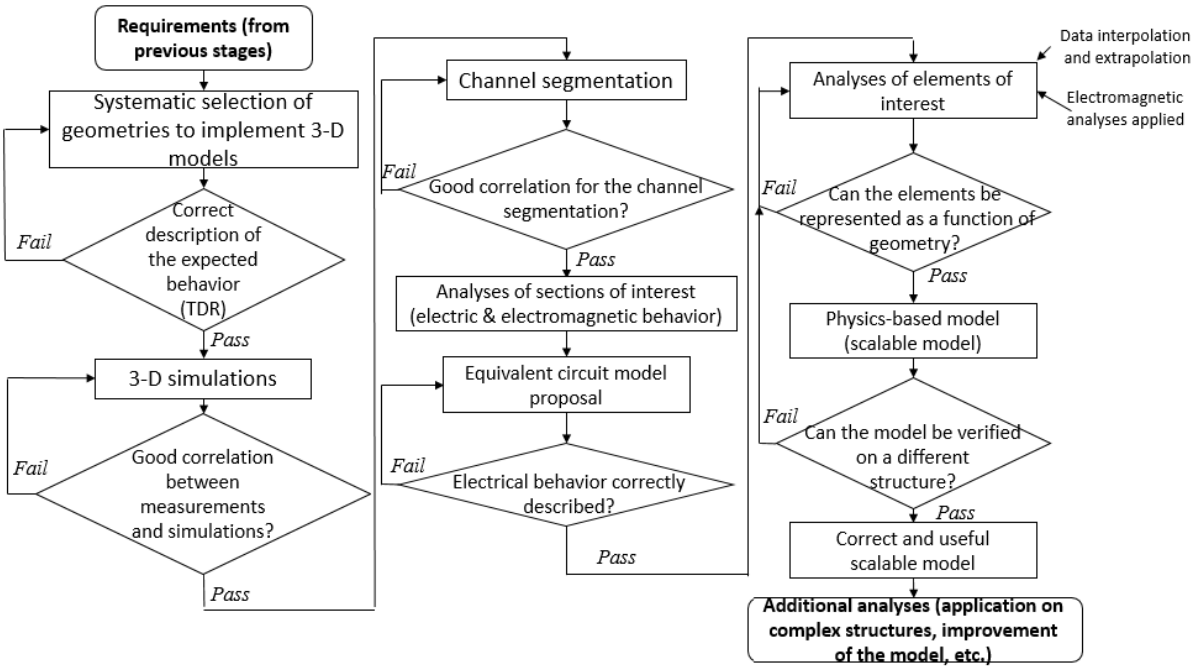

Figure 4.1: Flowchart describing the steps followed to carry out the modeling and characterization of the via transition in this project.

the previous chapter. Nevertheless, these expression were improved here to take into consideration additional effects that allow to represent the via transition with higher accuracy.

The methodology is validated through the model-experiment correlation of data associated with a channel whose geometry differs from the one corresponding to the channel employed during the parameter extraction process. It is worthy to mention that the variations in geometry as described here are related to the size of the structures (diameter of circular pads in vias), but the form (e.g., circular pads) is maintained in all cases.

4.2. Description of prototypes

For the present work, the information related to coupled channels was provided by Intel based on a test board. The information was provided in the form of a $*.brd$ file with the layout and stackup of the board, as well as S-parameter files with the

measurements performed on prototypes.

The PCB consists of 14 metallic and 13 dielectric layers symmetrically arranged with a total thickness of 77.4 mils. Going from top (layer 1) to bottom, metallic layers 2, 4, 6, 9, 11, and 13 are destined to serve as AC reference planes (either ground or DC power), while the others act as layers where signal traces will be formed. The dielectric layers consist of FR-4 laminates of different thickness and permittivity. All dielectric layers present a nominal loss tangent of 0.035 (provided by the PCB manufacturer), falling into the range of high-loss materials for PCBs.

For this project, four structures included within the prototype were selected to develop the proposal. All these structures, which complied with the requirements for the analyses. Three of the channels were selected for the electrical extraction and processing, while the remaining fourth was considered for final validation of the methodology. One of the structures analyzed is shown in Fig. 4.2. For the microstrip and stripline traces located on metallic layers, 1 and 3 respectively, the same width and pitch (center-to-center separation) are used. With this, the coupled lines are expected to have a differential characteristic impedance of 100 ohm ±10 %. The only variation between the analyzed cases was for the pad diameter. In this regard, sizes of 0.46, 0.76, and 1.07 mm (18, 30, and 42 mils, respectively) were observed. In addition, there is information about the dimension of pads and antipads at the level dedicated to signal traces.

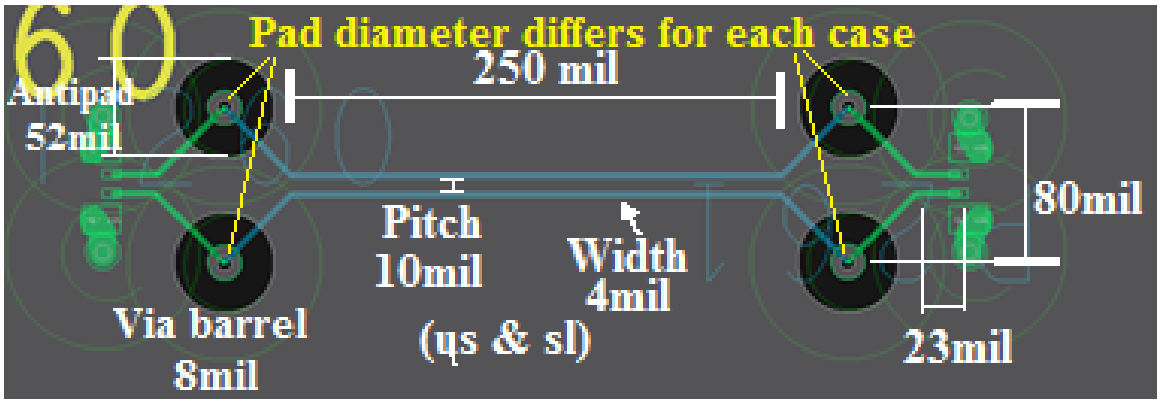

Figure 4.2: Layout of one of the prototyped channels provided by Intel. The indicated dimensions, with exception of the pad size, remain the same for all the channels used in this work.

4.3. TDR analysis

As explained in Chapter 3, TDR curves obtained from frequency-to-time domain conversions can be inspected to verify that the S-parameters correspond to what is expected from measurements performed to channels as the prototyped ones. For this reason, the ADS circuit simulator is used in what follows to check for the correctness of the S-parameter measurements available in this project.

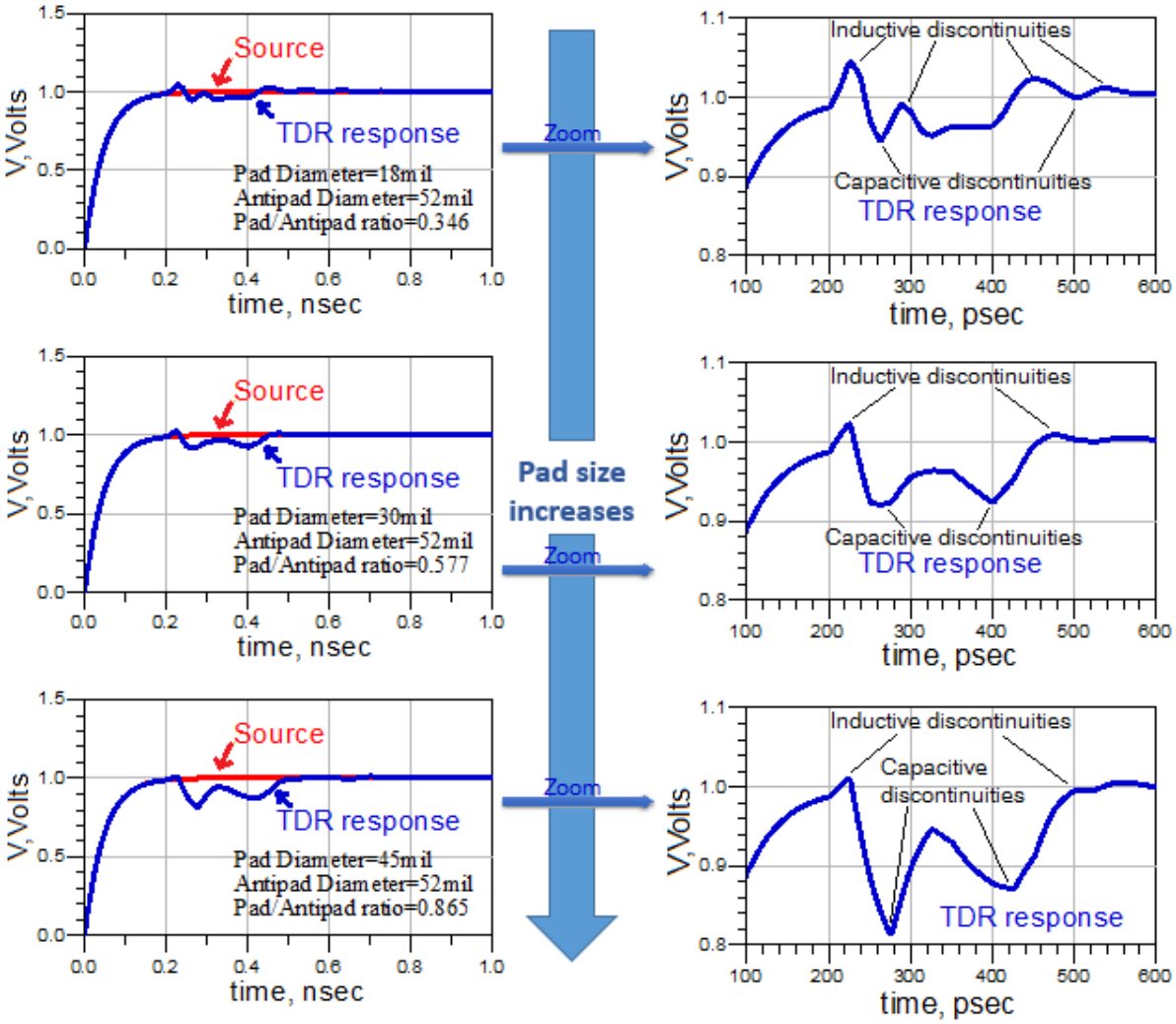

Figure 4.3: TDR curves obtained from frequency-to-time domain conversions of the analyzed measurements. Observe the presence of peaks and valleys in the responses, which denote the presence of inductive and capacitive discontinuities, respectively.

The curves corresponding to the measurements performed on the three prototyped

channels are shown in Fig. 4.3. Notice the presence of peaks and valleys in the responses, which denote the existence of inductive and capacitive discontinuities along the channel, as described in Chapter 3. Furthermore, it is observed the impact of the valleys to be stronger as the result of longer pad diameters, describing the presence of bigger capacitance values in the discontinuities, i.e. vias. In contrast, the magnitude of the inductive peaks increases as the pad diameter is reduced. This is expected due to longer portion of trace present on the antipad zone, for which the main effect is inductive. In this regard, this TDR qualitative analysis strongly suggests that the measurements provide realistic information of the effects occurring within the prototyped channels.

4.4. Calibration of the 3-D model

4.4.1. Model-experiment correlation

Once certain criteria related to geometry, material properties, and accuracy needed for the simulations are established, FEM was selected as the solution method used by the EM solver. After that, parametric variations of geometry were performed to get model-experiment correlation for the prototyped channels. Fig. 4.4 illustrates the corresponding common-mode and differential-mode responses compared to measurements. In addition, time domain curves are shown in this figure . In the latter case, the results were obtained by considering a step function with rising edge of $0.035ns$, covering the bandwidth of the data $(0 - 10GHz)$ based on the expressions shown in Chapter 3.

Must be noticed that, in the analyzed cases, the via connecting the microstrip and stripline is very short compared with the total length of the plated through hole that goes from the top to the bottom of the PCB. In fact, the extension of the via that goes from the stripline level to the bottom part of the PCB can be considered as a stub that introduces parasitic effects. Moreover, due to the fabrication process two unused pads are also included at the bottom layers of the via structure (i.e. symmetrically placed with respect to the pads used for the microstrip and stripline). The effect introduced by these pads is seen as an increase of the capacitance of the via stubs.

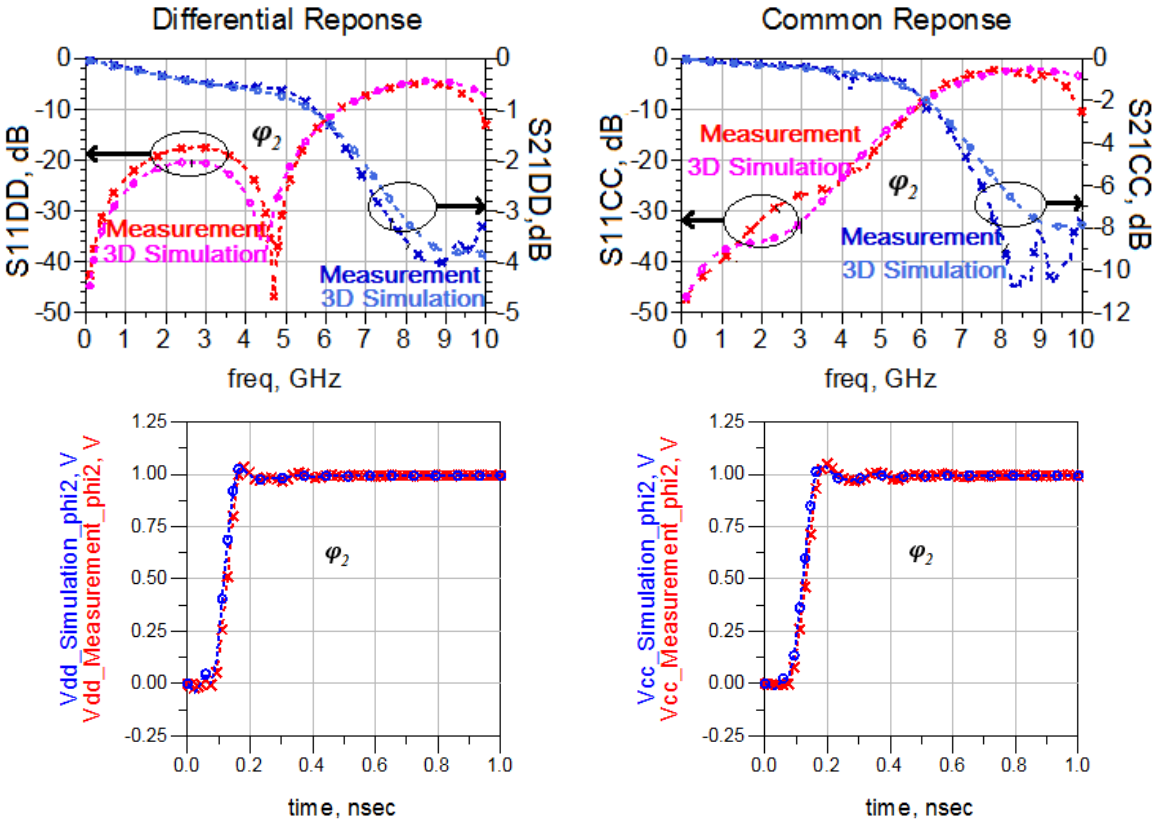

Figure 4.4: Differential and common mode responses of the channel. Top - Responses in the frequency domain. Bottom - Responses in the time domain.

Even these effects are considered not only when implementing the 3D model but also when developing the equivalent circuit representations described later in this chapter.

By comparing measured and simulated curves, it is worthwhile mentioning that excellent correlation was achieved, better than the one obtained in similar works reporting on differential links [20],[32]. It is important, however, to remark the fact that no figures of merit to assess the correlation were made here. Nevertheless, it is observed in the curves that the percentage variation of the simulated against the measured curves is minimum. Now, according to some authors, the existence of the resonance near 4.7 GHz in a channel like the one considered here is due to stub effects [20]. In the case of the common-mode propagation, there is a relatively higher difference between experimental and simulated data associated with the transmission near 9 GHz. This is attributed to problems with the calibration of measurement, issues with the return paths (i. e. ground vias location), as well as non-ideal effects, described in Chapter 2.

In order to verify that the modeling of the differential and common mode signal propagation is correct for the considered channels, extractions of the cross-mode conversions were also performed. As can be seen in Fig. 4.5, the mode conversion when considering measurements and simulations is lower than -25 dB within the bandwidth of interest. In this regard, cross modes are negligible. Thus, after carefully incorporating the detailed geometry of the prototyped channels and comparing measured with simulated data, the implemented 3D models are considered as well-calibrated and the simulations can be used with confidence for the purposes of this project.

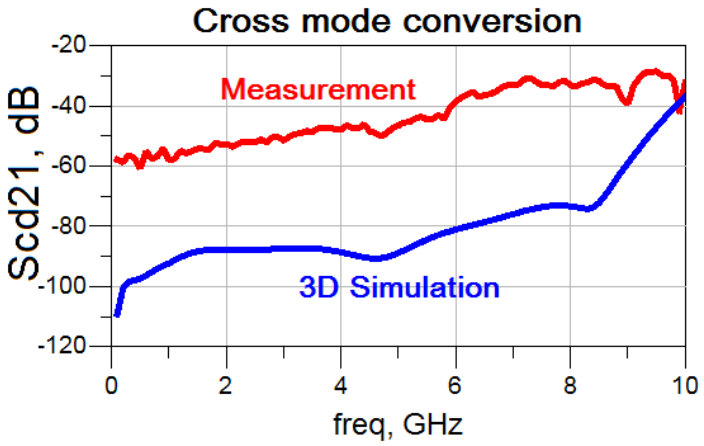

Figure 4.5: Mode conversion in the channel. A magnitude of conversions lower than -25dB is observed, which is negligible compared to the differential and common responses.

Once the model was calibrated, the next step is segmenting the channel into well-defined parts, as depicted in Fig. 4.6. This allows for the analysis of the section of interest. In the present case, the main interest is focused on the vias.

At this point, it is important to perform a new simulation of the channel but considering it as a multi-section interconnect. In this way, the responses of each section were assembled to compare their response to the first full-channel simulation. This was done to corroborate a correct partition of the channel, avoiding the presence of discontinuities, evanescent-modes or other undesired effects introduced by the simulator at the ports. Otherwise, further analyses or different segmentation methods have to be performed. In the present work many analyses for a correct segmentation were tested, and good correlations were finally obtained; this is verified in Fig. 4.7 and Fig. 4.8. Then, the responses for the sections of interest was compared.

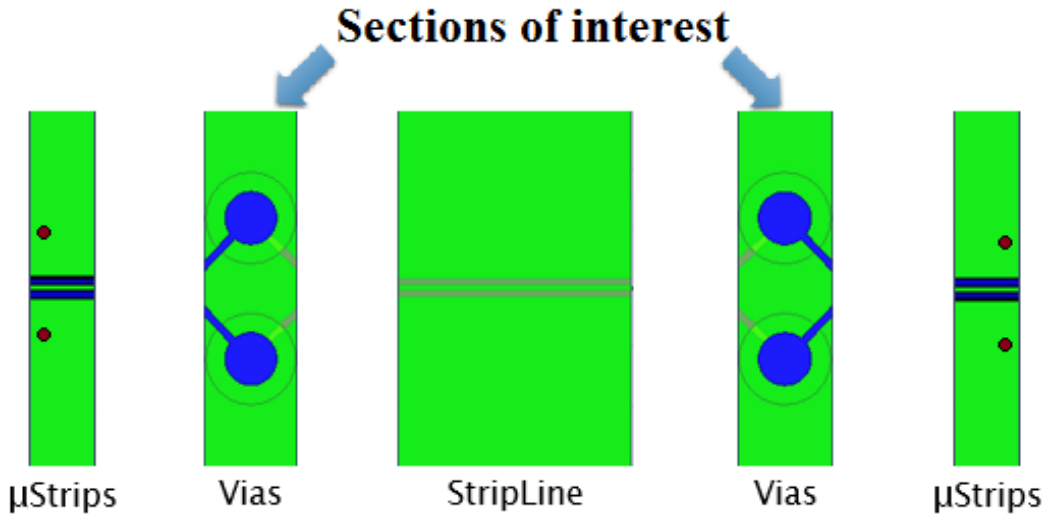

Figure 4.6: Segmentation of the channel.

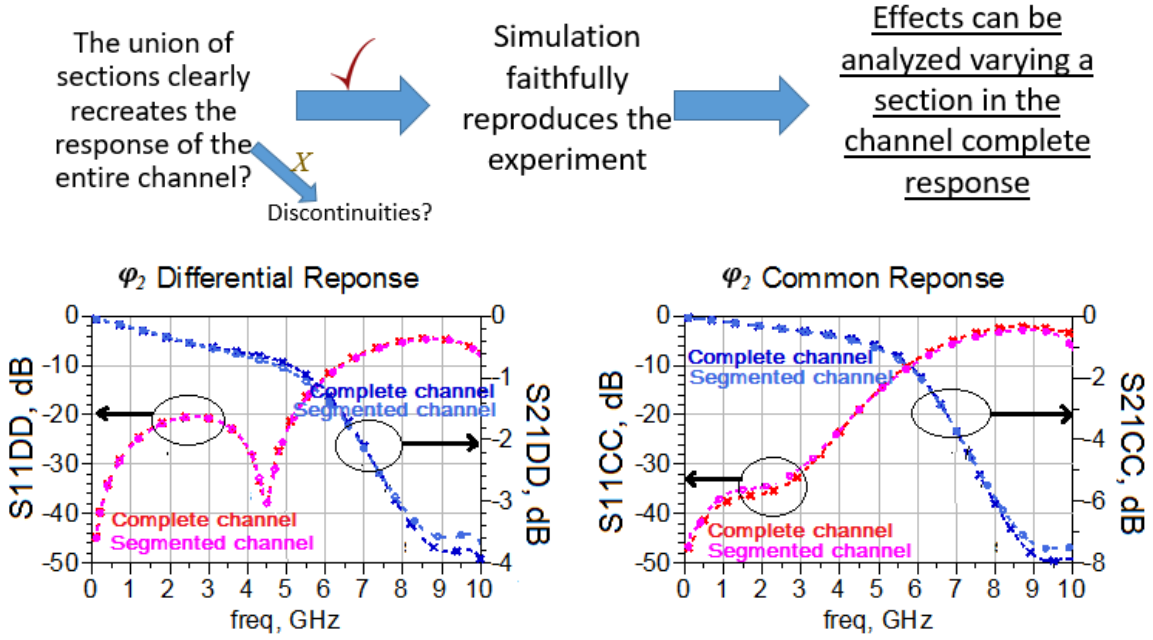

Figure 4.7: Validation of the channel partition. Top: If the response of the concatenation of sections correlates well to the complete-channel simulation, one can be sure that the part of interest is well represented by its simulated section; so, a further analysis can be done. Bottom: Responses of the channel under study, with pad diameter $\phi_2 = 30mil$. There is no significant variation between simulations, so each part reproduces faithfully its effect within the channel.

4.4.2. Correlated cases - sections of interest

In the prototyped cases, there is variation only in the pad diameter. The variation occurs in both transmission layers and via stubs (i.e. when the via passes through AC

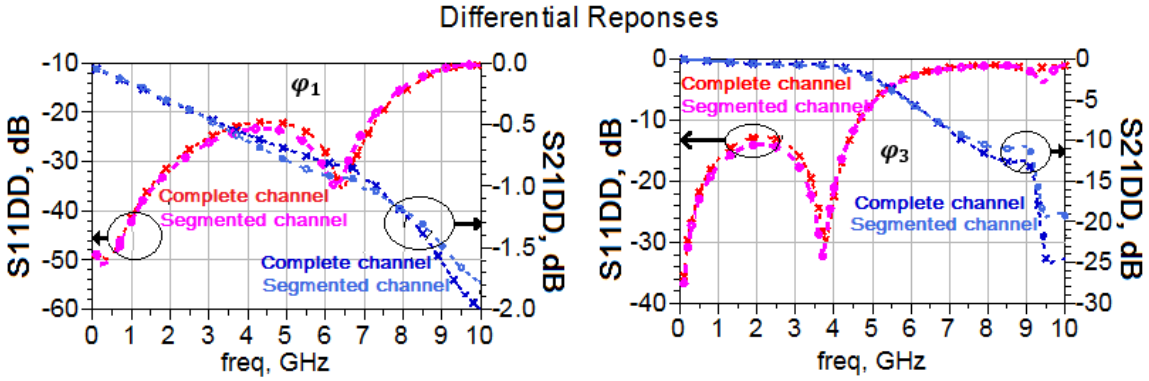

Figure 4.8: Correlation for the studied channels. For each case in which the pad diameter varies, $\phi_1 = 18mil$ and $\phi_3 = 42mil$, good correlations were obtained; so, it is possible to analyze the contributions of the vias to the channel.

ground planes). Thus, in the electrical characteristics of the channel, the variation is manifested as change in the effective capacitance and inductance of the via.

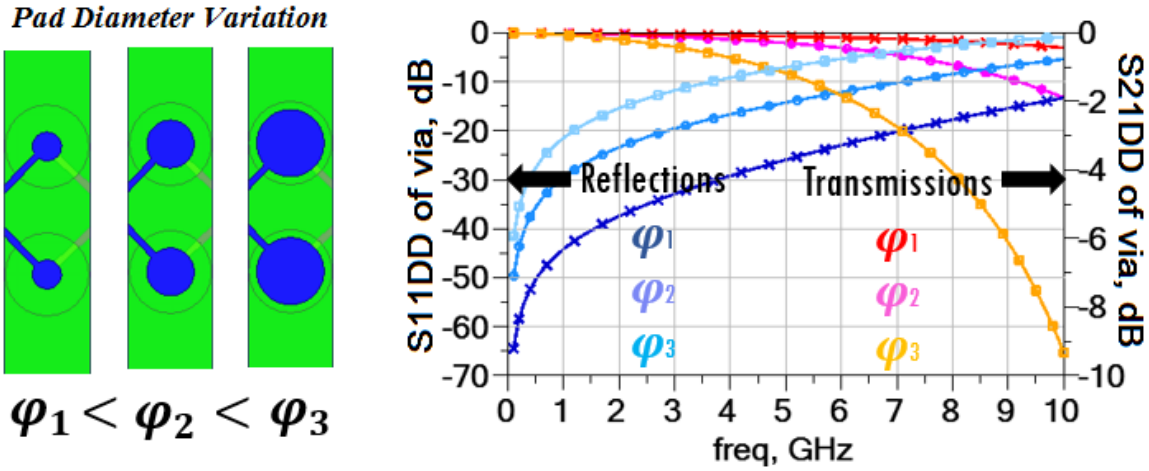

Figure 4.9: Effect of the via pad variation on the reflection and transmission response. Increased mismatch and higher insertion loss is observed as the pad diameter increases. Although only responses for differential mode signaling are shown, the responses are similar for common mode propagation.

Fig. 4.9 shows the physically expected variation in the propagation of signals as a function of both pad diameter and frequency. An approach for accounting for this dependence on frequency is explained in using the equivalent complex characteristic impedance of a the via [49]. In fact, its electrical behavior is related to an array of inductive and capacitive effects, both for the barrel in the transition and for the stub. The latter represents the most problematic effect due to its inherent behavior as a discontinuity.

4.5. Equivalent circuit model

4.5.1. Topological description

Once the correct representation of the electromagnetic behavior of the different channel sections is achieved, a description of the electrical characteristics of the structure by using lumped components is proposed. Fig. 4.10 shows the simulated structure considered for a pair of coupled vias as well as a distributed equivalent circuit that represents its electrical behavior. This includes coupling effects and losses. At low frequencies, the effect of the stubs is well-represented by means of single capacitances. Thus, within the range of frequencies of interest in this project, the barrel inductive effect must also be taken into account in the modeling. In addition, the inductance of the via traces is considered.

4.5.2. Parameter extraction methodology

Notice that the complexity of an equivalent model accounting for all the physical effects and the corresponding distributed nature is considerable. Thus, the model parameter extraction may become very difficult or yield unrealistic values when using traditional optimization extraction techniques. However, certain methodologies can be carried out to simplify the analyses that allow for the extraction of the parameters. Firstly, due to the symmetry of the structure, the analysis of responses in common and differential signaling is simpler than that related to directly using four-port single-ended S-parameters. Thus, the 4-port model is well described by two 2-port models, for which the differences in the responses are attributed to mutual capacitive and inductive effects. These are easily de-embedded making use of equations like those presented in [50]. An additional simplification was performed: based on the bandwidth of the responses and size of the structures, the electrical impact of specific zones in the vias is not strong enough to considerably affect the measurements. In this case, a model can be implemented with a few electrical components. The reduced model for analysis is shown in Fig. 4.11, where the subscript mm in the name of the components represents the signaling mode in each case, differential, dd, or common, cc.

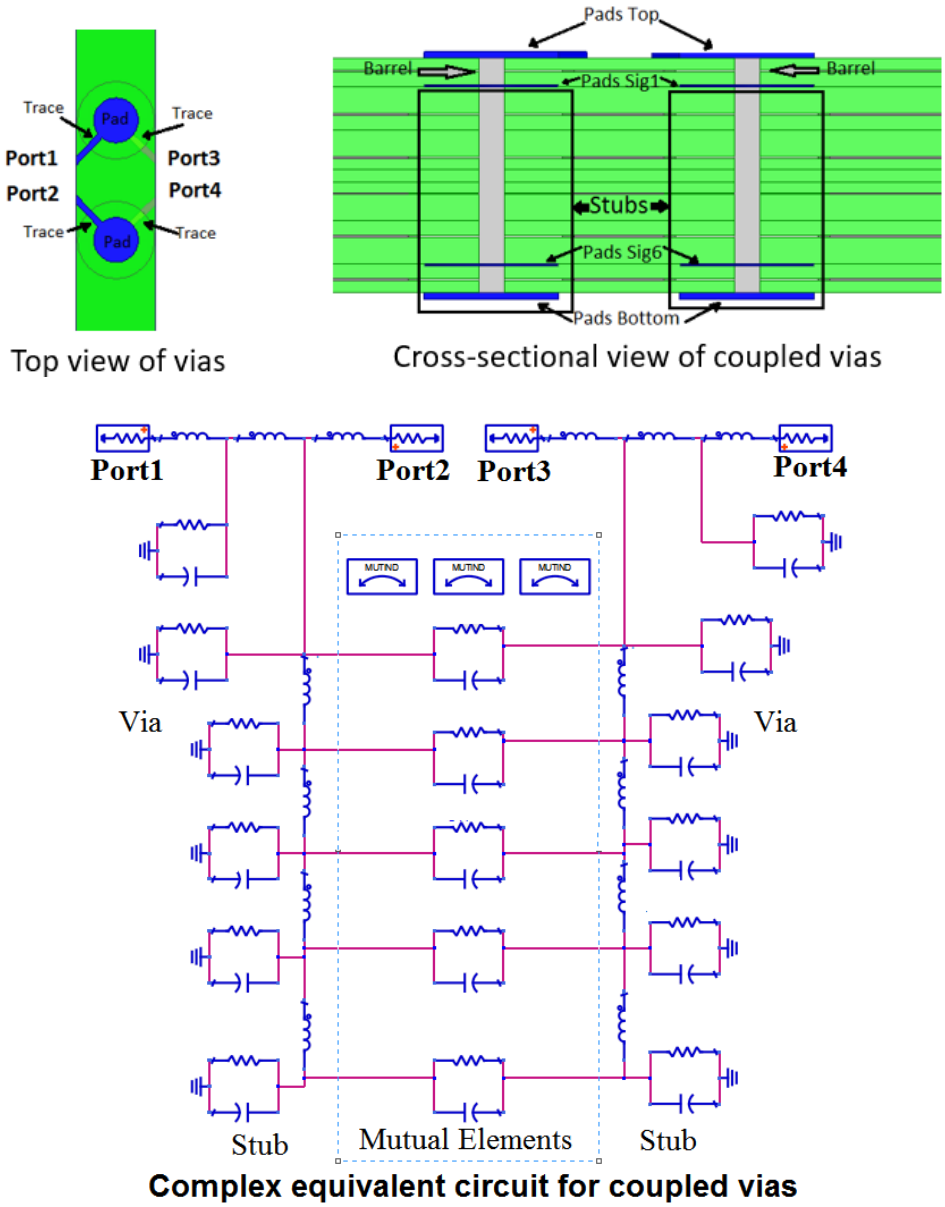

Figure 4.10: 3D and equivalent circuit models for coupled vias.

In these new models, the inductances $L1_{mm}$ and $L2_{mm}$ account for the inductive effect of the small traces crossing the antipad zones, as well as for the barrel inductance between their respective layers. $L3_{mm}$ represents the via-stub inductance. On the other hand, the metal losses in form of series resistors are also considered and represented by $R1_{mm}$, $R2_{mm}$, and $R3_{mm}$. $C1_{mm}$ and $C2_{mm}$ account for the capacitance of the overall structure and are supposed to present identical values because of the symmetry of the

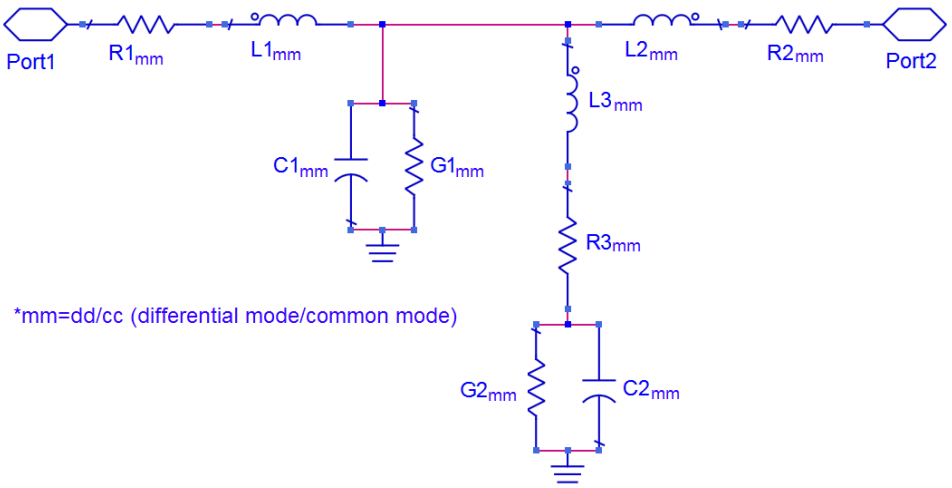

Figure 4.11: Simplified equivalent circuit model representing the coupled vias for the analyses in differential and common modes.

vias. It is assumed that the effect of pads is predominant over the barrel capacitance. Finally, shunt resistors (due to the polarization currents occurring within the dielectric laminates) account for the dielectric losses.

To proceed with the extraction, the common and differential S-parameters were converted to Z-parameters. This is due to the fact that this parameter set is easier to be associated to a T-network, which is a convenient representation for carrying out de-embedding of effects from the measured data.

Assuming the same geometry and length for each microstrip/stripline trace in the antipad zone, the obtained $L1$ and $L2$ inductances can be considered as identical. This is because there are no ground references modifying the inductance on that regions. Actually, this is verified in Fig. 4.12. Furthermore, when carefully inspecting the geometry and considering the corresponding impact on the electrical characteristics of the via, it is concluded that the expression used to calculate the via inductance, eq. (2.5.2), must be applied to the portion of the barrel in the transition layer. This considerably improves the results as shown later.

As for the case of the inductance, the values for the capacitances were extracted; the results are shown in Fig. 4.13. A dependence of frequency is observed. This is attributed to the contributions of distributed inductances and capacitances along the stub which are difficult to remove. The values at low frequencies were considered to be the correct.

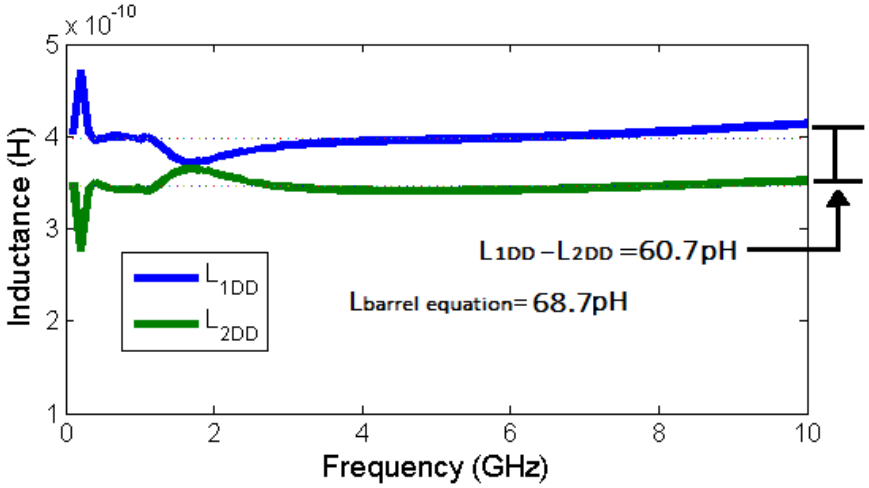

Figure 4.12: Extracted inductance versus frequency curves. Notice the difference in values to be near to the calculated value of the barrel inductance (non-stub) with equations. Due to the relatively small frequency variation observed in these curves, constant values are assumed without significantly penalizing accuracy to avoid unnecessary complication in the model implementation.

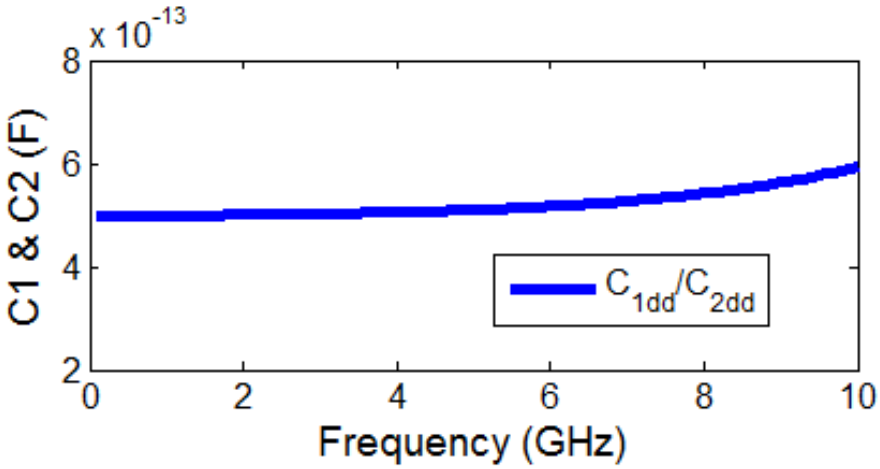

Figure 4.13: Capacitance versus frequency curves extracted for the reduced-differential model. Similarly as for the inductance cases, constant values are assumed in the final model.

Similar analyses were performed for the other two pairs of vias in differential and common models and, based on [50], values for elements of each via and for coupling were extracted.

After the extraction of the component values, a simulation on Agilent ADS (a SPICE-based tool) was performed as a validation step for verifying the equivalent circuit model for the coupled vias. In this case, a 4-port model for each structure was constructed. This model can be seen in Figure 4.14. The simulation results obtained

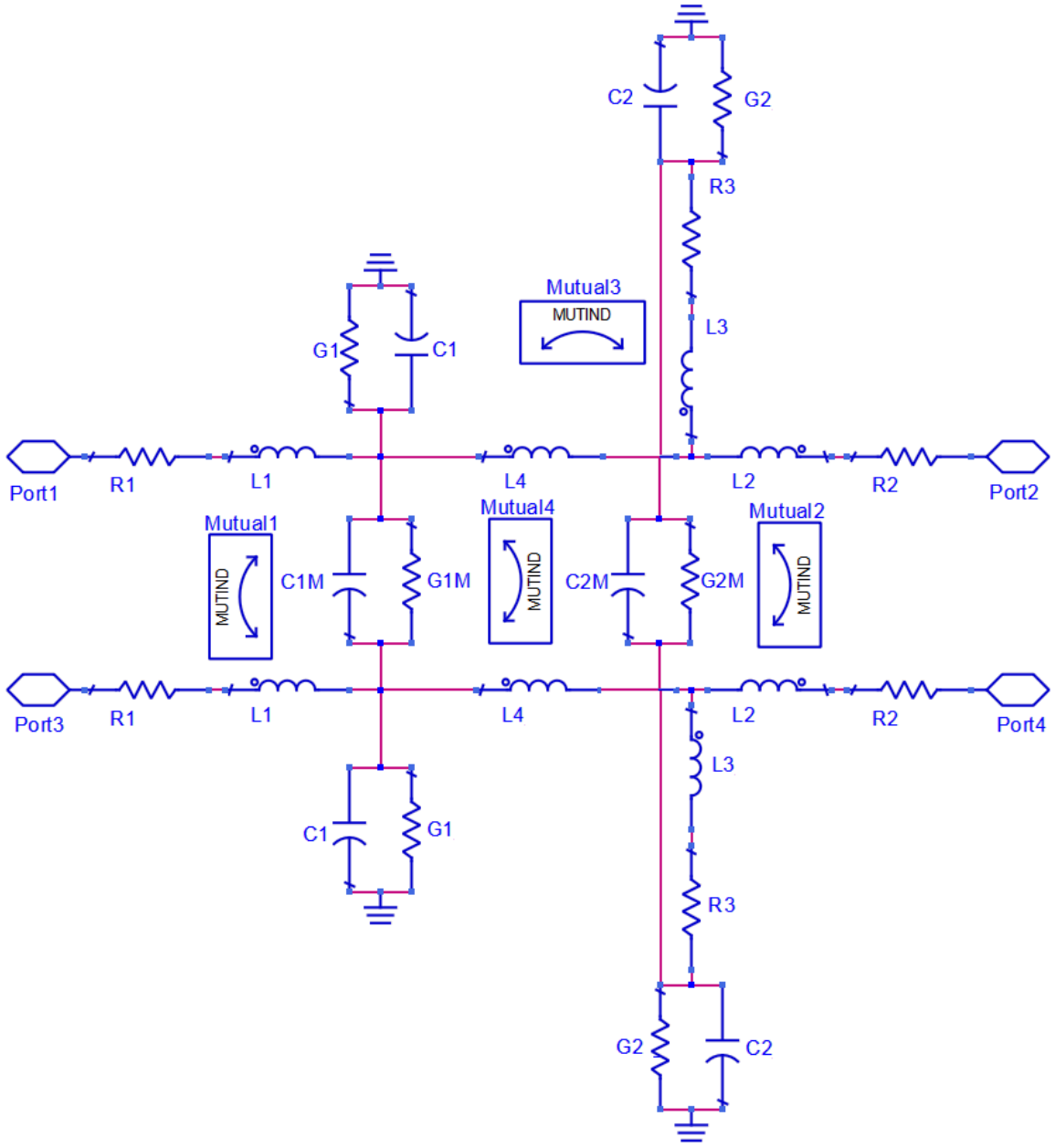

Figure 4.14: Equivalent 4-port circuit for representing the pair of coupled vias.

for the 3 structures when considering differential mode propagation are shown in Fig. 4.15. An excellent agreement between the 3D-simulation and the results obtained through the application of the equivalent circuit is observed for the three cases. The most notorious difference at first sight is in ϕ_1, but actually there is a maximum variation of $0.02dB$ for the transmission curves at high frequencies and $2dB$ for reflections

at low frequencies. Similar differences were observed in the other cases.

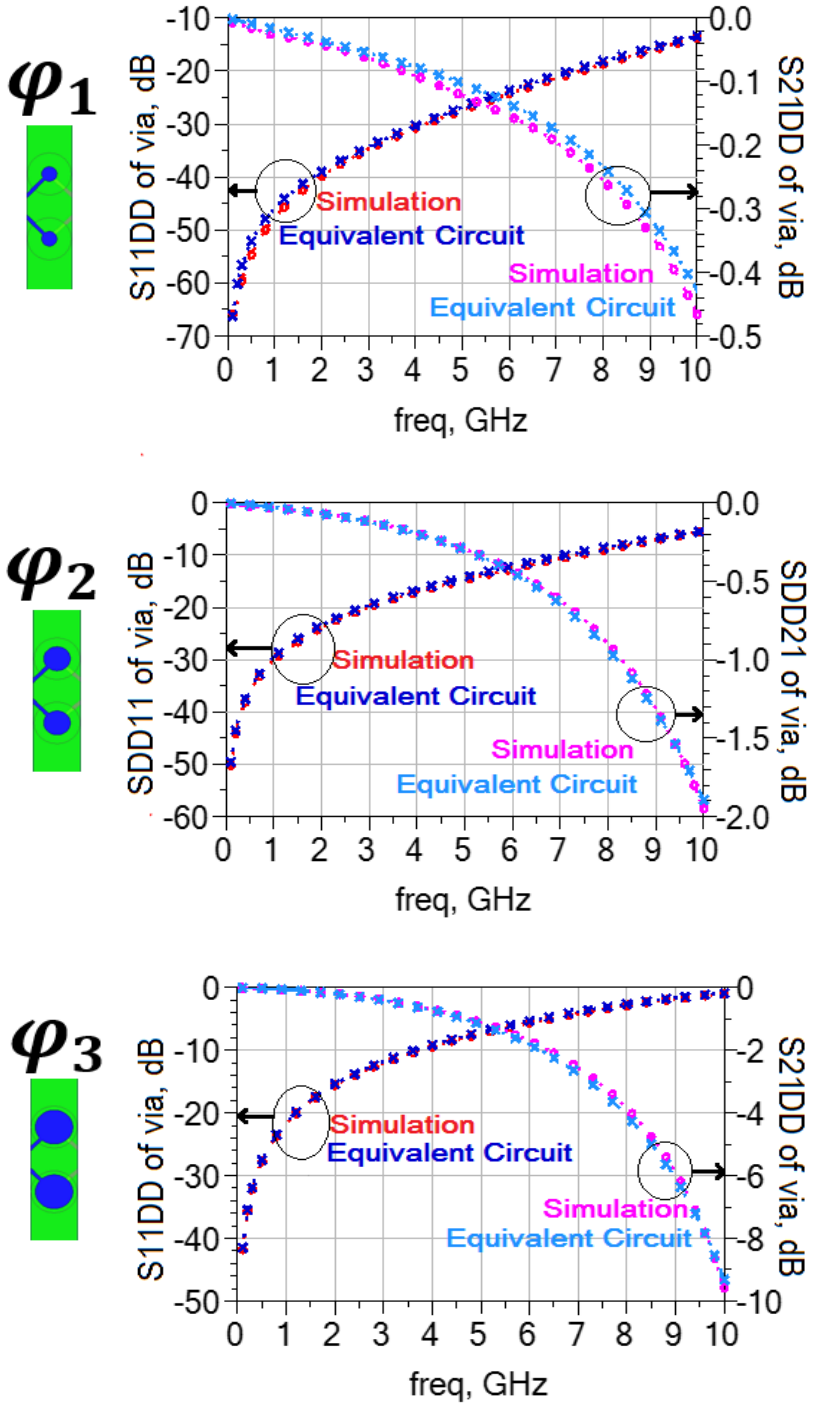

Figure 4.15: Comparison between 3D simulations and the proposed 4-port equivalent circuits.

4.5.3. Scalability: Extrapolations and interpolations

Once the values for the model parameters were extracted, a set of equations to describe the corresponding dependence on pad size is proposed. First, the inductive effect of the traces on antipads was analyzed. For this, the characterization of coupled microstrips and striplines in the channel was required so that the per-unit-length self-inductance was obtained. A linear relation accounting for this effect as a function of the length of the trace was easily obtained, as shown in Fig. 4.16. In this case, the effect of the clearance is negligible for the trace, because short dimensions were used.

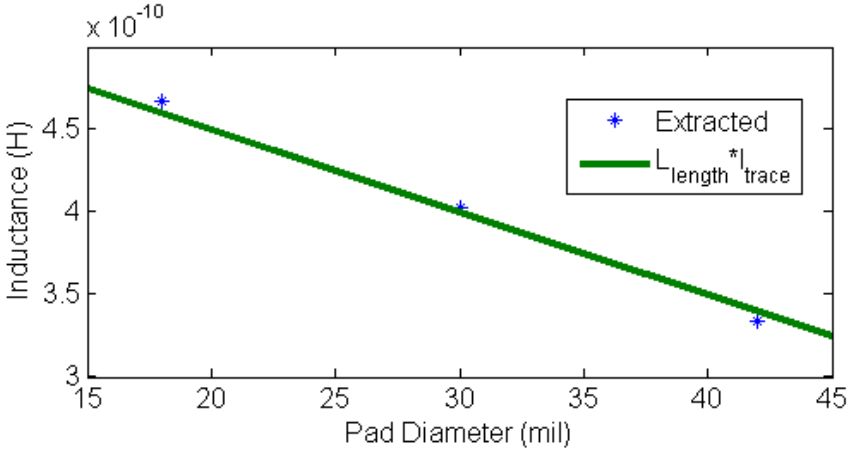

Figure 4.16: Linear relationship between the extracted inductance and the pad dimensions.

Regarding the capacitance, additional characterizations were performed. The responses of the self-capacitances obtained in the three cases, as function of the pad diameter, are shown in Fig. 4.17. To propose an expression that allows to obtain the corresponding curve, it was firstly assumed that a polynomial function based on the three points could serve well to obtain a correct interpolation and extrapolation of data.

The use of a polynomial function is well explained by the effects considered along the via. It can be observed that, for a decrement in the pad diameter, there is also a reduction in the capacitance value so that, for a pad diameter equal to zero, the only effect to be considered is that due the barrel capacitance. Although this behavior is expected, it is not completely well explained by the polynomial function because, near to the zero value in the pad diameter, an increment in the calculated capacitance

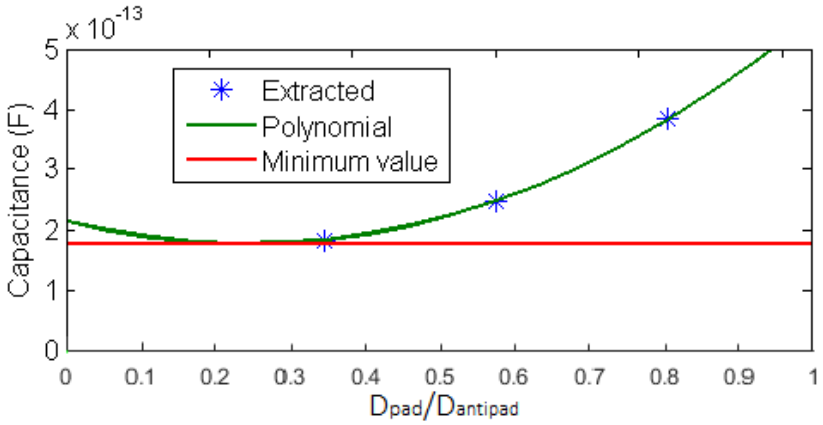

Figure 4.17: Self-capacitances extracted for the models. Dependence in geometry is observed, as is expected, but a polynomial function does not completely serve to characterize the effects.

is observed. However, a minimum value is extracted so that the barrel capacitance can be approximately calculated. Taking into account this minimum value, equations (2.5.1) and (3.5.2) were applied considering the dimensions of the pad instead those of the barrel. This was made to observe the variation between them and the response for the sizes and materials used. Higher values were observed between the values obtained from the formulas and the extracted values. So, a factor was introduced to obtain the best correlation. As depicted in Fig. 4.19, the best value for this factor is 0.16, which falls into the predictions of the reference [39]. Furthermore, it was observed that without considering the addition of the barrel capacitance, the value for the factor was about 0.35.

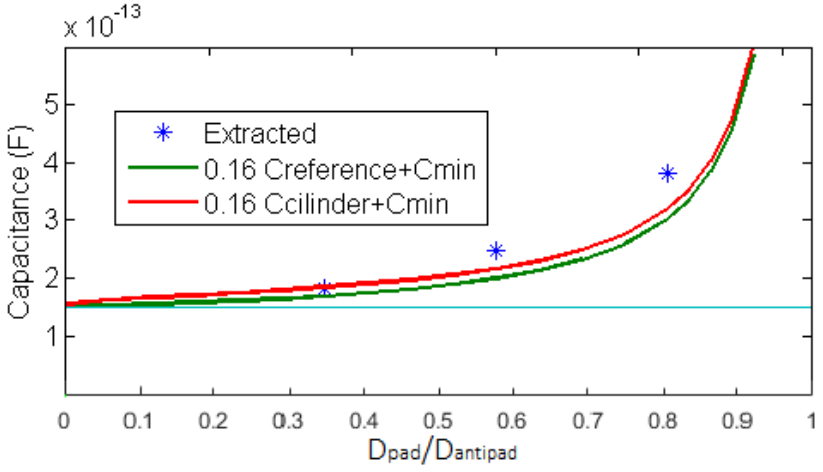

Figure 4.18: Extracted self-capacitances. Differences between the pad capacitance in ref. [22] and the formula for a cylinder capacitance are negligible.

After considering in more detail the behavior of the electric field for the structures, as depicted in Fig. 4.19, the expressions defined in Chapter 3 were used: eq. (3.5.2), eq. (3.5.10), and eq. (3.5.11). This allowed to get a better description of the electrical behavior impacting the self-capacitance. A much better correlation is observed in the case of eq. (3.5.10), although the analysis considered does not allow to explicitly separate the effects of each pair of closely spaced pads. With the corresponding considerations, the values of K_b and K_p were calculated as 1.38 and 1.2, respectively.

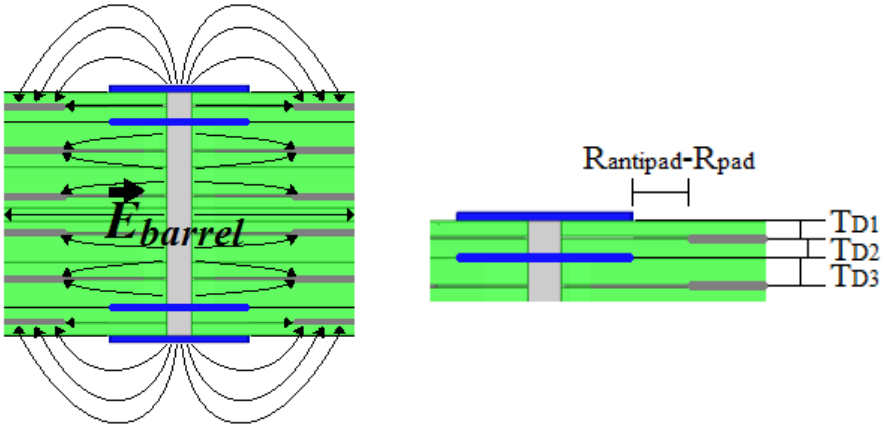

Figure 4.19: Left: Conceptual depiction of the distribution of the electric field along the via structure. Right: Detail of the structure illustrating that pads and ground layers are not coplanar.

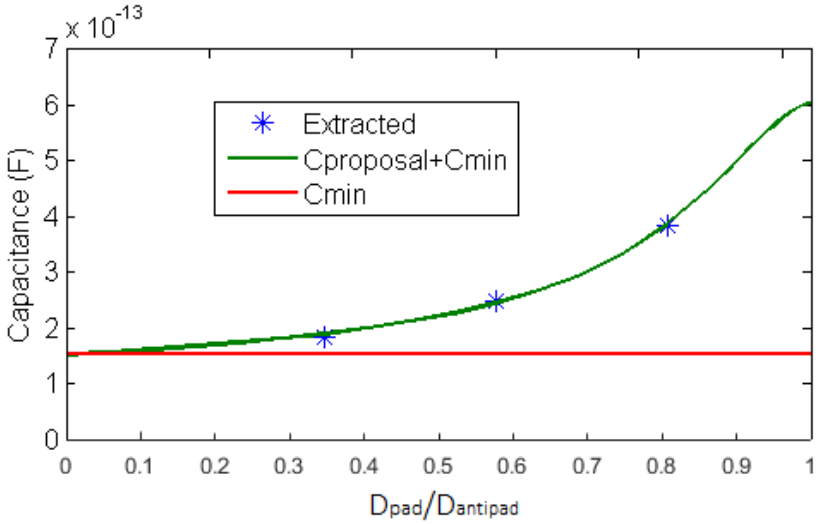

Figure 4.20: Capacitance curve versus pad size feature illustrating the good agreement between the scalable model equation and the extracted data.

In addition, for a further evaluation of eq. (3.5.10), a new set of simulations for

pairs of coupled vias presenting several pad variation were performed. Again, the values for the equivalent circuit models were extracted. Fig. 4.21 shows the results, comparing literature and proposal for the pad capacitance. Again, excellent correlations in all situations are observed when applying the proposal.

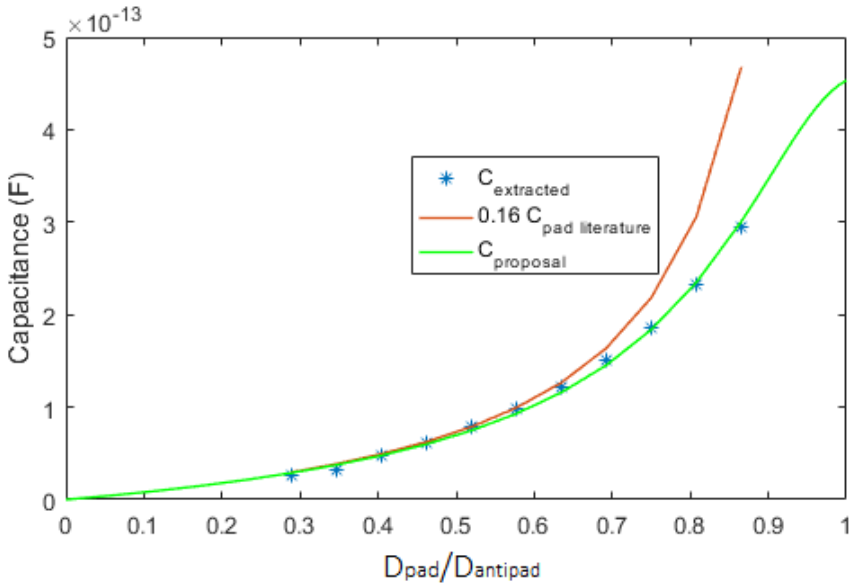

Figure 4.21: Interpolation using the proposed equation compared with the equation available in the literature, which considers a correction factor of 0.16.

Despite the presence of reference planes between vias, the mutual capacitance was calculated using eq. (3.5.12). As for the self-capacitances case, polynomial functions were obtained to extract the capacitance due to barrels. However, the resulting value was small enough to be considered negligible. In this case, the main contribution to the mutual capacitance is related to the pads. Another constant to the equation was added, K_2, to get a better correlation, as shown by eq. (4.5.1). The values for best correlation were $K_1 \approx 0.01$ and $K_2 \approx 0.610$. Results are displayed in Fig. 4.22.

$$C_{\text{mutual proposal}} = \frac{K_1 h_{\text{barrel}} \pi \epsilon_0 \epsilon_r}{acosh(\frac{K_2 D_{\text{barrel to barrel}}}{D_{\text{pad}}})} \tag{4.5.1}$$

Regarding the conductor losses in traces, constant values were considered. For dielectric losses, a linear model dependent on both frequency and capacitance was used, as explained in [51]. Once these expressions were obtained, a final validation was performed. To do this, the fourth structure, similar to the previous ones, was

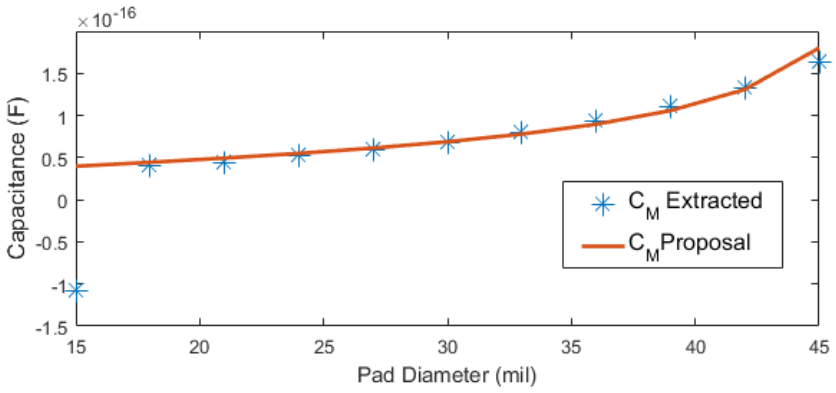

Figure 4.22: Extracted and calculated mutual capacitances. Good correlation observed.

used. In this, different values for the pad and antipad are considered. Using the previously developed equations and the values for constants obtained experimentally, the 4-port equivalent circuit was modeled. Thus, the response obtained when applying the equivalent circuit for the whole channel was quickly obtained and compared to measured data. This is shown in Fig. 4.23.

4.6. Conclusions

In this chapter, the methodology implemented for the extraction of scalable models for interconnects was verified and validated with a set of real-world structures, measurements and simulations, as well as proposed circuit equivalent models. It is observed that a correct segmentation of interconnect channels allows to identifying and characterizing sections of interest. With this, one can perform characterizations in the form of accurate equivalent circuits based on physics, reducing time for further analyses. Additionally, different cases not necessarily prototyped can be studied through data interpolation and extrapolation. This is achieved through using scalable models as the one formulated in this thesis.

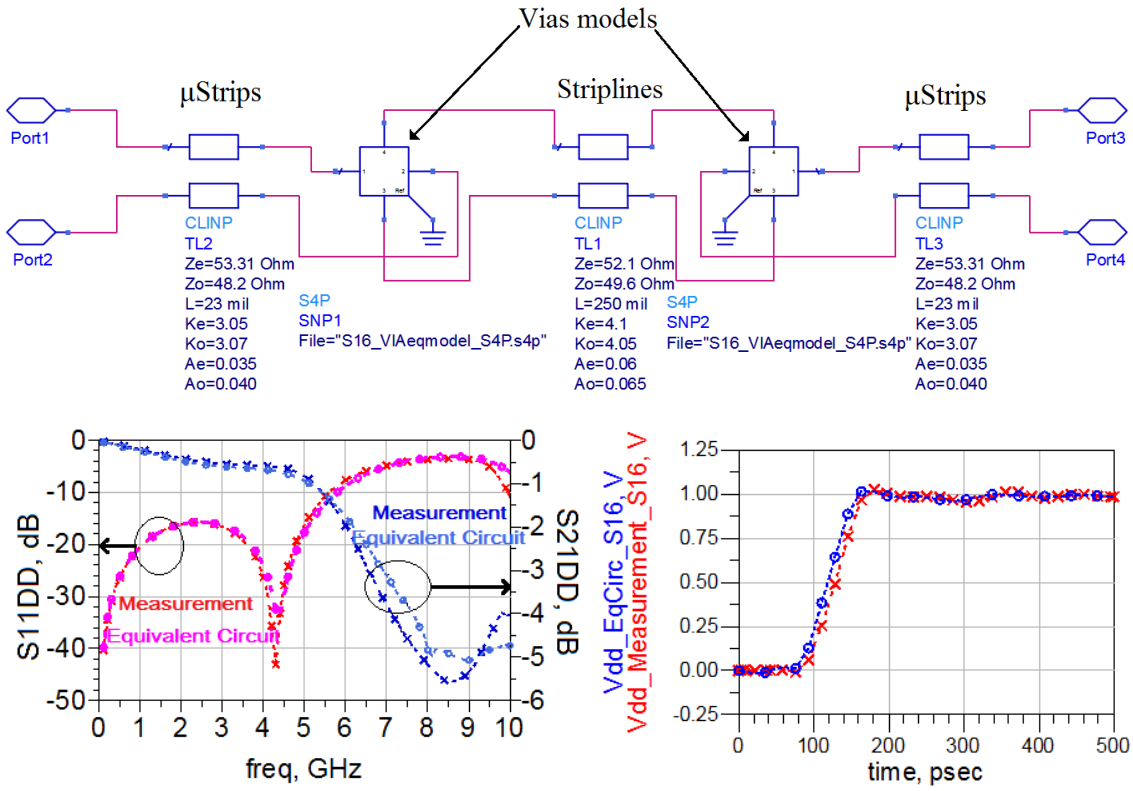

Figure 4.23: Equivalent circuit model implemented in ADS for the whole channel. Top: Block diagram. Bottom: S-parameter and time-domain data comparing simulated with experimental results.

Chapter 5

General conclusions

A detailed analysis for identifying the impact of via structures affecting the performance of channels used for guiding high-frequency signals on PCB was carried out in this thesis. The modeling of these interconnects is based on a systematic application of full-wave solvers, measurements on prototypes, interpolations, extrapolations and physics-based equations. The analysis involves the study of via-pad effects accounting for the degradation of signals. As a result, some observations and conclusions of the study are presented on this chapter.

5.1. Vias on interconnects

Vias, typically used to transmit signals in multilayer structures, can be seen as electrical discontinuities. If not properly designed, these structures may introduce significant signal reflections that degrade the integrity of the signals. Furthermore, these reflections, power losses, and data degradation is considerably accentuated at the high frequencies associated with current digital data rates. Therefore, the appropriate modeling of vias is mandatory for achieving the desired performance of interconnects on PCB technology. In this regard, multiple parasitics previously ignored cannot be neglected within the range of frequencies analyzed, since they can contribute significantly to the overall performance of the interconnections.

The behavior of pads reassembling cylindric capacitors has been shown to be noticeable. This allowed to formulate expression for the appropriate calculation of

the associated values. However, the contributions of fringing-fields to the electrical behavior of the structure, the use of dissimilar materials, as well as the non-ideal geometries presented in these types of structures, can account significantly for variation of the theoretical results. Is in these cases, when other analysis techniques such as numerical methods can bring a better description of the phenomena involved. In addition, it is important to take into consideration the inductive effect of the traces on antipad zones, as they perform connection between vias and transmission lines.

For the analysis of coupling effects occurring in pairs of vias, the same considerations apply for their modeling. In general, the presence of potentials of reference between these structures, considerably reduces the effect of mutual coupling.

5.2. Systematic characterizations and scalable models

It is observed that, a correct segmentation of communication channels based on calibrated simulations and prototypes, allows identifying critical effects affecting the performance. With this in mind, one can perform characterization in the form of simpler but accurate models, reducing time for further analysis.

The support from numerical methods applied on computational tools is noted. These can bring a better appreciation of the effects for the analyzed structures. However, a good understanding of the method applied, as well as a theoretical support, is required to identify the limitations of the obtained results.

As a result of the aforementioned, it is observed that through a correct set of measurements and analyses, the accurate behavior for the analyzed structures can be obtained. With this, new and accurate solutions can be obtained to reduce the time of analysis.

5.3. Future work

In the present work, although the responses of the models represent the behavior of the structure well enough, further characterizations to observe the contribution from different dielectrics and their relationship to the fringing-field need to be performed. In this respect, future research is proposed to modeling these aspects with accuracy.

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