PAPR Reduction and Asynchronous Multiplexing with CCK Non-Maximally Decimated Filter Banks in OFDM systems

By

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To my parents, who without going a single day to school,
gave me the best education at home

Abstract

First is presented an introduction to mobile communications, OFDM (Orthogonal Frequency Division Multiplexing), the FFT (Fast Fourier Transform), perfect reconstruction and efficient implementation in filter banks, finalizing with channelizer systems. The advantages and disadvantages of OFDM are elaborated in order to introduce a principal subject of our investigation, which is the channelization technique using non-maximally decimated polyphase filter banks based on the state-of-the-art from the literature. The channelizer is designed using a polyphase structure followed by an FFT block to modulate a prototype filter and thus implement N filters for the price of one, reducing significantly the workload of the system.

Orthogonal Frequency Division Multiplexing (OFDM) is adapted to the channelizer in order to test isolation between mobile stations (MS) when a communication link is established with the base station (BS). Typical synchronization techniques used in Wireless Local Area Network (WLAN) systems like frame detection and channel estimation are employed to test the correct operation and performance of the entire communication system.

Peak to Average Power Ratio (PAPR) is reduced by using a codification technique based on polyphase complementary codes which is adapted to the OFDM modulator. The results are verified by simulations in Matlab, ModelSim and FPGA implementation.

Resumen

Primero se presenta una introducción a los sistemas de comunicación móvil, multiplexación por división de frecuencia ortogonal (OFDM), la transformada rápida de Fourier (FFT), reconstrucción perfecta e implementación eficiente en bancos de filtros, finalizando con sistemas de canalización. Las ventajas y desventajas de OFDM son elaboradas de manera que se introduzca el principal tema de nuestra investigación, el cual es la técnica de canalización utilizando bancos de filtros polifásicos diezmados no-maximales basandose en la literatura actual. El canalizador es diseñado utilizando una estructura polifásica junto con la transformada rápida de Fourier (FFT) para modular un filtro prototipo y de esta manera implementar N filtros por el precio de uno, reduciendo significativamente la carga de trabajo del sistema.

Multiplexación por división de frecuencia ortogonal (OFDM) es adaptado al canalizador para probar el aislamiento entre las estaciones móviles (MS) cuando un enlace de comunicación es establecido con la estación base (BS). Técnicas de sincronización típicas utilizadas en sistemas de redes de área local inalámbricas (WLAN) como detección de trama y estimación del canal son empleadas para probar el correcto funcionamiento y rendimiento del sistema de comunicación entero.

La relación pico a valor medio de potencia (PAPR) es reducido utilizando una técnica de codificación basada en códigos complementarios polifásicos los cuales son adaptados al modulador OFDM.

Los resultados son verificados por simulaciones en Matlab, ModelSim e implementación en FPGA.

Preface

This thesis aims to analyze and implement a synthesis/analysis rational $M/2$ 64-channelizer with polyphase DFT (Discrete Fourier Transform) filter bank in order to isolate different users and avoid complex time synchronization employed in Long-Term Evolution (LTE) systems. OFDM (Orthogonal Frequency Division Multiplexing) signals with different delays are generated to emulate the users or BS's (Base Stations). Frame detection and channel estimation algorithms are employed in every channel. A polyphase Complementary Code Keying (CCK) technique is applied to OFDM in order to reduce high values of Peak to Average Power Ratio (PAPR).

The outline of the Thesis is described in the following set of different topics which can be analyzed independently as follows:

First, an introduction to mobile networks, multipath propagation and multicarrier systems is provided in Introduction. Then, a review of filter banks explaining perfect reconstruction and efficient implementation is presented in Chapter two. Subsequently a brief introduction to the Fast Fourier Transform (FFT) is presented.

For Chapter three, OFDM is presented describing advantages and disadvantages. A comparison in PAPR with the single carrier version is made. In addition, a brief explanation about the physical layer and multiple access for LTE is addressed at the end of the chapter.

Chapter four contains the introduction and design of channelization by transforming the super-heterodyne receiver in its digital form step by step. A review of methods is necessary for comparison. Finally a rational sampling rate modification is made to the channelizer.

Golay complementary codes that are designed and extended to non-binary data are presented in Chapter five. Implementation structures and decoding techniques are also introduced.

Analysis and simulations are described in Chapter six. Matlab and ModelSim are

used to design, test and debug every part of the entire channelization system.

FPGA implementation that aims to present and prove the reduction in resources for the channelizer system, is presented in Chapter seven.

Finally, conclusions and future work are detailed in Chapter eight.

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Chapter 1
Introduction

In this first chapter, principles of mobile communications are introduced. A comparison between single carrier and multicarrier systems is made in multipath propagation environments. Advantages and disadvantages are presented in both systems from a time-frequency point of view.

1.1. Introduction to Mobile Communication Systems

The most basic representation of a communication system consists of three simple blocks: transmitter, channel and receiver, as shown in figure 1.1.

Figure 1.1: Communications system simple diagram.

In wireless communication systems, a transmitter and a receiver are located in the same unit called a transceiver. A transceiver known as base station (BS), is in charge of connecting two or more transceivers called mobile stations (MS). A BS is separated from adjacent BS's in a covered distance range with hexagonal shape which is called a cell. A set of adjacent BS's are put together in cells with different frequencies to avoid interference; the whole set is a cellular system. A communication process is achieved by connecting two or more transceivers trough a link. If the BS sends information to a MS the link between them is called downlink, the opposite is called uplink.

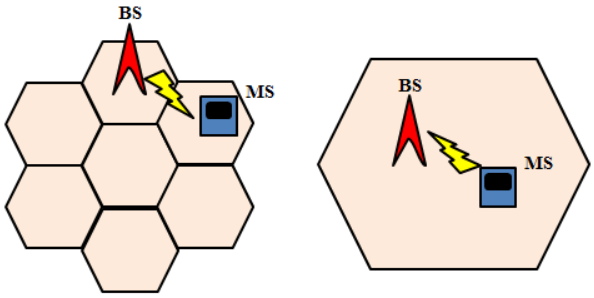

Figure 1.2: Downlink and uplink transmission.

1.2. Multipath Propagation

In wireless communications, digital data modulates an analog carrier signal before it is send to the receiver. When signals are transmitted by means of radio waves, these signals are propagated in multiple directions. As shown in figure 1.3, the signal sent from the BS arrives to the MS by different paths, due to reflection, diffraction and scattering. As a result, the MS receives delayed and attenuated versions of the signal.

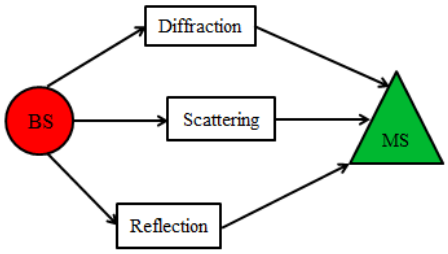

Figure 1.3: Multipath propagation.

Two problems are generated because of multipath propagation: time delay spread and fading in frequency. There exist two main types of modulation formats which address this problems in different way: single and multi carrier. Single carrier systems are those where the information is sent with a wide bandwidth, using a single waveform with a very short symbol duration in time. Multi carrier systems modulate the information in a way that a set of subcarriers with narrow bandwidth each, is sent as a composite signal in time by adding all the subcarriers. Every subcarrier presents a very long symbol duration in time compared with the single carrier system, generally NTs, where Ts is the symbol duration for single carrier.

Figure 1.4 shows how delay spread is addressed. The channel is modeled in a way that introduces a delay to every symbol. Single carrier systems use a very short symbol duration, thus when a symbol is passed through the channel, most of it is distorted by the adjacent symbol. For multicarrier system, long period symbols are sent through the channel and only a quarter part of the symbol is distorted.

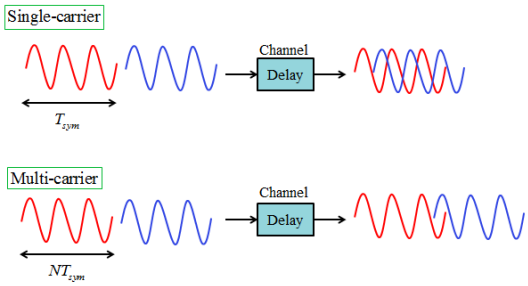

Figure 1.4: Delay spread in time for single-carrier and multi-carrier systems.

In the case of frequency fading, single carrier systems transmit a wideband signal which is longer than the frequency selective fading channel thus the signal is completely distorted. Multicarrier systems transmit a set of narrowband signals which see the selective fading as a flat channel. In consequence only the amplitude of the subcarriers is attenuated. Figure 1.5 shows both systems in the frequency domain. For multipath propagation, multicarrier systems are the best option, because the distortions in time can be avoided by inserting a cyclic prefix. In frequency, a single tap equalizer is required which compared to the adaptive filter used in time equalization for single carrier systems, results in a significant reduction of resources and complexity.

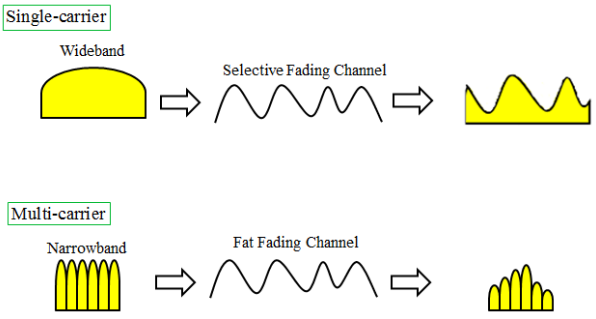

Figure 1.5: Frequency selective fading for single-carrier and multi-carrier systems.

Chapter 2

Review of Filter Banks and The Fast Fourier Transform

Filter bank theory and the Fast Fourier Transform are addressed in this chapter. Perfect reconstruction and efficient implementation with polyphase structures is presented. The main advantages and problems presented in the FFT are introduced. A combination of filter banks and the FFT is explained for transmultiplexer implementation.

2.1. Filter Banks

The filter bank is composed of the Analysis and Synthesis filter bank, as shown in figure 2.1. The set of filters in red are known as analysis filter bank $H_k(z)$ and are in charge of splitting an input signal into N subsignals. The set of filters in blue are known as synthesis filter bank $G_k(z)$ and combine N subsignals into a single signal [6]. The cascade connection of analysis/synthesis filter banks is called a subband coding system. Subband coding is mainly employed in speech coding.

The cascade connection of synthesis/analysis filter banks is called a transmultiplexer. They are mainly employed in data transmission, where a TDM-FDM-TDM conversion is carried out. A composite FDM signal is generated by the synthesis filter bank, where the upsampling blocks increase the sampling rate to insert every subsignal in a corresponding channel. The analysis section is in charge of extracting every single channel embedded in the composite signal. The downsampling blocks reduce the sampling rate of the channel for congruence with the extracted bandwidth. This system is shown in figure 2.2.

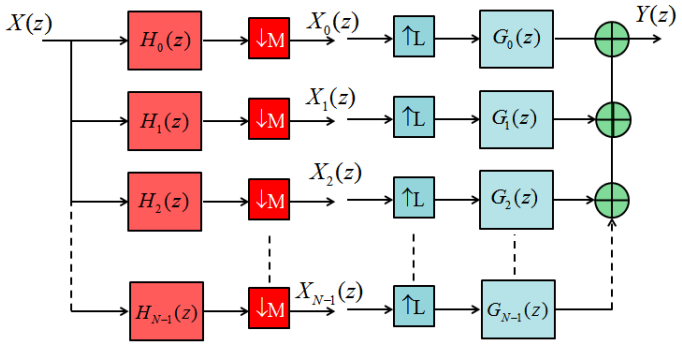

Figure 2.1: Subband coding system.

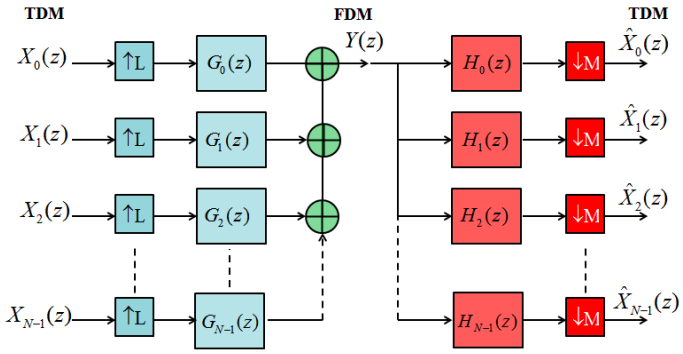

Figure 2.2: Transmultiplexer.

In subband coding and transmultiplexer systems, analysis and synthesis filters must be designed in order to obtain perfect reconstruction: The output must be a delayed and scaled version of the input signal [6, 7, 8]:

$$y(n) = cx(n-k). \tag{2.1.1}$$

To achieve perfect reconstruction, the transfer function $T(z)$ must be equivalent to a delay, as shown in equation (2.1.2). With this, linear distortion due to amplitude and phase is eliminated.

$$T(z) = z^{-d}. \tag{2.1.2}$$

Filter banks in a subband coding system must be designed to cancel aliasing. The transfer function corresponding to a subband coding systems is shown in equation

(2.1.3). Perfect reconstruction can only achieved for $l = 0$.

$$T(z) = \sum_{k=0}^{N-1} H_k(zW^{-l})G_k(z). \tag{2.1.3}$$

For the transmultiplexer, crosstalk elimination must be achieved to avoid interference from adjacent channels. Crosstalk is eliminated when the transfer function equals to zero only for $k \neq i$. The corresponding transfer function is shown in (2.1.4).

$$T_{ki}(z^N) = \sum_{l=0}^{N-1} G_k(zW^{-l})H_i(zW^{-l}). \tag{2.1.4}$$

Both systems, transmultiplexer and subband coding are considered complementary. A transmultiplexer that eliminates crosstalk can be implemented as a subband coding system with the same set of filters. Nevertheless, the opposite is true only if the transfer function corresponding to the subband system is a function of z^N [8]. In other words, the transfer function of the subband system must be equivalent to a delay that is multiple of N, where the upsampling/downsampling factors must be equal to the number of channels $N = M = L$. The delay corresponding to the transfer function, usually corresponds to the group delay that is generated in the synthesis and analysis filters when they are designed to be causal systems. Thus, in order to show the necessary condition of a delay to be a multiple of N, we replace both analysis/synthesis filter banks with an equivalent delay, as shown in figure 2.3. This is a subband coding system where filters are represented with their corresponding delays d_1 and d_2.

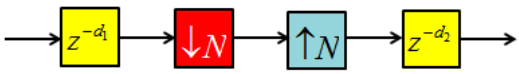

Figure 2.3: Subband coding system with delay representation.

When this filters are swapped to obtain a transmultiplexer, as shown in figure 2.4, the input signal is first upsampled, $N - 1$ zeros are inserted between samples. These zeros are then thrown away by the downsampling block, where only every N sample is retained. If the sum of the delay blocks is not a multiple of N, then, the downsampling block will retain zeros and the output won't be a delayed version of the input.

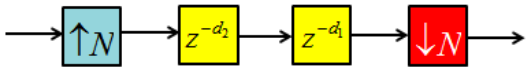

Figure 2.4: Transmultiplexer system with delay representation.

Hardware implementation of all filters, results in a high use of resources. A better implementation consists in the use of polyphase filter banks. Every synthesis/analysis filter along with their corresponding upsampling/downsampling blocks, form a decimation and interpolation structure respectively, as shown in figure 2.5.

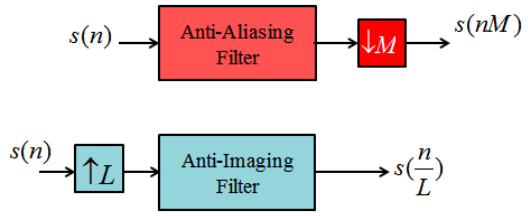

Figure 2.5: Decimation (red) and interpolation (blue) structures.

These filters can be decomposed in a set of subfilters of length M or L with different phases. This is known as polyphase decomposition. We decompose only one filter which will be called a prototype filter. The decomposition process is shown with an example. Suppose we have a filter of order 8 as shown in equation (2.1.5) and a downsampling by $M = 3$.

$$H(z) = h(0)+h(1)z^{-1}+h(2)z^{-2}+h(3)z^{-3}+h(4)z^{-4}+h(5)z^{-5}+h(6)z^{-6}+h(7)z^{-7}+h(8)z^{-8}. \tag{2.1.5}$$

First, a 2D mapping is made by loading a matrix by columns of M elements, equation (2.1.6) shows this mapping which sometimes is known as lexicographic.

$$\begin{aligned} H(z) = h(0) + h(3)z^{-3} + h(6)z^{-6} \\ +h(1)z^{-1} + h(4)z^{-4} + h(7)z^{-7} \\ +h(2)z^{-2} + h(5)z^{-5} + h(8)z^{-8}. \end{aligned} \tag{2.1.6}$$

It can be observed that except for row 0, every row can be factorized as shown in

equation (2.1.7).

$$\begin{aligned} H(z) &= h(0) + h(3)z^{-3} + h(6)z^{-6} \\ &+z^{-1}(h(1) + h(4)z^{-3} + h(7)z^{-6}) \\ &+z^{-2}(h(2) + h(5)z^{-3} + h(8)z^{-6}). \end{aligned} \tag{2.1.7}$$

This factorization permits to represent the original filter as an algebraic sum of expanded by M and delayed subfilters. Equation (2.1.8) expresses this mathematical structure.

$$H(z) = E_0(z^3) + z^{-1}E_1(z^3) + z^{-2}E_2(z^3). \tag{2.1.8}$$

Equation (2.1.9) represents the polyphase decomposition for a decimator in a more general form. Figure 2.6 illustrates the corresponding block diagram.

$$H_k(z) = \sum_{k=0}^{N-1} z^{-k}E_k(z^M). \tag{2.1.9}$$

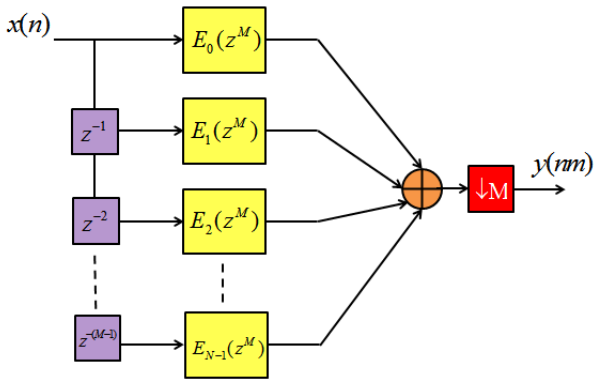

Figure 2.6: Decimator polyphase representation.

Every subfilter is expanded by M and located in the left side of the downsampling block. This allow us to invoke the third Noble identity which permit to place the downsampling block in the left side of every subfilter and causing a compression by M in the impulse response of every subfilter. This is shown in figure 2.7.

Now the filters are processing data in a lower sampling rate. In addition the number of operations per input is significantly reduced to N/M. Finally we observe

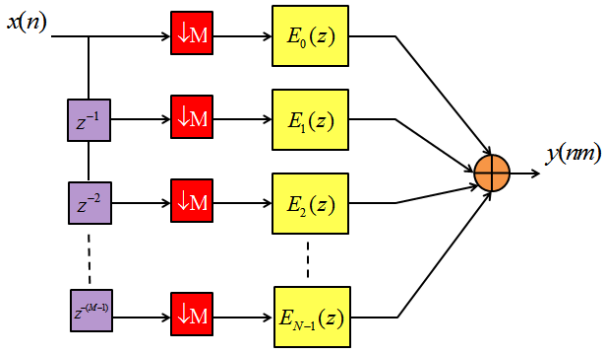

Figure 2.7: Decimator polyphase representation with Noble identity.

that only one branch is processing data in every clock cycle, which is not efficient. The structure can be improved by replacing the delay chain along the downsampling blocks for a simple commutator, as shown in figure 2.8.

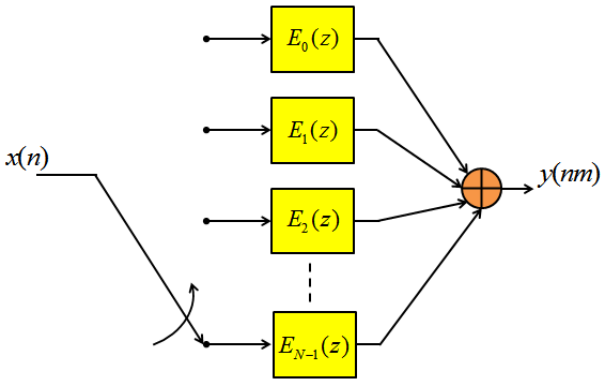

Figure 2.8: Efficient polyphase implementation.

Polyphase decomposition for an interpolator is just the dual version of the decimator where just a reverse of the signal flow is needed, as shown in figure 2.9.

Figure 2.10 presents the efficient implementation of the synthesis and analysis filters for a transmultiplexer.

However, with these structures, only one channel in DC can be processed. To implement the other filters, a modulation of the prototype filter can be made by using a set of phase rotators as shown in equation (2.1.10).

$$h_k(n) = h(n)e^{j\frac{2\pi}{N}kn}. \tag{2.1.10}$$

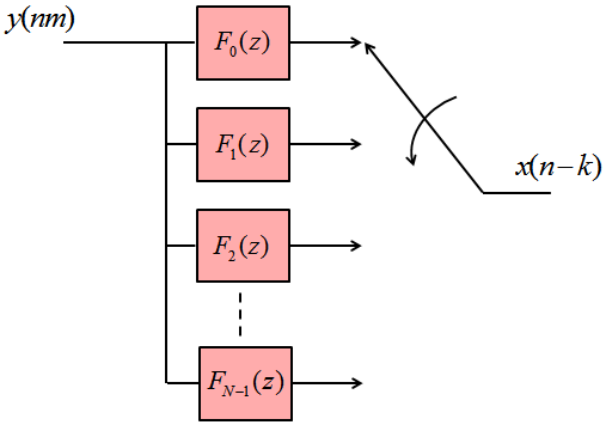

Figure 2.9: Efficient polyphase representation for interpolation.

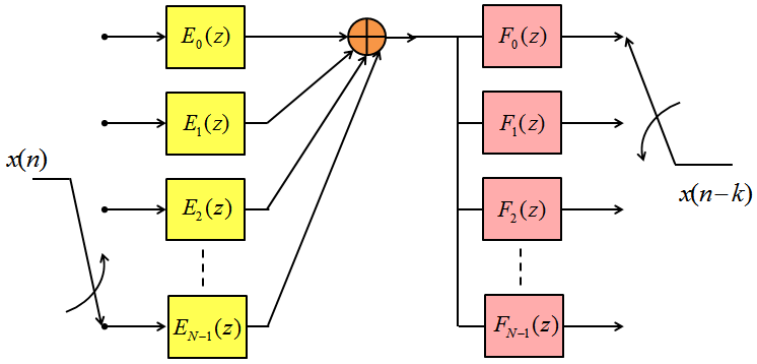

Figure 2.10: Efficient polyphase representation for decimation and interpolation.

This modification is applied to the polyphase structure, as shown in equation (2.1.11).

$$H_k(z) = \sum_{k=0}^{N-1} z^{-k} E_k(z^M) e^{j\frac{2\pi}{M}kn}. \tag{2.1.11}$$

We can observe that the set of phase rotators can be implemented by using an IDFT (Inverse Discrete Fourier Transform). The DFT polyphase filter bank structure for a multiplexer with efficient implementation is shown in figure 2.11.

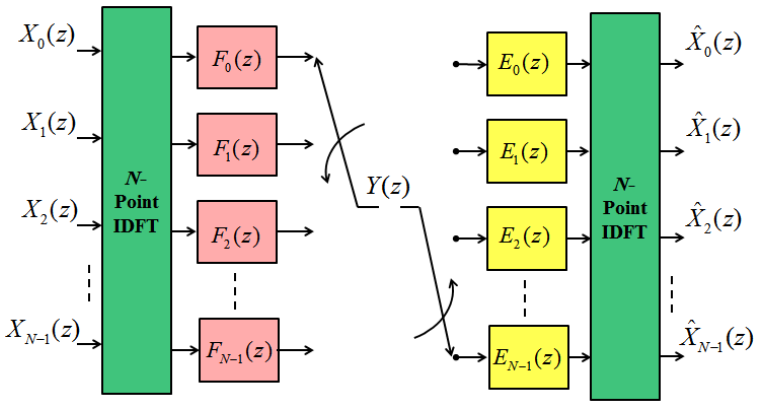

Figure 2.11: DFT filter bank for transmultiplexing.

2.2. The Fast Fourier Transform

The Fourier transform is a mathematical tool that permits to analyze signals and systems in the frequency domain and vice versa [9].To implement the Fourier transform in digital hardware like a microprocessor or an ASIC, the Discrete Fourier Transform (DFT) is employed.

The process of decomposing a time function in series of sines and cosines is known as Fourier analysis. It consists in the linear projection of the original time series function onto a set of basis functions $e^{-j\frac{2\pi}{N}kn}$. The recombination of these projected functions is known as Fourier synthesis [10]. Sines and cosines are considered orthogonal over a period if their inner product is zero, as shown in equation (2.2.1).

$$< f, g >= \sum_{n=0}^{N-1} cos(\omega n) sin(\omega n) = 0. \tag{2.2.1}$$

A sufficient but not necessary condition for the DFT to exist is that the time input series $x(n)$ must be absolutely summable,

$$\sum_{n-\infty}^{\infty} |x(n)| < \infty. \tag{2.2.2}$$

The DFT processes discrete samples in both time and frequency domain, as shown in figure 2.12. This causes periodicity in both domains. Therefore, only the range of frequencies within the sampling rate of the signal is shown. Whilst in the time domain

a truncation of the signal is made to process a finite number of samples.

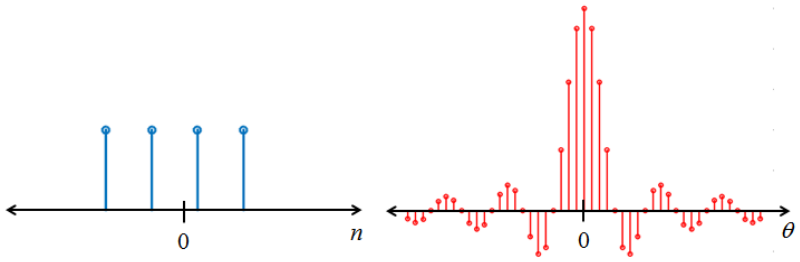

Figure 2.12: Discrete time pulse (blue) along its corresponding discrete spectrum (red).

The DFT mathematical expression is shown in equation 2.2.3.

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi}{N}kn}, \tag{2.2.3}$$

Where $x(n)$ is the time input series, $e^{-j\frac{2\pi}{N}kn}$ are the basis complex functions or *twiddle factors*, and $X(K)$ represents the discrete frequency output. The DFT is defined over a range of frequencies equal to the sampling rate. The spectral resolution is the separation between frequency samples (bins) and is defined as the ratio of the sampling rate to the number of points in the DFT. In computer hardware the DFT only presents the amplitudes of the corresponding frequencies that synthesize the input signal. To understand how the DFT works, we need to pay attention to figure 2.13. Here, the DFT is defined as an analysis process where the input signal passes through a set of correlation blocks and the amplitude of the corresponding frequency signal is delivered to the output. The inverse process consists in the multiplication of these amplitudes with their corresponding frequencies and a final summation rebuild the original time signal. This synthesis process is known as the Inverse Discrete Fourier Transform (IDFT).

Equation (2.2.4) presents the IDFT mathematical expression where the only difference with the DFT is a complex conjugation of the basis functions.

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X_k e^{j\frac{2\pi}{N}kn}, \tag{2.2.4}$$

Where $1/N$ corresponds to a scaling factor and N is the number of points. We can

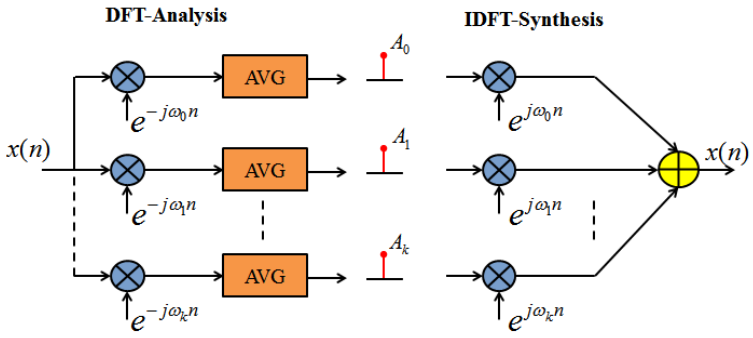

Figure 2.13: Analysis and synthesis representation of the DFT.

observe the same factor $e^{j\frac{2\pi}{N}kn}$ with opposite polarity in both, the DFT and IDFT. This factor is a set of roots in the unit circle and are known as the *twiddle factors* [11]. It represents a rotating vector in counterclockwise for the DFT and clockwise for the IDFT.

The DFT only processes data in a finite number of samples. Two main problems appear; spectral leakage and scalloping loss [9]. A sine time series evaluated from $-\infty$ to ∞ has a spectrum equal to a delta, as shown in the left side of figure 2.14. The DFT makes a truncation of the input signal which is equivalent to a multiplication with a rectangular function in time. In the frequency domain this is equivalent to a convolution of the sine spectrum with a sinc function. The spectrum gets spilled to adjacent bins. Windowing is a technique utilized to attenuate the sidelobes and avoid interference or wrong measurements in spectral analysis.

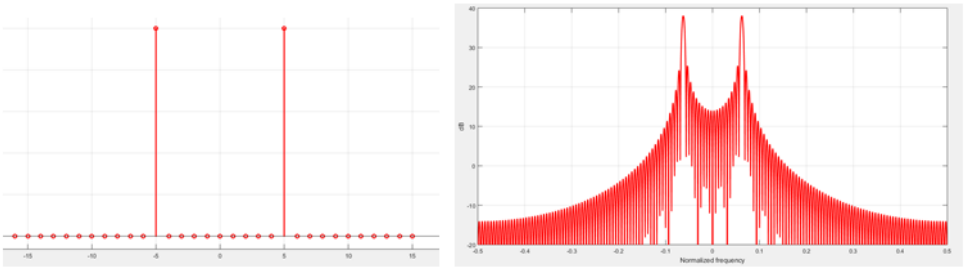

Figure 2.14: Spectral leakage.

When the DFT is computed to a time series of length N, an spectral vector of the same length is returned. The number of DFT points define the spectral resolution of

the signal. A low resolution causes scalloping loss in a signal, as shown in figure 2.15. If the main lobe of a sine spectrum falls between bins, a loss in amplitude appears. This can be overcome by increasing the spectral resolution or applying a flat window to the signal [12].

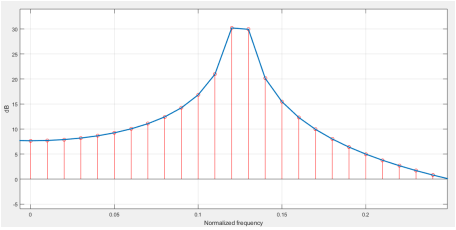

Figure 2.15: Scalloping loss in a sine spectrum.

The Fast Fourier Transform (FFT) is an algorithm which implements a Discrete Fourier Transform (DFT) in a way that the number of operations can be reduced from N^2 to $Nlog_x(N)$, where N is the number of operations and x is the radix. This is achieved by avoiding the redundancies in the twiddle factor due to periodicity and same values with opposite polarity [13].

Figure 2.16 shows a simple graphical description on how the IFFT works. The most simple explanation consists in a comparison with the tiles of a piano, where by touching a single tile a sound of specific frequency is emitted. Bin number 0 corresponds to DC component. Inserting a symbol in bin one corresponding to frequency one, will generate a sine wave with one cycle at the output, a symbol in bin 2, generates a two cycle sine wave and so on.

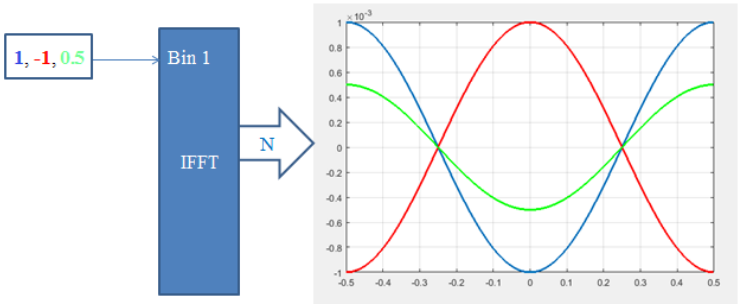

Figure 2.16: IFFT.

When the Inverse Fourier Transform (IFFT) is used in transmission data systems

like OFDM (Orthogonal Frequency Division Multiplexing), an integer number of cycles is very important to be taken into account to keep orthogonality. If the IFFT processes a signal, where the number of cycles is not an integer, as shown in figure 2.17, the signal will leakage to adjacent bins causing distortion and destroying orthogonality. In measurement applications like spectral analysis, an integer number of cycles is not necessary, spectral leakage is minimized by using some kind of window in the input time series.

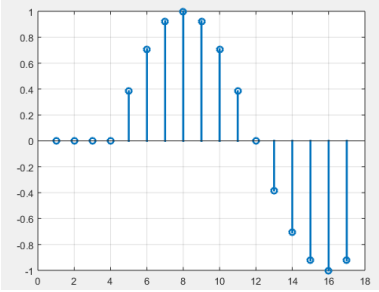

Figure 2.17: Sine wave with a non-integer number of cycles within the IFFT.

In practice, the FFT and IFFT can be implemented with the same algorithm, where by conjugating the input and output corresponding to the FFT, an IFFT is designed, as shown in figure 2.18.

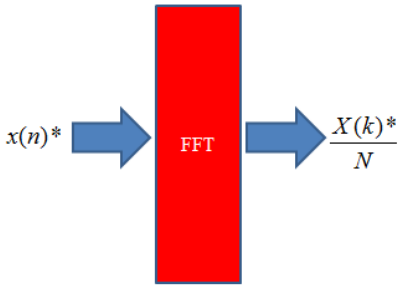

Figure 2.18: IFFT implemented using FFT algorithm.

Chapter 3

Orthogonal Frequency Division Multiplexing (OFDM)

In this chapter a description of OFDM, advantages and disadvantages are introduced. OFDM structure is described by blocks. Difference between transmitter and receiver due to Peak to Average Power Ratio (PAPR) is explained. A comparison between single-carrier and multicarrier OFDM is made according to PAPR values. Finally, a brief description of the physical and multiple access layer is given for Long-Term Evolution (LTE) networks.

3.1. Description

Orthogonal Frequency Division Multiplexing (OFDM) is a modulation scheme which can also be considered as a multiplexing technique. OFDM is a type of multicarrier system. OFDM generates in the transmitter a set of time orthogonal functions that are modulated in frequency domain, usually for QPSK or QAM subcarriers. As explained in Chapter two, a set of functions are considered orthogonal if their inner product is zero. OFDM uses sinc functions in the frequency domain which are overlapped every first zero crossing, as illustrated in figure 3.1. The sinc functions are located at every $\frac{2\pi}{N}k$, where N is the number of FFT points and $k = 0, 1, 2...N-1$.

The frequency sinc components are equal to complex sinusoids in time domain. Equation (3.1.1) represents the transformation from one domain to the other. The main block employed in OFDM is the Discrete Fourier Transform.

$$x_r(n) = \frac{1}{N}\sum_{k=0}^{N-1} X_r(k)e^{j\frac{2\pi k}{N}n}, \tag{3.1.1}$$

where N is the number of DFT points, k represents the corresponding modulating subcarrier, and r the corresponding OFDM symbol.

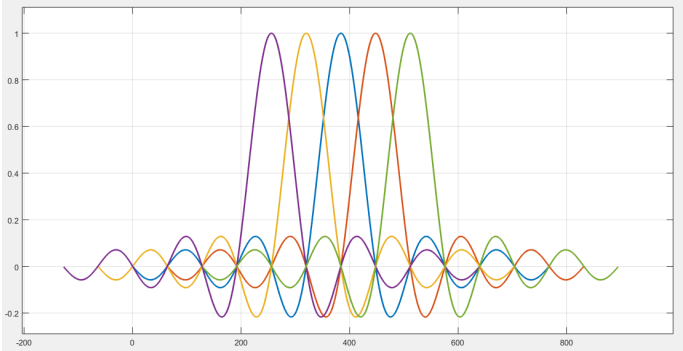

Figure 3.1: OFDM orthogonal sinc functions.

3.2. OFDM Structure

Figures 3.2 and 3.3 show the basic structure for an OFDM system.

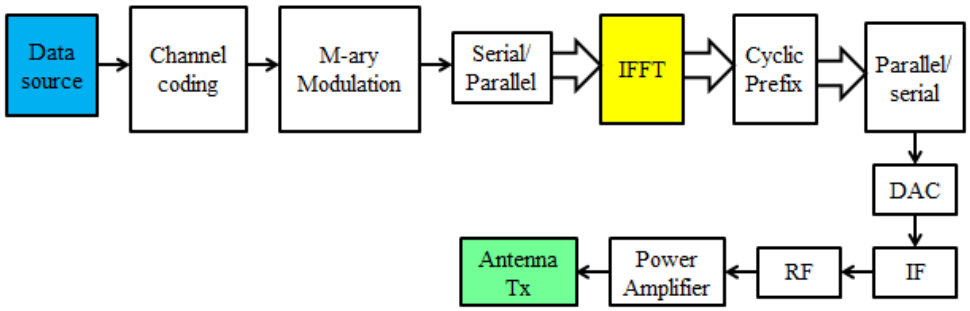

Figure 3.2: OFDM transmitter.

In the transmitter, binary data is generated from a data source which is encoded by adding redundant bits to diminish the probability of bit errors in the channel. An M-ary alphabet is chosen to map the bits to different phases. Typic modulation formats are QPSK and 16-QAM. Symbols are passed through serial to parallel block to be inserted in the IFFT block. After the IFFT block, groups of symbols are formed to get an OFDM symbol N times the M-ary symbol period. Every OFDM symbol has a number of subcarrier, where a copy of one quarter of these subcarriers is appended

at the beginning of every OFDM symbol to avoid Inter-Symbol Interference (ISI). Parallel to serial block is used again to have a symbol stream at the input of the digital to analog converter (DAC). The symbol stream called composite signal is passed through the IF and RF stages to apply the final upconversion process and through the power amplifier to be transmitted by the antenna. In the receiver side, the dual process is applied, so knowing how the transmitter works is sufficient.

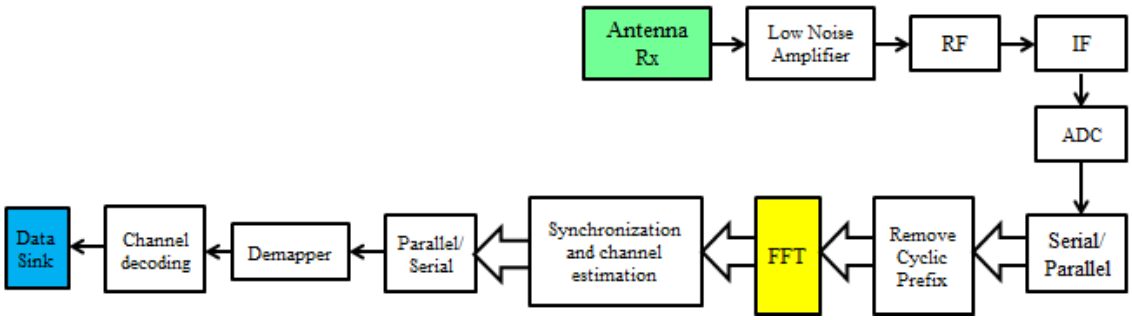

Figure 3.3: OFDM receiver.

3.3. Peak to Average Power Ratio

As mentioned before, the IFFT converts a complex input into sines and cosines which are send through in-phase and quadrature channels and then summed to form a complex exponential output. The I/Q channels present data with a Gaussian distribution $x = N(0, \sigma^2)$, $y = N(0, \sigma^2)$ where the magnitude is Rayleigh distributed.

$$R = \sqrt{x^2 + y^2}. \tag{3.3.1}$$

Peak to Average Power Ratio, consists in the superposition of a maximum of N low rate complex exponential signals $s(k)$ at different frequencies.

$$PAPR = \frac{max(|s(k)^2|)}{\frac{1}{N}\sum_{k=0}^{N-1}|s(k)^2|}. \tag{3.3.2}$$

High PAPR is generally undesirable as it leads to poor efficiency in the Power Amplifier (PA). High amplitude levels in the composite signal, may cause the PA to pass from the linear region to the non-linear region. When this happens, out and

in band undesirable components known as harmonic and intermodulation distortion THD and IMD appear.

In the transmitter side, N points in frequency (bins) are transformed in time by the IFFT as sine wave subcarriers of different frequencies which are summed forming a composite signal to be transmitted, as shown in figure 3.4. In this case, we can observe a high value in amplitude of 5.5 in the composite signal.

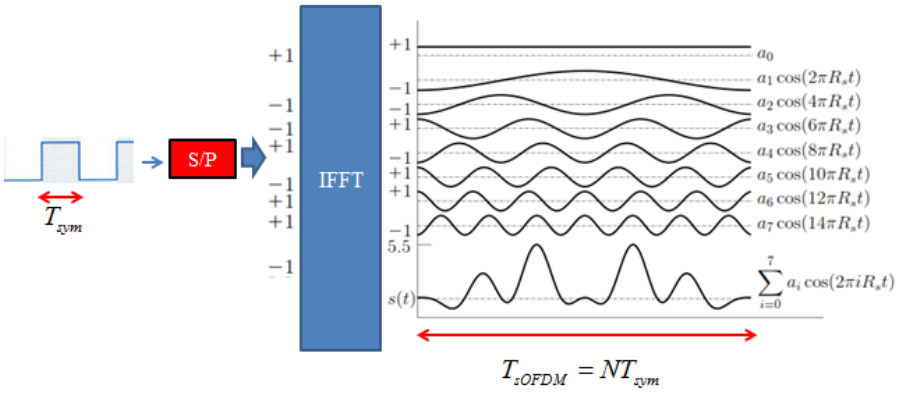

Figure 3.4: IFFT modulation [1].

3.4. Benefits and Problems

OFDM uses orthogonal functions which are overlapped in the frequency domain. This represents a significant increase in spectral efficiency compared to a typical FDM (Frequency Division Multiplexing) signal, as shown in figure 3.5.

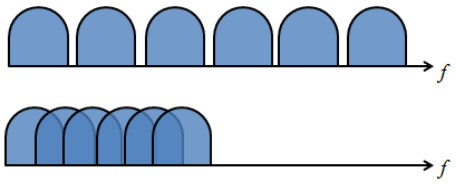

Figure 3.5: FDM (top) and OFDM (bottom) comparison .

To overcome frequency selective fading channels, a copy of the last quarter of every OFDM symbol is appended at the beginning; this is known as *cyclic prefix* (CP). The

appended CP converts the linear convolution between the transmitted signal and the channel into a circular convolution. Therefore, in the frequency domain, this results in a simple multiplication, which is of great advantage in multicarrier systems to estimate the channel with just a single tap equalizer. In addition, CP is inserted within a guard interval in time domain. This reduces the effects of Inter-Symbol Interference (ISI).

However, OFDM presents two main disadvantages: PAPR and high sensitivity to frequency offset [14]. As the number of subcarriers in the transmitter side increases, the IFFT generates high amplitude values at the output. This is due to the fact that IFFT makes a superposition in time domain of all subcarriers to generate a composite signal. High amplitude values provoke high PAPR which causes the Power Amplifier (PA) to work in a non-linear region, thus reducing its efficiency. Doppler shift and mismatching between local oscillators in the transmitter/receiver cause Carrier Frequency Offset (CFO) between subcarriers which destroys the orthogonality, as shown in equation (3.4.1).

$$X(k) = \sum_{k=0}^{N-1} r(n) e^{j\frac{2\pi(k+\varepsilon)}{N}n}, \tag{3.4.1}$$

where $r(n)$ is the received signal in time after the FFT, $X(k)$ is the received signal in frequency and ε corresponds to the offset in frequency. CFO is a big problem in OFDM because subcarriers are so close and any offset may cause frequency overlapping or a wrong location in their frequency subcarrier, distorting the data.

3.5. Single Carrier OFDM

PAPR is of great concerning in devices where the power must be saved as much as possible like in mobile communications. In the downlink, the transmitter is designed using ordinary OFDM and we need not to worry about power consumption due to the BS is always connected to the AC source. In the uplink, special attention must be payed to the transmitter due to the power source for the MS comes from a battery in a very reduced space. In order to diminish PAPR an alternative modulation scheme is used called single carrier OFDM. In this system, an extra modulation DFT block is added before the IFFT. The system is similar to any single carrier transmission but with the difference that, the symbols are made periodic, thus having a circular convolution in order to achieve an easier equalization in frequency like in ordinary

OFDM. The symbol period is N times shorter than in ordinary OFDM and the spectrum is N times wider. It is known that a single carrier needs pulse shaping so an upsampling process is necessary to increase the sampling rate and relax the analog filter requirements after the DAC. The upsampling process is carried out by increasing the register size in frequency L times (zero padding), where L is the upsampling factor, then interpolation is accomplished by default for a rectangular window embedded in the IFFT. Figure 3.6 shows an example of implementation with $L = 2$.

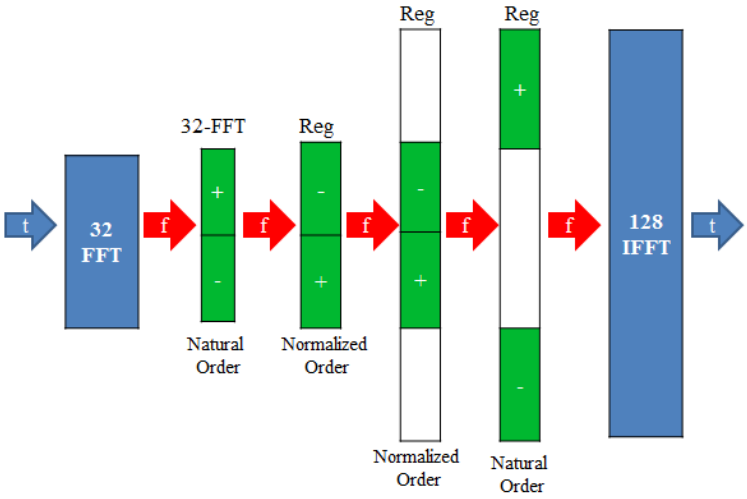

Figure 3.6: Single Carrier OFDM Implementation [2].

Figure 3.7 shows the improvement achieved in PAPR by using a single carrier OFDM transmission scheme versus ordinary OFDM. A general comparison between single carrier and ordinary OFDM is presented in Table 3.1.

OFDM	SC-OFDM
Multi-Carrier	Single-Carrier
Frequency domain detection	Time domain detection
Time symbols expanded	Symbols compressed into smaller chips
Parallel transmission of the data blocks	Serial transmission of the data blocks
	Similar to CDMA
High PAPR	Low PAPR

Table 3.1: Main differences between OFDM and SC-OFDM.

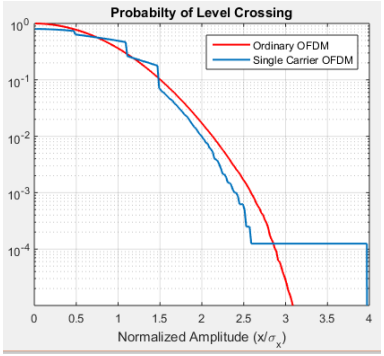

Figure 3.7: PAPR Comparison between ordinary OFDM (red) and single carrier OFDM (blue).

3.6. Physical Layer and Multiple Access

Physical layer (PHY) corresponds to the lowest level defined by the Open Systems Interconnection Model (OSI model). This layer defines the modulation scheme, synchronization, equalization, channel estimation, among others. The Media Access Control (MAC) layer, defines the multiple access technique, addressing, scheduling and allocation of the users in the different available channels for the shared medium.

Orthogonal Frequency Division Multiple Access (OFDMA) is the multiplexing technique used in LTE. Every user is assigned to a number of subcarriers in an FFT for a certain period of time. Time-frequency block assignments are called Physical Resource Blocks (PRBs). They consists of 6 or 7 OFDM symbols for long and short cyclic prefix respectively, with 12 subcarriers per OFDM symbol, transmitted in one slot of time. An LTE frame has a duration of 10ms, it is divided in 10 subframes of 1ms. Every subframe is partitioned in two slots of time with a duration of 0.5ms [15]. Figure 3.8 shows the frame time partition.

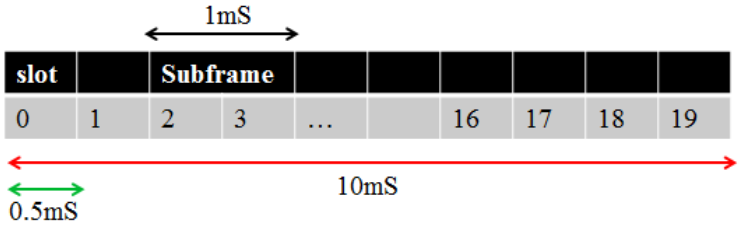

Figure 3.8: LTE frame.

LTE channels may vary from 1.2MHz to 20MHz with 128-FFT to 2048-FFT respectively. For all channel width, subcarrier spacing is always of 15KHZ. For a 2048-FFT, the clock corresponds to f_s =15KHz(2048) = 30.72MHz, where the symbol duration corresponds to $1/f_s$ = 32.55ns, as shown in figure 3.9.

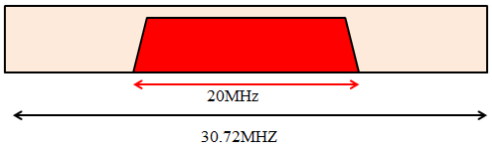

Figure 3.9: LTE bandwidth for a 2048-FFT.

To set a communication link between BS and MS, the MS must first recognize the cell by sending a random preamble, the BS responds by assigning a random sequence for allocation of the user in a PRB. Different users that wish to establish a link with the BS must be time synchronized by delaying and advancing the users depending on the distance between the MS and BS. Frequency Division Duplex (FDD) and Time Division Duplex (TDD) are supported. For FDD, users are added in the wireless channel. For correct demodulation, users must arrive at the same time to the BS despite their location, as shown in figure 3.10

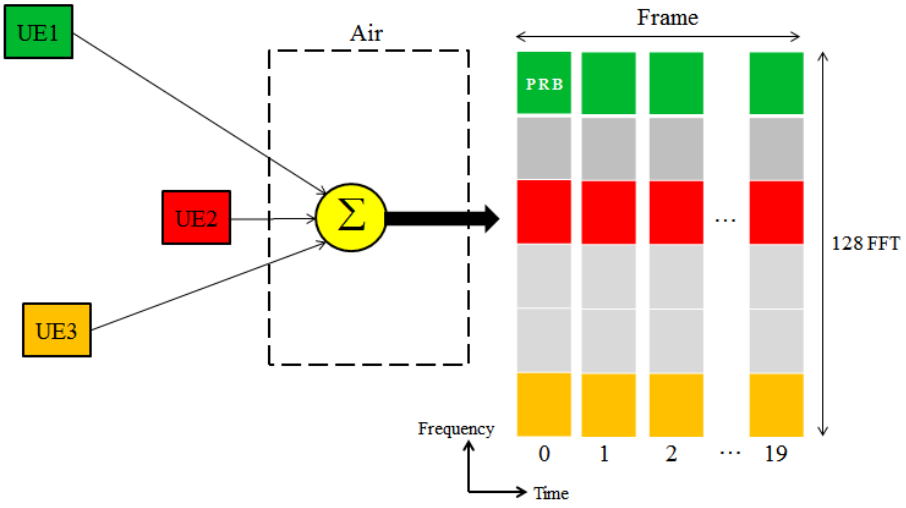

Figure 3.10: Uplink transmission scheme for LTE random access.

Chapter 4

Channelization

First, what is a channelizer and efficient implementation of using polyphase filter banks is explained step by step. A review of the most outstanding current methods in OFDM channelization is presented. Finally a design of arbitrary sampling rate different from the number of channels in the synthesis/analysis DFT polyphase filter bank channelizer is presented.

4.1. What is a Channelizer?

A *channelizer* is a system that inserts (in the transmitter side) or extracts (in the receiver side) channels from a composite signal. A typical block diagram for a digital receiver consists of an RF downconverter, Analog to Digital Converter (ADC) and a Digital DownConverter (DDC), as shown in figure 4.1.

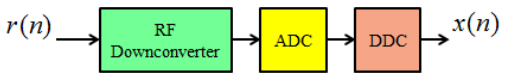

Figure 4.1: Basic blocks for a digital receiver.

In the first generation of DSP-based receivers, a set of these digital receivers connected in parallel form a *channelizer*, as shown in figure 4.2.

The transmitter channelizer is the reverse of the receiver. The composite N channels signal generated for the transmitter channelizer, is downconverted, filtered and downsampled to extract each individual channel by the receiver channelizer. The RF downconverter consists of different stages that converts the RF input signal to Intermediate Frequency (IF) or baseband by means of local oscillators (LO). When the

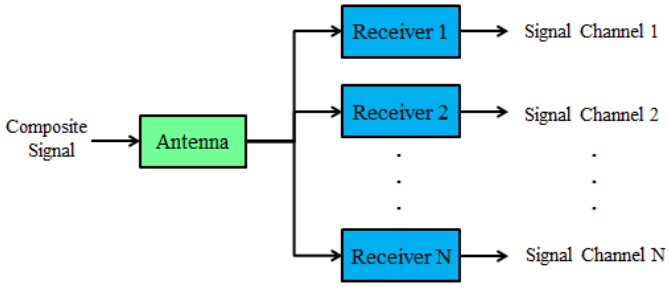

Figure 4.2: N Channels formed from N parallel receivers.

input RF signal passes from an RF band to baseband, the receiver is known as an homodyne receiver. When it passes from RF to IF, it is called an heterodyne receiver [16]. After the ADC, the DDC is in charge of converting the input composite signal to baseband by using a Direct Digital Synthesizer (DDS). The DDS selects a channel and a low pass filter attenuates the undesired frequency components. Finally, a downsampler reduces the sampling rate for congruence with the reduced bandwidth. This process is shown in figure 4.3.

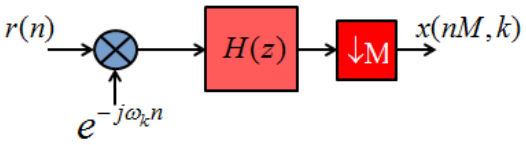

Figure 4.3: Basic blocks for a digital downconverter.

To see how the channelizer works, figure 4.4 shows a composite signal spectrum with only 3 channels. Each channel is located at sub-multiples of the sampling rate $k\frac{f_s}{N}$, where N is the number of channels and k is the location at each channel, $k = 0$ corresponds to the DC channel.

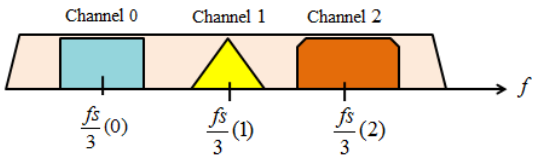

Figure 4.4: Three channels composite signal spectrum.

To extract channel number one, an heterodyne process is carried out by a DDS, then a digital low pass filter attenuates the adjacent channels, as shown in figure 4.5.

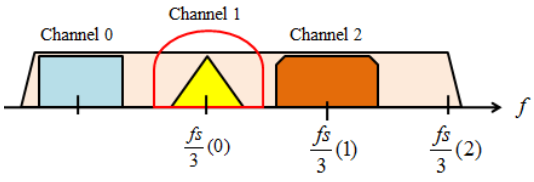

Figure 4.5: Heterodyned signal.

Figure 4.6 shows the extracted channel.

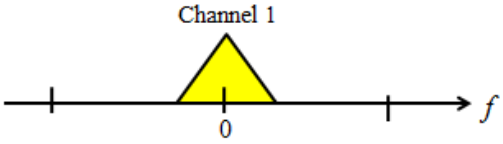

Figure 4.6: Extracted channel.

4.2. Channelizer Design

When a legacy copy of an analog implementation is taken to the digital domain, all the problems are also carried out. The first problem that can be observed in the digital receiver shown in figure 4.3 is due to the downsampler is located after the digital low pass filter. Only every M sample is retained while the others are discarded by the downsampler which is a waste of processing. By invoking the *equivalence theorem* [3], the DDS can be placed to the right side of the lowpass filter, but this must be replaced by a bandpass filter, as shown in figure 4.7.

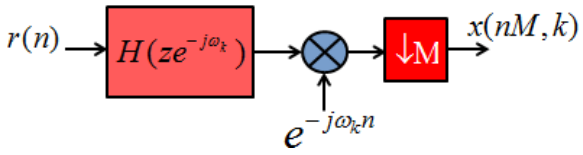

Figure 4.7: Equivalence theorem applied to the heterodyne receiver [3].

The aliasing effect due to a change in sampling rate is equivalent to a shift in frequency of the spectrum. An arbitrary spectral shift can be made with the downsampler, thus the heterodyne process using a DDS becomes superfluous. Figure 4.8 shows the receiver for a single channel.

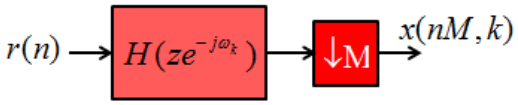

Figure 4.8: Improved heterodyne receiver.

The single channel receiver shown in figure 4.8 is basically a decimator filter.To avoid unnecessary processing of the signal, the position of the bandpass filter and downsampler can be interchanged. However, it can not be made directly because it violates the Nyquist sampling theorem. In Chapter 2 an efficient implementation for a decimator using polyphase filters was explained. The cascade connection of Synthesis/Analysis filter bank forms a transmultiplexer which is basically a channelizer, as shown in figure 4.9.

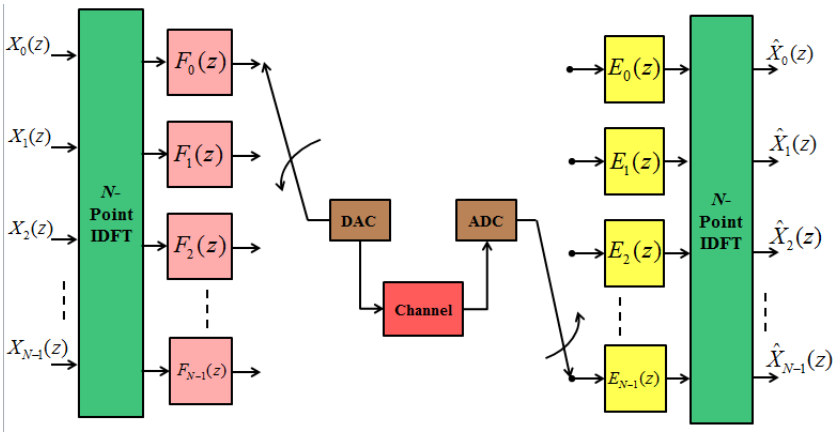

Figure 4.9: Synthesis/Analysis filter bank transmultiplexer implemented as a channelizer [3].

The number of DFT points N defines the number of channels embedded on the composite signal. The prototype filter defines the bandwidth of the channel and the upsampling/downsampling factors L, M the output sampling rate per channel. When the number of channels equals to the downsampling factor, $N = M$, the channelizer is based on a Maximally Decimated Filter Bank (MDFB). This means that the channel

bandwidth B, channel spacing p and output sampling rate per channel f_o are equal to fs/M, the system is critically sampled [4], as shown in figure 4.10.

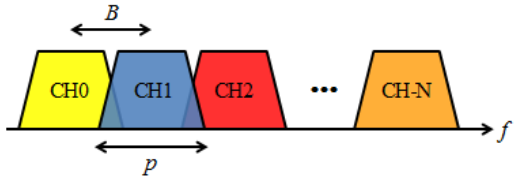

Figure 4.10: Channelizer composite signal.

Maximally decimated filter banks imposes restrictions and flexibility in subsequent processing stages in the channels. When a channel is extracted after the analysis bank, aliasing occurs in the transition bands, as shown in figure 4.11.

Figure 4.11: Extracted channel 0 from critically sampled system [4].

A practical channelizer needs an output sampling rate kf_0, as shown in figure 4.12. This is achieved by oversampling the transmultiplexer filter bank. Section 4.4 introduces a modification made to the channelizer in order to have oversampling in every channel.

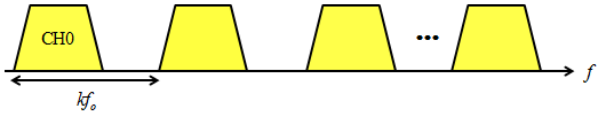

Figure 4.12: Extracted channel 0 from a non critically sampled system [4].

4.3. Review of Methods

Current research in channelizers, aims to design a system to overcome the main disadvantages presented in OFDM; high PAPR, spectral leakage and synchronous

multiplexing. Multicarrier and single carrier design variations in OFDM are investigated. Multicarrier methods usually employ filter banks with a high order prototype filter to isolate the different users that are located in the IFFT bin subcarriers in order to achieve asynchronous multiplexing and reduce spectral leakage to avoid Inter Carrier Interference (ICI). In addition, the flat response of the filter avoids scalloping loss in the subcarrier signal [17]. Figure 4.13 presents a comparison between an FFT subcarrier in ordinary OFDM and a subcarrier isolated by using a high order filter.

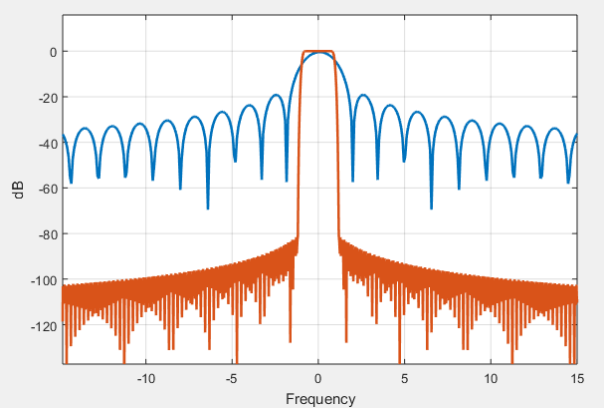

Figure 4.13: Ordinary OFDM subcarrier (blue) and high order filter isolation (red) in frequency.

The most prominent multicarrier systems to date are: Universal Filtered Multi-Carrier (UFMC), Filter Bank Multi-Carrier (FBMC), Generalized Frequency Division Multiplexing (GFDM) and Weighted Overlap and Add (WOLA).

FBMC presents a high spectral efficiency in the transmission due to it permits an overlapping of all subcarriers, as shown in figure 4.14.

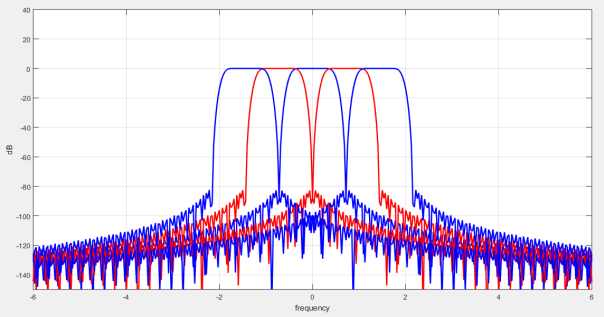

Figure 4.14: Frequency subcarrier overlapping in FBMC.

It is considered an non-orthogonal transmission [18]. To avoid distortion between subcarriers, FBMC uses Offset Quadrature Amplitude Modulation (OQAM).

Overlapping is achieved by extending the IFFT kM where k represents the oversampling factor and M the input data to the IFFT. In phase and Quadrature data is divided in odd and even indexes, as shown in figure 4.15. Real and imaginary parts are not transmitted simultaneously by interleaving and applying a delay equivalent to half the data length. This permits a frequency phase offset in adjacent overlapping subcarriers and thus avoiding distortion.

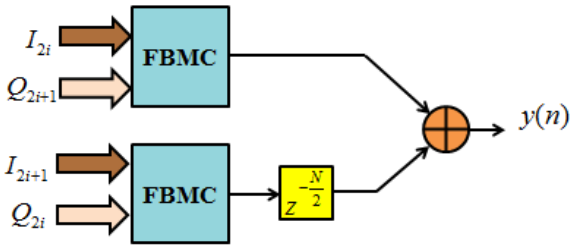

Figure 4.15: FBMC block diagram with OQAM modulation.

FBMC can be efficiently implemented by using polyphase filter banks, however it results complex due to OQAM, in addition, MIMO cannot be easily adapted as in OFDM. UFMC overcomes the main problems in FBMC by splitting the data in order to carry out a subband filtering. The data is usually divided in a set of subcarriers equal to a Physical Resource Block (PRB) in LTE, as shown in figure 4.16.

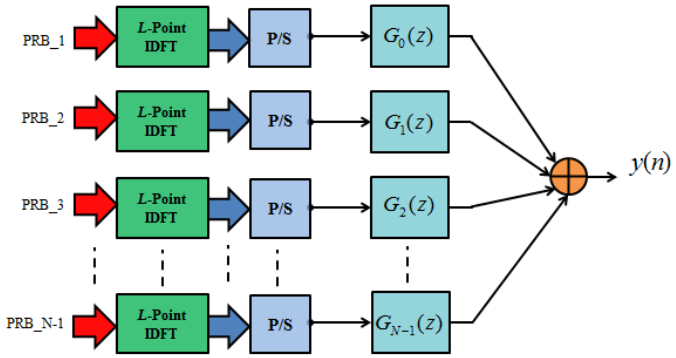

Figure 4.16: UFMC block diagram.

This allows to implement low order filters compared to FBMC. Data can be sent

in short burst transmissions with low latency [19]. Cyclic prefix is not used which increases the spectral efficiency, however ISI occurs. A comparison in more detail between FBMC and UFMC can be found in [20].

GFDM is similar to FBMC but with the difference that processing per OFDM blocks is made. In ordinary OFDM every symbol is appended with a CP, UFMC groups a number k of OFDM symbols and append a CP to the block instead of each OFDM symbol [21].

A similar system to DFT filter bank that uses an overlap and add technique is WOLA. Unlike the DFT filter bank channelizer introduced in Section 4.2, the number of channels in WOLA systems is different from the resampling factor M, this allows great flexibility to the channelizer. WOLA uses a weighting filter instead of a convolution filter by means of a Short Time Fourier Transform (STFT) [22]. The window applied to the input signal is seen as an stationary process, thus unlike DFT filter bank where the prototype filter is shifting, in WOLA systems the input signal is shifting. The processing data in WOLA is as follows: the input data M must be k times the FFT size N. Data is weighted in time by the filter $g(n)$, then, data is divided in blocks of N samples which are overlapped, added and stored in a register of size N. The IFFT transforms the overlapped data and a subsequent heterodyne process is achieved for translating to the desired channel frequency band. The WOLA block diagram is shown in figure 4.17. It can be observed that the channelizer size and the resampling factor are both independent [23].

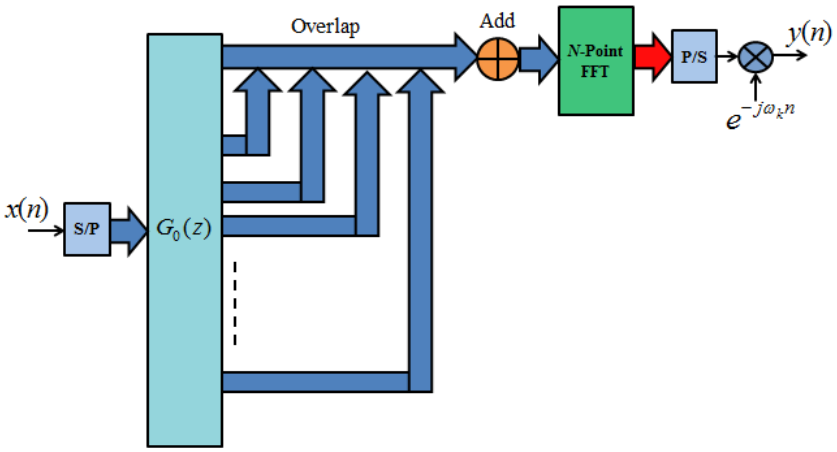

Figure 4.17: WOLA block diagram.

In the case of single carrier systems, they are mostly employed in the uplink transmission for high energy efficiency. A variation of the single carrier OFDM system presented in Chapter three called Shaped Single Carrier OFDM [2], reduces significantly PAPR by applying spectral filtering. This permits to apply high order modulation schemes in OFDM in order to increase data rate in the uplink transmission.

4.4. Non Maximally Decimated Channelizer

The channelizer designed with DFT polyphase filter banks presented in Section 4.2 has a fixed equal number of channels and downsampling/upsampling factors. It can be observed that the channelizer is composed of a filter bank, IFFT and a commutator that work independently. The filter bank defines the channel bandwidth, the IFFT defines the Nyquist zone of the channel and the commutator the output sampling rate of the channel. The commutator can be modified in order to have an arbitrary sampling rate that is different from the number of channels that are defined by the IFFT size. This is known as a Non-Maximally Decimated Filter Bank (NMDFB) [4].

In the analysis part, the channelizer processes every M input samples and outputs only one sample, thus having an output sampling rate of f_s/M. The downsampling factor M is fixed and defined by the number of polyphase components. The commutator can be modified in order to have an arbitrary factor L that permits a variable sampling rate at the output of every channel. This can be achieved by taking every L/M samples at the input instead of M. The commutator is normally located at position $N-1$ and inserts samples until the 0 position. For a 64 path analysis channelizer, the output sampling rate is $1/M = 1/64$, if an output sampling rate of $1/48$ is desired, L needs to be computed considering M is fixed as follows:

$$\frac{L}{M} = \frac{L}{64} = \frac{1}{48}. \tag{4.4.1}$$

$$L = \frac{64}{48} = \frac{4}{3}. \tag{4.4.2}$$

The commutator must be placed at position $M/L - 1 = 47$. However, if every 48 samples are inserted, the output signal will be distorted. From a one dimensional filter perspective, the input samples are shifted 48 samples at every cycle. This is equivalent to a serpentine shift in the two dimensional polyphase form. To achieve

this serpentine shift an input circular buffer (SS) is needed before the polyphase filters [3]. The serpentine shifting data buffer can be observed in figure 4.18.

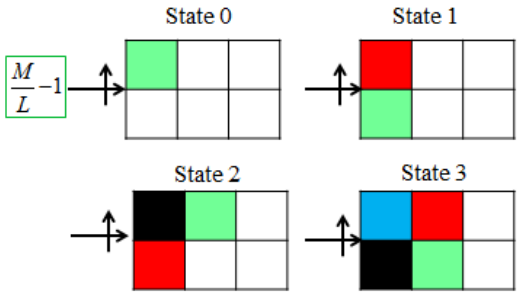

Figure 4.18: Serpentine shift circular buffer [3].

The modification in the input data causes a time offset in the polyphase filters which mismatch the origin of the IDFT. In order to fix this offset a circular phase correcting buffer (PC) is needed after the polyphase filters [3]. The complete block diagram for the modified receiver channelizer is shown in figure 4.19.

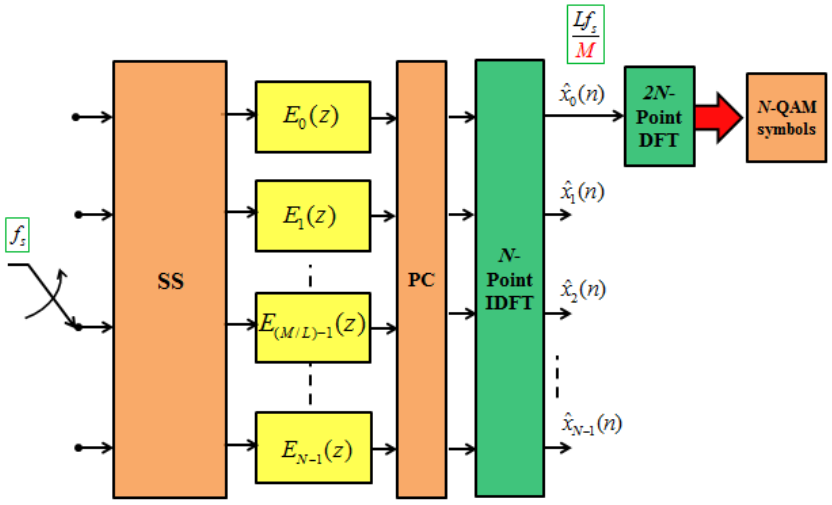

Figure 4.19: NMDFB receiver channelizer [3].

In the synthesis part for every 1 input sample, the channelizer outputs L samples. The upsampling factor L is fixed and defined by the number of polyphase components, but carried out by the IDFT. The commutator can be modified in order to have an arbitrary factor M that permits a variable sampling rate at the output of every

channel. This can be achieve by taking every L/M samples at the output instead of L. Unlike the transmitter channelizer, the commutator position must be located at $L/M - 1$. The same correcting circular buffers are needed but in reverse flow. The complete block diagram is shown in figure 4.20.

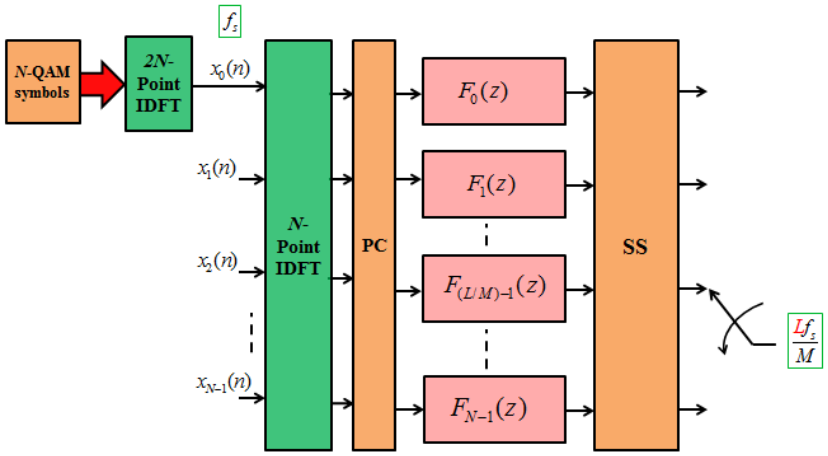

Figure 4.20: NMDFB transmitter channelizer [3].

It can be observed that in order to have an oversampled channel data, the DFT after the modulated QAM data, must be k times bigger than the IDFT channelizer size. The whole information about the Non-Maximally Decimated Channelizer exposed in this section was taken from [3] in order to be analyzed, simulated and implemented in FPGA.

Chapter 5

Polyphase Complementary Code Keying

In this chapter, the process of generating complementary codes is explained. Complementary codes with polyphase implementation is introduced for QPSK coding. Transmitter and receiver filter structures are presented for Complementary Code Keying (CCK) implementation. Decoding techniques with matched filter structure and phase rotators is explained.

5.1. Complementary codes

It is common to spread and compress the data to be transmitted in order to achieve a better performance. Data is usually spread in frequency by sending repeated bits in order to operate in noisy environments and avoid jamming distortion. Figure 5.1 shows the basic code/decode block diagram in communications systems. The transmitter spread the data and the receiver compresses in order to recover the original bandwidth, this is usually achieved by using a correlation technique.

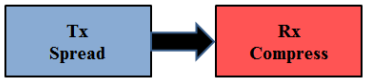

Figure 5.1: Simplified code scheme.

As mentioned in Chapter three, in OFDM systems, PAPR is of great concerning. Signals can reach high values that make the PA to operate in the non-linear region. This problem is addressed by using Golay complementary codes extended to non-

binary data. Complementary codes have the special property that the sum of their autocorrelations equals to an impulse in zero [24], similar to white noise. To generate the pair of complementary codes, initial values known as kernel, are commonly assigned as $A = 1, B = 1$. Then a recursion method shown in equation (5.1.1) is applied.

$$\begin{aligned} A(n+1) &= [A(n)B(n)] \\ B(n+1) &= [A(n)\bar{B}(n)]. \end{aligned} \tag{5.1.1}$$

In order to have a 2^N length code, N iterations must be made. Figure 5.2 shows the auto-correlation for a 256 length code which requires 8 iterations per code.

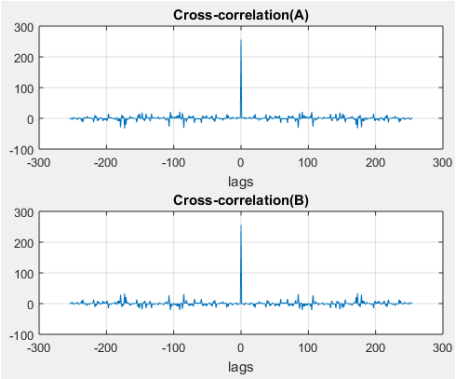

Figure 5.2: Autocorrelation of A (top) and B (bottom).

Every point of the auto-correlation pair has equal magnitude and opposite polarity, thus when summed, an impulse in zero is generated, as shown in figure 5.3.

Complementary codes have a constant spectrum which is of great interest. They can be applied to the in-phase and quadrature components in the transmitter and then transformed to the time domain. The time series after IFFT have a constant envelope and thus a reduction in PAPR is achieved. Basically an inversion of the domains is made by applying the codification in the frequency domain, as shown in figure 5.4.

Nevertheless, Golay complementary codes are applied to binary data, so an extension to non-binary data must be made. To achieve this, a set of phase rotators, as shown in figure 5.5 is applied to each stage of an all pass network which is in charge

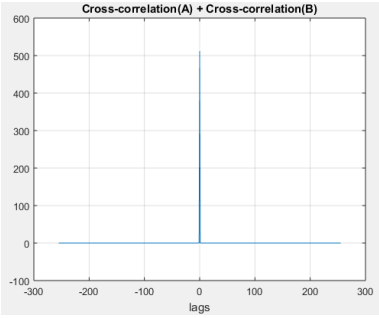

Figure 5.3: Sum of autocorrelation of A and B.

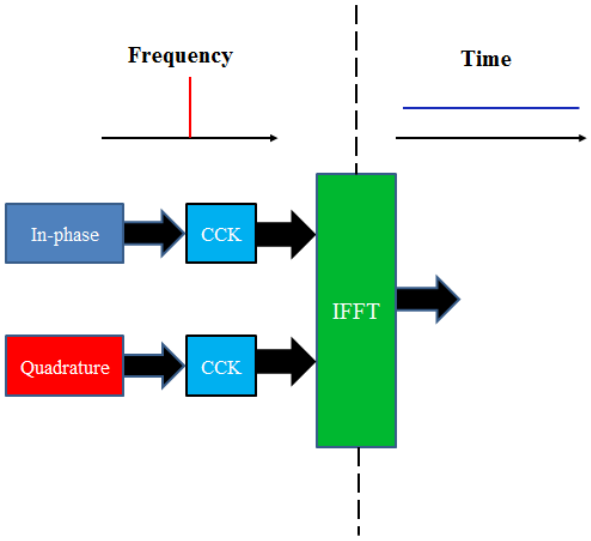

Figure 5.4: Constant frequency property of CCK applied in time to I/Q components before IFFT.

of generate the binary codes.

For a QPSK codification, these phase rotators correspond to the four different phases of the QPSK modulation. This structure has 3 stages to generate 2^N length polyphase codification, where $N = 3$, thus the number of iteration to generate a code by recursion equals to the number of stages.

5.2. Decoding Techniques

To compress the signal and recover the original data at the receiver, an inverse structure which is equivalent to a matched filter is designed. Figure 5.6 shows this

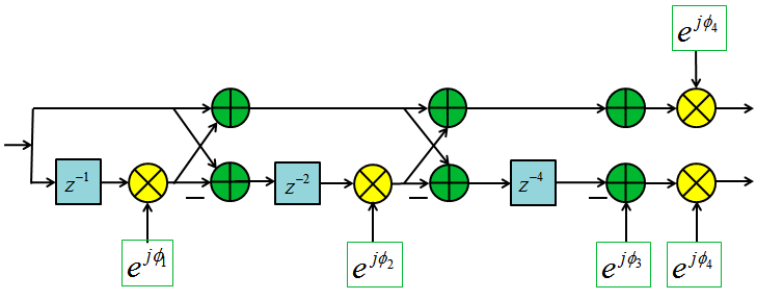

Figure 5.5: Three stage polyphase complementary code transmitter for 8-length codification [5].

structure. Every rotator is the conjugate of those from the receiver. The data flows in the opposite direction than in the transmitter, passing through every rotator with descending index.

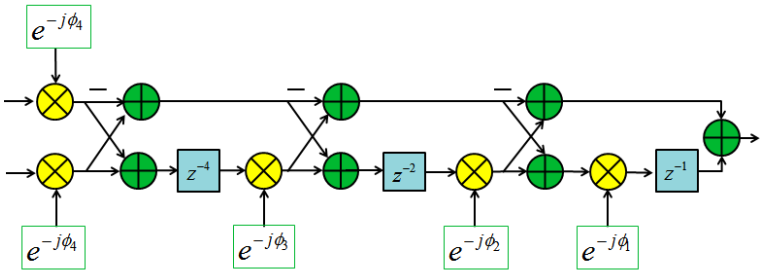

Figure 5.6: Three stage matched filter decoding [5].

A similar decoding technique is shown in equation (5.2.1), where the phases are recovered by multiplying the conjugated coded phases and averaging phase differences between pair carriers [25].

$$\begin{aligned}
\phi_1 &= \theta_0\bar{\theta}_4 + \theta_1\bar{\theta}_5 + \theta_2\bar{\theta}_6 + \theta_3\bar{\theta}_7 \\
\phi_2 &= \theta_0\bar{\theta}_2 + \theta_1\bar{\theta}_3 + \theta_4\bar{\theta}_6 + \theta_5\bar{\theta}_7 \\
\phi_3 &= \theta_0\bar{\theta}_1 + \theta_2\bar{\theta}_3 + \theta_4\bar{\theta}_5 + \theta_6\bar{\theta}_7 \\
\phi_0 &= \theta_3\bar{\phi}_3 + \theta_5\bar{\phi}_2 + \theta_6\bar{\phi}_1 + \theta_7.
\end{aligned} \tag{5.2.1}$$

Phase zero recovering is different from the other due to it is common to all sub-carriers, thus differential detection is applied.

Chapter 6

CCK OFDM Channelizer

First, an ordinary OFDM modulator is designed. Secondly, a 64 channelizer is designed with a rational sampling rate $M/2$. An adaptation of the CCK OFDM modulation is made to the channelizer. Frame detection, phase, frequency and channel estimation algorithms are applied to the channelizer.

6.1. CCK in OFDM Transceivers

First, an ordinary OFDM modulator is designed. A normalized 64-QAM and QPSK random generator inserts 54 symbols at the input of a 128 IFFT, leaving bin 0 corresponding to DC in a zero value to avoid distortion due to DC offset. The last quarter part of each OFDM symbol is copied to the beginning of the symbol to form the cyclic prefix. A frame of 50 OFDM symbols of size $128 + 32 = 160$ is designed. Figure 6.1 shows the corresponding time-frequency OFDM signal.

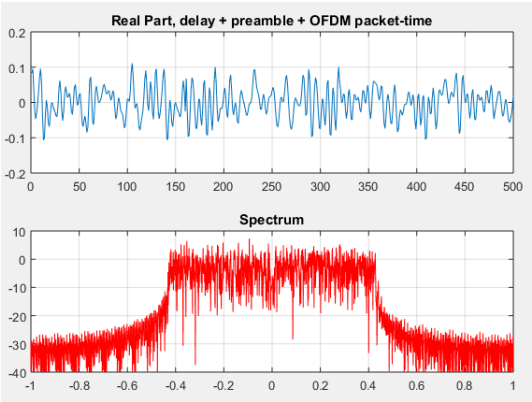

Figure 6.1: Time and frequency representation for QPSK and 64-QAM in ordinary OFDM modulation.

An OFDM modulator receives every OFDM symbol, discards the cyclic prefix and demodulates with a 128-FFT. Figures 6.2 and 6.3 show the real part of the demodulated signal and its corresponding constellation, note that no channel distortion, frequency, phase or time offset is present.

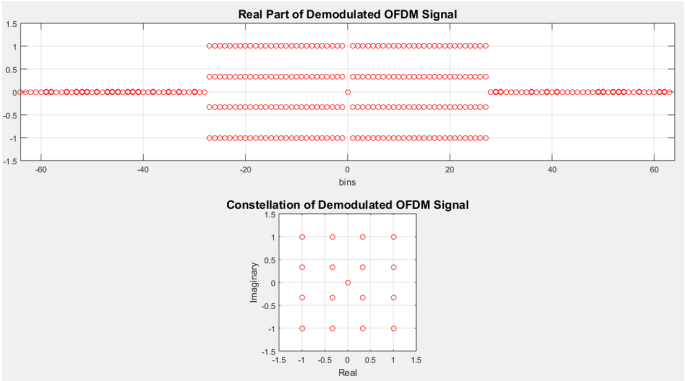

Figure 6.2: Real (up) and complex (down) overlapping of 16QAM symbols in frequency domain.

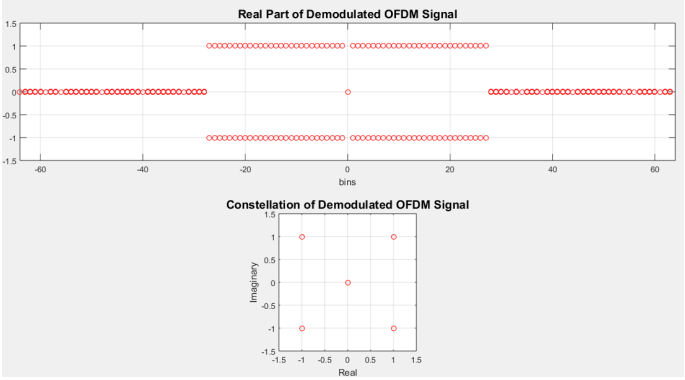

Figure 6.3: Real (up) and complex (down) overlapping of QPSK symbols in frequency domain with no distortion.

CCK encoding for an OFDM signal is carried out by generating an nxm matrix where n is the length of the code and m corresponds to the number of phases. Equation (6.1.1) shows an 8-length code matrix for a 4 phases QPSK signal [5], the extra phase π corresponds to the phase of the sign reversal in the implemented filter.

$$\begin{bmatrix}\theta_0\\ \theta_1\\ \theta_2\\ \theta_3\\ \theta_4\\ \theta_5\\ \theta_6\\ \theta_7\end{bmatrix} = \begin{bmatrix}0 & 0 & 0 & 1 & 0\\ 1 & 0 & 0 & 1 & 0\\ 0 & 1 & 0 & 1 & 0\\ 1 & 1 & 0 & 1 & 1\\ 0 & 0 & 1 & 1 & 0\\ 1 & 0 & 1 & 1 & 0\\ 0 & 1 & 1 & 1 & 1\\ 1 & 1 & 1 & 1 & 0\end{bmatrix} \begin{bmatrix}\phi_1\\ \phi_2\\ \phi_3\\ \phi_4\\ \pi\end{bmatrix}. \tag{6.1.1}$$

Every column corresponds to a binary Golay sequence. First, a single sequence is generated by recursion, as explained in equation (5.1.1); the others are derived from the first one by time reversing, complementing or inverting one or both codes at each iteration. Figure 6.4 presents the constellations for uncoded and encoded QPSK symbols. The encoded symbols are located in a circumference with equal magnitude and equal phase spacing.

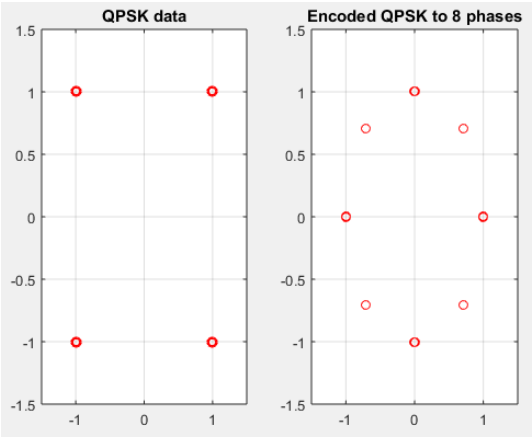

Figure 6.4: QPSK symbols and CCK encoding.

As mentioned in section 4.2, the main advantage of CCK encoding is the reduction in PAPR; it keeps a constant value of 1.41 and an incredible stability unlike other PAPR reduction techniques. Figure 6.5 shows the corresponding histogram and probability distribution function for PAPR.

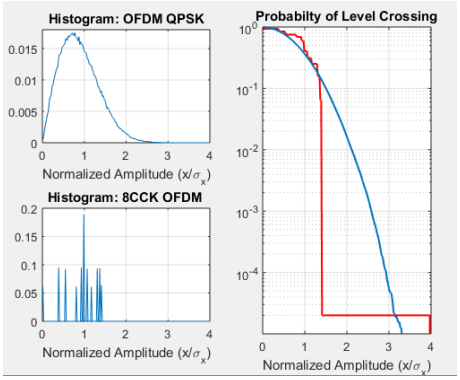

Figure 6.5: Ordinary and CCK OFDM PAPR comparison.

The encoded signal in time keeps a peak value of 0.25 and average of 0.16. The corresponding encoded QPSK demodulated signal is shown in figure 6.6. It can be observed that symbols keep a constant unity magnitude and equidistant phase.

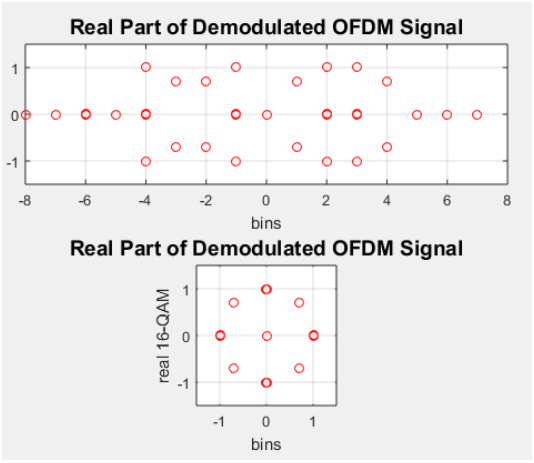

Figure 6.6: Demodulated encoded QPSK signal.

The trade-off for a PAPR reduction using CCK corresponds to an increase in code rate. For an 8-length coding corresponding to four phases, the code rate equals to 1/2. For a 16-length coding corresponding to five phases, the code rate equals to 5/16 and the PAPR reduction is similar for an 8-length coding. Therefore, increasing the number of phases to be mapped corresponds to an increase in code rate of $\frac{p}{2^{p-1}}$ where p is the number of phases, thus increasing the code length is not a good trade-off for PAPR. An alternative to alleviate high code rate is by partitioning in groups

of 4 symbols to be encoded into 8 phases [26]. Figure 6.7 shows a partition in two groups.

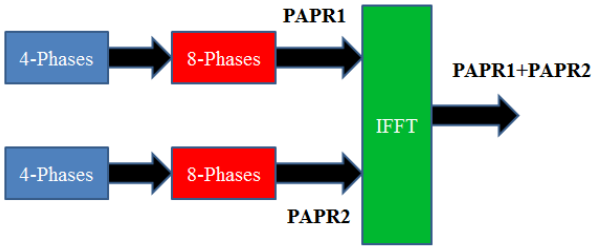

Figure 6.7: CCK 16 length with partitioning.

However, the encoded signals after the IFFT are time overlapped which increases PAPR $10log10(2M)$, where M is the number of groups. Figure 6.8 shows the increase in PAPR compared to standard OFDM.

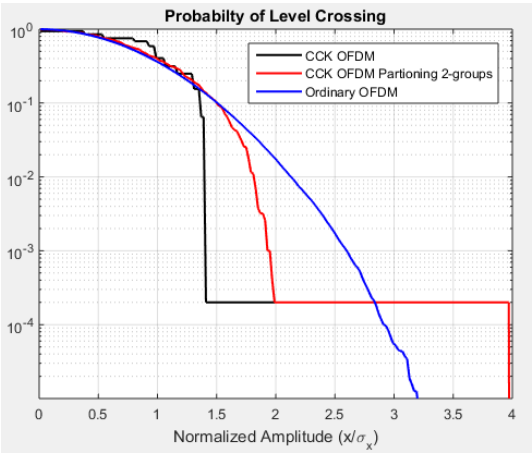

Figure 6.8: PAPR comparison with partitioning CCK.

Another option to alleviate high coding rate and and keep a constant PAPR of $\sqrt{2}$ consists in a time interleaving of the encoded data [26]. The number of groups in frequency before the IFFT can be replicated every $2\pi/M$ in order to have a zero packing in time. The number of Frequency replicas M, corresponds to $M-1$ zeros inserted between samples. By multiplying the groups for $e^{-j\theta r}$ in frequency, where $0 \leq r \leq M-1$, a time shift by r is made, thus the time overlapping disappears due to interleaving of the groups in the zero positions. Figure 6.9 shows this process for

two groups, 0 in blue and 1 in red.

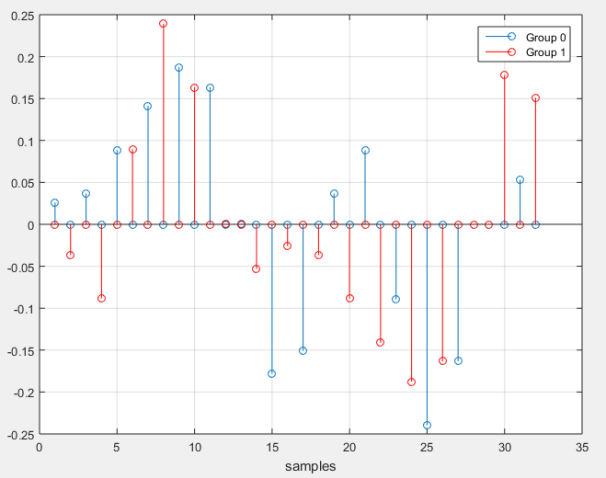

Figure 6.9: CCK 16 length interleaving for two groups.

By interleaving, PAPR is back to a constant value of $\sqrt{2}$, as shown in figure 6.10.

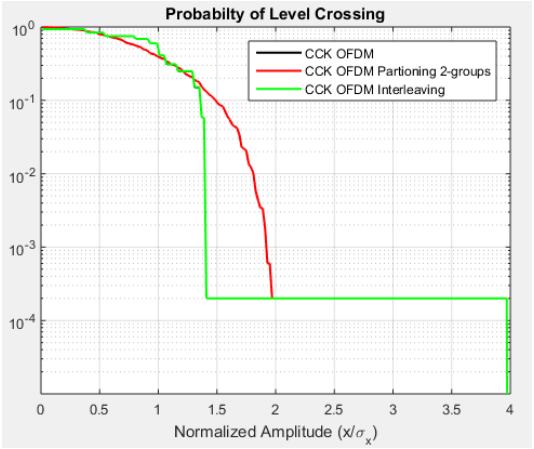

Figure 6.10: PAPR comparison for CCK 16 length with interleaving.

Implementation for two groups is shown in figure 6.11. It can be observed that interleaving is made in time domain after IFFT by summing the time series. The IFFT must be twice the size of the subcarrier in order to accommodate the replicas inside the first Nyquist zone. In addition r represents the branch number which is equivalent to the time shift that is applied to each group by the corresponding phase rotator in frequency.

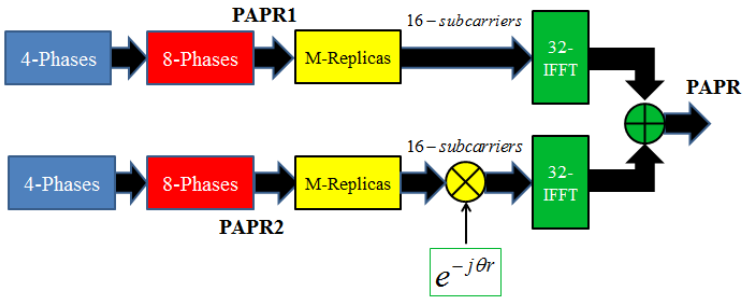

Figure 6.11: CCK interleaving block diagram.

The implementation in figure 6.11 is practically inefficient. As the number of groups increases, more IFFT blocks are required to transform every group. An alternative consists in implementing interleaving in frequency, as shown in figure 6.12.

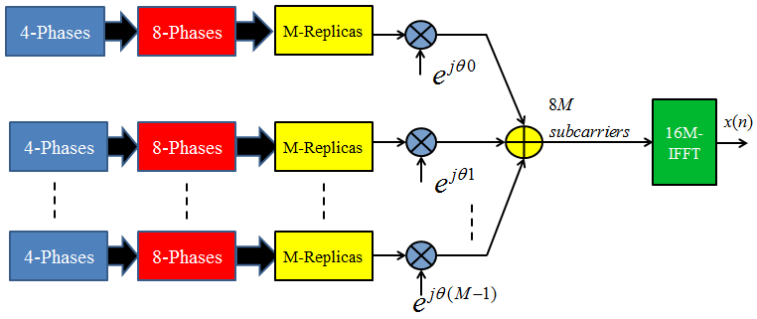

Figure 6.12: CCK interleaving with efficient implementation block diagram.

Every spectral group is phase rotated and then overlapped, then the IFFT outputs the set of time interleaved series. Due to different phases in each frequency group, aliasing is not present, as shown in figure 6.13.

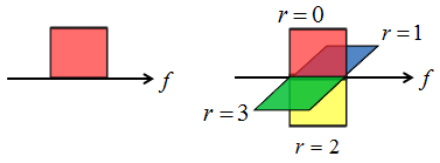

Figure 6.13: CCK interleaving with frequency phase representation.

6.2. OFDM Channelization

A 64-channelizer is designed and tested with a standard OFDM modulator. In communications, it is typical to use Square Root Raised Cosine (SRRC) filters in the transmitter as a shaping filter and in the receiver as a matched filter. However, these filters present poor performance in the stop-band [4], thus the prototype filters are designed using a Kaiser window method for the analysis and Remez algorithm for the synthesis part. Both filters are designed with 0.001 dB of in-band ripple and 80dB of attenuation which is inside the dynamic range of a 16-bit processor, as shown in figure 6.14.

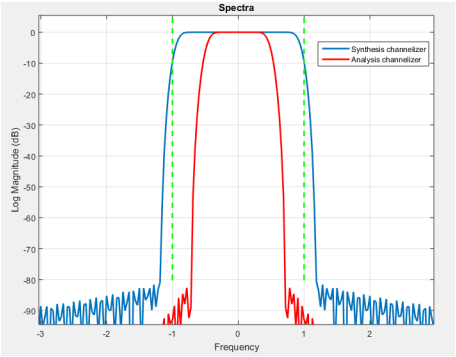

Figure 6.14: Analysis and synthesis prototype filter spectrum.

Due the output sampling rate is twice the channel spacing and the channel bandwidth, the synthesis filter bandwidth must be bigger enough to cover the entire analysis prototype filter including the transition bands, as shown in figure 6.15.

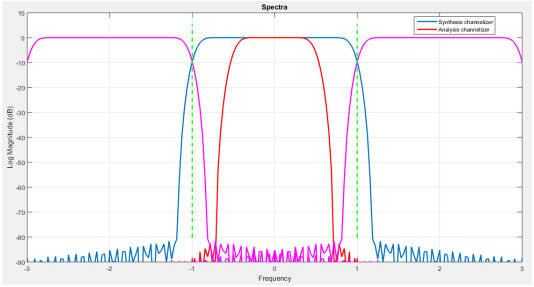

Figure 6.15: Filter bandwidth comparison with different sizes [4].

Different transition bands cause both filters to be of the same length of 767 taps.

The analysis filter is designed with a Kaiser-sinc window to obtain a Nyquist filter which is capable of collect most of the energy of the different channels. Figure 6.16 shows two adjacent channels at 0 and 1, which are joint at -6dB.

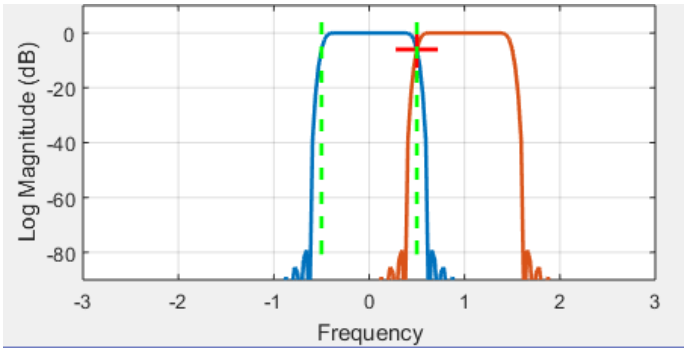

Figure 6.16: Vestigial symmetry in Nyquist filters.

To demonstrate the -6dB Nyquist property, an impulse can be inserted in two adjacent channels at the synthesis side, the remaining 62 channels must be set to zero. Figure 6.17 shows this joint at -6dB of channels 0 and 1.

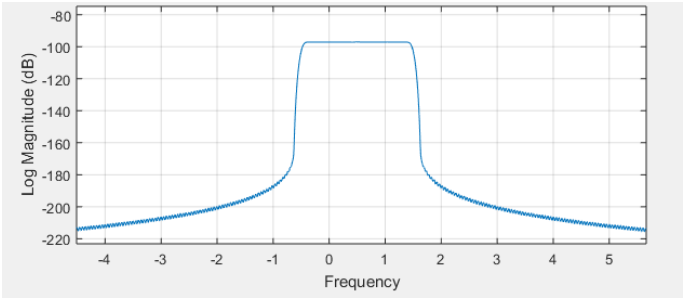

Figure 6.17: Frequency joint at -6dB in Nyquist filters.

The synthesis filter is designed with the Remez algorithm. The Remez algorithm is an equiripple design that exhibits constant level side lobes. When designing channelizers whit this method, adjacent channels low level energy resides inside the pass-band of a channel and are added causing a pilling up of the energy, this is known as pass-band noise and equals to the noise floor plus $10log_{10}(M-1)$, where M is the number of channels, as shown in figure 6.18. To prevent the stacking of energy inside the pass-band, the filter must be redesigned in order to have a $1/f$ side lobe attenuation [27].

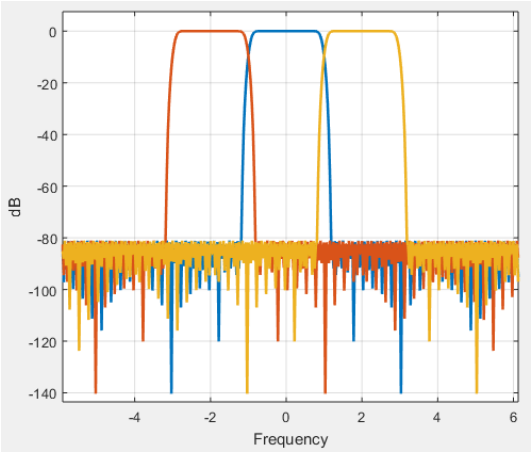

Figure 6.18: Constant side lobes in Remez algorithm filters.

Matlab contains a script called "remezfrf.m"which implements a penalty function that defines the constant side lobes in the Remez design. A modified version named "myfrf.m" is employed in the Remez programming expression in order to design the filter with a stopband decay of $1/f$, as shown in figure 6.19. More information about this function can be found in [27].

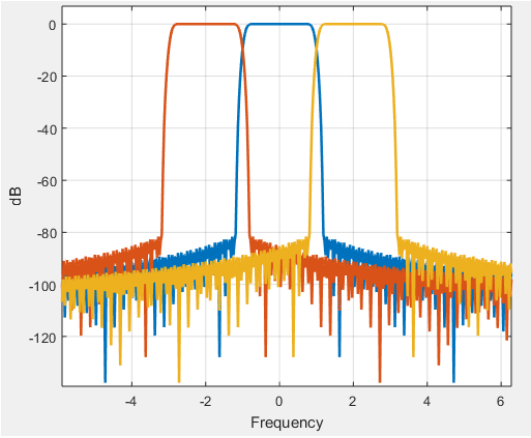

Figure 6.19: Slope decay in modified Remez algorithm.

The $M/2$ analysis 64-channelizer employs a 64-IFFT for the Nyquist channel selection, a 128-IFFT per channel to generate the OFDM symbols with $2f_s$, the $M/2$ sampling rate is achieved by delivering two repeated samples, two commutators are used, one at position 0 and the other at the middle position [4]. For every input,

the system outputs 32 samples, thus having an output sampling rate of $64f_s$. The 767 taps from the prototype synthesis filter are loaded in a 64X12 2D matrix where every polyphase filter is only of length 12, thus the system processes 12 operations per input instead of 767. QPSK and 16-QAM modulation is used in the OFDM system. The OFDM 64-Channelizer block diagram is shown in figure 6.20.

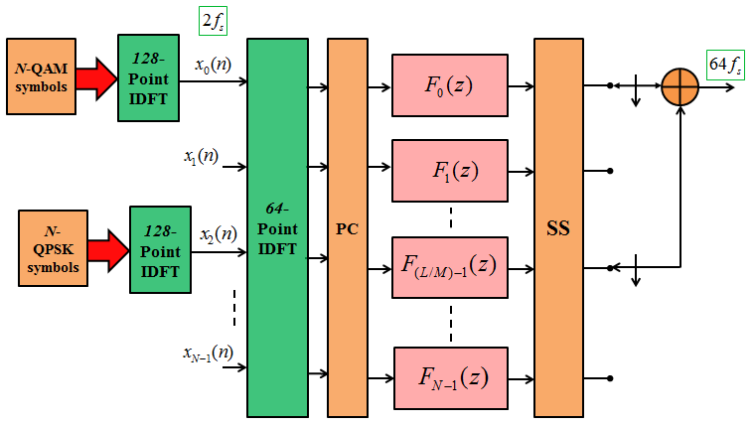

Figure 6.20: Ration arbitrary sampling rate synthesis channelizer [4].

The receiver is the dual of the transmitter, the commutator delivers two repeated samples. For every 32 input samples the system outputs one sample.

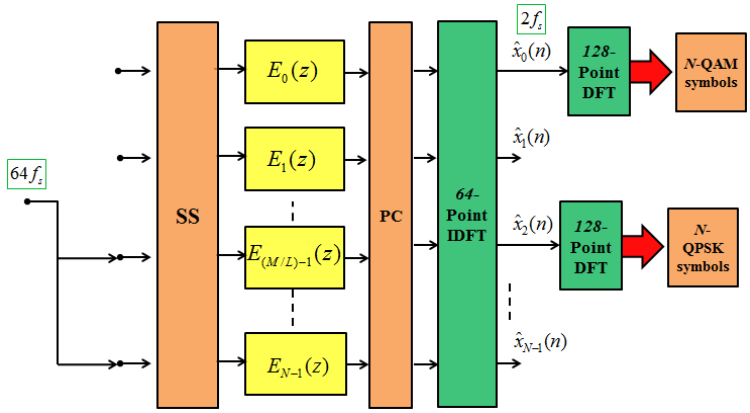

Figure 6.21: Rational arbitrary sampling rate analysis channelizer [4].

To test the channelizer with the OFDM modulator, five packets of 50 OFDM symbols each are created with coded QPSK and 16QAM and put at channels 1, 5, 6, -3 and -5. Figure 6.22 shows the composite signal in time and frequency. It can be

observed that the composite signal in time has a delay approximately of 384 samples which is equivalent to half the size of the prototype channelizer, this correspond to the group delay of the analysis FIR filter.

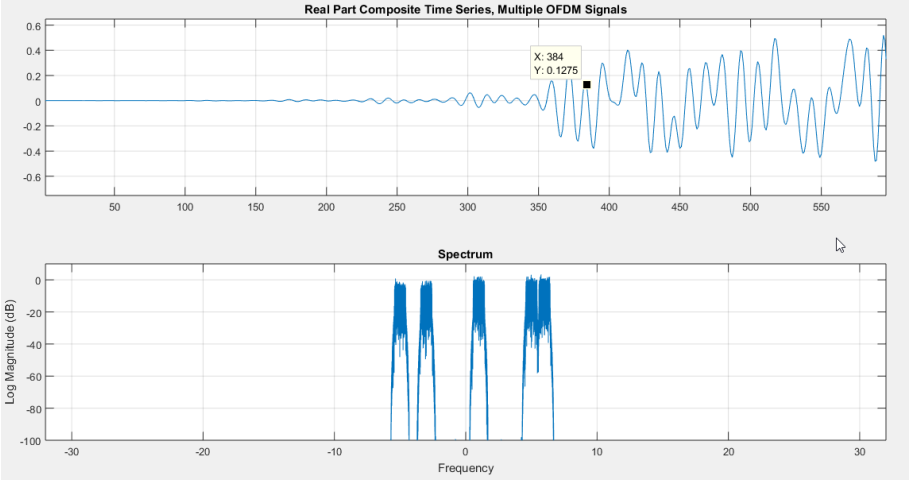

Figure 6.22: Composite signal after synthesis channelizer in time and frequency.

This composite signal must be passed through the analysis channelizer and decomposed to recover each channel. Figure 6.23 shows the channels recovered in every corresponding FFT bin.

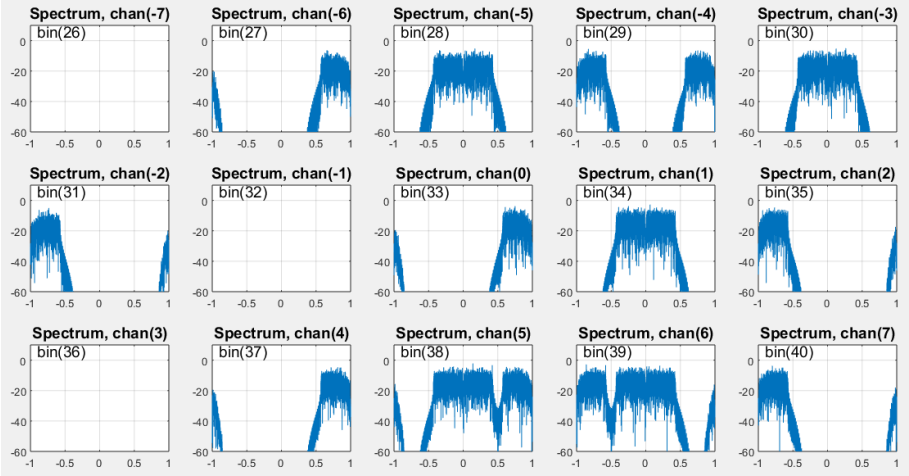

Figure 6.23: Extracted channels after analysis.

It can be observed that channels that must be empty contains some spectral

components. These components appear also in occupied channels. This is due to the bandwidth of the analysis and synthesis filters have different size. The bigger bandwidth touches its adjacent channels at the right and left taking part of them. The overlapping between the transition bands of both filters cause the empty channels to acquire these spectral components. The polyphase filter banks isolate every channel, however the spectral components of the adjacent channels causes distortion in the signal when different time delay are present in the channels. For instance two adjacent channels causes distortion to each other when they have different delays. Figure 6.24 shows the impulse response corresponding to a single channel.

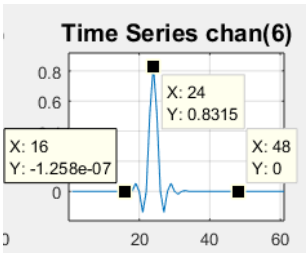

Figure 6.24: Impulse response for a single channel.

The delay present in a channel corresponds to the polyphase components in the transmitter/receiver channelizer. The prototype filters have polyphase components of length 12 each which form a total length of 768 taps per filter. The impulse response have a peak at sample 24, this corresponds to two times the total group delay of both polyphase components at the transmitter/receiver, the transient response is also the double, it has a value of 48, this increase in delay is due to the polyphase implementation. When a channels is demodulated, the start of the frame must be tracked in order to have a correct synchronization with the FFT origin at the receiver. However the group delay and the transient response are not a good reference to compute the start of the frame. The start of the frame is detected after the first sample is processed in the channelizer, this happens after 16 samples, as shown in figure 6.24. It might be obvious, however, the correct signal values are only available after the transient response, therefore, due to samples are taken before the transient response some samples get distorted at the start of the frame. This is necessary in order to have a correct time synchronization. Figure 6.25 illustrates a demodulated QPSK channel with an adjacent channel, no distortion is present, due to both channels

have the same delay.

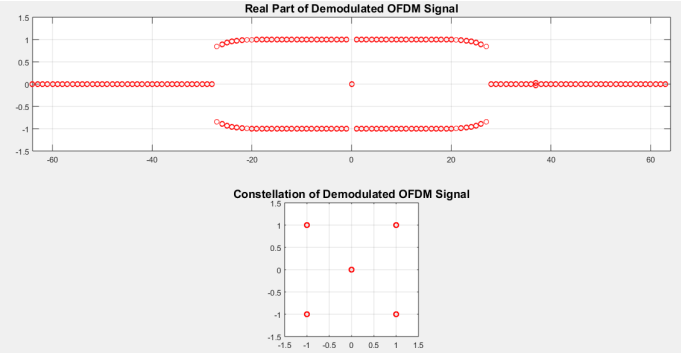

Figure 6.25: Demodulated QPSK channel.

Figure 6.26 shows the impulse response for two adjacent channels with no delay. Both channels have opposite polarity, in fact every odd channel has opposite polarity, this is due to the $M/2$ polyphase implementation. It can also be observed that there is some little distortion because of the extra spectral components mentioned formerly.

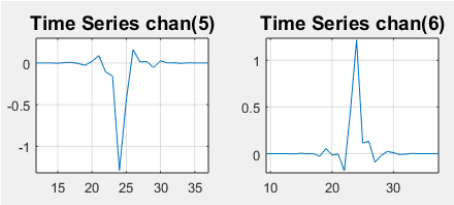

Figure 6.26: Adjacent impulse response channels.

If a small delay is applied to one of the channels, in this case, to the channel at the right position, the distortion is shifted in time and now can be appreciated, as shown in figure 6.27

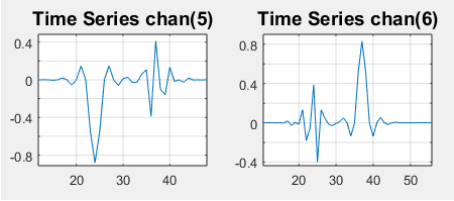

Figure 6.27: Adjacent impulse response channels with initial delay of 13 samples.

This proves that channels are still not isolated at all. A delay in one channel affects to its neighbor. If a bigger delay is applied in only one channel, the influence to its adjacent channel can be appreciated in more detail, as shown in figure 6.28.

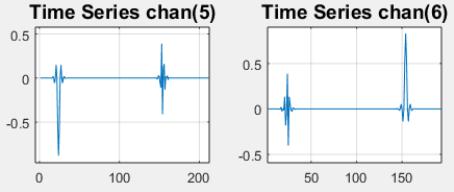

Figure 6.28: Adjacent impulse response channels with initial delay of 130 samples.

When demodulating, even with a correct time synchronization with the FFT origin, distortion is present, as shown in figure 6.29. It can be observed that the adjacent channel at the right position distorts the signal by complete.

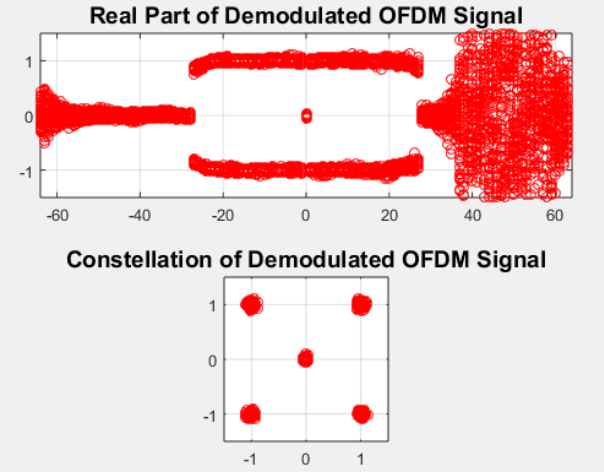

Figure 6.29: Extracted delayed channel after analysis with distortion .

To avoid distortion in the signal, the channel must be filtered by a lowpass filter, as shown in figure 6.30. The spectral components belonging to the adjacent channel are eliminated, thus the channels are completely isolated. The lowpass filter of order 37 is designed with the Remez algorithm. This filter adds an extra delay of 18 samples to every channel that must be taken into account when demodulating with the FFT.

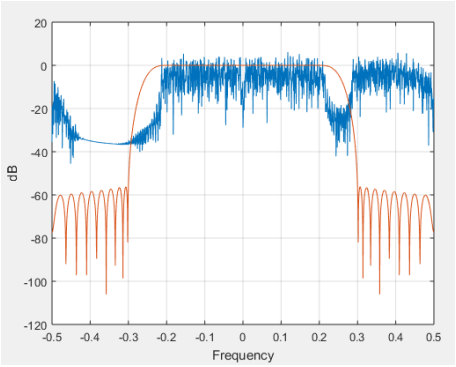

Figure 6.30: Pre-filtering for undesired spectral components.

Figure 6.31. illustrates the demodulated signal with pre-filtering to eliminate the undesired spectral components. It can be observed that there is a little remaining distortion outside of the pass-band that does not affect the OFDM data.

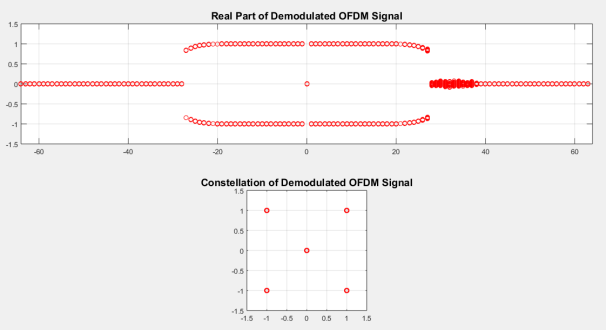

Figure 6.31: Isolated channel after pre-filtering.

6.3. Frame Detection and Channel Estimation

Every channel has a total delay of 34 samples. In MATLAB simulation, frame detection can be easily achieved by typing the correct delay index. However, a synchronization algorithm must be designed in order to automatically compute the right time delay in practice. To detect the start of the frame, synchronization by using a short preamble which is usually employed in WLAN 802.11 is designed. To implement the frame detection algorithm, first, a preamble with an OFDM symbol size is generated in the transmitter side. QPSK preamble is usually employed. A zero packing in

frequency is made in order to have replicas in time domain, as shown in figure 6.32. In fact, every replica is a short preamble.

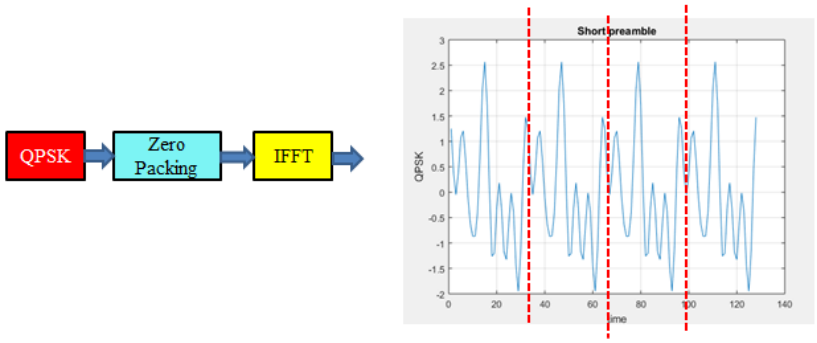

Figure 6.32: Short preamble zero packing.

The reason for sending repeated preambles is because in the receiver side a correlation detector based on the approach presented by Schimdl and Cox [28], will detect the start of the frame by estimating the received signal power. The detector block diagram is illustrated in figure 6.33.

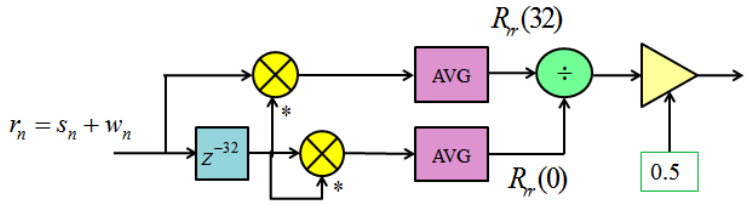

Figure 6.33: Frame detector at receiver.

The detector works as follows: the upper line computes the cross-correlation of the received signal plus noise with a delayed version. The received signal S_n passes through a delay line equal to the duration of one short preamble. Thus the cross-correlation of S'_n and its delayed version S_n results in autocorrelation due to periodicity of the short preambles $R_{ss'}(32) = R_{ss}(0)$. The lower line computes the cross-correlation of the received signal, this value is used to normalized the amplitude of the detection. The ratio of the cross and auto correlation passes through a detector which decides if there is a frame present when the ratio value exceeds 0.5, as shown in figure 6.34.

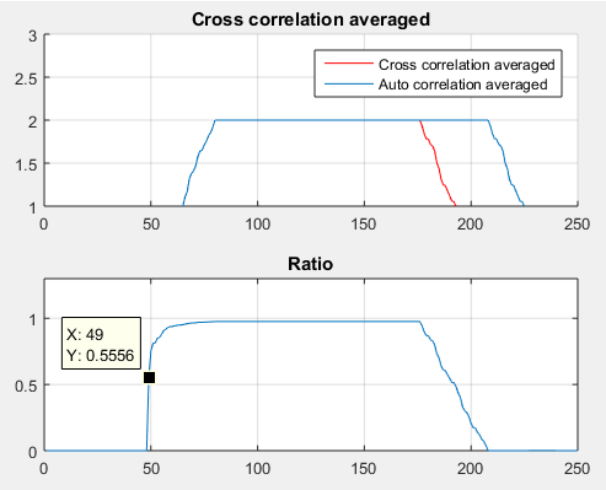

Figure 6.34: Frame detection threshold.

To estimate the frequency response of the channel, a long preamble is used. This preamble is known a priori by the receiver thus when it passes through the channel, it is multiplied in frequency, as shown in figure 6.35. The receiver multiplies this preamble after the channel by the reciprocal of the known frequency response and thus extracts the response of the channel.

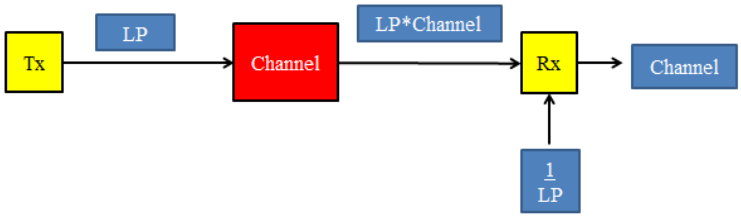

Figure 6.35: Channel estimation block diagram.

6.4. Comparison with Other Methods

The most remarkable differences regarding the channelization arbitrary sampling ratio were explained in Section 4.3. Most of the systems presented use filter banks to reduce ICI and isolate the channels. The only difference presented here is in PAPR reduction. Figure 6.36 illustrates a comparison in PAPR with different reduction tech-

niques. Standard OFDM systems presents the highest value in PAPR. Single-Carrier OFDM is used in the uplink transmission and only reduces PAPR for 1dB. Shaped single carrier OFDM (SSC-OFDM) uses a spectral window to reduce this value with a trade-off in excess bandwidth of the signal, this reduces spectral efficiency considerably. SSC-OFDM is similar to the CCK technique presented, with the difference that the main trade-off is related to coding rate which reduces the data rate transmission.

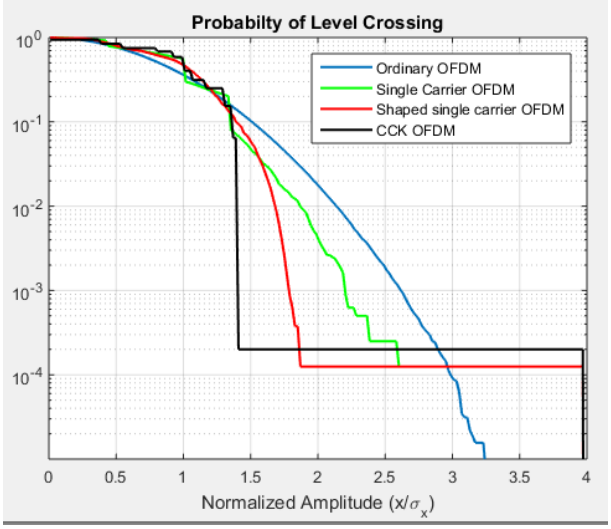

Figure 6.36: PAPR comparison.

Chapter 7

FPGA Implementation

In this final chapter, an implementation of two of the main components in the channelizer are made: the FFT and the polyphase filter bank. A 64 point FFT and a polyphase filter bank are implemented using Verilog in fixed point with Q1.14 format. Co-simulation with Modelsim-Quartus II is used for fixed point gate-level and RTL simulation, power analysis, timing constraints and synthesis in a DE2-70 board.

7.1. FFT Implementation

A 64 point FFT can be implemented in different ways, parallel, serial and pipelined among others. Parallel implementation is the fastest design, however it consumes a great amount of resources. Serial implementation computes a single butterfly per clock cycle using less resources in exchange for more processing time, requiring $N/2$ cycles per stage. Pipeline structure inserts registers in the critical path of the design in order to increase the maximum frequency. These causes the hardware to be used efficiently because the internal FFT blocks are always working in a parallel form in exchange for more latency in the system.

The design presented in this work is implemented in serial form using algorithm radix 2. Decimation in frequency is applied, thus bit reversal is needed at the output. For 64 points, 6 stages are required, each with $N/2$ butterflies. Therefore, $6(N/2) = 192$ cycles are required to compute the FFT for 64 input samples.

To guarantee an output signal value of one in magnitude and avoid overflow, the input is limited to $1/\sqrt{2}$. After every butterfly, the magnitude is doubled, thus an scaling of 1/2 is required [29]. Rounding to the nearest value is applied after every multiplier when passing from 32 to 16 bits in order to avoid DC bias.

The FFT was implemented using a state machine based on a design described in [30], as shown in figure 7.1.

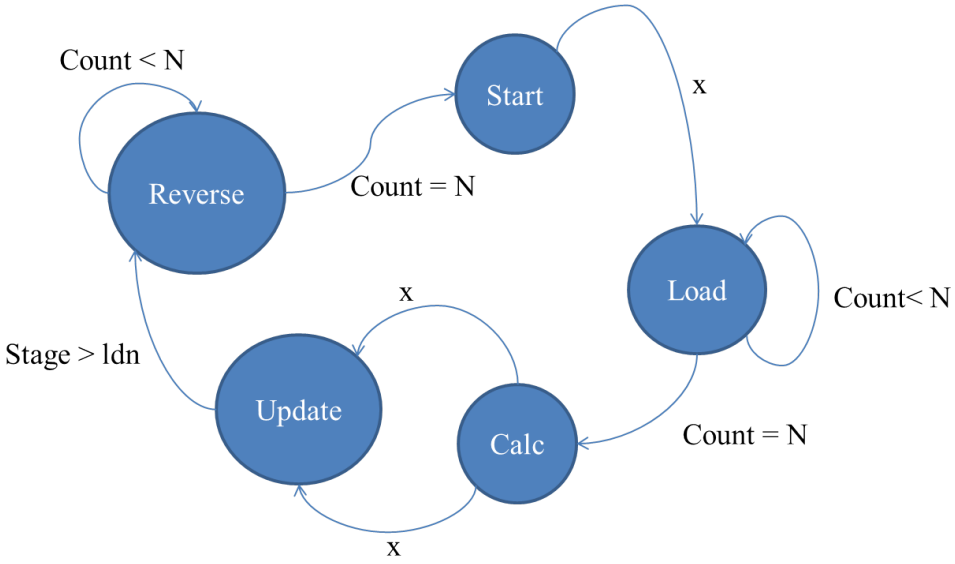

Figure 7.1: FFT state machine for serial implementation.

When putting a single value in an specific frequency bin, the output will have an integer number of sinusoid periods. To show the correct performance of the FFT, a value of 1 is set at bin 1, the real part will show a cosine period and the imaginary part a sine period, as illustrated in figure 7.2. The figure actually shows the IFFT, it is important to mention that with the same structure, the FFT and IFFT can be easily implemented by only conjugating the imaginary part of the twiddle factors.

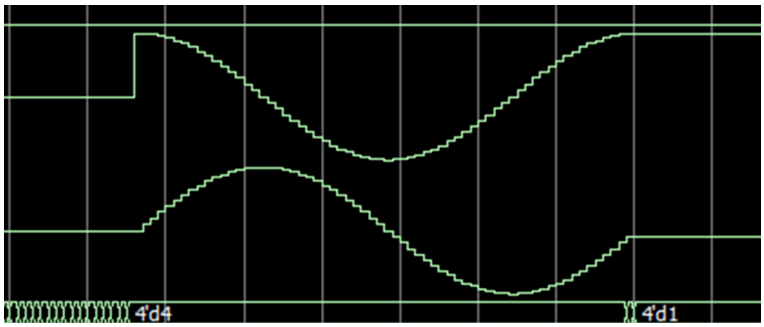

Figure 7.2: Real (top cosine) and imaginary (bottom sine).

If a different input is applied, for instance a single rectangular pulse that occupy 8 bins, the output will show a sinc function as shown in figure 7.3.

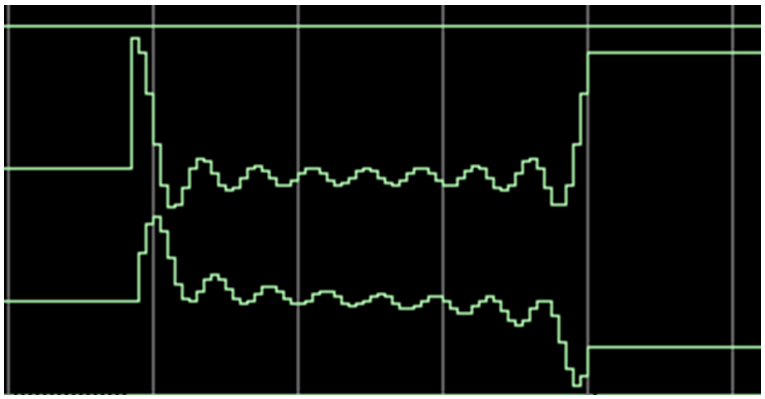

Figure 7.3: Frequency response of an input rectangular pulse shown in Modelsim.

When compared to the results in Matlab [31], it can be observed that they are the same, as shown in figure 7.4.

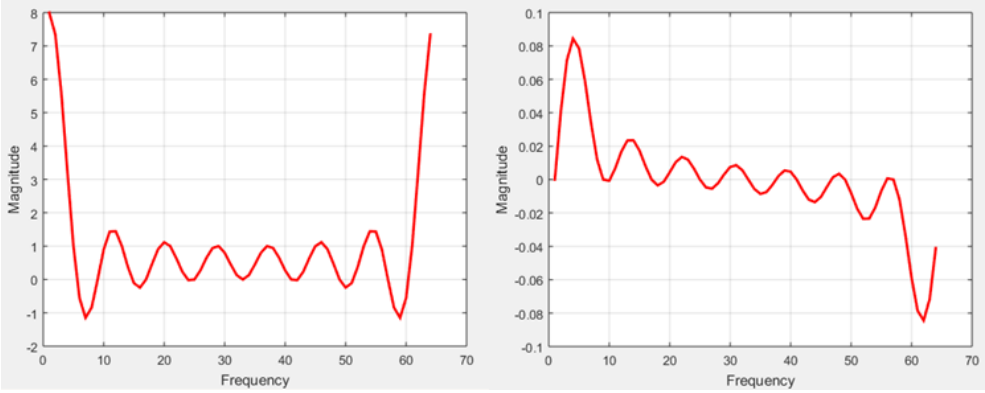

Figure 7.4: Real (left) and imaginary (right) components of a rectangular time pulse in MATLAB.

In table 7.1 can be observed the summary of the resources used for implementation. The design requires only 8 multipliers of 9 bits which is equivalent to 4 multipliers of 16 bits. Dynamic and static power dissipation was computed in Quartus II, the results can be observed in table 7.2. To compute the dynamic power, an input signal generated with a counter was applied obtaining an average toggle rate of 99.2 % equivalent to 8.778 millions of transitions/sec. Gate level simulation was required to consider the delay present in every component.

Flow Summary	
Flow Status	Successful - Tue Nov 29 21:30:08 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	DE2_TOP
Top-level Entity Name	FFT
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	6,085 / 33,216 (18 %)
Total combinational functions	6,085 / 33,216 (18 %)
Dedicated logic registers	2,125 / 33,216 (6 %)
Total registers	2125
Total pins	54 / 475 (11 %)
Total virtual pins	0
Total memory bits	3,968 / 483,840 (< 1 %)
Embedded Multiplier 9-bit elements	8 / 70 (11 %)
Total PLLs	0 / 4 (0 %)

Table 7.1: Workload summary for the FFT in Quartus II.

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Wed Nov 30 08:14:35 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	DE2_TOP
Top-level Entity Name	FFT
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	192.40 mW
Core Dynamic Thermal Power Dissipation	75.39 mW
Core Static Thermal Power Dissipation	80.20 mW
I/O Thermal Power Dissipation	36.80 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Table 7.2: Power analysis summary for the FFT in Quartus II.

7.2. Polyphase Filter Bank Implementation

The polyphase filter bank is implemented with 64 components corresponding to the number of channels and FFT points. The prototype filter is designed with a window method using a Kaiser window. The 768 fixed point coefficients are implemented in format Q1.14 and saved in a Look-Up table (LUT). These results in a dynamic range approximately of 80dB which corresponds to the attenuation of the designed filter. The filter is designed to work with a clock of 20MHz. The filter outputs 64 samples for every input sample. The output rate is equal to the clock and the input signal must be at least 64 times less than the output rate. The coefficients are indexed

using a counter to select the corresponding polyphase component. To test the design, an input signal with a low and high frequency is first downsampled by taking every M sample, as shown in figure 7.5.

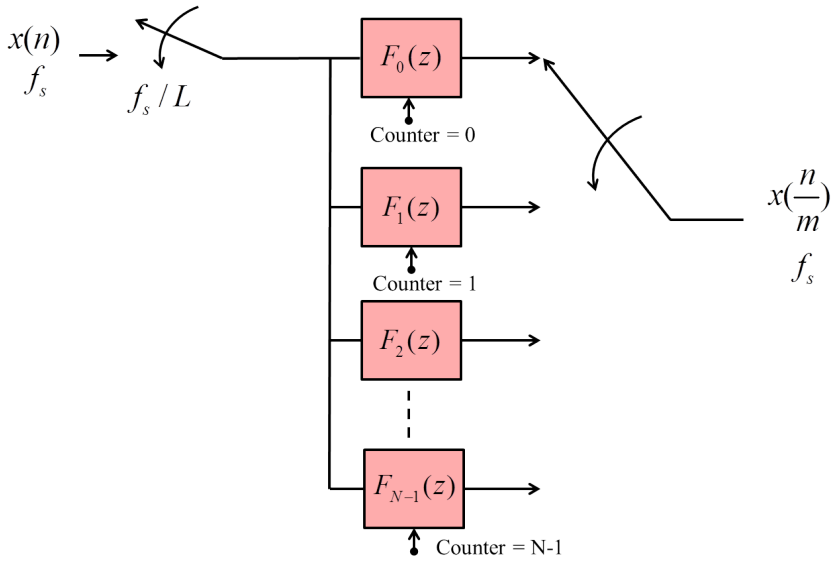

Figure 7.5: Polyphase filter bank block diagram for implementation.

The output must be a delayed version of the input sinusoid without the high frequency component. Figure 7.6 presents the corresponding signals in ModelSim [32].

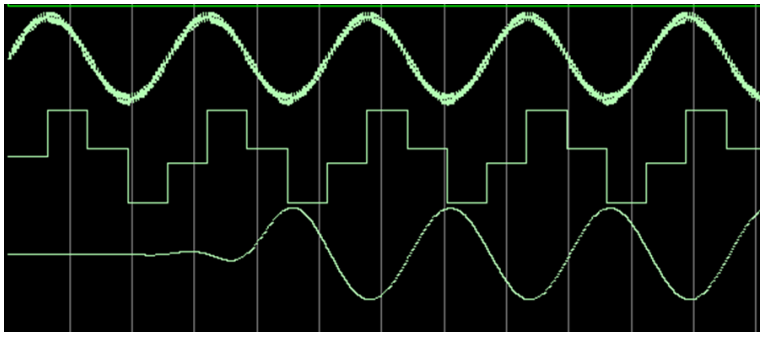

Figure 7.6: Input signal(top), downsampled signal by 64 (middle) and filtered output signal (bottom).

In table 7.3 can be observed the summary of the resources used for implementation. The design requires only 24 multipliers of 9 bits which is equivalent to 13 multipliers of 16 bits, however 12 are really used. This is the most outstanding advantage of using

polyphase implementation. For instance, compared to the direct implementation I, 768 multiplications would be required which is practically impossible. Dynamic and static power dissipation was computed in Quartus II [33], the results can be observed in table 7.4. To compute the dynamic power dissipation, an input signal generated with a counter was applied with a clock of 20MHz obtaining an average toggle rate of 61.1 % equivalent to 4.623 millions of transitions/sec. Gate level simulation was also required to consider the delay present in every component.

EDA Netlist Writer Summary	
EDA Netlist Writer Status	Successful - Tue Nov 29 19:44:34 2016
Revision Name	DE2_TOP
Top-level Entity Name	polyu64
Family	Cyclone II
Simulation Files Creation	Successful
Flow Status	Successful - Tue Nov 29 19:50:14 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1,796 / 33,216 (5 %)
Total combinational functions	1,620 / 33,216 (5 %)
Dedicated logic registers	199 / 33,216 (< 1 %)
Total registers	199
Total pins	34 / 475 (7 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	24 / 70 (34 %)
Total PLLs	0 / 4 (0 %)

Table 7.3: Workload summary for the polyphase filter in Quartus II.

PowerPlay Power Analyzer Summary	
PowerPlay Power Analyzer Status	Successful - Tue Nov 29 19:50:14 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	DE2_TOP
Top-level Entity Name	polyu64
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	128.88 mW
Core Dynamic Thermal Power Dissipation	14.35 mW
Core Static Thermal Power Dissipation	79.99 mW
I/O Thermal Power Dissipation	34.54 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

Table 7.4: Power analysis summary for the polyphase filter in Quartus II.

Chapter 8

Conclusions and Future Work

8.1. Conclusions

In this thesis main disadvantages in OFDM systems were presented in detail. DFT filter banks and Golay series were introduced in order to present the main subject of our research which is the analysis and implementation of the channelization technique based on Non-Maximally Decimated Filter Banks with an arbitrary rational sampling rate and PAPR reduction with CCK OFDM.

Synchronous multiplexing in LTE systems due to OFDM modulation for different mobile stations has been investigated to analyze the main drawbacks due to differences in user time alignment. Simulations in Matlab with QPSK and 16-QAM channels were carried out in the NMDFB channelizer in order to test the isolation in time and frequency between adjacent channels.

For PAPR reduction, different variations in CCK coding were studied, arriving to the conclusion that time interleaving was the best option with a trade-off in bit rate reduction as exposed in the referenced literature.

It was demonstrated by means of simulations in Matlab, that users can be independently modulated even though they have different modulation formats and time arrival in the base station.

Finally, FPGA implementation of the 64-FFT and the polyphase filter bank for the synthesis part was made. Power analysis and timing constraints were carried out for comparison purposes with other designs.

8.2. Future Work

PAPR reduction with CCK can be investigated in order to use the FFT block in the channelizer without the need to use another block for modulation. For the implementation, every channel can be implemented using a DSP adapted to the FPGA using a real time signal.

Appendix

Publications Derived from the Thesis

Fernando Ojeda, Fredric J. Harris, Gordana Jovanovic (2016). "PAPR Reduction and Asynchronous Multiplexing in OFDM Systems", Vigesimasexta Reunión Internacional de Otoño de Comunicaciones, Computación, Electrónica, Automatización, Robótica y Exposición Industrial ROC&C. IEEE Sección México.

Research Stay

Department of Electrical and Computer Engineering, San Diego State University (SDSU), Oct/2015 to Apr/2016.

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