Analysis of Hot Carrier Degradation Impact on Small Signal Model Parameters in Nanometric n-MOSFET

Por

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Abstract:

The reliability of sub-100nm MOSFETs due to Hot Carrier Stress becomes a critical topic as the channel length of the transistors shrinks at different rate as the power sources do. Much research has been made in this area from a DC point of view but only a few have analyzed the effect of this degradation in the parameters that constitute the small-signal model. An analysis of the level of hot carrier (HC) degradation caused up to 20 GHz is introduced. The degradation process is done through the application of controlled DC currents at well defines periods of time. The recorded S-parameters before and after DC degradation allows the observation of the corresponding changes in the transmission and reflection features, as well as in the intrinsic channel resistance and the transconductance.

Resumen:

La degradación en los MOSFETs debido a portadores de carga caliente es un tema que está tomando gran importancia ya que la utilización de estos en aplicaciones de cada vez mayor frecuencia demanda su continua disminución en dimensiones especialmente hablando de la longitud del canal de conducción lo cual facilita la generación de portadores de carga caliente y por ende la degradación debida a éstos. La mayor parte de la investigación de esta degradación se ha realizado con modelos para caracterizar su comportamiento en DC. En este trabajo se analiza este tipo de degradación desde el punto de vista del modelo de pequeña señal, hasta una frecuencia de 20GHz, aunado a esto se analiza una tendencia en los parámetros S medidos y simulados que ayudan a determinar concluyentemente los parámetros mayormente impactados por este tipo de degradación los cuales son los parámetros intrínsecos de la resistencia de canal y la transconductancia.
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1.1 General introduction

The global market for electronics is mostly fueled by the demand for faster, smaller and better electronic devices. Achieving these goals has been possible in part by increasing memory storage capacity as well as by rising data processing frequencies within the gigahertz range. In this regard, although the high-frequency properties of silicon are inferior compared to other materials used in the semiconductor industry (e.g., gallium arsenide), the relatively low production cost, the high level of integration, and the reduction of the channel length to nanometric scale make the silicon MOSFET a strong contender for RF applications [1].

Nevertheless, it is necessary to bear in mind that the channel length reduction has also brought new challenges; one of them is the negative impact of hot carriers caused by the strong electric fields present in nanometric devices. This problem has become apparent mainly due to the lack of proportionality between the scaling of the channel length and the input voltage applied between the source and drain terminals. As an example of this, consider a MOSFET with a channel length of 80 nm (like the ones experimentally studied in this work) and biased with drain-to-source voltage of 1 V; the electric field results in:

\[
E = \frac{v}{d} = \frac{1 \text{ V}}{80 \times 10^{-9} \text{ m}} = 12.5 \times 10^6 \text{ V/m}
\]

This considerably large field accelerates a fraction of the electrons that go from the source to the drain terminal [21]. Hence, these electrons acquire so much energy that they become hot carriers capable of over passing the conduction band of the oxide layer that separates and isolates the gate terminal from the inversion layer. Some of these hot carriers will be trapped into the oxide layer, creating a carrier’s interfacial density and diminishing the performance of the oxide layer. Moreover, they can even trespass the gate’s isolating layer, eventually causing oxide breakdown. This will be better explained in Section 1.7. In addition, a side effect associated with hot carriers is the impact ionization phenomenon, which originates a bulk current that degrades the behavior of the device. From a characterization point of view, however, this current is very helpful to quantify the electrical stress that the device is suffering. In fact, the degradation procedure used in this
work is based in this concept as will be seen in Chapter 3. Fig. 1.1 conceptually shows this effect.

Circuit design is an essential part of electronics technology, as important as the chip fabrication itself. In this regard, advances in the fabrication process always introduce new challenges for designers; therefore, in order to fully take advantage of the available technologies in continuous evolution like RF-CMOS, the designers need the development of models that aid to predict the behavior of the components for the greatly demanded high-speed applications. Furthermore, these models have to be accurate for a wide range of frequencies while maintaining as simple as possible the corresponding implementation in standard simulation tools (e.g., SPICE). Particularly, the characterization and modeling of the small-signal features of MOSFETs is required for designers and signal integrity engineers to simulate the behavior of an RF MOSFET at the same time as considering the related time-dependent degradation [25]. The reason why an accurate representation of the devices under small-signal operation is important is because it is the basis for designing linear amplifiers. In this regard, a small signal is that presenting a power so low that it can be applied at the input terminal of a MOSFET to obtain a response at the output that only change in magnitude and phase but not in frequency. For circuit design purposes, the most common alternative to represent MOSFET’s small-signal operation is using equivalent circuits. For this reason, the idea in a project like the one developed in this thesis is incorporating the effect of device degradation to these models.

There are several small-signal equivalent-circuit models for a MOSFET reported in the literature and they present some common features. One of these is the fact that the lumped electrical components of the model can be related to two main types of parameters: intrinsic and extrinsic parameters. The extrinsic parameters are those associated with the effects occurring outside the core of the transistor (i.e., the core corresponds to its active part: the inversion layer). For instance, the resistances at the drain, source, and gate terminals, as well as the junction and overlap capacitances are considered extrinsic parameters.
elements. It is important to mention at this point that there are additional extrinsic elements that were neglected in the past (before the decade of the 2000’s) since their effect becomes apparent only within the gigahertz range; into this category highlight the parasitic substrate elements. Recently, for this particular case, RF-MOSFET models include the associated effects through substrate resistances and capacitances [20–26]. On the other hand, regarding the intrinsic parameters, these are the ones related to the active part of the device, and are associated with the characteristics of the inversion layer, such as the transconductance. Most of these parameters, extrinsic and intrinsic, suffer in one or another way the effect of hot carrier degradation. Thus, in this context, by combining the ideas related to small-signal characteristics and degradation by hot carriers, an analysis of the impact of the hot carrier degradation on the small-signal MOSFET’s features is presented in this work under different bias conditions for a better understanding.

Now that a general idea of this work has been exposed, for the rest of the first chapter, important and related topics will be explained. Firstly, the explanation of the method applied to measure the current–voltage characteristic curves of a MOSFET is given. This will allow to understand how applying a combination of DC and RF signals can be used to fully characterize the impact of hot carriers on the high-frequency small-signal performance of a MOSFET.

### 1.2 Basic description of equipment for DC characterization

Instead of separate power supplies, voltmeters, and ammeters, such as those used to characterize individually packaged discreet devices, DC parametric analyzers like a Semiconductor Parametric Analyzer (SPA), also referred to as Semiconductor Device
Fig 1.3 Principle of Kelvin measurements illustrated in an SMU present at an SPA [3].

Analyzer (SDA), with several source-monitor-units (SMUs) are used for on-chip and on-wafer device measurements [2]. This allows to characterize the device under test (DUT) even considering currents presenting values as low as a few femtoamperes. In this case, forward and reverse currents and voltages are measured using the same SMU. Particularly, for a MOSFET, all four terminals are connected to individual SMUs in order to avoid re-cabling during forward and reverse measurements.

An SMU uses the Kelvin measurement technique to compensate for the parasitic series resistances associated with the cables and electrical transitions required to apply the stimuli to the DUT. This measurement procedure consists of a stimulating line (referred to as Force) with a second one in parallel (referred to as Sense) for every terminal of the DUT. Fig 1.3 shows a simplified diagram illustrating this technique. As can be seen, the voltage drop along the Force line due to the associated resistive losses is compensated by using an operational amplifier (OpAmp1) configured in a voltage-follower mode. In this case, the output of OpAmp1 will exhibit a voltage higher than the one desired at the test point since the Sense line, which carries negligible current and does not originates a significant voltage drop, feeds OpAmp1 with approximately the voltage present at the test point. This assures that the DUT is biased with exactly the desired voltage.

While OpAmp1 compensates for the DC errors due to the resistive losses introduced by the Force line, external electro-magnetic interference may also represent an issue to obtain reliable measurements and requires to be minimized. For this purpose, shielded cables are used for the Force and Sense lines. Unfortunately, this solution introduces parasitic capacitances between the shielding and the main line that affect the measurement speed and accuracy. Thus, in order to solve this additional problem, an extra inner shielding called “Guard” is used between the main lines and the outer cable shielding so that a second operational amplifier (OpAmp2) follows exactly the value of the desired test voltage and
supplies the charging current for the test cables (see Fig. 1.3). In this case, the main OpAmp1 allows to perform DC current measurements to the DUT without the influence of additional currents; in other words, the inner measurement loop does not experience the charging problem anymore. An important fact is that the Guard contact should never be connected to either the Force or Sense lines because the inner loop (including OpAmp1 of the SMU) would be measuring the DUT current plus the charging current of the auxiliary second OpAmp 2. Chapter 3 will present some discussions about this practice showing the inconvenience of attempting to connect the SPA to a Vector Network Analyzer (VNA) without care. It is important to point out this fact because the built-in bias-T DC input module, which is an optional accessory in most commercial VNAs, is coaxial connector compatible, not triaxial. Therefore, a special connector to isolate the Guard instead of the ground has to be used. Otherwise, the measurements would be affected by the charging currents as mentioned above [2, 3].

Now that the main principle to perform DC measurements to on-wafer MOSFETs was mentioned, S-parameters measurements are briefly discussed afterwards.

### 1.3 S-parameters

In linear electrical network theory, scattering parameters or S-parameters are related to concepts such as gain, loss, and reflection. In contrast to Y and Z-parameters (defined from voltages and currents), S-parameters can be directly obtained at microwave frequencies since terminating the DUT with perfectly reflecting loads is not required when performing the corresponding measurements. This is because the scattering parameters are related to the traveling waves that are scattered and reflected when a network is inserted into a transmission line of certain characteristic impedance, $Z_0$. Furthermore, as in the case of any other set of network parameters, S-parameters measured to multiple devices can be cascaded to predict the overall system performance using simple transformations. This is one of the reasons why S-parameters are widely used to perform microwave circuit simulations. In addition, Z, Y, or H-parameters can be obtained from S-parameters. Here, these parameters can be used to analyze the characteristics of a MOSFET under test when it is considered as a two-port device connected in common-source configuration. In this case, the convention dictates that the gate terminal is considered as the port 1 (input terminal), the drain terminal is the port 2 (output terminal), while the source terminal is grounded (reference terminal). For the devices analyzed in this work, the bulk terminal can be accessed through a separate external connection that allows to apply a voltage independent of the source terminal using a DC probe, this will be explained in Chapter 3.
In matrix form, the S-parameters are defined using the following matrix equation that relates the vector representing the power waves coming out at each port \( (b_i^2) \) in terms of the incident power waves at each port \( (a_i^2) \) in the following way:

\[
\begin{pmatrix}
|b_1|^2 \\
|b_2|^2
\end{pmatrix} = \begin{pmatrix}
|S_{11}|^2 & |S_{12}|^2 \\
|S_{21}|^2 & |S_{22}|^2
\end{pmatrix} \ast \begin{pmatrix}
|a_1|^2 \\
|a_2|^2
\end{pmatrix}
\]  

(1.2)

Particularizing for a MOSFET in common-source configuration, the parameters in (1.2) represent the following:

- \( |a_i|^2 \) power wave traveling towards the gate \( (i = 1) \) and drain \( (i = 2) \) terminals
- \( |b_i|^2 \) power wave coming out from the gate \( (i = 1) \) and drain \( (i = 2) \) terminals
- \( S_{11} \) reflection coefficient at the gate with the drain terminated at \( Z_0 \)
- \( S_{22} \) reflection coefficient at the drain with the gate terminated at \( Z_0 \)
- \( S_{12} \) power transmitted from the drain to the gate: reverse gain indicator
- \( S_{21} \) power transmitted from the gate to the drain: direct gain indicator

### 1.4 About non-lineal devices

When measuring S-parameters of nonlinear devices with a VNA, it must be assured that the DUT operates within a small-signal region (i.e., linear mode). Otherwise, the high frequency test signals cannot be considered to be sinusoidal, and the occurrence of harmonics will lead to meaningless S-parameter measurements. Thus, an absolute prerequisite for appropriately interpreting two-port network parameters obtained under the small-signal behavior assumption is that the circuit must be the linear and time invariant. Only in this case, data processing like for example de-embedding is possible. In fact, nonlinear high-frequency measurements cannot be de-embedded by means of Y and Z-matrix subtractions [4]. As a matter of fact, when working with non-linear devices signal compression and distortion occurs, the DC operating point may be shifted, loadlines and transfer curves become dynamic, and matrix conversions are no longer possible. Thus, conventional de-embedding is no longer valid in this case [4–7].

### 1.5 About substrate losses in silicon MOSFET

MOSFETs are fabricated on a silicon substrate. Silicon can be considered as a semi-conducting material rather than a semi-insulating material like gallium-arsenide. This is due to the fact that in practice the resistivity of silicon is much lower than that of gallium-arsenide. Thus, since the resistivity of the silicon substrate is closely related to the device fabrication, relatively high semiconductor doping is required to reduce the resistivity.
Unfortunately, in a CMOS process, it is not easy to maintain the condition of either p-type or n-type substrate under a high resistivity condition. In consequence, the relatively low resistivity of the doped silicon substrate results in large parasitic effects. For this reason, the performance of integrated CMOS RF circuits is often dominated by these substrate-related parasitics, not by the intrinsic MOSFETs. This is one of the challenges faced by RF circuit designers today.

For RF MOSFETs, the influence of the distributed substrate effects is accounted for by means of a substrate equivalent circuit network. In this case, the impact of the corresponding substrate resistances becomes more significant as the operation frequency increases. This is due to the fact that, at relatively low frequencies, the impedance of the junction capacitances (i.e., the drain/source-to-bulk capacitances) is so large that the effect of the substrate resistances seen from the drain terminal becomes negligible. However, as frequency increases, the impedance of the junction capacitances is reduced and the effect of the substrate resistances becomes apparent. In fact, the modeling and parameter extraction required to implement a high-frequency model for an RF MOSFET fabricated on a bulk technology is more difficult when compared for instance with SOI MOSFETs, mainly because of the lossy silicon substrate. Actually, a more complicated model with a larger number of parameters is required to describe the behavior of the MOSFET in this case [8, 9]. Notwithstanding this obvious disadvantage, the reason why bulk MOSFETs is still preferred is because of their significantly lower cost. For this reason, the effect of the substrate losses is one of the more carefully analyzed throughout this thesis.

1.6 Hot carrier degradation

Understanding the mechanism of generation and the corresponding impact of hot carriers on the performance of RF MOSFETs is a key aspect considered in this work. For this reason, it is briefly revised in this section. Hot carrier generation and the effects on the characteristics of MOSFETs have been known for long time [10–12]. Hot carriers result from the high electric fields present inside the MOSFET, which naturally appear when biasing voltages are applied to a short-channel length device. Therefore, the mechanisms of hot carrier generation are explained based on the operating conditions of MOS transistors.

When applying a bias voltage between the gate and substrate terminals \((V_{gb})\) bigger than the threshold voltage \((V_{th})\), an inversion layer (i.e., the channel) is formed underneath the gate oxide. In this condition, if a potential difference \((V_{db})\) is applied across the drain and source terminals of the transistor, a current will flow through the channel. In fact, the channel can be seen as a small resistor. In the linear (or triode) region, the value of \(V_{ds}\) is small when compared with \(V_{gb}\); therefore, the charge distribution and the electric field in the inversion layer are almost uniform along the channel. As \(V_{ds}\) increases, however, the
resulting potential at the silicon surface near the drain decreases and so the carrier density in the inversion layer near the drain. Moreover, if $V_{ds}$ increases so that the MOSFET operates in saturation, a depletion region will be formed next to the drain. This depleted region is called the pinch off-region and originates a non-uniform distribution of charges across the channel [13]. In these two operating conditions, which are the two main situations encountered in analog circuits, electrons can gain much energy from the electric field. In fact, it is possible that carriers with high energy (i.e., the hot carriers), may have high enough energy to overcome the potential barrier between the silicon and the silicon dioxide and penetrate into the gate oxide [14, 15]. Some fraction of these hot-carriers can also break the atomic bonds at the interface of the silicon substrate and the gate oxide and generate allowed states for charge carriers which are called interface traps.

There are some mechanisms that are observed during hot carrier degradation; in a few words, these mechanisms explain the appearance of a finite gate current and the substrate current. Even though there are other mechanisms originating hot carriers, their impact for the MOSFETs considered in this work is not noticeable.

For analysis purposes, a controlled stress procedure is employed in this work, which is mainly based on applying voltages that yield substrate current caused by the drain avalanche mechanism; this occurs when the hot carriers collide with the lattice atoms while traveling from the source to drain terminals and generate electron-hole pairs. These electron-hole pairs also gain high energy due the electric field in the channel region and produce new electron-hole pairs; this is similar to the avalanche process in a reversed biased p-n junction. During the same process, the energetic carriers can impinge on the atomic bonds at the interface of the substrate and at the gate oxide or inside the oxide. Eventually, a break down may occur due to this process, thus creating dangling bonds. As a result, new electronic states are created at the interface and affect the electrical performance of the device. In an nMOSFET, the extra electrons generated by the avalanche process are collected by the drain, and the generated holes go through the substrate terminal to form the substrate current $I_{sub}$ [17]. Since the hot carrier degradation is not a new topic in MOSFETs, important attempts to diminish its effects have been done; one of them is the development of the Lightly Doped Drain MOSFET (LDD MOSFET) observed in [19] and briefly discussed in the following section.

### 1.7 Lightly doped drain MOSFETs

In order to reduce the hot-carrier induced effects, the doping profile of the drain and source regions are modified in such a way that the electric field in the pinch-off region is reduced by introducing a narrow, lightly doped n-type region between the channel and the n+ drain/source diffusion regions. These are the so called LDD regions. Using this modified
structure, the peaks of the electric field occurring at the drain-to-channel and source-to-channel transitions is reduced by spreading the field into the n-regions. Therefore, it is possible to achieve shorter channel lengths while maintaining the same $V_{ds}$ voltage, or even using higher power supply voltages avoiding hot-carrier generation at the pinch-off region. As a result of reducing the electric field, impact ionization is also reduced. For the same reason, avalanche breakdown also occurs at higher $V_{ds}$ voltages, alleviating the fall-off of $V_{th}$ due to short channel effects. The main disadvantage associated with this structure, however, is the increasing of the MOSFET parasitic resistance in series with drain and source terminals. This effect has to be studied in detail for device optimization and it should be accounted for when performing device simulations [19].

1.8 Motivation of this work

The study of reliability in MOSFETs is necessary firstly because of its wide use in current applications and its potential to continue boosting the implementation of high-speed electronic systems. Due to this, MOSFETs are currently being operated at frequencies in the order of many gigahertz. Therefore, when using MOSFETs as amplification devices as in analog applications, small-signal models are required. Unfortunately, there is no general small-signal model valid for any operation condition, geometry, and level of degradation. In fact, some models proposed to cover all these aspects are very complex; in contrast, some others are widely used due to their simplicity but presenting limited accuracy.

On the other hand, the main problem that comes with new technologies using nanometric MOSFETs is the generation of hot carriers. Despite the degradation due to this carriers is well known, the corresponding impact on the high-frequency features of MOSFETs is a relatively new topic. This is because the methods and analyses applied in the past for micrometric MOSFETS are not suitable for the new nanometric devices. This is one of the reasons behind the proposals presented in this work.

1.9 Objective

Within the scope of this M.Sc. thesis, different objectives were established. Firstly, performing and developing a measurement and controlled stress procedure for an RF nanometric-MOSFET. An additional objective is proposing a simple small-signal model accurate for frequencies up to 20 GHz. In this case, the model can be implemented using measured S-parameters so that the corresponding characteristics can be quantified before and after degradation using RF tools such as the Smith Chart. From this, a detailed analysis of the impact of hot carrier degradation on every parameter within the small-signal model is
performed allowing to predict the possible fails that occur when the transistor is exposed to electrical stress.
Even though the impact of hot carriers on the performance of MOSFETs has been thoroughly studied during the past decades, research in this topic has been focused mostly to DC operation. Nonetheless, with the wide use of these devices under high-frequency signal stimuli, paying attention to the impact of hot carriers on the MOSFET features considering AC operation is taking importance. For this reason, it is necessary to include in this thesis a review of the most relevant work available in the literature related to characterizing and modeling of RF MOSFETs under hot carrier stress. This review covers some of the most significant contributions in this topic discussing their corresponding advantages and disadvantages.

2.1 Analysis of 300 nm nMOSFET up to 20 GHz (2002)

In [25], the authors Naseh and Deen analyzed the effect of the degradation by hot carriers on the cutoff frequency ($f_T$), the maximum oscillation frequency ($f_{\text{max}}$), the transconductance ($g_m$), and the threshold voltage ($V_{th}$). In this work, the authors established the maximum degradation time in an empirical fashion. Regarding this, the results were obtained from measurements performed to a multifingered 300-nm LDD nMOSFET with a total width of 120 μm. The experimental setup is similar to the one used in this thesis and consists of an SPA interconnected with a VNA so that it is possible to apply DC bias

Fig. 2.1 Normalized $g_m$ versus time for three different bias points (i.e., different drain current for each bias point). Notice that the reduction of $g_m$ ($-\Delta g_m$) is higher after longer stress time. Stress condition: $V_d = 3.7 \, \text{V}$, $V_g = 0.65 \, \text{V}$ [25].
Fig. 2.2 Normalized $f_T$ versus time versus time for three different bias points (i.e., different drain current for each bias point). Notice that the reduction of $f_T$ ($-\Delta f_T$) is higher after longer stress time. Stress condition: $V_d = 3.7$ V, $V_g = 0.65$ V [25].

Fig. 2.3 Normalized $f_{\text{max}}$ versus time versus time for three different bias points (i.e., different drain current for each bias point). Notice that the reduction of $f_{\text{max}}$ ($-\Delta f_{\text{max}}$) is higher after longer stress time. Stress condition: $V_d = 3.7$ V, $V_g = 0.65$ V [25].

voltages while the S-parameters are measured. The frequency sweep ranges from 50 MHz to 20 GHz. On the other hand, in order to define the DC stress conditions, $V_g = 0.65$ V and $V_d = 3.7$ V, a bulk current was established with a magnitude between 10 to 15% that of the drain current since it is assumed that $I_b$ is caused by impact ionization. This way of establishing the stress current is a standard for degrading the MOSFET under controlled conditions [28]; for this reason, it is followed in this thesis as will be seen later.

As expected, all of the analyzed parameters suffer a substantial change due to the effect of hot-carriers. The importance of this article is that using the small-signal model, the authors are capable to explain the effects of hot-carriers in the RF main figures of merit. In this case, a more accentuated impact is observed in $f_T$ and $f_{\text{max}}$ than in $g_m$, which is explained by the increase with stress time of the capacitance between the gate and source terminals ($C_{gs}$). Figures 2.1 to 2.4 show the experimental data corroborating this effect. All
Fig. 2.4 Normalized $V_{th}$ versus time. Notice that the increase in $V_{th}$ ($\Delta V_{th}$) is higher after longer stress time. Stress condition $V_d = 3.7$ V, $V_g = 0.65$ V [25].

of these figures present normalized curves that are obtained by dividing the reduction ($-\Delta$) in the value of the considered parameter after degradation by the original value (i.e., value when the device is fresh); then, the corresponding impact can be assessed.

As a result of stressing a MOSFET during 2,000 seconds, the following changes in the figures of merit were observed: 9% of reduction for $g_m$, 15% of reduction for $f_T$, 20% of reduction for $f_{max}$, and 7% of increase for $V_{th}$. An interesting observation is that once the device is degraded, the reduction in $g_m$, $f_T$ and $f_{max}$ becomes almost independent of the bias condition since the experimental points plotted in Figures 2.1, 2.2, and 2.3 converge at the far right of the graph. This is not explained by the authors but it is attributed to the fact that the performance of the device is severely diminished after degradation and the figures of merit cannot be substantially improved even modifying the bias point.

In order to identify and analyze the impact of hot-carrier induced degradation on the small-signal properties of a MOSFET, the equivalent circuit model shown in Fig. 2.5 is used. The reason for using this model is because once the parameter extraction is done, the change in the corresponding parameters after degradation will allow to identify the regions within the device and the features most significantly affected by hot carriers. In this regard, the authors found that the junction capacitances between the gate and the drain and source terminals are significantly impacted by hot-carrier induced stress. This points out the fact that the traps and degradation of the oxide layer will be affecting the small-signal behavior by changing the output features of the transistor; this is logical. However, as will be shown later in this document, the main impact in the DC and RF performance of the nMOS is more related to changes in the inversion channel intrinsic parameters, which are the channel resistance and the transconductance.
In order to assess the impact of hot-carrier induced degradation on MOSFET’s small-signal behavior, once the model parameters were extracted by applying the methods in [29] and [30], it was possible to plot $C_{gs}$ and $C_{gd}$ versus degradation time in Figures 2.6 and 2.7. It is observed in this case that the junction capacitance from gate to drain did not suffer any change after the degradation. On the other hand, the junction capacitance in the source side suffers an exponential degradation, and the question that arises is how this will affect $f_T$ and $f_{max}$.

Afterwards, using the obtained capacitance versus time curves and the extracted $g_m$, calculated and experimentally determined $f_T$ data were found to be accurately correlated; this is important because in the RF context, the main figures of merit are $f_T$ and $f_{max}$. For comparative purposes, the authors of this article as well as the authors of the rest of the articles calculate these figures of merit with the same following equations no matter the
frequency or the characteristics of the device. For the cutoff frequency:

\[ f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})} \]  (2.1)

Likewise, \( f_{\text{max}} \) was directly obtained using:

\[ f_{\text{max}} = \frac{f_T/2}{R_g \times \left( g_m + \frac{2\pi C_{gd} g_m}{C_{gs} + C_{gd}} \right)} \]  (2.2)

As can be seen, these figures of merit are related to the parameters of the small-signal model. For this reason, the explanation of the degradation in \( f_T \) and \( f_{\text{max}} \) can be conveniently performed through a small-signal analysis.

In conclusion for this article, the authors quantitatively analyze the transconductance decreasing as well as the \( V_{th} \) increasing due to the degradation in the gate capacitance, which is due to the hot carrier degradation of the gate oxide. Furthermore, they observed that \( f_T \) and \( f_{\text{max}} \) will also be impacted, which is assessed indirectly by observing the increase of the \( C_{gs} \) capacitance explained before [25]. Bear in mind, that in the paper revised in this section, a relatively large device was considered. Therefore, in case that the same stress procedure is implemented on a smaller device, a degradation considering the same stress currents for 2,000 seconds is extremely high. Another remark about the analysis presented in [25] is the fact that the small-signal model is obtained; nonetheless, the impact of the degradation is not associated directly to the S-parameter data, which would be very helpful for analyzing the transmission and reflection characteristics of the device when fresh and when presenting degradation. On the other hand, the total degradation of \( V_{th} \) that can be compared with the rest of the reported analyses reviewed in this thesis is very small.
and therefore there are other effects such as the asymptotic behavior in the degradation that could not been seen.

2.2 Analysis of a 120-nm nMOSFET up to 5.8 GHz (2006)

In [20], Huang and Chang studied the effect of hot carriers on the main figures of merit of RF MOSFETs. Similarly as in the previously studied case, the authors are interested on the small-signal MOSFET behavior. Thus, they focus on the transconductance since other important figures of merit like $f_{\text{max}}$ and $f_r$ are directly dependent on $g_m$ (please see equations (2.1) and (2.2)). Notice that although this seems to be a more particularized analysis, the corresponding effect on some important characteristics of the MOSFET at high frequencies can be inferred by observing the changes of $g_m$ with time when hot carriers degrade the device. In this case, it was found that after the device goes through degradation induced by DC currents, these figures of merit suffered more seriously by the oxide breakdown (OBD) caused by the sudden overpower than by hot carriers stress (HCS) induced by DC currents. This impact of these two undesired effects under small-signal operation is clarified and explained by using an equivalent circuit model. At this point, it is necessary to mention that in [20] a smaller device than in the work revised in the previous section was used and also the effect related to instantaneous high RF power stress is analyzed (i.e., which causes OBD)).

The experiment was performed to 130-nm RF CMOS transistors presenting a 2-nm gate oxide thickness. In this case, for inducing HCS degradation to a fresh device in a controlled way, a bias of $V_g = 1.2$ V and $V_d = 1.4$ V was applied for a total time of 15,000 s. In a parallel experiment performed also to a fresh device, to analyze the OBD effect a bias of $V_g = 3.9$ V and $V_d = 0$ V was applied. For the latter case, the oxide-breakdown was
caused using a threshold on-stress current of 1 mA. The results show that the oxide breakdown impacts greatly the device’s performance, especially increasing the “off” current flowing from drain to source ($I_{DS}$). In Fig. 2.8, the curves corresponding to the drain current and the transconductance before and after stress are shown. Notice in this figure that the transconductance also presents a change after degrading the device using the procedure used by these authors.

For all the devices analyzed with these two kinds of degradation, the result is the same, the effect of the sudden overpower signal in the gate terminal deteriorates significantly more the oxide bonds than what the hot-carriers do. In order to examine and corroborate this, the authors used the small-signal model shown in Fig. 2.9. The main parameters of this model are directly extracted by using Y-parameters [31].

The small-signal model used to assess the impact of degradation considers the effect of the substrate, as well as the dependence of the drain and source resistances on the gate bias. From the extraction of the small signal model parameters, the Table I was constructed, where it is shown the impact on the small-signal parameters. Once again, it is noticed that the impact corresponding to hot-carrier as well as to oxide-breakdown is more significative in the intrinsic part of the device: $R_{ch}$.

From the extracted small-signal parameters, it is observed that most of the extrinsic parameters did not suffer any change at all. The main affected parameter of this type is the

<table>
<thead>
<tr>
<th></th>
<th>$R_s$ (Ω)</th>
<th>$R_d$ (Ω)</th>
<th>$R_g$ (Ω)</th>
<th>$R_ch$ (Ω)</th>
<th>$C_{gd}$ (pF)</th>
<th>$C_{gs}$ (pF)</th>
<th>$C_{ds}$ (pF)</th>
<th>$C_{jd}$ (pF)</th>
<th>$C_{bk}$ (pF)</th>
<th>$G_{mo}$ (mS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fresh</td>
<td>1.7</td>
<td>7.71</td>
<td>3.51</td>
<td>75</td>
<td>1400</td>
<td>0.0574</td>
<td>0.215</td>
<td>0.38</td>
<td>0.358</td>
<td>3</td>
</tr>
<tr>
<td>After HC</td>
<td>1.7</td>
<td>7.89</td>
<td>3.52</td>
<td>76.2</td>
<td>1400</td>
<td>0.0578</td>
<td>0.239</td>
<td>0.38</td>
<td>0.358</td>
<td>3</td>
</tr>
<tr>
<td>After OBD</td>
<td>1.84</td>
<td>7.76</td>
<td>3.51</td>
<td>68.7</td>
<td>1400</td>
<td>0.0578</td>
<td>0.221</td>
<td>0.38</td>
<td>0.358</td>
<td>3</td>
</tr>
</tbody>
</table>
junction capacitance located at the source side, but the change in this element is small when compared to the change observed in $R_{ch}$ and $g_m$. Most of the authors consider that the main impact of stressing the device is reflected in the junction capacitances at the gate to source/drain; however, as it will be shown later in the analysis carried out in this project, this degradation is not as important as that associated with the intrinsic parameters.

It is important to notice that there is no S-parameters analysis in this paper, and the parameter extraction is made for a single frequency of 5.8 GHz. Hence, it should be interesting if a correlation between measured and simulated S-parameters for a certain range of frequencies is performed. Also, there is no explanation of the bias chosen for the hot-carrier method applied or the reasons for the considered stress-time.

### 2.3 Analysis of a 180-nm nMOSFET up to 5.26 GHz (2010)

In [23], Chien-Hsuan et al. consider DC induced and instantaneous RF power induced stress to cells of nMOS transistors fabricated in a 180 nm triple-well 1P6M CMOS process. Bear in mind that both types of degradation, DC and RF stressing procedures originate hot carriers and oxide breakdown. This paper explores both cases. For this purpose, the drain current, threshold voltage, output power, and power-added efficiency were degraded after the output power exceeded the power capacity. At this condition, the voltage between drain and gate is large and originates oxide breakdown. A load-pull system was used to perform the measurements for optimized input and output power matching conditions. All of the characteristics of the devices were measured at 5.2 GHz. In Figure 2.10, it is shown the experiment setup. The importance of this article is that the instantaneous high RF power stress is explained with more detail.
In the measurement setup, the output power yields a high voltage swing and high current density so that a significant amount of hot carriers is present in the channel. In this setup, the calibration consists of determining the reflected input power and output power by power meter with a calibration substrate.

The studied power cell was a 64-finger transistor module with total width of 320 μm. The bias condition of the designed cell was \( I_d = 83 \) mA at \( V_{gs} = 1.2 \) V and \( V_d = 1.8 \) V. Two experiments were done to compare the degradation under different stresses. For DC stress, the cell was biased with at high voltage of \( V_{gs} = 1.8 \) V and \( V_{ds} = 2.5 \) V for 90 minutes. At this condition, the drain current was 155 mA. Therefore, the current density and lateral electric field increase to expedite the hot-carrier generation.

For RF stress, the input power was set to 4 dBm and the source and load tuner were set to optimize the power match. With the input power of 4 dBm, the cell delivered an output power of 17 dBm with a reflection coefficient near 1 with a phase of \(-132\) degrees. All influence of the harmonics, distortion, and gate voltage swing were considered, while emulating the real situation of the cell within a power amplifier. The drain voltage was sinusoidal varying between 0.6 and 2.94 V with a drain-current presenting values between 7 and 151 mA. In other words, the gate voltage swing was amplified and out of phase with respect to the drain signal and increased the electric field at the gate oxide [32].

After 90 minutes of DC stress, the degree of degradation in the drain-source current reached 10% (i.e., it was reduced to 90% of its value when the device is fresh), while the RF stress yield a degradation of 18%, this is shown in Fig. 2.11. After 90 minutes of DC hot carrier stress, it was observed a shift in \( V_{th} \) of 0.04 V, and the output power decreased to 16 dBm, but the optimum load reflection coefficient did not substantially change [33].
A good process and analysis for RF stress is performed in this paper, showing that the effect of RF stress is more accentuated than the effect due to the DC biasing; however, this analysis does not have a model with parameters for a deeper understanding of the overall impact on the transistor’s performance. However, an interesting idea is introduced to represent a damaged transistor. The model that is employed in this paper is a two-transistor in series model (Fig. 2.12), where one transistor represents the stressed cell with a larger threshold voltage and the other transistor has a diminished source-drain punch through voltage due to the reduction of the effective channel length [34].

This work is an example of an alternative way to analyze hot-carrier induced degradation without obtaining the S-parameters. It was observed that the true corroboration of the hypothesis and of the model is based on simulations; however, for an RF MOSFET the small-signal model that allows to predict the behavior for different frequencies is very necessary and in this case. Unfortunately, this model is not explored in this paper.

**2.4 Analysis of a 40-nm nMOSFET up to 10 GHz (2011)**

In [24] Negre et al. performed again an investigation of RF parameter degradation under both DC and RF stress. Degradation kinetics of the main parameters is physically explained and modeled using a PSP compact model to predict the behavior of the stressed devices. The importance of this work is that a compact model to predict the degradation is developed and also that the device is the smallest of all of the reviewed.
The experiment consists of using a passive load pull setup to apply DC and RF stress on the device and periodically interrupting for DC and RF measurements (Fig. 2.13). The parametric analyzer and the synthesizer are used to apply respectively DC and RF stress components on the device. For the measurements, the parametric analyzer and the VNA are used to monitor respectively DC parameters and S-parameters form 1 GHz to 50 GHz. A power meter is used to monitor the power level delivered by the synthesizer, and the impedance tuners are used to control the impedances presented to the device. The use of switches allows to automatically calibrate the setup, extracting and applying the RF signal and measuring the S-parameters of the device. The device consisted on a common-source-configured nMOSFET with gate length of 40 nm and a total gate width of 57.6 μm with 10 fingers.

In this case, a DC bias is applied for hot-carrier induced degradation while an RF signal was applied to the gate or the drain. The stress consisted of DC voltages of $V_g = 1.8$ V and $V_d = 1$ V, while an RF power input of 9 dBm at a frequency of 1 GHz is generated on the drain. The equivalent time domain voltage applied to the drain presents a peak value of
Fig. 2.15 DC parameters drift for a stress condition of $V_g = 1.8$ V and $V_d = 1$ V RF power of 9 dBm at 1 GHz. The aging model (lines) has been established from DC stress to predict the drift under RF stress. [24].

1.8 V. The stress is interrupted five times per decade to measure the threshold voltage, the maximum transconductance, the linear and saturation currents, as well as the S-parameters at a set of bias points. Once again, the authors do not provide details on the steps followed to determine the stress time or bias conditions. Furthermore, the model used in this work (see Fig. 2.14) does not consider the impact of the substrate parasitics; therefore, it is only suitable for frequencies up to 10 GHz [27].

According to this analysis and as expected, $C_{gd}$, $g_m$, and $G_{ds}$ are the most impacted elements. The change in the later parameters can be explained by its association to the threshold voltage. Thus, as the oxide layer between the gate and the inversion channel starts to degrade, the broken bonds due to the hot-carriers enter into this interstitial layer and more voltage is needed to develop the necessary electric field to create the channel. Therefore, when comparing this new state with the fresh and original one, an increase in the resistance of the channel is observed since more voltage is needed to obtain the same current from the source to drain terminals; in addition, a reduction in the direct gain from gate to drain or transconductance is exhibited [35]. Fig 2.15 shows the corresponding results.

The degradation in $C_{gd}$ is explained by the introduction of interface states in the drain area [36]. In Fig 2.16 the main impacted elements of the small-signal model identified above are plotted versus $V_g$ to see the change in the corresponding curves. One of the most important ideas discussed in this study is the introduction of an ageing model based on the shift of DC parameters. The level of degradation undergone by the device follows a power law dependence on the stress time. This dynamic is attributed to the generation of interface states; thus, the total degradation can be expressed by equation (2.3).
Fig. 2.16 Extracted (symbols) and simulated (lines) RF parameters before (black) and after (red) 1000 s of RF stress [24].

\[ \Delta = \left( \sum_i A_i \frac{1}{t} \right)^n \]  

where \( \Delta \) is an indicator of the level of degradation, \( A \) is a parameter dependent on the device processing technology, geometry, and bias voltage conditions [24]. It is necessary to consider that most of the terms in this equation are proposed to fitting measured with simulated data. Anyhow, it is true that the behavior of the degradation is similar in all the parameters (as will be seen in further chapters of this thesis) and it follows a power law behavior, but the final equation that predicts this degradation for all kind of devices is still not available in the literature.

The second most important contribution of this study is that it is shown for the first time a correlation between simulated and measured S-parameters for two bias conditions (linear and saturation) before and after degradation, as it is shown in Fig. 2.17. The analysis is very practical and useful, especially the part related to the hot carrier induced degradation. However, it is required an improvement of the small-signal model used for the analysis since the substrate elements was neglected in this paper. However, even with this inconvenience the main impact is found to be in the intrinsic elements related to the transconductance and the channel resistance.
2.5 Analysis of a 150-nm nMOSFET up to 20 GHz (2011)

In [26], Sagong et al. explained the hot carrier-induced degradation with a modified surface channel resistance model that can be applied to both, conventional SiO$_2$ and high-k nMOSFETs. This new model is combined with the small-signal model built from DC and RF measurements. The device considered for RF characterization is a two-finger nMOSFET with a total width of 40 um and a channel length of 150 nm.

The hot carrier degradation process consists on applying stress bias conditions of $V_{gs} = V_{th} + 2$ V = 2.5 V, and $V_{ds} = 2.3$ V for 2,000 s with another 2,000 s of relaxation. These conditions allow to compare the degradation for a high-k/metal gate as well as for a silicon-dioxide-isolated gate MOSFET. The small-signal model used in this work is shown in Fig. 2.18 and considers the effect of the substrate losses in the S-parameters; therefore, the accuracy of this model allows its application up to 20 GHz [37].
In this approach, for analyzing the degradation of the channel resistance, a division into two separate parts is considered as illustrated in Figure 2.19. The nomenclature used in Fig. 19 considers $L$ and $W$ the length and width of the device, respectively, $C_{ox}$ the gate oxide capacitance per unit area, $V_{ac}(X)$ the applied AC voltage, and $V_m$ the amplitude of the AC voltage. Thus, it is expected that after hot-carrier induced degradation, the bulk trap density ($N_{ot}$) and the interface trap density ($N_{it}$) increase near the drain region, which in turn increase $R_{ch,d}$ and decrease $R_{ch,s}$ [26]. The variation of these resistances was confirmed by verifying the variation in the extracted terminal resistances $R_d$ and $R_s$. This is possible since the access resistances at the drain and source terminals include part of the damaged channel resistance near each junction. Thus, the damage near the drain region is seen as an increase in the terminal resistance $R_d$ while $R_s$ decreases due to the increase in the source-side effective potential. In turn, $C_{gd}$ decreases while $C_{gs}$ increases after hot-carrier stress. These changes are confirmed by the results obtained from RF measurements.

For the case of high-k nMOSFET, both $R_d$ and $R_s$ values increases after stress. This effect is caused by charge trapping near the source in conjunction with hot-carrier injection in the drain. However, the calculated values for the effective capacitances $C_{gd}$ and $C_{gs}$ significantly differ from the measured results and that is why variations in $C_{gg}$ (2.4) should consider a separate fitting parameter to explain the hot-carrier induced device degradation [26]. Mathematically, the following expression can be used for this purpose:

$$C_{gg} = \frac{C_{ox}}{(1 + g \cdot R_s)^2} \quad (2.4)$$

where $R_s$ is the series resistance including the effective gate, channel, and substrate resistances, and $g$ is the effective conductance related to the gate direct tunneling leakage.
The variations in the parameters extracted from the simulation are in close agreement with the variation of the measured parameters (Table II). The measured Y-parameters before and after hot-carrier stress match well with the simulated Y-parameters.

As it is shown in Table II, there are some differences in the degradation of a SiO$_2$ nMOSFET compared to an HfO$_2$ nMOSFET. For the purposes of this work, we are going to focus in the first type. It is still true that the most impacted element of the small-signal model is the channel resistance; however, in this work the authors found a significant impact of hot-carrier degradation in the terminal resistances, even surpassing that corresponding to the transconductance. The explanation of the great impact in the terminal resistances as explained before is the channel resistance degradation focused near the terminals. In other words, there is no change at all in the actual terminal resistances, the change that is seen in the corresponding small-signal parameters is the effect occurring in the channel resistance near the drain and near the source terminals. For the case of the transconductance, the small degradation obtained compared to the channel resistance is not expected. Analyzing the case of the high-k transistor, the degradation in the transconductance is similar to that in the channel resistance, which is in agreement with the results obtained in this thesis and in the previous works reviewed; therefore, this is probably an error in the extraction method.

Some important aspects are taken from this paper, besides the main approach of this investigation is for high-k nMOSFETs. Here, it is introduced a relaxation time after stressing, and the explanation of the changes in the terminal resistances due to the non-homogeneous degradation along the channel resistance. Also, an important conclusion is that the effect of the hot-carrier induced degradation is more severe in high-k devices (Table II).

2.6 Conclusions of the chapter

In this chapter, relevant research dealing with small-signal model extraction considering hot carrier induced degradation was revised. It is important to remark the fact that the reasons

<table>
<thead>
<tr>
<th>RF parameter</th>
<th>SiO$_2$ nMOSFET</th>
<th>HfO$_2$ nMOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$ (%)</td>
<td>Measured: -4.6</td>
<td>Simulated: -4.5</td>
</tr>
<tr>
<td>$R_{ch}$ (%)</td>
<td>-18.3</td>
<td>-19.1</td>
</tr>
<tr>
<td>$C_{gg}$ (%)</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>$C_{gd}$ (%)</td>
<td>-7.1</td>
<td>-7.1</td>
</tr>
<tr>
<td>$R_{d}$ (%)</td>
<td>2.8</td>
<td>2.9</td>
</tr>
<tr>
<td>$R_s$ (%)</td>
<td>7</td>
<td>7</td>
</tr>
</tbody>
</table>
to use the stress bias conditions for $V_g$ and for $V_d$ or the time used are determined in an empirical fashion. The consequence for this is that after a long period of stress, the impact of the degradation in $V_{th}$ or in the small-signal model parameter is very small. That is why it is very difficult to establish a generalized hot carrier degradation process. On the other hand, it is noticed that the few reported stress processes are applied for relatively large transistors; therefore, as will be seen in the next chapter, this process has to be adapted for the new generation of sub-100 nm channel length nMOSFETs.

Another main idea obtained from these previous studies is that the small-signal model applied has to consider the influence of the substrate parasitics in order to be accurate for frequencies up to 20 GHz. If a good stress process is applied, a better approach for the parameters will be obtained and then it is possible to observe an impact in the S-parameters after the hot-carrier degradation. From the results observed in previous research, the major degradation indicator is the shift in the threshold voltage, the transconductance, and the channel resistance, which can be thoroughly analyzed from small-signal collected data. Finally and for future work, it is important to mention the importance to study in a similar way the RF degradation inducing soft-oxide breakdown [23][24][25] and also considering high-k materials [26] because the impact is more accentuated in this case and it is presented in most RF MOSFETs.
This chapter is dedicated to explain the experiments performed in this project to analyze the impact of HC degradation on the small-signal features of RF-MOSFETs; the explanation includes the description of the analyzed devices. The objective in mind was the development of a systematic process that allows quantifying the degradation by hot-carriers on a MOSFET using the equipment available in a microwave laboratory.

The device considered here is a multi-fingered RF nMOSFET with a channel length of 80 nm presenting a common source configuration and embedded within ground-signal-ground RF pads with a 150-μm pitch. These pads make the device VNA-measurement compatible in order to facilitate the measurement of S-parameters using RF coplanar probes, which allow the determination of the main impacted electrical features through a small-signal model parameter extraction. For this purpose, the resources available at the High-Frequency Laboratory of INAOE are the following:

- Agilent B1500A semiconductor device analyzer (SDA, also known as SPA for semiconductor parameter analyzer),
- Agilent E8361A precision network analyzer (PNA, also generically known as VNA),
- Karl Suss PA200 workstation for on-wafer device measurement,
- computer with Agilent’s IC-CAP (IC characterization and analysis program) software to control the measurement equipment via a USB compatible GPIB (general purpose interface bus) cable, and
- RF and DC cables and probes.

While establishing the characterization procedure, the first step was to define the time during which the device will be stressed as well as the bias conditions that will be applied to the source-drain and gate terminals. In this project, the first approach to begin with the device characterization consists on a procedure that is based on the one proposed in [25]. Thus, device degradation was performed though the application of a source-drain bias so large that the measured bulk current corresponds to 16% of the drain current. This condition is maintained for 2,000 s after which S-parameter measurements are taken to analyze the impact on the small-signal device features. The degradation and subsequent small-signal parameter characterization is performed several times always considering intervals of 2,000 s. The obtained results, shown in Fig. 31, indicate an enormous device degradation for the first 2000 s, and an asymptotic behavior of the corresponding curves for the last 2000 s.
These results help to visualize that a more refined procedure is necessary to quantify the progress through time of the device degradation. For this reason, smaller degradation time intervals as well as a smaller current to generate hot-carriers stress are necessary to obtain more useful results. In this regard, the proposed solution was to perform preliminary DC experiments in identical devices such as those to be characterized at high frequencies. Thus, by observing the degradation of the DC features of these devices as a function of time, the stress time as well as the optimal degradation current we determined. This will be explained with more detail later in this chapter.

3.1 The device under test

Sketches providing information about the considered devices under test are shown in Fig. 3.2, whereas Fig. 3.3 shows the image of the DUT’s top view obtained using a microscope. The available devices were designed and fabricated in IMEC, Leuven, Belgium, and are contained in dices within a quarter of wafer donated to INAOE. For every device and on the same dice are also the de-embedding structures, a special feature of this device is that it counts with a shielding under the interconnections and the silicon board; this shielding avoids the coupling between the pads through the substrate of the transistor especially at high frequencies. Also, there is a big area underneath the shielding, which is connected to the DC bias probe, this means that the bulk is separate from the source which allows applying a DC bias at the same time while the RF measurements are taken.

The characterized device is an n channel CMOS in common source configuration with a separate bulk terminal for the substrate DC bias of type p. This RF-nMOS is on the technology scale of 80 nm which means a channel length approximately of 80 nm with a channel width of 3 um multi-fingered with a total number of 64 fingers. As it is shown in
Fig. 3.2 Simplified sketches showing the DUT’s layout (left), and the cross section considering only two fingers and indicating the parasitic BJTs formed between the S/D junctions and the substrate (right).

Fig. 3.3 Picture showing the image of the DUT’s top view obtained using a microscope.

Fig. 3.2, the device is a multi-fingered MOSFET, and therefore there is a parasitic current path through the bulk represented with the junction transistors, this represents a minor change compared with a single finger device, as the effect of these parasitic transistors is considered in the small-signal model [44].

3.2 DC experiments

As mentioned before, during the proposal of the characterization methodology, two configurations setups were employed: one is simpler and only for DC measurements, the other is more complete and includes DC with RF stimuli and measurements. The DC setup is described in this section.
The DC setup is needed to establish the specifications for degradation through HC-induced stress, and the conditions to be applied to the DUT before the measurements involving RF equipment. Fig. 3.4 shows a sketch illustrating the DC setup, whereas Fig. 3.5 shows a picture taken during a measurement session indicating the SPA and the workstation with microscope. Another picture allowing to see details of the on-wafer probing is shown in Fig 3.6a. Fig. 3.6b shows a camera view of the pads being contacted by the probes.

For performing the DC measurements, the source/monitor units (e.g., SMU1 to SMU4) of the SPA are connected to the probe holders that allow applying stimuli to the DUT and measure the response. As previously discussed in Chapter 1, the Kelvin principle for measurement allows to eliminate parasitic effects of the cables and series resistances. In Fig 3.6a the DC probes are placed on the wafer and Fig 3.6b shows how the DUT looks with the DC probes landed on the drain, source, and bulk and gate pads (not labeled).

The nMOSFET used for these DC measurements was a transistor configured so that four pads are used to separately access the source, gate, drain, and bulk terminals. This
device presents a channel length of 120 nm and a total width of 10 μm. It is important to mention that this device was part of an array designed to obtain the DC characteristics of the MOSFETs in the fabrication process; this it is a single-gate-electrode device (not multi-fingered). Following with the description of the experiment, and in accordance with the discussions in Section 2.1, the bias conditions for $V_g$ and $V_d$ to induce HC-related degradation to the device are defined by considering the relationship between the bulk current caused by impact ionization and the hot carrier induced degradation. Therefore, after observing that the considerable degradation achieved after 2,000 seconds of stress with bias conditions obtained by maintaining a bulk current equal to a 6% of the drain current, more useful stress conditions were searched. Otherwise, the progress of the degradation with time cannot be appropriately analyzed. After several tests carried out in an empirical but systematic way, a bulk current approximately to the 1% of the drain current was defined to degrade the device. Fig. 3.7 shows the voltages applied to achieve this condition in a fresh (i.e., not previously stressed) MOSFET. It is very important to mention that any source of light should be avoided during the measurement of the DC curves to minimize noise in the obtained data.

Figures 3.8 and 3.9 show the change in the characteristic curves of the device after stressing the device during several periods of time. The curves suffer a dramatic reduction after 1,500 s. However, notice that the selection of 25 s as the period to monitor
degradation is convenient to observe the impact of hot carriers in these curves. An interesting effect is that a higher rate of change in this curves is observed at the first intervals, characterized by a shift in the threshold voltage Fig. 3.9 and a diminished drain current Fig. 3.8 and 3.9. Due to the appropriateness of this time steps, the next step of the experiment uses the same intervals as well as the bias conditions to induce stress.

### 3.3 RF experiment setup

Now that the stress procedure with the required bias conditions and the time intervals was carefully established though DC experiments, the RF measurement setup can be defined for an RF MOSFET considering its different operation regions. To start with the corresponding explanation, Fig. 3.10 illustrates the way the equipment is configured to collect the S-
Fig. 3.10 Sketch showing the configuration of the equipment for measuring the S-parameters to an RF-MOSFET.

parameters of a MOSFET presenting coplanar GSG pads. An actual view of the setup is shown in Fig. 11, where the different equipment employed to characterize the device are included. Notice that in this case a more complex setup is needed when compared with the one used for a DC characterization alone. In fact, electrical interconnection of the SPA and the VNA is required, as well as the connection of the GPIB cable in parallel to simultaneously control both equipments using a computer with IC-CAP software. Regarding the electrical connection of the VNA and the SPE, this is needed due to the fact that the VNA does not provide DC bias to the device and external stimuli should be applied through an internal bias-tee that can be accessed through a module that is located in its rear panel (see Fig. 12). The stimuli is provided by the SPA’s SMU modules, which allow the measurement of the current and voltages present at the device through the RF probes connected to the VNA. This is convenient since no additional probes would be required to apply the device bias for operation after degradation. In order to illustrate the different

Fig. 3.11 Setup for performing RF measurements showing the workstation with microscope, the VNA and the SPA.
connections required to implement the setup, Fig. 12 shows the rear panel of the VNA indicating the different connections to interface the VNA with the SPA. Notice that the coaxial cables connect the force/sense lines coming from the SPA’s SMUs to the VNA’s bias-tee.

Some important considerations must be followed in order to correctly apply the DC stimuli and measure the DC curves using the SPA while it is connected through the bias-tee of the VNA. This is because, as mentioned in Chapter 1, the SPA uses the Kelvin concept that requires separate wires for the force and sense lines. For this reason, the SMUs present tri-axial outputs. In contrast, the VNA bias-tee inputs are coaxial. Even though some penalty in accuracy would have to be paid to resolve this problem, special connectors that isolate the guard terminal of the SMUs and keep the continuity of the SMUs ground with the ground in the VNA ports have to be used. Also, the default ground connector of the SPA has to be disconnected so the ground of the SPA is floated and then the ground of the SPA and the VNA present the same zero potential. In Fig. 3.13 this is appropriately labeled.
Notice in Fig. 13 (right side) that one of the SMUs (SMU3) is dedicated to bias the bulk terminal of the MOSFET. Since the VNA used in this project is a two-port system where the port 1 goes to the gate and the port 2 to the drain terminal, a third probe is required to apply the DC bias (see Fig. 3.10). The latter is directly connected to the SPA without passing through the VNA. In the case of study here, whereas the ground-signal-ground RF probes that are connected to the VNA present a 150-μm pitch, the DC probe connected to the SMU3 of the SPA is specially designed to apply stimuli between the bulk contact and one of the side contacts in the GSG array where the MOSFET is embedded. Bear in mind that all the probes require to present a low impedance so this will not affect significantly the measurements up to 20 GHz. This idea is exhaustively discussed in reference [41].

An important step before starting RF measurements and after setting up the equipment is planarizing the RF probes. In fact, this process consists on guaranteeing that the three RF tips per probe make contact in the DUT at the same time when landing. This is accomplished with the aid of a planarization substrate such as that shown in Fig. 3.15. Thus, by repeatedly landing the probes and adjusting the height of each tip by changing the probe angle it is possible to adjust the probe to verify the tips will contact the all the DUT’s pads applying the same pressure.

After the probes are planarized, the next step is moving the measurement reference
plane up to the end of the probe tips. This step is known as calibration and it consists in a procedure to eliminate the systematic errors in the measurements associated to the parasitic effects introduced by the RF probes and connections. The specific calibration procedure applied here was the LRM (line–reflect–match), because it requires the off-wafer measurement of three high quality structures (i.e., with very low parasitics and very low variation on electrical properties with temperature, time, etc.). These structures are: a transmission line with known phase delay at a given frequency (line standard), a standard for shorting the probe signal tip with the ground tips (short), and a load of 50 Ω to terminate each RF probe (match standard). All of these calibration structures are found in the impedance standard substrate (ISS) provided by the probe manufacturer. In this project, the part number of the employed calibration substrate is 101-190C and it is shown in Fig. 3.16. Individual photographs of the camera views corresponding to each one of the calibration standards while measured by the probes are shown in Fig. 3.17. Thus, using the measured data corresponding to these structures, a mathematical processing is applied to calculate the error terms associated with each port [38]. For this purpose, in order to speed up the measurement process, specialized software can be used to carry out the measurements as well as the data processing. At INAOE, the software used to perform this task is Cascade’s Wincal, which also allows to verify the validity of the calibration.

When the calibration process is appropriately executed, the measured data correspond to the DUT and the parasitic effects from the VNA to the probe tips are removed so that at the edge of the RF probes defines the measurement plane. Fig. 3.18 graphically illustrates this concept.

Fig. 3.16 Calibration substrate (ISS) placed over the chuck of the probe station.

Fig. 3.17 Camera views of the calibration structures while the RF probes are landed (black shadows in the screen).
Once the calibration is done, it is time to perform the S-parameter measurements of the devices at the desired DC bias. In order to do so, the first step is to place the silicon wafer over the chuck and locate the group of devices to be measured. Fig. 3.21 shows the wafer ready to be measured. Afterwards, the RF probes and de DC probe have to be landed over the desired pads on the transistor. Fig. 3.19 shows the user perspective of the chuck after placing the wafer without and with the probes in position to perform the measurements. It is important to notice that the wafer should be appropriately oriented; otherwise, the setup would require a different arrangement.

3.4 De-embedding

The calibration procedure only removes the effect of the systematic errors associated with the measurement equipment. Nevertheless, the pads and other interconnects that serve as interface between the probes and the DUT also introduce errors to the measurements. For this reason, further measurement correction is necessary to eliminate the effect of these transitions that occur on-wafer and are part of the fabricated prototype. Thus, in order to eliminate the parasitic contribution of the DUT internal test fixture it is necessary to apply the so-called de-embedding procedure. Generally, the parasitic effects of the test fixture are removed from the experimental data using a procedure such as that reported in [39]. This is based on the separate measurement of a set of dummy structures fabricate on-wafer and

---

Fig. 3.18 Photograph illustrating the measurement plane after calibration.

Fig. 3.19 Photograph showing the quarter of wafer where the devices are contained: placed over the chuck (left), and with the probes placed to perform the measurements (right).
substituting the transistor by known terminations: open, short, and through. After measuring these structures with the calibrated RF setup, the corresponding parasitic effects can be removed from the experimental data using a mathematical algorithm and the measurement plane is shifted at the level of the transistor. It is important to mention that the efficiency of the de-embedding method is related to the quality of the structures used as well as the consistency of the measurements (e.g., minimum difference in probe landing from measurement to measurement).

Regarding the processing of the experimental data obtained from the dummy structures, substantial noise may be present at either very high (beyond 15 GHz) or very low frequencies (around 1 GHz). In this case, the measurement uncertainty increases as the impedance of the measured structure becomes more different to the system’s reference impedance (usually 50 Ω). Thus, the correct modeling of these structures is crucial to consider high frequency effects such as the skin effect that can be incorporated to the de-embedding process [40]. In fact, it is a common practice to shield the pads from the substrate to reduce the parasitic and avoid to increase the measurement uncertainty; this is achieved because the shield reduces the negative influence of the pad coupling through the substrate. For this purpose a metal layer is formed between the pads and the substrate leaving only a window to interconnect the pads with the DUT.

In this project, to perform the de-embedding the DUT plus the probing pads is assumed to be represented by means of the equivalent circuit shown in Fig. 3.20. This circuit considers the corresponding parasitic effects using generic admittance and impedance blocks $Z_i$ and $Z_o$. These blocks include the series parasitic associated with the pads and the lines interconnecting the test fixture with the DUT. $Y_i$ and $Y_o$ consider the electrical coupling from the signal pads to the ground pads and the shield plane; $Y_1$ and $Y_2$ are used to represent the shunt parasitic occurring at the test fixture to the DUT interface, and finally $Z_s$ is associated with interconnections between the DUT and the ground pads.

The $Z$’s series elements are obtained from the measurement of the short structure and once they are obtained they can be removed. Similarly, the $Y$’s elements are obtained from the measurements of the open dummy structure, and once they are considered the de-embedding process is completed and the parasitic effects from the test fixture are removed from the measured S-parameters.
After performing the calibration and the de-embedding procedures, the next step is to measure the S-parameters. These measurements were performed from 10 MHz to 20 GHz by applying a signal power of –20 dBm, which guarantees small-signal operation and maintains an adequate signal-noise ratio. The S-parameters were collected at three different bias conditions: zero-bias ($V_{gs} = V_{ds} = V_{bs} = 0$ V), strong inversion ($V_{gs} = 0.7$ V, $V_{ds} = 0$ V and $V_{bs} = –1.2$ V), and saturation region ($V_{gs} = 0.7$ V, $V_{ds} = 1.2$ V and $V_{bs} = –1.2$ V).

The intervals for stressing the devices consider short time at the beginning and longer time when the device already presents degradation. In fact, it was observed in several occasions that after 2,000 seconds of stress, the degradation has an asymptotic behavior, which means that the device reaches a limit in its degradation before the total oxide breakdown and the total non-functionality. Therefore, at the beginning of the stressing procedure, the time intervals were 25, 50, 75 and 100 s; afterwards longer time was considered: 150, 200, 300 and 500 s. At the end of the process, the longest stress times considered were 1,000, 1,500 and till 2,000 s. After each stress time, the S-parameters were measured for the three bias conditions defined in the previous paragraph. It is recommended that the full device degradation procedure is carried in one single round of measurements (one laboratory session) and with careful to not cause a critical oxide breakdown; otherwise, the process has to be started again from the beginning using a new fresh device.

### 3.5 Conclusions of the chapter

In this chapter, the necessary steps followed to perform the measurements for the characterization of the impact by the hot-carriers in a deep sub-micrometer RF nMOSFET were defined and detailed described. Most of these steps were performed for the first time.

The software ICCAP helped to simplify the measurement process as it was possible to program the hot-carrier degradation stress periods for the different bias conditions small-signal models. However, it was necessary to be in the place and checking after every stress time period, because the calibration of the RF probes may require some adjustments after long periods of time.
This chapter is dedicated to present and discuss the results obtained after performing the experiments described in Chapter 3. Accurate small-signal models for representing the characterized MOSFETs under three different operation conditions were considered to analyze the high-frequency features of these devices after HC degradation: zero-bias, strong inversion, and saturation region. This chapter also includes a detailed description of the method used to extract the model parameters from the experimental S-parameters. Thus, by observing the changes in the extracted parameters, the effect of hot carriers on the MOSFET’s features is assessed in a quantitative fashion. The validation of these results were corroborated with excellent correlations of simulated with measured S-parameters up to 20 GHz for all the degradation stages.

This represents one of the first efforts to characterize the small-signal features of MOSFETs through equivalent circuit modeling. Moreover, it was performed with consistency for different bias conditions and considering the substrate effects, which makes this method more reliable than previously reported approaches for this range of frequencies. This is possible because one of the advantages of performing analyses using RF measurements is the fact that DC measurements cannot be taken when the device is in off state. The importance of carrying out measurements at this particular condition relies on the feasibility to identify and determine the substrate parasitics in a straightforward way when there is no inversion channel. Thus, by separately analyzing experimental data under different operation conditions and at different degradation stages, relevant information can be obtained to allow the implementation of a small-signal model taking into account device operation conditions that occur within an actual IC. This and other concepts are thoroughly discussed along this chapter.

4.1 Zero-Bias Condition

For the case of the zero-bias ($V_{ds} = 0$ V) cold-FET ($V_{gs} = 0$ V) condition, the effect of the parasite network associated with the substrate is highlighted; this is because the channel resistance is very high; thus, the equivalent impedance between the source and drain terminals through the channel region is comparable to that occurring through the substrate. For the zero-bias cold-FET operation, the equivalent circuit for the MOSFET is shown in Fig. 4.1. It consists of one resistance at the gate or input terminal, another resistance for the substrate and a junction capacitance at the drain side that interconnects the gate and the
substrate with the drain terminal; similarly, for the source terminal the series resistance and junction capacitance are considered.

The equations used to extract the parameters in the model shown in Fig. 4.1 are:

\[
\begin{align*}
-\text{Im}(Y_{12}) & \approx \omega C_{gd} & (4.1) \\
\text{Im}(Y_{22}) & \approx \omega \left( C_{gd} + C_{jd} \right) & (4.2) \\
- \frac{1}{\text{Im}(Z_{22})} & \approx \omega \left( C_{jd} + C_{gs} \frac{C_{gd}}{C_{gs} + C_{gd}} \right) & (4.3) \\
\text{Im}(Y_{11}) & \approx \omega \left( C_{gs} + C_{gd} \right) & (4.4) \\
\text{Re}(Y_{11}) & \approx \omega^2 R_g \left( C_{gs} + C_{gd} \right)^2 & (4.5) \\
\text{Re}(Y_{22}) & \approx \omega^2 R_b C_{jd}^2 & (4.6)
\end{align*}
\]
For these equations, it was assumed that at relatively low frequencies the high-order terms involving powers of $\omega$ higher than 2 can be neglected. Bear in mind, however, that this is valid provided that the device is operated under the zero-bias cold-FET condition [41].

As the device is in off state, there is no inversion channel and the device is reciprocal since no gain occurs between the gate and drain terminals. This is corroborated from the measured S-parameters: $S_{21} = S_{12}$, which also indicates that the device in this condition behaves as a passive linear network. Fig. 2 shows measured data plotted in a Smith Chart illustrating that even after long time of stress the S-parameters exhibit almost no change. This experiment points out the fact that since the device’s intrinsic parameters play no role under this operation condition, the effect of HC degradation is not evident at $V_{ds} = V_{gs} = 0$ V.

From the S-parameters measured before and after the degradation intervals, it is observed in Figure 4.2 a small progressive shortening of the curves corresponding to the reflection parameter at the input of the transistor (i.e., $S_{11}$), which is interpreted as a reduction of the input impedance attributed to the impact of HC-induced degradation on the junction capacitances $C_{gs}$ and $C_{gd}$. However, as it will be shown, the degradation in these junction capacitances is not permanent. To experimentally verify this fact, a measurement in the same device was performed after a considerably long relaxation time (one week after degradation). The corresponding S-parameters shown in Figure 4.3 exhibit almost no change when compared to the ones obtained when the device was fresh.
For the model parameter extraction, the procedure reported in [41] was followed. The corresponding linear regressions used with this purpose are shown in Fig. 4.4 where data up to 4 GHz was used. This upper frequency limit is determined empirically by observing the highest frequency at which the experimental data plotted either versus $\omega$ or $\omega^2$ show linearity (depending on the equation used for the extraction). The deviation of these data from a straight line at higher frequencies is due to the fact that the expressions (4.1) to (4.6) neglect the effect of $C_{js}$ by assuming $j/\omega C_{js}||R_b \approx R_b$, which is only valid up to some gigahertz. The extractions in Fig. 4.4 show good linearity and allow an adequate parameter extraction when data up to 4 GHz are used.

When analyzing the extractions performed to obtain the small-signal model parameters at different degradation stages, it is observed that there is no substantial change at this particular bias condition. This again points out the fact of the small impact of hot carriers in the extrinsic elements including those related to the substrate network.
4.2 Strong inversion at zero $V_{ds}$

The second operation condition for analysis is strong inversion at $V_{ds} = 0$ V. For this scenario, a gate-to-source bias higher than the threshold voltage ($V_{th} = 0.35$ V) is applied ($V_{gs} = 0.7$ V). This voltage should be high enough to guarantee the creation of a well-formed inversion channel. As there is no significant electric field between the source and drain terminal since $V_{ds} = 0$ V, the inversion layer is almost symmetrical and the device remains passive (i.e., $g_m = 0$).

During the experiments, this bias condition was applied to the device while considering two different values for the voltage applied to the substrate. The first case (Fig. 4.5).

![Fig. 4.5 Measured S-parameters for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.]

Fig. 4.5 Measured S-parameters for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.

![Fig. 4.6 Measured S-parameters for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.]

Fig. 4.6 Measured S-parameters for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.
4.5) corresponds to a zero voltage applied to the substrate, and the second one (Fig. 4.6) was obtained with \( V_{bs} = -1.2 \) V. From the measured S-parameters, it is observed that the main difference between this two scenarios is the change in the reflection parameter at the output (drain) port \( S_{22} \), and in the transmission \( S_{xy} \) parameters. For the first case, with \( V_b = 0 \) V, the channel resistance is smaller than in the case when \( V_{bs} \) increases. This is clearly verified by observing the \( S_{22} \) parameter curve, which includes the effect of this resistance and is near the left side of the Smith Chart over the real axis (approaching the short circuit condition) when \( V_b = 0 \) V. It is important to consider this effect for the parameter extraction since smaller values of the channel resistance considerably increase the uncertainty of the corresponding determination using S-parameter measurements.

The dependence of the channel resistance on \( V_{bs} \) was analyzed in [41], which is explained using textbook knowledge related to the threshold voltage shift (from 3 to 3.5 V) caused by the substrate bias. For this reason, to increase the certainty of the extracted values for the channel resistance, the parameter extraction for the strong inversion condition was made for \( V_b = -1.2 \) V. Even though the corresponding value will differ in other bias conditions, the impact of HC-induced degradation can be assessed in a more efficient way when considering this voltage at the substrate terminal.

In order to obtain the value for the channel resistance, it is necessary to remove from the measured data the effect of the parameters extracted at zero bias in the previous section (i.e., \( R_b \) and \( C_{jd} \)), as they are weakly dependent on \( V_{gs} \) [42]. This step is performed by transforming the S-parameters associated with the transistor at the desired bias condition to Y-parameters (represented by means of the Y matrix); afterwards, the Y-parameters corrected from the effect of the substrate parasitics (represented by \( Y^* \)) are obtained by applying the following matrix operation:

\[
Y^* = Y - \begin{bmatrix} 0 & 0 \\ 0 & \frac{\omega^2 C_{jd}^2 R_b + j\omega C_{jd}}{1 + \omega^2 C_{jd}^2 R_b^2} \end{bmatrix} \quad (4.7)
\]

Notice that \( C_{js} \) is not considered in this particular formulation because at \( V_{gs} > V_{th} \) the source series resistance is much smaller than the reactance associated with this capacitance at the frequencies studied in this paper. From \( Y^* \) transformed to Z-parameters, the following equation can be written [43]:

\[
-\omega (\text{Im}(Z_{22}^*))^{-1} = C_x \omega^2 + (R_{ch}^2 C_x)^{-1} \quad (4.8)
\]

with \( C_x = \frac{c_{ds} + c_{gs} c_{gd}}{c_{gs} + c_{gd}} \) \quad (4.9)

Therefore, in accordance to (4.8), it is possible to extract \( R_{ch} \) and \( C_x \) from the slope and intercept with the ordinates of the linear regression shown in Fig. 4.7, where the extraction is performed for the different considered stress stages. As can be noticed,
substantial change in the extracted parameters is exhibited as the stress time is increased. This is associated with the fact that when longer time of hot carrier stress is considered, $C_x$ is smaller and whereas $R_{ch}$ increases, which is a clear degradation of the desired features. In addition, the plot corresponding to data obtained after one week of relaxation time after the stressing procedure is shown. This curve points out the fact that the intrinsic MOSFET’s characteristics do not recover from the effects of the HC-induced stress.

Further analysis can be performed by analyzing the impact of HC-induced stress on the series resistances $R_s$ and $R_d$. For this purpose, the corresponding parameter extraction

![Graph showing linear regression](image1)

**Fig. 4.7** Linear regression of experimental data to extract $R_{ch}$ and $C_x$ for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.

![Graph showing curves](image2)

**Fig. 4.8** Curves to obtain $R_d$ and $R_s$ for $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V at different stress stages.
Fig. 4.9 Small-signal equivalent circuit for the zero-bias strong inversion condition with the values obtained and simulated corresponding to $V_{gs} = 0.7 \, \text{V}$, $V_{ds} = 0 \, \text{V}$, and $V_{bs} = -1.2 \, \text{V}$.

has to be carried out by using the following equations:

\begin{align*}
R_s & = \text{Re}(Z_{12}^{1/2}) - \frac{1}{2} \frac{R_{ch}}{1 + (\omega R_{ch} C_x)^2} \\
R_d & = \text{Re}(Z_{22}^{1/2}) - R_s - \frac{R_{ch}}{1 + (\omega R_{ch} C_x)^2}
\end{align*}

(4.10) \hspace{1cm} (4.11)

When applying (4.10) and (4.11), it is observed that the series resistances $R_d$ and $R_s$ are considerably impacted as illustrated in Fig. 4.6. In fact, the change in percentage for the series resistances even surpasses the change in $R_{ch}$ when the same stress stages are considered. This is due to the fact that the damaged part of $R_{ch}$ is then considered as part of the parasitic series resistances, which is an interesting observation since it would allow the appropriate implementation of a degradation-dependent equivalent circuit model. Thus, by maintaining the value for the series resistances as that obtained for the fresh device and associating the increase in resistance to $R_{ch}$ allows a much better correlation of simulated with experimental data. This is physically justified since the impact of HC-induced degradation impacts more considerably the intrinsic MOSFET’s parameters and explains why the model allows a better reproduction of the data obtained experimentally. In this regard, if the new parameters are used to complement the cold equivalent circuit ($R_{ch}$, $R_d$ and $R_s$), the new equivalent circuit for strong inversion bias condition is in Fig. 4.9.
Simulated and experimental S-parameters at $V_{gs} = 0.7$ V, $V_{ds} = 0$ V, and $V_{bs} = -1.2$ V for a fresh device. The discrepancy between the curves for $S_{11}$ is due to the fact that the values for $R_g$, $C_{gs}$, and $C_{gd}$ were obtained at $V_{ds} = 0$ V. Better correlation is obtained after tuning $R_g$, $C_{gs}$ and $C_{gd}$.

At this point, comparing the model with experimental data, poor correlation is observed for $S_{11}$ as can be observed in Fig. 4.10. The discrepancy between these curves is attributed to the fact that the values for $R_g$, $C_{gs}$ and $C_{gd}$ were obtained at $V_{ds} = V_{gs} = 0$ V. At this bias condition, the relatively large device’s intrinsic impedance allows for a proper determination of the substrate parasitics. In contrast, extracting the elements in the input branch (i.e., the gate impedance) at $V_{ds} = V_{gs} = 0$ V introduces uncertainty and parameter overestimation occurs. For this reason, these parameters must be tuned to better correlate simulated with experimental data. In accordance to Fig. 4.10, the input impedance has to be reduced so that the curve corresponding to $S_{11}$ falls in constant resistance circle within the
Smith Chart. In other words, $R_g$ has to be smaller, whereas the capacitances between input and output ports must be bigger so that the $S_{11}$ curve is longer within the same frequency range. Once this is assumed, Fig. 4.11 shows a good correlation when considering $R_g = 1.5 \, \Omega$, $C_{gs} = 100 \, \text{fF}$, and $C_{gd} = 80 \, \text{fF}$.

Once it is verified that the small-signal model accurately reproduces experimental data corresponding to a fresh device, model correlations are performed at different degradation stages. In this regard, after 200 seconds of hot carrier stress, the channel resistance increases from 0.5 $\Omega$ to 6.5 $\Omega$. Again similarly as in the case of the cold bias condition, a reduction in $C_{gd}$ and $C_{gs}$ is observed, but this is not a definite degradation because by observing experimental data obtained after one week of relaxation, this capacitances present their original value. The correlation of the simulated and measured...
data after 200 s is shown in Fig. 4.12. Afterwards, the model–experiment correlation for the data obtained after 2,000 seconds of hot carrier stress is shown in Fig. 4.13. In this case, the channel resistance increases from 0.5 Ω to 15 Ω which is substantial and physically expected. Furthermore, the junction capacitances decreases once again. Finally, after 1 week of relaxation for the stressed device, $R_{ch}$ presents a value of 13 Ω, which represents a slight recovery, whereas the capacitances $C_{gd}$ and $C_{gs}$ exhibit to their original values of 80 fF and 100 fF, respectively. The curves corresponding to this experiment are shown in Fig. 4.14.

Summarizing, at this point the impact due hot carrier degradation is identified to be mainly on the channel resistance and the progress of the correspondig change with time is
shown in Fig. 4.15. This figure also shows that if this change in $R_{ch}$ through the time is compared with the shift of $V_{th}$, a direct and proportional relationship is observable as predicted by well known models relating these two parameters.

### 4.3 Saturation

Following the same systematic procedure as in the previously studied operation regions, the next step is to extract the device’s intrinsic parameters within the saturation condition. In this case, the transconductance takes importance and therefore the device behaviour is as an active component, which means that $S_{21}$ is no longer equal to the $S_{12}$. It is important to remember that as the parameter $S_{21}$ is an indicator of the ratio between power transmitted to the drain when a signal is injected at the gate, any change in this parameter would allow the identification of HC-induced degradation impacting the device’s transconductance.

The equivalent circuit for this bias condition is shown in Fig. 4.16. In this case, the extra parameters and the main differences comparing to the strong inversion bias condition are two. The first one is the need to consider the intrinsic capacitance of the inversion channel $C_{ds}$ and the second effect to be considered is that corresponding to the voltage controlled current source in the inversion channel that involves the transconductance $g_m$. 

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Fig. 4.16 Small-signal equivalent circuit for the saturation bias condition with the values obtained after applying the extraction method.
Fig. 4.17 Simulated and experimental S-parameters at $V_{gs} = 0.7$ V, $V_{ds} = 1.2$ V, and $V_{bs} = -1.2$ V at several stress stages.

The procedure for extracting the corresponding parameters is that reported in [44]. However, for this scenario, even with a substrate bias it is difficult to obtain a good correlation between the simulated and the experimental data. An explanation for these difficulties is the difference between the transistors analyzed as the device from the reference is an nMOSFET with channel length of 180 nm, finger width of 5um and 20 fingers. Thus, in order to simplify the parameter extraction while keeping it accurate for this case, the parameters extracted in the previous steps with a substrate voltage of $-1.2$ V, $V_{gs} = 0.7$ V and $V_{ds} = 1.2$ V were used. The corresponding experimental data before the stress, after 200 s, 2,000 s of stress, and after one week of relaxation are shown in Fig. 4.17. In this figure, the parameter $S_{21}$ is scaled by a factor of 1/8 to ease the comparison with the rest of the parameters.

Fig. 4.18 First attempt for correlating simulated and experimental data at $V_{gs} = 0.7$ V, $V_{bs} = 1.2$ V, and $V_{bs} = -1.2$ V for a fresh device.
The first attempt to correlate the model with the experimental data in saturation for a fresh device is shown in Fig. 4.18, where $R_{ch} = 36 \, \Omega$ and $g_m^* = 200 \, mS$ were assumed. As can be seen, the capacitances in the modelled $S_{11}$, $S_{22}$, and $S_{21}$ curves obtained from the simulation present magnitudes bigger than those corresponding to the experimental data. Thus, for a better model–experiment correlation, the junction capacitance $C_{gd}$ is reduced to 55 fF, achieving the results shown in Fig. 4.19.

Summarizing the differences between the parameters obtained in saturation and those in the previously considered bias conditions before applying any stress or damage, $R_{ch}$ is larger in saturation. Also there is a reduction in the junction capacitance from the gate to the drain terminal indicating that for high frequencies the device’s input impedance seen from the gate is bigger as the electric field from source to drain along the inversion channel increases. Also an explanation for this reduction is due to the pinch out near this terminal.
Fig. 4.21 Correlation of simulated and experimental data at $V_{gs} = 0.7$ V, $V_{ds} = 1.2$ V, and $V_{bs} = -1.2$ V for after 2,000 s of stress.

Fig. 4.22 Correlation of simulated and experimental data at $V_{gs} = 0.7$ V, $V_{ds} = 1.2$ V, and $V_{bs} = -1.2$ V after one week of relaxation.

Fig. 4.23 Time-dependent degradation of $R_{ch}$ and $g_m$.

Now, considering the experiments performed after stressing the device, after 200 s of hot carrier stress there is an increase in $R_{ch}$ to 41 Ohms and a reduction in $g_m$ to 172 mS, the model-experiment correlation for the corresponding S-parameters is shown in Fig. 4.20. Afterwards, at the stage of 2,000 s of stress, $R_{ch}$ reached a value of 50 $\Omega$, whereas $g_m$ presents a value of 137 mS. For this case, there is also a reduction in $C_{gs}$ and $C_{ds}$ to 100 fF.
and 50 fF, respectively. The S-parameter model-experiment correlation for this degradation stage is shown in Fig. 4.21.

Finally, after waiting one week to allow device relaxation, there is a recovery in \( R_{ch} \), \( g_{m} \), \( C_{gs} \), and \( C_{gd} \). \( R_{ch} \) reached a fixed value of 47 \( \Omega \), while the transconductance reached a fixed value of 150 mS. \( C_{gs} \) and \( C_{ds} \) present their original values before any stress, which are 130 fF and 55 fF respectively. The Smith Chart illustrating these values allow a proper reproduction of experimental data is shown in Fig. 4.22. Once again, the behavior of the change observed in \( R_{ch} \) presents the same trend as that exhibited in the strong inversion region and is correlated with the trend of \( V_{th} \) when plotted versus the stress time. As expected, this behaviour is similar but with opposite sign for \( g_{m} \), which is illustrated in Fig. 4.25. This indicates and corroborates the asymptotic behavior that shows a stabilization in the degradation.

4.4 Conclusion of the chapter

This chapter presents the experimental results of applying the equivalent circuit parameter extraction for the different bias conditions in order to build the different small-signal models required to assess the corresponding impact of HC-induced degradation. In fact, as it was pointed out in this chapter, a unique small-signal model simplified for different operation conditions and at different degradation stages. Using this concept, the more complex circuit required in the saturation region can be built from the simplest model at the zero-bias condition by adding the components required to represent the device in the strong inversion condition, and thus finally including the effect of the transconductance and the channel capacitance. Bearing this in mind, analyses at different degradation stages can be carried out in a direct and systematic way.

It was verified the usefulness of considering shorter time steps at the beginning of the stress procedure to observe the trend of the change in the small-signal parameters as a function of time. Another good practice was to wait for a long time (one week) after the stress procedure was performed and measure the device again. This practice shows for the first time that some of the impacted parameters from the small-signal model such as the joint capacitances suffer of a temporary degradation and corroborates that the only significantly impacted parameters are the \( R_{ch} \) and the \( g_{m}^{*} \).

The dependence of some junction capacitances on \( V_{gs} \) and \( V_{ds} \), as well as the small values found on some terminal resistances made the original extraction procedure to be not very adequate. It was necessary to tune directly the values of a few capacitances to reach a good correlation between the simulated and measured data.
The extraction procedure presented in this thesis for obtaining the small-signal parameters as a function of the time in a MOSFET stressed by hot carriers was very usefully and accurate for modeling fresh and degraded devices up to 20 GHz. However, due to the small size in the channel length of the considered transistor, the extraction of the rest of the extrinsic parameters required of discretional tuning, as well as the extraction of the intrinsic parameters in saturation.

The procedure for applying the degradation that was learned and used in this work is based in the measure of the bulk current generated by the impact ionization of the hot-carriers which is similar to the method used in previous works, however, as it was corroborated, this previous methods were not suitable for the new dimensions and technology of the RF MOSFETs, on the other hand the bulk current ratio and the time steps selected in this thesis are suitable for the current state of art MOSFETs. This advantage will be useful for future work related with the analysis of this type of degradation.

A good correlation of simulations with experimental data was achieved when the extracted parameters for the strong inversion and for saturation bias conditions was obtained with the understanding of the effect of the hot carriers degradation stress in the device. It is necessary, however, for further work to improve this method for extraction of the small signal model parameters for strong inversion and saturation bias conditions for nanometric channel lengths.

An important contribution of this project is the understanding of the hot carrier degradation observed through S-parameters measurements for the three bias operation conditions: zero-bias, strong inversion, and saturation. From these observations it was clear that from the zero-bias condition there is no change in the S-parameters after the several steps of degradation, and therefore this means that there is no degradation in the substrate elements of the model.

From the observations in the strong inversion condition it is corroborated that the impact of the hot carrier degradation is only in the channel resistance. There is a pseudo impact in the junction capacitances due to the stress; however, as it is observed in the measurements after one week of relaxation that this capacitance recovers its original value. Also, the direct relationship between the $S_{22}$ parameter and the channel resistance is used to perform a direct reading of the degradation through plotting this parameter in a Smith
Chart. In fact, after achieving an excellent correlation between the modeled and the experimental data, now it is possible to attribute the shift in the low-frequency $S_{22}$ parameter to degradation in the channel resistance when the bias voltages remain constant. As expected, after comparing the change in the channel resistance with change in the threshold voltage it is corroborated that these two parameters drift with time at the same rate.

The advantage of the small-signal model used in this work, is that allows concentrating the impact of the hot carrier degradation in only two small-signal model parameters with a good representation of experimental data up to 20 GHz. In addition to this, it was possible to identify the relationship between each of this small-signal model parameter with a corresponding $S$-parameter. And for now on it is possible to easily estimate the degradation by observing the $S$-parameters. For IC designers this work will be a useful and easy method to understand the behavior of the degradation in the small signal model parameters, and also with this thesis the designers will be able to easily predict and understand the $S$-parameters for frequencies up to 20GHz of this type of MOSFET.

About the future work, the current investigations around the world related with the degradation due to hot-carriers are characterizing in large signal, this is useful and necessary for one of the most significant topics related with the RF MOSFETs which is the amplifiers field. In order to perform this measurements is needed more specialized equipment, and different calibration and de-embedding methods never made before in this Lab. Therefore this research in large signal will come with several new challenges for the continuing growing of the knowledge in the characterization of MOSFETs in frequencies of GHz. But hopefully, this work will be a base for the future analysis in degradation by hot-carriers.
References:


