Design-for-Test Techniques for Opens in Undetected Branches in CMOS Latches and Flip-Flops

Antonio Zenteno Ramirez, Guillermo Espinosa, and Victor Champac

***Abstract*—In this paper, a design-for-testability (DFT) technique to test open defects in otherwise undetectable faulty branches in fully static CMOS latches and flip-flops is proposed. The main benefits of our proposal are: 1) it is able to detect a parametric range of resistive opens defects and 2) the performance degradation is very low. The testability of the added DFT circuitry is also addressed. The cost of the proposed technique in terms of speed degradation, area overhead, and extra pins is analyzed. Comparison with other previously proposed testable latches is carried out. Circuits with the proposed technique have been designed and fabricated. Good agreement is observed between the analytical analysis, simulations and experimental measures performed on the fabricated circuits.**

***Index Terms*—Design-for-testability (DFT), flip-flops, latches, resistive opens, undetected opens.**

I. Introduction

UNDETECTABLE opens in some branches of CMOS latches and flip-flops have been studied [1], [2]. Opens in vias-contacts [3], [4] are likely to occur. The number of vias-contacts is high in actual integrated circuits due to the many metal levels [3], [4]. In the damascene-copper process, vias and metal are patterned and etched prior to the additive metalization. Because of this micromasking during the next lithography step can occur [5]. The open density in copper shows a higher value than those found in aluminum [5]. Random particle induced-contact defects is the main test target in production testing [4]. In addition, silicided opens can occur due to excess anneal during manufacturing [6].

Memory elements like latches and flip-flops are widely used in the design of digital CMOS integrated circuits. Their application depends on the requirements of performance, gate count, power dissipation, area, etc. [7]. Resistive opens affecting certain branches of fully static CMOS memory elements are undetected by logic and delay testing [1], [2]. For these opens the input data is correctly written and memorized. However, for high resistive opens the latch may fail to retain the information after some time in the presence of leakage or noise [8], [9]. Testable latches have been proposed for making detectable stuck-open faults in these otherwise undetectable branches. Reddy *et al.* [1] have proposed a testable latch where an additional controllable input is added to the last stage of the latch. Then a proper sequence of vectors is generated for testing

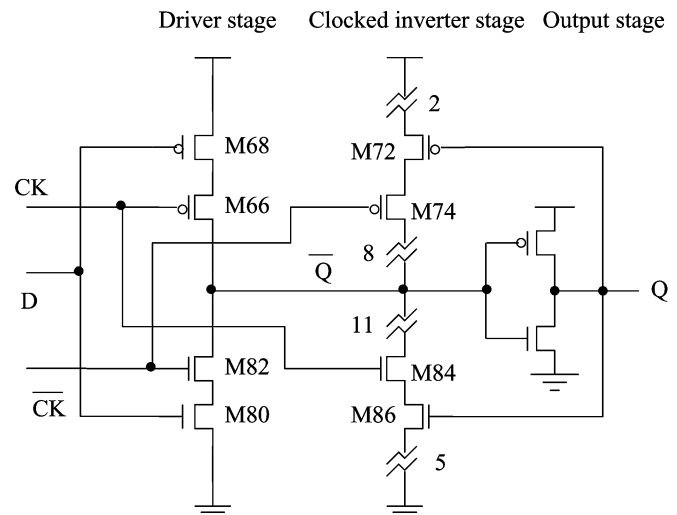

Fig. 1. Symmetrical CMOS latch with undetected.

these opens. Also, the delay is penalized due to the added series transistors. Rubio *et al.* [2] have proposed a testable latch. The number of test vectors is lower than in proposal [1]. One additional input is required The delay is also penalized due to the added series transistors.

In this paper, a design-for-testability (DFT) technique for testing full and resistive opens in undetectable branches of fully static CMOS memory elements is proposed. To the best of our knowledge, this is the first testable latch able to cover both full opens and parametric resistive opens in otherwise undetectable faulty branches. Design considerations for the DFT circuitry are stated. The results are compared with previous reported testable structures. Measurements made in specially designed and fabricated circuits show the feasibility of the proposed technique. The rest of this paper is organized as follows. In Section II, opens in undetectable branches of CMOS memory elements are analyzed. In Section III, a new testable latch is proposed. In Section IV, the application to a large number of cells is analyzed. In Section V, the cost of the proposed technique is evaluated. In Section VI, experimental results on specially designed and fabricated circuits are presented. Finally, in Section VII, the conclusions of this paper are given.

II. Undetected Open Branches in the CMOS Latch Cell

It is well known that opens in the clocked inverter stage (CIS) of the symmetric D-latch (see Fig. 1) are undetectable [1], [2], [10]. This is because the input data is correctly written through the driver stage despite the defective stage. Then, the data is correctly memorized in a dynamic way. As a consequence these

Manuscript received August 19, 2005; revised September 13, 2006. This work was supported by CONACYT/Mexico.

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Digital Object Identifier 10.1109/TVLSI.2007.896910

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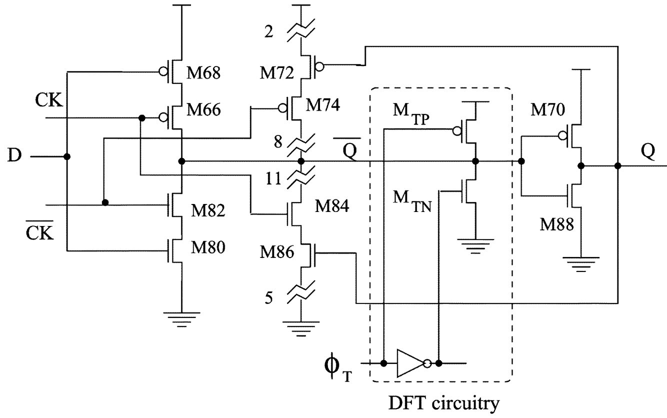

Fig. 2. Proposed testable latch with one control signal.

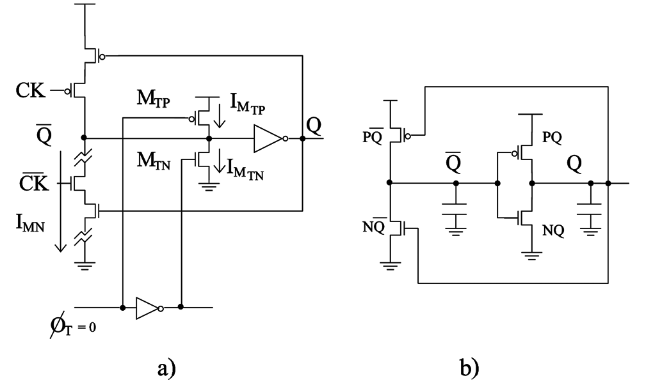

Fig. 3. (a) Memorizing stage with DFT circuitry for testing resistive opens in the nMOS network. (b) Simplified defect-free latch memorizing circuitry.

opens cannot be detected by either logic or delay testing. However, in the presence of leakage or noise, the latch may fail to retain the information after some time for high resistive opens [8], [9]. A data retention test can be used to test these opens. However, this approach is expensive in terms of test time. Because of these testable latches covering full opens have been proposed [1], [2].

In this paper, a symmetric CMOS D-latch cell has been considered (see Fig. 1). However, the proposed approach can be extended to other similar structures [7], [11]. Possible open locations affecting conductive paths of the CIS are given in Fig. 1. Our approach not only considers stuck-open faults [1]–[3] but also resistive opens in the CIS branches. Opens are modeled with a lumped resistance which can take a continuous range of values. We use HP 0.35-μm, N-well CMOS technology.

III. Proposed DFT Testable Latch Cell

A testable latch allowing to test otherwise undetectable open defects in the CIS of the latch structure is presented. The testability of the added DFT circuitry is also addressed.

A. DFT Proposal

The proposed testable CMOS latch cell is shown in Fig. 2. Four additional transistors and only one control signal are required. The network under test (nMOS or pMOS) is selected by proper initialization of the latch state. Resistive opens in the nMOS (pMOS) network are tested as follows:

- initialize the latch to 1 (0) state;
- in the memory phase, activate transistors M_{TP} and M_{TN};
- deactivate both transistors M_{TP} and M_{TN};
- observe the output of the CMOS latch.

The detectability of the open defects is determined by the voltages imposed by the DFT circuitry during the memory phase and the latch input/output characteristics [12]. The voltage values imposed during the memorizing phase are determined by the transistor sizes of the DFT circuitry and the latch memorizing circuitry. The memorizing stage with the added DFT circuitry is shown in Fig. 3(a). Let us consider a resistive open in the nMOS network. The latch output was initialized to one state. When the two DFT transistors M_{TP} and M_{TN} are activated there is a competition of three networks [See Fig. 3(a)]: the nMOS branch under test, M_{TP} transistor, and M_{TN} transistor. Due to the resistive open, the strength of the nMOS branch of the CIS decreases. Hence, different voltage values at Q and $\overline{Q}$ appear for the defect-free and the defective cases. The voltage at $\overline{Q}$ (Q) for the defective latch is higher (lower) than for the defect-free latch. When the transistors M_{TP} and M_{TN} are deactivated, the cell evolves to a stable quiescent state. The transistors M_{TP} and M_{TN} are sized such that the state of the defective latch flips its state but the state of the defect-free latch remains unchanged. This behavior is further explained next.

The circuit analysis of the simplified memorizing circuitry of the defect-free latch [See Fig. 3(b)] gives [12], [13]

$$C_{\overline{Q}}\frac{dv_{\overline{Q}}}{dt} = B_{P\overline{Q}}(V_{DD} - V_Q) - B_{N\overline{Q}}V_Q \quad (1)$$

$$C_Q\frac{dv_Q}{dt} = B_{PQ}(V_{DD} - V_{\overline{Q}}) - B_{NQ}V_{\overline{Q}} \quad (2)$$

where $B_{P\overline{Q}}$ ($B_{N\overline{Q}}$) is the transconductance of the equivalent $P\overline{Q}$ ($N\overline{Q}$) transistor. Similar definitions apply for NQ and PQ transistors.

The used transistor current model considers that the drain current depends linearly on the applied gate voltage [13]. The solution of the previous equations gives [13]

$$V_{\overline{Q}}(t) = A + X_1e^{\sqrt{r}t} + Y_1e^{-\sqrt{r}t} \quad (3)$$

$$V_Q(t) = B - \mu X_1e^{\sqrt{r}t} + \mu Y_1e^{-\sqrt{r}t} \quad (4)$$

where X_1 and Y_1 are given by technological parameters and initial voltage conditions. r and μ are given by technological parameters. A and B are given by both technological parameters and power supply voltage.

The input/output characteristic of the defect-free latch (see dotted curves in Fig. 4) has been obtained by plotting the previous equations and using different imposed voltages at the nodes Q and $\overline{Q}$. Each point of the input/output characteristic is obtained by plotting the resulting V_Q and $V_{\overline{Q}}$ voltage pairs from the equations $V_Q(t)$ and $V_{\overline{Q}}(t)$ for the same time t. The direction of the trajectory of the curves is indicated with arrows (see Fig. 4). A symmetrical memorizing circuitry has been considered. A straight line **S1** (see Fig. 4) is approximately drawn on the input/output characteristic of the defect-free latch. This line defines two semi-planes which determine the final

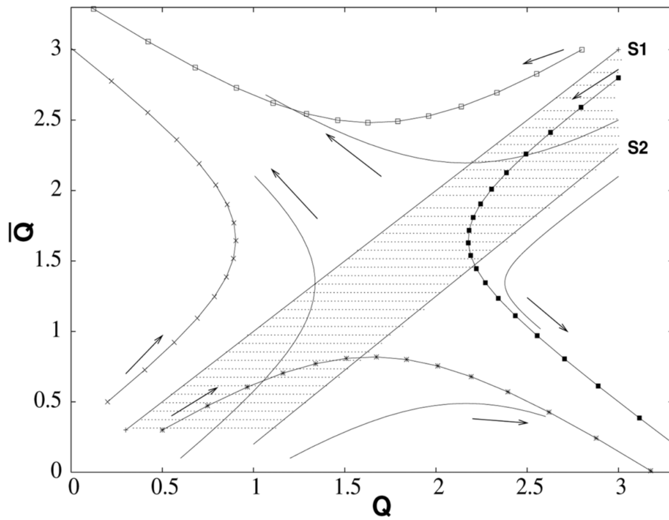

Fig. 4. Defect-free (dotted curves) and faulty (nondotted curves) latch input/output characteristics.

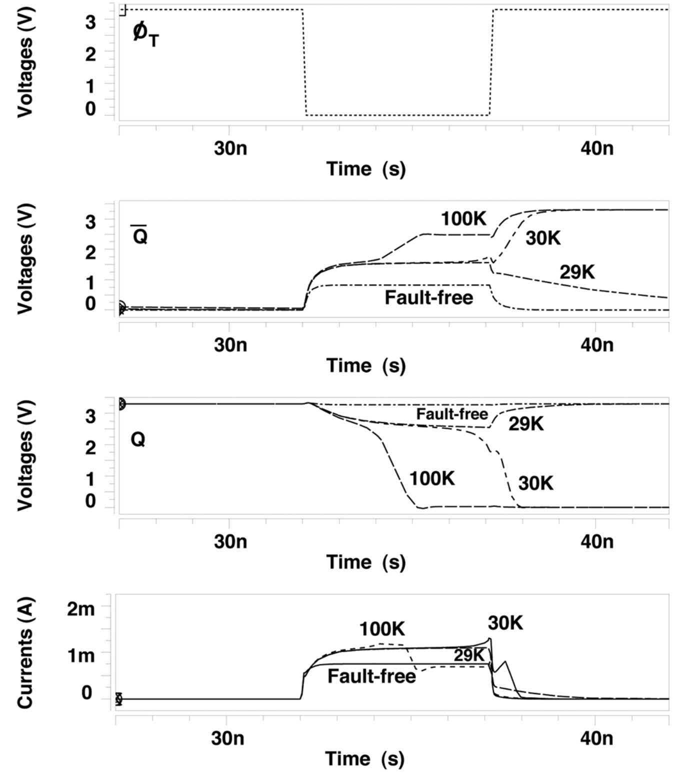

Fig. 5. Timing diagram for latch with one control signal. Resistive open R_{11}, $W_{MTP} = 3\ \mu$m, $W_{MTN} = 1.3\ \mu$m, $T_{WT} = 5$ ns.

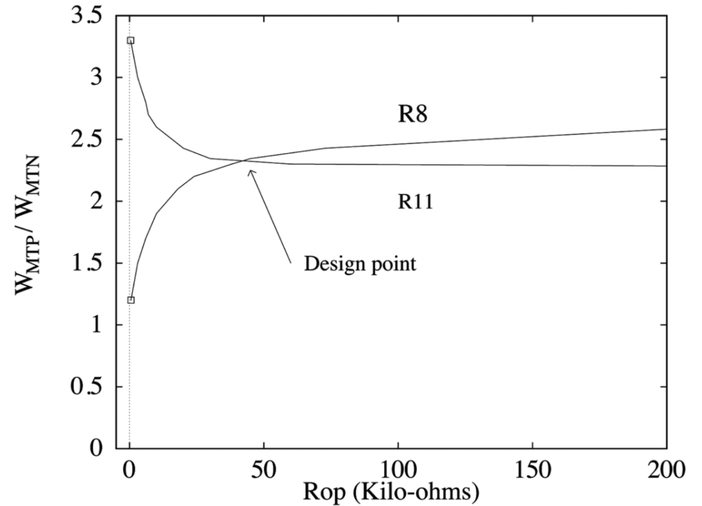

Fig. 6. Channel width sizing of the DFT transistors M_{TP}, M_{TN}. Width activation signal $T_{WT} = 5.0$ ns. R_8: open in the pMOS branch, R_{11}: open in the nMOS branch.

state of the latch. The defect-free latch evolves to a final high (low) logic state for all those imposed voltages located to the right (left) of the straight line S1.

The effect of a resistive open in the nMOS network is similar to decrease its strength. In a first-order approach, this can be modeled in the previous equations by reducing the transconductance $B_{N\overline{Q}}$. The input/output characteristic for the latch with a typical case of a resistive open is also drawn in Fig. 4 (see non-dotted curves). In a similar way to the defect-free latch a straight line **S2** is also approximately drawn on the input/output characteristic the defective latch. Two semi-planes also appear for the defective case. Because of the defect, the location of the straight line **S2** has different location than for the defect-free case **S1**.

As previously stated, let us remind that for testing opens in the nMOS network the latch nodes Q and $\overline{Q}$ are initialized to 1,0. It can be observed that for imposed voltages at Q and $\overline{Q}$ located in the shadow area (see Fig. 4), the defective (defect-free) latch changes (remains at) the initialized state of the latch. Hence, the defect is detected. In other words, the DFT circuitry must be designed to impose voltage values located in the shadow area.

Simulation results are shown in Fig. 5. Different resistance values for open R_{11} (see Fig. 2) have been considered. The latch is initialized to logic 1 (see Fig. 5). During the activation phase ($\phi_T = 0$), the voltage at the node Q ($\overline{Q}$) decreases (increases). Then, ϕ_T goes to 1 to deactivate the DFT transistors M_{TP} and M_{TN}. Resistive opens equal or higher (lower) than 30-kΩ flip (do not flip) the state of the CMOS latch. Hence, these opens are (are not) detected. The minimum detected resistance value of the opens in the nMOS and pMOS networks depends on the width of the activation signal ($T_{WT} = 5$ ns) and the channel ratio W_{MTP}/W_{MTN} of the two test transistors (3/1.3 μm).

The required conditions to test resistive opens in both branches of the CIS stage are given in Fig. 6. W_{MTP}/W_{MTN} is the required channel ratio of the two DFT transistors to detect a given resistive open. A proper W_{MTP}/W_{MTN} ratio must be chosen to be able to detect resistive opens in both branches of the clocked inverter stage (see Fig. 1). The minimum detected resistive open in the pMOS (nMOS) branch increases (decreases) as the ratio W_{MTP}/W_{MTN} increases. The optimum W_{MTP}/W_{MTN} is the intersection of the curves (see Fig. 6). At this point, the minimum detected resistive open is optimized for both branches (nMOS and pMOS). For a smaller width of the activation signal the sizes of the DFT transistors should be made larger. In addition, it must be assured that the defect-free latch does not change its state under process variations. The selected initial imposed voltage should be also sufficiently far from the metastability line S1 (see Fig. 4).

B. Testability of the DFT Circuitry

In this subsection, the testability of the added DFT circuitry is analyzed. The DFT circuitry is composed of the transistors M_{TP}, M_{TN} and the inverter (see Fig. 2). Let us focus in the transistors M_{TP} and M_{TN}. Defects affecting the DFT inverter can be analyzed in a similar way. Stuck-open faults, resistive open defects and stuck-on faults are considered. Stuck-open faults and resistive opens located in conducting paths of the two DFT transistors can be tested using the same procedure than for opens affecting undetectable branches of the latch. For a stuck-open fault at the nMOS DFT transistor (see Fig. 2) the latch is initialized to one logic. When in memory phase the two DFT transistors are activated, the voltage at $\overline{Q}$ (Q) increases (decreases). The voltage at $\overline{Q}$ (Q) tends to a higher (lower) value than for the defect-free case because the nMOS transistor if off. After the two DFT transistors are deactivated the defect-free (defective) maintains (changes) the initialized state. Hence, the defect is detected. Resistive opens are tested in a similar way. Low values of resistive opens can be detected. For the used latch topology resistive opens as low as 5 kΩ are detectable.

Stuck-on faults are tested writing and memorizing the data with the DFT circuitry always deactivated. Let us consider a stuck-on fault at the pMOS DFT transistor (see Fig. 2). Because of the pMOS DFT transistor is "on," the voltage at $\overline{Q}$ does not completely discharge to zero volts when $D = 1$ is written. Then, during the memorizing phase the latch evolves to the opposite state. Hence, the defect is detected.

IV. Application to a Large Number of Cells

Let us assume a scan design. Using the proposed technique, a current pulse appears at the power buses during the activation the DFT circuitry (see bottom panel in Fig. 5). When the DFT circuitries of the flip-flops in the scan chain are simultaneously activated the current drawn from the power supply could be important. Due to the high current density, mass transport due to the momentum transfer between conducting electrons and diffusion metal atoms [14] can occur. This phenomena is known as electromigration [14]. As a consequence the metal lines can be degraded and even an open failure can occur [15]. Conditions for an open failure to occur in metal lines under short pulse stressing has been studied by Banerjee *et al.* [15].

The activation of the DFT circuitries for blocks of scan cells can be skewed to minimize stressing on the power buses during test mode. This is implemented inserting delay circuitries in the path of the control signal of blocks of scan cells (see Fig. 7). In this way, the activation of the DFT circuitries of each block of scan cells is time skewed. Hence, at a given time there is a stressing current pulse due to only one block of flip-flops.

For comparison purposes, the current drawn from the power supply for 750 symmetrical flip-flops cells simultaneously activated and time skewed is shown in Fig. 8. The acceptable stressing current pulse for a line can be determined from the work of Banerjee *et al.* [15]. In this example, the scan chain has been divided in three blocks of 250 cells each one. A delay circuitry composed of 12 inverters has been implemented.

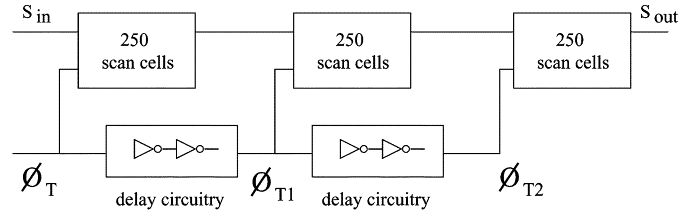

Fig. 7. Skewing activation of scan cell by blocks.

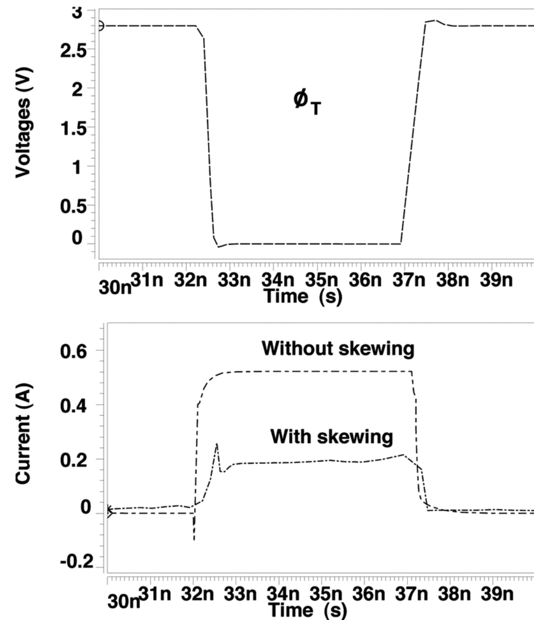

Fig. 8. Current consumption in a 750 scan cell with and without delay circuitry (two blocks). First panel: activation signal. Second panel: current consumption.

V. Cost Evaluation and Comparison With Other Testable Latches

In this section, first the cost of the proposed technique is discussed. Then, a comparison with other testable latches is carried-out.

A. Cost Evaluation

The cost of the proposed technique has been evaluated in terms of speed degradation, area overhead, and extra pins. A summary of the cost is given in Table I. ΔT_d is the speed penalty (writing time) of the latch including the DFT transistors with respect to the case nonincluding the DFT circuitry. In a similar way, ΔA is the area penalty per cell. $R_{\rm Min}^{\rm Det}$ is the value of the minimum detected resistance. As it can be seen in Table I, the delay penalty due to the added DFT transistors is very low. The area overhead per cell due to the added DFT transistors is small (less than 5%). Considering 750 symmetrical flip-flops cells in the scan chain the delay circuitry adds an area overhead of 0.5%. In addition, the control signal needs to be routed through the memory cells. The routing layer of the control signal running inside the cell represents a small percentage (less than 2%) of the cell area. Nevertheless, this signal needs to be handled properly by the routing tools in order to minimize area penalization.

TABLE I
COST OF THE LATCH WITH ONE CONTROL SIGNAL $T_{WT} = 5$ ns

$\frac{W_p}{W_n}$	R_{Min}^{Det}N	R_{Min}^{Det}P	$\Delta T_d(\%)$	$\Delta A(\%)$
2.2	1MΩ	24KΩ	1.0	4.7
2.3	30KΩ	45KΩ	2.3	4.7
2.7	7KΩ	650KΩ	3.1	4.8

TABLE II
COMPARISON WITH OTHER TESTABLE LATCHES

Technique	Add Inputs	Add Trans.	ΔT_d (%)	Vectors Number	R_{DET}
[1]	1	4	21.5	12	R_∞
[2]	2	4	34	8	R_∞
Our proposal	1	4	2.3	8	>40K-∞

B. Comparison With Other Testable Latches

Table II shows a comparison between our proposal and other testable latch structures [1], [2]. Our proposal requires one additional input. The number of additional inputs for proposals previously reported are also given. In our proposal, the number of additional transistors per cell is smaller than for the other techniques. The delay penalization using our proposal is significantly smaller than using the others techniques [1], [2]. For the delay estimation of the techniques of [1] and [2] DFT transistors of similar channel widths to the original ones are added in the pMOS and nMOS branches. Our technique requires eight vectors for testing both CIS branches of the latch. For testing one branch, the first vector writes the desired state into the latch. The second vector memorizes this state. Then, the third vector activates the DFT circuitry and the fourth vector deactivates the DFT circuitry. A similar sequence is required for complementary branch. The main benefit of our proposal is that it can detect a parametric range of the resistance of the open. The proposals from other authors only detect a line completely open (or infinite resistive open).

VI. EXPERIMENTAL RESULTS

Defect-free and defective CMOS latches have been designed and fabricated in AMS 0.35-μm CMOS technology. Transmission gates (TG) are used in the designed circuits for introducing opens during the experimental measurements. The resistance of the opens is modified by controlling the voltages at the gates of each transistor of the TG. The resistance values of the opens introduced in the experimental measurements have been estimated by electrical simulation.

The schematic of the designed and fabricated testable CMOS latch is shown in Fig. 2. The nMOS (M_{TN}) and the pMOS (M_{TP}) transistors are symmetrically sized. The designed transistor sizes are $W_{MTP} = 2.7$ μm and $W_{MTN} = 1.0$ μm. These sizes were also selected for assuring that the defect-free latch does not change the initialized state in the presence of process variations. Monte Carlo analysis has been carried out. The following tolerance parameters have been considered: 18% for the threshold voltage, 7.5% for the gate oxide thickness, and 5% for the mobility. A parameter tolerance of 5% has been considered for the channel widths and lengths. Resistive open R_5 has been considered (sSee Fig. 2). The voltages at the gates of the TG are $V_P = 2$ V and $V_N = 1.1$ V. HSPICE simulation gives

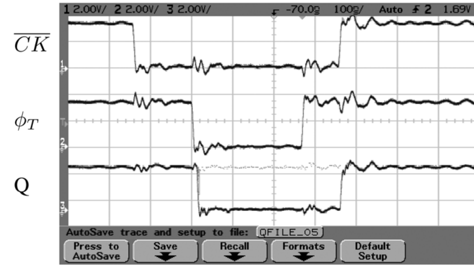

Fig. 9. Output of the DFT circuitry for the case of $R_{\text{open}} = 35.8$ kΩ, $T_{wt} = 260$ ns. Upper waveform: clock signal $\overline{CK}$. Middle waveform: activation signal ϕ_T. Lower waveform: output signal Q.

TABLE III
PULSE WIDTH ACTIVATION T_{wt} USED TO DETECT RESISTIVE OPENS IN THE CIS FOR THE ONE CONTROL SIGNAL DFT PROPOSAL

T_{wt} (ns)	R_{op} (KΩ)
40	54.3
80	46.9
260	35.8
440	28.7

$R_{\text{open}} = 35.8$ kΩ. A width of $T_{wt} = 260$ ns is used (see middle waveform of Fig. 9). The output node Q changes to low when $\phi_T = 0$ (see lower waveform of Fig. 9). When the DFT circuitry is deactivated node Q remains at low level. Hence, the open is detected.

The minimum required test activation time (T_{wt}) of ϕ_T for different resistive opens is given in Table III. Wider activation times are required in order to detect smaller resistive opens.

VII. CONCLUSION

A DFT technique to test resistive opens in otherwise undetectable branches in fully static CMOS latches and flip-flops has been proposed. The main benefit of our proposal is that it is able to detect a parametric range of resistive opens with a reduced performance degradation. The proposed test strategy requires one extra control signal. The required design conditions of the DFT circuitry have been determined. Also, the detectability of faults in the DFT circuitry has been examined. There is a tradeoff between the test activation time and the sizes of the DFT transistors. Skewing the activation signal of large blocks of scan cells allows the application of the proposed technique to a large number of cells. Symmetric CMOS latches implementing the proposed technique have been designed and fabricated. The experimental results show good agreement with the analytical analysis and simulation results.

ACKNOWLEDGMENT

The authors would like to thank C. J. Corona for her valuable support with the computer software and the Department of Microelectronics, LIRMM, France, for the facilities given.

REFERENCES

[1] M. K. Reddy and S. M. Reddy, "Detecting FET stuck-open faults in CMOS latches and flip-flops," *IEEE Design Test*, vol. 3, no. 5, pp. 17–26, Oct. 1986.

[2] A. Rubio, S. Kajihara, and K. Kinoshita, "Class of undetectable stuck-open branches in CMOS memory elements," *Proc. Inst. Elect. Eng.-G*, vol. 139, no. 4, pp. 503–506, 1992.

[3] K. M. Thompson, "Intel and the myths of test," *IEEE Design Test Comput.*, vol. 13, no. 1, pp. 79–81, 1996.
[4] K. Baker, G. Gronthoud, M. Lousberg, I. Schanstra, and C. Hawkins, "Defect-based delay testing of resistive vias-contacts a critical evaluation," in *Proc. Int. Test Conf.*, 1999, pp. 467–476.
[5] A. Stamper, T. L. McDevitt, and S. L. Luce, "Sub-0.25-micron interconnect scaling: Damascene copper versus substractive aluminum," in *Proc. IEEE Adv. Semiconduct. Manuf. Conf.*, 1998, pp. 337–346.
[6] C. -W. Tseng, E. J. McCluskey, X. Shao, and D. M. Wu, "Cold delay defect screening," in *Proc. 18th IEEE VLSI Test Symp.*, 2000, pp. 183–188.
[7] V. Stojanovic and V. G. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.
[8] A. J. Van de Goor, *Testing Semiconductor Memories Theory and Practice*. New York: Wiley, 1991.
[9] J. Xu, R. Kundu, and F. J. Ferguson, "A systematic DFT procedure for library cells," in *Proc. 17th IEEE VLSI Test Symp.*, 1999, pp. 460–466.
[10] W. K. Al-Assadi, Y. K. Malaiya, and A. P. Jayasumana, "Faulty behavior of storage elements and its effects on sequential circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 1, no. 4, pp. 446–452, Dec. 1993.
[11] S. M. Samsom, K. Baker, and A. P. Thijssen, "A comparative analysis of the coverage of voltage and $I_{\rm DDQ}$ tests of realistic faults in a CMOS flip-flop," in *Proc. ESSCIRC 20th Eur. Solid-State Circuits Conf.*, 1994, pp. 228–231.
[12] W. A. M. Van Noije, W. T. Liu, and J. S. Navarro, Jr, "Metastability behavior of mismatched CMOS flip-flops using state diagram analysis," in *Proc. IEEE Custom Integr. Circuits Conf.*, 1993, pp. 27.7.1–27.7.4.
[13] M. Shoji, *Theory of CMOS Digital Circuits and Circuit Failures*. Princeton, NJ: Princeton Univ. Press, 1992.
[14] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. ED-16, no. 4, pp. 338–347, Apr. 1969.
[15] K. Banerjee, A. Amerasekera, N. Cheung, and C. Hu, "High-current failure model for VLSI interconnects under short-pulse stress conditions," *IEEE Electron Devices Lett.*, vol. 18, no. 9, pp. 405–407, Sep. 1997.

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