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New strategies to improve offset and the speed–accuracy–power tradeoff in CMOS amplifiers

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Abstract Four continuous-time strategies to improve the speed–accuracy–power tradeoff in CMOS amplifiers by using low-power offset-compensation circuits are presented. The offset contribution at the output voltage is extracted and used to modify the DC component of the input voltage or the value of the active load, through low frequency feedback loops, which are realized using two transistors operating in weak inversion and a small capacitor. Because these circuits do not affect the bandwidth and allow using small transistors, the power consumption is greatly reduced with respect to an uncompensated amplifier of the same speed and offset behavior. The proposed strategies present reduced costs in area, power consumption and complexity, and a decrease in the low frequency noise contributions. MonteCarlo, HSPICE simulations results of common source, class AB and fully differential amplifiers, and experimental results of a class AB amplifier, all implemented in a 0.5-μm CMOS technology are shown. Statistical analyses of these strategies are also presented. Improvements up to 99.74% and 398.6% in the offset and the power consumption are respectively observed.

Keywords CMOS amplifiers · Floating gate transistors · Mismatch · Offset compensation

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1 Introduction

Continuous time amplifiers are some of the most important building blocks in analog signal processing and communications. However, the requirements of downscaling CMOS processes have forced analog and mixed signal circuits to operate within continuously decreasing supply voltages and almost the same threshold voltages, reducing their dynamic ranges [1]. Several techniques have been proposed to reduce supply requirements, such as MOS transistors operating in weak inversion, floating gate transistors and current-mode processing [1]. Nevertheless, circuits achieved with those techniques are prone to present offset components as a consequence of the presence of mismatch, lithographic defects, temperature effects and mechanical stress. Since undesired offsets degrade even more the dynamic range, the amplifiers are more sensible to noise and nonlinear effects. Mismatch can be reduced by increasing the transistor's dimensions, but the speed–accuracy–power tradeoff is seriously affected. For a large group of current and voltage processing circuits (current mirrors, amplifiers and more complex multi-stage circuits), this tradeoff only depends of technological and mismatch parameters and can be written as [2]:

$$\frac{\text{Speed} \cdot \text{Accuracy}^2}{\text{Power}} \propto \frac{1}{C_{\text{ox}} A_{VT}^2} \tag{1}$$

where A_{VT} is a constant associated with the standard deviation of the threshold voltage in the Pelgrom's mismatch model [3] and C_{ox} is the oxide capacitance per unit of area. Despite expression (1) improves with deep submicron technologies, that improvement is limited by the voltage supply narrowing [2]. From (1) is observed that high speed and high accuracy can only be achieved by

increasing the power consumption. For that reason, the only way to overcome this problem is by using near to ideal offset compensation (or autozeroing) arrangements. An ideal offset compensation strategy should present the following characteristics:

(i) A simple principle of operation and easy design.
(ii) Negligible costs in hardware, area requirements and power consumption.
(iii) Do not degrade bandwidth.
(iv) Continuous time operation (i.e., normal system operation should not be interrupted by calibration phases).

Additionally, the capacity to reduce 1/*f* noise and a complete on chip realization can be also considered desirable features for any offset compensation strategy.

Some of the most frequently used offset compensation techniques are layout techniques [4], trimming circuits [5–8], autozeroing, chopping, and ping-pong amplifiers [9–13] and use of digital-to-analog converters to adjust amplifier load currents [14]. However, those techniques do not fulfill all these requirements and/or affect the speed–accuracy–power tradeoff, among other additional disadvantages, as shown in Table 1.

To obtain offset compensation strategies which fulfills previously mentioned features, and enhance the speed–accuracy–power tradeoff, this paper presents four offset compensation schemes based on continuous time, low power and low hardware complexity circuits. These strategies are sustained on a low frequency compensation principle, proposed in this paper, denominated ''semi-active feedback'' (SF). This principle is a practical, compact and easy modification of the offset measurement principle based on servo loop converters [15]. The offset of the output voltage is extracted and is used to modify the DC component of the input voltage or the value of the active load, through low frequency feedback loops. This way, the characteristic bandwidth is not affected, whereas the percentage of offset compensation is proportional to the gain of the amplifier. The simplicity of the compensation circuits, which only need two transistors operating in weak inversion and a small capacitor, allows its operation with almost negligible power requirements.

The paper is organized as follows. Section 2 describes the four offset compensation strategies and provides a study of their design restrictions and noise behavior. These strategies will be proved in common source, class AB and fully differential amplifiers. Techniques for statistical analysis, used to compare the proposed strategies, are described in Sect. 3. HSPICE, MonteCarlo simulations and experimental results are presented in Sects. 4 and 5, respectively. Finally, in Sect. 6 some conclusions are drawn.

Table 1 Some disadvantages of the offset compensation techniques

Technique	Disadvantages
Layout	Barely modeled in the literature to reduce mismatch effects.
	It is not properly an offset compensation technique.
Trimming	Complex and expensive in hardware and design.
	Unconventional CMOS processes, large voltages or currents and post-fabrication treatment are required.
	1/f noise and dynamic offset are not compensated.
	Resistor trimming is expensive.
Auto-zeroing and correlated double sampling	Complex and expensive in hardware and design.
	High power consumption.
	Charge injection and switched noise effects.
	Only applicable in sampled data systems.
	The operation of the circuits is interrupted.
	Low speed.
Chopper	Complex and expensive in hardware and design.
	The passive filters are hard to integrate.
	Limited to low-bandwidth applications.
Adjusting of load currents with digital to analog converters	Extremely expensive in hardware and area requirements.
	1/f noise and dynamic offset are not compensated.
	Post-fabrication treatment is required
Servo loop converters	Hard to integrate in a chip.
	More than an offset compensation technique, is an offset measurement technique.
	It operates only in DC or very low frequencies, for what is not adequate for offset compensation in broadband applications.
	The accuracy of this approach depends on accurately knowing the values of internal matching resistors.

2 Offset compensation techniques

In Fig. 1(a), $H(s)$ is an offset-uncompensated, first-order inverter amplifier with DC gain A_0 and bandwidth a, whereas $R(s)$ is an offset compensation feedback loop with bandwidth am. In a straightforward analysis of Fig. 1(a) is observed that

$$\frac{V_0}{V_{in}} = H_C(s) \approx \frac{-A_0 a(s+am)}{(s+\xi_1)(s+\xi_2)}, \tag{2}$$

with:

$$\xi_{1,2} = -\frac{a}{2}\left(-1 \pm \sqrt{1 - 4A_0 m}\right), A_0 \gg 1, m \ll 1 \quad (3)$$

Choosing $4A_0 m \ll 1$, both poles are real and negative, ξ_1 next to zero and $\xi_2 \approx a$, as is shown in Fig. 1(b). The zero is real and negative too. Under these considerations the stability is guaranteed. Additionally, if $am < \xi_1$ then $R(s)$ is a very low frequency feedback loop. This way, the bandpass compensated response has practically the same characteristics that the uncompensated one: gain A_0 between ξ_1 and ξ_2 and a bandwidth $|\xi_2 - \xi_1|$ barely different to the uncompensated bandwidth, a. Therefore, the overall bandwidth is not degraded by the compensation and low frequency signals, such as offset and $1/f$ noise components, are not amplified by a factor A_0 because $H_C(s = 0) = A_0/(A_0 + 1) \approx 1$. Consequently, the resulting percentage of offset compensation (with regard to an uncompensated amplifier) is given by:

$$\begin{aligned} offset\_comp|_{open\_loop} &= 100\left(1 - \frac{H_C(0)}{H(0)}\right)\% \\ &\approx 100\left(1 - \frac{1}{A_0}\right)\% \end{aligned} \quad (4)$$

The compensation effect remains if an additional feedback loop is added to the compensated amplifier, as shown in Fig. 1(c). In this case, the low frequency response can be expressed as $V_0/V_{in}(0) = H_C(0)/(1 + H_C(0)\beta) \approx 1/(1 + \beta)$, while the corresponding uncompensated response is $V_0/V_{in}(0) = A_0(0)/(1 + A_0(0)\beta) \approx 1/\beta$. The percentage of offset compensation results:

$$offset\_comp|_{closed\_loop} \approx 100\left(1 - \frac{\beta}{\beta + 1}\right)\% \quad (5)$$

or in the case of a finite gain A_0:

$$offset\_comp|_{closed\_loop} = 100\left(1 - \frac{1 + A_0\beta}{1 + A_0(\beta + 1)}\right)\% \quad (6)$$

Equation (6) has been used to plot the curves showing the closed loop offset compensation versus $1/\beta$ that are given in Fig. 2. From inspection, it can be noticed that the offset compensation reach its highest value for $\beta < 0.1$ (closed loop gain of 10 or more). Even in the case of $A_0 = 1$, an offset compensation of approximately 50% can be obtained.

2.1 R(s) realization

Since large-valued passive elements are not available in integrated circuits, $R(s)$ is designed as a first order RC filter, where a very large-value resistor is realized by using active elements, as shown in Fig. 3(a). In [16], it was presented a simple scheme to design a large-valued, large-swing, floating resistive element using a series

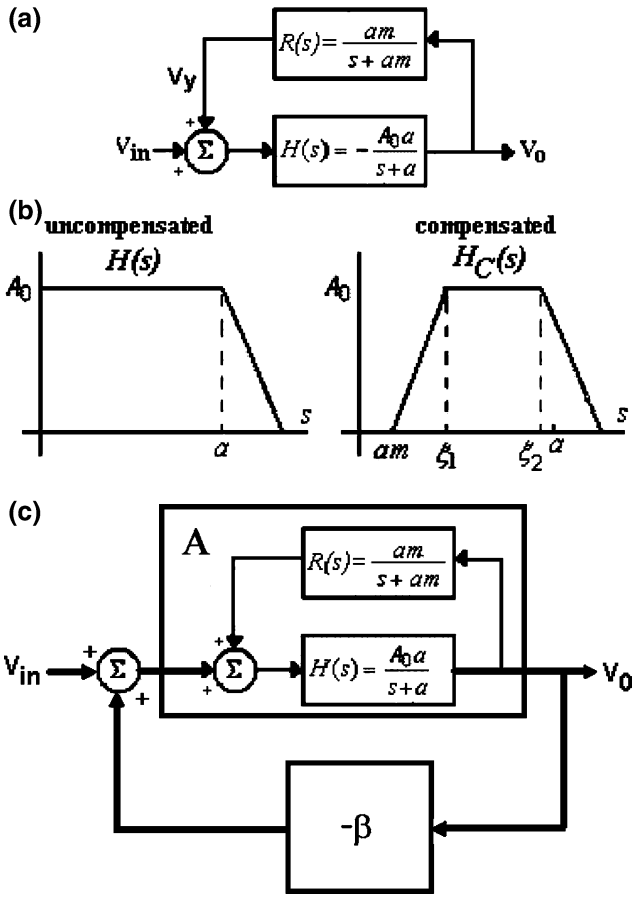

Fig. 1 (**a**) Semiactive feedback principle used as an offset compensation loop. (**b**) Frequency response of the uncompensated and compensated amplifiers. (**c**) Closed loop amplifier with offset compensation

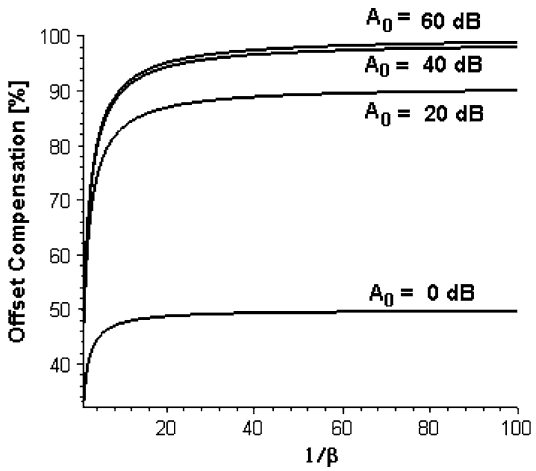

Fig. 2 Closed-loop offset compensation versus $1/\beta$

combination of a PMOS and a NMOS transistor, both biased in the subthreshold region (Fig. 3(b)). The effective resistance always remains very large in spite of large variations in the output voltage because positive or negative variations tend to turn on one transistor and turn off the other. The control voltages V_{bp} and V_{bn} allow controlling ξ_1 and keep M_{p5} and M_{n5} in weak inversion operation to force $R_G \ll R_B$ (where R_B is the resistance of the parasitic PN junctions of the MOS transistors), to avoid a parasitic resistive divider [16–18]. Since the impedance of R_G is on the order of Giga-Ohms, small capacitors can be used to implement the capacitor C, minimizing the area requirements. Because of the active realization of the passive RC filter, the compensation techniques will be denominated ''offset compensation techniques with semiactive feedback''.

2.2 Semiactive feedback through input (SFI)

A compensation scheme with SFI is shown in Fig. 4(b) for the case of a common source amplifier with floating gate inputs. The same amplifier is illustrated in Fig. 4(a) without the compensation feedback arrangement. The offset at the uncompensated output V_0, defined as the deviation of the DC output voltage from $V_{DD}/2$ (or a value established as analog ground), can be expressed as the product of the amplifiers's gain and the equivalent input offset, V_{offset}:

$$V_0 = -g_{mMn2}\left(r_{ds_{Mn2}} || r_{ds_{Mp1}}\right) V_{offset} \tag{7}$$

where g_m and r_{ds} denote transistor transconductances and output resistances, respectively. With the same considerations, the offset compensated output of the amplifier of Fig. 4(b), V_{01}, is calculated as:

$$-g_{mMn1}\left(r_{ds_{Mn1}} || r_{ds_{Mp1}}\right)\left(\frac{C_2}{C_1+C_2}V_{offset} + \frac{C_1}{C_1+C_2}V_{01}\right) = V_{01} \tag{8}$$

so:

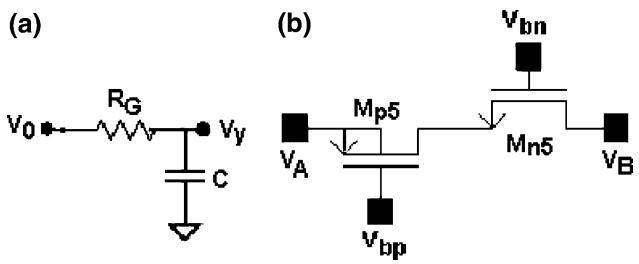

Fig. 3 (**a**) Semiactive first-order, low-pass filter, (**b**) R_G implementation with NMOS and PMOS transistors biased in subthreshold operation

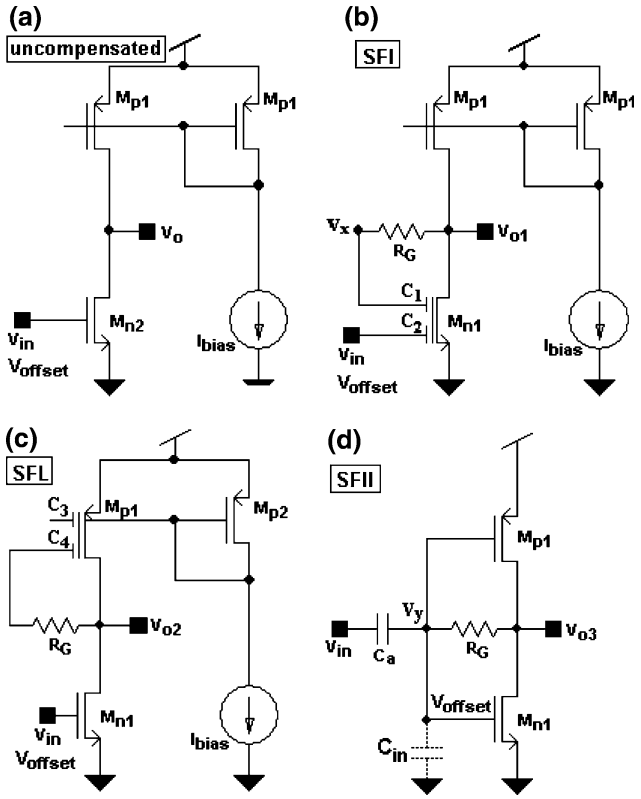

Fig. 4 (**a**) Uncompensated amplifier. (**b**) Amplifier compensated by SFI. (**c**) Amplifier compensated by SFL. (**d**) Amplifier compensated by SFII

$$V_{01} \approx -\frac{C_2}{C_1}V_{offset}, \frac{g_{mMn1}C_1}{C_1+C_2}\left(r_{ds_{Mn1}} || r_{ds_{Mp1}}\right) \gg 1 \tag{9}$$

where C_1 and C_2 are the floating gate capacitors and $V_x = V_{01}$ in DC. From (7) and (9), the offset compensation results:

$$\begin{aligned} Offset\_comp &= 100\left(1 - \frac{V_{01}}{V_0}\right)\% = 100\left(1 - \frac{A_{01}}{A_0}\right)\% \\ &= 100\left(1 - \frac{C_2}{g_{mMn2}\left(r_{ds_{Mn2}} || r_{ds_{Mp1}}\right)C_1}\right)\% \\ &= 100\left(1 - \frac{C_2}{C_1 A_0}\right)\% \end{aligned} \tag{10}$$

The compensation effect can be easily identified: if the DC component of $V_{01}(t_1)$ increases (diminishes) at instant t_1, then $V_x(t_1)$ also increases (diminishes). In the next instant t_2, the voltage $V_{01}(t_2)$ diminishes (increases) because $V_x(t_1)$ is the input of an inverter amplifier. Therefore, as consequence of the continuous time operation, any offset contribution of any nature (temperature, mismatch, lithographic defects, etc.) will be compensated.

2.3 Semiactive feedback through load (SFL)

Figure 4(c) shows a compensation scheme using semiactive feedback through the active load for the amplifier of Fig. 4(a). Analyzing the circuit of Fig. 4(c) with the same procedure employed in Sect. 2.2, the offset compensation can be expressed by:

$$\begin{aligned} Offset\_comp &= 100\left(1-\frac{V_{02}}{V_0}\right)\% = 100\left(1-\frac{A_{02}}{A_0}\right)\% \\ &= 100\left[1-\left(1+\frac{C_3}{C_4}\right)\frac{g_{mMn1}}{g_{mMp1}}\frac{1}{A_0}\right]\% \end{aligned} \tag{11}$$

Because there is not a floating gate that degrade g_{mMn1} [1], the SFL operates at higher frequencies but with smaller gain in the bandpass region $|\xi_2-\xi_1|$ than the SFI technique.

2.4 Semiactive feedback with isolated input (SFII)

Figure 4(d) shows the class AB amplifier with AC coupled input proposed in [16]. The AC coupling capacitor C_a and the resistance R_G form a high pass circuit with a corner frequency $f_{3dB\_low} = 1/(2\pi R_G C_a)$ (with $C_a \gg C_{in}$). Therefore, the amplifier cancels offset components at the input signal because its DC gain is zero. On the other hand, the equivalent offset component at V_Y is amplified in the case of an uncompensated class AB amplifier (i.e., without R_G) agree with:

$$V_{03} = -\frac{g_{mMn1}+g_{mMp1}}{g_{dsMn1}+g_{dsMp1}}V_{offset} = A_{0(AB)}V_{offset} \tag{12}$$

For the compensated amplifier, $V_Y = V_{offset} = -V_0\ |_{DC}$ because R_G and C form a low pass filter between the output and the node V_Y. The offset compensation results:

$$\begin{aligned} Offset\_comp &= 100\left(1-\frac{V_{03}}{V_0}\right)\% \\ &= 100\left(1-\frac{1}{A_{0(AB)}}\right)\% \end{aligned} \tag{13}$$

2.5 Semiactive feedback for fully differential circuits

The previously proposed techniques can be generalized for fully differential operation. In [19], two offset compensation arrangements (without floating gate transistors) using the SFL technique were presented. Those strategies, denominated *Unbalanced Branches Compensation technique* (UBC) and *Unbalanced Current Extraction Compensation Technique* (UCEC), consist on creating unbalanced bias currents and are particularly useful to design offset-compensated multipliers and dividers.

The semiactive feedback principle of Fig. 1(a) can be modified as is shown in Fig. 5(a) to obtain input referred offset contributions in the range of microvolts. In a straightforward analysis of Fig. 5(a), the input refereed offset becomes

$$V_{os\_input\_referred} = \frac{g_{m1}/g_{m2}}{A_{V1}A_{V2}}V_{os1} + \frac{1}{A_{V1}}V_{os2} \tag{14}$$

where A_{V1} and A_{V2} are the DC gains of the uncompensated and compensation amplifiers, respectively, V_{os1} and V_{os2} are the input refereed offsets of those amplifiers, and g_{m1}, g_{m2} are voltage to current conversation factors. An implementation of this scheme in a *Fully Differential Semiactive Feedback through Input (FDSFI)* configuration is illustrated in Fig. 5(b). The amplifier A_{V1} (composed by blocks g_{m1} and A_{V1}/g_{m1} in Fig. 5(a)) is a two stage, fully differential OTA with nulling-resistor frequency compensation and a Common-Mode Feedback circuit (CMFB). The CMFB is realized using large-valued, floating resistive elements of only a PMOS transistor, as proposed in [17], but with the PMOS transistors operating in weak inversion. Series-connected R_G elements are used to increase voltage swing. The compensation amplifier A_{V2} is a one stage, fully differential amplifier with an identical CMFB arrangement. The outputs of A_{V2}, V_{rp} and V_{rn}, are filtered using two second-order semiactive filters, F_1 and F_2 to obtain the control signals V_{ctr_n} and V_{ctr_p}. These signals and the input signals are converted to current (small signal approach) using the transistors M_{n1} and M_{n2} (blocks g_{m1} and g_{m2} in Fig. 5(a)) and added in the drain node of M_{n1}. This strategy avoids the use of floating gate transistors. Note that the bandwidth and gain are not degraded if $g_{m2} \ll g_{m1}$. The offset compensation with regard to an uncompensated OTA results:

$$Offset\_comp \approx 100\left(1-\frac{1}{A_{V1}}\left|\frac{V_{os2}}{V_{os1}}\right|\right)\% \tag{15}$$

The proposed techniques present the following characteristics:

- The speed-accuracy-power tradeoff is improved because the conditions of a near-to-ideal offset compensation strategy are satisfied.
- The compensation is proportional to $1/\beta$ and the gain of the uncompensated amplifier.
- The AC responses are almost unaffected.
- Negligible costs in area requirements and power consumption.

2.6 Noise analysis

Figure 6(a) shows the noise generated by each device of the circuit of Fig. 4(a), represented symbolically by an equivalent

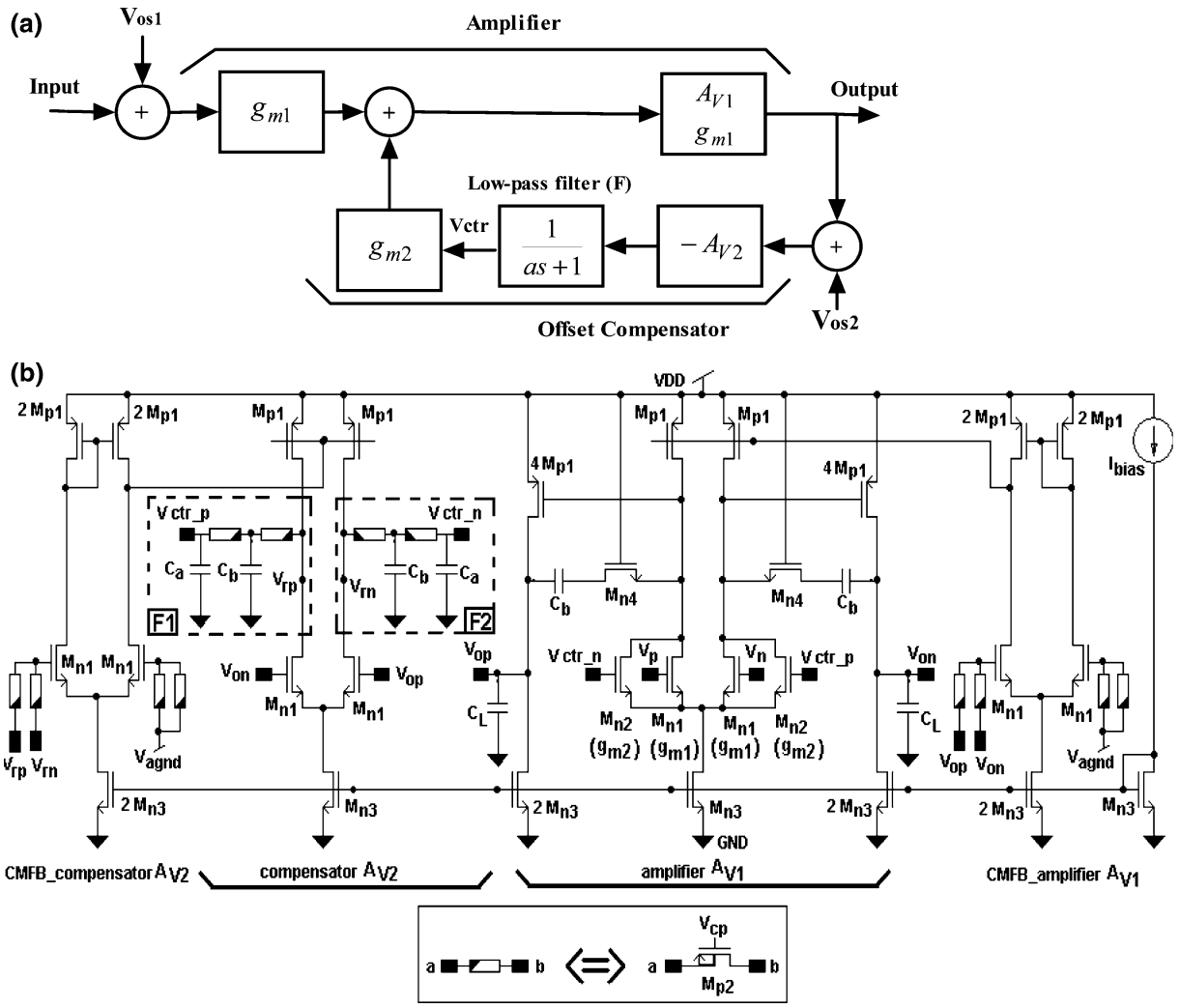

Fig. 5 (**a**) Semiactive feedback principle suitable to obtain input referred offsets in the range of microvolts. (**b**) Implementation of the compensation scheme of (**a**) in a fully differential OTA with offset compensation by FDSFI

voltage source v_{ni} connected to its gate. The equivalent input and output noise voltages have the mean square values [20]:

$$\overline{v_{n\_input}^2} = \overline{v_{n1}^2} + \left(\frac{g_{mp}}{g_{mn}}\right)^2 \overline{v_{n2}^2} \tag{16}$$

$$\overline{v_{n\_output}^2} = g_{mn}^2 R_0^2 \overline{v_{n1}^2} + g_{mp}^2 R_0^2 \overline{v_{n2}^2} \tag{17}$$

where R_0 is the output resistance. In the case of flicker noise and mismatch considered as a DC noise, the sources v_{ni} are given by [3, 20]

$$\overline{v_{ni}^2} = \frac{K_F \Delta f}{2\mu CoxWLf} \tag{18}$$

$$\overline{v_{ni}^2} = \sigma_{\Delta VT}^2 = \frac{A_{VT}^2}{WL} \tag{19}$$

where K_F is the flicker noise constant and A_{VT} is a constant associated with the CMOS process. From (16), (18), and (19) the input noise mean square voltages becomes

$$\overline{v_{n\_flicker\_input}^2} = \frac{KF_n \Delta f}{2\mu_n Coxf} \frac{1}{W_1 L_1} \left[1 + \frac{KF_n}{KF_p} \left(\frac{L_1}{L_2}\right)^2\right] \tag{20}$$

$$v_{offset}^2 = A_{VTn}^2 \frac{1}{W_1 L_1} \left[1 + \frac{A_{VTp}^2 \mu_p}{A_{VTn}^2 \mu_n} \left(\frac{L_1}{L_2}\right)^2\right] \tag{21}$$

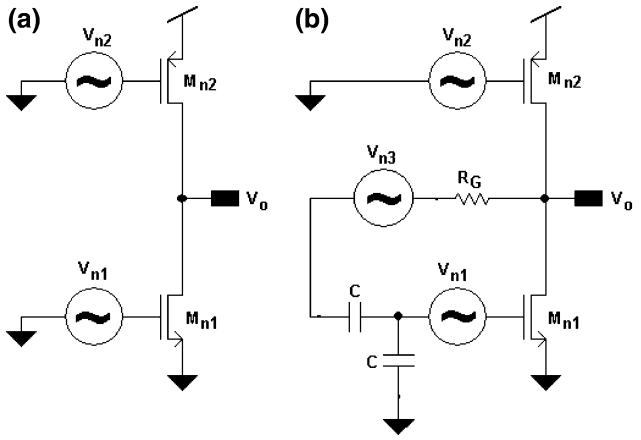

Fig. 6 (**a**) Noise sources of the circuit of Fig. 4(a). (**b**). Noise sources of the circuit of Fig. 4(b)

It can be noticed that the variance of the offset voltage has the same form as the variance of the 1/*f* noise voltage. Additionally, mismatch can be considered the extrapolated limit of low frequency noise. Consequently, if the offset contributions are reduced in a continuous time form, then the 1/*f* noise is reduced too.

Figure 6(b) shows the noise sources of the circuit of Fig. 4(b). Using small signal analysis in low frequencies (smaller than $s = \xi_1$), the output and input referred noises can be expressed as:

$$\overline{V_{n\_input}^2} = \frac{A_{v1}^2\overline{V_{n1}^2} + A_{v2}^2\overline{V_{n2}^2} + A_{v3}^2\overline{V_{n3}^2}}{A_V} = 4\overline{V_{n1}^2} + g_{mp}^2R_0^2\overline{V_{n2}^2} + \overline{V_{n3}^2} \tag{22}$$

$$\overline{V_{n\_output}^2} = A_{v1}^2\overline{V_{n1}^2} + A_{v2}^2\overline{V_{n2}^2} + A_{v3}^2\overline{V_{n3}^2} = 4\overline{V_{n1}^2} + g_{mp}^2R_0^2\overline{V_{n2}^2} + \overline{V_{n3}^2} \tag{23}$$

where $|A_{v1}| = 2$, $|A_{v2}| = g_{mp}R_0$, $|A_{v3}| = 1$ and $|A_v| = 1$ are the voltage gains with respect to V_{n1}, V_{n2}, V_{n3} and the input. From (23), is observed that the signal noise V_{n3}, generated by the active resistor, is not amplified. Also this noise is very small, with a maximum value given by $4qI_{DO}\exp[(V_G - V_S)/nV_T]\Delta f$ [21]. Comparing (17) and (23), a considerable reduction in the low frequency output noise of the offset compensated circuit can be appreciated. Agree with (16) and (22), it is not the case in the input refereed noise because the output noise of the PMOS transistor is divided only by $A_V = 1$. However, this disadvantage is easily solved using fully differential structures (for example, the circuit of Fig. 5(b)) in order to convert those noise components in common mode signals. In addition, for single ended structures the problem is appreciated only in frequencies below $s = \xi_1$ because of for $s > \xi_1$ the amplifier has the same gain A_V that the uncompensated one. With these analysis is concluded that the compensated amplifiers are not limited by noise to low-bandwidth applications.

3 Statistical analysis

In this section, a statistical method to estimate the offset variance in each compensation strategy is presented. Assuming V_{offset} to be a normal-distributed, random variable with unknown mean, v_{off}, and unknown variance, σ_{off}^2, taken from a space of n random samples, $V_{offset1}$, $V_{offset2}, \ldots V_{offsetn}$. A confidence interval of 100(1–α) percent for the standard deviation can be calculated as [22]:

$$\sigma_{off} \leq \sqrt{\frac{(n-1)S^2}{\chi_{1-\alpha,n-1}}} \tag{24}$$

with

$$\chi^2 = \frac{(n-1)S^2}{\sigma^2} \tag{25}$$

where S^2 is the variance of the n samples and the statistics χ^2 has the distribution shown in Fig. 7. The area under the interval $[\chi^2_{(1-\alpha/2),\,n-1}, \chi^2_{\alpha/2,\,n-1}]$ indicates that there is a probability of $(1 - \alpha)\%$ of obtain the real standard deviation in the interval given by (24).

4 Simulation results

The circuits of the Figs. 4 and 5 have been designed using BSIM3 models for a 0.5 μm CMOS AMIS process. Pelgrom's model was used for the HSPICE, MonteCarlo simulations. This model establishes [3, 23]:

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} \tag{26a}$$

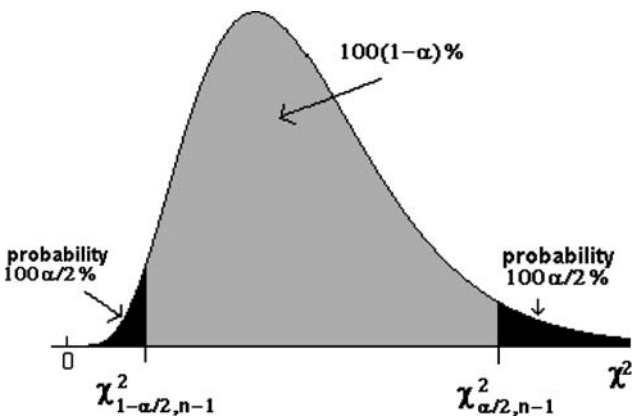

Fig. 7 χ^2 distribution used in the estimating of the offset variance

$$\frac{\sigma_\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}} \tag{26b}$$

where A_{VT} and A_β are constants associated with the process, WL is the effective area of the transistors and σ denotes standard deviation. Details of the circuits of Fig. 4 are described in Table 2. For constants A_{VTn} = 14 mV µm, A_{VTp} = 20 mV µm, $A_{\beta n}$ = 2% µm, $A_{\beta p}$ = 3%µm, six sigma analysis and the transistor dimensions of Table 2, maximum 3σ variations of Δ_{VTn} = 21.2 mV, Δ_{VTp} = 30.2 mV, $\Delta_{\beta n}$ = 3% and $\Delta_{\beta p}$ = 4.4% were calculated. Capacitors were simulated with maximum variations of 5%. Figure 8(a) shows the offset contributions versus Monte Carlo index (41-cases) for each of these amplifiers. In Fig. 8(b), the corresponding histograms have shown a tendency to normal distributions. The uncompensated amplifier presents output offsets in the range of ±100 mV (input referred offset in the range of ±3.07 mV), whereas the compensated circuits of Fig. 4(b)–(d) present offsets in the ranges of ±14 mV (input referred offset in the range of ±516.6 µV), ±10 mV (input referred offset in the range of ±476.2 µV) and ±2 mV (input referred offset in the range of ±73.26 µV), respectively. Confidence intervals of 99% for the standard deviation of these output offset contributions have been calculated using the expression (24) with n = 41.

Table 2 Design details of the amplifiers of Fig. 4

	Value
M_{n1}	W/L (µm) = 19.8/0.9
M_{n2}	W/L (µm) = 16.8/0.9
M_{p1}	W/L (µm) = 39.6/0.9
M_{p2}	W/L (µm) = 19.8/0.9
M_{n5}	W/L (µm) = 45.0/0.9
M_{p5}	W/L (µm) = 9.0/0.9
I_{bias}, V_{DD} , V_{bn}, V_{bp}	51.3 µA, 1.8 V, 1.8 V, 0.8 V
C_1, C_2, C_3, C_4, C_a, C_L	1 pF

The corresponding percentages of compensation respect to the uncompensated amplifier are presented in Table 3.

The DC and AC responses of the circuits of Fig. 4 have been plotted in Fig. 9 and summarized in Table 4. The SFI and SFL compensated amplifiers present the small DC gains predicted by expressions (9) and (11), while the SFII compensated amplifier presents a DC gain of zero, for what any offset component at the input signal is not amplified. It is observed that the presence of R_G degrades the output swing. Latter effect can be further reduced by increasing V_{bn} or the width of M_{n5}. The bandwidths are not significantly decreased (with regard to the uncompensated

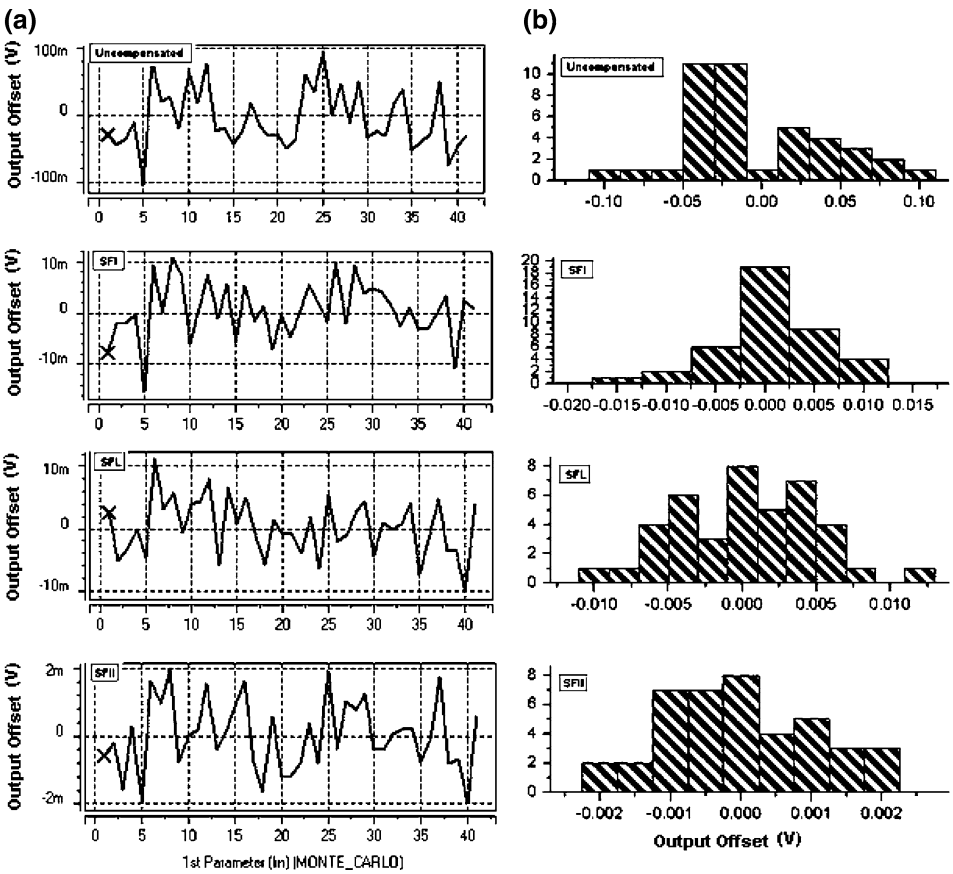

Fig. 8 (**a**) Operating point, Monte Carlo analysis at the output of the circuits of Fig. 4. (**b**) Histograms of the output offset contributions in (**a**)

Table 3 Confidence intervals of 99% for the standard deviation of the output offset contributions of the circuits of Fig. 4

Compensation strategy	Standard deviation	Compensation
Uncompensated	<60.8 mV	–
SFI	<7.5 mV	87.68%
SFL	<6.2 mV	89.77%
SFII	<1.4 mV	97.65%

amplifier's bandwidth), except in the SFII case, where the architecture defines the bandwidth. It can be also noticed that the phase margins are practically unaffected.

The output and input noise AC responses of the uncompensated and compensated circuits of Fig. 4 are illustrated in Fig. 10. The compensated and uncompensated responses have practically the same input and output referred noises above 10 Hz. The output noises of the compensated circuits are smaller than the output noise of the uncompensated circuit below 10 Hz, and the contrary occurs with the input-referred noise, as was predicted in Sect. 2.6.

Compensated and uncompensated versions of the circuit of Fig. 5(b) have been designed with the details summarized in Table 5. Maximum 3σ variations of Δ_{VTn} = 8.6 mV, Δ_{VTp} = 11.6 mV, $\Delta_{\beta n}$ = 1.2% and $\Delta_{\beta p}$ = 1.7% were calculated (For the PMOS transistors of R_G, Δ_{VTp} = 69.2 mV and $\Delta_{\beta p}$ = 10.3%). Figure 11(a) shows the corresponding input-referred offset contributions versus Monte Carlo index (41-cases) for open loop operation. It is observed that the uncompensated and compensated amplifiers presents offsets in the ranges ±1.5 mV and (–2 μV, 10 μV), respectively. Theoretically, these levels can be reduced to nanovolts if the differential pairs are designed with large L (instead of minimum L) and the gain of the amplifier is increased to 100 dB. According to the corresponding histograms of Fig. 11(b), the uncompensated circuit does not presents a normal distribution because of the output of the amplifier is saturated by these levels of input offset (see Fig. 12). Confidence intervals of 99% for the offset standard deviation were calculated using the expression (24). From Table 6 can be appreciated a 99.74% of offset compensation (underestimated because of the saturation of the uncompensated amplifier).

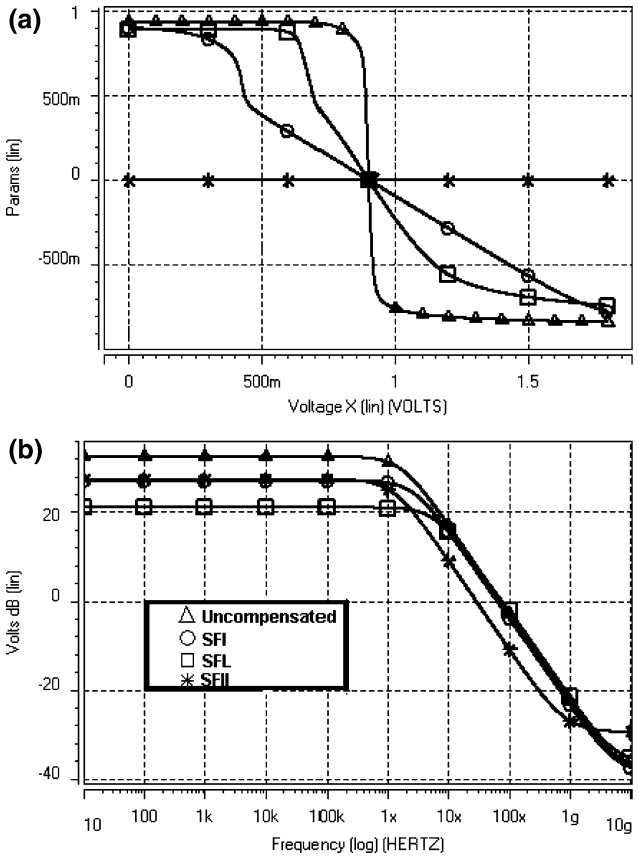

Fig. 9 Behavior of the circuits of Fig. 4. (**a**) DC response. (**b**) AC response

Table 4 DC and AC behavior of the amplifiers of Fig. 4

Amplifier	A_V (DC) (V/V)	$A_V(\xi_1 < s < \xi_2)$ (V/V)	f_c (MHz)	BWP (MHz)	Phase margin
Uncompensated	32.5	32.5	1.7	71.6	89.2
SFI	0.95	27.1	2.7	62.4	86.2
SFL	2.3	21.0	6.3	75	95.2
SFII	0	27.3	1.2	28	89.8

The AC responses of the uncompensated and compensated OTAs are illustrated in Fig. 13 and summarized in Table 7. The magnitude response of the compensated circuit presents the form predicted in Fig. 1(b). Above ξ_1 = 50 Hz, the compensated and uncompensated responses have practically the same gain, cutoff frequency, gain-bandwidth product and phase margin. The noise behavior is similar in booth circuits too. Below 50 Hz, the output noise of the compensated circuit is smaller than the output noise of the uncompensated one, and the contrary occurs with the input-referred noise, as was predicted in Sect. 2.6. However, the difference is the low frequency, input-referred noises is small because the noise in the PMOS loads is converted in a common mode signal in the fully differential amplifier. Note that the noise and offset contributions can be easily reduced because the design was realized with minimum L transistors in the differential pairs. Also, ξ_1 can be reduced if V_{cp} is increased (PMOS transistor of R_G nearest to the turned off state).

The power consumption increases with the compensation 42.8%, from 0.77 mW to 1.1 mW. That increment can be reduced to 10% if CMFB circuits are realized as

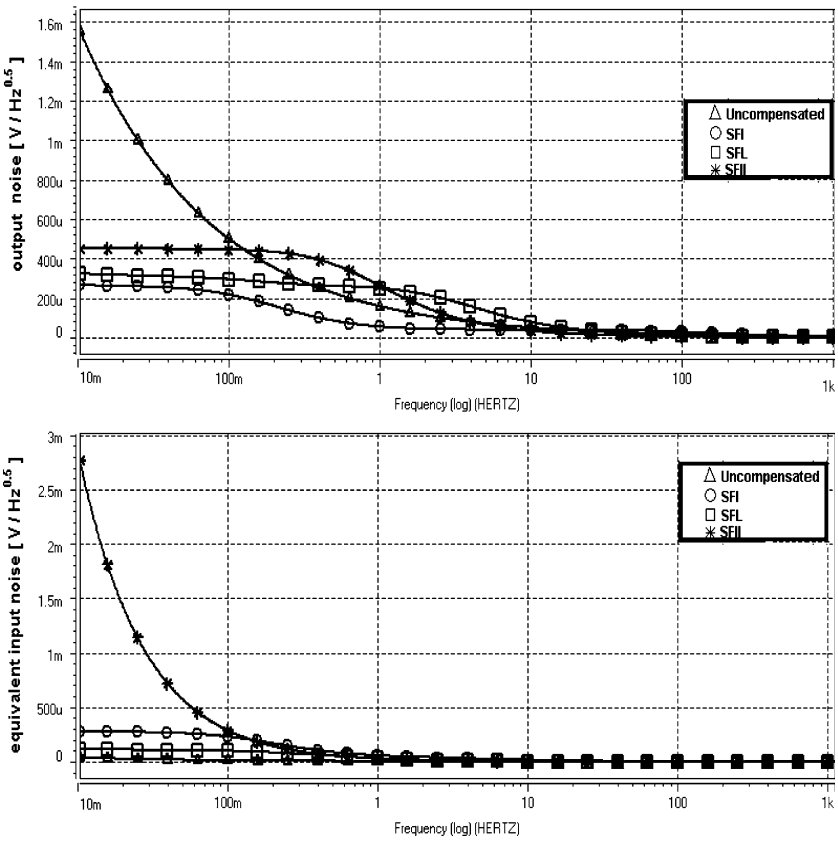

Fig. 10 Output and input noise AC responses of the circuits of Fig. 4

proposed in [17], and the tail current of the compensation amplifier is reduced to 25 μA instead of 50 μA.

Next, the improvement in the speed–accuracy–power tradeoff will be evaluated. If an increment of $N\%$ in the accuracy (maintaining the speed) is wanted without using a compensation array, then the power consumption should be increased because the speed–accuracy–power tradeoff is a constant, i.e.:

$$\frac{\text{Speed}_1 \cdot \text{Accuracy}_1^2}{\text{Power}_1} = \frac{\text{Speed}_1 \cdot \text{Accuracy}_1 (1 + N/100)^2}{\text{Power}_2} \tag{27}$$

so:

$$\frac{\text{Power}_2}{\text{Power}_1} = (1 + N/100)^2 \tag{28}$$

Therefore, for increasing the accuracy in the $N = 99.74\%$ obtained with the circuit of Fig. 5(b), an increment of 398.6% in the power consumption would be required. This percentage is under-estimated because huge transistors would be necessary for obtain the required accuracy, where additional global mismatch effects appear [23].

5 Experimental results

The circuit of Fig. 4(d) was fabricated with AMIS 0.5-μm CMOS technology, with three metal and two poly layers, through MOSIS. The design details are presented in Table 8 and the microphotograph shown in Fig. 14. This structure occupies a silicon area of 100 μm × 180 μm, including the test pad. The experiment was realized using a Cascade Microtech test station MTS-2200 and an oscilloscope TDS 3054 Tektronic. The input employed was a sinusoidal signal with amplitude of 120 mV and

Table 5 Design details of the amplifier of Fig. 5(b)

	Value
M_{n1}	W/L (μm) = 48/0.6
M_{n2}	W/L (μm) = 12/1.2
M_{n3}	W/L (μm) = 24/1.2
M_{n4}	W/L (μm) = 8.4/0.9
M_{p1}	W/L (μm) = 24/1.2
M_{p2} (resistor R_G)	W/L (μm) = 1.5/0.6
I_{bias}, V_{DD} , V_{agnd}, V_{cp}	50 μA, 2.2 V, 1.5, 1.8 V, 1.1 V
C_a, C_b, C_L	1.2 pF, 0.6 pF, 0.5 pF

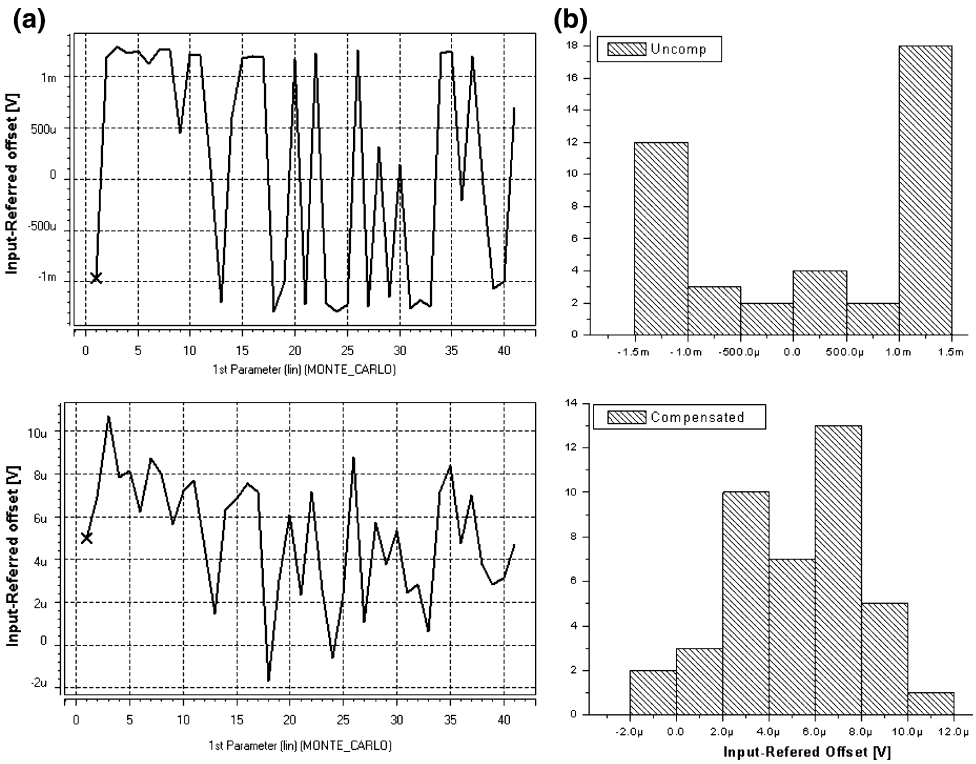

Fig. 11 (**a**) Monte Carlo analysis ($n = 41$) of the input referred offset of Fig. 5(a), uncompensated and compensated, respectively. (**b**) Histograms of the offset contributions in (**a**)

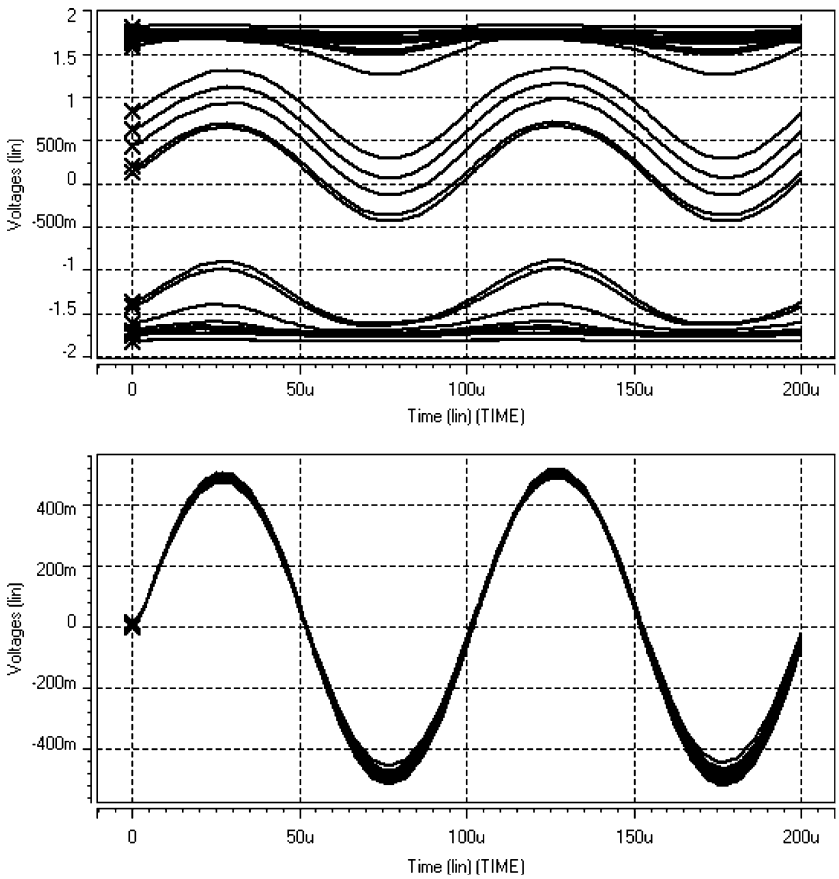

Fig. 12 Uncompensated and compensated open-loop time responses of the circuit of Fig. 5(b). The MonteCarlo analysis was realized with $n = 41$ and an input signal of amplitude 0.4 mV and frequency 10 KHz

Table 6 Confidence intervals of 99% for the standard deviation of the input-referred offset in the uncompensated and compensated OTAs of Fig. 5(b)

Compensation strategy	Standard deviation	Compensation
Uncompensated	<1.46 mV	–
Compensated	<3.79 μV	99.74%

frequency of 10 Hz. As was expected, the input signal was rejected at this frequency and the output only presented a mean DC value of 1.087 V. Four chips were measured to obtain the standard deviation of this value. Ten thousand data were obtained with the oscilloscope for each of the chips. The results have been summarized in Table 9. The standard deviation of the mean output-referred offsets was 5.1 mV. This value is bigger than the predicted in Table 3, but still very low when compared to Monte Carlo simulations of the uncompensated circuit of Fig. 4(a). The main reason for this difference is the smaller dimensions of the transistors of the Table 8 when compared to the transistors of the Table 2. Moreover, additional global mismatch variations appear from chip to chip. Note that the mean and standard deviation offsets are in the range of the input offset of a MOS transistor, consequently is verified that the input offset is not amplified by the gain of the amplifier, as was discussed in Sect. 2.4. Also, it was observed that any additional offset component of the input signals is rejected by the amplifier, for what A_V $(s = 0) = 0$ V/V as was obtained in Table 4. Later on, the frequency of the input signal was increased to 1 kHz. It was observed that in this frequency the input signal is not rejected, and the output presented the inverting behavior expected.

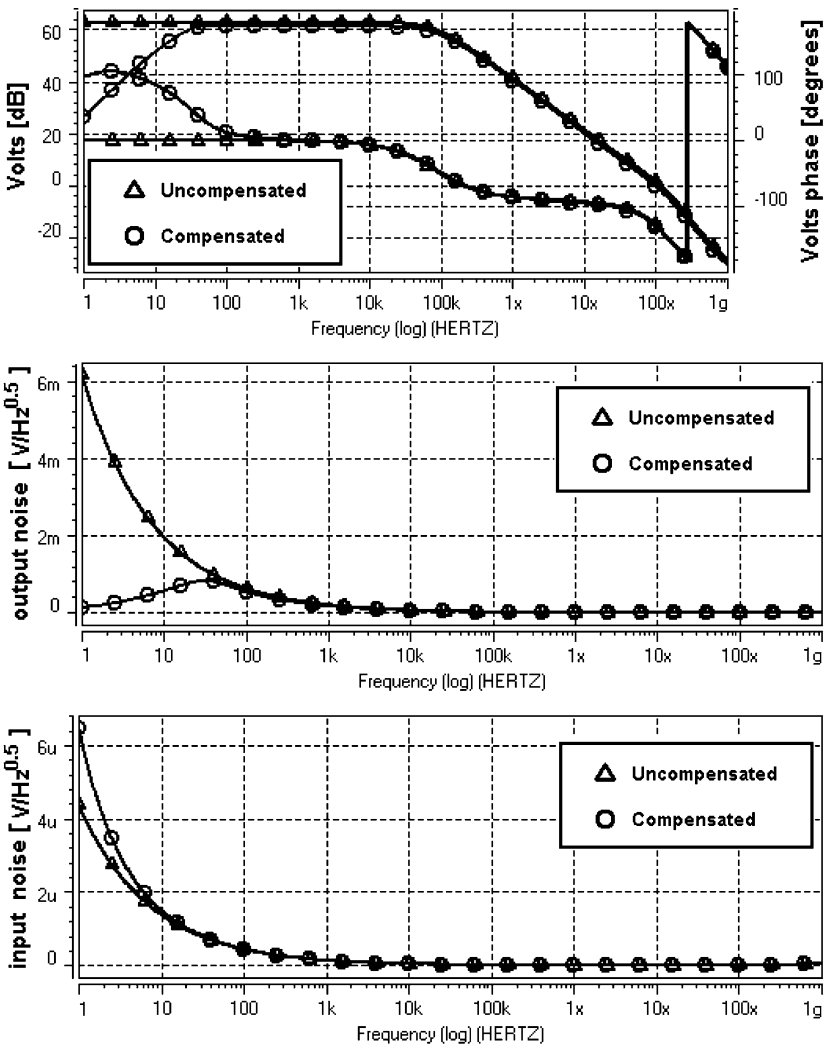

Fig. 13 Magnitude, phase, output-referred noise and input-referred noise AC responses of the uncompensated and compensated OTAs of Fig. 5(b)

Table 7 AC behavior of the uncompensated and compensated OTAs of Fig. 5(b)

Amplifier	$A_V(\xi_1 < s < \xi_2)$ (V/V)	f_c (KHz)	BWP (MHz)	Phase margin	Input Noise @ 100 Hz	Output Noise @ 100 Hz
Uncompensated	62.97 dB	83.17	112	47	436 nV/Hz$^{1/2}$	0.61 mV/Hz$^{1/2}$
Compensated	61.45 dB	87.09	97.8	51.3	440 nV/Hz$^{1/2}$	0.53 mV/Hz$^{1/2}$

Table 8 Design details of the fabricated amplifier of Fig. 4(d)

	Value
M_{n1}	W/L (μm) = 12/0.9
M_{p1}	W/L (μm) = 21/0.9
M_{n5}	W/L (μm) = 12/0.6
M_{p5}	W/L (μm) = 10.5/0.6
V_{DD}, V_{bn}, V_{bp}	2.5 V, 1.8 V, 0.1 V
C_a	0.5 pF

Table 9 Measured results of the fabricated prototype

Chip	Mean output	Absolute deviation, with regard to the overall mean (mV)
Chip 1	1.0878 V	6.11
Chip 2	1.0770 V	4.78
Chip 3	1.0840 V	2.23
Chip 4	1.0782 V	3.56
Overall mean	1.0812 V	
Standard deviation	5.09 mV	

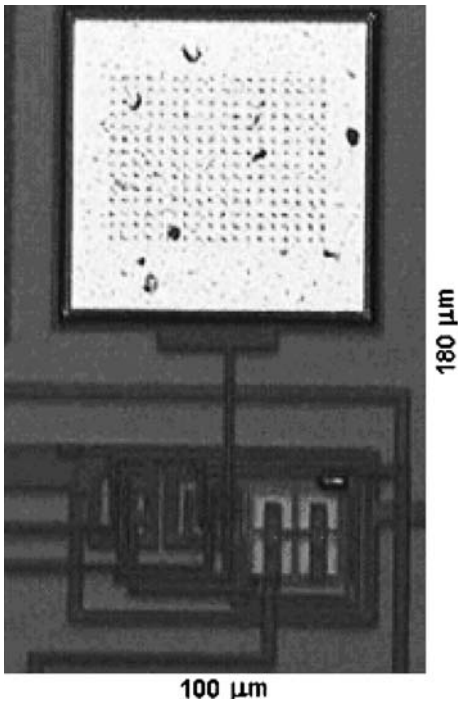

Fig. 14 Microphotograph of the fabricated amplifier of Fig. 4(d)

6 Conclusions

Four novel, continuous-time offset compensation strategies to CMOS amplifiers have been presented. These strategies, based in a semiactive feedback approach realized in a standard CMOS process, satisfy the requirements of a near to ideal offset compensation strategy. The approach does not require post-fabrication treatment, reducing the costs, and allowing improve the speed–accuracy–power tradeoff due to their negligible requirements of power and area. Consequently, these techniques are appropriate for analog VLSI, where trimming techniques would be extremely impractical. Also, this approach scales with the technology, a characteristic very important because mismatch effects worsen with the scaling. Other advantage is the very easy implementation of the compensation strategies, for what the designers do not require a very specialized background. An experimental prototype has been fabricated and measure to verify the feasibility and functionality of the semiactive feedback strategy. Finally, the semiactive feedback technique can be used in other analog processing blocks, such as multipliers, dividers, filters and other structures.

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