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# Multiple operating points in a square-root domain first-order filter

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SUMMARY

In this paper novel corrective circuits to avoid multiple operating points in a square-root domain first-order filter are proposed. By employing a DC test it is demonstrated that the filter possesses three operating points (two stable and one unstable) and the corrective circuits enforce the proper operating mode. The corrective circuits and filter are able to operate with very low supply voltages (as low as $V_{GS} + 2V_{DS_{sat}}$). Moreover, a detailed analysis concerning the impact that produces the corrective circuits on the filter performance is discussed. Both measurement and simulation results are provided to validate the circuits and analysis employed. Copyright © 2006 John Wiley & Sons, Ltd.

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KEY WORDS: multiple operating points; MOS translinear loops; current-mode circuits; companding

## 1. INTRODUCTION

DC analysis, one of the most important and difficult tasks for designing analog circuits, is concerned with the static operation of the circuit. DC analysis consists in determining the circuit variables when the input stimuli are DC sources [1]. Thus it can be considered as the task of finding the solutions for a resistive network model. These solutions are coined as 'the operating points'. Circuits with multiple operating points often appear in electronics [1] when certain circumstances of both circuit topology and circuit parameters coalesce. A lot of theoretical research effort has been devoted to explore multiple operating points (MOP) in transistor circuits [2, 3], in spite of this fact the issue has been solved only partially [4, 5]. Due to the fact that the currently available

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circuit simulation packages resort to the well-known Newton–Raphson method, they are able to find only one DC operating point. Recent works are focused on finding MOP by using alternative methods [6, 7], but they are neither general nor easy to be implemented.

In fact the existence of MOP is not only a problem for circuit analysis but also for circuit design. Particularly in continuous time implementations this behaviour needs to be avoided in order to enforce the correct operation mode at any time. However, very limited attention has been devoted to explore MOP [8, 9] by circuit designers. To solve partially this lack of research, this paper focuses on a circuit designer-oriented treatment of the MOP problem that after achieving a detailed analysis of the circuit behaviour, it provides a solution at circuit level. This methodology is applied to a square-root domain (SRD) system that exhibits MOP, but it can be readily extended to other circuits.

The SRD systems [10], a subset of the so called companding systems, are an interesting alternative to develop circuits with very low supply voltage ($V_{DD}<2V_{GS}$) required in portable equipment and systems implemented by the most modern CMOS fabrication process [11]. The companding technique exploits the current mode and the large signal behaviour of transistors to achieve a non-linear compression of the voltage swings, allowing an extended dynamic range and less sensitive of the signal/noise ratio to the reduction of supply voltage. Although there is an internally non-linear behaviour in these systems the input–output relationships remain linear [12]. This fact is obtained implementing specific non-linear blocks in such a way that the linearization arises as a whole, i.e. the internal non-linearities cancel out conveniently leading to a linear system. Often these non-linear blocks are implemented employing translinear techniques [13, 14]. The first companding systems were implemented employing BJT transistors (or MOS transistors in weak inversion) exploiting their exponential $I$–$V$ characteristic leading to log-domain systems [15–17]. Afterward the systems were realized by the quasi-quadratic law of MOS transistors to avoid the problems of mismatches and poor bandwidth of MOS devices in weak inversion region, leading to SRD systems [18, 19].

In this paper a SRD first-order filter is designed based on the MOS translinear loops described in Reference [20]. Here, a dynamic biasing is proposed that allows to reduce significantly the channel-length modulation effect in the TL loop. The filter operates with a 1.5 V supply voltage showing MOP. To identify the number of solutions and their stability, a method based on testing the $V$–$I$ characteristics on selected ports in the SRD filter is employed. As a result three operating points are identified, being two stable and one unstable. Finally, novel corrective circuits to make the filter usable in practical applications are proposed, and the performance impact of these circuits on the filter is investigated. These novel circuits can be readily extended for avoiding MOP in other circuits or applications. Simulations and measurement results from a fabricated prototype are offered in order to validate the techniques and analysis proposed here.

The paper is organized as follows: in Section 2, the blocks to implement the SRD filter are presented. Concepts regarding the number of operating point and their stability are described in Section 3. In Section 4, novel circuits that avoid MOP are proposed and their impact on the filter performance is investigated. Finally, conclusions are drawn in Section 5.

## 2. THE FIRST-ORDER SRD FILTER

Companding systems can be implemented applying a non-linear mapping on a linear prototype. Often the law employed for the mapping is the non-linear $V$–$I$ characteristic of transistor leading

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to log-domain systems (BJT or MOS transistors in weak inversion) [16, 17] or SRD systems (MOS transistor in strong inversion and saturation region) [18, 19]. This non-linear mapping translates the linear components of the prototype into non-linear ones that build the companding system. These non-linear blocks can be easily implemented by the large signal behaviour of a transistor loop arrangement (translinear loops) [13, 14].

In the following paragraphs a class-A SRD first-order filter will be designed employing a differential equation that describes the operation of an externally equivalent linear prototype [21]. Consider a damped current-mode integrator expressed by the following linear differential equation:

$$\tau \dot{I}_{\text{out}} + I_{\text{out}} = k I_{\text{in}} \tag{1}$$

being $k$ and $\omega_{-3\,\text{dB}} = 1/\tau$ the DC gain and cut-off frequency, respectively. Now consider that the output current $I_{\text{out}}$ is non-linearly related to a certain voltage $V_{\text{c}}$ by

$$I_{\text{out}} = \frac{\beta}{2}(V_{\text{c}} - V_{\text{T}})^2 \tag{2}$$

i.e. the quadratic behaviour of a MOS transistor working in strong inversion and saturation region, where $V_{\text{c}}$, $\beta$ and $V_{\text{T}}$ are the gate-source voltage, the transconductance parameter and the threshold voltage, respectively. It can be shown in Reference [21] that substituting Equation (2) in Equation (1), applying the chain rule, scaling by a factor $C$ (a capacitance) and solving for $V_{\text{c}}$, Equation (1) becomes,

$$C\dot{V}_{\text{c}} = \frac{Ck}{\tau\beta}\frac{I_{\text{in}}}{(V_{\text{c}} - V_{\text{T}})} - \frac{C}{2\tau}(V_{\text{c}} - V_{\text{T}}) \tag{3}$$

Equation (3) can be interpreted as a nodal equation [22], where LHS is easily achieved through a linear capacitor $C$, and RHS by two non-linear transconductors. In References [18, 21], it is demonstrated that Equation (3) can also be expressed in terms of bias current as

$$C\dot{V}_{\text{c}} = \sqrt{\frac{2I_{B2}}{\beta}}\frac{I_{\text{in}}}{(V_{\text{c}} - V_{\text{T}})} - \sqrt{\frac{\beta I_{B1}}{2}}(V_{\text{c}} - V_{\text{T}}) \tag{4}$$

where the cut-off frequency and DC gain are related to $I_{B1}$ and $I_{B2}$ by

$$\omega_{-3\,\text{dB}} = \frac{1}{\tau} = \frac{\sqrt{2\beta I_{B1}}}{C}, \quad k = \sqrt{\frac{I_{B2}}{I_{B1}}} \tag{5}$$

Equation (4) can be alternatively represented by a dynamic non-linear current-mode expression employing Equation (2), i.e.

$$C\dot{V}_{\text{c}} = \sqrt{I_{B2}}\frac{I_{\text{in}}}{\sqrt{I_{\text{out}}}} - \sqrt{I_{B1}}\sqrt{I_{\text{out}}} \tag{6}$$

Equation (6) represents a current-mode system with its internal capacitance voltage ($V_{\text{c}} = \sqrt{2I_{\text{out}}/\beta} + V_{\text{T}}$) compressed. In spite of the highly non-linear terms involved in Equation (6), the input–output relationship ($I_{\text{in}}$–$I_{\text{out}}$) remains linear.

By employing Equation (6), the structure of the SRD first-order filter can be derived, as depicted in Figure 1. Herein, the non-linear mapping (2) is obtained by matched transistors $M_1$, $M_2$, and $M_3$.

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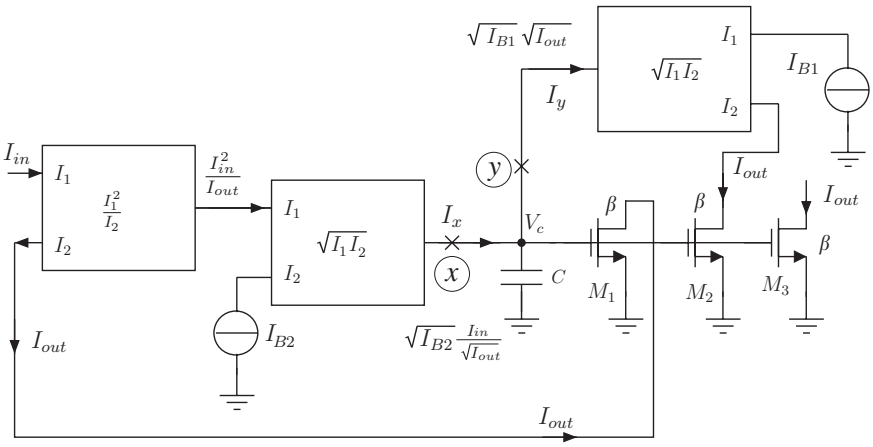


Figure 1. SRD filter implementation employing squarer/divider and geometric mean cells.

In Figure 1, the RHS of Equation (6) is implemented by a pair of current-mode geometric-mean cells as well as a squarer/divider cell [21].

The first term of the RHS in Equation (6) is denoted as $I_x$:

$$I_x = \sqrt{I_{B2}}\,\frac{I_{\text{in}}}{\sqrt{I_{\text{out}}}} = \sqrt{\frac{2I_{B2}}{\beta}}\,\frac{I_{\text{in}}}{(V_{\text{c}} - V_{\text{T}})} \tag{7}$$

that is obtained cascading a squarer/divider cell and a geometric-mean cell.

The second term of the RHS is denoted as $I_y$:

$$I_y = \sqrt{I_{B1}}\sqrt{I_{\text{out}}} = \sqrt{\frac{\beta I_{B1}}{2}}\,(V_{\text{c}} - V_{\text{T}}) \tag{8}$$

that is simply achieved by a geometric-mean cell.

In Figure 1, the voltage at the capacitor $V_{\text{c}}$ is stabilized by a double negative feedback loop. On one hand, the loop through $V_{\text{c}}$ and $I_y$, and on the other, the loop through $V_{\text{c}}$ and $I_x$. Thus for any increment at the input current $\Delta I_{\text{in}}$, a corresponding increment will be reflected on $\Delta I_x$, $\Delta V_{\text{c}}$, $\Delta I_{\text{out}}$, and $\Delta I_y$. These increments due to the feedback loops discharge the capacitor current compensating the initial increments. In DC regime ($\dot{V}_{\text{c}} = 0$), and assuming class-A operation, an analytical expression for the voltage across the capacitance denoted as $V_{\text{DC}_{\text{c}}}$ can be found as

$$V_{\text{DC}_{\text{c}}} = \sqrt{\frac{2}{\beta}\sqrt{\frac{I_{B2}}{I_{B1}}}} \times \sqrt{I_{\text{DC}_{\text{in}}}} + V_{\text{T}} \tag{9}$$

where $I_{\text{DC}_{\text{in}}}$ is the DC input current.

As a result, the DC current components $I_{\text{DC}_x} = I_{\text{DC}_y}$ are given by

$$I_{\text{DC}_x} = I_{\text{DC}_y} = \sqrt[4]{I_{B1} I_{B2}} \times \sqrt{I_{\text{DC}_{\text{in}}}} \tag{10}$$

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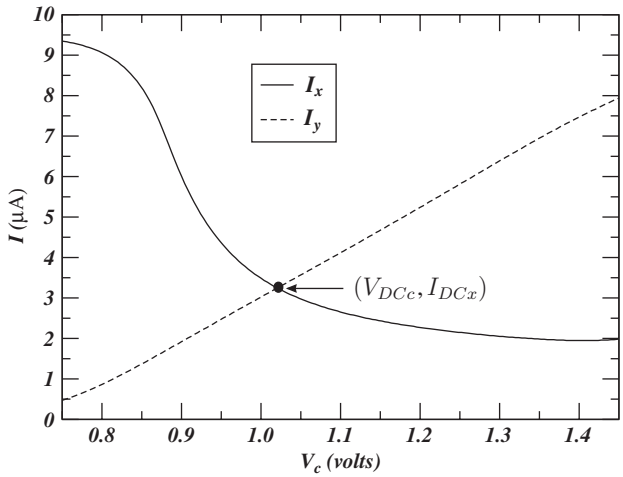


Figure 2. DC solution employing a graphical representation.

In order to provide more insight, Figure 2 shows typical measured $V$–$I$ characteristics of the DC response for the currents $I_x$ and $I_y$. Both currents are represented as a function of $V_c$ (see Equations (7) and (8)). These $V$–$I$ characteristics were obtained employing a 0.8 μm AMS CMOS technology with $V_T = 0.8$ V, $\beta = 95$ μA/V$^2$ and the circuits presented in Reference [20].

In Figure 2 current saturation for $I_x$ is observed for values lower than 0.85 V, deviating from the expected behaviour described by Equation (7). Both currents $I_x$ and $I_y$ are monotonic functions of $V_c$ leading to a unique DC operating point ($I_x = I_y$). In the following sections it will be shown that the block implementation for the SRD filter in this paper offers a non-monotonic function for $I_x$ causing MOP [23].

### 2.1. Block implementation

The basic non-linear blocks described in Equation (6) can be easily designed using second-order up–down voltage translinear loops (see Figure 3). Figure 3 shows a typical circuit [14], where the translinear loop is formed through transistors $M_1$–$M_4$ and the remaining transistors are used to bias it properly. As it is well known, the principle involves the following relationship among their drain currents:

$$\sqrt{I_{d1}} + \sqrt{I_{d2}} = \sqrt{I_{d3}} + \sqrt{I_{d4}} \tag{11}$$

Equation (11) is deduced assuming the same $W/L$ ratio for the transistors $M_1$ to $M_4$ in Figure 3, and that they are working in the strong inversion and saturation region [14].

Manipulating conveniently the drain currents of translinear loop in Figure 3, the cell can be configured as either a geometric mean or squarer/divider circuit. To this end, the strategy to inject currents into the TL loop is described by

$$I_{d3} = I_{d4} = \frac{I_{d1} + I_{d2} + 2I_5}{4} \tag{12}$$

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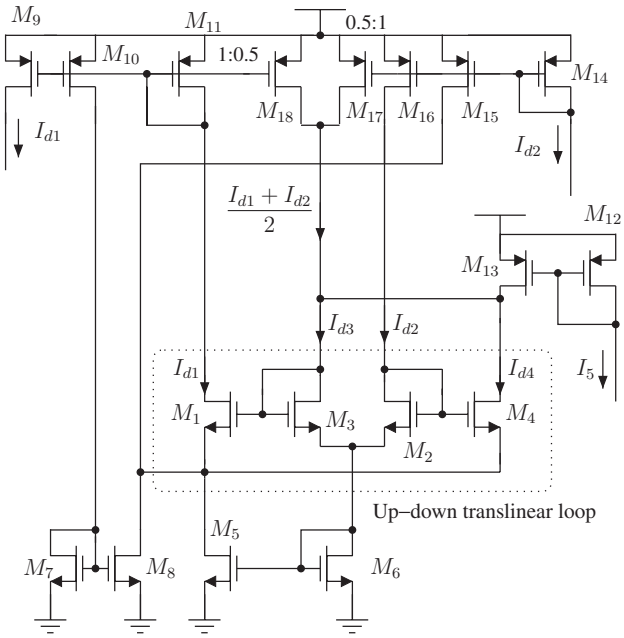


Figure 3. Typical up–down voltage translinear loop with biasing circuitry included.

where $I_5$ is an arbitrary current. Substituting Equation (12) in Equation (11) and solving for $I_5$ it stands by

$$I_5 = \sqrt{I_{d1} I_{d2}} \tag{13}$$

Thereby, depending on which current is taken as output (inputs), the TL loop can be configured as geometric-mean cell or squarer/divider cell. For instance, the circuit shown in Figure 3 is biased to operate as a squarer/divider cell with $I_5$ and $I_{d2}$ as inputs and $I_{d1}$ as output. In Figure 3 transistors $M_5$–$M_6$, $M_7$–$M_8$, $M_9$–$M_{11}$, $M_{12}$–$M_{13}$, and $M_{14}$–$M_{16}$ are current mirrors with $M_{18}$ and $M_{17}$ half of $M_9$ and $M_{14}$, respectively. Note that the transistor $M_6$ connected as diode sets a proper biasing at the bottom of the translinear loop, in such a way that sources of $M_1$ and $M_4$ are accommodated according to Equation (11). The minimum voltage to operate the cell of Figure 3 correctly is $V_{GSM_6} + V_{GSM_2} + V_{DS_{sat}M_{16}} = 2V_{GS} + V_{DS_{sat}}$.

Most of the former designs employing MOS TL loops follow the bias technique shown in Figure 3, therefore they do not fully exploit the capability to work with very low voltage [14]. Thus for reducing the supply voltage as much low as possible, their biasing circuit needs to be modified [21]. In this sense, the biasing circuit employed is based on the strategy reported in Reference [20]. In such a strategy shown in Figure 4, two transistors in triode region ($M_5$ and $M_6$) are employed reducing the supply voltage requirements. Another characteristic of this approach is the inclusion of static level shifters $V_B$'s to enlarge the dynamic range of the translinear loops. In this paper the inclusion of the dynamic level shifter $V_F$ is proposed. This level shifter minimizes the channel-length modulation effect over the TL loop that implements the squarer/divider cell as will be described subsequently.

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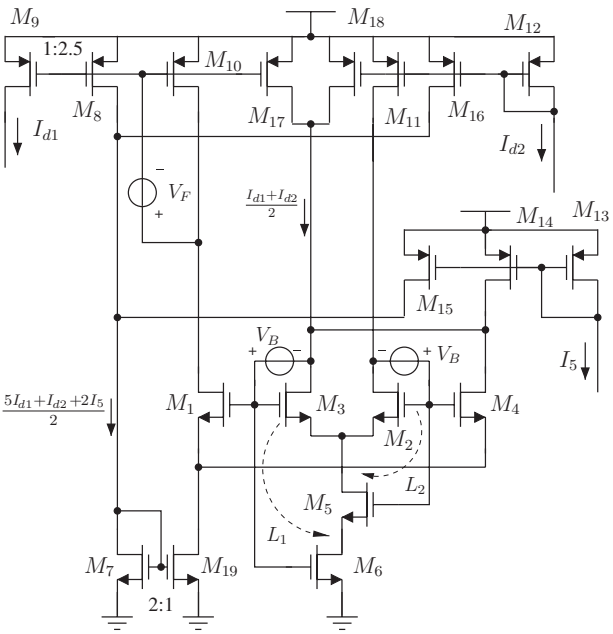


Figure 4. Proposed squarer/divider circuit with extended dynamic range. Transistors $M_5$ and $M_6$ are working in triode region forming a coupled negative feedback $L_1$ and $L_2$.

Figure 4 depicts an up–down TL loop as squarer/divider. $M_1$–$M_4$ form the main loop and transistors $M_5$–$M_6$ are operating as voltage controlled resistors with values of

$$R_5 \approx \frac{1}{\beta_5(V_{gs5} - V_{\mathrm{T}})}, \quad R_6 \approx \frac{1}{\beta_6(V_{gs6} - V_{\mathrm{T}})} \tag{14}$$

The remaining transistors form current mirrors to apply the proper current injection to the TL loop in compliance with Equation (12). The design applies an alternative biasing scheme at the bottom of the TL loop ($M_2$ and $M_3$ sources) [20], since the classical diode-connection employed in Figure 3 by transistor $M_6$ [24] has been omitted, significantly reducing the voltage requirements from $V_{\mathrm{GS}}$ to $2V_{\mathrm{DS_{triode}}}$ volts. Here, it has been considered that $2V_{\mathrm{DS_{triode}}} \geqslant V_{\mathrm{DS19}}$ to maintain transistor $M_{19}$ in saturation. This is easily obtained with a correct selection of the aspect ratios of transistors $M_5$ and $M_6$. This fact and the feedback introduced by $L_1$ and $L_2$ set an appropriate bias voltage at the bottom of the TL loop as shown in Figure 5.

In the right-hand side of Figure 5, when a current increment in $I_1$ or $I_2$ (the drain of $M_2$ or $M_3$) occurs, the current $I_s$ as well as voltages $V_{\mathrm{d}}$, $V_1$, and $V_2$ are incremented. These increments lead to decrement in the resistances $R_5$ and $R_6$ (see Equation (14)), yielding an appropriate voltage reduction in $V_{\mathrm{d}}$ at the common sources of $M_2$–$M_3$, that compensates the initial current increment. A thorough analysis of Figure 5 reveals that $V_{\mathrm{d}}$ is given in current terms by

$$V_{\mathrm{d}} = \sqrt{\frac{2}{\beta}}\sqrt{(\sqrt{I_2 + m(I_2 + I_1)} - \sqrt{I_2} + \sqrt{I_1})^2 + n(I_1 + I_2)} - \sqrt{I_1} \tag{15}$$

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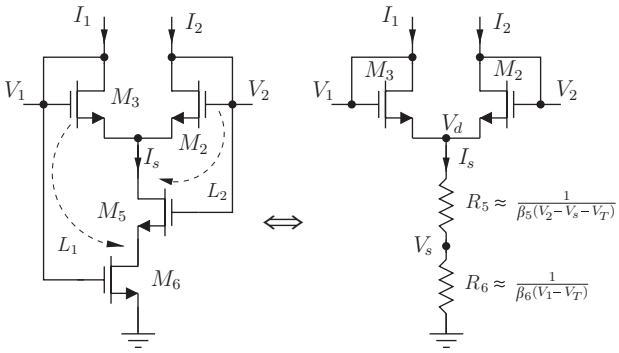


Figure 5. Coupled negative feedback $L_1$ and $L_2$ formed by transistors $M_5$ and $M_6$ acting as resistors.

Table I. Transistor aspect ratios.

| | $M_{1–5}$ | $M_6$ | $M_7$ | $M_8$ | $M_{9–15}$ | $M_{16–18}$ | $M_{19}$ |
|---|---|---|---|---|---|---|---|
| $W$ | 24 | 80 | 240 | 320 | 128 | 64 | 120 |
| $L$ | 4 | 4 | 3.2 | 3.2 | 3.2 | 3.2 | 3.2 |

with $\beta$ the transconductance parameter of the transistors forming the translinear loop, $m$ and $n$ the aspect ratio of transconductance $\beta/\beta_5$ and $\beta/\beta_6$, respectively. To derive Equation (15) the drain currents of $M_5$ and $M_6$ were modelled by the second-order expression $I_d = \beta(V_{\mathrm{GS}} - V_{\mathrm{T}} - V_{\mathrm{DS}}/2)V_{\mathrm{DS}}$. Equation (15) can be employed to calculate the width and length of transistors $M_5$ and $M_6$ to accomplish the condition $V_{\mathrm{d}} \approx V_{\mathrm{DS19}}$. With this alternative biasing scheme the circuit of Figure 4 can operate with a supply voltage as low as $V_{\mathrm{GS}} + 2V_{\mathrm{DS_{sat}}}$. The transistor aspect ratios in Figure 4 are shown in Table I with $m = 1$ and $n = 0.3$.

The TL loop in Figure 4 can operate at such supply voltage ($V_{\mathrm{GS}} + 2V_{\mathrm{DS_{sat}}}$) without the inclusion of floating sources, but they are employed to extend the dynamic range ($V_{\mathrm{B}}$'s) and accuracy ($V_{\mathrm{F}}$). As mentioned in Reference [20], level shifters $V_{\mathrm{B}}$'s allow to increment the voltage swings of TL loop, since the drain voltages of transistors driving the currents at top of TL loop are $V_{\mathrm{B}}$ Volts lower than the gate voltages of TL loop. For instance, transistor $M_{14}$ will be in saturation with

$$V_{\mathrm{DS14}} = V_{\mathrm{GM3}} - V_{\mathrm{B}} - V_{dd} \leqslant V_{\mathrm{GS14}} - V_{\mathrm{T}} \tag{16}$$

Therefore, transistors $M_{11}$, $M_{14}$, $M_{17}$, and $M_{18}$ can drive more gate voltage swings from TL cell, before they enter in their triode region. The level shifters employed in the design were constant with a value $V_{\mathrm{B}} = V_{\mathrm{T}} - V_{\mathrm{DS_{sat}}}$. Level shifter $V_{\mathrm{F}}$ is employed to minimize the channel-length modulation effect over the TL loop [24]. To this end, all the drain voltages of TL loop need to be almost equal [14]. Figure 4 reveals that only the drain $M_1$ needs to be set. Moreover, it can be noted that a constant value for $V_{\mathrm{F}}$ leads to unbalance at the drain voltages of the TL loop. This is demonstrated considering that a current increment in $M_2$–$M_4$ allows a voltage increment at their drains, and also an increment in current $I_{d1} = I_5^2/I_{d2}$. The incremented current $I_{d1}$ is injected to PMOS diode connected transistor $M_{10}$ whose gate voltage decreases at the same time that the drain voltage of $M_1$. To compensate for such a behaviour, a dynamic biasing for $V_{\mathrm{F}}$ is proposed which will be described in the following paragraphs.

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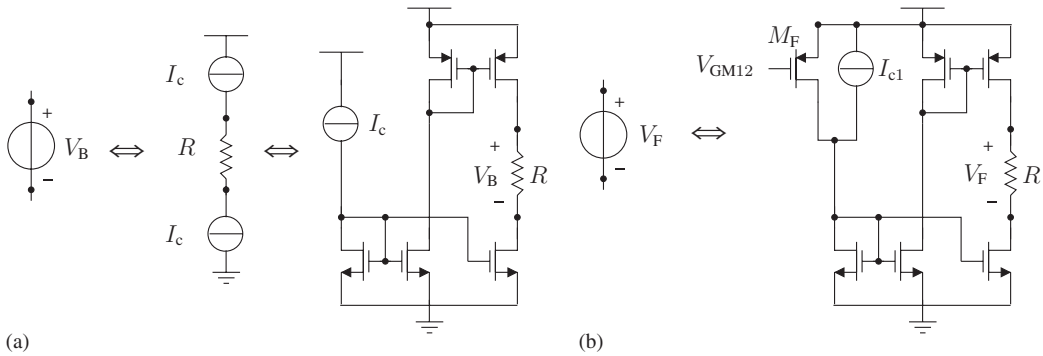


Figure 6. (a) Implementation of $V_B$; and (b) implementation of $V_F$.

The level shifters were implemented via polysilicon resistors and current mirrors [25]. Figure 6(a) shows this approach where the floating source $V_B$ is formed by the connection in series of a current source $I_c$, resistor $R$ and another current source $I_c$. Both current sources $I_c$ can be easily implemented using current mirrors. The floating voltage source is taken from the terminals of resistor $R$, therefore $V_B = R \times I_c$. The control current $I_c$ sets the proper value of the floating source. In our case, it was an external current in order to compensate for fabrication process tolerances of $R$. Note that for correct operation of the floating source a high impedance node with a well defined voltage must be connected at one of its terminals. This means that the floating sources terminals are high-impedance nodes and they cannot drive current. In the design of Figure 4, they are connected at gates of MOS transistors assuring their proper operation. Thus the positive terminal of the floating source $V_B$ is at $V_{GS} + V_{DS_{sat}}$ owing to a gate voltage of a MOS transistor belonging to TL loop is connected at such a terminal. Therefore, the minimum supply voltage to operate the level shifters correctly is $V_{GS} + 2V_{DS_{sat}}$. The transistor aspect ratios employed in the design for the currents mirrors in Figure 6(a) were large $W/L = 80/3$ to maximize the output range.

Regarding $V_F$ a dynamic biasing is required. This can be achieved employing the design shown in Figure 6(b), where the gate of transistor $M_F$ is connected at the gate of transistor $M_{12}$ of Figure 4. The value of $V_F$ is given by

$$V_F = (aI_{d2} + I_{c1})R \tag{17}$$

where the aspect ratio of $M_F$ is $a$ times that of $M_{12}$. In order to keep transistor $M_{10}$ in the saturation region, $V_F$ must be

$$V_F = (aI_{d2} + I_{c1})R < |V_T| \tag{18}$$

Now considering that $R$, $I_{c1}$, and $I_{d2}$ are independent variables, the parameter $a$ can be determined by

$$a < \frac{|V_T|/R - I_{c1}}{I_{d2}} \tag{19}$$

In Equation (19) the current $I_{d2}$ has to be the maximum current in the square/root cell that preserves operation in saturation of transistor $M_{10}$.

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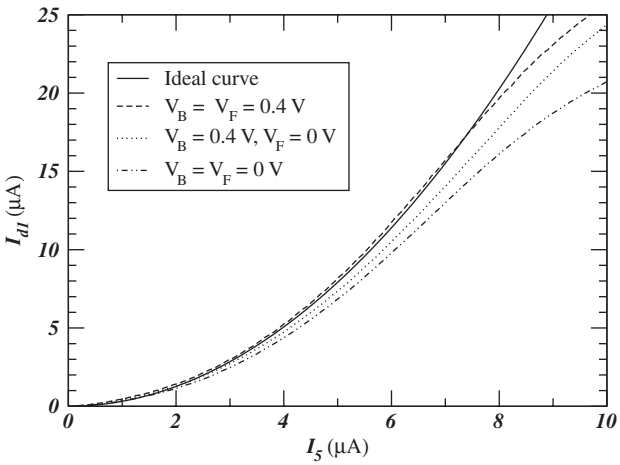


Figure 7. Squarer/divider cell DC operation (measurement results).

Table II. Comparison of the proposed squarer/divider cell and Reference [20].

| | Proposed | In Reference [20] |
|---|---|---|
| Bandwidth (MHz) | 1.48 | 1.21 |
| Power consumption (μW) | 470 | 340 |
| Area ($mm^2$) | 0.055 | 0.050 |

Figure 7 shows measurement results for the squarer/divider cell described in Figure 4 from a prototype fabricated in AMS 0.8 μm CMOS process. The supply voltage was set to 1.5 V thanks to the proper biasing scheme described in Reference [20]. The input current $I_5$ was swept from 0 to 10 μA and $I_{d2} = 3$ μA. As can be observed the cell performs a proper $I$–$I$ characteristic for $V_B = V_F = 0.4$ V demonstrating the suitability of this approach. The value of $V_B$ and $V_F$ were set by the external control currents $I_c$ and $I_{c1}$ of the level shifter implementation in Figure 6, respectively. Resistor $R$ was 50 kΩ and parameter $a = 0.25$ with $W/L = 32/3.2$ for $M_F$.

Table II compares the simulation results in terms of bandwidth, power consumption, and area between the squarer/divider cell proposed here and that proposed in Reference [20]. These results were obtained assuming $I_{d1} = I_{d2} = 10$ μA, $I_{c1} = 4$ μA, and $I_c = 10$ μA for both approaches. As can be observed the three parameters of the cell proposed here are higher than that in Reference [20] representing a 18, 27, and 9% increase, respectively.

In order to design the SRD filter a geometric-mean cell is required. The geometric-mean cell can be easily implemented following the same strategy presented in Reference [20] i.e. changing the input–output impedances of the squarer/divider. The level shifter $V_F$ was not used in this configuration since the channel-length modulation effect can be neglected.

Second-order effects introduced by the level shifters $V_B$ into the TL loop are analysed in Reference [20] and some practical considerations are given to improve the performance of the loop. Such analysis can be easily extended to evaluate the effects of $V_F$ on the loop.

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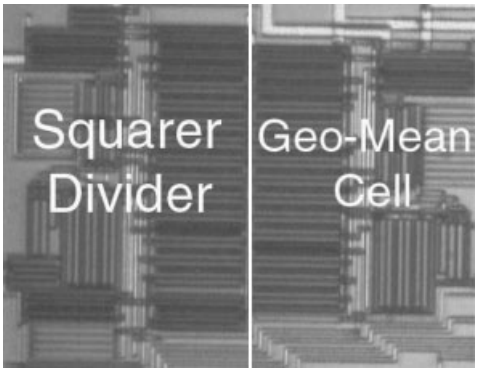


Figure 8. Microphotograph of the squarer/divider and geometric-mean cells.

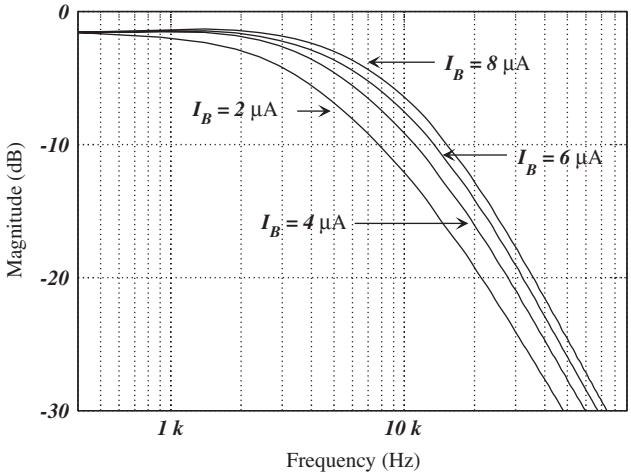


Figure 9. Frequency response of the SRD filter for $I_B = I_{B1} = I_{B2} = 2\,\mu A$, $4\,\mu A$, $6\,\mu A$ and $8\,\mu A$, respectively.

### 2.2. *MOP in the filter*

A prototype of the SRD first-order filter was fabricated as mentioned before in an AMS 0.8 μm DPDM *n*-well CMOS process (see Figure 8), occupying a total area of $0.22\,mm^2$. Both cells, the geometric-mean and the squarer/divider cell, were tested featuring suitability for very low voltage operation ($V_{DD} = 1.5$ V) thanks to the biasing scheme described in Reference [20]. Afterward, the SRD filter was tested with an external capacitor $C = 1$ nF. Measurement results in the time and frequency domains were obtained, offering good agreement with the expected results, see for instance Figure 9. However, sometimes in the tested filter an unintended operating point was established. The selection of the operating point was possible through the initial condition at the capacitance $C$ (see $V_c$ in Figure 1), thereby setting it to ground, the desired operating point was

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selected, on the other hand setting it to $V_{DD}$ another stable equilibrium point was reached. This fact allowed to focus attention on this circuit mode to select the ports to explore MOP and their stability (see the following section for details).

In the simulation process to verify the filter design only the correct operating point was observed. This fact is due to the lack of simulators for detecting MOP. In an attempt to solve this problem several simulators incorporate special numeric methods namely homotopy or continuation to systematically and automatically detect operating points [6]. However, these methods are neither general nor more efficient numerically than those used in SPICE-like simulators. The method used in the simulator (Spectre, a SPICE-like simulator) to assure convergence in DC was source stepping [26] managing to find the correct operating point but not warning about MOP problems. The transistor model was the BSIM3v3, which offers good accuracy for transistors working in strong inversion and saturation region. After observing the MOP behaviour of the SRD filter in the laboratory, initial DC condition at the filter capacitance ($V_c = 1.5$ V) was set in the simulator discovering the second stable operating point. To overcome this drawback, several corrective circuits that eliminate the MOP will be presented in Section 4.

## 3. DETERMINING THE NUMBER OF DC SOLUTIONS

In order to determine the number of operating points in the SRD filter, it is necessary to obtain the static $V$–$I$ characteristics of the circuit by resorting to a DC port analysis [27].

As said before, the tuning of the DC operating point is possible by setting the initial DC conditions at the filter capacitance ($V_c$). Therefore, the ports for this analysis are defined by opening the points $x$, and $y$ in Figure 1, and taking into account that the condition $I_x = I_y$ has to be met. To this end, a DC sweep from 0.85 to 1.5 V was applied at $V_c$ ($I_c = 0$) and the currents at ports $x$ and $y$ were sensed, using $V_{DD} = 1.5$ V, $I_{in} = I_{B1} = I_{B2} = 5$ μA.

From Equation (7), the ideal behaviour of $I_x$ is an inversely proportional function of $V_c$, whereas from Equation (8) $I_y$ establishes a directly proportional dependence on $V_c$.

Figure 10 shows the measurements $I_x$ vs $V_c$ and $I_y$ vs $V_c$ from the fabricated prototype. On one hand, the $I_x$ curve exhibits a saturation current for values below $V_c = 0.9$ V, besides a slope change is also noticed. On the other hand, the $I_y$ curve exhibits a good behaviour for the whole range since it only involves the geometric-mean cell. The circuit exhibits $V$–$I$ characteristics in compliance with Equations (7) and (8), for values between $V_c = 0.9$ and 1.2 V approximately, the operating range of the SRD filter.

The graphic DC solution ($I_x = I_y$) of the SRD filter is also depicted in Figure 10 (the intersections between $I_x$ and $I_y$), where three operating points **A** (the expected one), **B**, and **C** can be appreciated. Notice the $\mathcal{N}$-type curve of $I_x$ from approximately $V_c = 0.9$ to 1.4 V in which its slope changes sign, which leads to the MOP condition [23].

### *3.1. Stability of MOP*

The laboratory tests of the filter give two stable operating points, therefore at least one unstable operating point was expected in compliance with the general result found in Reference [28]. The stability of operating points was tested employing the technique described in Reference [29], i.e. performing a small-signal analysis on the DC linearized equivalent circuit.

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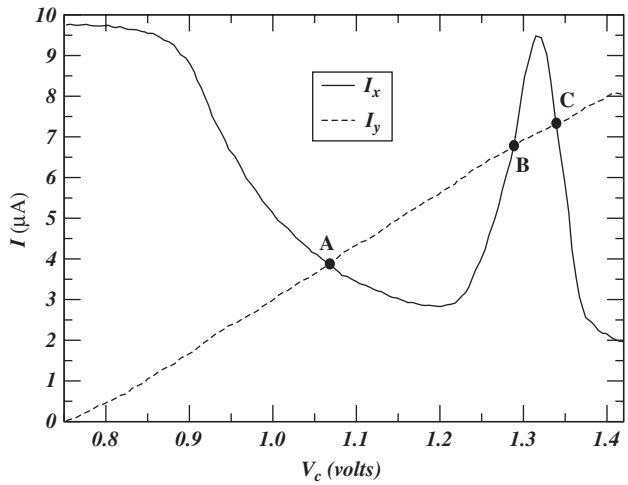


Figure 10. Filter DC solutions (measurement results).

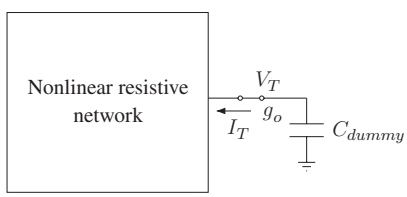


Figure 11. Stability of linearized circuit.

In this scheme, the stability of the DC operating point is related to the stability of an associated dynamical network in the time-domain. Such a dynamical network is the result of adding a dynamical component (capacitor or inductor) to the original static circuit as shown in Figure 11.

The main idea is described in Figure 11, where the box represents the non-linear elements of the circuit, and $C_{\text{dummy}}$ is the extra capacitance added to perform the analysis. The stability of the operating point can be established from the linearized static circuit, that can be modelled as a linear conductance $g_o$ forming together with $C_{\text{dummy}}$ a first-order system. If the linear conductance $g_o$ is positive, the operating point is stable, otherwise the operating point is unstable.

This method shows the advantage that the value of the linear conductance $g_o$ can be easily determined from the voltage-to-current transfer characteristics $V_{\text{T}}$ vs $I_{\text{T}}$.

In our case the node employed to perform the stability analysis is again $V_{\text{T}} = V_{\text{c}}$, where the dummy capacitance can be directly $C = C_{\text{dummy}}$. The current $I_{\text{T}}$ is determined by $I_{\text{T}} = I_y - I_x$. Figure 12 shows the transfer characteristic of $V_{\text{c}}$ vs $I_{\text{T}}$.

The operating points are described by the condition $I_{\text{T}} = I_y - I_x = 0$. Again the three operating points can be identified, but in this case it is possible to determine their stability employing

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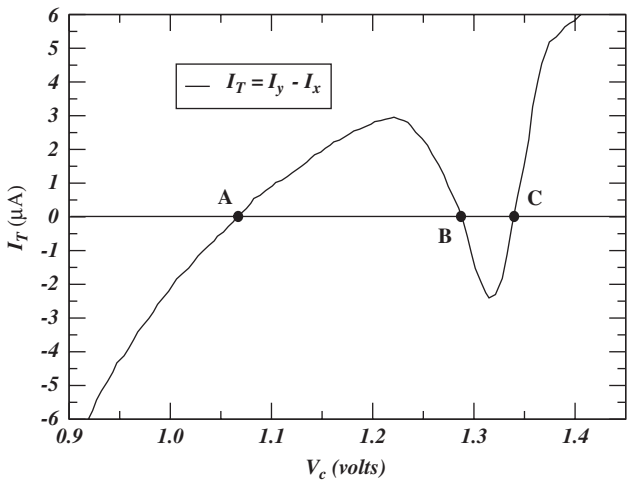


Figure 12. Stability of the MOP.

Figure 12. It clearly results that the points **A** and **C** are stable ($g_o = \mathrm{d}I_\mathrm{T}/\mathrm{d}V_\mathrm{c} > 0$), whereas the point **B** is unstable ($g_o = \mathrm{d}I_\mathrm{T}/\mathrm{d}V_\mathrm{c} < 0$). Therefore the last operating point is unobservable in the practical prototype [28] since any perturbation on it conveys to move it to a stable operating point, either **A** or **C**.

## 4. AVOIDING THE UNINTENDED OPERATING POINTS

In order to assure only one operating point in the SRD filter two procedures can be followed:

(1) To determine the branches and devices that are involved in the cause of MOP in the filter. With this information to plan design strategies for manipulating the topology and/or device parameters to obtain only one operating point maintaining the circuit performance. This approach is the most difficult one due to the lack of formal theory on this issue, being rather heuristic, and very sensitive to fabrication tolerances. Thus proper operation completely relies on the designer's experience.
(2) To add extra circuitry for controlling the MOP. The proposed strategy is shown in Figure 13. Here the corrective circuit senses the internal signals and generates output signals that assure only an operating point. Thus the problem is reduced to control currents and voltages instead of topology and device parameters as in the first approach, providing an elegant solution to the problem. Therefore, this is the approach that will be employed to avoid MOP. The corrective circuit must be as simple as possible to avoid considerable area and power consumption overload. Moreover, the influence of such corrective circuit on the filter needs to be minimized to maintain the performance of the SRD filter.

In Figure 13 the general diagram of proposed corrective circuit to avoid MOP is shown. It is based on an limiter implemented by a negative feedback formed through a comparator and an

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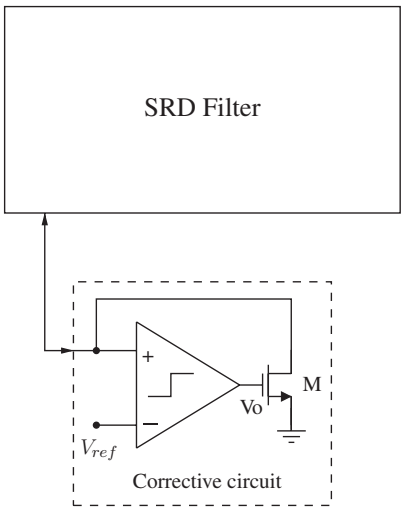


Figure 13. Proposed approach to eliminate MOP.

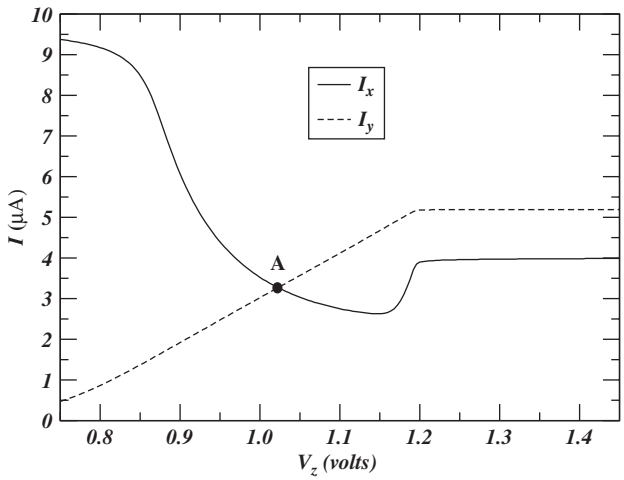


Figure 14. Eliminating MOP employing the scheme of Figure 15.

MOS transistor M. For sensing signals lower than $V_{\text{ref}}$, the transistor M is in cut-off avoiding to close the loop, therefore the corrective circuit does not affect the normal operation of the filter. On the other hand when the sensing signals are higher than $V_{\text{ref}}$ M is turned on and the feedback is formed, keeping the sensing signal equal to $V_{\text{ref}}$ and thus avoiding the other operating points. In our case the voltage at the capacitance $V_{\text{c}}$ of the SRD filter was selected as the sensed signal. Thereby, the SRD filter can be set at the correct operating point (see Figure 14).

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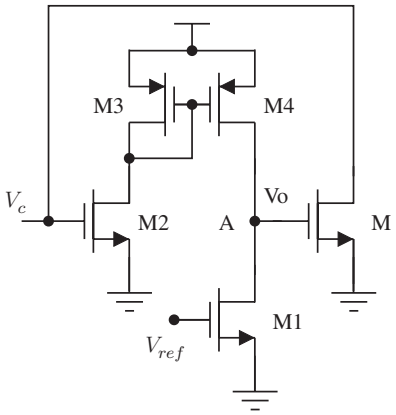


Figure 15. Corrective circuit proposed to avoid MOP.

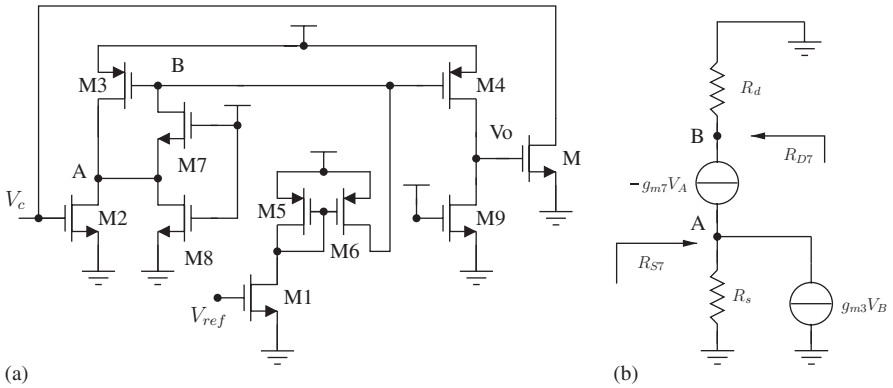


Figure 16. Corrective circuit proposed to avoid MOP with improved bandwidth and gain.

Figure 14 shows the DC characteristics for the currents $I_x$ and $I_y$ of Figure 1 employing the scheme of Figure 13 by means of the circuit of Figure 15. Note that the limiter influence on the SRD filter can be observed for voltages higher than 1.2 V eliminating **B** and **C** from Figure 10. Similar DC characteristics as shown in Figure 14 can be obtained for the other circuits described in Figures 15–17. In the following paragraphs novel corrective circuits capable to operate under very low voltage constraint will be presented. The corrective circuits feature simplicity and reduced die area.

### *4.1. Corrective circuits*

In this subsection novel corrective circuits to avoid MOP in the SRD filter are offered. As a general requirement the corrective circuits need to operate under very low voltage conditions to be compatible with the SRD filter. These circuits are shown in Figures 15–17.

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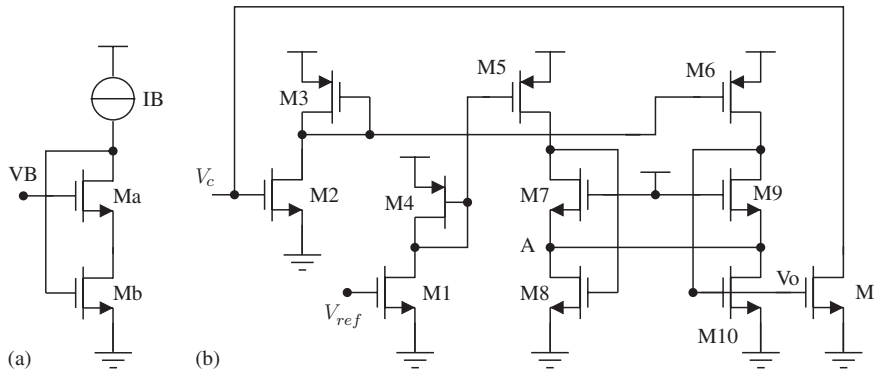


Figure 17. Corrective circuit proposed to avoid MOP based on a winner take all cell.

In the schematics voltage $V_c$ is the voltage at the capacitor of Figure 1 and $V_{ref}$ a reference voltage that can be easily determined making use of Figure 10. In all the circuits for $V_c < V_{ref}$ transistor M is in cut-off avoiding to close the loop, leading to the normal operation of the SRD filter. When a value of $V_c$ is slightly higher than $V_{ref}$ a negative feedback is formed limiting $V_c$ to $V_{ref}$ assuring only the proper operating point.

If the requirements in terms of bandwidth and accuracy are not too high the corrective circuit of Figure 15 can be employed to eliminate MOP. In that circuit transistors M1 = M2, and M3 = M4 form a current mirror. In Figure 15 voltages $V_c$ and $V_{ref}$ are non-linearly converted to currents through M2 and M1, then the drain current of M2 is mirrored to M4. The circuit forces equal drain currents in M1 and M4 thus slewing voltage at the high impedance node $V_o$. Hence the output $V_o$ is swinging between the supply rails depending on the magnitude of the gate voltages M1 and M2, being low for $V_c < V_{ref}$ and high for $V_c > V_{ref}$, so the circuit acts as current comparator. Owing to the poor gain in open loop and high impedance at the node where the current signals comparison is realized, this circuit features an offset at the input (when M is turned on) and limited bandwidth, respectively.

To overcome the restrictions of the circuit in Figure 15 the novel circuit in Figure 16 is proposed. Figure 16(a) shows the transistor circuit whereas Figure 16(b) shows the small signal circuit of transistors M3, M6, M7, and M8. In Figure 16(a) transistors M3 and M7 reduce the node impedance where the current comparison is realized increasing the bandwidth [30], and an extra amplification stage (M4 and M9) reduces the offset at the input in closed loop operation. Transistor M8 is employed to keep M3 operating in strong inversion and saturation region setting the quiescent value at the gate of the amplifier implemented by M4. Here again voltages $V_c$ and $V_{ref}$ are converted to currents by means of M2 and M1, then the drain current of M1 is mirrored to M6 and applied at the low impedance gate of M3. Now the current comparison is performed at the low impedance node labelled A. The negative feedback formed by M3 and M7 leads to low input impedance at the source and drain of M7 (see Figure 16(b)). On one hand, $R_{S7} = 1/(g_{m3} g_{m7} R_d)$ is the input resistance looking at the source of M7, where $R_d$ is the total resistance from the gate of M3 to ground. On the other hand, $R_{D7} = 1/g_{m3} + 1/(g_{m3} g_{m7} R_s)$ is the resistance looking at the drain of M7 where $R_s$ is the total resistance from the drain of M2 to ground. Thus the current comparison is realized at a low impedance node (node A in Figure 16(a)) and reflected at the gate of M3, also a low impedance node [30]. Subsequently this error signal is amplified by M4. The branch that

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sets the minimum supply is that formed by M8, M7 and M3, therefore the circuit is able to operate with supply voltages as low as $V_{GS} + 2V_{DS_{sat}}$ leading to compatibility with the supply voltage of the SRD filter.

Finally the novel circuit proposed in Figure 17 is another alternative to implement the corrective circuit, featuring high speed with high precision. In the circuit it is assumed that M1 = M2, M3 = M4 = M5 = M6, M7 = M9, M8 = M10. Here a useful cell to design circuits with very low voltage, namely 'Flipped Voltage Follower' (FVF) is employed [31] (see Figure 17(a)). A FVF is a voltage follower in a feedback configuration of two transistors and a bias current. Transistors Ma and Mb in Figure 17(a) form one of such a structure and current IB provides the bias current. Here transistor Ma is acting as a voltage follower, and transistor Mb provides a local shunt feedback that allows a very low impedance (on the other of tens of ohms [31]) at the drain of Mb. Assuming that both transistors Ma and Mb are operating in strong inversion and saturation region, the source voltage of Ma defined as $V_{SMa}$ is set by [31]

$$V_{SMa} = VB - \sqrt{\frac{2IB}{\beta}} - V_T \tag{20}$$

where $\beta$ is the transconductance of Ma. Another feature of FVF is that it can sink large currents by keeping almost constant the voltage $V_{SMa}$.

In Figure 17(b) two flipped voltage followers M5, M7–M8 and M6, M9–M10 sharing their very low impedance node (node A in Figure 17(b)) can be identified. Such a connection forms a current-mode winner take all circuit (maximum circuit). The drains of transistors M5 and M6 drive currents involving a quadratic expression in terms of $V_{ref}$ and $V_c$, respectively, i.e.

$$I_{DM5} = \frac{\beta_1}{2}(V_{ref} - V_T)^2, \quad I_{DM6} = \frac{\beta_1}{2}(V_c - V_T)^2 \tag{21}$$

where $\beta_1$ is the transconductance parameter of M1. Thus currents $I_{DM5}$ and $I_{DM6}$ compete for setting the voltage A in Figure 17(b)). On one hand $I_{DM5}$ tries to set at

$$V_A = V_{dd} - \sqrt{\frac{2I_{DM5}}{\beta}} - V_T = V_{dd} - \sqrt{\frac{\beta_1}{\beta}}V_{ref} - V_T\left(1 - \sqrt{\frac{\beta_1}{\beta}}\right) \tag{22}$$

On other hand $I_{DM6}$

$$V_A = V_{dd} - \sqrt{\frac{2I_{DM6}}{\beta}} - V_T = V_{dd} - \sqrt{\frac{\beta_1}{\beta}}V_c - V_T\left(1 - \sqrt{\frac{\beta_1}{\beta}}\right) \tag{23}$$

where $\beta$ is the transconductance parameter of M7. The voltage that will win is the lower one i.e. higher current $I_{DM6}$ or $I_{DM5}$ [32]. In such a configuration only one transistor M8 or M10 can be on. Thus if $I_{DM6} > I_{DM5}$[‡] ($I_{DM6} < I_{DM5}$) M10 will be on (off), M8 off (on), and M9 (M7) in the triode region, owing to the very low impedance at source of M7 (M9), the current that flows through M10 (M8) is $I_{DM6} + I_{DM5}$. By connecting the gate of M to gate of M10 the circuit performs the functionality required. This cell is able to operate with supply voltage as low as $V_{GS} + V_{DS_{sat}}$

[‡] $I_{DM6} > I_{DM5} \Rightarrow V_c > V_{ref}$

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Table III. Comparison of the proposed corrective circuits.

| Circuit | Delay (ns) | DC gain (dB) | Bandwidth (MHz) | Power (μW) | Area (μm$^2$) |
|---|---|---|---|---|---|
| Figure 15 | 38 | 23 | 70 | 30 | 105 |
| Figure 16 | 22 | 30 | 148 | 60 | 210 |
| Figure 17 | 3 | 16 | 180 | 45 | 240 |

(see transistors that form the branch by M5, M7, and M8) being completely compatible with the SRD filter.

Table III shows a performance comparison among the comparators employed in the proposed corrective circuits. The delay was estimated employing a square signal at 50 MHz with an amplitude from 0 to 1.5 V. The voltage $V_{\text{ref}}$ was set to 0.9 V. The bandwidth described in Table III is unity-gain bandwidth. The power consumption was evaluated when the loop was closed. The aspect ratios for all transistors were $W/L = 10\mu/0.8\mu$. The proposed circuit of Figure 16 increases the bandwidth and DC gain from the circuit of Figure 15 as expected, however these benefits require larger chip areas and power consumption. Finally the circuit in Figure 17 is the fastest one at the expense of a larger chip area, less DC gain and power consumption regarding the circuit in Figure 16. All the circuits can operate with very low supply voltage and can be readily employed in other applications.

### *4.2. Second-order effects*

The extra circuitry added to avoid MOP loads the SRD filter modifying its bandwidth, power consumption, and THD. Thus an analysis is required in order to evaluate such behaviour and minimize the influence of the corrective circuits on the filter performance.

According to Figures 15–17 the second-order effects of the corrective circuits on the SRD filter can be modelled by a capacitance and resistance in parallel connected from $V_{\text{c}}$ to ground. The capacitance is mainly due to the gate capacitance of M2 and the resistance by the drain-source resistance of M.

The capacitance effect can be easily reduced choosing smaller dimensions for transistor M2 in the corrective circuits with respect to $C$ and parasitic $C_{\text{GS}}$ of $M_1$–$M_3$ of the SRD filter (see Figure 1). Thereby the capacitance contributions by the corrective circuits can be neglected.

Regarding the resistance, it could contribute to increase significantly the filter distortion. This is due to the fact that resistance $R_M$ (the resistance from drain to source of M) introduces new terms in Equation (4) that degrade the filter linearity [18, 20]. To provide more insight and evaluate its impact consider that $R_M$ is linear, thus Equation (4) is modified as follows:

$$C\dot{V}_{\text{c}} = \sqrt{\frac{2I_{B2}}{\beta}}\,\frac{I_{\text{in}}}{(V_{\text{c}} - V_{\text{T}})} - \sqrt{\frac{\beta I_{B1}}{2}}\,(V_{\text{c}} - V_{\text{T}}) - \frac{V_{\text{c}}}{R_M} \tag{24}$$

employing Equation (2) to translate the companding filter to the equivalent linear one, it is found that:

$$\tau\dot{I}_{\text{out}} + I_{\text{out}} = kI_{\text{in}} - \frac{2}{\sqrt{2\beta I_{B1}}}\,\frac{I_{\text{out}}}{R_M} - \frac{V_{\text{T}}}{\sqrt{I_{B1}}}\,\frac{\sqrt{I_{\text{out}}}}{R_M} \tag{25}$$

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As can be observed extra terms are added to linear behaviour. On one hand a linear term dependent non-linearly on $I_{B1}$ modifies the cut-off frequency of the filter. On the other hand a strong non-linear term of $I_{\text{out}}$ is involved that could degrade linearity of the filter. However the $R_M$ values in the operation of the SRD filter are high enough (in the order of Giga Ohms) since M is off and the loop is open. Therefore the influence of these terms can be neglected. Thus it is demonstrated that the corrective circuits avoid MOP and the impact of such circuits on the filter performance can be made negligible.

## 5. CONCLUSIONS

A SRD first-order filter with multiple operating points was presented. The basic building blocks were based on voltage translinear loops and level shifters leading to a very low voltage operation (as low as $V_{\text{GS}} + 2V_{\text{DS}_{\text{sat}}}$). A prototype with 1.5 V supply voltage and three operating points was investigated. Several novel corrective circuits were proposed and validated through simulation results to eliminate the multiple operating points in the filter. Finally, the effects of these corrective circuits over the filter performance were analysed demonstrating their robustness and proper operation. The technique proposed here can be readily extended to avoid MOP on other systems that offers this unwanted behaviour in continuous time designs.

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