International Journal of Electronics

ISSN: 0020-7217 (Print) 1362-3060 (Online) Journal homepage: http://www.tandfonline.com/loi/tetn20

Designing SRCOs by combining SPICE and Verilog-A

E. Tlelo-Cuautle , M.-A. Duarte-Villaseñor , J.-M. García-Ortega & C. Sánchez-López

To cite this article: E. Tlelo-Cuautle , M.-A. Duarte-Villaseñor , J.-M. García-Ortega & C. Sánchez-López (2007) Designing SRCOs by combining SPICE and Verilog-A, International Journal of Electronics, 94:4, 373-379, DOI: 10.1080/00207210701294940

To link to this article: https://doi.org/10.1080/00207210701294940

International Journal of Electronics,
Vol. 94, No. 4, April 2007, 373–379

Taylor & Francis
Taylor & Francis Group

Designing SRCOs by combining SPICE and Verilog-A

E. TLELO-CUAUTLE*†, M.-A. DUARTE-VILLASEÑOR†,
J.-M. GARCÍA-ORTEGA† and C. SÁNCHEZ-LÓPEZ‡

†INAOE – Department of Electronics, Luis Enrique Erro No. 1,
Tonantzintla, Puebla, 72000, Mexico
‡UAT – Department of Electronics, San Luis Apizaquito s/n,
Tlaxcala, 72000, Mexico

(*Received 8 June 2006; in final form 20 February 2007*)

The design of single-resistance-controlled oscillators (SRCOs) is presented by using current followers (CF) and voltage followers (VF). First, the design of the followers is described by using SPICE and standard CMOS technology of 0.35 μm. Second, a SRCO is simulated in SPICE by using the designed CF and VF. Third, the SRCO is simulated in Verilog-A by using ideal and real behavioural models for the followers. Finally, the good agreement on the simulation results leads us to conclude on the usefulness to combine SPICE and Verilog-A to enhance analogue integrated circuit design.

Keywords: Modelling and simulation; Single-resistance-controlled oscillator; Current and voltage follower; Analogue integrated circuit design

1. Introduction

Nowadays, the development of personal wireless communication systems imposes the trend to integrate the radiofrequency front-ends, analogue-to-digital converters and based-band digital signal processors in a single chip. Furthermore, oscillators are critical components of electronic systems since they provide time or frequency reference for the whole chip. In this manner, novel methods have been proposed to design sinusoidal oscillators (Gu *et al*. 2005, Martínez and Monge 2005, Gupta and Senani 2006). Martínez and Monge (2005) proposed the synthesis of variable frequency single-resistance-controlled oscillators (SRCOs), which can be implemented with various active elements chosen in order to achieve some given characteristics required for the whole electronic structure. Gupta and Senani (2006) use current followers (CF) and voltage followers (VF), which have advantages of wider bandwidth and low power consumption compared to other more complex active devices. They derived a state-variable synthesis approach for SRCOs requiring a much smaller number (only two to four) of followers. On the other hand, since systems based on oscillators are inefficient to simulate using traditional methods, e.g., SPICE. Gu *et al*. (2005) proposed a macromodelling approach by using the Verilog language to speed up circuit simulations.

*Corresponding author. Email: e.tlelo@ieee.org

International Journal of Electronics
ISSN 0020–7217 print/ISSN 1362–3060 online © 2007 Taylor & Francis
http://www.tandf.co.uk/journals
DOI: 10.1080/00207210701294940

Henceforth, this paper is devoted to showing a design approach for SRCOs by modelling the behaviour of the followers at a level of abstraction higher than the transistor one by Verilog-A. In this manner, in § 2 is described the design of the CF and VF from the preliminary results given in Souliotis *et al*. (2001) and Tlelo-Cuautle *et al*. (2005). The analogue blocks are sized with standard CMOS technology of 0.35 μm and simulated by SPICE. In § 3, a SRCO is designed at the transistor level of abstraction by using the designed followers. In § 4, the SRCO is simulated by using ideal and real behavioural models for the CF and VF within Verilog (Kundert and Zinke 2004), a language provided in FitzPatrick and Miller (1998). Finally, the conclusions are summarized in § 5.

2. Designing CFs and VFs

Analogue circuit synthesis is devoted to explore or to search for all circuit topologies to accomplish desired target specifications. Besides, the generation and selection of topologies can be solved by beginning from the most abstract description of analogue blocks, as shown in Tlelo-Cuautle *et al*. (2005). On the other hand, as described in Gupta and Senani (2006), the behavioural description of the CF has two derivations: the CF+ and the CF−. The former can be implemented as shown in figure 1(a), and the latter in figure 1(b). As one sees, the CF+ is basically a current mirror (CM), while the CF− can be designed by cascading two CMs, as highlighted in Souliotis *et al*. (2001). The VF can be implemented as shown in figure 2. An important thing is that these followers are simpler than the ones used in Gupta and Senani (2006).

For instance, by using standard CMOS technology of 0.35 μm, the aspect ratios of all MOSFETs in figure 1(a, b) are $W = 40\,\mu m$ and $L = 1\,\mu m$. The aspect ratios of all MOSFETs in figure 2 are $W = 20\,\mu m$ and $L = 1\,\mu m$, however, M5 and M6 should be sized to $W = 40\,\mu m$, as for the CFs. The bias levels are $\pm 1.5\,V$ and $Iref = 20\,\mu A$. SPICE simulation results show that the CF+ has a gain = 0.9999 with a

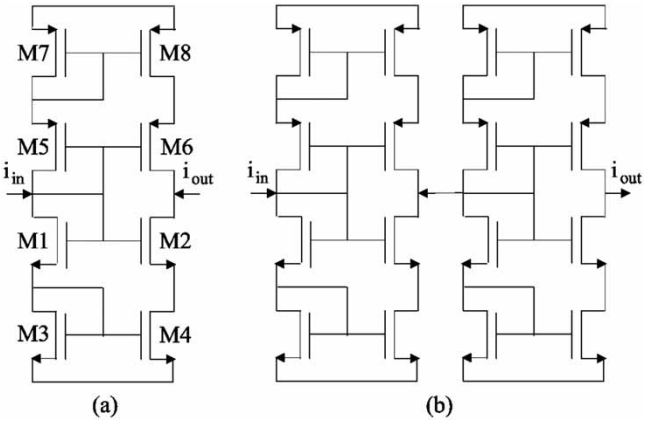

Figure 1. Circuit descriptions of (a) CF+ taken from Souliotis *et al*. (2001) and (b) CF−.

bandwidth = 319.85 MHz, while the VF has a gain = 0.9921 with a bandwidth = 421.75 MHz.

3. Design of a SRCO at the transistor level

By using the CMOS compatible followers designed in § 2 to design the SRCO shown in figure 3, by setting R1 = 38 k, R2 = R3 = 47 k, C1 = C2 = 10p, and with the initial conditions across C1 and C2 as v(1) = 0.1 and v(2) = 0.1, respectively, the resulting SPICE simulation is shown in figure 4. Although the condition of oscillation derived in Gupta and Senani (2006) must accomplish that R1 = R3, in the physical implementation R1 < R3 since one should consider the parasitic resistances and capacitances embedded into the followers. In this manner, R1 was adjusted to 38 k to generate the desired oscillation.

4. Simulation of a SRCO by Verilog-A

Traditional simulation methods in SPICE-like simulators often consume significant CPU time to simulate the transient behaviour of oscillating systems, since small time steps and many simulation cycles are required. To cope with this problem,

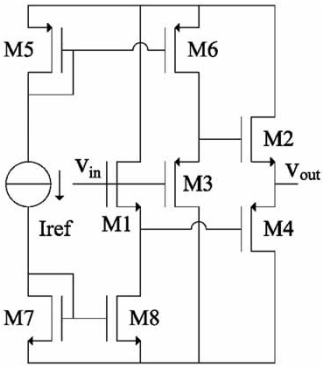

Figure 2. Circuit description of VF taken from Tlelo-Cuautle *et al.* (2005).

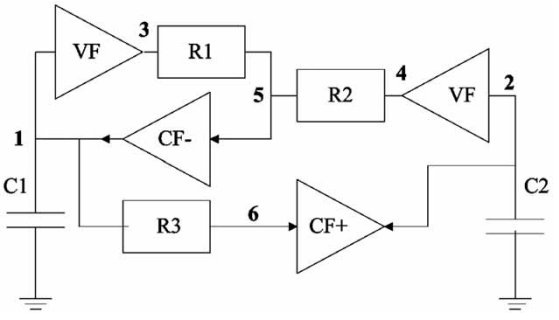

Figure 3. Second order SRCO taken from Gupta and Senani (2006).

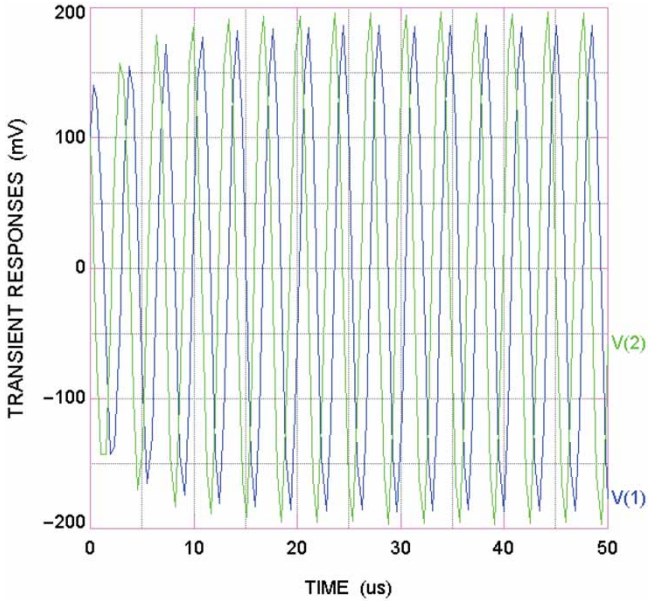

Figure 4. SPICE simulation of the SRCO shown in figure 3, designed with the followers from § 2.

```
`include "std.va"
`include "const.va"

module vf(out, in);
inout out, in;
electrical out, in;
parameter real gain=0.9921;
parameter real pole=6.24*421e6;
analog begin
V(out) <+ laplace_nd(V(in),{gain*pole},{pole,1});
end
endmodule

module cfp(out, in);
inout out, in;
electrical out, in;
parameter real gain=0.9999;
parameter real pole=6.24*319e6;
analog begin
I(out) <+ laplace_nd(I(in),{gain*pole},{pole,1});
end
endmodule
```

Figure 5. Behavioural descriptions of the VF (module vf) and CF+ (module cfp) by Verilog-A.

behavioural modelling strategies can be applied to speed up circuit simulations and facilitate system–level simulations (Gu *et al*. 2005). In this manner, the behavioural models for the CF+ and the VF shown in figures 1 and 2 can be approximated from their SPICE simulation results. In figure 5, the description of the frequency behaviour for the CF+ and VF designed in § 2 is shown. As one sees, each follower is modelled by considering its finite gain and finite bandwidth.

```
.verilog "realVFCF.va"
X1 4 2 vf
X2 3 1 vf
X3 2 6 cfp
X4 1 7 cfp
X5 7 5 cfp
R1 3 5 46.75k
R2 4 5 47k
R3 6 1 47k
C1 1 0 10p
C2 2 0 10p
.ic v(1)=0.1
.ic v(2)=0.1
.tran .01u  50u
.op
.end
```

Figure 6. Description of the SRCO by using the models from figure 5.

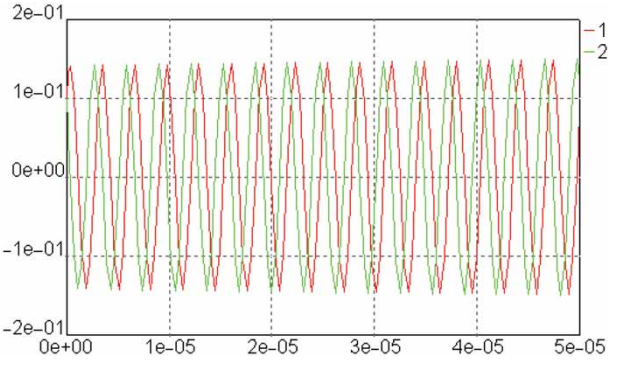

Figure 7. Verilog-A simulation result from the description shown by figure 6.

By using figure 5, the description of the SRCO from figure 3 at a high level of abstraction, is shown in figure 6. The Verilog-A simulation result is shown in figure 7. Note that now R1 was adjusted to 46.75 k to generate the desired oscillation. Furthermore, the Verilog-A language allows the description of electronic systems with varying amounts of detail, i.e. a system can be described and simulated at a high level of abstraction early in the design cycle to facilitate architectural trade-offs (Kundert and Zinke 2004). That way, by describing the ideal behaviour of the VF and CF+ by $V(\text{out}) <+ V(\text{in})$ and $I(\text{out}) <+ I(\text{in})$, respectively, the Verilog-A simulation result is shown in figure 8. For this ideal simulation, the condition of oscillation must be accomplished, i.e. $R1 = R3 = 47\,\text{k}$, otherwise the system does not oscillate.

5. Conclusion

It has been introduced the simulation of SRCOs from the design of CMOS compatible CFs and VFs by SPICE, to its behavioural modelling by Verilog-A.

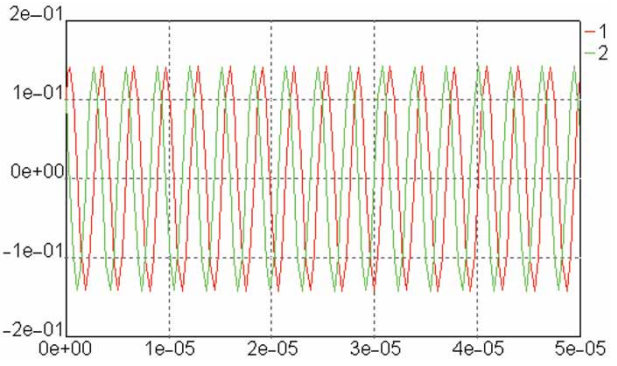

Figure 8. Verilog-A simulation result by using ideal descriptions for the followers.

As a result, the condition of oscillation for the SRCO was tuned by adjusting the value of R1. In this manner, in the ideal case $R1 = R3$ to accomplish the condition of oscillation. Further, when the followers were modelled by Laplace in Verilog-A, R1 was diminished to 46.75 k to generate the oscillation behaviour due to the fact that neither the gain $= 1$ nor the bandwidth $= \infty$. Also, when the followers were designed at the transistor level, R1 was adjusted to 38 k to generate the oscillation behaviour because the introduction of parasitic resistances and capacitances.

As a conclusion, from the good agreement on the simulation results between SPICE and Verilog-A, one can conclude on the usefulness and suitability to combine them to adopt a top-down approach to enhance analogue integrated circuit design. That is, Verilog-A can be used to describe a system at a high level of abstraction before converting the modules to the transistor level implementation. Further, a refinement process can be performed to design the modules down to the transistor level, e.g. by using standard CMOS technology. The main advantage is the speeding up in time simulation along with the verification of the first cut of design before its physical implementation.

Acknowledgment

This work has been partially supported by CONACyT/MEXICO with the project number 48396-Y.

References

D. FitzPatrick and I. Miller, *Analog behavioral Modeling with the Verilog-A Language*, Massachusetts, USA: Kluwer Academic Publishers, 1998.

B. Gu, K.K. Gullapalli, S. Hamm, B. Mulvaney, X. Lai and J. Roychowdhury, ''Implementing nonlinear oscillator macromodels using Verilog-AMS for accurate prediction of injection locking behaviors of oscillators'', in *IEEE BMAS*, 2005, pp. 43–47.

S.S. Gupta and R. Senani, ''New single-resistance-controlled oscillator configurations using unity-gain cells'', *Analog Integrated Circuits and Signal Processing*, 46, pp. 111–119, 2006.

K.S. Kundert and O. Zinke, *The Designer's Guide to Verilog AMS*, Boston: Kluwer Academic Publishers, 2004.

P.A. Martínez and B.M. Monge, "Generation of two integrator loop variable frequency sinusoidal oscillator", *Int. J. Elect.*, 92, pp. 619–629, 2005.
G. Souliotis, A. Chrisanthopoulos and I. Haritantis, "Current differential amplifiers: new circuits and applications", *Int. J. Circ. Theory Appl.*, 29, pp. 553–574, 2001.
E. Tlelo-Cuautle, D. Torres-Muñoz and L. Torres-Papaqui, "On the computational synthesis of CMOS voltage followers", *IEICE Trans. Fundam. Elect., Commun. Comp. Sci.*, E88-A-12, pp. 3479–3484, 2005.